HP EEsof Design Solutions

HP RF and Microwave Design System

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Feature Enhancements and Corrections 1

Introduction

MDS 7.1 incorporates a number of enhancements, including a variety of new example files for Circuit Envelope and the UCSD HBT model. For descriptions of these and other enhancements, refer to the section "Enhancements", below.

A number of defects have also been found and corrected. Many of the corrections were distributed in patches following the release of MDS 7.0. MDS 7.1 combines these corrections, and some additional ones, into a single update. For more information, refer to "Corrections to MDS 7.0" on page 1-8.

Enhancements

Enhancements have been made to MDS models, simulation examples, libraries, the SPICE netlist translator, HP Momentum, and the IFF translator. Descriptions are given in the following sections.

Examples

Circuit Envelope Phase-locked Loop Examples

Five examples that illustrate the baseband phase-frequency detector (PFD) model have been added to the `Envelope` file. They are in the workbench `Envelope/Feedback_loops_env/PLL_TIS`. Brief descriptions of these simulation examples follow.

`PLL_wBaseband_PFD` simulates the transient response of a PLL using a baseband phase-frequency detector behavioral model and current sources to act like a charge-pump PFD.

`PLL_wTuned_PFD` simulates the transient response of a PLL using a tuned PFD model, which behaves more ideally and simulates faster.

`Ref_feedthru` simulates reference signal feedthrough that appears as sidebands at the output of the VCO. Mismatches are added to the PFD to generate the undesired feedthrough.

`Stepped_CP_current` illustrates how the charge-pump current amplitude may be changed during the transient response in order to achieve a faster lock time.

`Stepped_LPF_BW` illustrates how a resistor can be switched to alter low-pass filter bandwidth in order to achieve a slightly faster lock time.

New FSK Sources

Two simple frequency-shift keying (FSK) source examples have been added to the `Envelope/Subsystem_env` example. They illustrate how easy it is to generate pseudo-random 2- or 4-level FSK signals with Circuit Envelope.

Cartesian Feedback Amplifier Example

An example file of cartesian feedback amplifier is included in MDS 7.1.

To insert the file onto the blue screen:

1. From the SUI choose `Browse/Open`.
2. Under `Viewing Environment` choose `UNIX System`.
3. Click `Browsing Options...` and under `UNIX System` choose `Examples`.
4. Click `OK`.
5. Choose `CartesianFB` from the list of files then click `Apply`.

A brief description of cartesian feedback amplifiers and descriptions of the simulation examples follow.

Cartesian feedback amplifiers are used to generate high output power signals with low adjacent-channel power ratios (ACPR). This is accomplished by coupling off part of the amplifier output signal, demodulating it, and using the demodulated signal to pre-distort the input baseband I and Q signals via a comparator/filter circuit. In more detail, the demodulated I and Q signals at the output of the power amplifier are fed back to the summing input of the comparator/filter circuit, after a 180 degree phase shift. The comparator/filter circuit will predistort its output to maintain a virtual ground at the comparator summing node. This will occur if both inputs to the comparator/filter circuit are in phase when the loop is open. When the loop is closed, the inputs to the

comparator/filter circuit will be equal but in opposite phase. (Compare the I and Q waveforms in `TimeSignalsFBoff` and `TimeSignalsFBon`.)

To achieve loop stability, a low pass filter (part of the comparator/filter circuit) is used to limit the loop bandwidth. The cutoff frequency must be sufficiently wider than the bandwidth spread due to the amplifier nonlinearity. This limits the upper modulation bandwidth but is sufficient for mobile purposes. Linearity is limited by two factors: the loop gain and the accuracy of the feedback path. The loop gain has to be as large as possible but is limited by the loop stability which is closely dependent on the phase response.

Adjustment of the phase shifter is critical. With the loop opened, the phase should be adjusted so that there is no phase rotation of the demodulated I and Q signals with respect to the input I and Q signals to the comparator/filter circuit.

`ComparatorTest` is a simple test to verify that the comparator/filter is working properly.

`ComparatorFresp` simulates the comparator/filter's frequency response.

`IMDtest` has two simulations of the cartesian feedback amplifier, one with the feedback applied and one without it. In these cases, the baseband I and Q signals are sinusoids that are in phase.

`AmplifierTest` simulates the large-signal S-parameters of the amplifier as a function of input signal power level.

`CartesianFBoff` simulates the output power and ACPR of the amplifier without the feedback applied.

`CartesianFBon` simulates the output power and ACPR of the amplifier with the feedback applied. There is about a 1 dB improvement in ACPR for the same output level. Someone more familiar with cartesian feedback design should be able to adjust the circuit parameters and achieve better performance.

`BBdataGeneration` shows how the baseband, filtered I and Q data is generated. This data corresponds to the NADC format, and is pi/4 DQPSK modulation.

New RFIC IQ Modulator Examples

The IQmodulator example file shows a variety of simulations that are useful when designing an RFIC IQ modulator. The objective is to show the various simulator capabilities, as well as how to set up and run various simulations efficiently. The time has not been taken to extensively optimize this design to

reduce power consumption, minimize bias voltages, and so on, although the various simulation set-ups could be used to improve the design. Also, bias circuitry has not been included.

The design is a direct-conversion IQ modulator. A 960 MHz LO signal is directly modulated by baseband I and Q data signals. The modulator consists of a mixer, a combiner, a buffer (which also converts a differential-mode signal into a single-ended signal), and a power amplifier. A 90-degree phase shifter has not been included, although one could be created using an RC-CR network and the `DE_SO` circuit (in the `SingEnd_to_Diff` workbench) to generate two differential-mode LO signals that are 90 degrees out of phase.

A number of different simulations have been run on each of the different parts of the modulator, as well as simulations on the entire modulator. This example illustrates that, rather than designing and simulating the modulator as an entire unit, the design can easily be improved by simulating one part of the modulator at a time. For example, if the adjacent-channel power ratio at the output is too high, how would a designer determine which part of the modulator is causing the most distortion? By breaking the modulator into pieces, it becomes much easier to determine the origin of the distortion.

The `PA_Buffer_Comb_Mix workbench` combines the four stages together, and includes simulations with modulated signals, to generate adjacent-channel power ratio and error vector magnitude results.

For instructions on how to insert a file, refer to “Cartesian Feedback Amplifier Example” on page 1-2.

Updated 16 QAM Modem Example

The 16 QAM modem example, `digital_comm/QAM16_MODEM`, has been updated to include ACPR and error-vector magnitude (EVM) simulations. This example was originally created using harmonic balance to simulate a modulator/demodulator with a pseudo-random bit sequence. This simulation can now be performed with Circuit Envelope. It simulates more accurately (because more harmonics may be simulated) using significantly less memory (because the baseband data signals are defined in the time-domain rather than having to use a large-signal tone), and with longer, more realistic bit sequences.

Updated PI4QPSK Modem Example

The Pi4QPSK modem example, `digital_comm/PI4QPSK_MODEM`, has been updated to run with Circuit Envelope. ACPR and EVM calculations have been added, and a longer, more realistic bit sequence can now be simulated.

Updated QPSK Transceiver Example

The `digital_comm/QPSK_TRANSCEIVER` example has also been updated to run with Circuit Envelope. In this example, too, ACPR and EVM calculations have been added, and a longer, more realistic bit sequence can now be simulated.

New Oscillator Example

A new oscillator example can be found in the oscillators example file `oscillators/RFIC_osc`. It is a 25-BJT RFIC oscillator that generates an approximately triangular wave at about 375 MHz. This example includes a simulation to determine the best value of `OSCTEST` impedance, harmonic balance simulation, phase noise simulation, and transient simulation for comparison with the harmonic balance result.

New Momentum Example

A silicon substrate example has been added to the `Mom_examples` file.

HBT Model Example

An SDD implementation of the University of California at San Diego heterojunction bipolar transistor (HBT) model has been added to MDS (see “HBT Model” on page 1-7). An example using this model can be found in the miscellaneous file `miscellaneous/HBT_example`. This example has a DC I-V curve simulation of the NPNHBT device. A sample HBT device with model parameters is also included.

New Circuit Envelope Training File

A Circuit Envelope training file is included in MDS 7.1 and may be inserted onto the blue screen.

1. From the SUI choose `Browse/Open`.
2. Under `Viewing Environment` choose `UNIX System`.
3. Click `Browsing Options...` and under `UNIX System` choose `Examples`.

4. Click `OK`.
5. Choose `CEtraining` from the list of files then click `Apply`.

Brief descriptions of these simulation examples follow.

Note This example file requires approximately 38 Mbytes of disk space.

`AmpMultiChannel` shows the degradation to a pi/4 DQPSK signal passing through an amplifier with similar, modulated signals on the upper and lower adjacent channels.

`MixerIMDsweep` shows a mixer's intermodulation distortion versus bias voltage sweep.

`AmpParamSweep` shows an amplifier's adjacent-channel power ratio (ACPR), output power, and error vector magnitude (EVM), as a function of the bias voltage.

`QAM` shows the generation of a 16-QAM signal with a diamond-shaped constellation, and the simulation of the EVM and ACPR caused by an amplifier. The constellation and eye diagrams are also plotted.

`MixerMultiTone` shows the intermodulation distortion generated by a mixer when a multi-tone input signal is used.

`DoubleDownConv` shows the intermodulation distortion generated by a double-converting mixer chain.

Circuit Envelope Presentation Available

Presentation and text files from a technical information session covering the details of the Circuit Envelope phase-locked loop examples, and a video showing an HP EEsof applications engineer giving this presentation, are available. The presentation focuses primarily on the baseband phase-frequency detector behavioral model, which models charge-pump PFDs commonly used with modern PLLs. For more information on obtaining these materials, contact your HP EEsof field representative.

Models and Simulators

New simulator examples and model enhancements are described below.

HBT Model

A version of the UCSD HBT model is now included in MDS. It is available as an SDD and can be found in the library file `NPNHBT`. The menu path is `INSERT/MDS COMPONENTS/NONLINEAR DEVICES/HBT/NPNHBT`. Details about the model can be found at `http://hbt.ucsd.edu` and in Chapter 2, Documentation Additions, Notes, and Corrections.

BSIM3 Model

A multiple device option, `M`, has been added to the BSIM 3 model. The `M` parameter simulates multiple parallel devices. MOSFET channel width, diode leakage, capacitors, and resistors are affected. The default is `1.0`.

SPICE Netlist Translator

Several MOSFET model parameters are now supported: `pdiblc1`, `pdiblc2`, and `M`. Also, the default values for `NRD` and `NRS` are set according to the SPICE simulator used: HSpice, HPSpice, PSpice, or Berkeley Spice.

Instrument I/O

Instrument I/O filesets that are compatible with HP-UX 10.2 are included with this release. For installation instructions refer to "System Administration and Customization" on page 2-2 in this manual and "Installing HP SICL" in Chapter 14 of *System Administration and Customization*.

The NEC parts library has been updated to NEC version 11.1. Over 800 sets of S-parameters and more than 40 non-linear models are available. NEC devices are located in the file `MDSLIB3`.

HP Momentum

2GB swap space is now standard for HP Momentum, improving simulation of complex designs.

IFF Translator

It is possible to use Cadence components in MDS simulations after an IFF transfer from Cadence to MDS. For details, consult Appendix B of the CAE Framework Communication User's Guide.

Corrections to MDS 7.0

The following corrections are included in MDS 7.1. Some were also previously included in MDS patches 7.01 - 7.08.

Examples and Libraries

Changes were made to `mwlib` to correct erratic pin snapping behavior.

The Circuit Envelope amplifier example file for the IBM platform was incorrect and has been modified.

The Circuit Envelope and mixer example files have been modified to eliminate warning messages.

A defect in the database update program caused some layout icons in example and library files to be translated incorrectly. When these icons were accessed they would generate a warning that they may corrupt the database. Although there was no problem with the icons, the examples and library files have been corrected.

Documentation

Online documentation from the blue screen `HELP` button has been improved to describe how to print an entire manual.

The English online documentation for the IBIS models has been changed to reflect the support of IBIS 2.1.

An error where some pull-down menu items would bring up `HELP` instead of the desired action has been corrected.

For other documentation corrections refer to Chapter 2, Documentation Additions, Notes, and Corrections.

Models and Simulators

Phase Noise Simulation Changes

Phase noise changes have been made with this release. A discussion on these changes is given below.

Phase Noise Theory Phase noise in an oscillator can be analyzed from two separate, independent viewpoints: FM noise and mixing noise. FM noise may be viewed as the oscillator acting as a VCO and changing its operating frequency due to FM modulation caused by noise generated in the oscillator. Mixing noise comes from the nonlinear behavior of the oscillator, where noise mixes with the oscillator signal and harmonics to sideband frequencies on either side of the oscillator signal. These two viewpoints are two different ways of looking at the same problem. There should be a region of offset frequencies where mixing noise and FM noise produce the same phase noise results.

FM noise is obtained from the large-signal (harmonic balance) oscillator solution. The sensitivity of the oscillation frequency ω_o is obtained with respect to any injected noise in the circuit. After summing over all of the noise sources, the total spectral density of frequency fluctuations is obtained and converted to phase noise. This noise has a characteristic shape of f^{-2} (or f^{-3} if $1/f$ noise sources are present). This description is valid at small offset frequencies, but is no good at large offsets as it goes to zero; it will not exhibit a noise floor. The MDS model for FM noise is based on a sensitivity analysis of the oscillator frequency due to perturbations from noise, evaluated at DC. This model may not predict phase noise well if there are low-pass filters in the circuit (for example, power supply decoupling) that tend to filter out noise.

To model oscillator phase noise due to mixing, the noise at the sidebands on either side of the carrier ($\omega_0 \pm \omega$) are obtained from a small signal mixer analysis where noise sources ($\omega \pm k\omega_0$) mix with the oscillator large signals ($k\omega_0$) to produce these noise sidebands. The noise at these two sideband frequencies and their correlation is then manipulated to produce the phase noise. Mixing noise tends to be valid at large offset frequencies and will show a finite noise floor.

MDS Phase Noise MDS 7.0 considered that the total phase noise could be obtained by adding the FM and mixing phase noise terms together. A pseudo noise voltage was output by the simulator, which the user then divided by the oscillator rms voltage squared on the presentation page to get the phase noise in dBc.

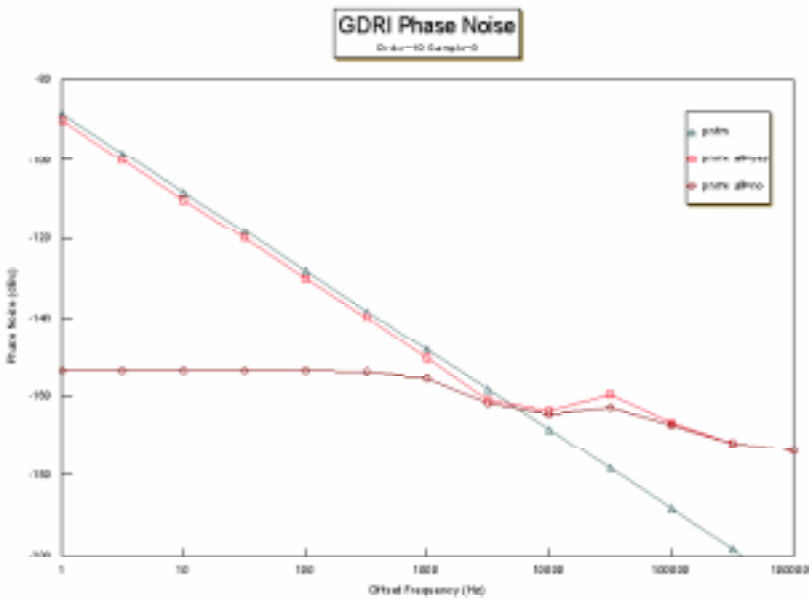
However, the FM and mixing phase noise terms are not independent and thus should not be added to produce the overall phase noise. Rather, these two terms are different views of the same process. To this end, MDS 7.1 has made available the phase noise (directly in dBc) from each of these processes individually. Assuming a circuit had a node named vout, the following variables are available for use in a presentation following a phase noise analysis:

hb_noise.vout	the original combined pseudo noise voltage
hb_noise.vout.pnmx	the phase noise (in dBc) from mixing analysis
hb_noise.vout.pnfm	the phase noise (in dBc) from FM analysis

The old output variable `hb_noise.vout` should not be used. Instead, the two variables `hb_noise.vout.pnmx` and `hb_noise.vout.pnfm` that represent the different models of phase noise should be plotted separately. There should be a region of offset frequencies where the FM and mixing noise produce the same results.

This can be the case in MDS 7.1, but only if `allSSfreqs=yes`. The `allSSfreqs` parameter controls the number of small signal frequencies used in the mixing analysis; if true, then the sidebands around all of the large signal frequencies are used (2*order+1 small signal tones); otherwise sidebands are used only around the lowest half of the large signal frequencies (order+1 small signal tones). MDS 7.0 incorrectly forced `allSSfreqs=no`, silently overriding whatever the user specified, but further research has shown that `allSSfreqs=yes` is the required setting. Setting `allSSfreqs=no` can severely underestimate the mixing noise, especially at small offsets. This is not because the extra sidebands contribute more noise, but is due to a matrix stability issue. The user should ensure that `allSSfreqs=yes` to obtain good phase noise results from the mixing analysis.

Shown below are the different components of phase noise for a simple oscillator. Phase noise due to mixing, `pnmx`, is shown for both `allSSfreqs=yes` and `allSSfreqs=no`. Good agreement can be seen between the phase noise from the FM analysis, `pnfm`, and the mixing `allSSfreqs=yes` case. There is not a good agreement at smaller offsets when `allSSfreqs=no`.



Not all oscillators will show such good agreement between mixing noise and FM noise. There can exist an offset frequency below which the mixing noise goes flat and no longer shows an f^{-2} behavior. The mixing description of phase noise is more valid at large offsets. Not all oscillators will exhibit this problem. To some extent, this corner frequency can be reduced by increasing oversample or order, at the expense of increased run time.

References

[1] J.M. Paillot *et al*, "A General Program for Stead State, Stability, and FM Noise Analysis of Microwave Oscillators," *1990 IEEE MTT-S Digest*, pp. 1287–1290.

[2] V. Rizzoli *et al*, "General Purpose Noise Analysis of Forced Nonlinear Microwave Circuits," *Proc. Military Microwaves 1992 (Brighton)*, pp. 293–298.

[3] V. Rizzoli *et al*, "General Noise Analysis of Nonlinear Microwave Circuits by the Piecewise Harmonic-Balance Technique," *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, pp. 807–819, May 1994.

[4] V. Rizzoli *et al*, "A General-Purpose Harmonic-Balance Approach to the Computation of Near-Carrier Noise in Free-Running Microwave Oscillators," *1993 IEEE MTT-S Digest*, pp. 309–312.

Other Model and Simulator Changes

An error where the SML frequency multiplier caused convergence problems has been corrected.

The errors of no convergence on MOS Model 9 and a MOS Model 9 segmentation fault with nonlinear noise have been corrected.

`FM_DEMOD` and `PM_DEMOD` components have been improved for cases where they were behaving incorrectly.

The SML polynomial and pole_zero filters have been fixed so that S11 and S22 are now 0.0.

Resistors used in most tuned modulators and demodulators now have 0 deg noise temperature, which improves the accuracy of the noise simulations.

Harmonic balance convergence of the MexTram model has been improved.

The error where HP Impulse incorrectly issued a warning message that a circuit was purely resistive and that a fixed step-size would be used has been corrected.

The error that caused the simulator to abort when the gradient optimizer performed 100 iterations or more has been corrected.

The problem of degraded convergence when using GaAsFETs with Circuit Envelope has been corrected.

The error that caused the simulator to terminate when a parameter of a linear device depended on frequency has been corrected.

The harmonic balance engine has been improved to better handle when the circuit matrix is singular.

The Circuit Envelope panel of the simulation setup dialog box would occasionally display incorrect time units for time-step and stop time. This has been corrected.

S-port device with S11 not in the dataset, but other S-parameters in the dataset, caused system to crash. This has been corrected.

A problem that could cause large admittances for short-length components at DC has been corrected. This affected the TFR, RIBBON, WIRE, MSRBEND, SLOBEND, SLOC, and SSTFR components.

An error in the MSTAPER model caused incorrect results at DC for a lossless MSTAPER. This is no longer the case.

The problem that sometimes caused incorrect values for device parameters that depend on the simulation temperature field temp has been fixed.

The error that caused Circuit Envelope to crash when an MSTL parameter depended on the parameter freq has been corrected.

A MOSFET bug that could cause a segmentation violation has been fixed.

BROCTL, BR3CTL, and BR4CTL components have been enhanced to allow negative spacing between strips on different layers.

IBIS models now support IBIS 2.1

A problem with reading ICCAP data files into MDS has been corrected.

A problem that sometimes caused noise sidebands to be incorrect for a two-tone simulation with the noise frequency above the LO frequency has been corrected.

A problem where large simulations caused MDS to run out of swap space on SUN platforms has been fixed.

An error where oscillator phase noise analysis produced incorrect phase noise results has been corrected.

HPfet and HPdiode models now correctly handle measured parasitic resistors when the value is zero.

The scaling for HPfet was incorrect when the scaling factor was large (<20) or small (>0.01) This has been fixed.

Obsolete parameters were removed from the EDIT COMPONENT dialog box for the eebjt2 model.

The impedance of port3 in the AM_MOD component is fixed. The impedance depended on the modulator's sensitivity. It has been corrected to be equal to the parameter Z0.

The Circuit Envelope implementation of the TL model was incorrect when the outer conductor nodes were not grounded. This has been corrected.

The YPORT device was not being properly handled in Circuit Envelope. This problem has been fixed.

The pole-zero and polynomial filters have been fixed to work with Circuit Envelope.

An error in controller-swept Circuit Envelope analysis has been corrected. After the first sweep, the noise sources were turned off and the first time point of some sources was wrong.

Scaling of the phase-noise modulator has been corrected.

Gaussian and other SML filters were incorrectly handled in Circuit Envelope. This has been corrected.

Small signal mixer/nonlinear noise of many FDD based models has been corrected.

An error where the baseband phase-frequency detector behaved incorrectly in certain cases has been fixed.

S-domain dependent sources with one pole had incorrect initial values. They are now correct.

S-parameter devices requiring pole/zero fits (not TLs) for Circuit Envelope were incorrect. This has been fixed.

MDS Layout

An incorrect auto-layout of circuits with pin offset from trace center has been fixed.

An incorrect auto-layout of round spiral inductors has been fixed.

An error with the way edge pins were reconnected after a component was deleted has been corrected.

An error where bad components were being created in a copy/multiple of a layout subcircuit has been corrected.

An error with degenerate arcs causing an arithmetic exception for certain unit changes with small physical unit resolutions has been corrected.

SPICE Netlist Translator

A variety of changes to improve HSPICE syntax parser have been made.

Subcircuit name comparison is now case-insensitive. Previously, this generated a warning in the log file if a subcircuit reference was unresolved.

An error in processing of `nH` and `pF` suffixes has been corrected. Previously, output values had a loss of precision and were output as 0.

For `BJT` and `Diode` devices, the use of the `AREA` keyword will now be recognized if it is used as a variable name.

The capability to handle `K=value` syntax on coupled inductors has been added.

The prefix `MOD` is now added to all models and model references to ensure unique names.

The `BJT` params `rb`, `rc`, `re`, `rbm`, and `ikr` are set to "" if their value is `0`. The translator does not evaluate expressions, thus the simulator will continue to have a problem if the expression evaluates to 0.

An error in reading `Resistor` when TC values are given has been corrected to allow curly braces around subcircuit parameters. For example: {name=value}. Note: This is an undocumented HSPICE syntax.

Wire labels attached to internal pins are now named `%NETxxxxx` and are not passed to the dataset. External pins are still named `Nx`. This will prevent the dataset from becoming too large.

HP Momentum

The following corrections and improvements have been made.

General Performance Improvements

Attenuations are found in GCPWs, even in lossless materials. This is now reflected in the cross-section solver results. GAMMA and Z0 are complex numbers, even for lossless substrates and conductors.

For high frequencies, slots start resonating when the width of the slot equals half the wavelength. When this occurs, the cross section solver computations are stopped, and the last correctly computed impedance and propagation constants are used for the rest of the frequency interval.

Database extraction does a correction on substrates older than A.02.56 to include the new via singularities. The new singularities address the spikes in the S-parameters observed in several circuits with vias.

When inserting an MDS microstrip component, the pins were not removed, resulting in an incorrect port numbering. A work around was to “smash” the components. The problem is now fixed by determining whether or not the flag indicating the parent component is set.

Interface

The following interface problems have been corrected:

The reference line was in the way if an unexpected order was used for inserting CPW ports.

CPW ports did not point inward.

Inserting limited edge ports on one side of a rectangle wa problematic.

For edge ports limited by X,Y values, return to quit did not work.

There ws incorrect phase after de-embedding.

The Momentum interface did not store thickness for slot layers correctly.

After an error in the mesh, the planar solver did not start.

Incorrect DBGenerator message in LOG if the substrate is being extended.

De-embedding direction passed from UI to engines was wrong for slot ports.

In some cases, moving the reference plane for CPW ports caused the UI to flag the ports as non-colinear.

The coax ports connected to the top plane through a multiple layer via erroneously detected as being not connected at all.

DBGenerator

For very thin conductors, the DBGenerator resets the thickness to 0 and a warning message appears. In some cases the DBGenerator gave an error instead of a warning and stopped the calculations. This is now resolved.

For some examples with parallel plate mode, a “failed to converge” error could occur. This is fixed.

Accuracy has been improved for via-via and via-strip couplings.

Grid

The mesher no longer passes incorrect port numbers to the solver for grouped ports on slot level.

The mesher no longer crashes if the only overlap between a via and the metal pattern is the first segment of the via.

Using edge mesh in combination with TML seeding no longer fails.

Cross Section Solver

CPWs and coupled strips lying on the interface between two infinite half spaces with different dielectric constants can now be computed by the cross section solver.

The number of ports for the cross section solver was limited to 99 ports. This has been expanded.

The cross section solver no longer reuses data when calibrated ports are changed to internal ports and the circuit is re-simulated with no other changes.

Platforms

The SOLARIS simulator daemon was using excessive CPU time. This has been corrected.

The Instrument I/O library (`PIL` library) was missing for the HP 700 and is now available.

The problem where IBIS models would crash on the SUN platform has been corrected.

When multiple circuit pages were read from an IFF file, the SUN platform would crash and the HP platform hung. This has been fixed.

MGC/PCB and IFF Translator

Additional HP IFF hierarchical export options now allow for exporting either complete hierarchy or only hierarchy in the current file.

The “MGC PCB” layout export supports the Mentor Graphics B2 release.

MGC/PCB exports will now validate the path information of the schematics used to create the auto-layout. This will identify any layout instances that do not have corresponding schematic instances. The MGC/PCB export now aborts the transfer if the path information is incorrect.

The `design_info` file for the MGC/PCB exports now has all object types as upper case.

The attribute `HAS_SHEET` has been added to identify when a symbol/instance has a schematic representation.

IFF Layout exports now validate the path information for each instance. If the path information is incorrect, the path is removed from the instance in the IFF file.

Presentations

The unit `pA` was interpreted incorrectly. It is now interpreted as “pico ampere.”

Miscellaneous

A problem with reading ICCAP datasets has been fixed.

Documentation Additions, Notes, and Corrections 2

The corrections in this chapter should be applied to hard copy documentation. On-line documentation may include the changes.

System Installation

The following topics have been added to the MDS *System Installation* manual. A new hardcopy version of this manual is included with MDS 7.1.

Setting up Redundant FLEXlm Servers

A section added to Appendix A of the MDS 7.1 *System Installation Manual* describes how to set up redundant FLEXlm servers.

Combining License Files

A section added to Appendix A of the MDS 7.1 *System Installation Manual* describes how to combine FLEXlm license files.

Automating FLEXlm Startup with HP-UX 10.x

A section added to Chapter 3 of the MDS 7.1 *System Installation Manual* describes how to automate FLEXlm startup for platforms with HP-UX 10.x.

System Administration and Customization

Chapter 14, page 14-12: change the source path in step 1 under "For HP-UX 9.x" to read:

```
/cdrom/sicl/pil.upd
```

Chapter 14, pages 14-12: change all references of `tmp/sw` to `tmp/mydepot`.

Chapter 14, pages 14-12 through 14-16: The references to HP-UX 10.x in this chapter mean HP-UX 10.01 and HP-UX 10.20 only. SICL files are not available for HP-UX 10.10.

Chapter 14, page 14-13: change step 4 to read:

Execute one of the following two commands, based upon your operating system:

`tar xvf /cdrom/sicl1.tar`	HP-UX 10.01
`tar xvf /cdrom/sicl2.tar`	HP-UX 10.20

Chapter 14, page 14-13: in step 5, change `tmp/sw` to `tmp/mydepot/sw`.

Chapter 14, page 14-13: change step 6 to read:

```
/opt/sicl/bin/sicl_tl install
```

Chapter 14, page 14-14: in step 4, remove the reference to `Change Software View`. Under `Source Depot Path`, change `/tmp/sw` to `/tmp/mydepot/sw`. Above `Source Host Name`, insert:

`Source Deopt Type`	Specifies the source depot type. Select `Local Directory`.

Chapter 14, page 14-16: in the note under step 11, change the examples to:

`swverify -x target_directory=/tmp/mydepot/sw -d E2091D` (HP-UX 10.01)
`swverify -x target_directory=/tmp/mydepot/sw -d E2091E` (HP-UX 10.20)

Designer's Task Reference, Volume 2

Page 3-26, Table 3-4: change `arctan` output from "real or complex" to "real."

Page B-4, Table B-1: change the formula on row 3 to read:

$$V_k = A \cdot \exp(j(2 \cdot pi \cdot f_m \cdot time + B))$$

Designer's Task Reference, Volume 4

Nesting Level Parameter

Change the Nesting level description on page 2-6 to match the description for `NESTLVL` in the *Component Catalog*, Volume 2, page 14-7.

Group Delay Parameter

Page 3-5: add the following definition for group delay:

Group delay controls whether the group delays of the requested parameters are sent to the dataset. In the case of an AC simulation, this parameter does not appear.

The dialog box has been updated as shown.

Circuit Envelope Example File Locations

The file locations for some of the Circuit Envelope examples in Appendix C were not included in the manual. The locations follow.

Single-Stage Amplifier:
`Envelope/amplifiers_env/Amp_wDigMod/PI4DQPSK/single_stage_NADC`

Mixer IMD:
`Envelope/mixers_env/IMD_analysis/MixerIMD`

Phase-locked Loop, Divide-by-N Frequency Synthesizer:
`Envelope/Feedback_loops_env/PLL_DECT_LO_Synthesizer/VCO_Switching_Div_N`

Function Description Errors

Page I-3, Table I-1: change `arctan` output from “real or complex” to “real.”

Page I-6: change the delay function equation to:

$$\text{delay}(f) = -\frac{d\theta}{d\omega}, (f = Ae^{j\theta})$$

$$= -\text{deriv}(\text{phasedeg}(f), \text{freq})/360$$

where ω is the analysis frequency in radians/second and θ is the angle of *f*, in radians.

Designer's Task Reference, Volume 5

Circuit Envelope Presentations Templates

Pages 5-35 and 5-36: Replace the existing table with the following:

Template	Description
NADC_tests	
NADC_ACPR	Adjacent-channel power ratio, output spectrum, output power, PAE, gain, including the receive-side filtering
NADC_ACPR_ transmitted	Adjacent-channel power ratio, output spectrum, output power, PAE, gain, excluding receive-side filtering.
BER	Bit error ratio of NADC-modulated signal
EVM	Error vector magnitude of NADC-modulated signal
EYEconst	Eye and constellation diagrams
NADC_tests_ PwrSwp	These templates are identical to the ones listed under NADC_tests, except that here the RF power is swept, so ACPR and in-channel power versus Pavs are also plotted.
PHS_tests	These templates are identical to the NADC_tests ones, except that the symbol rate is 192 kHz.
PHS_tests_ PwrSwp	These templates are identical to the NADC_tests_Pwr_Swp ones, except that the symbol rate is 192 kHz.
GSM_tests	
GSM_ACPR	Adjacent-channel power ratio, output spectrum, output power, PAE, gain, with GSM signal source.
GSM_Ph_Freq _errors	Instantaneous phase and frequency errors, and instantaneous load power versus time.
CDMA_tests	
CDMA_ACPR	Adjacent-channel power ratio, output spectrum, output power, PAE, gain, with CDMA signal source.
EYEconst	Eye and constellation diagrams.

Multitone	Averaged output spectrum for all phase states and output spectra for each phase state.
MixerIMD	Output spectrum around the IF, input-and output-referred TOI, 5th-and 7th-order intercepts, and IF modulation waveform.
MixerIMD_ RFpwrSwp	These templates are identical to the ones listed under MixerIMD, with IMD terms and intercept points calculated versus RF power level.
MixerIMD_ LOpwrSwp	These templates are identical to the ones listed under MixerIMD, with IMD terms and intercept points calculated versus LO power level.

Gain Circles

Correct the gain circles documentation on page 7-24 as follows:

Source mismatch gain should be “This expression generates gain circles due to source mismatch...”

Power gain should be “This expression generates gain circles due to load mismatch. The circles are the locus of source reflection coefficients resulting in the specified gain.”

The following paragraphs should be added:

`Gs` and `Gl` are mismatch gain circles and the values of gain that are specified are relative to the actual gain (dB(S21)) at the frequency of interest. Thus, a mismatch gain circle of 1 dB implies that the actual gain could be improved by 1 dB if the specified locus of points were used for termination impedance.

`G` and `Ga` give the actual gain values for an amplifier and can never be greater than max(dB(S21)). The circles will be plotted relative to the actual Z0 defined on the circuit page, not necessarily 50 ohms.

Component Catalog, Volume 4

MEXTRAM Model

Page 4-21: add the following default values to the table of parameters:

LEVEL: 503

EXMOD: yes

EXPHI: yes

EXAVL: yes

IS: 9.6369e-18

BF: 138.9

XIBI: 0.0

IBF: 2.7223e-15

VLF: 0.6181

IK: 1.5e-2

BRI: 6.243

IBR: 4.6066e-14

VLR: 0.5473

XEXT: 0.5358

QBO: 9.3424e-14

ETA: 4.8

AVL: 76.43

EFI: 0.7306

IHC: 5.8359e-4

RCC: 11.09

RCV: 981.9

SCRCV: 1769.0

SFH: 0.3556

RBC: 134.4

RBV: 307.7

RE: 1.696

TAUNE: 6.6626e-12

MTAU: 1.0

CJE: 4.9094e-14

VDE: 0.8764

PE: 0.3242

XCJE: 0.26

CJC: 8.7983e-14

VDC: 0.6390

PC: 0.6135

XP: 0.5

MC: 0.5

XCJC: 2.7018e-2

TREF: 22

DTA: 0.0

VGE: 1.129

VGB: 1.206

VGC: 1.120

VGJ: 1.129

VI: 2.1e-2

NA: 4.4e+17

ER: 2.0e-3

AB: 1.0

AEPI: 1.9

AEX: 0.31

AC: 0.26

KF: 0

KFN: 0

AF: 1.0

MULT: —

ISS: 5.8602e-17

IKS: 6.7099e-6

CJS: 2.2196e-13

VDS: 0.5156

PS: 0.3299

VGS: 1.12

AS: 1.9

BSIM3 Model Parameter

Page 4-103: Add the following parameter to the table:

`M`	Number of devices in parallel	—	`1.0`

The multiple device option, `M`, has been added to the BSIM 3 model. The `M` parameter simulates multiple parallel devices. MOSFET channel width, diode leakage, capacitors, and resistors are affected. The default is `1.0`.

HBT Model

Menu Path

```
INSERT/MDS COMPONENTS/NONLINEAR DEVICES/HBT/NPNHBT
INSERT/COMPONENT/BY LABEL/NPNHBT
```

Parameters

Parameter	Description	Units	Default
Forward Delay			
TFB	Base transit time	sec.	0
TFC0	Collector forward transit time	sec.	0
VTC	Characteristic voltage for TFC	V	1000
ITC	Characteristic current for TFC	A	1000
ITC2	Characteristic current for TFC	A	2000
TKRK	Forward transit time for Kirk effect	sec.	0
VKRK	Characteristic voltage for Kirk effect	V	1E3
IKRK	Characteristic current for Kirk effect	A	1E3
XTTF	Exponent for TF temperature dependence	—	0
XTIKRK	Exponent for IKRK temperature dependence	—	0
XTITC	Exponent for ITC temperature dependence	—	0
XTITIC2	Exponent for ITC2 temperature dependence	—	0
XTVKRK	Exponent for VKRK temperature dependence	—	0
XTTKRK	Exponent for TKRK temperature dependence	—	0
FEX	Factor to determine excess phase	—	0
TBEXS	Excess BE heterojunction transit time	sec.	0
TBCXS	Excess BC heterojunction transit time	sec.	0
Emitter/Base Currents			
BF	Forward ideal current gain	—	1E4
ISE	Saturation value for nonideal base current	A	1E-30
NE	Ideality factor for nonideal forward base current	—	2

TNE	Coefficient for NE temperature dependence	—	0
EAE	Activation energy for ISA temperature dependence	V	0
ISEX	Saturation value for emitter leakage diode	V	1E-30
NEX	Ideality factor for emitter leakage diode	—	2
TNEX	Coefficient for NEX temperature dependence	—	0
EAX	Added activation energy for ISEX temp dependence	V	0
XTB	Exponent for beta temperature dependence	—	0
Collector Capacitance			
CJC	Intrinsic BC depletion capacitance at zero bias	F	0
MJC	Exponent for voltage variation of Intrinsic BC Cj	—	0.33
VJC	Intrinsic BC diode built-in potential for Cj estimation	V	1.4
CCMIN	Minimum value of intrinsic BC Cj	F	0
ICRIT0	Critical current for intrinsic Cj variation		1E3
FC	Factor for start of high bias BC Cj approximation	A	0.8
TVJC	Coefficient for VJC temperature dependence	V/C	0
CJCX	Extrinsic BC depletion capacitance at zero bias	F	0
VJCX	Extrinsic BC diode built-in potential for Cj estimation	V	1.4
TVJCX	Coefficient for VJCX temperature dependence	V/C	0
MJCX	Exponent for voltage variation of Extrinsic BC Cj	—	0.33
CXMIN	Minimum extrinsic Cbc	F	0
XCJC	Factor for partitioning extrinsic BC Cj	—	1
CBCX	External base-collector capacitance	F	0
Temperature Parameters			
SELFT	Flag denoting self-heating should be included	logic	0
CTH	Thermal capacitance of device	C/joule	0

TNOM	Temperature at which model parameters are given	C	27
RTH	Thermal resistance from device to thermal ground	C/W	1E-3
XRT	Exponent for RTH temperature dependence	—	0
DTMAX	Maximum expected temperature rise above heatsink	C	1000
TOPER	Estimated device operating temperature	C	27
TEMP	External temperature node	C	
Noise Parameters			
KFN	BE flicker noise constant	—	0
AFN	BE flicker noise exponent for current	—	1
BFN	BE flicker noise exponent for frequency	—	1
Reverse Delay			
TR	Reverse charge storage time for intrinsic BC diode	sec.	0
TRX	Reverse charge storage time for extrinsic BC diode	sec.	0
Primary Current			
IS	Saturation value for forward collector current	A	1E-25
IK	Knee current for dc high injection effect	A	1E10
NF	Forward collector current ideality factor	—	1
NR	Reverse current ideality factor	—	1
VAF	Forward Early voltage	V	1000
VAR	Reverse Early voltage	V	1000
EG	Activation energy for IS temperature dependence	V	1.5
ISA	Collector current EB barrier limiting current	A	1E10
NA	Collector current EB barrier ideality factor	—	2
EAA	Activation energy for ISA temperature dependence	V	0
ISB	Collector current BC barrier limiting current	A	1E10

NB	Collector current BC barrier ideality factor	—	2
EAB	Activation energy for ISB temperature dependence	V	0
XTI	Exponent for IS temperature dependence	—	0
Collector/Base Currents			
ISC	Saturation value for intrinsic bc junction current	A	1E-30
ISCX	Saturation value for extrinsic bc junction current	A	1E-30
NC	Ideality factor for intrinsic bc junction current	—	2
NCX	Ideality factor for extrinsic bc junction current	—	2
TNC	Coefficient for NC temperature dependence	—	0
EAC	Activation energy for ISB temperature dependence	V	0
BR	Reverse ideal current gain	—	1E4
BKDN	Flag denoting that BC breakdown should be included	logic	0
BVC	Collector-base breakdown voltage BVcbo	V	1000
NBC	Exponent for BC multiplication factor vs voltage	—	8
FA	Factor for specification of avalanche voltage	—	0.9
Emitter Capacitance			
CJE	BE depletion capacitance at zero bias	F	0
MJE	Exponent for voltage variation of BE Cj	—	0.5
VJE	BE diode built-in potential for Cj estimation	V	1.6
CEMIN	Minimum BE capacitance	F	0
TVJE	Coefficient for VJE temperature dependence	V/C	0
CBEX	External base-emitter capacitance	F	0
FCE	Factor for start of high bias BE Cj approximation	—	0.8
Substrate Diode			
CJS	Collector-substrate depletion capacitance (0 bias)	F	0

MJS	Exponent for voltage variation of CS Cj	—	0.5
VJS	CS diode built-in potential for Cj estimation	V	1.4
ICS	Saturation value for collector-substrate current	A	0
NCS	Ideality factor for collector-substrate current	—	2
TVJS	Coefficient for VJS temperature dependence	V/C	0
Parasitic Resistances			
RE	Emitter resistance	ohm	1
RBI	Intrinsic base resistance	ohm	1
RBX	Extrinsic base resistance	ohm	1
RCI	Intrinsic collector resistance	ohm	1
RCX	Extrinsic collector resistance	ohm	1
REX	Extrinsic emitter leakage diode series resistance	ohm	1
XRE	Exponent for RE temperature dependence	—	0
XREX	Exponent for REX temperature dependence	—	0
XRB	Exponent for RB temperature dependence	—	0
XRC	Exponent for RC temperature dependence	—	0
Other			
Area	Device area	—	1

Notes

Complete model information can be found at `http://hbt.ucsd.edu`.

An npn transistor is assumed. The equivalent circuit network for the large-signal HBT model is shown in Figure 2-1. There are up to 5 external nodes (E, B, C, Th, S) and up to 7 internal nodes (Ei, Bi, Ci, Bx, Cx, Ex, T). If the flag `SELFT` is set `false`, the temperature nodes `Th` and `T` are not defined. Tcom is a global thermal ground, corresponding to absolute zero temperature.

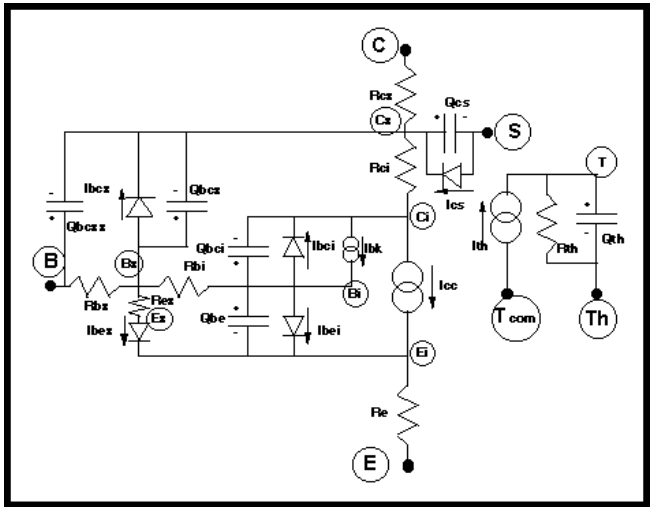


Figure 2-1. Circuit diagram for large signal HBT model

For ac analysis, a corresponding small-signal model is defined. The topology of this model is shown in Figure 2-2. It is noteworthy that the model contains dependent current sources that have the function of transcapacitances as well as transconductances.

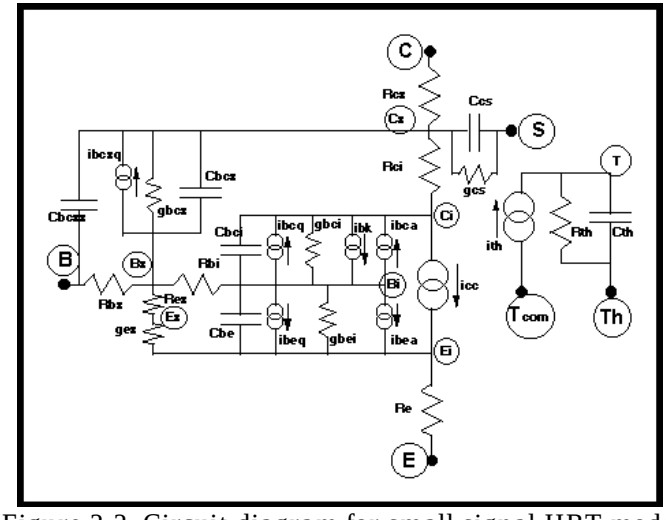


Figure 2-2. Circuit diagram for small signal HBT model

The HBT model allows various degrees of trade-off between accuracy and computational complexity. Flags permit turning off several features of the model in order to allow faster computation or easier convergence. Models of lower complexity are obtained by deleting some of the nodes and corresponding equations.

In formulating the present HBT model, backward compatibility with the "standard" SPICE Gummel-Poon model has been sacrificed. Most, but not all, formulations from Berkeley SPICE have been retained.

Scaling of parameters according to specification of device area is supported, as in the conventional BJT model.

There is no scaling associated with device perimeter. Scaling is introduced in conventional fashion; for area factor `Area`:

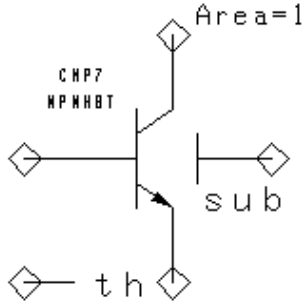
- Currents, charges and capacitances scale as `Area`
- Resistances scale as 1/`Area`
- N, VJ, MJ, Beta, TF components, VA, activation energies, and exponents for T variation remain unchanged.

The model in MDS follows the UCSD HBT model equations version 10c 8/96 as closely as possible, with the following differences:

Parameter Names	
UCSD	**MDS**
TOP	TOPER
A	Area
Maximum value of Node T (junction temperature)	
UCSD	**MDS**
Th+DTMAX	TEMP+DTMAX
Minimum value of Node T (junction temperature)	
UCSD	**MDS**
Th	TEMP

Additional parameter value limitations include:

- Series and thermal resistance cannot be zero.
- `ITC` and `ITC2` cannot be zero.
- Minimum capacitance parameters, such as `CEMIN`, cannot be set to zero unless the corresponding capacitance, `JE`, is also set to zero.
- The optional nodes `Th` and `Sub` must be connected.



HP 855243A I/O Buffer Library User's Guide

The following model descriptions have been added to the online version of the I/O Buffer Library User's Guide:

- IBIS termination
- IBIS I/O open sink (drain) driver
- IBIS I/O open source driver
- IBIS I/O open sink (drain) driver, inverted output
- IBIS I/O open source driver, inverted
- IBIS three-state driver
- IBIS open sink (drain) driver
- IBIS open source driver
- IBIS three-state driver, inverted output
- IBIS open sink (drain) driver, inverted output
- IBIS open source driver, inverted output

CAE Communication Framework User's Guide

A new online version of the CAE Communication Framework Links User's Guide is available with MDS 7.1. It includes updates for the following topics:

- Installing the translator for use with Cadence products
- Transferring Cadence libraries
- Transferring files between MDS and Mentor products
- Transferring files between MDS and Cadence products
- Using Cadence components in an MDS simulation

Using the Design Database Language (DDL)

Some of the DDL examples have been corrupted so that the character combinations : : and “” do not appear in program lines. For example, on page 9-12 and 9-13., the examples should be:

```
scion[@power ::= “”,
      @vendor ::= “”,
      @cost ::= “”,
      done]
```

```
scion[@power ::= “0.00 mW”,
      @vendor ::= “000-000”,
      @cost ::= “.00”]
```

```
scion[ column[ @name := “”],done]
```

```
scion[ column[IF(@name,”vendor”,
                 @name := “”,”)]done]
```

The characters : : are used in the operator ::=, which is used when assigning an attribute as in the above examples or, in general, @<somename>. It indicates that if the attribute <somename> does not exist, then you must create it.

The characters “” represent a NULL string in these examples. However, “” is also used when trying to place quotes inside a string. For example,

```
$a = “””this string includes a double quote in the beg and end of
the string”””;
```

If you were to print out $a, the result would be:

```
“this string includes a double quote in the beg and end of the
string”
```

Design Database Language (DDL) Reference

See the comments for *Using the Design Database Language (DDL),* above.