Parallel Cell / Traffic Generator and Analyzer System

HP E4829B, HP E4821A

Product Overview

The HP E4829B is a flexible cell / traffic generator and analyzer system for the functional verification and debugging of today's complex cell-based communication designs. These include ATM switches, hubs, routers, chip sets and ASICs from parallel custom or UTOPIA interfaces.

Designed for use by network equipment manufacturers and the semiconductor industry, it is a superior tool for optimizing and accelerating design verification to allow the earlier delivery of your products / results to your customer.

The HP E4829B parallel cell / traffic generator and analyzer system is used in research and development to verify the correct functional operation and performance of ATM designs from parallel interfaces.

In order to improve the verification process of ATM ASICs / chips or ATM sub-modules, such as switch fabrics and line interface cards, the HP E4829B features stimulus and analysis capabilities at UTOPIA standard interfaces, as well as at proprietary 8/16 bit wide parallel interfaces. Combined with this, the HP E4829B is also able to handle cell lengths of varying sizes. This means that you can isolate problems more quickly and with greater efficiency during system debug and troubleshooting.

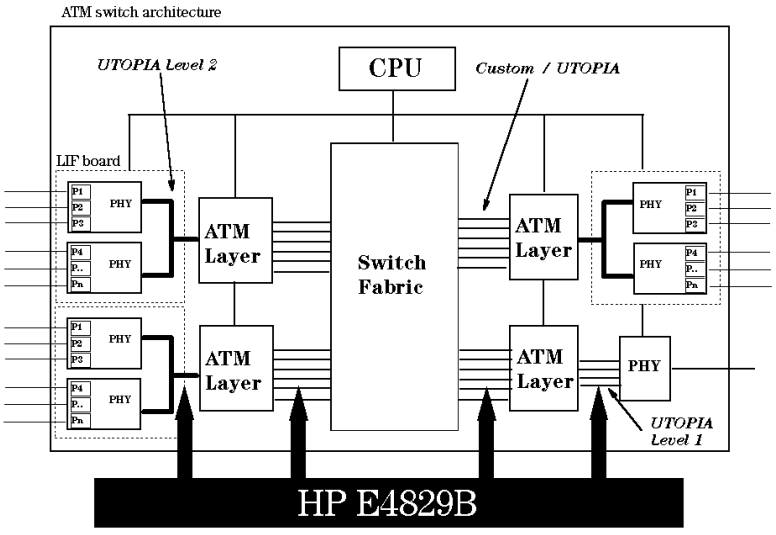

Figure 1: typical ATM switch design where HP E4829B is applied

Performance Characteristics and Ordering Information

Key benefits:
- allows concurrent engineering
- eliminates the need for self-built test equipment
- reduces the time-to-market.

Key applications:
- ATM switch fabric exercising, e.g. the verification of cell integrity, header translation, routing tag handling and cell delay variation measurements
- verification of ATM layer functions, e.g. traffic shaping, cell insertion / discarding and policing functions
- functional PHY device verification, FIFO stressing
- BER performance measurement of system components
- UTOPIA Level 2 (MultiPHY) addressing and signaling test.

Meeting the needs of ATM design

ATM switch, hub or router designs are today typically divided into three main parts: PHY interface, ATM-function block and ATM switch fabric (see figure 1). To ensure a faster time-to-market, you have to develop these blocks independently and concurrently. In principle, this requires the reliable testing of the individual blocks to secure the smooth integration of the system during your final design stage.

The HP E4829B addresses your test needs in an efficient and reliable way, and its features help ASIC, chip and board designers meet their goals. It provides reliable and comparable measurement results between design teams and eliminates the need for self-built test equipment.

Regardless of whichever tests you would like to undertake, the HP E4829B is designed to conduct them all, and will:

- exercise your switch fabric e.g. by stimulating and analyzing cells with an added routing tag,
- verify the policing functions of your ATM block,
- stress your PHY devices e.g. verify proper FIFO operation at corner cases,
- validate cell delay, cell delay variation and cell errors,
- carry out BER measurements of system components.

The HP E4829B therefore clearly provides as much flexibility as you need.

Flexible cell length and structure

The HP E4829B handles any cell with a byte length between 16 and 128, and can be used to add a routing tag to your cell. This flexibility can be achieved by combining single cell segments to build cells. To set up the cell according to your specific measurement needs, you can choose from either ATM-header segments, such as real-time generated HEC fields, real-time PRBS and a CRC-10, or from time-stamp or memory-based segments.

Shape your cell streams in an application-realistic way

The HP E4829B stimulates any traffic shape from relaxed periodic up to random burst traffic. Four independent traffic generators can be programmed. The individual cell sequence can be set up and started independently to meet your application-specific needs,

Key features:
- connects to 8/16 bit parallel interfaces
- UTOPIA Level 1 and Level 2 support
- 90 KHz to 52 MHz internal or external clock
- flexible cell structures
- flexible cell length from 16…128 byte
- routing tag handling
- memory and real-time-based cell generation, including HEC, CRC-10 and time-stamp
- traffic shaping
- real-time HEC, CRC-10 and BER test
- cell trigger
- cell acquisition.

e.g. emulating a dedicated frame of cells. In a MultiPHY environment, a single module can handle up to twenty-six physical ports. The traffic can be set up in a deterministic way to archive repeatable and comparable measurements.

Analyze cell streams in real-time

The analyzer checks received cells in real-time against CRC-10 / HEC / BER and parity cell errors, and compares the received cell with eight individual cell trigger masks. The trigger mask allows each individual bit of a cell to be masked.

Up to four counters can be used to count detected cells or cell errors in real-time, e.g. to measure cell error rates or cell loss.

For in-depth analysis, a maximum of 128 Kwords of cell data can be acquired based on matched cell trigger masks or cell errors. Each acquired cell is also marked with an RX time-stamp for absolute cell delay variation.

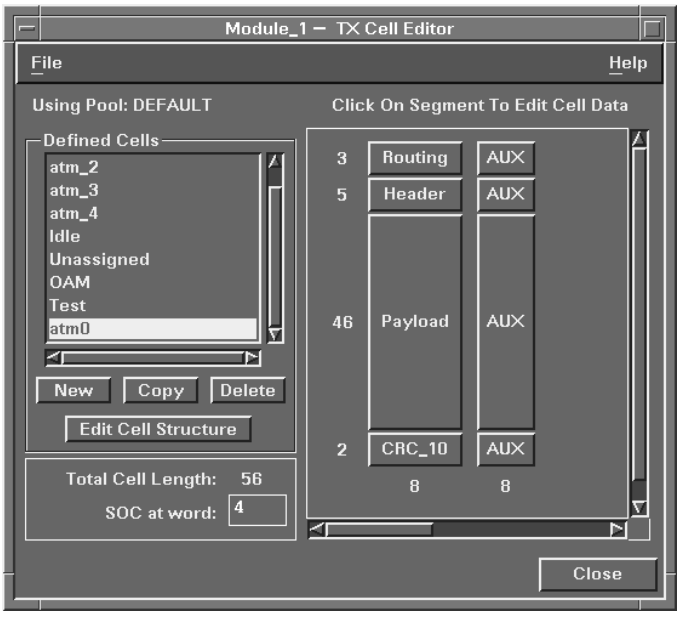

Figure 2: Cell editor

To check whether your delay variations work within certain limits over a period of time, a real-time TX time-stamp analysis can tell you how many of the cells violated your specified margins.

The modular system accommodates future needs

You are able to configure up to eight ports, based on the HP E4821A VXI hardware module (which holds one complete TX / RX port). The application-specific software modules, together with a different active POD, provide test access to 8/16 bit custom / UTOPIA Level 1 or UTOPIA Level 2 (MultiPHY) interfaces.

Combine with the broadband series test system

The HP E4821A module can also be plugged into an existing HP E4210B / HP E4200B broadband series test system (BSTS). Therefore, the parallel cell / traffic generator and analyzer system can be added to a BSTS as an independent test solution. The two applications will share a VXI frame and an embedded series 700 workstation, but the hardware, as well as the software of the BSTS and HP E4821A, are run completely independently.

Configurations

This is a brief overview of the configurations of the parallel cell / traffic generator and analyzer. Please refer to the configuration guide, P/N 5964-1605E, for more details.

Figure 3: HP E4829B 13-slot entry system

HP E4829B 13-slot entry system

The pre-installed system has one port, including:

- one HP E1401B 13-slot C-size VXI mainframe
- one HP E1497A V743 embedded controller with 32 MB
- one HP E4208B embedded disc with per-installed HP-UX 9.05 and SICL
- LAN transceiver
- graphical user interface
- one HP E4821A hardware module including:
  TX / RX PODs and application-specific software for 8/16 bit customer / UTOPIA Level 1 interfaces
  and/or
  TX / RX PODs and application-specific software for 8/16 bit UTOPIA Level 2 (MultiPHY) interfaces.

Up to seven additional ports can be added to the entry system.

In addition, a CD-drive, monitor, keyboard and mouse are required.

Adding additional ports

Each additional port requires:

- one HP E4821A hardware module including:
  TX / RX PODs and application-specific software for 8/16 bit customer / UTOPIA Level 1 interfaces
  and/or
  TX / RX PODs and application-specific software for 8/16 bit UTOPIA Level 2 (MultiPHY) interfaces.

BSTS configuration

To add the first port to a BSTS system, you will need:

- one HP E4871A graphical user interface
- one HP E4821A hardware module with:
  TX / RX PODs and application-specific software for 8/16 bit customer / UTOPIA Level 1 interfaces
  and/or
  TX / RX PODs and application-specific software for 8/16 bit UTOPIA Level 2 (MultiPHY) interfaces.

Figure 4: BSTS with HP E4821A

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Fax: (81-426) 56-7840

Latin America:
Hewlett-Packard
Latin American Region Headquarters
5200 Blue Lagoon Drive
9th Floor
Miami, Florida 33126
U.S.A.
(305) 267 4245/4220

Australia/New Zealand:
Hewlett-Packard Australia Ltd.
31-41 Joseph Street
Blackburn, Victoria 3130
Australia
1 800 629 485

Asia Pacific:
Hewlett-Packard Asia Pacific Ltd
17-21/F Shell Tower, Times Square,
1 Matheson Street, Causeway Bay,
Hong Kong
Fax: (852) 2506 9285

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