ANN-8804 REV A.
POWER HANDLING CONSIDERATIONS FOR SMD TERMINATIONS, ATTENUATORS AND RESISTORS

This document describes the power rating of high power surface mount resistive products. Furthermore, techniques for maximizing power handling performance of these parts are detailed.

SMD POWER RATING AND DERATING:

Anaren Microwave provides power ratings for all SMD resistive components. This power rating is based on the temperature at the solder interface, where the solder is in contact with the SMD component (see Figures 1a and 1b). This solder interface temperature is 100°C. This means that if the solder temperature is maintained at 100°C, then the part may safely operate at the specified power rating. If the solder interface temperature is greater than 100°C, then the operating power must be a percent of the power rating according to the derating curve (see Figure 2).

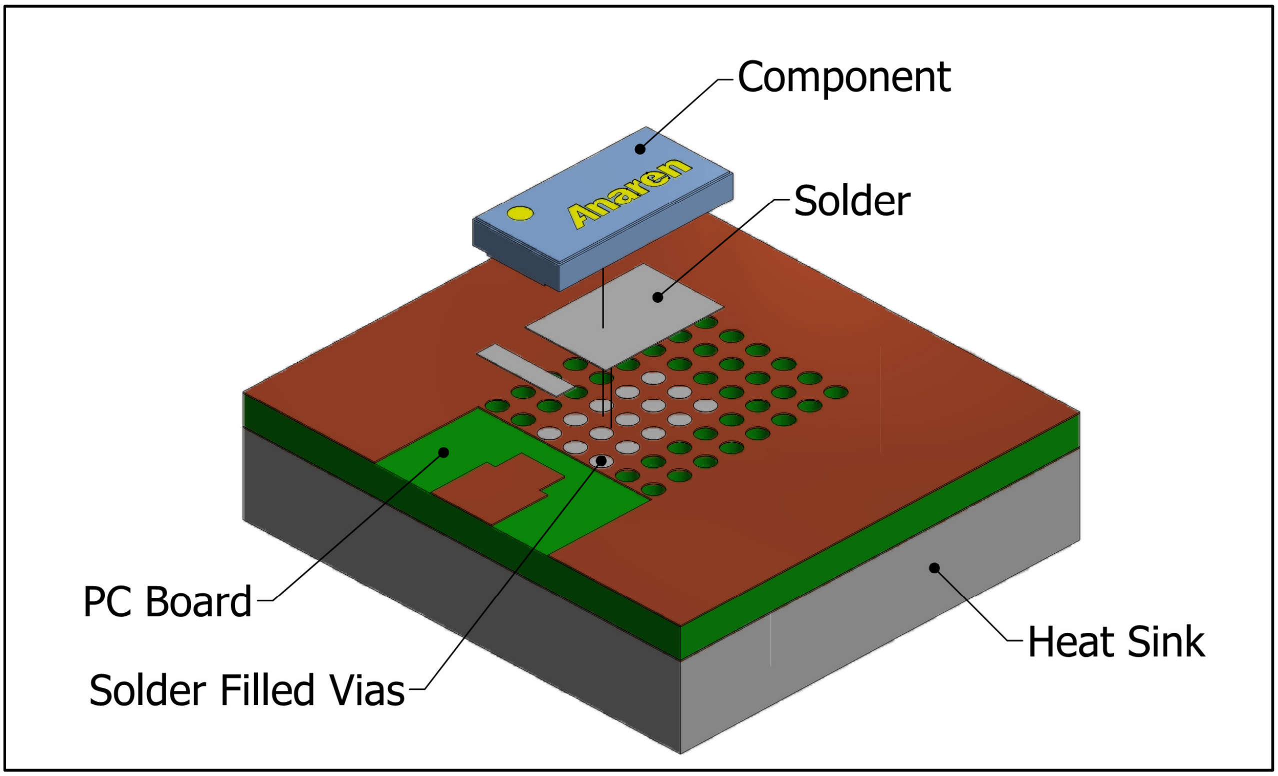

Figure 1a: 3-D view of a typical stackup and layout for SMD component.

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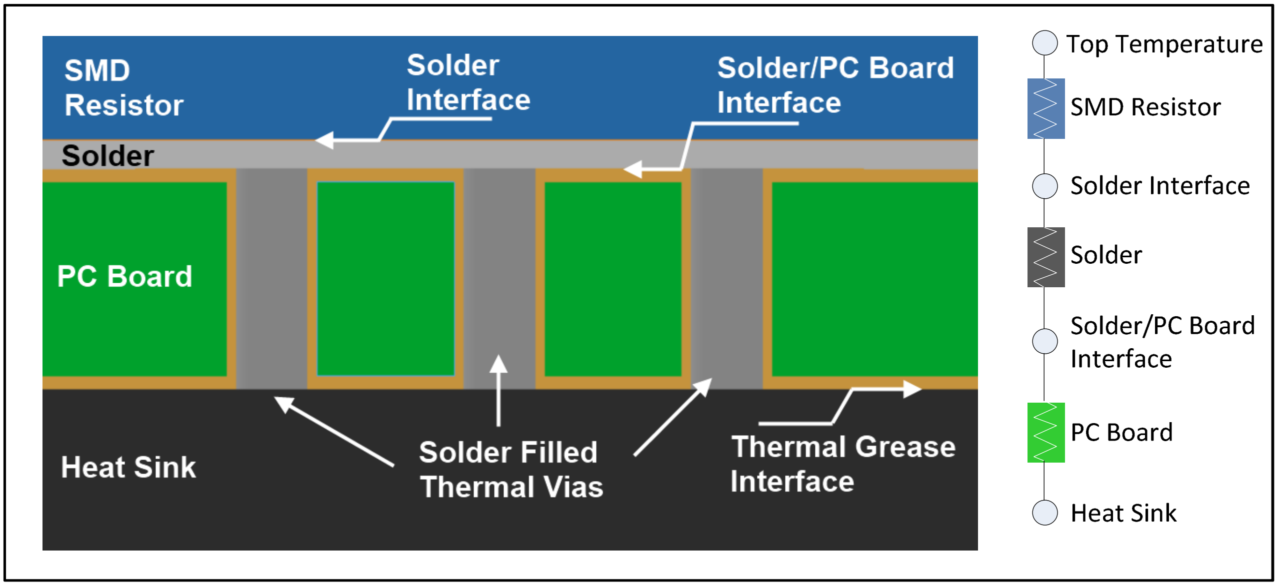


Figure 1b: 2-D cross section view of a typical stackup and layout for SMD component and corresponding thermal path.

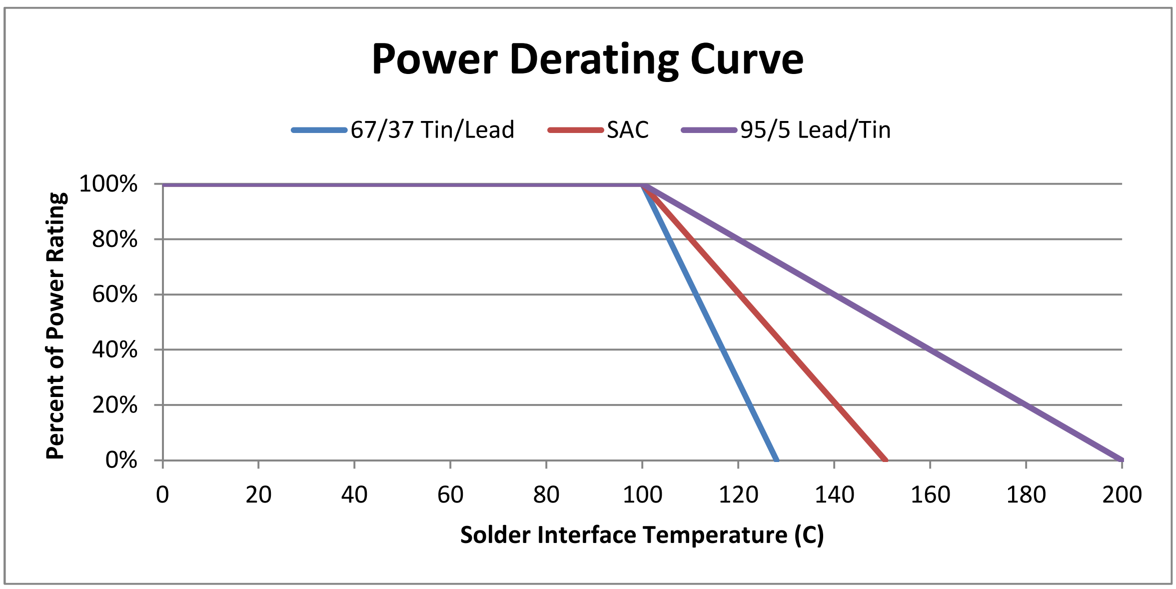


Figure 2: Power derating as a result of increased solder interface temperature.

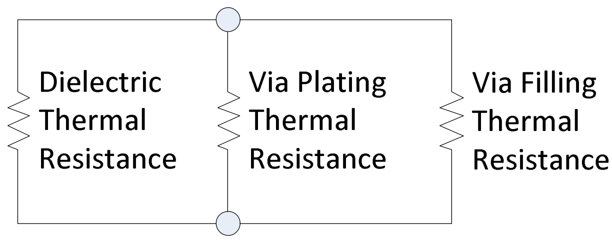
The power handling performance of the parts is affected by the design of the Printed Circuit board to which it is attached, and the assembly processes. The following three sections describe the effects these aspects have on power handling performance and how they can be optimized.

1. **PRINTED CIRCUIT BOARD DESIGN:**

In the system described in Figures 1a and 1b, the PCB will have the highest thermal resistance and the board design will have the most significant impact on the power handling of the system. It is very important to reduce the thermal resistance of the PC board as much as possible.

The total thermal resistance of the PCB is the reciprocal sum of the thermal resistances of the dielectric, the via plating, and the via fill (see equation and circuit diagram below).

$$\frac{1}{\theta_{pcb}} = \frac{1}{\theta_d} + \frac{1}{\theta_{vp}} + \frac{1}{\theta_{vf}}$$



where:

- θ_{pcb}: total PCB thermal resistance
- θ_d: dielectric thermal resistance
- θ_{vp}: via plating thermal resistance
- θ_{vf}: via filling thermal resistance.

Each thermal resistance in the above equation is a result of thermal conductivity. Other forms of heat transfer (convection and radiation) will not significantly contribute. To calculate the thermal resistance due to thermal conductivity, the following equation is used:

$$\theta = \frac{L}{kA}$$

where:

- θ: thermal resistance
- L: length through which heat must travel
- k: thermal conductivity of the material
- A: area of the cross section through which heat must travel.

For most PCBs, the dielectric material has a much lower thermal conductivity than copper or solder and so the thermal resistance of the dielectric is very high (and the reciprocal is near zero) and can be ignored. For example, a typical 0.030" thick PCB composed of PTFE based dielectric has a thermal resistance through the dielectric of $\theta_d = 4100 \frac{°C}{W}$.

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Ensuring that all thermal vias are solder filled can significantly reduce the overall thermal resistance of the PCB. Typical SAC solder has a thermal conductivity of 60 $^{W}/_{m\text{-}K}$ and it is recommended that all thermal vias be filled with solder.

***Note**: Most via fill pastes have low thermal conductivity and in most cases it is better to have only some vias filled with solder than to have all vias filled with via fill paste.* For example, if we consider a single via of 0.035" diameter and with 0.001" thick copper plating in the same PCB as described in the previous example, the resulting thermal resistances are provided in the following table:

Situation	**Thermal Resistance**
Via plating only, no solder filling	28.3 $^{°C}/_{W}$
Solder filling only	23.0 $^{°C}/_{W}$
Combined via plating and soldering filling	12.7 $^{°C}/_{W}$

The thermal resistance of the thermal vias is also affected by:

- The quantity of vias
- The via diameter
- The copper plating thickness in the vias
- The PCB height

In all cases, increasing the copper plating thickness or decreasing the PCB height will decrease the thermal resistance of the thermal vias.

Increasing the cross sectional area of the thermal vias will decrease the thermal resistance because the copper and solder have higher thermal conductivity than the PC board material. However, the number of thermal vias that can fit underneath the ground pad is dependent on the via diameter. In most cases, reducing the via diameter to allow more vias to fit in the area will improve the thermal resistance. Consider the same PC board as the previous examples with all vias solder filled and a 0.100" by 0.200" rectangular ground pad. The table below shows the number of vias that can fit, the cross sectional area of those vias, and the resulting thermal resistance of the PC board, when varying the via diameter.

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***Note**: The table below describes the use of a four point layout (see Page 6 for information about alternative three point layout).*

Via Diameter	Number of Vias	Via cross sectional area (in^2)	Resulting Thermal Resistance $\left(\frac{°C}{W}\right)$
0.010"	91	0.71471	0.0922
0.015"	50	0.58905	0.0939
0.020"	32	0.50265	0.0956
0.025"	18	*** 0.35343	0.1206
0.030"	15	*** 0.35343	0.1085
0.035"	10	0.27489	0.1269
0.040"	8	0.25133	0.1273

*** Though 0.025" and 0.030" diameter vias yield the same cross sectional area, the proportion of copper to solder is higher in the 0.030" diameter vias. Since copper has a higher thermal conductivity than solder, the thermal resistance is lower.

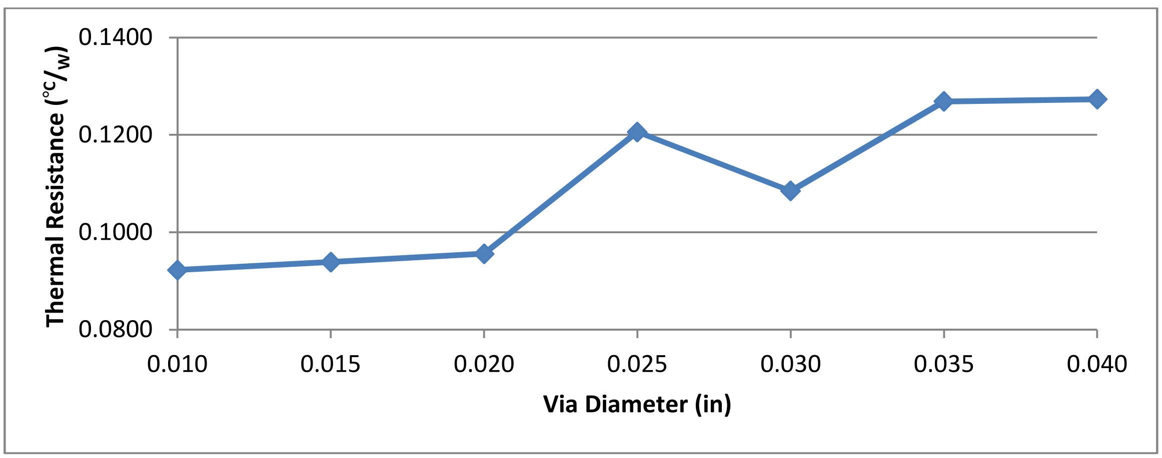

Figure 3: Thermal resistance of thermal vias with respect to the via diameter. A smaller diameter yields more vias and in general will yield a lower thermal resistance.

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2. SOLDER JOINT QUALITY:

All of the power dissipated in the SMD component must pass through solder before reaching the heat sink. A poor quality solder joint could reduce the power handling capability of the part. It is important to maintain solder joints that are 0.002" to 0.003" in height and have 20% or lower, void percentage.

3. THERMAL VIA QUANTITY:

Once a via diameter has been chosen, the manner in which the thermal vias are arranged can affect the number of vias that will fit in the area allotted. There are two layouts that maximize the number of vias: three point layout and four point layout (see Figure 4). If the three point layout can provide additional thermal vias, then it should be used. For example, in Figure 4, the four point layout provides 30 thermal vias while the three point layout provides 32 thermal vias of the same diameter in the same area.

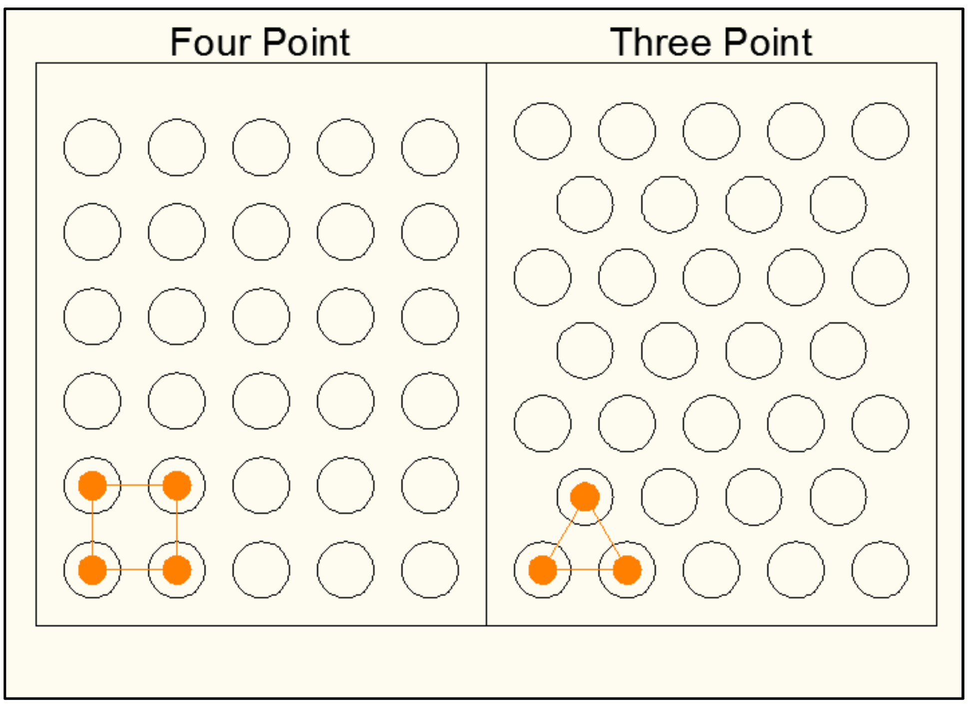

Figure 4: The two most common thermal via layout patterns.

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CONCLUSION:

The power handling value provided by Anaren for all SMD resistive components is the input power at which the component can be safely operated, when the solder interface temperature is maintained at 100°C or lower. However, in a typical design, the temperature at the solder interface is affected by the PC board design. Thus, Anaren makes the following recommendations when designing a PCB for mounting SMD terminations, attenuators and resistors:

- Minimize the thickness of the PCB
- Maximize the cross sectional area of thermal vias underneath the ground pad of the SMD component.
- Ensure good quality solder joints that are 0.002" to 0.003" in height and have 20% or less, solder void percentage.
- Maximize the number of thermal vias under the ground pad by utilizing the three point layout (in some situations, both the three and four point layouts will yield the same number of vias. In those situations it does not matter which layout is chosen).

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