5ESS® Switch
Maintenance Reference Handbook
5E13 and Later Software Releases

Document: 235-105-500
Issue Date: January 2002
Issue Number: 12.00

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Product Line: 5ESS Switch
Title: Maintenance Reference Handbook
Information Product Code: 235-105-500
Issue Number: 12.00
Publication Date: January 2002

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1. INTRODUCTION

1.1 PURPOSE

This information product is a convenient reference for maintaining the *5ESS®* switch for software releases 5E13 and later. It contains commonly used information to help respond to reported faults and abnormal operating conditions.

This information product is not a troubleshooting guide. Nor is it, because of its limited content, a substitute for detailed system documentation. It is a memory jogger and a reference guide to appropriate instruction materials. Therefore, potential users of this information product must be familiar with the information in 235-900-1xx, *Product Specifications*, and 235-100-125, *System Description*.

1.2 UPDATE INFORMATION

1.2.1 REASON FOR UPDATE

This information product is being reissued to cover the 5E16 software release, any software update information, and editorial changes. These changes are in the following sections:

- Section 3.5 - Updated Table 3-4 so that it agrees with similar table in 235-105-220, *5ESS® Switch Corrective Maintenance Procedures*
- Section 5 , Table 5-1 - Added information for the Integrated Ring Node Version 2 (IRN2) CNI cabinet
- Section 5 , Table 5-30 - Updated Module Controller and Time Slot Interchanger Unit Model 3 (MCTU3) circuit pack information
- Section 5 - Added Table 5-50 , Switch Module MCTU3 J-5D003LB-1 Circuit Packs
- Section 5 - Added Tables 5-62 , 5-63 , 5-64 , and 5-65 for the IRN2 CNI cabinet
- Section 5.1 - Replaced Figure 5.1-14 with correct figure
- Section 5.2.9 - Removed EBUS paragraph and corrected circuit pack number to read UN310 instead of TN310
- Section 5.2.10 - This is a new section which includes EBUS description and circuit pack information
- Section 5.3 - Updated title of 235-200-100 to *5ESS® Switch FLEXENT™/AUTOPLEX® Wireless Networks Applications OA&M Manual*
- Section 5.3 - Changed titles and updated contents of Access Interface Unit (AIU) Diagnostic Phase Description Tables 5.3-9 , 5.3-10 , 5.3-12 , 5.3-13 , and 5.3-14
- Section 5.3 - Updated contents of MCTSI SM-2000 Diagnostic Phase Description Table 5.3-64
- Section 5.3 - Added note to include reference to *BZ-RS User Guide* in Table 5.3-9
- Section 5.3.1 - Updated terminology from Electronic Media Networked Service (EMNS) to Web and Media Management (WMM) to reflect name change
- Section 5.3.25 - Updated MCTSI circuit pack information in Figures 5.3-34 , 5.3-35 , and 5.3-36
- Section 5.4.1 - Removed reference to discontinued document 235-190-120, *5ESS®Switch Common Channel Signaling Service Feature, Feature Document*, and replaced with reference to document 235-200-115, *5ESS®Switch CNI Common Channel Signaling*

- Section 5.4.4 - Corrected group numbers in description to read 00, 01, and 02 instead of 01, 01, and 02
- Glossary - Added/updated glossary terms
- Index.

1.2.2 SUPPORTED SOFTWARE RELEASE

In accordance with the *5ESS*® Switch Software Support Plan, the 5E12 software release is rated **Discontinued Availability (DA)** as of September 2000. The information supporting 5E12 and earlier software releases is being removed over time, instead of concurrently, from all documentation.

If you are supporting offices that use a software release prior to 5E13 and you have a need for the information that is being removed, retain the associated pages as they are removed from the paper information products, or retain the earlier copy of the CD-ROM.

1.2.3 TERMINOLOGY

1.2.3.1 Communication Module Name Change

The term Communication Module (CM) has been changed to the Global Messaging Server (GMS), representing the new portfolio name of this particular module. The current names of the specific types of the GMS (the CM2 and CM3) have not been changed. Where the CM name has been used in a generic way within this information product, the name will be changed to GMS. Where the specific version of GMS (CM2 or CM3) is being described or mentioned, the name will not be changed. However, the GMS name may be added to the description in certain places as a reminder of the change, and that the particular version is a part of the overall portfolio. The following list provides some examples of how you may see these names used together:

- Global Messaging Server (formerly Communication Module)
- GMS (formerly CM)
- Global Messaging Server-CM2
- GMS-CM2
- Global Messaging Server-CM3
- GMS-CM3.

These name changes will be made over time as other technical changes are required. Also, these changes may not be reflected in all software interfaces (input and output messages, Master Control Center screens, and Recent Change and Verify screens). Where the information product references these areas, the names are used as they are within the software interface.

1.2.3.2 Bellcore/Telcordia Name Change

As of March 18, 1999, Bellcore officially changed its name to ***Telcordia Technologies***. Not all pages of this information product are being reissued to reflect this change; instead, the pages will be reissued over time, as technical and other changes are required. Customers on standing order for this information product may see that, on previous-issue pages, the Bellcore name is still exclusively used.

Customers receiving new orders for this information product will see the ***Telcordia Technologies*** name used as appropriate throughout the information product, and the Bellcore name used only to identify items

that were produced under the Bellcore name. Exceptions may exist in software-influenced elements such as input and output messages, Master Control Center screens, and Recent Change and Verify screens. These elements will not be changed in this information product until such time as they are changed in the software code. Information product updates will not be made specifically to remove historical references to Bellcore.

1.2.3.3 *5ESS*®-2000 Switch Name Change

This *5ESS*® switch paper information product may contain references to the *5ESS*® switch, the *5ESS*®-2000 switch, or the *5ESS AnyMedia*® switch. The official name of the product has been changed to the "*5ESS*® switch."

The information product will not be totally reissued to update these references. Instead, the changes will be made over time as other technical changes are required. In the interim, assume that any reference to the *5ESS*®-2000 switch or to the *5ESS AnyMedia*™ switch is also applicable to the *5ESS*® switch. Also note that the name change may not have been carried forward into software-influenced items such as input and output messages, Master Control Center screens, and Recent Change and Verify screens.

1.3 ORGANIZATION

This information product contains Sections 1 through 6 , Glossary, and Index. A table of contents at the beginning of the information product gives a condensed view of the major subjects covered in each section.

Each section has a table of contents with a more comprehensive view of the subjects covered in that particular section. Figures and tables appear within the text of the section as close as possible to their respective references.

The information presented in this information product includes the name of other information products where in-depth, trouble-clearing procedures can be located, how to clear alarms, and how circuit packs are coded. There is a section on power distribution and a glossary that contains *5ESS*® switch specific terms.

The major section in this information product, Section 5.3 , addresses the functional modules of the *5ESS*® switch. Subsections contain the equipment bay and shelf layouts for the Administrative Module, Communication Module, Switching Module, and the Common Network Interface and their associated peripheral units. The illustrations show shelf layout, equipment location (EQL) numbers, pack codes, and backplane information for some of the shelves.

1.4 USER FEEDBACK

We are constantly striving to improve the quality and usability of this information product. Please use one of the following options to provide us with your comments:

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If you have questions or comments about the distribution of our information products, see Section 1.5 , Distribution.

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To order, call the following telephone number:

- **1-888-LUCENT8 (1-888-582-3688)** or fax to **1-800-566-9568** (from inside the continental United States)
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1.6 TECHNICAL ASSISTANCE

For initial technical assistance, call the North American Regional Technical Assistance Center (NARTAC) at **1-800-225-RTAC (1-800-225-7822)**.

For further assistance, call the Customer Technical Assistance Management (CTAM) center at the following number:

- **1-800-225-4672** (from inside the continental United States)
- **+1-630-224-4672** (from outside the continental United States).

Both centers are staffed 24 hours a day, 7 days a week.

2. MAINTENANCE SUPPORT DOCUMENTATION

2.1 GENERAL

Familiarity with the contents of 235-001-001, *Documentation Description and Ordering Guide*, can be helpful to anyone involved in *5ESS*® switch operations. Specifically, be familiar with information products considered "system interactive'' within the structure of the guide, especially those designed for maintenance functions. See Table 2-1 for a list of support information products interaction.

2.2 SYSTEM INTERACTIVE DOCUMENTS

The following is a list of reference documents for personnel in maintenance operations. A brief description of each document is given.

- 235-105-110, *System Maintenance Requirements and Tools*: This document describes maintenance concepts and built-in maintenance capabilities of the switch. It contains sections covering maintenance philosophy, maintenance tools, and Master Control Center (MCC) display pages.
- 235-105-210, *Routine Operations and Maintenance Procedures*: This document contains the descriptive material and detailed procedures for routine operations and maintenance of the *5ESS*® switch.
- 235-105-220, *Corrective Maintenance Procedures*: This document contains hardware-maintenance procedures, office dependent data maintenance procedures, supporting list of diagnostic phase descriptions, and utility call trace procedures.
- 235-105-250, *System Recovery Procedures*: This document contains descriptive material and detailed procedures for hardware and software recovery.

2.3 ASSOCIATED DOCUMENTS

Refer to the following list for documents that address maintenance procedures and associated information.

- 235-600-700, *Input Messages Manual*
- 235-600-750, *Output Messages Manual*
- 235-600-1xx, *Translation Data*

  NOTE: xx denotes the variable that reflects the respective software release.
- 235-600-400, *Audits Manual and Appendix*
- 235-600-500, *Asserts Manual and Appendix*

NOTE: For the number of a software release specific information product, refer to 235-000-000, *Numerical Index*.

Table 2-1 Support Document Interaction

Document Number	Document Title	Document Description
235-001-001	*Documentation Description and Ordering Guide*	List of *5ESS*® switch documents with brief descriptions.
235-000-000	*Numerical Index*	Menu of documents available as of index date.
System Interaction Documents		
235-105-110	*System Maintenance Requirements and*	

	Tools	□ Maintenance Philosophy □ Maintenance Tools □ MCC Display Pages
235-105-210	*Routine Operations and Maintenance Procedures*	□ Equipment Test List □ System Control Operations Description and Procedures □ Memory Alteration Description and Procedures □ Remote Office Test Line Fan and Alarm Tests □ Moving Head Disk Description and Procedures □ Miscellaneous Routine Procedures □ Routine Exercise Description and Procedures □ Feature Activation Procedures □ Operations Support Systems Activation Procedures □ Appendix - O&M Checklist
235-105-220	*Corrective Maintenance Procedures*	□ Hardware Maintenance Procedures □ Diagnostic Phase Descriptions □ Utility Call Trace Procedures □ Office Dependent Data Maintenance Procedures
235-600-115	*Input Reference Guide*	Summary of MCC index display pages, function keys system responses and construction of input message formats.
Be Familiar with Documents		
235-100-125	*System Description*	**a**
235-105-119	*Maintenance Guide Utilizing OMS5*	**a**
235-105-200	*Precutover and Cutover Procedures*	**a**
235-105-250	*System Recovery*	**a**
235-190-101	*Business and Residence Modular Features*	**a**
235-080-100	*TG-5 Translations Guide*	**a**
Notes: a. See document overview for the document description.		

2.4 DOCUMENTS REFERENCED FROM MAINTENANCE PROCEDURES

Table 2-2 is an index of information product numbers and sections that address specific maintenance

procedures.

The listed procedures appear in subject groups in alphabetical order.

Because all referenced information products are in the 235-105 series, only the last three digits of the official number appear in the column headed DOCUMENT.

System Initialization/Reinitialization Procedures are not in this table. Refer to 235-105-250 for those procedures.

Table 2-2 Documents Referenced from Maintenance Procedures

PROCEDURE	DOCUMENT
AC	
Check and Adjust AC Jack Amplifiers in Test Access Unit	220
ACTIVATE	
Execute the Activate Form	210
ADMINISTRATIVE MODULE MAINTENANCE	
Analyze and Clear Administrative Services Module (ASM) Problems	220
Analyze and Clear Nondiagnosable CU Memory Errors	220
Analyze Postmortem Dump	220
Analyze REPT:CU Error Interrupt Handler Log File (ERLOG) Entries	220
Analyze REPT:CU MEMLOG File Entries	220
Remove and/or Install Small Computer System Interface (SCSI) Disk Unit Package (DUP)	220
Replace Digital Audio Tape (DAT) Drive	220
Replace SCSI DUP Subunits	220
Respond to and Restore a Locked-Up Video Terminal	220
Troubleshoot SCSI DUP	220
Update Incore Data Base in 3B20D/21D Computer	210
ADMINISTRATIVE SERVICES MODULE	
Make Administrative Services Module Tape Backup	210
Restore Administrative Services Module Disk Files from Configuration Backup Tape	210
AIR FILTERS	
Replace Fan Tray Air Filters in SCSI Cabinet	210
Replace Fan Unit Air Filters	210
Replace Fan Unit Air Filters in Integrated Services Line Unit Drawer-Type Units	210
ALARMS	
Access Alarm Display Pages at MCC Video Terminal	220
Determine Location of a Fault in the AM, CM, or SM/SM-2000 Equipment	220
Clear Stuck/False Alarm Condition	220
Office Alarm, Test Critical	210
Office Alarm, Test Major	210
Office Alarm, Test Major Miscellaneous	210
Office Alarm, Test Minor	210
Office Alarm, Test Minor Miscellaneous	210
Perform CM/Time-Multiplexed Switch Fan Alarm Tests	210
Perform SM Fan Alarm Tests	210
Remove and Replace SM/SM-2000 Fan Unit Alarm Board	220
Replace 256A Fan Alarm Circuit Pack	220
Respond to *5ESS*® Switch Alarms	220
Respond To and Resolve Alarm Associated with an ESM Fault	220
Respond To and Resolve DAYLOG Message Lost Alarm	220
Respond To and Resolve RC/V Log Warning Alarm	220
Test Integrated Services Line Unit Fan Alarm	210
Test Office Exit Pilot Alarm Circuits	210
Test Processor Control Frame or Processor Cabinet Alarms	210
Test RSM Office Alarms	210
A-LINK	
Clear In Line Unit A-Link Failure	220
AUTOMATIC MESSAGE ACCOUNTING (AMA)	
Allow an AMA Session	210
AMA Teleprocessing Emergency Tape Writing Procedure (for Digital Audio Tape)	210
AMA Teleprocessing Emergency Tape Writing Procedure (for 9-Track)	210
Analyze and Resolve Assert Error Report	220
Analyze and Resolve Audit Error Report	220
Bring Up Automatic Message Accounting Teleprocessing System (AMATPS)	210
Change AMAOPTION Attribute	210
Clear AMA Configuration Information	210
Configure AMA Dual Stream Billing	210
Configure AMA Single Stream Billing From Dual Stream	210
Degrow AMA Partition for Storage Module Drive-Moving Head Disk Pair on 3B20D Computer Model 3	210
Dump AMA Block to Receive-Only Printer	210

Equip AMA Disk Partitions	210
Initialize the AMA System Process in Each Switching Module	210
Initialize the AMA System Process in the Administrative Module	210
Install Automatic Message Accounting Teleprocessing System (AMATPS) Options on *Paradyne*® 3810 Modem	210
Load Tape Into Digital Audio Tape Drive	210
Mount and Verify AMA Tape (for Digital Audio Tape)	210
Mount and Verify AMA Tape (for 9-Track)	210
Nonteleprocessing Write of AMA Data from Disk to Tape (for Digital Audio Tape)	210
Nonteleprocessing Write of AMA Data from Disk to Tape (for 9-Track)	210
Remove AMA Tape	210
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Set AMAOPTION Attribute for AMA Teleprocessing System □ 5E8 and Later	210
Set AMA Stream Value	210
Set AMA Stream Value for Each Switching Module	210
Set Up AMA Control File	210
Validate Automatic Message Accounting Teleprocessing System (AMATPS) Hardware Configuration	210
Verify AMA Operation with On-Line Functional Test - 5E8 and Later	210
B-LINK	
Clear B-Link or LUCHAN Failure in Line Unit Grid	220
CALL PROCESSING	
Analyze and Clear Per-Call Test Failure	220
Perform Ringer Count Check, On an On-Hook Analog Line □ Using Directly Connected Test Unit	220
CALL TRACE	
Analyze Hardware Summary Output Messages	220
Analyze Software Data Output Messages	220
Call Trace Procedures	220
Determine Hardware and Software Used During Call Processing	220
Obtain Most Recent Software Call Trace Data	220
Perform In-Process Call Trace	220
Perform Nuisance (Terminating Tandem/Interoffice) Call Trace	220
CENTRAL TRUNK TEST UNIT (CTTU)	
Bring Up CTTU	210
Define CTTU Logical Test Port Group	210
Enable CTTU as Recipient of 101 Test Line	210
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Common Network Interface Power Pack Replacement	220
Common Network Interface Ring Circuit Pack Replacement	220
Common Network Interface Ring Fuse Replacement	220
Convert TN 56 Circuit Packs to TN 2012 Circuit Packs	210
Determine Switch/Strap Settings for Transmission Rate Conversion Unit Circuit Packs	220
Perform Sequential Removal and Insertion Circuit Packs - LU	220
Replace Alarm Status Unit/Alarm Status Unit 2 Circuit Module	220
Replace Scanner and Signal Distributor UN33B Circuit Pack	220
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Analog Coin Phone Test to Perform Near-to-Far-End Check of Line State [via Subscriber Line Instrument Measurement (SLIM)]	220
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Clear Message Switch Problems	220
Clear Network Clock Problems	220
Clear Network Link Interface Problems	220
Clear Office Network and Timing Complex Common Problems	220
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Replace TRCU3 Fuse Alarm Module (CM-2601A)	220
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Respond To and Resolve an RC/V Log Warning Alarm	220
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Test Digital Subscriber Line Basic Rate Interface (BRI) Dial-Up	220
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Define Logical Test Port Trunk Group for DCTU	210
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Grow Digital Networking Unit - Synchronous Optical Network Virtual Tributary 1.5/Digital Signal 1 Facility - 5E13(1) and Later	210
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Perform Differential Backup - ODD	210
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Implement 108-Type Test Line Capabilities of ISTF/GDSF	220
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Respond To and Resolve Locked-Up Video Terminal	220

3. MAINTENANCE PROCEDURES SUPPORT INFORMATION

3.1 INTRODUCTION

This section contains information related to operating and maintaining the *5ESS*® switch. The basic data are generally referenced to the master control center (MCC) displays and audible notices.

Figure 3-1 is a flowchart that describes a typical procedure for determining maintenance requirements.

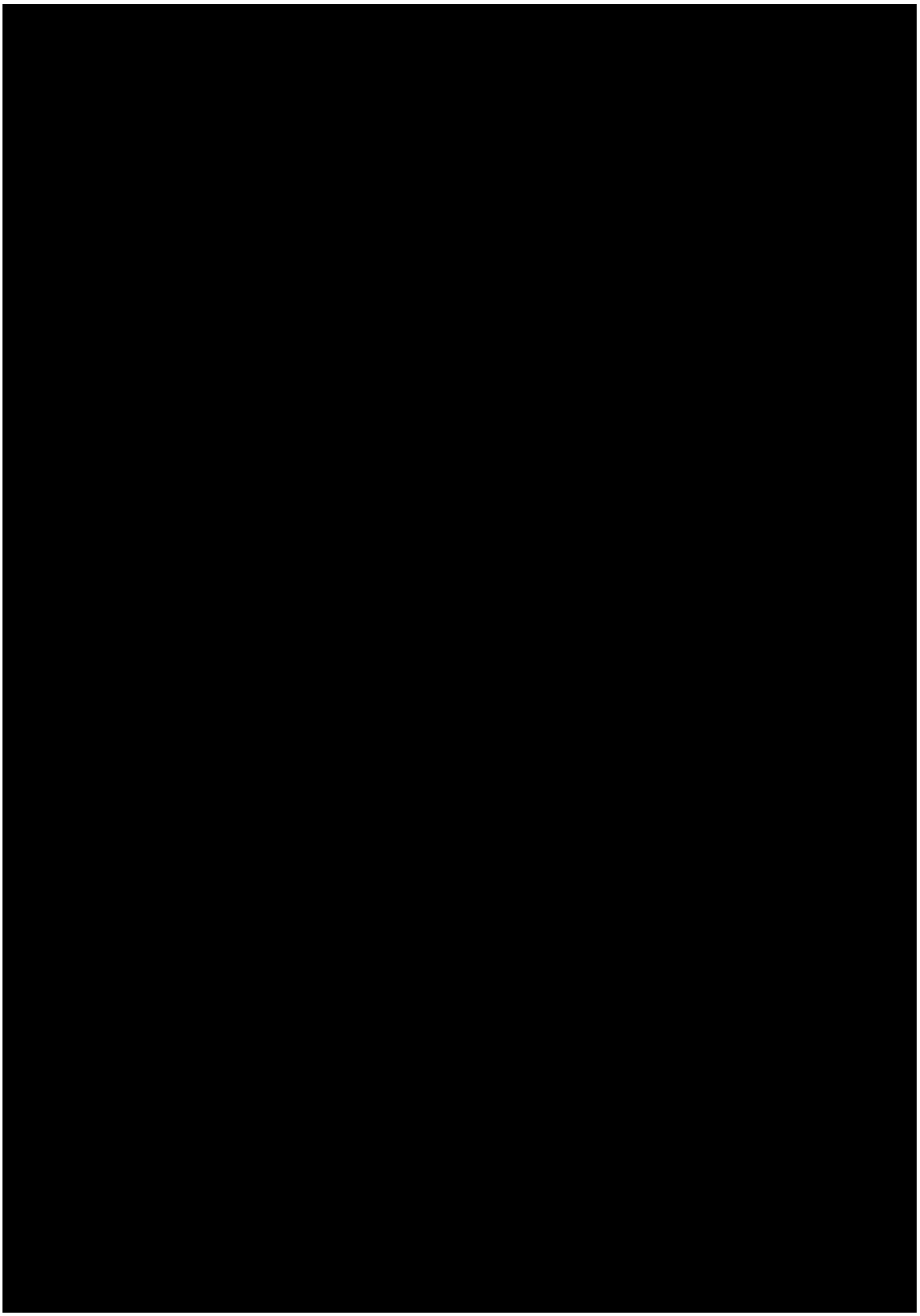

Figure 3-1 Determining Maintenance Requirements

3.2 AUDIBLE AND VISUAL ALARMS

3.2.1 DISPLAY OF SWITCH STATES

Whenever an alarm condition occurs, an audible/visual alarm is activated to ensure that maintenance personnel are informed even if the MCC terminal is not being monitored. To make it easier for maintenance personnel to quickly locate off-normal conditions on the video displays, various video attributes such as reverse video, flashing, intensity, and color (optional) are used in addition to text. The particular combination of these attributes depends on the maintenance "state.'' Table 3-1 lists the most commonly used MCC states and their video characteristics. For more detailed listings of switch states, refer to 235-105-110, *System Maintenance Requirements and Tools*.

Table 3-1 Display of *5ESS*® Switch States MCC Video Terminal

STATE	TEXT DISPLAYED	COLOR TERMINAL	BLACK AND WHITE TERMINAL
Critical Alarm	none	Steady or flashing white on red	Steady or flashing black on white
Deferred	DEFR	Steady yellow on red	Steady black on white
Major Alarm	none	Steady or flashing red on yellow	Steady or flashing black on white
Minor Alarm	none	Steady or flashing black on white	Steady or flashing black on white
Active	ACT	Steady black on green	Steady white on black
Active Forced	ACTF	Steady red on green	Steady white on black
Degrade	DGR	Steady red on green	Steady black on white
Degrade Forced	DGRF	Steady red on green	Steady white on black
Growth	GROW	Steady black on cyan	Steady white on black
Idle	IDLE	Steady black on white	Steady black on white
Inhibit	INH	Steady blue on yellow	Steady black on white
Initialization	INIT	Steady black on yellow	Steady white on black
Limited	LMTD	Steady red on white	Steady white on black
Normal (default)	none	Steady white on black	Steady white on black
Out of Service	OOS	Steady white on red	Steady black on white
Out-of-Service Power	OOSP	Steady white on red	Steady black on white
Out-of-Service Transient	OOST	Steady blue on white	Steady white on black
Out-of-Service Family	OOSF	Steady red on white	Steady white on black
Special Growth	SGRO	Steady black on cyan	Steady white on black
Standby	STBY	Steady black on white	Steady white on black
Test	TEST	Steady blue on white	Steady white on black
Trouble	none	Steady white on red	Steady black on white
Unavailable	UNV	Steady red on yellow	Steady black on white
Unavailable Power	UNVP	Steady red on yellow	Steady black on white
Unavailable Transient	UNVT	Steady blue on yellow	Steady black on white
Unequipped	UNEQ	Steady white	Steady white

		on black	on black
Customer	CDNY [a]	Steady red on yellow	Steady black on white
Camp On	CAMP	Steady red on green	Steady white on black

Notes:

a. CDNY is displayed after camp-on timeout occurs on ISLU LGC and some LU COMC circuits.

3.3 SIMULATE OFFICE ALARMS

Table 3-2 lists the procedures used to simulate office alarms.

Table 3-2 Simulate Office Alarms

ALARM	COMMENT [a]
Critical fire	Use local procedures.
Fire alarm trouble	Use local procedures.
High temperature	Apply heat to sensor.
Low temperature	Apply ice to sensor.
Air dryer	Remove fuse of power ON air dryer.
Door intrusion	Open door.
Air conditioner	Remove power at AC disconnect.
Miscellaneous power supplies	Not applicable.
Miscellaneous alarm circuit	Not applicable.
Discharge fuse fail	On power plant, short pins 8 and 9 on any of the circuit breakers.
Inverter fail	To simulate loss of -48 V from the inverter, short pins 2 and 3 on TB5 of K1 relay of the inverter.
Inverter transfer alarm	Operate the TEST switch at the front of inverter.
Miscellaneous	Not applicable.
Low voltage	With conditions permitting, power down all battery charging rectifiers. Low-volt alarm will activate when plant voltage monitor reads between -48.25 V and -51.25 V.
Rectifier fail	Power any single rectifier down.
Fuse ALM PDF	Insert blown indicator fuse in at least one fuse position of each fuse block.
Alarm battery ALM	Insert blown indicator fuse in Alarm Battery Source.
CO BATT DISCHG	Power all battery charging rectifiers down.
STBY PLANT ALM	See STBY PLANT manual.
High volt	Increase voltage output of one rectifier enough to raise plant voltage monitor to -53.25 V.
Commercial power failure	Operate TEST switch at front of inverter.

Notes:

a. Due to possible danger, difficulty, or potential damage to unit when attempting to force a true alarm condition, a short across the scan lead or an open in the scan lead loop should be used to simulate an alarm for alarms where no comment is given. The ``TERM'' column of the office engineering records indicates whether an alarm is normally opened or closed.

3.4 ACTIVATION OF OFFICE ALARMS (REMOTE SWITCHING MODULE)

Table 3-3 lists the procedure to follow in testing activation of remote switching module office alarms.

Table 3-3 Activation of Office Alarms Remote Switching Module

ALARM	COMMENT
Critical Fire	See fire alarm manual to activate fire sensing device.
Fire Alarm Trouble	See fire alarm manual.
High Temperature	Apply heat to sensor.
Low Temperature	Apply ice near sensor.
Air Dryer	Remove fuse of power ON air dryer.
Door Intrusion	Open door.
Air Conditioner	Remove power at AC disconnect.
Miscellaneous Power	Remove power source. [a]
Miscellaneous Alarms	[a]
Discharge Fuse Fail	Short pins 8 and 9 on one of the circuit breakers.
Low Voltage	If conditions permit, power down all battery charging rectifiers.

	Low voltage alarm will activate when plant voltage is between -48.25 V and -51.25 V. If alarm does not activate when voltage goes below -48.25 V, power up rectifiers and follow procedure. **a**
Rectifier Fail	Power any single rectifier down.
Fuse ALM PDF	Insert blown indicator fuse in at least one fuse position of each fuse block of each power distribution frame (PDF).
Alarm Battery	Insert blown indicator fuse in Alarm Battery Source.
Battery Discharge	Power all battery charging rectifiers down.
Standby	See STBY (standby) PLANT manual.
High Voltage	If rectifiers have been properly balanced, DO NOT try to simulate a high-voltage alarm by altering rectifier control. If conditions permit, increase voltage output of one rectifier enough to raise plant voltage to -53.25 V. If alarm is not activated, then follow procedure described in footnote.
Commercial Power Failure	**a**

Notes:

a. Where possible danger, difficulty, or potential damage to a unit exists when attempting to simulate an alarm condition, locate the scan leads nearest to its sensor and simulate the alarm at that point. Either open the scan lead loop or short scan leads, as applicable. Unfortunately, this method does NOT verify the actual sensing device; but in many cases, it is the safest method.

3.5 OPERATIONS AND MAINTENANCE (O&M) CHECKLIST

Table 3-4 lists O&M checks to be performed on the *5ESS*® switch.

Table 3-4 *5ESS*® Switch O&M Checklist

CHK #	ITEM(s) FOR CHECK	``HOW TO CHECK''	``HOW TO CLEAR''
A. CONTINUOUS CHECKS/MONITORING			
1	Critical alarm	Audible and/or visual alarm present. Observe the STATUS area at the top of the Master Control Center (MCC) display to determine the alarm level (critical, major, or minor) and affected functional area. For additional information, scan the receive-only printer (ROP) for alarmed output messages.	Use Procedure 6.1, Respond to *5ESS*® Switch Alarms, in 235-105-220, *Corrective Maintenance Procedures*, to perform an immediate analysis of the problem and, if repairs are necessary, initiate them without delay. For most ***critical*** failures, analysis and recovery procedures are located in the 235-105-250, *System Recovery* manual. Some examples of critical failures include administrative module (AM) and switching module (SM) initializations, loss of communication to an SM, and craft interface lockout. If automatic system recovery actions are in progress, allow time for them to complete before attempting manual intervention.
2	Major alarm	Audible and/or visual alarms are present. Observe the STATUS area at the top of the MCC display to determine the alarm level (critical, major, or minor) and affected functional area. For additional information, scan the ROP for alarmed output messages.	Use Procedure 6.1, Respond to *5ESS*® Switch Alarms, in 235-105-220, *Corrective Maintenance Procedures*, to perform an immediate analysis of the problem. If repairs are necessary, schedule them as soon as possible (in an hour or so). An example of a problem causing a major alarm is a simplex failure of a critical duplicated unit such as a communication module processor (CMP) or module controller time slot interchanger (MCTSI).

3	Minor alarms	Audible and/or visual alarm present. Observe the STATUS area at the top of the MCC display to determine the alarm level (critical, major, or minor) and affected functional area. For additional information, scan the ROP for alarmed output messages.	Use Procedure 6.1, Respond to *5ESS*® Switch Alarms, in 235-105-220, *Corrective Maintenance Procedures*, to analyze the problem and perform any necessary repairs. This action may be deferred for several hours, but minor alarm conditions should be resolved on at least a daily basis.
B. DAILY CHECKS [a]			
1	Excessive Administrative Module (AM), Switching Module (SM/SM-2000), Communication Module Processor (CMP), or Common Network Interface (CNI) Initializations	Use OMS5 Daily Report or scan the receive-only printer (ROP) printouts for **INIT...** output messages associated with the AM, SM/SM-2000, CMP, CNI, module controller time slot interchanger (MCTSI) or quad-link packet switch gateway processor (QGP). Also scan the ROP for processor recovery messages (PRMs).	Use 235-600-750, *Output Message Manual*, and/or 235-600-602, *Processor Recovery Messages Guide*, to analyze the **INIT** (and related) output messages and/or PRMs. The severity of recovery actions taken during an initialization varies depending on the initialization level (usually identified by the **LVL**= field in the output messages). Low-level initializations take recovery actions such as "return-to-point-of-interrupt" (RPI) or "single-processor-purge" (SPP). Examples of recovery actions taken during high-level initializations include "full process initialization" (FPI), "selective initialization" (SI), and "full initialization" (FI). Refer to 235-105-250, *System Recovery*, for a detailed description of initialization levels. Determine and correct the cause (or "trigger") of the initialization (if not already corrected by automatic initialization recovery actions). Problems that result in low-level initializations should be resolved promptly to avoid escalation to more severe recovery actions.
2	Excessive Interrupts	Use OMS5 Daily Report or scan the ROP printouts for **REPT...** output messages.	Use Procedure 5.7, Analyze and Clear Trouble Causing Excessive Interrupts, in 235-105-220, *Corrective Maintenance Procedures*.
3	Grid fabric failures	Use OMS5 Daily Report or scan ROP printouts for **TST GRID ...STF** or **TST GRIDBD...STF** output messages.	Use Procedure 3.3, Clear LU Grid Exercise Test Failure, in 235-105-220, *Corrective Maintenance Procedures*.
4	Equipment, out-of-service (OOS)	Equipment that is OOS is reflected on the MCC display pages and reported in the OMS5 Daily Report. In addition, some output messages that report the status of OOS units include **OP OOS** , **OP CFGSTAT**, and **OP QNETSTAT**. The corresponding input messages can be used to manually check equipment status. Refer to 235-600-700, *Input Message Manual*, and 235-600-750, *Output Message Manual*, for additional information.	For OOS communication module (CM) units, use Procedure 11.1, Analyze Communication Module Problems, in 235-105-220, *Corrective Maintenance Procedures* to resolve the problem and restore the units to service. For other OOS units/circuits that have failed diagnostics obtained the diagnostic output messages from the ROP and then use Procedure 3.1, Clear Diagnostic Failure in Hardware (Units/Circuits) of *5ESS*® Switch, in 235-105-220, *Corrective Maintenance Procedures*.
5	Lines, OOS	Use OMS5 Daily Report or enter **OP:LIST,LINES;** OOS and check resulting output message.	For each OOS line, use Procedure 7.2, Analyze and Resolve OOS Line List Entries, in 235-105-220, *Corrective*

			Maintenance Procedures.
6	Trunks, OOS	Use OMS5 Daily Report or enter **OP:LIST,TRUNKS;** OOS and check resulting output message.	For each OOS trunk, use Procedure 8.2, Analyze and Resolve OOS Trunk List Entries, in 235-105-220, *Corrective Maintenance Procedures*.
7	Excessive Machine Detected Interoffice (MDII) reports	Use OMS5 Daily Report, the RC/V view, or scan the ROP printouts for **REPT: MDII...** output messages.	Use ROP printouts to identify a specific trunk or Trunk Unit (TU) equipment. For trunk testing, use Procedure 8.1, Perform Trunk Maintenance, in 235-105-220, *Corrective Maintenance Procedures*.
8	Excessive call failure reports (operational, per-call test, or call cutoff)	Use OMS5 Daily Report or scan the ROP printouts for **REPT...** output messages.	Using 235-600-750, *Output Messages Manual*, correlate the reports for specific circuits to be removed and repaired (if this has not already been done). For **REPT ALINK** problems, use Procedure 3.2, Clear A-LINK Failure in Line Unit, in 235-105-220, *Corrective Maintenance Procedures*. For **REPT BLINK** (or **LUCHAN**) problems, use Procedure 3.4, Clear B-LINK or LUCHAN Failure in Line Unit Grid, in 235-105-220, *Corrective Maintenance Procedures*. For **REPT LEN** (or **PCTF**) problems, use Procedure 3.5, Clear LEN Failure in Line Unit Grid, in 235-105-220, *Corrective Maintenance Procedures*. For call cutoffs, the input message **ALW:SCORPT, TRC...** may be helpful.
9	Data base relation REORG failures	Use OMS5 Daily Report or scan the ROP printouts for **REORG NEEDED...** or **CANCELLED...**	Use Procedure 16.7, Perform Manual Reorganization of Hashed Relations With Access Editor, in 235-105-220, *Corrective Maintenance Procedures*.
10	Excessive Asserts or Defensive Check Failures (DCFs)	Use OMS5 Daily Report or scan the ROP printouts for **REPT** output messages. Note that some DCFs (or "asserts") are also reported by **INIT...** output messages.	Use 235-600-500, *Asserts Manual*, and 235-600-750, *Output Messages Manual*, to analyze DCF output messages. Resolve these problems promptly since escalation to more severe automatic recovery actions may result from repeated DCFs.
11	Excessive audit reports	Use OMS5 Daily Report or scan the ROP printouts for **AUD...** output messages.	Use 235-600-400, *Audits Manual*, for possible resolution. If unable to resolve, seek next higher level of technical assistance.
12	ODD Backup failures	Use OMS5 Daily Report or scan the ROP printouts for **BKUP ODD, NRODD|RODD=X (or AM or CMP) ABORTED** output messages.	Try to do the backup again. If it still fails, some data base audits (**OPNDC**, **TRNDC**, or **MEMMAN**) and a **CLR:TRN** may clear the problem. If an assert message (in DAYLOG file) is involved, use 235-600-500, *Asserts Manual*. If unable to resolve, seek next higher level of technical assistance.
13	Manual inhibits of automatic checks and functions	When a normal system function is inhibited, the MCC display reflects this off-normal condition. Some of the input messages that can be used to check for inhibits are: **OP:BREVC**, **OP:ERRCHK**, **OP:HDWCHK**, **OP:OFFNORM**, and **OP:REXINH**.	Unless there is a valid reason for the function to be inhibited, clear each inhibit using the appropriate **ALW:...** input message. If the function is inhibited due to a problem, resolve that problem before clearing the inhibit.
14	Excessive ALE hourly alerts	Use OMS5 Daily Report or scan the	For each line reported, use Procedure

		ROP printouts for **REPT ALE HOURLY ALERT**.	7.13, Digital Subscriber Line Automatic Line Evaluation, in 235-105-220, *Corrective Maintenance Procedures*.
15	Excessive ALE daily alerts	Use OMS5 Daily Report or scan the ROP printouts for **REPT ALE DAILY ALERT**.	For each line reported, use Procedure 7.13, Digital Subscriber Line Automatic Line Evaluation, in 235-105-220, *Corrective Maintenance Procedures*.
C. SCHEDULED TASKS			
□	All scheduled routine maintenance tasks	Per procedures located in Section 2 □ Equipment Test List, 235-105-210, *Routine Operations and Maintenance Procedures*.	Each *5ESS*® switch may have variations of the ETL due to specific hardware and software configurations.

Notes:

a. Use of the OMS5 program is recommended as a time-saver in doing the daily checks 1-15. The OMS5 program can run in the Switching Control Center System (SCCS) and the Total Network Management (TNM) environments. Refer to 235-105-119, *5ESS® Switch Maintenance Guide - Utilizing OMS5-SCC*, or 235-105-130, *5ESS® Switch Maintenance Guide - Utilizing OMS5-TNM*, as appropriate.

3.6 EMERGENCY ACTION INTERFACE (EAI) MAINTENANCE COMMANDS

Table 3-5 lists EAI commands and their resulting actions.

Table 3-5 Emergency Action Interface Maintenance Commands

COMMAND	DESCRIPTION
Commands 10 through 15 have a direct and immediate effect on the system. Some commands force the Administration Module (AM) into a particular configuration and some release a forced configuration.	
10	Inhibits automatic processor recovery switch capability. Forces CU0 to be the on-line processor and CU1 to be the off-line processor. May result in recovery action if CU0 was off-line at time of force.
11	Same as 10, except CU1 is forced on-line and CU0 is forced off-line.
12	Same as 10, except the currently active processor is forced on-line and the other is forced off-line.
13	Removes on-line and off-line forces and allows automatic processor recovery action to determine the on-line and off-line CU.
14	Clears all of the following which may be in effect: forces on- or off-line, sets on primary or secondary disk and timer inhibits.
15 **a**	Initializes all craft interface related processes in the active CU.
Commands 20 through 43 are preparation commands that specify certain conditions prior to a system initialization. These conditions do not take effect until an initialization command is given.	
20	Inhibits automatic processor recovery disk until selection and forces both processors to access their primary disk units on a boot.
21	Removes force on primary disk unit select.
22	Same as 20, except forces the processors to access their secondary disk units.
23	Removes force on secondary unit select.
24	Inhibits the sanity timer from expiring and initiating automatic recovery action.
	Video and to remain displayed until released.
25	Removes the sanity timer inhibit.
26	Releases any trapped failure PRMs (processor recovery messages) and causes the next failure PRM to be displayed in reverse.
27	Releases any trapped failure PRMs and allows further PRMs to be displayed.
28 **b**	Dumps to the display and printer the contents of the buffer in the active CU containing nonfatal error PRMs generated during the most recent processor recovery.
30 **c**	Forces the processor to initialize from the backup root file system.
31 **c**	Allows the processor to initialize from the primary root file system.
32 **c**	Forces the processor to initialize only the *UNIX*® RTR operating system. The application software is not initialized.
33 **c**	Allows the processor to initialize both the *UNIX*® RTR operating system and the application software.
34 **c**	Inhibits hardware checks from initiating automatic recovery action.
35 **c**	Allows the hardware checks to initiate automatic recovery action.
36 **c**	Inhibits software checks from initiating automatic recovery action.
37 **c**	Allows software checks to initiate automatic recovery action.
38 **c**	Inhibits error interrupts.
39 **c**	Allows error interrupts.

40 **c**	Inhibits the use of cache memory.
41 **c**	Allows the use of cache memory.
42 **c**	Allows the setting of a parameter which is made available to application software.
43 **c**	Clears the application parameter.
Commands 50 through 56 are initialization commands. They cause the conditions that were specified previously with commands 20 through 43 to take effect.	
50 **d**	Signals the application software to initialize.
51 **d**	Forces initialization of the duplex *UNIX*® RTR (level 1 initialization).
52 **d**	Forces bootstrap and reloads the *UNIX*® RTR operating system from disk (level 2 initialization).
53 **d**	Same as 52, plus, reloads Equipment Configuration Data (level 3 initialization).
54 **d**	Same as 53, plus, clearing of the memory (level 4 initialization).
55 **d e**	Loads selected disk from tape unit 0.
56 **d e**	Loads selected disk from tape unit 1.

Notes:

a. Command 15 is not operational during DIOP regardless of **OK** or **NG** system response.

b. Command 28 is not supported in the current *UNIX*® RTR operating system software release

c. Commands 30 through 43 generate the next state of the MTTY (maintenance teletypewriter) peripheral control information which is sent to the processor the next time commands 50 through 56 are executed.

d. Commands 50 through 56, in addition to the description given, cause the current next state information to be sent to the processor.

e. Commands 55 and 56 require a CU to be forced on-line (Commands 10, 11, or 12) and a disk unit to be selected (Commands 20 or 22).

3.7 TYPICAL SCAN POINT ASSIGNMENTS - OFFICE ALARMS (REMOTE SWITCHING MODULES)

Tables 3-6 and 3-7 show a typical scan point assignment scheme for office input/output alarms in a remote switching module, respectively.

Table 3-6 Typical Scan Point Assignments, Office Alarms - Remote Switching Module (Alarm Input Option)

SCAN POINT	UNIT/FRAME/CONDITION	ALARM LEAD
SC00	Fire Alarm **a**	Critical
SC01	Fire Alarm Trouble **a**	Major
SC02	High Temperature **b**	Major
SC03	Low Temperature **b**	Major
SC04	Air Dryer Trouble **b**	Major
SC05	Air Conditioner **b**	Major
SC06	Low Voltage **b**	Major
SC07	Low Humidity **b**	Major
SC08	High Humidity **b**	Major
SC09	Door Alarm **b**	Minor
SC10	Window Alarm **b**	Minor
SC11	Carrier Alarm **b**	Minor
SC12 - SC31	**c**	**c**
SC32	Discharge Fuse Alarm **a**	Major
SC33	Inverter Failure Alarm **a**	Major
SC34	Miscellaneous Power Failure Alarm **a**	Major **d**
SC35	Miscellaneous Power Failure Alarm **a**	Major **d**
SC36	Miscellaneous Power Failure Alarm **a**	Minor **d**
SC37	Rectifier Failure Alarm **a**	Major
SC38	Alarm Battery Failure Alarm **a**	Major

SC39	CO Battery Discharge Alarm [a]	Major
SC40	High-Voltage Alarm [a]	Major
SC41	Commercial Power Failure Alarm [a]	Major
SC42	Standby Plant Low-Fuel Alarm [a]	Minor
SC43	Standby Plant Operating Alarm [a]	Major
SC44	Standby Plant Rectifier Failure Alarm [a]	Minor
SC45	Standby Plant Failure Alarm [a]	Major
SC46	Miscellaneous Cabinet Fuse Alarm 0 [a]	Major
SC47	Miscellaneous Cabinet Fuse Alarm 1 [a]	Major
SC48	PDF-0 Fuse Failure Alarm [a]	Major
SC49	PDF-1 Fuse Failure Alarm 1 [a]	Major

Notes:

a. Mandatory assignment.

b. Typical assignment: actual assignment determined by switch owner.

c. Assignment determined by switch owner.

d. Status can be MINOR, MAJOR, or CRITICAL. Switch owner makes decision. Default is MINOR.

Table 3-7 Typical Scan Point Assignments, Office Alarms - Remote Switching Module (Alarm Output Option)

SC/SD	UNIT/FRAME/CONDITION	ALARM LEAD
SC50	ASC/RAU Alarm Active	Info [a]
SC51	ASC/RAU Alarm Test Switch	Info [a]
SC52	ASC/RAU Power Fail	Info [a]
SC53	ASC/RAU Alarm RET Switch	Info [a]
SC54	ASC Alarm Manual Mode Switch	Info [a]
SD100	ASC CTR/RAU Sanity	Info [a]
SD101	ASC SMTBL/RAU EON	Info [a]
SD102	ASC/RAU Building Power	Info [a]
SD103	ASC/RAU Test In Progress	Info [a]
SD104	ASC/RAU Critical Lamp	Info [a]
SD105	ASC/RAU Standard Alarm Lamp	Info [a]
SD106	ASC/RAU Major Lamp	Info [a]
SD107	ASC/RAU Minor Lamp	Info [a]
SD108	ASC OSMAB/RAU ATST	Info [a]
SD109	ASC Manual Mode Lamp	Info [a]
SD110	ASC Critical Audible	Info [a]
SD111	ASC Major Audible	Info [a]
SD112	ASC Minor Audible	Info [a]
SD113	ASC Cycle Timer Inhibit	Info [a]

Notes:

a. These default values cannot be changed.

4. EQUIPMENT

4.1 INTRODUCTION

This section contains information on the physical equipment that makes up the *5ESS*® switch. It has location and identification information that is helpful for switch maintenance.

4.2 EQUIPMENT LOCATIONS

A standard method of locating equipment is to identify an office floor, an aisle on the floor, a module in the aisle (such as AM, SM, or CM), a cabinet (or bay as it is sometimes referred to) in the module, equipment shelves in the cabinet, and circuit packs in the shelves. Further, circuit pack connectors and their respective pin assignments are standard reference points for maintenance procedures.

An aisle (or equipment row) is a series of cabinets arranged for maintenance access at both the front and rear of each unit.

The locations of shelves, circuit packs, and backplane pins within a cabinet are defined by an equipment location (EQL) number.

The EQL number can be used to:

- locate the shelf by specifying the vertical distance from the floor (labeled as "Vertical" in Figure 4-1)
- locate the circuit pack by specifying the horizontal location in the shelf assembly (labeled as "Horizontal" in Figure 4-1), and
- locate the backplane pins by specifying the column and row.

Less than the full EQL may be referenced depending on the level at which the EQL is being used. For example, when a faulty system component is diagnosed, the system prints a Trouble Locating Procedure (TLP) on the Receive Only Printer (ROP). The TLP typically contains information such as floor and aisle, module number, cabinet number, and EQL, all of which can be used to uniquely identify the suspected faulty circuit pack. The EQL in this case typically contains only the vertical and horizontal identifiers. As another example, if the cabinet and vertical identifiers are known, a backplane pin location can be expressed with only the last six digits of the EQL shown in Figure 4-1 .

NOTE: As noted previously, less than the full EQL can be referenced, depending on the level of detail to be conveyed. Conversely, the EQL can be expanded to include the equipment cabinet number.

Figure 4-1 EQL Numbers Defined

4.2.1 CABINET (BAY) DESIGNATIONS

The cabinet designation typically consists of the cabinet abbreviation (for example SMC, LTP, CM) and up to three characters (xxx). (Effective with *5ESS*® switch software release 5E16 and later, all cabinet designations consist of three characters.) For cabinets associated with modules that may contain more than one row of equipment, the first character (**x**xx) designates the equipment row. For instance, an SM-2000 can consist of up to three rows of cabinets, with the SMC cabinet residing in row 0. The valid row designations for an SM-2000 are 0, 1, and 2. The row located across the wiring aisle from row 0 is designated as row 1, and the row on the other side of row 0 is row 2.

NOTE: There are exceptions to these cabinet designation descriptions for cabinets located outside their associated SM equipment lineups (known as noncollocated). For example, noncollocated cabinets containing Multiplex Access Interface Units (XAIUs) have cabinet numbers ranging from 900-999. Also, noncollocated cabinets containing Digital Network Unit - Synchronous Optical Network (DNU-S) units can have cabinet numbers ranging from 1-14, 90-104, and 200-208.

Peripheral units may be connected to the SM-2000 via an Optical Extended Control and Data Unit (OXU) and can be located in a maximum of 3 equipment rows per OXU. Each SM-2000 can support up to 8 OXUs. When an OXU is configured in the primary mode, the first character (**x**, designating the equipment row) is an alpha character. Valid equipment row designations for peripherals connected through an OXU configured in the primary mode are as follows.

OXU Number	Equipment Row Designations
OXU1	A,B,C
OXU2	D,E,F
OXU3	G,H,J
OXU4	K,L,M
OXU5	N,P,Q
OXU6	R,S,T
OXU7	U,V,W
OXU8	X,Y,Z

For OXU1, the equipment row in which the OXU is located is called row A. The row located across the wiring aisle from row A is row B, and the row on the other side of row A is row C. Equipment rows associated with OXU2 through OXU8 are designated similarly.

NOTE: The cabinet number may be omitted for some cabinets (for example, ring node).

4.2.2 SHELF ASSEMBLY LOCATION

The shelf assembly location is referred to as "Vertical" in Figure 4-1 . The Vertical is the first two digits of the EQL printed on the TLP.

The digits represent the vertical distance that the shelf is located from the base of the frame. Vertical increments (of 4 inches) are stamped on the front and rear of the frame uprights. The markings start at the base and range from 00 to 72.

4.2.3 CIRCUIT PACK LOCATION

The circuit pack location is referred to as the "Horizontal" in Figure 4-1 . The Horizontal is the last three digits of the EQL printed on the TLP. Horizontal locations are stamped on the designation strips above the circuit pack apertures. The stamping begins at the front left of the shelf and range from 006 to 184.

EQLs identifying circuit pack locations in integrated services line unit (ISLU) drawer units require a third dimension number. The third number represents the location of the circuit pack in the ``pull-out'' shelf unit. For example, the EQL 49-006-110 identifies the KCD3 line group controller located at shelf number 49, drawer unit at horizontal aperture number 006, and drawer unit circuit pack 110. The third number group

appears in the TLP printout when ISLU faults are addressed.

Horizontal increment numbers are stamped along the bottom of the backplane. When viewed from the back (wiring side) of the backplane, the horizontal increments are counted from right to left beginning at the bottom right.

There is a hinged ``flip-up'' label strip mounted above each shelf unit in a bay. On its front, the strip has a self-adhesive label mounted which contains information about the contents of the shelf unit, such as unit names and service group designations. On its back, the strip also has a label which identifies the unit vertical level, circuit pack locations, and pack identity information. Figure 4-2 illustrates the front and back labels and defines the information. Some of the information is required and some is optional. It is recommended that enough information be present to make the use of the strip worthwhile.

Figure 4-2 Equipment Label

4.2.4 PIN LOCATION

When an EQL includes a printed wiring board pin number, this number is the last three digits of the EQL and they correspond with the same pin code on the backplane. Note that the EQL printed on the TLP typically does not contain the pin location. Each pin field is made up of single-digit column numbers (**z**zz) (0 to 7), read horizontally, and two-digit row numbers (z**zz**) (00 to 56), read vertically. Rows are numbered 00 to 24 upward to the horizontal center line of the shelf and 32 to 56 upward from the horizontal center line. Row numbers 25 through 31 are not generally used as backplane pin locations. They appear in the spaces normally used as ``key zones.'' Figure 4-3 illustrates the pin layout and the means of location.

When viewed from the rear of the backplane, the digits are numbered from right to left beginning with 0. These locations are numbered for both equipped and unequipped pin positions.

When circuit pack connectors contain fewer than the maximum number of pins, pin rows are numbered according to the pin location in the full connector. This numbering convention ensures that the backplane pin numbers and the connector pin numbers agree.

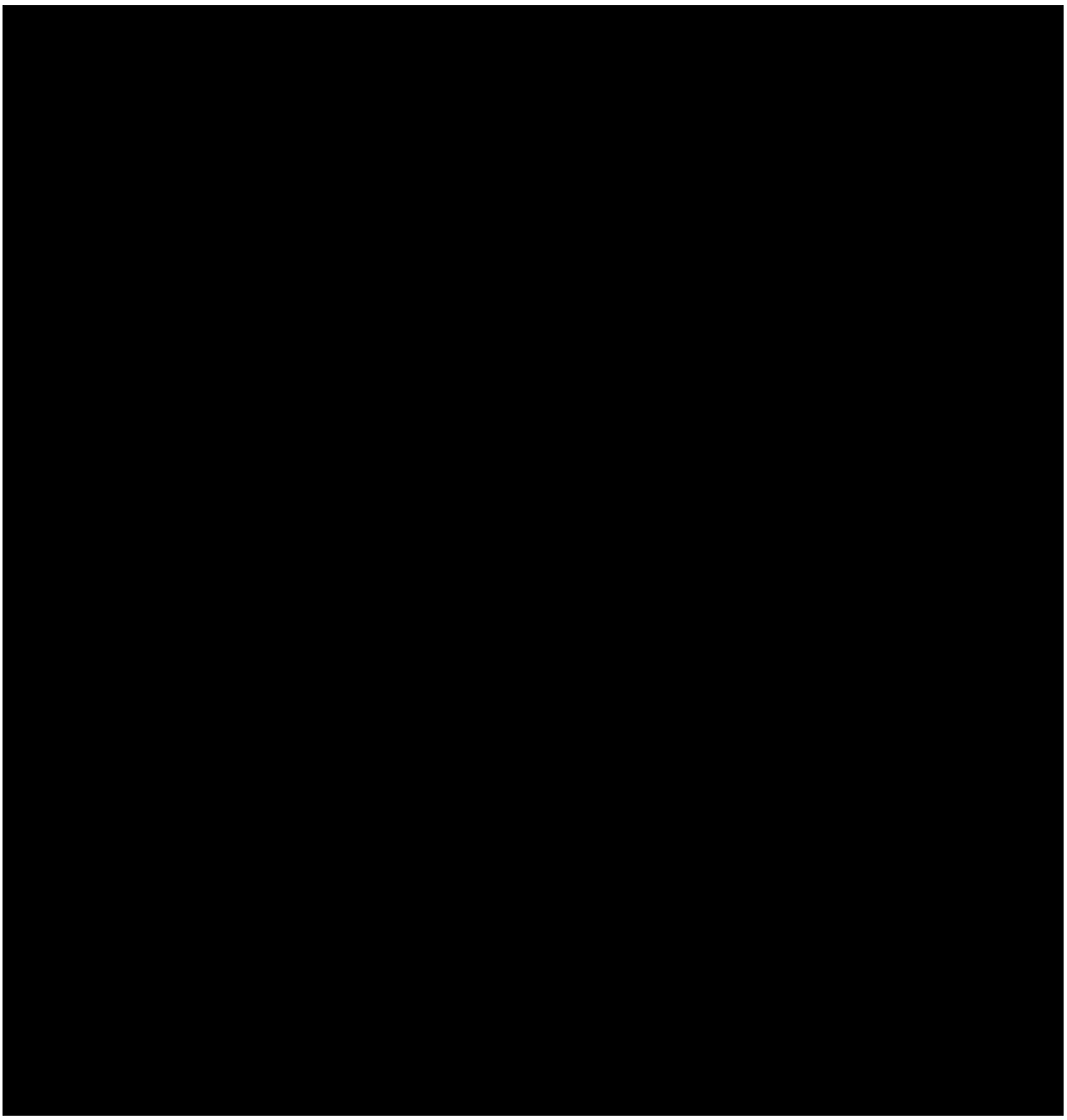

Figure 4-3 Terminal Field Position, Horizontal Row, and Vertical Column Numbers

4.2.5 EXAMPLES

The following three examples explain how to use an EQL to locate specific points of interest.

Examples 1 and 2 are TLPs specifying the location of a faulty circuit pack. Example 3 is a request to locate a specific pin number on a backplane.

Example 1:

See Figure 4-4 for an illustration of Example 1.

When a circuit pack is suspected of a fault, a TLP is printed by the ROP and gives the pack location. This report includes the aisle number, the module number, the cabinet number, and an EQL number or a portion thereof. In this example, the cabinet containing the suspected faulty circuit pack is associated with Switching Module (SM) 1 and is Line Trunk and Peripheral (LTP) cabinet 102. The "1" in "102" portion of the cabinet identifier means that LTP cabinet 02 (the cabinet with the suspected faulty circuit pack) is located in equipment row 1, which is across the wiring aisle from row 0. For detailed identification, the code number of the circuit pack is on the report.

Figure 4-4 Circuit Pack Location - Example 1

Example 2:

See Figure 4-5 for an illustration of Example 1.

When a circuit pack is suspected of a fault, a TLP is printed by the ROP and gives the pack location. This report includes the aisle number, the module number, the cabinet number, and an EQL number or a portion thereof. In this example, the cabinet containing the suspected faulty circuit pack is associated with Switching Module (SM) 12 and is Line Trunk and Peripheral (LTP) cabinet A02. The "A" in "A02" portion of the EQL means that the unit with the suspected faulty circuit pack is connected to an OXU and the primary OXU is OXU1. The "A" also means that the cabinet is located in the same equipment row as the OXU. For detailed identification, the code number of the circuit pack is on the report.

Figure 4-5 Circuit Pack Location - Example 2

Example 3:

See Figure 4-3 for an illustration of Example 3.

To locate a connector pin, use the EQL and the panel stamping on the back of the frame. For example, EQL 016-447 indicates panel stamped pin field 016 and the pin at vertical column 4, row 47.

4.3 CIRCUIT PACKS

4.3.1 INTRODUCTION

Interaction of circuit packs within the switch establishes the capability and reliability of the system. Circuit fault detection, identification, and replacement make up a significant part of switch maintenance. Circuit packs have interchangeable information.

This section contains information about circuit packs; how to identify, handle, install, and replace them.

4.3.2 CIRCUIT PACK IDENTITY CODES

Identity codes consist of an apparatus code, a series number, and a *Common Language*^{TM} CLEI code. There are two types of circuit packs: a microcoded circuit pack that contains firmware and a circuit pack which contains no firmware. This information is screened on the faceplate (which has replaced the tab and latch and is interchangeable). The microcoded circuit pack contains the letters ``MC'' in the alphanumeric firmware identifier located at the top of the faceplate.

Figure 4-6 illustrates examples of the circuit pack identification information screened on the faceplate.

The circuit pack code identifies the type of circuit pack with an alphanumeric designation; for example, TN336. (TN-type pack connectors contain 200 pins in 4 columns and UN-type pack connectors contain 300 pins in 6 columns.)

The series number indicates the hardware level of the circuit pack. For example, ``1'' is located under the carrier pack code on the faceplate.

The CLEI code is the identifier of circuit packs. The code is used mainly for inventory control, but it is also the means of identifying a specific circuit pack during maintenance procedures. The CLEI code appears on a self-adhering label on the circuit pack latch. Information on that portion of the label consists of scannable bar codes plus a readable 10-character CLEI code.

A breakdown of the CLEI code is as follows:

- Characters 1 through 3 describe the family and the subfamily.
- Character 4 is the code type.
- Characters 5 through 7 are a unique identity code.
- Characters 8 through 10 are the manufacturer, supplier, and complementary data.

Figure 4-6 Circuit Packs

The first seven characters (CLEI 7) of the code reflect any changes to a pack. Whenever a new CLEI 7 code is assigned, a new bar code and designation strip are generated.

The circuit pack firmware label appearing on the circuit pack faceplate contains a fourth identifying code

called a MICROCODE (MC) number. The information on the MC label consists of the alphanumeric firmware identification and the firmware issue number; for example, MC4C 001A1 10.

4.3.3 HANDLING CIRCUIT PACKS

4.3.3.1 Cautions

When it is necessary to handle circuit packs, ALWAYS observe the following cautions:

CAUTION 1: Handle circuit packs by their edges or faceplates to avoid deforming components and leads or scratching the gold plated contacts. Damage or contamination can cause poor connections.

CAUTION 2: Before removing or inserting a circuit pack, power down the circuit, unless otherwise specifically directed by a maintenance procedure.

CAUTION 3: Sequential circuit pack removal and replacement is sometimes required. For example, Line Unit circuit packs may require this action (see 235-105-220). Always refer to detailed maintenance procedures if you have any questions about the removal sequence.

CAUTION 4: When changing circuit packs to locate a problem, always restore a circuit pack to its original location if the replacement circuit pack does not clear the fault. This helps isolate the trouble by returning the circuit to the original configuration which existed at the time the failure was first detected.

CAUTION 5: When handling circuit packs, always use care to avoid static discharges. Keep circuit packs in their antistatic shipping containers or some other antistatic environment until inserted. When inserting or removing circuit packs, be properly grounded, using a wrist strap connected to a frame ground or a designated ground connect point.

4.3.3.2 Replacing Circuit Packs

Review the previous cautions for handling circuit packs.

Using information in the MCC, locate the suspected faulty circuit pack.

Most repairs of line and trunk units in switch modules do not need power removal and restoration. However, high-level control units [Control Unit (CU), Disk File Controller (DFC), Input/Output Processor (IOP), Message Switch Control Unit (MSCU), ONTC, Dual Link Interface (DLI), RLI and Modular Controller Time Slot Interchanger (MCTSI)] have a power control/display circuit pack (TN3, TN5, TN6, SN412, SN516, SN1077, etc.) and need unit power down before a circuit pack is removed or replaced.

Figure 4-7 illustrates the controls and indicators on a Control/display circuit pack

If unit power removal is required, perform the following steps:

(1) Move the RST/ROS slide switch to the ROS position and wait for the ROS light-emitting diode (LED) to light.

(2) Wait until the RQIP LED lights, then goes off.

(3) Wait until the Out of Service (OOS) lamp lights.

(4) Press the OFF pushbutton and wait until OFF LED lights.

Unit power is now off.

(5) Open the circuit pack latch and remove the pack. Keep the pack nearby if immediate replacement is

needed.

(6) Verify that the replacement circuit pack is the correct type and issue number.

(7) Inspect the replacement pack for visible defects.

(8) Inspect the contact surfaces and mating connectors for missing gold contacts, bent springs, and any other visible defects.

(9) Carefully align the circuit pack with the upper and lower guide slots.

(10) Insert the circuit pack into the guide slots and seat it by pushing firmly on the tabs located on the faceplate.

Restore power to the unit with the replaced circuit pack by performing the following steps:

(1) Press the ON pushbutton and wait until OFF LED goes off.

(2) Move the RST/ROS slide switch to the RST position.

(3) Wait for the RQIP lamp to light and the OOS and RQIP lamps to go off.

Power is now restored to the unit.

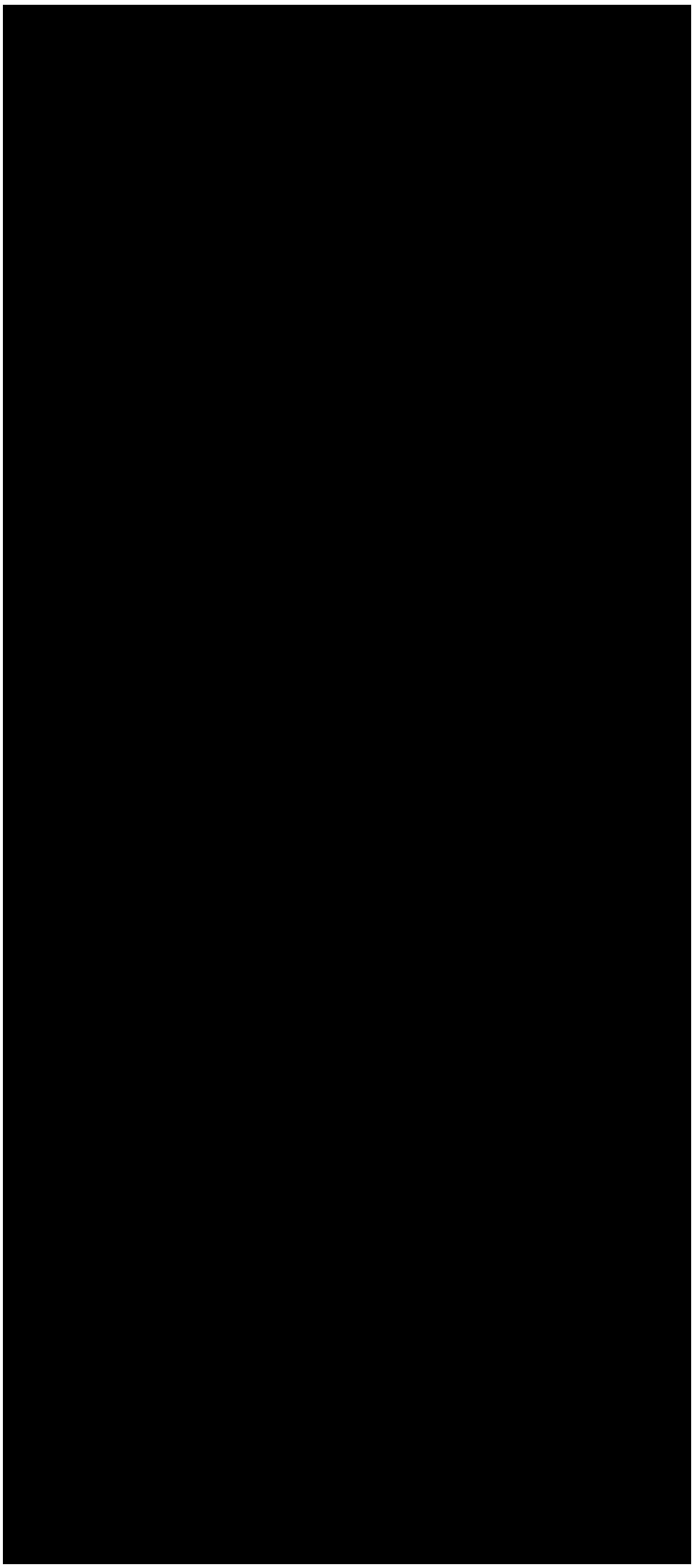

Figure 4-7 Control/Display Circuit Pack

4.4 FANS AND FILTERS

4.4.1 FAN TYPES

Five types of fan assemblies are used in the switching module (SM) bays. The types are shown in Table 4-1 with a figure reference for each.

Table 4-1 SM Fans

ASSEMBLY	ID NO.	USED IN	FIGURE
3 Fans	J5D003BE-X(1-2)	SM Bays	4-7
6 Fans	J5D003BN-X(1-2)	SM Bays	4-8
3 Fans	J5D004AK-1	ISLU Drawers	4-9, 4-10 **a**
6 Fans	J5D003BW-1	SM Bays	4-11 **b**
3/6 Fans	J5D003FH-2	CM2C *5ESS*® cabinets	4-12

Notes:

a. There are two versions of this fan assembly: one manufactured prior to June 1989 and one made since that date. The principal difference between the two versions is access for replacement. In the pre-June version, access is from the bottom of the assembly; in the later version, it is from the top.

b. This fan assembly is required only when there are more than three packet switches mounted in an SM bay. It is an exhaust fan only, requiring no filter, and it mounts in the top of the bay. It is used to supplement the standard bay fans.

4.4.1.1 Fan Assembly J5D003BE-X(1-2)

This is a 3-fan assembly (Figure 4-8) that is generally used throughout all configurations. It is mounted in the bottom aperture of a bay and access to the filter is from the front of the bay.

4.4.1.2 Fan Assembly J5D003BN-X(1-2)

This is a 6-fan assembly (Figure 4-9) that accommodates the addition of packet switches and the module controller time slot interchanger, model 2 (MCTSU2). It is mounted in the bottom shelf position of a bay and access to the filter is from the front of the bay.

4.4.1.3 Fan Assembly J5D004AK-1

This is a 3-fan assembly (Figures 4-10 and 4-11) that is mounted in each integrated service line unit (ISLU) drawer to cool the contents of the drawer. It supplements the 6-fan assembly in the bay. Access to the filter is from the rear of the drawer unit.

The two versions of the drawer fan assembly are as follows:

- One version, manufactured before June 1989, requires access from underneath the drawer to replace a fan.
- The second version, manufactured after June 1989, has access from the top of the drawer.

4.4.1.4 Fan Assembly J5D003BW-1

This is a 6-fan assembly (Figure 4-12) that mounts in the top shelf position of an SM bay containing packet switches. It is an exhaust fan unit required to supplement the standard bay fan assemblies when more than three packet switches are mounted in the bay. It contains no filter.

Figure 4-8 Fan Assembly (3 Fans) - J5D003BE-X (1-2)

Figure 4-9 Fan Assembly (6 Fans) - J5D003BN-X (1-2)

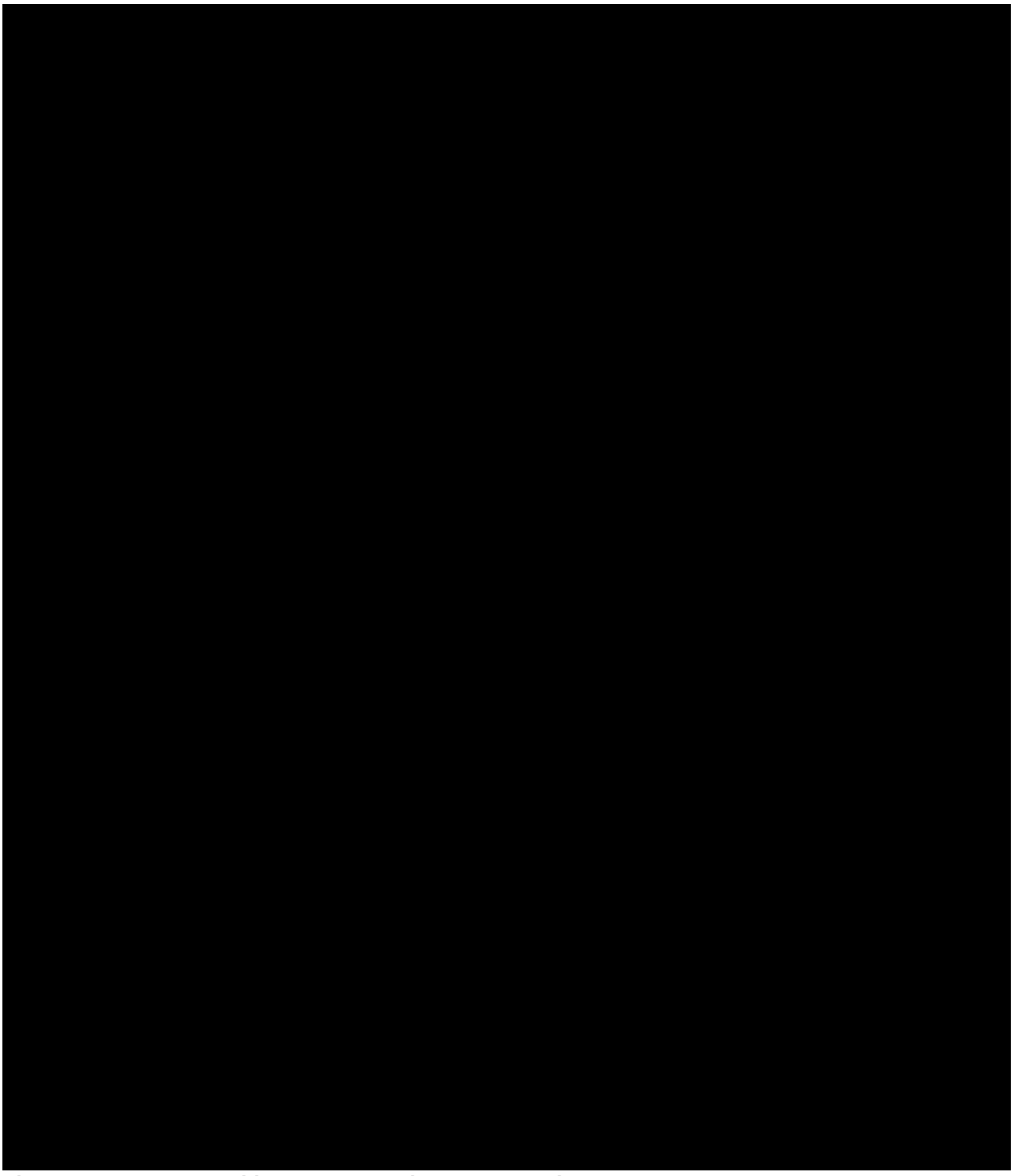

Figure 4-10 Fan Assembly J5D004AK-1 (Pre-June 1989)

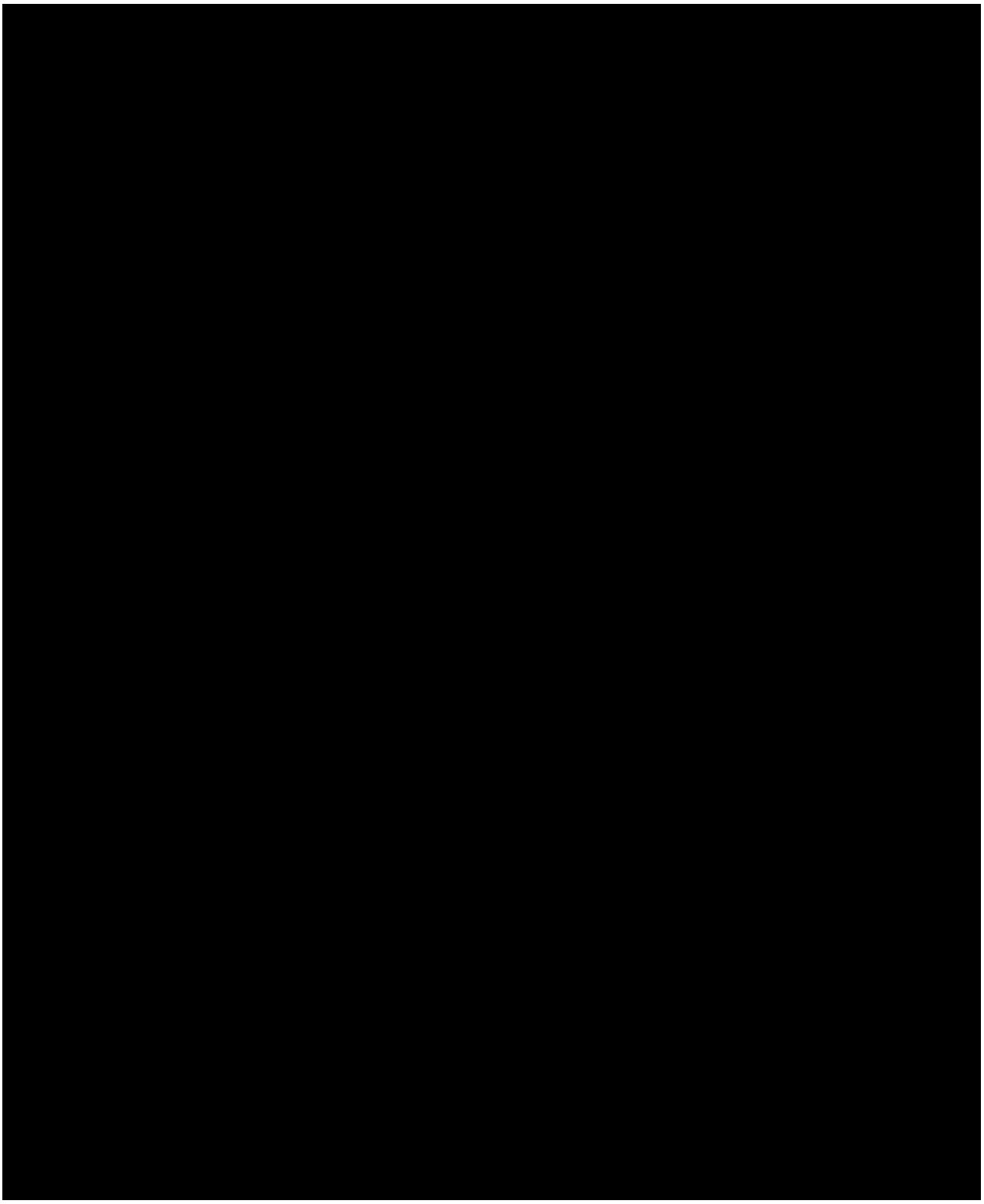

Figure 4-11 Fan Assembly J5D004AK-1 (Post-June 1989)

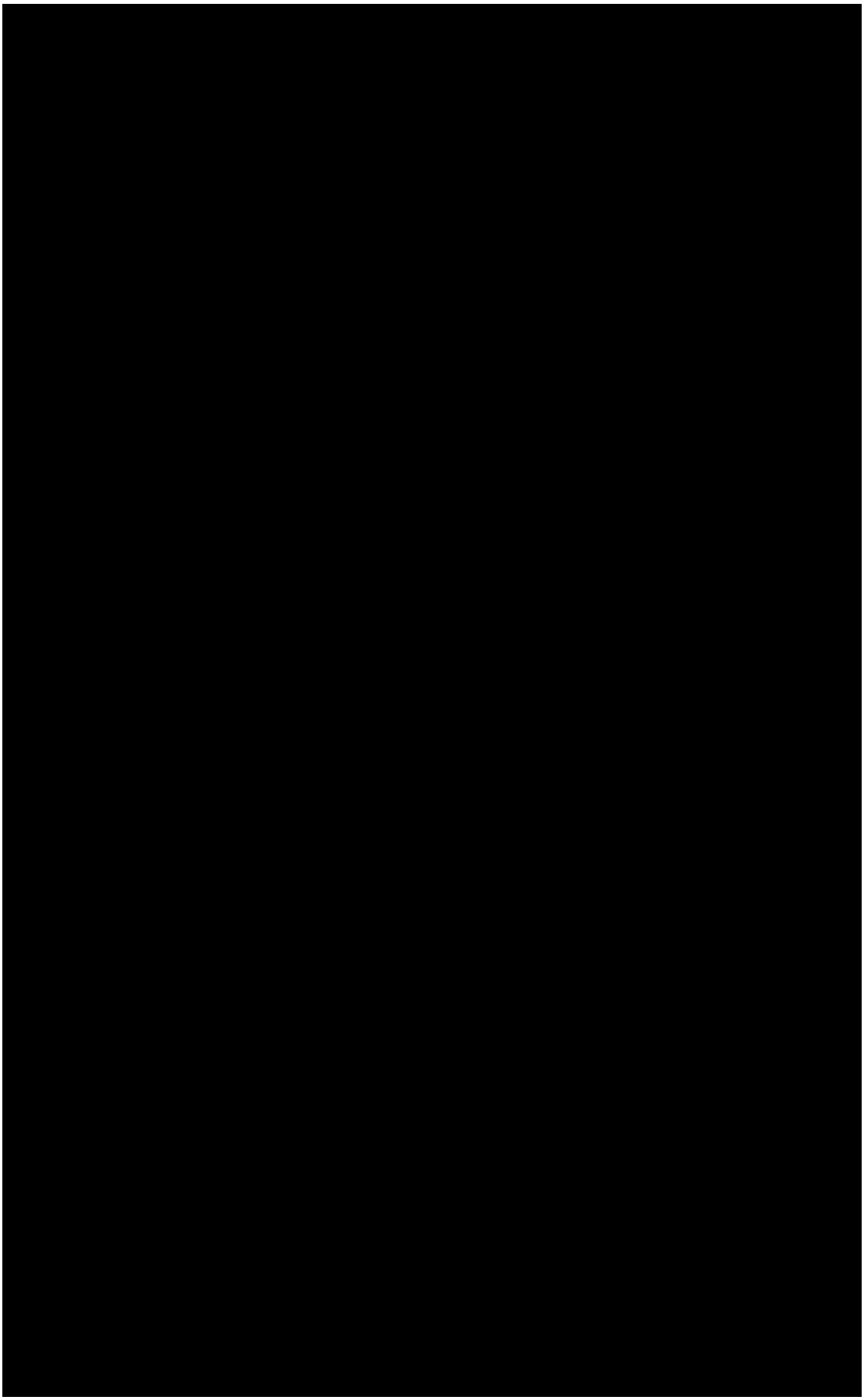

Figure 4-12 Fan Assembly J5D003BW-1 (6-Fan Exhaust)

4.4.1.5 Six-Fan Bi-Directional Mid Fan Unit - J5D003FH-2

This fan unit is located in the middle position of a cabinet. This is a 3- to 6-fan assembly. This fan unit is currently only used with the SM-2000 for additional cooling to the upper and lower shelves. Figures 4-13 and 4-14 show the rear and front views of the fan unit.

Figure 4-13 Fan Assembly (3-6 Fans) Rear View - J5D003FH-2

Figure 4-14 Fan Assembly (3-6 Fans) Front View - J5D003FH-2

4.4.2 GENERAL FAN OPERATION

Once turned on, the fans run continuously at +5 V DC, converted from -48 V DC. Fuses located in the fuse/filter panel may be removed to power down fan assemblies, except for the ISLU drawer fans.

Details for fusing and alarming assignments are shown on the office ED-5D651-15.

Fan performance for the 3-fan, 6-fan, bi-directional fan, and exhaust fan units is monitored by an alarm circuit pack located in the rear of the fan unit. Fan performance for the ISLU is monitored by a 256A alarm circuit pack located on the rear of the fan unit for each ISLU drawer. Other fan units have their own alarm card. Lighted Light Emitting Diodes (LEDs) on the circuit pack identify a defective fan. The LED at the top of the switching module controller (SMC) or the line trunk peripheral (LTP) bay containing the fan also lights.

Powering down a fan unit does not result in an alarm condition. Fan alarm circuits are normally open and close only as a result of a fan malfunction.

Fan malfunctions are indicated by messages at the Master Control Center (MCC) and a major audible alarm. LEDs also light on the fan unit as seen from the rear of the bay and at the top of the bay as seen from the front.

It is not necessary to power down a fan unit to replace a filter except in the ISLU drawers. It is necessary to power down an ISLU fan to replace a filter. Fans in ISLU drawers share fuses with line groups in the

drawers; therefore, DO NOT REMOVE FUSES TO POWER DOWN AN ISLU FAN UNIT. The ISLU drawer/fuse relationship is shown in Table 4-2 .

Table 4-2 ISLU Drawer/Fuse Relationship

	DRAWERS			
FANS	**1**	**2**	**3**	**4**
A	LG3	LG7	LG11	LG15
B	LG2	LG6	LG10	LG14
C	LG1	LG5	LG9	LG13

To remove ISLU fan power, disconnect the upper cable assembly which may prevent removal of the filter (Figure 4-15).

Detailed procedures for filter replacement are found in 235-105-210.

Use fan blockers to restrict contaminated airflow while a filter is being replaced, but do not use fan blockers in fans located at the front of the bay.

Power down any fan unit to replace a faulty fan. When fan replacement is complete, reinsert the fuse (or reconnect the cable on the ISLU fan unit) to restart the unit.

Detailed procedures for faulty fan replacement are found in 235-105-220.

The ISLU alarm pack (256A) must be connected to other ISLUs in the module and to the 3-fan and 6-fan units in the bottom of LTP SMC bays.

Figure 4-15 Rear View of ISLU Drawer Fan Assembly

5. FUNCTIONAL MODULES

This section gives information about the four modules that control the operations of the *5ESS*® switch. Each module section is ``stand alone'' to find information easily.

The four sections are:

Section 5.1 - Administrative Module.

Section 5.2 - Communication Modules.

Section 5.3 - Switching Modules.

Section 5.4 - Common Network Interface.

Table 5-1 - Functional Modules, Unit J Codes and SD Numbers, lists functional modules, module component units and their associated J Codes and Schematic Diagram (SD) numbers. The remaining tables in this section (divided into two types of tables) identify the circuit packs in the functional modules of the switch. For example, Table 5-2 lists the circuit packs present in a complete module and the number of each required to equip the respective units in the module, while Table 5-3 lists the circuit pack contents of an individual unit (identified by J numbers), the number required, and alternate compatible circuit packs, if any, that can be used.

The circuit packs are only those referred to in this document. The tables are not intended to list **ALL** circuit packs for any version of a switch. For variations in local circuit pack requirements, refer to office drawing T-XXXX-DO-3780. (The variable XXXX represents the number applicable to the local office ``T'' drawing.)

Also see ED4C168-14 and ED4C168-17 [Interprocess Message Switch/Common Network Interface (IMS/CNI)] for circuit pack interchangeability information.

Table 5-1 Functional Modules, Unit J Codes and SD Numbers

UNIT NAME	J CODE	SD NUMBER
ADMINISTRATIVE MODULE		
Administrative Module (3B20D Computer)	J1C176C-1	SD4C122-02
Processor Unit Cabinet (3B21D Computer)	J3T060AA-1	SD3T011-01
Growth Unit Cabinet (3B21D Computer)	J3T060AB	SD3T012-01
Power Distribution Unit	J1C147BE-1	SD4C102-01
Central Processor Unit	J1C147BA-1	SD4C098-01
Main Store Input/Output Disk File Controller Unit	J1C147BB-1	SD4C099-01
Main Store Input/Output Growth Unit	J1C147BC-1	SD4C097-01
Cooling Unit	ED-4C387-30	N/A
Port Switch Unit	J1C130BC-1	SD4C065-01
Tape/Disk Cabinet	J1C186A-1	SD4C126-01
Small Computer System Interface (SCSI) Unit	J3T027A	SD3T006-01
SCSI Disk File Controller	J3T027AA	N/A
Computer Peripheral	J3T059A-1	SD3T013-01
Growth Cabinet (3B21D Computer)	N/A	N/A
Computer Processor Cabinet (3B21D Computer)	J3T060A-1	SD3T014-01
Computer Processor Unit (3B21D Computer)	J3T060AA-1	SD3T011-01
Computer Growth Unit (3B21D Computer)	J3T060AB-1	SD3T012-01
Processor Computer System (3B21D Computer)	J3T061A-1	SD3T015-01
Moving Head Disk(s)	KS22483	N/A
MSCU Model 3	J5D020AH-1	SD5D508-01
Tape Drive	KS23113	N/A
Digital Audio Tape	J3T060A-1	N/A
COMMUNICATION MODULES		
Message Switch Cabinet	J5D006C-1	SD5D146-01
Message Switch Control Unit	J5D006AB-1	SD5D026-01
Message Switch Peripheral Unit (Community 1)	J5D006AD-1	SD5D136-01
Message Switch Peripheral Unit (Community 2 and 3)	J5D006AC-1	SD5D126-01
Message Switch Peripheral Unit-Model 3	J5D020AC-1	SD5D078-01
Message Interface Clock Unit	J5D006ED-1	SD5D082-01
Time Multiplex Switch Cabinet	J5D001C-1	SD5D147-01
Time Multiplex Switch Unit	J5D007AB-1	SD5D043-01
Time Multiplexed Switch Unit Model 2	J5D020AD-1	SD5D061-01

Time Multiplexed Switch Unit Model 3	J5D020AG-1	SD5D061-01
Time Multiplex Control Unit	J5D001AA	SD5D037-01
Communication Module - Model 2 (Basic)	J5D020A-1	SD5D140-01
Communication Module - Model 2 (Growth)	J5D020B-1	SD5D140-01
Time Multiplexed Switch Unit Model 2	J5D020AD-1	SD5D061-01
Time Multiplexed Switch Unit Model 3	J5D020AG-1	SD5D191-01
Time Multiplexed Switch Unit Model 4	J5D020C01	SD5D567-01
Communication Module Control Unit	J5D020AA-1	SD5D060-01
Message Switch Control Unit-Model 2	J5D020AB-1	SD5D077-01
Message Switch Control Unit-Model 3	J5D020AH-1	SD5D508-01
Message Switch Peripheral Unit-Model 3	J5D020AC-1	SD5D078-01
Communication Module-Model 2 (Basic)	J5D020A-1	SD5D140-01
Communication Module-Model 2 (Growth)	J5D020B-1	SD5D140-01
Communication Module Control Unit	J5D020AA-1	SD5D060-01
Communication Module Processor Unit	J5D020AF-1	SD5D178-01
Communication Module Unit	J5D020AJ-5	SD5D513-01
Communication Module Unit Model 2	J5D020C01	SD5D568-01
E Bus Unit	J5D020E-1	N/A
SWITCHING MODULES		
FIU Module 3 (supports RSMs)	J5D003AP-3	SD5D401-02
Switching Module Control Cabinet	J5D003E-1	SD5D118-03
TRCU (supports ORMs)	J5D003ED-2	SD5D118-03
Switching Module Control Cabinet	J5D003L-1	SD5D160-01
Remote Control Unit (supports RSM)	J5D003FC-1	SD5D075-01
Digital Line Trunk Unit (RISLU)	J5D003FF-1	
Line Trunk Peripheral Unit	J5D003F-1 or F-2	SD5D119-01
Basic Digital Carrier Unit - Model 2	J5D003AR-2	SD5D202-01
Supplementary Digital Carrier Unit - Model 2	J5D003AS-2	SD5D203-02
Digital Service Unit (Local or Global)	J5D003AE-1	SD5D035-01
Digital Service Unit - Model 2	J5D003EA-1	SD5D042-01
Digital Service Unit - Model 2 (RAF & ISTF)	J5D003EA-1	SD5D092-01
Digital Service Unit - Model 3	N/A	N/A
Modular Metallic Service Unit	J5D003BD-1	SD5D015-01
Directly Connected Test Unit	J1P023AM-1	SD2P077-01
Memory Expansion Unit	J5D003BH-1	SD5D048-01
Module Controller Time Slot Interchanger	J5D003EC-1	SD5D094-01
Line Unit - Model 2	J5D004AC-2	SD5D052-01
Line Unit - Model 3	J5D004AD-1	SD5D180-01
Digital Line Trunk Unit (DLTU)	J5D003AD-1	SD5D205-01
Digital Line Trunk Unit - Model 2 (DLTU2)	J5D024AA-1	SD5D5xxxx
Analog Trunk Unit	J5D003AC-1	SD5D300-01
Switching Module Control Cabinet	J5D003L-1	SD5D160-01
Integrated Digital Carrier Unit	J5D003FL-1	SD5D301-01
Integrated Services Line Unit	J5D004AK-1	SD5D091-01
Digital Service Unit - Model 2 (RAF & ISTF)	J5D003EA-1	SD5D092-01
Packet Switch Unit	J5D003BL-1	SD5D074-01
Module Controller Time Slot Interchanger - (Model 2)	J5D003LA-1	SD5D151-01
Module Controller Time Slot Interchanger - (Model 3)	J5D003LB-1	SD5D536-01
Switch Module Processor 2	J5D003AY-1	SD5D129-01
Digital Network Unit-SONET	J5D003FR-1	SD5D525-01
5ESS® Switch Cabinet	J5D003N-1	SD5D198-01
TSIU4	J5D003NB-1	SD5D196-01
SMPU4	J5D003NA-1	SD5D195-01
DSU3	J5D003NC-1	SD5D197-01
COMMON NETWORK INTERFACE (CNI)		
CNI Cabinet [Small Scale Integration (SSI)]	J3F011C-1	
Group 00:		
□Shelves Positions 0 and 1	J3F011AA	SD3F008-01
□Shelf Position 2	J3F011AC	SD3F010-01
Group 32:		
□Shelves Positions 3 and 4	J3F011AA	SD3F008-01
□Shelf Position 5	J3F011AC	SD3F010-01
CNI Cabinet [Integrated Ring Node Version 2 (IRN2)]	J3F011C-2	SD3F020-01
Group 00, 01, 02:		
□Shelf Position 0	J3F011GD	SD3F067-01
□Shelf Positions 1 and 2	J3F011GC	SD3F066-01
Groups 32, 33, 34:		
□Shelf Position 4	J3F011GD	SD3F067-01
□Shelf Positions 5 and 6	J3F011GC	SD3F066-01
Digital Facility Access (DFA) Cabinet	J3F010F1	SD3F027-01
Digital Service Unit	J3F010BE-1	
Digital Service Adapter Unit	J3F010BA-1	

Table 5-2 Administrative Module (AM) Circuit Packs (3B20D)

CIRCUIT PACK CODE	FUNCTION	UNITS [a] CPU	IOPBU	IOPGU	IOPDFCU	PSU
TC5	Power Control	1				
TF2	Scanner Signal Distributor Interface					1
TF4	Port Switch					2
TN3B	Disk File Controller Power Control				1	
TN5B	Power Control	1				
TN6	I/O Power Controller		1			
TN9	Power Converter		2	2		
TN10	Emergency Act Interface	1				
TN14	Microcontrol Store B				1	
TN56	Main Store Array			8	8	
TN61B	Peripheral Interface Controller		1	1		
TN64B	Duplex Dual Serial Bus Selector				1	
TN68	Microcontrol A				2	
TN69B	Duplex Serial Bus Selector		1	1		
TN70B	Bus Interface Controller		1		1	
TN74B	TTY Peripheral Controller		1	1		
TN83B	Maintenance Terminal Controller		1	1		
TN84B	Microcontrol Store		1	1		
TN983	Maintenance Terminal Controller		1	1		
TN2012	Main Store Array			8	8	
UN1C	Data Manipulation Unit 0	1	1			
UN2B	Special Register 0	1	1			
UN3B	Special Register 1	1	1			
UN3C	Special Register 1	1				
UN6B	Store Data Control	1				
UN9B	Dual Serial Channel			4	1	
UN10B	Cache Memory Controller	2				
UN10C	Cache Memory Controller	2				
UN11C	Cache Memory	1				
UN15B	Microlevel Test Set	1				
UN19B	Dual Serial Channels			4		
UN21B	Utility Circuit	1				
UN23C	Data Manipulation Unit	1				
UN25B	Selectable Microprocessor Interface		2			
UN28B	Maintenance Channel	1				
UN33D	Maintenance Channel		8			
UN43C	Store Address Control	1				
UN43D	Store Address Control	1				
UN45B	Store Address Control	1				
UN45C	Store Address Control	1				
UN46C	Direct Memory Access				3	
UN48B	4KWMS	3				
UN55	Disk File Controller Interface				1	
UN59C	Main Store Controller				1	
UN64	Peripheral Disk Interface				1	
UN133	Main Store Update	1				
UN133B	Main Store Update	1				
UN139	MC4C	1				
UN245	Special Register 1	1				
195FA	Power Unit	2		2	2	

Notes:

a. Legend:

CPU Central Processor Unit

IOPBU Input/Output Basic Unit

IOPGU Input/Output Growth Unit MAS Growth

IOPDFCU Input/Output Disk File Controller

PSU Port Switch Unit

Table 5-3 AM Central Processor Unit J1C147BA-1 Circuit Packs (3B20D)

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
195FA	Power Unit	2	-
TC5	Power Control	1	-
TN5B	Power Control	1	-
TN10	Emergency Act Interface	1	-
UN1C	Data Manipulation Unit 0	1	-
UN2B	Special Register 0	1	-
UN3B	Special Register 1	1	-
UN3C	Special Register 1	1	-
UN6B	Store Data Control	1	-
UN10B	Cache Memory (Controller)	2	-
UN10C	Cache Memory (Controller)	2	-
UN11C	Cache Memory	1	-
UN15B	Microlevel Test Set	1	-
UN21B	Utility Circuit	1	-
UN23C	Data Manipulation Unit 1	1	-
UN28B	Maintenance Channel	1	-
UN43C	Store Address Control	1	-
UN43D	Store Address Control	1	-
UN45B	Store Address Translator	1	-
UN45C	Store Address Translator	1	-
UN48B	4KWMS	3	-
UN133	Main Store Update	1	-
UN133B	Main Store Update	1	-
UN139	MC4C	1	-
UN245	Special Register 1	1	-

Table 5-4 AM Input/Output Basic Unit J1C147BD-1 Circuit Packs (3B20D Computer)

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
494G1	Power Unit Controller	1	-
495FA	Power Unit	2	-
TN6	I/O Power Controller	1	-
TN9	Power Converter	2	-
TN61B	Peripheral Interface Controller	1	-
TN69B	Duplex Serial Bus Selector	1	-
TN70B	Bus Interface Controller	1	-
TN74B	TTY Peripheral Controller	1	-
TN83B	Maintenance Terminal Controller	1	TN983
TN84B	Microcontrol Store	1	-
TN983	Maintenance Terminal Controller	1	TN83B
UN25B	Selectable Microprocessor Interface	2	-
UN33D	Peripheral Controller	8	-

Table 5-5 AM Input/Output Growth Unit J1C147BC-1 Circuit Packs (3B20D Computer)

CIRCUIT PACK CODE	NAME	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
195FA	Power Unit	2	-
TN9	Power Converter	2	-
TN28	Main Store Array	8	TN56
TN56	Main Store Array	8	TN28
UN9B	Dual Serial Channels	4	UN19B
UN19B	Dual Serial Channels	4	UN9B
a	Peripheral Controllers	8	-

Notes:

a. Various Peripheral Controllers are optional for use in the IOP Growth Unit. For specific local-office assignments, refer to office drawing T-XXXX-DO-3780.

Table 5-6 AM Input/Output Disk File Controller J1C147BB-1 Circuit Packs (3B20D Computer)

CIRCUIT PACK CODE	NAME	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
195FA	Power Unit	2	-
TN3B	Disk File Controller Power Control	1	-
TN14	Microcontrol Store B	1	-
TN28	Main Store	8	TN56
TN56	Main Store	8	TN28
TN64B	Duplex Dual Serial Bus Selector	1	-
TN68	Microcontrol A	2	-
TN70B	Bus Interface Controller	1	-
TN2012	Main Store	8	TN56
UN9B	Dual Serial Channel	1	-
UN46C	Direct Memory Access	3	-
UN55	Disk File Controller Interface	1	-
UN59C	Main Store Controller	1	-
UN64	Peripheral Disk Interface	1	-

Table 5-7 AM Port Switch Unit J1C130BC-1 Circuit Packs (3B20D Computer)

CIRCUIT PACK CODE	NAME	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
TF2	Scanner and Signal Distributor Interface	1	-
TF4	Port Switch	2	-

Table 5-8 Administrative Module (AM) Circuit Packs (3B21D Computer)

CIRCUIT PACK CODE	FUNCTION	UNITS		
		CU	DFC	IOP
410AA	Power Converter	2	2	8
KBN10	Input/Output Processor			4
KBN15	Direct Memory Access	2		
KLW31	Central Control	2		
KLW40	Memory Module	2		
TN74B	Terminal Controller			27
TN75C	Sync DLC			20
TN82C	X.25 Sync DLC			2
TN983	Maintenance TTY			2
TN1820	IOP Switch			4
TN1821	Control Unit Power Switch	2		
TN2116	Disk File Controller B		2	
UN33D	Scanner and Signal Distributor			13
UN373	Disk File Controller A		2	
UN375	SCSI Disk (MHD)		16	
UN377	Port Switch and Distributor Buffer			1
UN379	Utility Circuit	2		

Table 5-9 AM Processor Unit (Basic) J3T060AA-1 Circuit Packs (3B21D Computer)

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
410AA	Power Converter	5	-
KBN10	Input/Output Processor	1	-
KBN15	Direct Memory Access	1	-
KLW31	Central Control	1	-
KLW40	Memory Module	1	-
TN74B	Terminal Controller	8	
TN75C	Sync DLC	8	
TN82C	X.25 Sync DLC	1	
TN1820	Input/Output Process Power Switch	1	-
TN1821	Control Unit Power Switch	1	-
TN2116	Disk File Controller B	1	-
TN983	MTTY Controller	1	-
UN33D	Scanner and Signal Distributor	7	-

UN373	Disk File Controller A	1	-
UN375	SCSI Disk	4	-
UN377	Port Switch and Distributor Buffer	1	-
UN379	Utility Circuit	1	-

Table 5-10 AM Growth Unit J3T060AB-1 Circuit Packs (3B21D Computer)

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
410AA	Power Converter	2	-
KBN10	Input/Output Processor	1	-
TN74B	Terminal Controller	16	-
TN75C	Sync DLC	16	-
TN1820	Input/Output Power Switch	1	-
UN82C	X.25 Sync DLC	16	-
UN375	SCSI Disk (MHD)	5	-

Table 5-11 Communication Module (CM) Circuit Packs

CIRCUIT PACK CODE	FUNCTION	UNITS [a]													
		CMCU	CMPU	CMU2	EBUS	MICU	MSCU	MSCU2	MSPU	MSPU2	MSPU3	TMCU	TMSU	TMSU2	TMSU4
410AA	-5 V Power Converter	1	1											2	
410CA	-2 V Power Converter													1	
495FB	Power Converter						2	2	1	2	2	2	4		
495G1	Power								1						
495KA	+12 V, +5 V, Power Converter	1				1									
495MA	-2 V Power Converter	1													
KBN1/4	Fabric Board													4	
KBN2	Fabric Controller													2	
MMB100	Oscillator			1											
MMC100	TMS Foundation			2											
MMC101	TMS Expansion														2
MMD100	Message Switch			1											
MMD101	Network Clock and Control			1											
SN412	Power Control and Display	1	1				1	2	1	1	2			1	
SN516	Power Control and Display	1	1				1	2			2			1	
TN61B	Peripheral Interface Controller						1								
TN69B	Duplex Dual Serial Bus Selector							1							
TN70B	Bus Interface Controller						1	1							
UN183	Control Interface	1													
TN242	Fabric Board												8		
TN243	Link Interface												14		
TN244	Shelf Interface												2		
TN245	Sync./Standalone					1									
TN252	Message Link Interface											1			
TN265	TMS Main Board											1			
TN267	Test Board											1			
TN268	TMS Controller (UP)											1			
TN269	TMS Interface											1			
TN270	Clock Interface											1			
TN698	Duplex Dual Serial Bus Selector						1								
TN834	Link Interface					1									
TN835	Link Interface					1									
TN848	Microcontrol Store						2								
TN856	Message Switch Peripheral Processor								2	2					
TN856B	Message Switch Peripheral Processor							2			8				
TN858	Module Message Processor								8						
TN1681	Quad-Link Interface 2												1		
TN1682	Quad-Link Packet Switch												1		
TN1683	Quad-Link Gateway Processor Board	1													

TN1684	Quad-Link Processor Board	1													
TN859	Message Interface					1									
TN860	Message Interface					1									
TN861	Message Interface					1									
TN862	Message Interface					1									
TN870	Message Interface Bus Controller										8				
TN881	Clock Interface	1													
TN882	Control Interface Bus	1													
TN883	Foundation Link Interface													1	
TN884	Time Multiplexed Switch Controller	1													
TN886	Pump Peripheral Controller						1	1	1						
TN888	Quad Link Interface													8	
TN1034	Dual Message Interface	2													
TN1130	Digital Phase Lock Loop					1									
TN1131	Controller					1									
TN1274B	Synchronizer	1													
TN1276	Digital Phase Lock Loop	1													
TN1284	Oscillator	1													
TN1286	Oscillator	1													
TN1368	Communication Module Processor		1						1	1					
TN1369	Memory		1						1						
TN1800	Communication Module Processor		1												
UN25B	I/O Microprocessor Interface						2	4							
UN74	Fanout												2		
UN173	Foundation Peripheral Controller							1	1						
UN178	Peripheral Interface Controller							1							
UN182	Shelf Utility Board													1	
UN186	Dual Message Interface	2													
UN187	Dual Message Interface	1													
UN197	Multiplexer and Controller				1										
UN310	Transmit Data	1			3										
UN311	Transmit Data				3										
UN312	End Clock				1										
UN313	Transmit Clock				1										

Notes:

a. Legend:

CMCU Communication Module Control Unit

CMPU Communication Module Processor Unit

CMU2 Communication Module Unit Model 2

EBUS E Bus Unit

MICU Message Interface Clock Unit

MSCU Message Switch Control Unit

MSCU2 Message Switch Control Unit 2

MSPU Message Switch Peripheral Unit

MSPU2 Message Switch Peripheral Unit 2

MSPU3 Message Switch Peripheral Unit 3

TMCU Time-Multiplexed Control Unit

TMSU Time-Multiplexed Switch Unit

TMSU2 Time-Multiplexed Switch Unit Model 2

TMSU4 Time-Multiplexed Switch Unit Model 4

Table 5-12 CM Control Unit J5D020AA-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
410AA	-5 V A Power Converter	1	
495KA	+12 V, +5 V, Power Converter	1	
495MA	-2 V Power Converter	1	
SN412	Power Control and Display	1	
SN516	Power Converter and Display	1	
TN881	Clock Interface	1	
TN882	Control Interface Bus	1	
TN884C	Time Multiplex Switch Controller	1	
TN1034	Dual Message Interface	2	
TN1274B	Synchronizer	1	
TN1276	Digital Phase Lock Loop	1	
TN1284B	Oscillator	1	
TN1286B	Oscillator	1	
UN183	Control Interface	1	
UN186	Dual Message Interface	2	
UN187	Dual Message Interface	1	
UN310	Transmit Data	1	

Table 5-13 CM Processor Unit J5D020AF-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
410AA	-5 V A Power Converter	1	
SN412	Power Control and Display	1	
SN516	Power Control and Display	1	
TN1368	Communications Module Processor	1	
TN1369	Processor Memory	1	
TN1800	Communications Module Processor	1	
TN1681	Quad-Link Interface 2	1	
TN1682	Quad-Link Packet Switch	1	
TN1683/4	Quad-Link Gateway Processor Board	1	

Table 5-14 CM Unit Model 2 (Global Messaging Server) J5D020C01 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED
MMB100	Oscillator	1
MMB100	Time-Multiplexed Switch Foundation	2
MMD100	Message Switch	1
MMD101	Network Clock and Control	1

Table 5-15 CM E Bus Unit Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
UN197	Multiplexer and Controller	1	
UN198	Loop Around	4	
UN310	End Data	3	
UN311	Transmit Data	3	
UN312	End Clock	1	
UN313	Transmit Clock	1	

Table 5-16 CM Message Interface Clock Unit J5D006ED-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
495KA	+12 V, +5 V, Power Converter	1	
TN245	Synchronization/Standalone	1	
TN834	Link Interface	1	
TN835	Link Interface	1	
TN859	Message Interface	1	
TN860	Message Interface	1	

TN861	Message Interface	1	
TN862	Message Interface	1	
TN1130	Digital Phase Lock Loop	1	
TN1131	Controller	1	

Table 5-17 CM Message Switch Control Unit J5D006AB-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
495FB	Power Converter	2	
SN412	Power Control and Display	1	
SN516	Power Control and Display	1	
TN61B	Peripheral Interface Controller	1	
TN70B	Bus Interface Controller	1	
TN698	Duplex Dual Serial Bus Selector	1	
TN848	Microcontrol Store	2	
TN886	Pump Peripheral Controller	1	
UN25B	I/O Microprocessor Interface	2	

Table 5-18 CM Message Switch Control Unit 2 J5D020AB-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
495FB	Power Converter	2	
SN412	Power Control and Display	2	
SN516	Power Control and Display	2	
TN69B	Duplex Dual Serial Bus Selector	1	
TN70C	Bus Interface Controller	1	
TN856C	Message Switch Peripheral Processor	2	
TN886	Pump Peripheral Controller	1	
UN25B	I/O Microprocessor Interface	4	
UN173	Foundation Peripheral Controller	1	
UN178	Peripheral Interface Controller	1	
UN199	Programmable Microcontroller Store	1	

Table 5-19 CM Message Switch Control Unit 3 J5D020AH-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
SN516B	Message Switch Peripheral Unit Control and Display	1	
495FB	Message Switch Peripheral Unit Converter	1	
TN856C	Message Switch Peripheral Processor	1	
TN886	Pump Peripheral Controller	1	
UN173	Foundation Peripheral Controller	1	
SN516B	Message Switch Control Unit Control and Display	1	
495FB	Message Switch Control Unit Converter	1	
UN25B	I/O Microprocessor Interface	3	
KBN10	IOP2/MSC3	1	

Table 5-20 CM Message Switch Peripheral Unit J5D006AD-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
495FB	Power Converter	1	
SN412	Control and Display	1	
TN856	Message Switch Peripheral Processor	2	
TN886	Pump Peripheral Controller	1	
TN1368	Communication Module Processor	1	
TN1369	Message Switch Memory	1	
UN173	Foundation Peripheral Cont.	1	

Table 5-21 CM Message Switch Peripheral Unit 2 J5D020AB-1 Circuit Packs

CIRCUIT PACK		NUMBER REQUIR	ALTERNATE CIRCUIT

CODE	FUNCTION	ED	PACK
495G1	Power Converter	1	
SN412	Power Control and Display	1	
TN856	Message Switch Peripheral Processor	2	
TN858	Module Message Processor	8	
TN1368	Communication Module Processor	1	
UN170	Module Message Processor	4	

Table 5-22 CM Message Switch Peripheral Unit 3 J5D020AC-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
495FB	Power Converter	2	
SN412	Power Control and Display	2	
SN516C	Power Control and Display	2	
TN856B	Message Switch Periph. Processor	8	
TN870	Message Interface Bus Controller	8	

Table 5-23 CM Time-Multiplexed Control Unit J5D001AA-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
495FB	Power Converter	2	
TN252	Message Link Interface	1	
TN265	TMS Main Board	1	
TN267	Test Board	1	
TN268	TMS Controller (UP)	1	
TN269	TMS Interface	1	
TN270	Clock Interface	1	

Table 5-24 CM Time-Multiplexed Switch Unit J5D001AB-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
495FB	Power Converter	4	
TN242	Fabric Board	8	
TN243	Link Interface	14	
TN244	Shelf Interface	2	
UN74	Fan Out	2	

Table 5-25 CM Time-Multiplexed Switch Unit 2 J5D020AD-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
410AA	-5 V Power Converter	2	
410CA	-2 V Power Converter	1	
KBN1/4	Fabric Board	4	
KBN2	Fabric Controller	2	
SN412	Power Control and Display	1	
SN516	Power Control and Display	1	
TN883	Foundation Link Interface	1	
TN888	Quad-Link Interface	8	
UN182	Shelf Utility Board	1	
TN1681	Quad-Link Interface 2	1	
TN1682	Quad-Link Packet Switch	1	

Table 5-26 CM Time-Multiplexed Switch Unit 3 J5D020AG-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
410AA	-5 V Power Converter	2	
410CA	-2 V Power Converter	1	
495CA	-2 V Power Converter	1	
KBN5	Fabric Board	1	

SN516	Power Control and Display	1	
TN883	Foundation Link Interface	1	
TN888	Quad-Link Interface	8	
TN1681	Quad-Link Interface 2	8	
TN1682	Quad-Link Packet Switch	4	
UN182	Shelf Utility Board	1	

Table 5-27 CM Time-Multiplexed Switch Unit Model 4 (Global Messaging Server) J5D020C01 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED
MMC101	Time-Multiplexed Switch Expansion	2

Table 5-28 Communication Module (CM) Circuit Packs

CIRCUIT PACK CODE	FUNCTION	UNITS	
		CMU	CMPU
410AA	-5 V Power Converter	1	2
KBN10	MSCU3	1	
SN516B	Power Control and Display	1	2
TN856C	Message Switch Peripheral Processor	3	
TN870	Message Interface Bus Controller	1	
TN886	Pump Peripheral Controller	1	
TN1274B	External Synchronizer	1	
TN1276	Digital Phase Lock Loop	1	
TN1284B	High Stability Oscillator	1	
TN1286B	Medium Stability Oscillator	1	
TN1812	CM2C Clock and Control Interface	1	
TN1813	CM2C TMS Controller Board	1	
TN1830	CM2C SMLI Board	1	
TN1369	CMP Memory Board		2
TN1800	CMP Core Board		2
UN173	Foundation Peripheral Controller	1	
UN187	Message Interface Controller	1	

Table 5-29 Communication Module Unit Circuit Packs J5D020AJ-5

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
410AA	-5 V Power Converter	1	
KBN10	MSCU3	1	
SN516B	Power Control and Display	1	
TN856C	Message Switch Peripheral Processor	4	
TN870	Message Interface Bus Controller	2	
TN886	Pump Peripheral Controller	1	
TN1274B	External Synchronizer	1	
TN1276	Digital Phase Lock Loop	1	
TN1284B	High Stability Oscillator	1	TN1286B
TN1286B	Medium Stability Oscillator	1	TN1284B
TN1812	CM2C Clock and Control Interface	1	
TN1813	CM2C TMS Controller Board	1	
TN1830	CM2C SMLI Board	1	
UN173	Foundation Peripheral Controller	1	
UN187	Message Interface Controller	1	

Table 5-30 SM Circuit Packs

		UNITS [a, b, c]																		
		ATU	ISLU	BDC	SDC	DLT	DLT	DGS	DLS	DLS	DSU	DSU	DCT	LU2	LU3	MEU	MCT	MCT	MCT	MMS	PSU

CIRCUIT PACK CODE	FUNCTION		CSU	LU2	LU2	U	U2	U	U	U(M)	2	2(P)	U				U	U2	U3	U	
295FB	Power (-5 V)												1								
299FB	Power (-5 V)												1								
410AA	Power Converter																2				
414AA	Power Converter																	2			
429AA	Power Controller/ Display & Power Converter																				2
494GB	Power Unit	2												2	2						
494LA	Power Converter			2																	
494NA	Power (-12 V)												2								
495D	Power (-150 V)												2								
495FB	Power Converter							2	2	2						2					
495JC	Power Unit		2																		
ANN3B	Digital Facility Interface					10															
ANN4B	*SLC*® Carrier Digital Facility Interface			20	10																
ANN5B	Digital Facility Interface					10															
KBN6	Peripheral Trans-mission Interface																				2
KBN7	Elect. Line Interface																				2
KBN20B or KBN21B or KBN22B	SB20CORE support application pack with 32MB (KBN20B), or with 64 MB (KBN21B), or with 96 MB (KBN22B)																		2d		
SN100	Test Access Circuit	2																			
SN101B	Control Data Interface	2																			
SN215	Equalizer			1	1	1															
SN216	Equalizer			1	1	1															
SN217	Equalizer			1	1	1															
SN218	Equalizer			1	1	1															
SN219	Equalizer			1	1	1															
SN248B	Port Circuit												4								
SN346B	Power			2	1	1	1														
SN422	Controller												1								

SN423	Equipment Access Network												3							
SN516	Control and Display															2				
TN56	Memory														1 4	1 0				
TN128	Digital Service Unit (Common)							2	2											
TN132	Universal Tone Generator								2											
TN133	Universal Code Decoder								1 4											
TN138	Metallic Access																		8	
TN220B	Scan																		2	
TN221	Signal Distributor																		2	
TN234	Universal Conference							2												
TN302	TTF Common							1												
TN303	TTF Tone Generator Board							1												
TN304B	TTF Measure-ment Board							3												
TN305	TTF Common							1												
TN328B	Automatic Line Insulation Test																		2	
TN329	Automatic Line Insulation Test																		2	
TN330	Automatic Line Insulation Test																		2	
TN335C	Channels													8	8					
TN629B	PICB Interface												1							
TN831B	Gated Diode XPoint													2	2					
TN832B	Gated Diode XPoint													2	2					
TN833C or TN1890 [e]	Local Digital Service Unit										2	1 0					4	2		
TN838	Half Grid													1 6	2 0					
TN841	Universal Conference							2												
TN842B	Common Data													2						
TN843	Common Control													2						
TN844	High-Level Service Circuit		6											6	6					
TN871B	Module Processor															2				
TN872	Module Processor															2				
TN873	Module Processor															2				
TN874B	Module Processor															2				
TN875C	Module															2				

	Processor																			
TN876	Data Interface															4				
TN878	Boot-strapper															1				
TN879B	Common Control																		1	
TN880	Gated Diode XPoint Compen-sator																		2	
TN1032	Universal Conference							2												
TN1040	Distant Frame Test Access Circuit																		2	
TN1042B or UN395/ UN395B [f]	Packet Interface																2	2		
TN1048	Half Grid												16	20						
TN1053	Recorded Announce-ment Function										4									
TN1054	Recorded Announce-ment Function										4									
TN1058	Half Grid												16	20						
TN1077E or TN1077F	Dual Link Interface															2	2	2		
TN1081B	Protocol Handler																		16	
TN1082	Control Fanout																		2	
TN1083B	Packet Fanout																		2	
TN1086B	Time Slot Inter-changer Signal Processor															2	2	2		
TN1346	Common Control		2																	
TN1347	Ring Generator		2																	
TN1348	Metallic Access Network		4																	
TN1366B	Protocol Handler																		16	
TN1367	Protocol Handler																		16	
TN1370	Terminal Board																			
TN1374	Memory																12			
TN1376	Memory																12			

TN1377	Data Interface																4	4		
TN1384	Ring Generator		2																	
TN1397	Module Processor															2				
TN1401B	High-Level Service Circuit		6																	
TN1423	Core Board															2				
TN1424	Power Converter																	2		
TN1524	Data Interface																4	4		
TN1527	Module Processor															2				
TN1533	Module Processor															2				
TN1561	Half Grid													20						
TN1611	Digital Facility Interface						10													
TN1612	Digital Facility Interface						10													
TN1637	Digital Service Circuit									2										
TN1670	Loop Side Interface																			4
TN2012	Memory														6	10				
UN71B or UN71C	Control Interface															4	4	4		
UN106	Common Control		2																	
UN120	Control Multi-plexer			2																
UN121	Data Multi-plexer			2																
UN192	Data Fanout																		2	
UN306	Common Control Interface		2																	
UN307	Common Data		4																	
UN322	Common Data and Control													2						
UN359	Common Control Processor																			2
UN515	Processor Core																2			
UN516	Core Support																2			
UN517	Core Support																2			
UN518	Application																2			

Notes:

a. Legend:

ATU Analog Trunk Unit

BDCLU2 Basic Digital Carrier Line Unit 2

DCTU Directly Connected Test Unit

DLTU Digital Line Trunk Unit

DLTU2 Digital Line Trunk Unit 2

DSU2 Digital Service Unit 2

DSU2 (P) Digital Service Unit 2 (Peripheral)

GDSU Global Digital Service Unit

IDCU Integrated Digital Carrier Unit

ISLU CSU Integrated Services Line Unit Common Shelf Unit

LDSU Local Digital Service Unit

LDSU (M) Local Digital Service Unit (Modified)

LU2 Line Unit 2

LU3 Line Unit 3

MEU Memory Expansion Unit

MCTU Module Controller Time Slot Interchanger

MCTU-2 Module Controller Time Slot Interchanger 2

MCTU-3 Module Controller Time Slot Interchanger 3

MMSU Modular Metallic Service Unit

PSU Packet Switch Unit

SDCLU2 Supplementary Digital Carrier Line Unit 2

TTF Transmission Test Facility

b. Access Interface Unit (AIU) circuit packs are listed in table 5-54 due to space considerations.

c. Expansion Access Interface Unit (EAIU) circuit packs are listed in table 5-55 due to space considerations.

d. One pack per service group for a total of 2 packs per MCTU3; same pack code must be equipped in both service groups.

e. For the MCTU3, the Local Digital Service Unit can be either the TN833 or TN1890.

f. For the MCTU3, the Packet Interface can be either the TN1042, UN395, or UN395B.

Table 5-31 Switching Module 2000 (SM-2000) Circuit Packs

CIRCUIT PACK CODE	FUNCTION	UNITS [a]					
		TSIU	SMPU	DSU	DNU-S	PDXU	XAIU
486AA	Power Unit	1-2					
UM74	TSICOM	1					
UM73	DX	1-6					
KLU1	TSIS (Release 1)	1-4					
KLU1	TSIS (Release 2)	1-1 0					
BKD1*	NLI (Release 1)	2-8					
BKD1*	NLI (Release 2)	2-2					

		0					
BKD2*	PLI (Release 2)	0-20			2-24		
BKD3*	ENLI (Release 2)	0-6					
BKD10*	PLI for the PLTU [b]	0-36					
410AA	Power		2				
SN516B	C/D		1				
UN540	Core 40		1				
UN560	Core 60 (Release 2)		1				
TN1685	Memory (Release 2)		1				
KBN8	BSN		1				
UN538	Message Handler		2-4				
UN539	APC		1				
TN1042	PI		1				
UN395	PI2 (Release 2)		1				
UN71B	CI		1				
UN363	DSC3			2			
UN1841	SAS DSC (DSU2)			1			
UN1842	SAS Memory Board (DSU2)			1			
KLU2	Common Controller				2		
KLU3	Common Data				2-4		
KTU1	Transmission Multiplexer				1-14		
KTU2	STSX-1 Facility Interface				2-4		
9822DY	STSX-1 Line Interface				0-12		
982TN	Common Optical Termination				2-24		
	FCD					2	
	PLI					2	
	QCOMDAC						2
	AIU Application Packs						0-20

Notes:

a. Legend:

* Optional

AIU Access Interface Unit

APC Application Control Board

BSN Bus Service Node Board

C/D Control and Display

CI Control Interface

DNU-S Digital Network Unit - SONET

DSC3 Digital Service Circuit - Model 3

DSU Digital Service Unit

DX Data Expansion Board

ENLI Electrical Network Line Interface

FCD Fiber Common Data

NLI Network Link Interface

PDXU Peripheral Control and Timing (PCT) Data Exchanger Unit

PI Packet Interface

PLI Peripheral Link Interface

PLTU Peripheral Control and Timing (PCT) Line and Trunk (virtual) Unit

QCOMDAC Quad Common Data and Control

SMPU Switching Module Processor Unit

TSICOM Time Slot Interchange Common

TSIS Time Slot Interface Slice

TSIU Time Slot Interchange Unit

XAIU Multiplex Access Interface Unit

b. The PLI (BKD10 optical paddle board) provides an optical interface to TSI link(s) through a connection on the TSIU backplane.

Table 5-32 SM Analog Trunk Unit J5D003AC-1 Circuit Packs

CIRCUIT PACK CODE [a]	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
494GB	Power Unit	2	
SN100	Test Access Circuit	2	
SN101B	Control Data Interface	2	

Notes:

a. The following circuit packs can be used in a service group (MAX 8): SN102C, SN103C, SN104, SN105, SN107, SN112, SN113B, SN114, and SN115.

Table 5-33 SM Integrated Digital Carrier Unit J5D003FL-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
KBN6	Periph. Trmsn. Interface	2	
KBN7	Elecl. Line Interface	2	
TN1670	Loop Side Interface	4	
429AA	Power Cont./Displ. & Power Conv.	2	
UN359	Common Control Processor	2	

Table 5-34 SM ISLU Common Shelf Unit J5D004AG-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
495JC	Power Unit	2	
TN844E	High-Level Srv. Circuit	6	
TN1346	Common Control Procr.	2	
TN1347B	Ring Generator	2	
TN1348B	Metallic Access Network	4	
TN1384B	Ring Generator	2	
TN1401B	High-Level Srv. Circuit	6	
UN106	Common Control	2	
UN306	Common Control Interface	2	
UN307	Common Data	4	

Table 5-35 SM Basic Digital Carrier Line Unit 2 J5D003AR-2 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
494LA	Power Converter	2	
ANN4B	*SLC*® Carrier Digital Facility Interface	20	
SN215	Equalizer	1 [a]	
SN216	Equalizer	1 [a]	
SN217	Equalizer	1 [a]	

SN218	Equalizer	1 [a]	
SN219	Equalizer	1 [a]	
SN346B	Power	2	
UN120	Control Multiplexer	2	
UN121	Data Multiplexer	2	

Notes:

a. Determined by engineering requirements.

Table 5-36 SM Supplementary Digital Carrier Line Unit J5D003AS-2 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
ANN4B	*SLC*® Digital Facility Interface	10	
SN215	Equalizer	1 [a]	
SN216	Equalizer	1 [a]	
SN217	Equalizer	1 [a]	
SN218	Equalizer	1 [a]	
SN219	Equalizer	1 [a]	
SN346B	Power	1	

Notes:

a. Only one equalizer required; determined by engineering requirements.

Table 5-37 SM Digital Line Trunk Unit J5D003AD-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
ANN3C	Digital Facility Interface	10	
ANN5C	Digital Facility Interface	10	
SN215	Equalizer	1 [a]	
SN216	Equalizer	1 [a]	
SN217	Equalizer	1 [a]	
SN218	Equalizer	1 [a]	
SN219	Equalizer	1 [a]	
SN346B	Power	1	

Notes:

a. Only one equalizer required; determined by engineering requirements.

Table 5-38 SM Digital Line Trunk Unit 2 J5D024AA-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
SN346B	Power	1	
TN1611B	Digital Facility Interface	10	
TN1612B	Digital Facility Interface	10	

Table 5-39 SM Global Digital Service Unit J5D003AE-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
495FB	Power Converter	2	
TN128	Digital Service Unit (Common)	2	
TN234	Universal Conference	2	
TN302	TTF Common	1	
TN303	TTF Tone Generator Board	1	
TN304B	TTF Measurement Board	3	
TN305	TTF Common	1	
TN841	Universal Conference	2	
TN1032	Universal Conference	2	

Table 5-40 SM Local Digital Service Unit J5D003AE-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
495FB	Power Converter	2	
TN128	Digital Service Unit (Common)	2	
TN132	Universal Tone Generator	2	
TN133	Universal Tone Decoder	14	

Table 5-41 SM Local Digital Service Unit (Modified) J5D003AE-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
495FB	Power Converter	2	
TN1637	Digital Service Circuit	2	

Table 5-42 SM Digital Service Unit 2 J5D003EA-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
TN833	Local Digital Service Unit	2	

Table 5-43 SM Digital Service Unit 2 (Peripheral) J5D003EA-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
TN833	Local Digital Service Unit	4	
TN1053	Recorded Announcement Function	4	
TN1054	Recorded Announcement Function	8	

Table 5-44 SM Directly Connected Test Unit J1P023AM-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
295FB	-5 V Power	1	
299FB	-5 V Power	1	
494NA	-12 V Power	2	
495D	-150 V Power	2	
SN248B	Port Circuit	4	
SN422	Controller	1	
SN423	Equipment Access Network	3	
TN629B	PICB Interface	1	

Table 5-45 SM Line Unit 2 J5D004AC-2 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
494GB	Power Unit	2	
TN335E	Channels	8	
TN831B	Gated Diode XPoint	2	
TN832B	Gated Diode XPoint	2	
TN838	Half Grid	16	
TN842B	Common Data	2	
TN843	Common Control	2	
TN844E	High-Level Srv. Circuit	6	
TN1048	Half Grid	16	
TN1058C	Half Grid	16	

Table 5-46 SM Line Unit 3 J5D004AD-2 Circuit Packs

CIRCUIT PACK		NUMBER REQUIR	ALTERNATE CIRCUIT

CODE	FUNCTION	ED	PACK
494GB	Power Unit	2	
TN335E	Channels	8	
TN831B	Gated Diode XPoint	2	
TN832B	Gated Diode XPoint	2	
TN838	Half Grid	20	
TN844E	High-Level Service Circuit	6	
TN1048	Half Grid	20	
TN1058C	Half Grid	20	
TN1561	Half Grid	20	
UN322	Common Data and Control	2	

Table 5-47 SM Memory Expansion Unit J5D003BH-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
495FB	Power Converter	2	
TN56	Memory	14	
TN2012	Memory	6	

Table 5-48 SM Module Controller/Time Slot Interchanger J5D003EC-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
410AA	Power Converter	2	
SN516	Control and Display	2	
TN56	Memory	10	
TN871B	Module Processor	2	
TN872	Module Processor	2	
TN873	Module Processor	2	
TN874B	Module Processor	2	
TN875C	Module Processor	2	
TN876	Data Interface	4	
TN878	Bootstrapper	1	
TN1077E	Dual Link Interface	2	
TN1086B	Time Slot Interface Signal Processor	2	
TN1397	Module Processor	2	
TN1407(B)	Module Processor	2	
TN1423	Module Processor	2	
TN1527	Module Processor	2	
TN1533	Module Processor	2	
TN2012	Memory	10	
UN71B	Control Interface	4	

Table 5-49 SM Module Controller/Time Slot Interchanger 2 J5D003LA-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
414AA	Power Converter	2	
TN833C or TN1890	Local Digital Service Unit (Digital Service Circuit [a])	4	
TN1042B	Packet Interface	2	
TN1077F	Dual Link Interface	2	
TN1086B	TS Interface Signal Processor	2	
TN1374 or TN1376 or TN1661	Memory	12	
TN1377 or TN1524	Data Interface	4	
UN71B or	Control Interface	4	

UN71C			
UN515B or UN520	Processor Core	2	
UN516B	Core Support 1	2	
UN517C	Core Support 2	2	
UN518	Application	2	

Notes:

a. The LDSU circuit pack also is named the DSC. When LDSU-related software is installed, the DSC circuit pack is named the LDSU.

Table 5-50 SM Module Controller/Time Slot Interchanger 3 J5D003LB-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
KBN20B or KBN21B or KBN22B	SB20CORE	2	
TN833C or TN1890	Local Digital Service Unit (Digital Service Circuit [a])	2	
TN1077F	Dual Link Interface	2	
TN1086B	Time Slot Interchanger/Signal Processor	2	
TN1377 or TN1524	Data Interface	4	
TN1424	Power Converter	2	
UN71B or UN71C	Control Interface	4	
UN395 or UN395B or TN1042B	Packet Interface	2	

Notes:

a. The LDSU circuit pack also is named the DSC. When LDSU-related software is installed, the DSC circuit pack is named the LDSU.

Table 5-51 SM Modular Metallic Service Unit J5D003BD-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
494LA	Power Pack	2	
TN138	Metallic Access Pack	8	
TN220B	Scan	2	
TN221	Signal Distributor	2	
TN328B	Automatic Line Insulation Test Pack	2 **a**	
TN329	Automatic Line Insulation Test Pack	2 **a**	
TN330	Automatic Line Insulation Test Pack	2 **a**	
TN879B	Common Pack	1	
TN880	GDX Compensator Pack	2 **a**	
TN1040	Distant Frame Test Access Circuit	2	
TN1422	Subscriber Line Insulation Measurement Board	1 **a b**	

Notes:

a. Optional

b. Additional boards are permitted

Table 5-52 SM Packet Switch Unit J5D003BL-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
TN1081B	Protocol Handler	1-16	
TN1082B	Control Fanout	2	
TN1083C	Packet Fanout	2	
TN1366B	Protocol Handler 2	1-16	
TN1367	Protocol Handler 3	1-16	
UN192B	Data Fanout	2	

Table 5-53 Digital Network Unit - SONET J5D003FR-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	MAXIMUM	NUMBER REQUIRED
KLU2	Common Controller	2	2
KLU3	Common Data	4	2
KTU1	Transmission Multiplexer	14	1
KTU2	STSX-1 Facility Interface	4	2
9822DY	STSX-1 Line Interface	12	0
BKD2	Peripheral Link Interface	24	2
982TN	Common Optical Termination	24	2

Table 5-54 SM Access Interface Unit (AIU) J8G000AA-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
DAC100	Common Data and Control (COMDAC)	2	
	Application Packs	0-20	

Table 5-55 SM Expansion Access Interface Unit (EAIU) J8G000AA-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
DAC624	Remote Common Data and Control (RCOMDAC)	2	
	Application Packs	0-20	

Table 5-56 SM Peripheral Control and Timing (PCT) Data Exchanger Unit (PDXU) J8G000BA-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
	Fiber Common Data (FCD)	2	
	Peripheral Link Interface (PLI) Paddle Board	2	

Table 5-57 SM Multiplex Access Interface Unit (XAIU) J8G000AA-1 Circuit Packs

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
DAC120	Quad Common Data and Control (QCOMDAC)	2	
	AIU Application Packs	0-20	

Table 5-58 Common Network Interface (CNI) Circuit Packs [Small Scale Integration (SSI)]

CIRCUIT PACK CODE	FUNCTION	UNITS [a]		
		DLN	RPCN	LN
495FA	Power Unit	1	1	1
TN69B	Duplex Dual Serial Bus Selector	1	1	

TN914	3B20D Computer Interface	1	1	
TN915	Padded Interface Buffer		1	1
TN916	Link Interface (Nonencrypted)			1
TN917	Link Interface (Encrypted)			1
TN918	Interframe Buffer (Not always present)	1	1	1
TN922	Node Processor	1	1	1
TN1340	Attached Processor	1		
UN122C	Ring Interface 0	1	1	1
UN123B	Ring Interface 1	1	1	1

Notes:

a. Legend:

DLN Direct Link Node

RPCN Ring Peripheral Controller Node

LN Link Node

Table 5-59 CNI Direct Link Node Unit Circuit Packs, Small Scale Integration (SSI)

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
495FA	Power Unit	1	
TN69B	Duplex Dual Serial Bus Selector	1	
TN914	3B20D Computer Interface	1	
TN918	Interframe Buffer	1	
TN922	Node Processor	1	
TN1340	Attached Processor	1	
UN122C	Ring Interface 0	1	
UN123B	Ring Interface 1	1	

Table 5-60 CNI Ring Peripheral Controller Node Circuit Packs, SSI

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
495FA	Power Unit	1	
TN69B	Duplex Dual Serial Bus Selector	1	
TN914	3B20D Computer Interface	1	
TN915	Padded Interface Buffer (Not Always Present)	1	
TN918	Interframe Buffer (Not Always Present)	1	
TN922	Node Processor	1	
UN122C	Ring Interface 0	1	
UN123B	Ring Interface 1	1	

Table 5-61 CNI Link Node Unit Circuit Packs, SSI

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED	ALTERNATE CIRCUIT PACK
495FA	Power Unit	1	
TN915	Padded Interface Buffer	1	
TN916	Link Interface	1	
TN917	Link Interface	1	
TN918	Interframe Buffer	1	
TN922	Node Processor	1	
UN122C	Ring Interface 0	1	
UN123B	Ring Interface 1	1	

Table 5-62 CNI Circuit Packs, Integrated Ring Node Version 2 (IRN2)

CIRCUIT PACK CODE	FUNCTION	UNITS [a]		
		DLN30	RPCN	LN

410AA	Power Unit	**b**	**c**	**b**, **c**, **d**
TN69B	Duplex Dual Serial Bus Selector	1	1	
TN914	3B20D/3B21D Computer Interface	1	1	
TN916	Link Interface (Nonencrypted with processor outage feature)			1
TN1803	Interframe Buffer		1	**e**
UN304B	Integrated Ring Node Version 2	1	1	1
TN1630C	Attached Processor-30	1		

Notes:

a. Legend:

DLN30 - Direct Link Node 30

RPCN - Ring Peripheral Controller Node

LN - Link Node

b. The DLN30 shares a 410AA power unit with Link Node (LN)-3 and LN-4 on the J3F011GD shelf unit.

c. The RPCN shares a 410AA power unit with LN-1 on the J3F011GD shelf unit.

d. The LNs on the J3F011GD shelf unit (LN-3 and LN-4) share one 410AA power unit with the DLN30. The LNs on the J3F011GC shelf unit share two 410AA power units as follows: LN-1, LN-2, LN-3, and LN-4 share the power unit on the left-hand side of the cabinet (horizontal position 008); LN-5, LN-6, LN-7, and LN-8 share the power unit on the right-hand side of the cabinet (horizontal position 178).

e. For a fully equipped IRN2 CNI Cabinet, LN-4 (on J3F011GD shelf unit) and each LN-8 (on each J3F011GC shelf unit) require one TN1803 Interframe Buffer.

Table 5-63 CNI Direct Link Node 30 Unit Circuit Packs, IRN2

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED
410AA	Power Unit	1 **a**
TN69B	Duplex Dual Serial Bus Selector	1
TN914	3B20D/3B21D Computer Interface	1
TN1630C	Attached Processor-30	1
UN304B	Integrated Ring Node Version 2	1

Notes:

a. The DLN30 shares a 410AA power unit with Link Node (LN)-3 on the J3F011GD shelf unit.

Table 5-64 CNI Ring Peripheral Controller Node Circuit Packs, IRN2

CIRCUIT PACK CODE	FUNCTION	NUMBER REQUIRED
410AA	Power Unit	1 **a**
TN69B	Duplex Dual Serial Bus Selector	1
TN914	3B20D/3B21D Computer Interface	1
TN1803	Interframe Buffer	1
UN304B	Integrated Ring Node Version 2	1

Notes:

a. The Ring Peripheral Controller Node (RPCN) shares a 410AA power unit with Link Node (LN)-1 on the J3F011GD shelf unit.

Table 5-65 CNI Link Node Unit Circuit Packs, IRN2

CIRCUIT		

PACK CODE	FUNCTION	NUMBER REQUIRED
410AA	Power Unit	**a**
TN916	Link Interface	1
TN1803	Interframe Buffer	**b**
UN304B	Integrated Ring Node Version 2	1

Notes:

a. The Link Nodes (LNs) on the J3F011GD shelf unit (LN-3 and LN-4) share one 410AA power unit with the DLN30. The LNs on the J3F011GC shelf unit share two 410AA power units as follows: LN-1, LN-2, LN-3, and LN-4 share the power unit on the left-hand side of the cabinet (horizontal position 008); LN-5, LN-6, LN-7, and LN-8 share the power unit on the right-hand side of the cabinet (horizontal position 178).

b. For a fully equipped IRN2 CNI Cabinet, LN-4 (on J3F011GD shelf unit) and each LN-8 (on each J3F011GC shelf unit) require one TN1803 Interframe Buffer.

5.1 ADMINISTRATIVE MODULE

5.1.1 3B20D COMPUTER - J1C176C-1

The Administrative Module (AM) consists of a Lucent 3B20D - Model 3 computer, a tape disk cabinet, and associated devices (terminals and printers) to control input and output. The 3B21D is necessary to support the SM-2000. Each processor cabinet contains the following shelf assemblies:

- Central Processor Unit
- Main Store, Input/Output Processor, Disk File Controller Unit
- Input/Output Processor Basic Unit
- Input/Output Processor Growth Unit
- Power Distribution Unit
- Port Switch (Cabinet 0 only)
- Cooling Unit.

Figure 5.1-1 illustrates the typical AM and units contained in the Processor Cabinet and Tape/Disk Cabinet.

The 3B20D - Model 3 computer (processor) is in a cabinet separated into Bay 0 and Bay 1. All units are duplicated except the port switch.

This processor performs the central processing functions, controls data flow between the disk drives and the high-speed tape and data flow among other dedicated processors throughout the remaining units.

The tape disk cabinet contains a tape drive and disk units as required for recording, storing, and reading data. Self-diagnostics are run on the tape transport and the fault recovery codes may be displayed as described in Table 5.1-1 .

A typical small computer system interface (SCSI) can be used with the AM and is described in this section.

Figure 5.1-2 illustrates a typical AM (3B20D computer) including the SCSI configuration. Refer to Table 5.1-2 for SCSI controller unit information and bus assignments.

For diagnostic execution input message and POKE command source information, refer to the following documents:

- 235-105-110, *System Maintenance Requirements and Tools*
- 235-105-210, *Routine Operations and Maintenance Procedures*
- 235-105-220, *Corrective Maintenance Procedures*
- 235-600-750, *Output Message Manual*.

Figure 5.1-1 Administrative Module - 3B20D Computer

Figure 5.1-2 Administrative Module - 3B20D Computer (Including SCSI)

5.1.1.1 Central Processor Unit (CPU) - J1C147BA-1

The Central Processor Unit (CPU) is a single-shelf unit with high-speed control functions required by the AM.

All connections between the CPU and the Input/Output (I/O) devices occur over the Central Control Input/Output (CCIO) bus, which connects the CPU to one or two Direct Memory Access Controllers (DMACs) and up to two other I/O positions.

The DMACs provide Direct Memory Access (DMA) to the main store, bypassing the CPU. The I/O positions do not use DMA and communicate with the Main Store (MAS) through the CPU using programmed I/O. The I/O can be application channel interfaces or Dual Serial Channels (DSCHs). Each DMAC can control two DSCHs by way of the Direct Memory Access Input/Output (DIO) bus. Each DSCH can control up to eight devices.

The devices are dual ported to two dual serial channels by way of the Duplex Dual Serial Bus Selector (DDSBS) to give each processor access to all other devices.

The CPU is located at location 60. Figure 5.1-3 illustrates the CPU and the respective circuit packs contained in the unit.

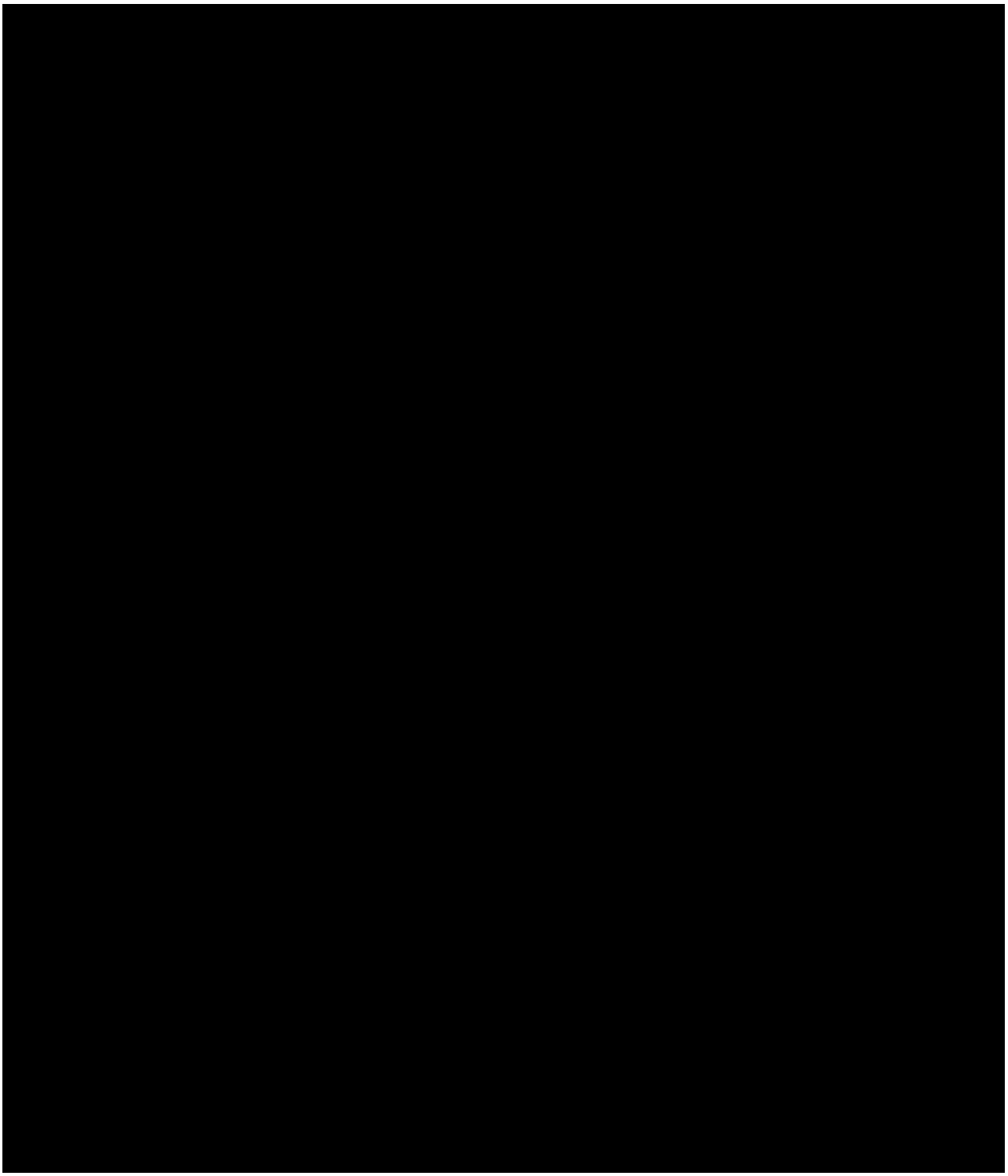

Figure 5.1-3 Central Processor Unit - J1C147BA-1

5.1.1.2 Cooling Unit - ED-4C387-30

Each administrative module processor control unit contains a cooling unit for air circulation for internal equipment (circuit packs, etc.). The cooling unit fans operate on inverted 120 V AC converted from -48 V DC which is supplied directly from the Power Distribution Unit. The input -48 V DC is converted to +5 V DC for alarm circuitry power requirements.

Turning on any of the power control circuit packs in the Processor Control Cabinet (PCC) starts the fans;

they stop if all units in the PCC are powered down.

Fuses are fixed assigned to the power distribution unit in the top of the cabinet.

The cooling unit is alarmed by scan and single-distributor points on Input/Output Process (IOP) units 0 and 1. If a single fan fails, a minor alarm is generated; and the failed fan alarm Light Emitting Diode (LED) lights. The remaining three fans are sufficient to cool the cabinet until failure is corrected. If a multiple fan failure occurs, a major alarm is generated and the failed fan's alarm LEDs light. Fan failures do not automatically shut down the PCC.

Each cooling unit consists of two slide-out drawers, each of which contains two fans, a filter assembly, and power and logic circuitry. The front panel of each drawer has two LEDs (one for each fan), an OFF pushbutton switch to power down both fans, and an ON/RESET pushbutton switch to turn fans on or reset alarm conditions within the unit.

Figure 5.1-4 illustrates the cooling unit for the 3B20D computer (shown with a drawer partially opened) with details of the control panel.

Refer to SD-5D007-01 for dedicated coding scan and SD assignments.

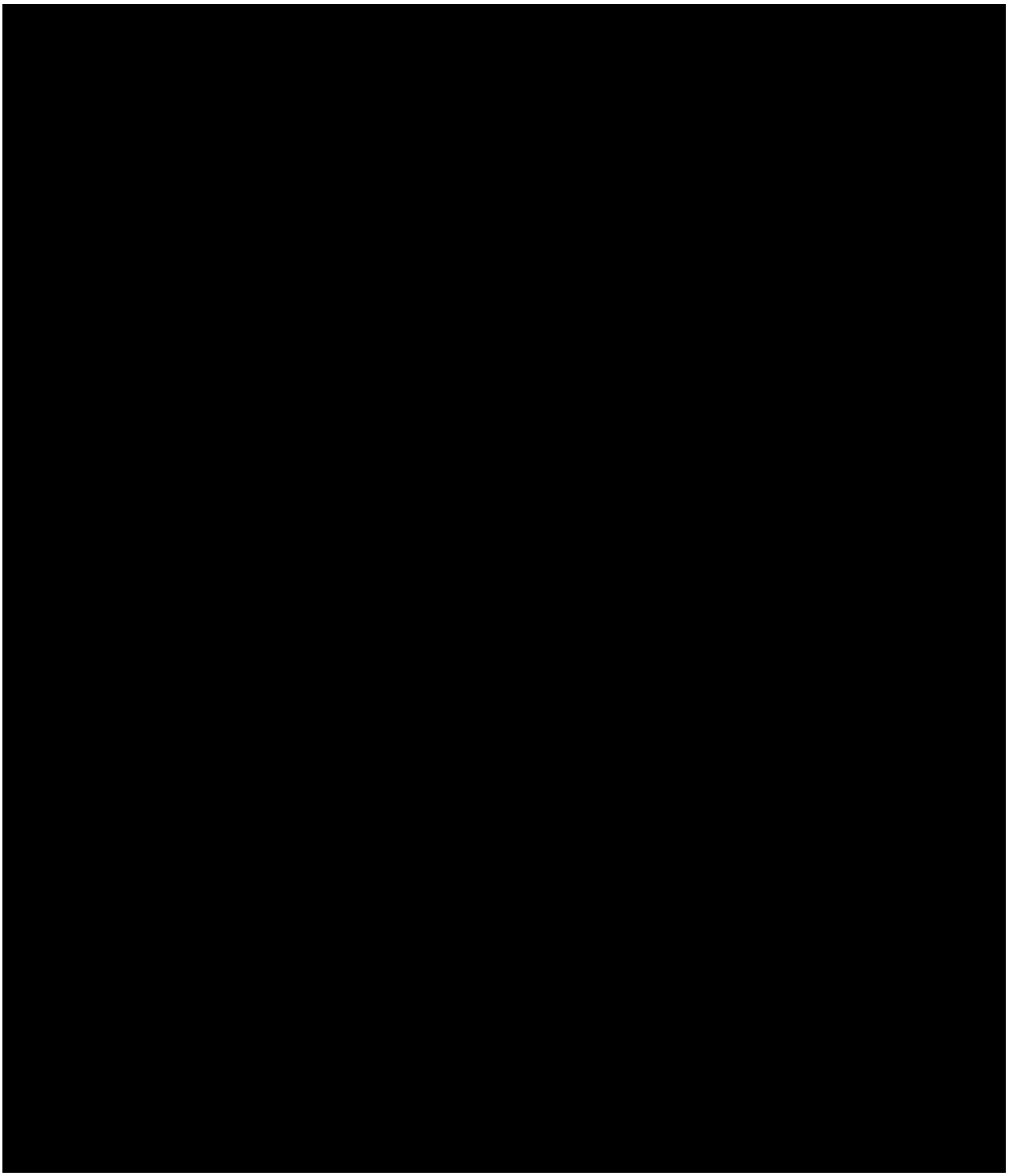

Figure 5.1-4 Cooling Unit - ED-4C387-30

5.1.1.3 Input/Output (Top) Basic Unit - J1C147BD-1

The IOP Basic Unit (IOPBU) is a processor used to control transfers between the Main Store (MAS) and peripheral equipment such as magnetic tape units, terminals, and other slow- and medium-speed peripheral units requiring block transfers of data to and from the MAS. Local and remote terminals requiring connection to the exchange must get access through the IOPBU.

The IOPBU consists of a series of control packs (positions 110 - 175) and two communities [Community 0

(positions 072 - 102) and Community 1 (positions 032 - 042)].

The IOPBU can interface with up to four peripheral communities (0 and 1 on IOP Basic and 2 and 3 on IOP Growth units). Each community consists of four slots numbered 0-3.

The IOPBU is a single-shelf unit mounted at Bay 0 location 36. A duplicate is in Bay 1. Figure 5.1-5 illustrates the IOPBU and the respective circuit packs contained in it.

For assignments of IOP layout, refer to Office Record T-XXXX-DX-3780.

NOTE: The XXXX variable in the ``T'' drawing number represents a specific number assigned to a local office.

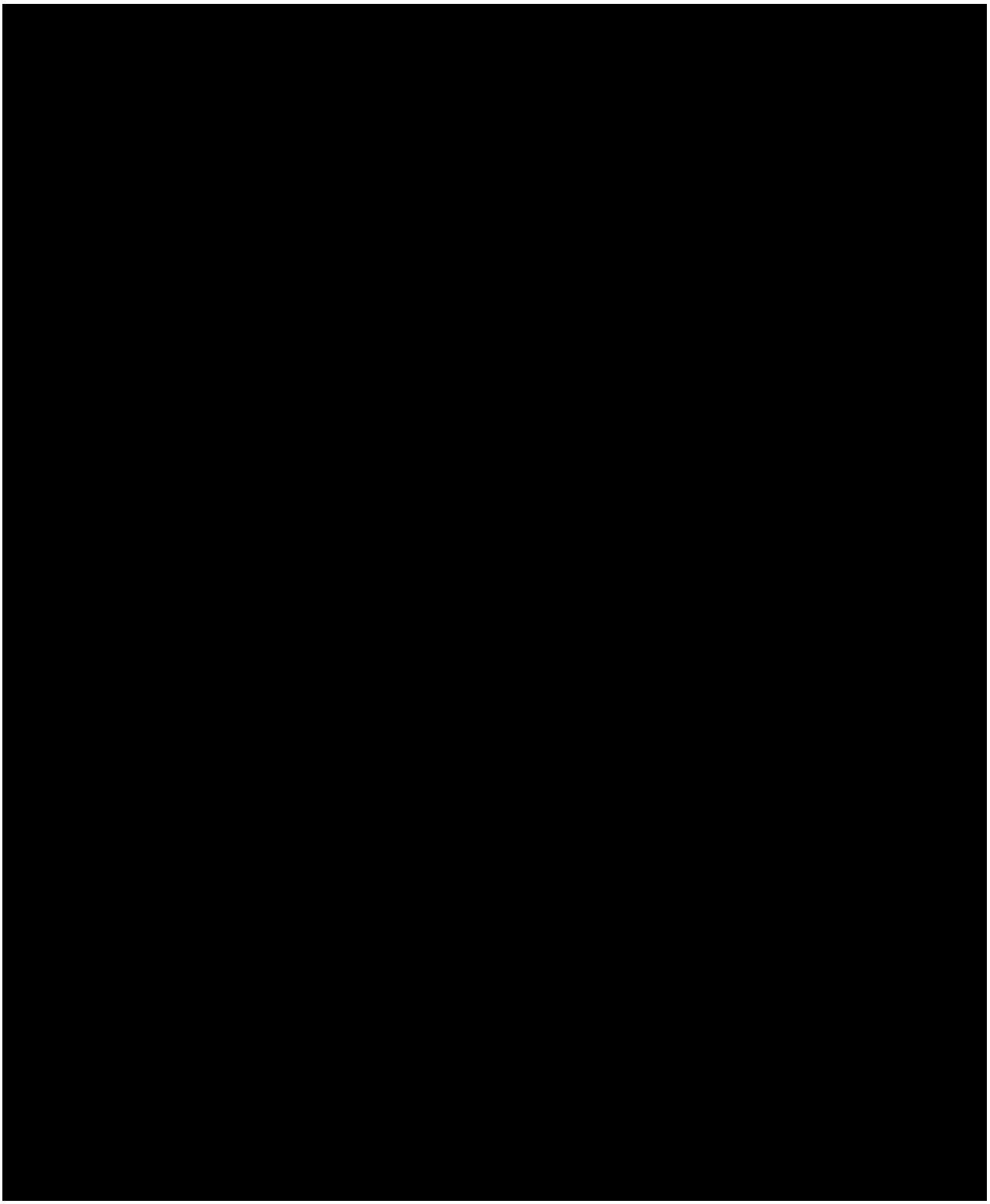

Figure 5.1-5 IOP Basic Unit - J1C147BD-1

5.1.1.4 Main Store Input/Output Growth Unit - J1C147BC-1

The Main Store Input/Output Growth Unit (MASIOPGU) is an optional unit, the need for which is dictated by the required number of addressable memory megabytes on a Main Store (MAS) main unit. The MASIOPGU is a single-shelf unit which mounts in location 42 in Bay 0 of the Administrative Module cabinet. A duplicate unit is mounted in the same location in Bay 1. If a MASIOPGU is not required, a

plenum closes the cabinet space.

The purpose of the unit is to expand the 16-MB capacity of the MAS main unit to a possible 32 megabytes in 2-MB increments. The growth unit has positions for eight additional 2- or 4-MB main store memory array circuit packs; mixing of the two types of memory arrays is not supported.

Figure 5.1-6 illustrates the MASIOPGU and the respective circuit packs contained within it.

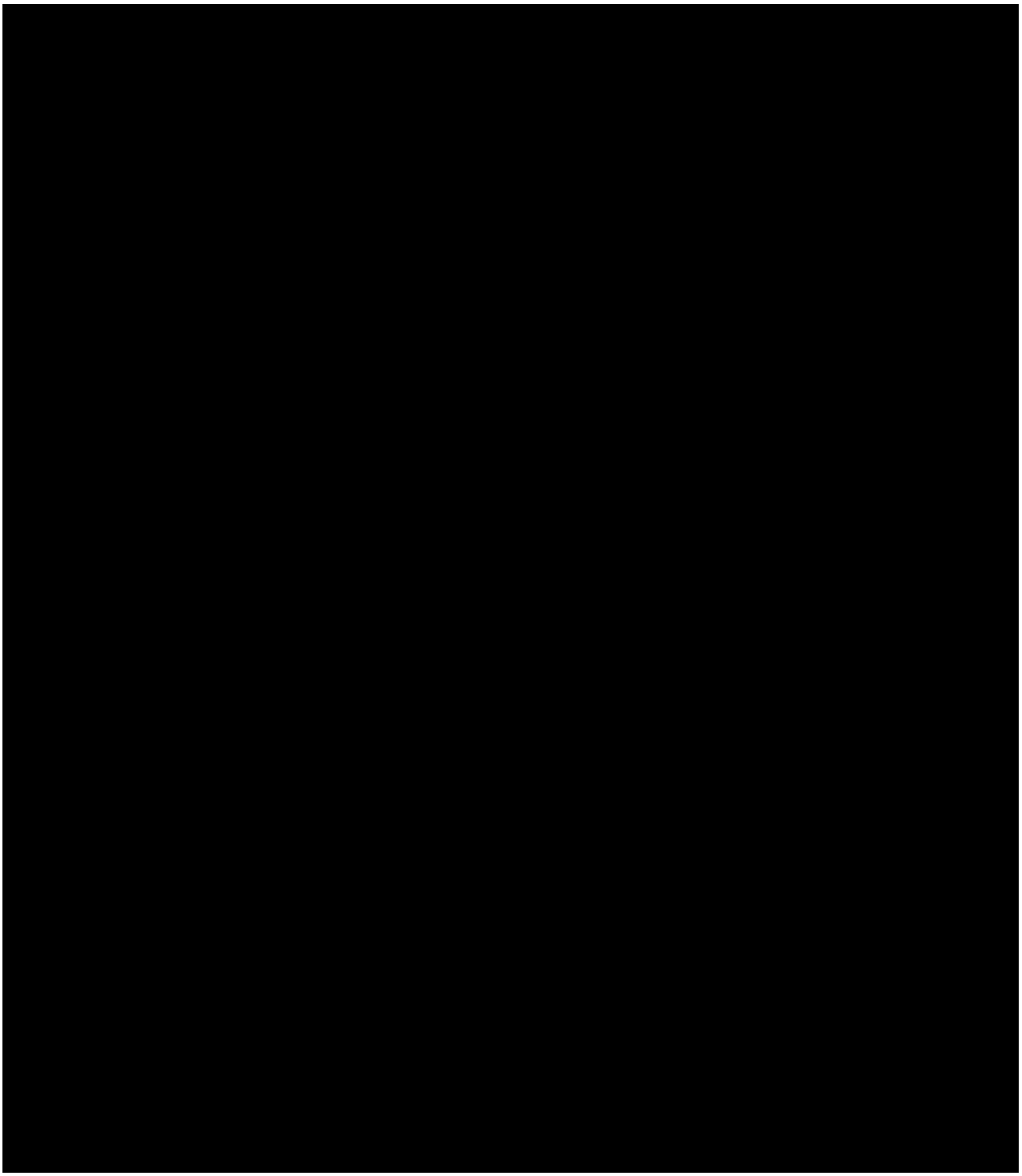

Figure 5.1-6 Main Store Input/Output Growth Unit (3B20D Computer) - J1C147BC-1

5.1.1.5 Main Store Input/Output Disk File Controller Unit (3B20D Computer) - J1C147BB-1

The Main Store Input/Output Disk File Controller Unit (MASIOPDFCU) is a single-shelf unit mounted in location 51 in the Administrative Module (3B20D computer) cabinet, Bay 0. The unit is considered the main unit of the partitioned Main Store (MAS). A duplicate unit is at the same location in Cabinet 1.

The MASIOPDFCU contains the Main Store Controller (MASC) and eight Main Store Arrays (MASAs). The MASC controls access to the MAS and determines multiple store request priorities. It also performs hamming and parity checks.

Each MASA occupies one circuit pack (TN56) and contains 2 megabytes of addressable memory for a possible total of 16 MB per MAS. The capacity may be increased to 32 megabytes (in 2-MB increments) by the addition of a MAS Growth unit.

Figure 5.1-7 illustrates the MASIOPDFCU unit and its respective circuit packs.

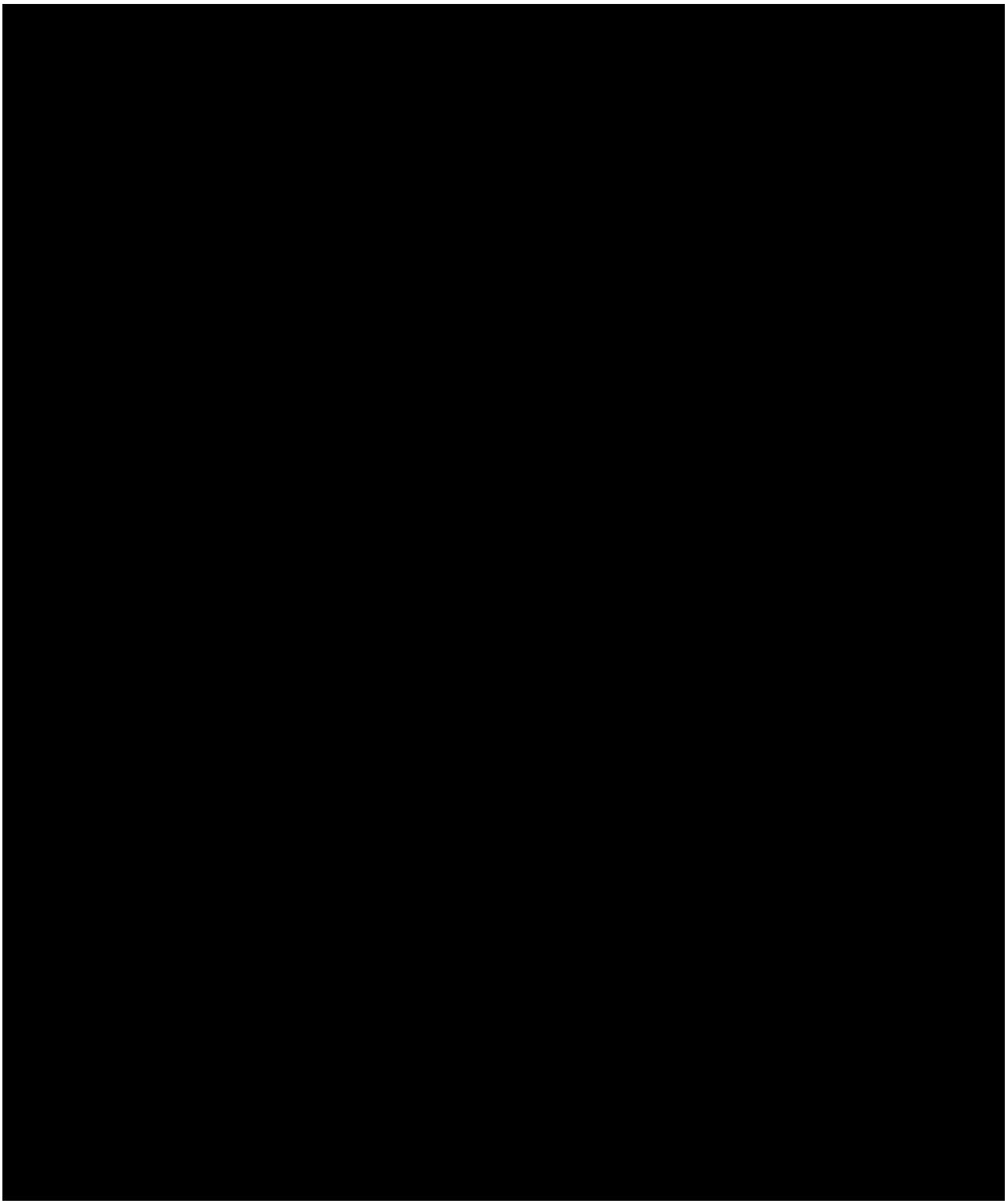

Figure 5.1-7 Main Store Input/Output Disk File Controller Unit (3B20D Computer) - J1C147BB-1

5.1.1.6 Port Switch Unit - J1C130BC-1

The Port Switch Unit (PSU) is a single-shelf unit mounted in location 14 in the Administrative Module (AM) cabinet, Bay 0. A duplicate PSU in Bay 1 is not required.

The PSU is an interface between the Master Control Center (MCC) Teletypewriter (TTY) and printer and the MCC TTY controllers. It ensures that the MCC is always connected to the active controller. The PSU

can be used to select states (ACTIVE or STANDBY) of the TTY controllers. Such selection is useful for testing TTY circuitry and it lets TTY devices operate if a TTY controller fails.

The PSU is equipped with two port switch circuits, one serving the MCC video terminal and the other serving the MCC receive-only printer (ROP). Each associated switch has three settings: 0, 1, or AUTO. Position setting 0 or 1 manually forces the MCC terminal to connect to controller 0 or 1, and the AUTO position setting keeps the terminal connected to the controller associated with the active (0 or 1) side.

Figure 5.1-8 illustrates the PSU and the respective circuit packs contained in the unit.

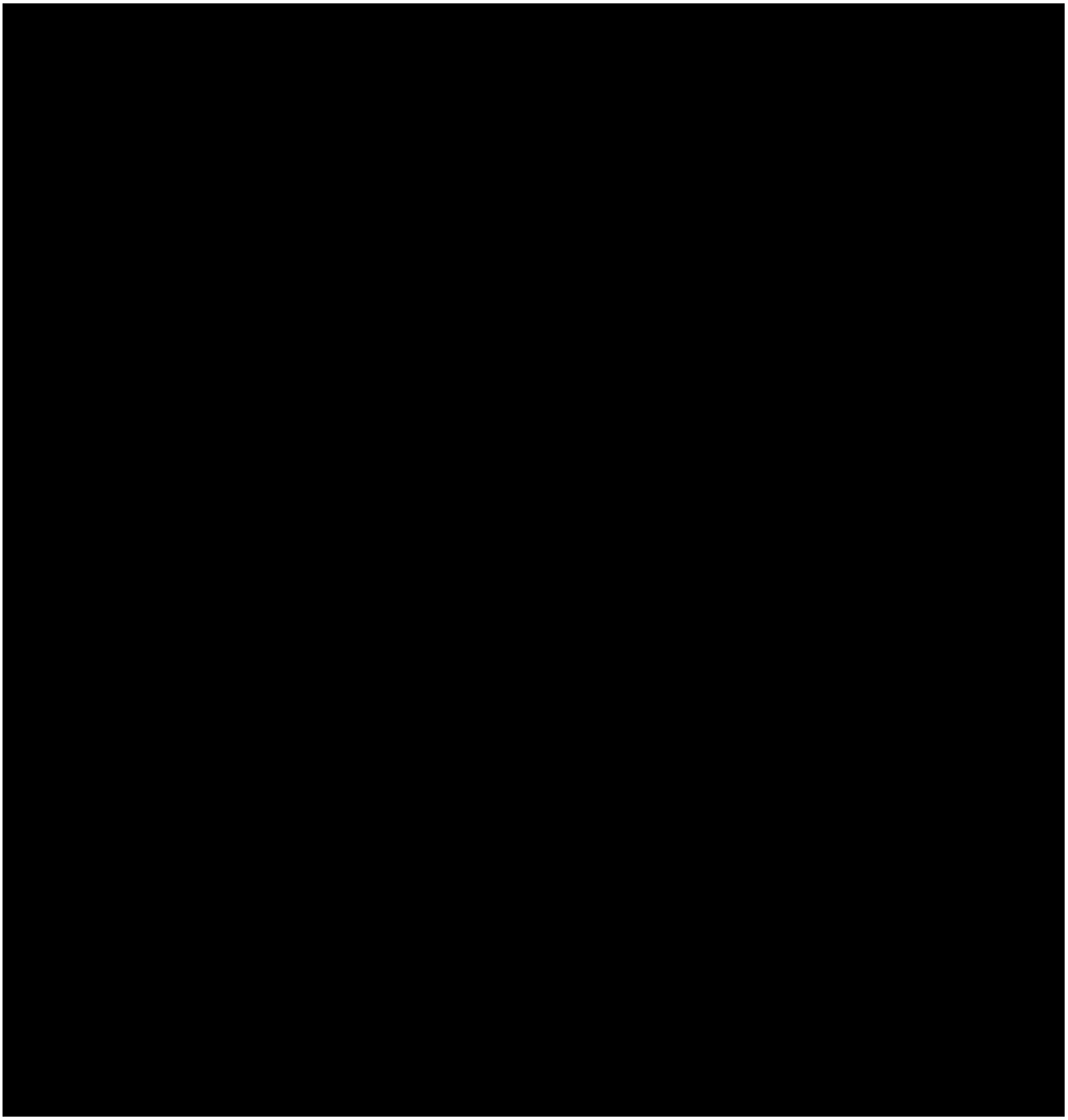

Figure 5.1-8 Port Switch Unit - J1C130BC-1

5.1.1.7 Power Distribution Unit (PDU) - J1C147BA-1

The Power Distribution Unit (PDU) is a single-shelf unit mounted in the top of Processor Cabinet Bays 0

and 1. It is an assembly of fuse blocks, input jacks, and terminal blocks.

Power is routed from the Power Distribution Frame (PDF) on cable pairs into the PDU and distributed out through fused circuits by way of terminal blocks feeding the processor cabinet units. Refer to ED-4C184-12 for details on running power feeders to AM cabinets.

The Port Switch Unit (PSU) in Bay 0 is supplied -48 V DC directly from Jack J in the PDU. In Bay 1, Jack J is not connected.

Specific fuse assignments are made at the local office as indicated in appropriate office records.

Figure 5.1-9 illustrates the PDU and its location in the processor cabinet. A rear view shows input/output provisions.

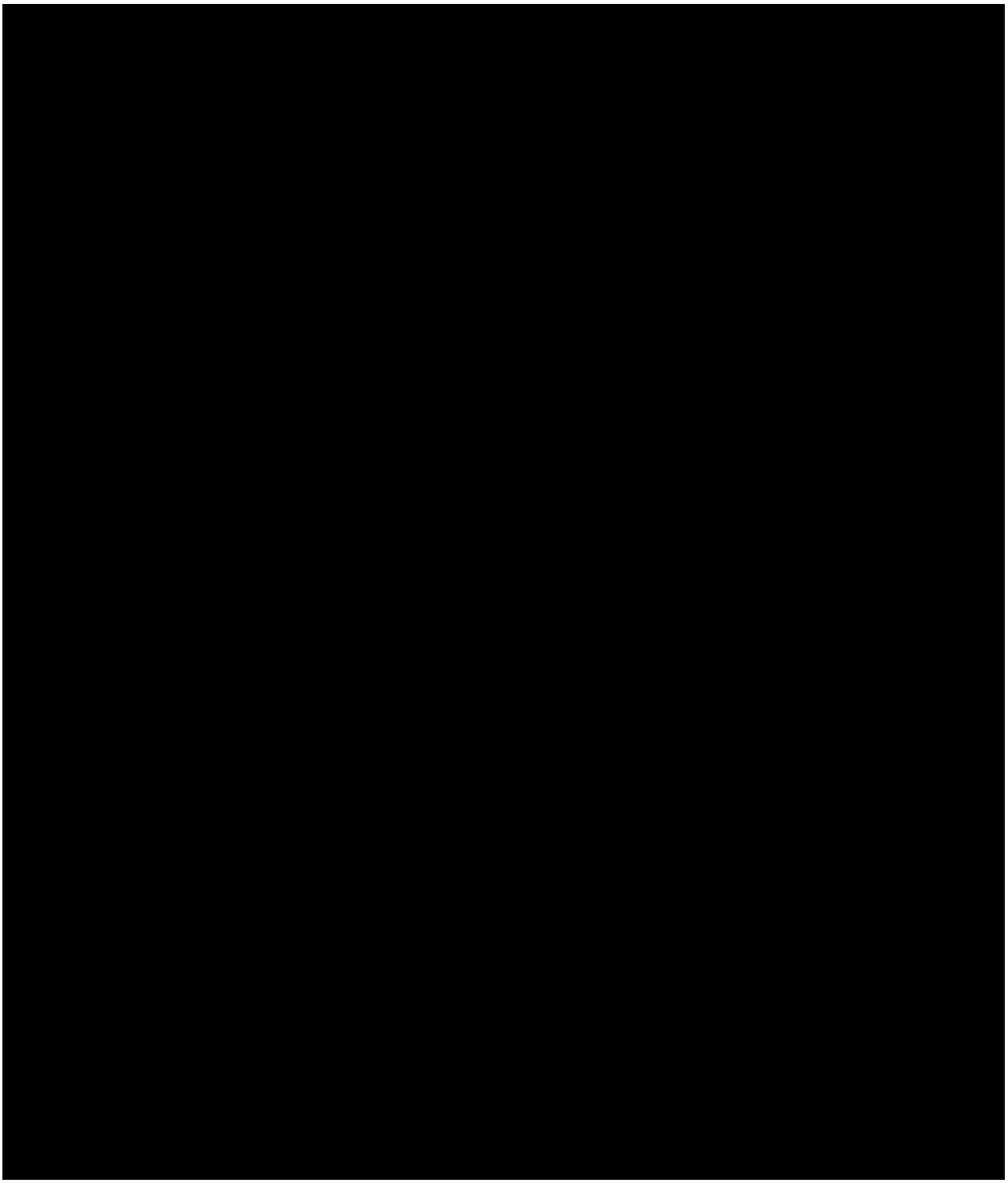

Figure 5.1-9 Power Distribution Unit - J1C147BA-1

5.1.1.8 Tape/Disk Cabinet - J1C192A-1

The Tape/Disk Cabinet contains tape units and disk drives as required for specific *5ESS*® switch office configurations. A cabinet can contain a tape unit and four disk drives or no tape unit and up to eight disk drives for growth accommodation.

Streaming tape units are used in the computer. Two types are available: KS-22762, 1600 bits per inch (BPI) and KS-23113, 6250/1600 BPI. Each unit contains a tape transport and a power distribution unit. The

units have a protective, plastic-hinged front cover with a cut-out for access to the control panel. A circuit breaker keeps the transport power supply from drawing more than 10 amperes of current. The breaker must be in the one position for unit operation.

Figure 5.1-10 illustrates the tape/disk cabinet and the components in it.

Tape diagnostics, self (off-line) and system (on-line), are run on transports to ensure proper operation.

Self-diagnostics are run on the transport during normal operation and when requested from the operator control panel. Test result codes are shown on the digital display (Figure 5.1-11). When a fault occurs during normal operations, reference the displayed digital fault code to the functional fault recovery table (Table 5.1-1) to determine corrective action.

The operator initializes diagnostic test 01, which runs for about 10 minutes. Tests 02 and 03 are available to KS-trained (maintenance) personnel to analyze certain failures in test 01 and can give false indications if run at other times.

Run test 01 as follows:

PRESS POWER ON SWITCH.

LOGIC OFF indicator lights.

TOUCH LOGIC ON SWITCH.

LOGIC OFF indicator goes off. (Diagnostics include a power-on health check that runs when the LOGIC ON switch is touched. If the digital display indicates a fault, verify power to the unit, verify that the operation is legal or change the tape. If the fault does not clear, call KS maintenance.)

LOGIC ON indicator lights.

THREAD TAPE. [Do not move tape to Beginning of Tape (BOT).]

CLOSE DOOR.

TOUCH TEST SWITCH (Display reads 01)

TOUCH EXECUTE SWITCH.

Test proceeds with various motion and read/write exercises for about 10 minutes.

If the test is successful, the tape rewinds, the digital display reads 00, and the RESET indicator illuminates.

If the test fails, the diagnostic halts, the RESET indicator lights, and a fault code (number) is displayed. Reference the fault code in Table 5.1-1 to determine corrective action.

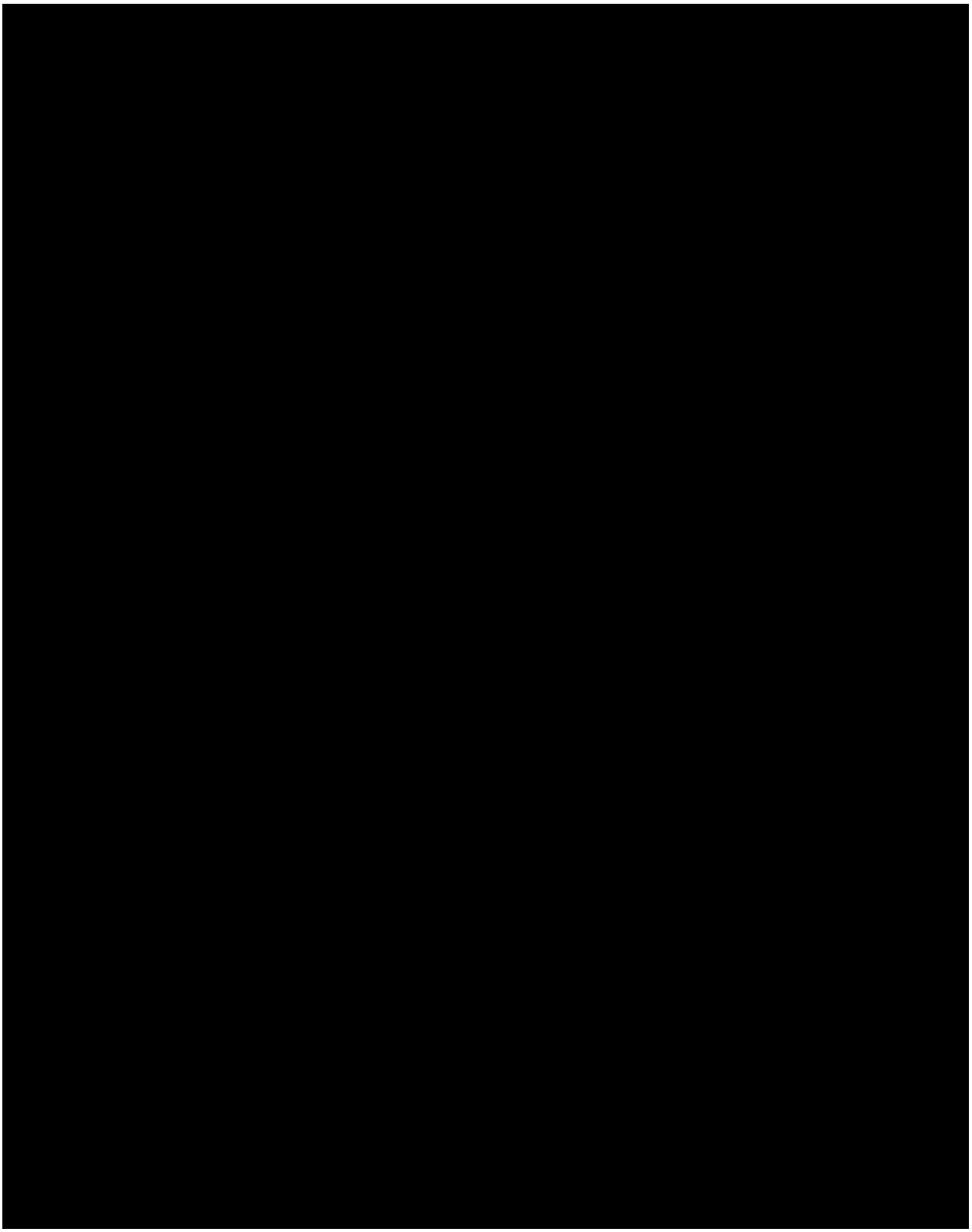

Figure 5.1-10 Tape/Disk Cabinet - J1C192A-1

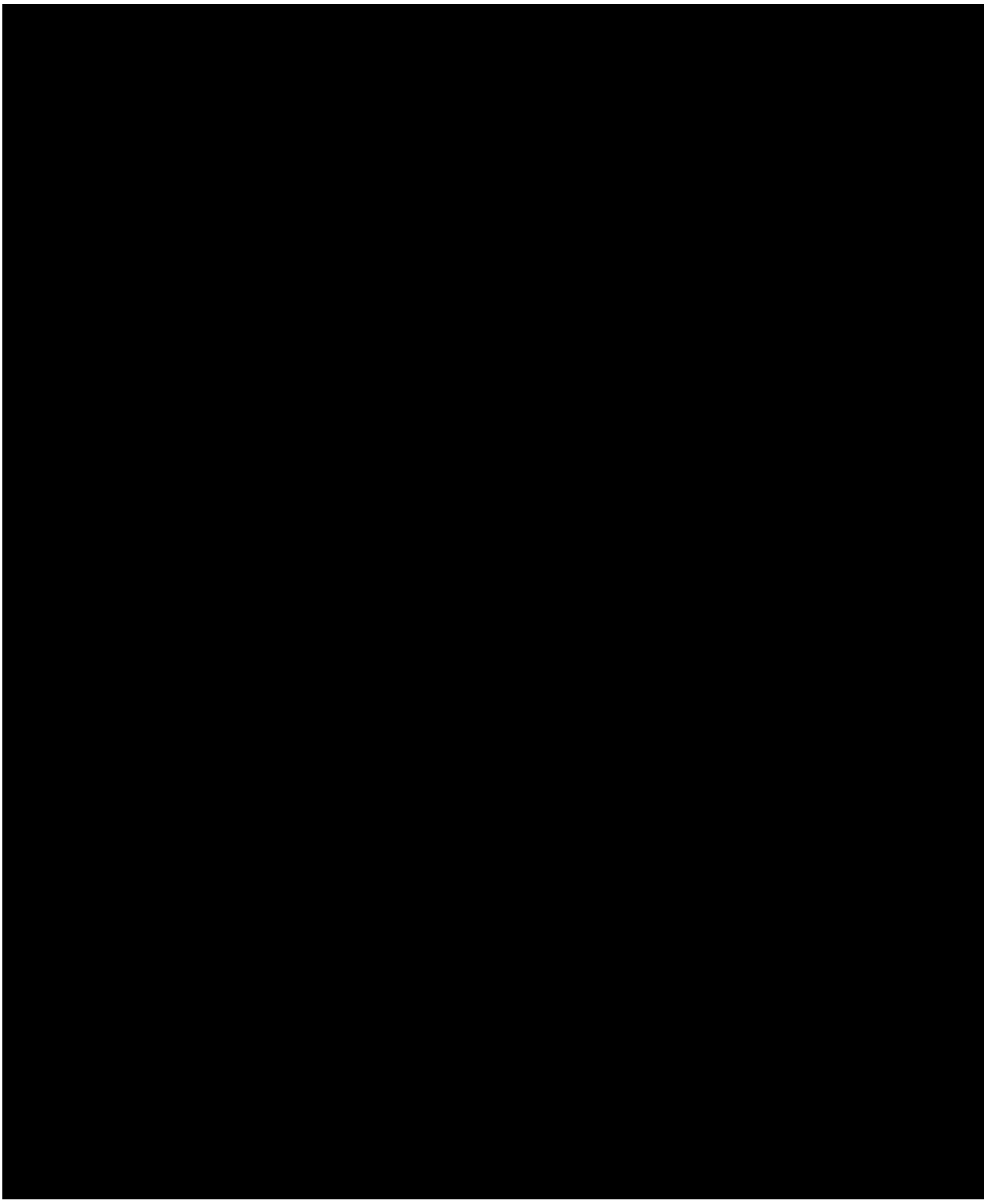

Figure 5.1-11 Operator Control Panel

Table 5.1-1 Operator Test 01 Fault Recovery

FAULT CODE	CAUSE OF FAULT	CORRECTIVE ACTION		
		1	2	3
01-09	Read/Write Errors	Clean Read/Write Head	Change Tape	Call Maintenance
10	Operator Door Open	Close Door	Call Maintenance	□

11	Tape Not Threaded	Thread Tape	Call Maintenance	□
12	Hub Not Latched	Latch Hub	Change Tape	Call Maintenance
13	Tape Incorrectly Threaded	Thread Tape Per Diagram	Call Maintenance	□
14	BOT Marker Fault	Check Location of Marker	Change Tape	Call Maintenance
15	Reset Switch Aborted Load/Unload	Retry Operation	Call Maintenance	□
16	Tape Not Write Enabled	Install Write Enable Ring	Call Maintenance	□
17	EOT Marker Fault	Check Location of Marker	Change Tape	Call Maintenance
18	Tape Already Loaded	Unload and Thread Tape	Call Maintenance	□
20-29	Tape/Unit Fault	Clean Read/Write Head	Change Tape	Call Maintenance
30-99	Unit Fault	Call Maintenance	□	□

5.1.2 3B21D COMPUTER SYSTEM - J3T061A-1

The 3B21D computer is a high-speed, fault-tolerant, high-reliability, duplex computer. See Figure 5.1-2 . The 3B21D computer is similar to 3B20D computer except for the following:

- Expansion slots in the 3B21D computer control unit complex
- Maximum main store memory configuration is increased from 64 MB to 128 MB
- Tape unit - connects to a Disk File Controller (DFC) via SCSI bus versus tape unit connects through input/output processor in the 3B20D computer.
- Disk file controller - supports up to three DFCs versus four in the 3B20D computer. A minimum DFC consists of one disk file controller A, one SCSI host adapter, and one power converter.
- Direct Memory Access (DMA) - supports up to 32 dual serial channels versus 64 in the 3B20D computer.

The 3B21D computer system is packaged in one to three cabinets. Figure 5.1-12 depicts the two 3B21D computer cabinets. The cabinets are as follows:

- Processor cabinet - which is required at all times.
- First peripheral growth cabinets (J3T059A-1) - which are for the 9-track tape units. Tape drives are required as part of the configuration. The first peripheral growth cabinet is located to the right of the processor cabinet. The 3B21D computer currently uses a 9-track tape unit for procedures such as downloading disks and for an AMA backup system. However, it can also support the Digital Audio Tape (DAT) units. These units are considerably smaller than the current 9-track tape units. The use of the DAT eliminates the need for a tape frame on the 3B21D computer AM, thus reducing it from a 2-frame to a 1-frame configuration.

Each cabinet measures 72 inches (182 cm) high by 30 inches (76 cm) wide by 24 inches (60 cm) deep. Figure 5.1-13 shows the layout of the processor unit cabinet. Figure 5.1-14 shows the layout of the growth unit cabinet.

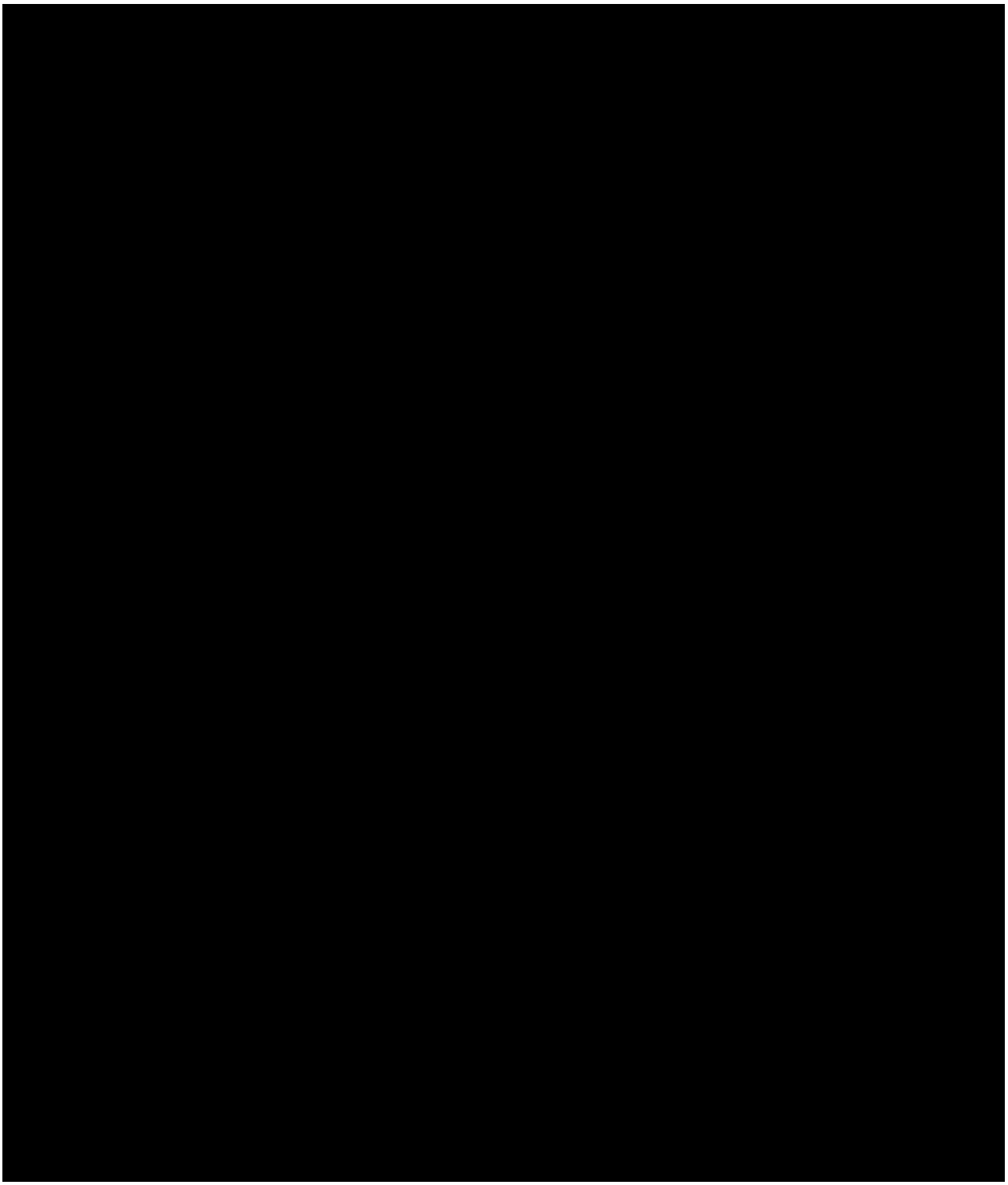

Figure 5.1-12 3B21D Computer Cabinets

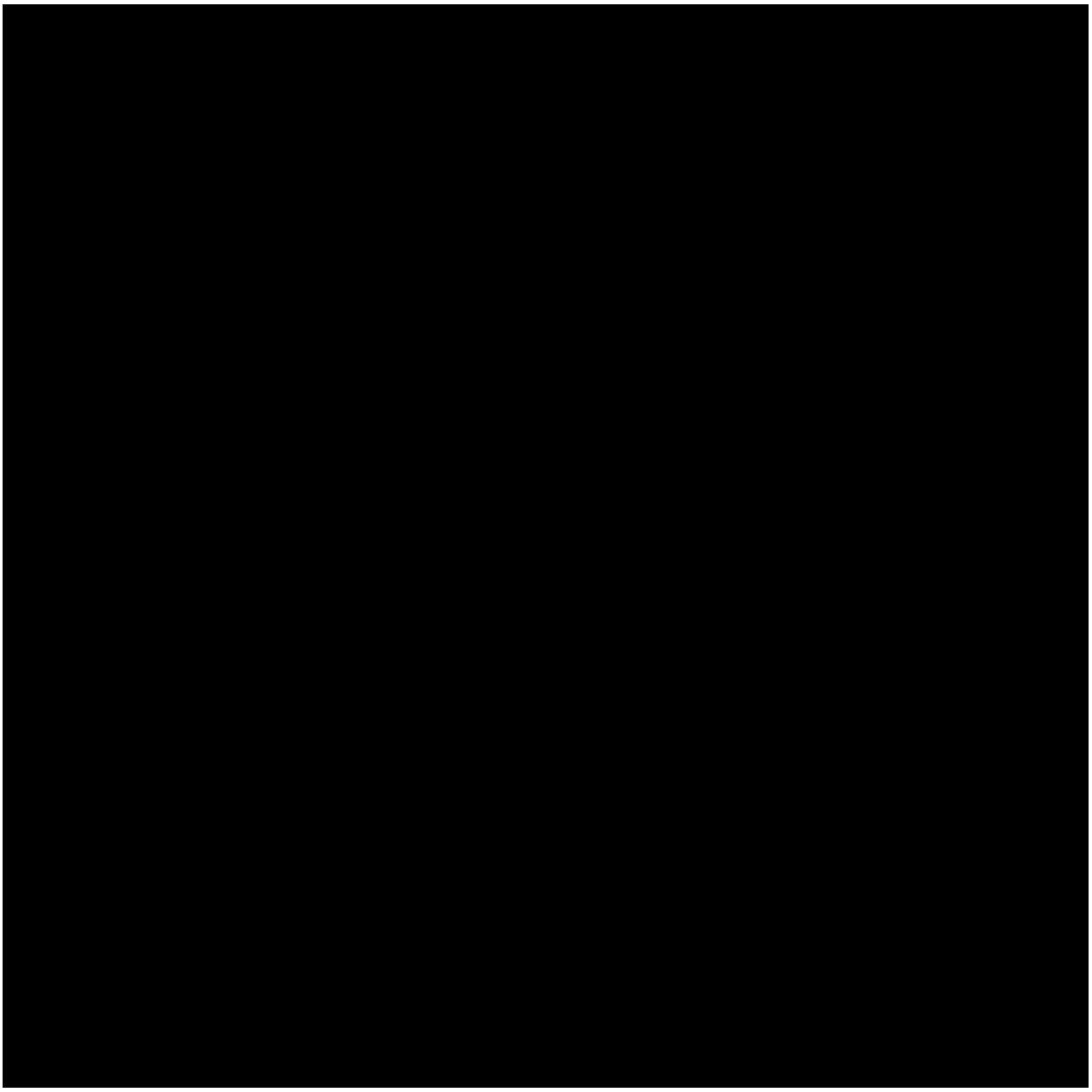

Figure 5.1-13 Processor Unit Shelf Layout - J3T060AA-1

Figure 5.1-14 Growth Unit Shelf Layout - J3T060AB-1

5.1.2.1 Small Computer System Interface (SCSI)

The Small Computer System Interface (SCSI), used in the 3B21D computer, is an interface for computer input/output devices, primarily data storage units. The exchange uses a distributed-processing system, but the data storage remains centralized. The SCSI is designed for multiple access to a central mass data storage area.

The SCSI bus has 50 terminating leads in a 2-by-25-pin female connector. For the AM application, the SCSI bus is limited to five devices, four disk drives, the central processor unit (CPU), and the disk file controller (DFC).

The SCSI bus numbering is detailed in Table 5.1-2 .

In the AM, the DFC serves as two SCSI host adapters (intelligent devices that direct data flow).

The SCSI bus interface has an arrangement for peripheral devices for the AM as it evolves.

The SCSI has the following:

- More disk space
- Increased reliability
- Lower floor space requirement
- Simpler DFC design incorporation.

Older disk systems need up to three cabinets to house the maximum of 16 disks. The SCSI disk system contains up to 16 disk units in a single cabinet and can grow two additional DFCs providing up to 32 disk

units housed in only two cabinets. Equipping the AM with SCSI disk units also reduces maintenance costs.

The SCSI disk units are configured with the same amount of memory capacity as the 340-MB storage module device (SMD) disk units. This configuration may change in the future to let the SCSI disk units take advantage of their entire memory spectrum.

Figure 5.1-2 illustrates the AM including SCSI.

Table 5.1-2 SCSI Peripheral Unit Controller and Bus Assignments

SCSI PERIPHERAL UNIT [a]		PROCESSOR CABINET CONFIGURATION			ADDITIONAL GROWTH (WITH REDUCED IOP CAPABILITY)
DESCRIPTION	LOCATION PROCESSOR CABINET	BASIC	EXAMPLE 1 WITH GROWTH UNIT AT EQL 57	EXAMPLE 2 WITH GROWTH UNITS AT EQLS 57 AND 06	
		DFC/SCSI BUS	DFC/SCSI BUS	DFC/SCSI BUS	DFC/SCSI BUS
SPU00	28-162	DFC 0/SBUS 0	DFC 0/SBUS 0	DFC 0/SBUS 0	
SPU01	53-162	DFC 1/SBUS 1	DFC 1/SBUS 1	DFC 1/SBUS 1	
SPU02	19-170	DFC 0/SBUS 2	DFC 0/SBUS 2	DFC 0/SBUS 2	
SPU03	45-170	DFC 1/SBUS 3	DFC 1/SBUS 3	DFC 1/SBUS 3	
SPU04	28-146	DFC 0/SBUS 0	DFC 0/SBUS 0	DFC 0/SBUS 0	
SPU05	53-146	DFC 1/SBUS 1	DFC 1/SBUS 1	DFC 1/SBUS 1	
SPU06	19-154				DFC 0/SBUS 2
SPU07	45-154				DFC 1/SBUS 3
SPU08	28-118				DFC 0/SBUS 0
SPU09	53-118				DFC 1/SBUS 1
SPU10	19-138				DFC 0/SBUS 2
SPU11	45-138				DFC 1/SBUS 3
SPU12	28-102				DFC 0/SBUS 0
SPU13	53-102				DFC 1/SBUS 1
SPU14	19-118				DFC 0/SBUS 2
SPU15	45-118				DFC 1/SBUS 3
SPU16	19-102				DFC 0/SBUS 2
SPU17	45-102				DFC 1/SBUS 3
SPU18	11-180			DFC 0/SBUS 2	
SPU19	62-180		DFC 1/SBUS 1	DFC 1/SBUS 3	
SPU20	11-164			DFC 0/SBUS 0	
SPU21	62-164		DFC 0/SBUS 0	DFC 1/SBUS 1	
SPU22	11-148			DFC 0/SBUS 2	
SPU23	62-148		DFC 1/SBUS 1	DFC 1/SBUS 3	
SPU24	11-132			DFC 0/SBUS 0	
SPU25	62-132		DFC 0/SBUS 0	DFC 1/SBUS 1	
SPU26	11-116			DFC 0/SBUS 2	
SPU27	62-116		DFC 1/SBUS 1	DFC 1/SBUS 3	
SPU28	11-096				DFC 0/SBUS 0
SPU29	62-096				DFC 1/SBUS 1
SPU30	11-080				DFC 0/SBUS 2
SPU31	62-080				DFC 1/SBUS 3
SPU32	11-064				DFC 0/SBUS 0
SPU33	62-064				DFC 1/SBUS 1
SPU34	11-048				DFC 0/SBUS 2
SPU35	62-048				DFC 1/SBUS 3
SPU54 (MT)	19-186	DFC 0/SBUS 0	DFC 0/SBUS 0	DFC 0/SBUS 0	
	PERIPHERAL CABINET				
SPU56 (9-TRACK1)	10-XXX	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	
SPU57 (9-TRACK0)	42-XXX	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	
SPU58 (9-TRACK3)	17-XXX	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	
SPU59 (9-TRACK2)	42-XXX	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	

Notes:

a. An SCSI Peripheral Unit (SPU) can be any SCSI device such as 9-track tape, Digital Audio Tape (DAT), Moving Head Disk (MHD) drive, or magnetic tape (MT) unit.

The SCSI disk unit (DU) consists of a disk drive and a power supply. The disk unit is an industry standard

Winchester-type drive, supported by a built-in processor to accept instructions from the disk file controller (DFC) via the SCSI bus. The SCSI DFC controls the transfer of data between the CU and up to eight SCSI disk drives. The major subcircuits are as follows:

- Duplex Dual Serial Bus Selector (DDSBS) - TN69B Connects the DFC to the DSCH.
- Host Adapter (HA) Interfaces the DDSBS, intelligent control logic, and two different SCSI buses. The HA consists of a UN294 and TN2116 circuit pack.

The assembled housing for the Disk Unit Package (DUP) slides and locks onto a shelf that holds two DUPs. See Figure 5.1-15 for an exploded view of the DUP components.

The DUP consists of the following components:

- Disk module
- Power supply board (CGG2)
- Power switch board (CGG1)
- Fan module
- Internal device selector microswitch and cable assembly
- Internal cable assemblies
- Internal power cable assemblies
- Housing and mountings.

The front panel of the DUP disk module has cutouts for access to the internal device selector switch, the operating controls and LED indicators. Figure 5.1-16 illustrates the DUP controls and indicators.

A fan module is on the unit chassis of each DUP for ventilation. The module contains a single fan with a panel for alarm and control mounting. For detailed fan replacement procedures, refer to 235-105-220. Figure 5.1-17 illustrates a rear view of the fan module.

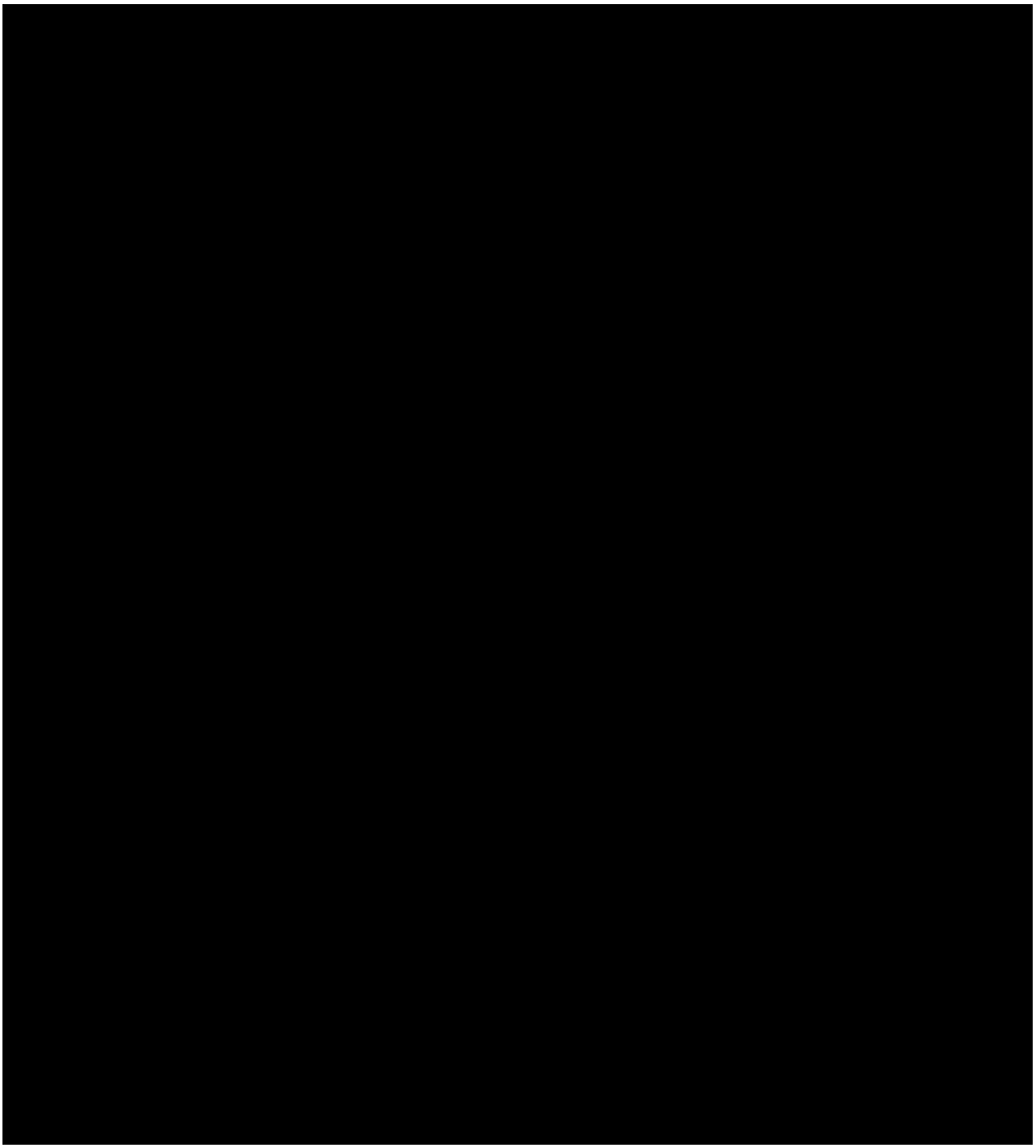

Figure 5.1-15 Disk Unit Package Components

Figure 5.1-16 DUP Controls and Indicators

Figure 5.1-17 Fan Module

5.1.2.2 Digital Audio Tape (DAT) - UN376

The Digital Audio Tape (DAT) has a faceplate-mounted circuit pack, 3.5-inch, single-ended SCSI digital data storage (DDS) formatted DAT drive. The DAT drive uses 4-mm wide tape in 90-, 60-, and 30-meter cartridges. The usable storage capacity of the DAT drive varies with the length of the tape and the recording mode. In a noncompressed mode, the capacity is 650 MB for 30 M; 1300 MB for 60 M; and 2500 MB for the 90-M tape.

The SCSI device identification for the DAT drive is set to any available device address from 0 to 6, inclusive, using three SCSI device identification switches on the circuit pack.

Refer to 235-105-510, *5ESS® Switch, 3B21D Computer Hardware Reference Manual* for additional information.

5.1.2.3 Processor Cabinet, Basic System - J3T060A-1

The basic system configuration consists of the Processor Cabinet equipped with the following major units:

- One Modular Filter and Fuse Panel Unit, J5D003FJ-1
- One Bi-directional Cooling Unit, J5D003FH-2
- Two Processor Units, J3T060AA-1.

The basic system configuration has the following equipment:

- Control Unit (CU) 0 and CU 1.
- Direct Memory Access 0 (DMA 0) is part of the basic system. The DMA 1 is optional.
- Disk File Controller 0 (DFC 0) and DFC 1 supporting seven SCSI Peripheral Units (SPUs). An SPU slot can be equipped with a UN375 Moving Head Disk (MHD) circuit pack or a UN376 DAT circuit pack. The DFC 0 supports four SPUs; DFC 1 supports three SPUs. There are five dedicated SPU slots in the basic units (Processor Unit 0 and 1). Optionally, two additional SPUs (SPU04 and SPU05) can be grown instead of equipping Input/Output Processor (IOP) Peripheral Controller (PC) Community 3 (PC31 and 32.) The PC30 slot in each Processor Unit is always available for use as a PC. One DAT drive (SPU54) is controlled by DFC 0.
- IOP 0 with Peripheral Communities 0, 1, 2, and 3.
- IOP 1 with Peripheral Communities 0, 1, 2, and 3.

5.1.2.4 Peripheral Growth Cabinet - J3T059A-1

The first Peripheral Growth Cabinet has one SCSI 9-track tape drive, KS-23909. This is the first 9-track tape drive (SPU57) in the 3B21D computer system.

A single SCSI bus cable connects a 9-track tape drive to any available SCSI bus (SBUS 0, 1, 2, or 3).

The 9-track tape drives are AC powered and plug directly into an AC power outlet. The drives can be configured to use either 50- or 60-Hertz power.

5.1.2.5 SCSI Peripheral Unit Controller

An SCSI peripheral unit (SPU) can be any device such as 9-track tape, digital audio tape, moving head disk or magnetic tape unit.

The naming convention for the two SCSI buses is ``BUS A'' and ``BUS B.'' The 3B21D computer system designations for the SCSI buses are different, as follows:

- The SCSI BUS A and BUS B of DFC 0 are ``SBUS 0'' and ``SBUS 2,'' respectively.
- The SCSI BUS A and BUS B of DFC 1 are ``SBUS 1'' and ``SBUS 3,'' respectively.

A DFC includes a UN373 (DFCA), TN2116 (DFCB) and is powered by a 410AA (DC-to-DC converter). The equipment locations (EQLs) for DFC 0 and DFC 1 are as follows:

- DFC 0 is in the Processor Cabinet, Processor Unit 0, at 28-170 (TN2116), 28-178 (UN373), and 28-188 (CONVE).
- DFC 1 is in the Processor Cabinet, Processor Unit 1, at 53-170 (TN2116), 53-178 (UN373), and 53-188 (CONVE).

For more detailed information on the 3B21D computer, refer to 235-105-510, *5ESS® Switch 3B21D Computer Hardware Reference Manual*.

5.1.3 ADMINISTRATIVE SERVICES MODULE (ASM)

The *5ESS®* switch Administrative Services Module (ASM) integrates a commercial hardware and software platform into the *5ESS®* switch architecture. The ASM enables service providers to offer switching features even faster. The ASM is a simplex *Sun® Netra®* t1120 server, running the *Solaris™* 2.6 operating system. It is NEBS Level 3 compliant and has access to the Administrative Module (AM) of the switch via Lucent Technologies' proprietary Dual Serial Channel Computer Interconnect high-speed interface. This link supports multiple channels for parallel operations, providing high-speed DMA access to the switch. The ASM supports a wide variety of commercially available software and hardware for network access. Capabilities such as UUCP File Transfer Protocol with Transmission Control Protocol/Internet Protocol (TCP/IP), and 10 BaseT Ethernet are included in the base configuration.

5.1.3.1 Power

The ASM is designed to be rack-mounted in a Miscellaneous Cabinet located no more than 100 feet from the AM and is powered by dual - 48 V DC battery feeds.

5.1.3.2 Configuration

The ASM is equipped with the following:

- Sun Netra t1120 server NEBS Level 3 Certified
- Solaris 2.6 operating system
- 256-Mb memory
- Single processor
- CD-ROM (4x)
- Two RS-232 ports
- Cables
- One Ethernet port

- Four PCI slots
- 1 pair 18.2G mirrored disks
- DAT tape drive
- Alarm interface
- Optional Miscellaneous Cabinet.

5.1.3.3 Functional Description

The *Sun*® *Netra*® t1120 server runs on the *Solaris*™2.6 operating system. It currently provides capacity for administering data changes on the switch, downloading software updates to the switch, and for evolving the switch database to a new software release.

5.1.4 DIAGNOSTIC PHASE DESCRIPTIONS

This section contains the diagnostic phase descriptive information (in the form of tables) for the AM hardware (units/circuits) of the *5ESS*® switch. The entries closely follow those used on the MCC display pages and input/output messages.

The entry [PR Name=*xxxxxxxx*] in the DESCRIPTION/WHAT IS TESTED column in a mnemonic reference to the appropriate diagnostic PR (program listing).

The following is a list of the diagnostic phase tables:

- Table 5.1-3 , Diagnostic Phase Descriptions for ACHI

  The following is a list of the diagnostic phase description tables for the 3B20D (AM):

  - Table 5.1-4 , Diagnostic Phase Descriptions for CU CC in the 3B20D (AM)
  - Table 5.1-5 , Diagnostic Phase Descriptions for CU CH in the 3B20D (AM)
  - Table 5.1-6 , Diagnostic Phase Descriptions for CU CSU in the 3B20D (AM)
  - Table 5.1-8 , Diagnostic Phase Descriptions for CU DMA in the 3B20D (AM)
  - Table 5.1-9 , Diagnostic Phase Descriptions for CU MASC in the 3B20D (AM)
  - Table 5.1-10 , Diagnostic Phase Descriptions for CU SAT in the 3B20D (AM)
  - Table 5.1-11 , Diagnostic Phase Descriptions for CU UC in the 3B20D (AM).

  The following is a list of the diagnostic phase description tables for the 3B21D (AM):

  - Table 5.1-12 , Diagnostic Phase Descriptions for CU CC in the 3B21D (AM)
  - Table 5.1-13 , Diagnostic Phase Descriptions for CU DCI in the 3B21D (AM)
  - Table 5.1-14 , Diagnostic Phase Descriptions for CU DFCS in the 3B21D (AM)
  - Table 5.1-15 , Diagnostic Phase Descriptions for CU DMA in the 3B21D (AM)
  - Table 5.1-16 , Diagnostic Phase Descriptions for CU DMCH in the 3B21D (AM)

- Table 5.1-17 , Diagnostic Phase Descriptions for CU IOP in the 3B21D (AM)
- Table 5.1-18 , Diagnostic Phase Descriptions for CU MASC in the 3B21D (AM)
- Table 5.1-19 , Diagnostic Phase Descriptions for CU MHDS in the 3B21D (AM)
- Table 5.1-20 , Diagnostic Phase Descriptions for CU MT in the 3B21D (AM)
- Table 5.1-21 , Diagnostic Phase Descriptions for CU MTC in the 3B21D (AM)
- Table 5.1-22 , Diagnostic Phase Descriptions for CU UC in the 3B21D (AM).

- Table 5.1-23 , Diagnostic Phase Descriptions for DFC-Mod 1
- Table 5.1-24 , Diagnostic Phase Descriptions for DFC-SCSI
- Table 5.1-25 , Diagnostic Phase Descriptions for DUIC
- Table 5.1-26 , Diagnostic Phase Descriptions for IOP
- Table 5.1-27 , Diagnostic Phase Descriptions for MHD-Mod 1
- Table 5.1-28 , Diagnostic Phase Descriptions for MHD-SCSI
- Table 5.1-29 , Diagnostic Phase Descriptions for MTC
- Table 5.1-30 , Diagnostic Phase Descriptions for MTTYC
- Table 5.1-31 , Diagnostic Phase Descriptions for SCSDC
- Table 5.1-32 , Diagnostic Phase Descriptions for SDLC
- Table 5.1-33 , Diagnostic Phase Descriptions for TTYC

Table 5.1-3 Diagnostic Phase Descriptions for ACHI

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the CC I/O bus interface. [PR Name=DL:ACHI01].
2	Performs the data register loop-around tests. [PR Name=DL:ACHI02]
3	Performs the miscellaneous function tests. [PR Name=DL:ACHI03]

Table 5.1-4 Diagnostic Phase Descriptions for CU CC in the 3B20D (Model 1)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Performs MCH master tests. [PR Name=DL:CC01]
2	Performs the MCH slave communication tests. [PR Name=DL:CC02]
3	Performs the MCH slave command tests. [PR Name=DL:CC03]
4	Performs the MCH microstore address and data register tests. [PR Name=DL:CC04]
5	Performs the MC clock circuit tests, the microinstruction register tests, and the MC parity tests. [PR Name=DL:CC05]
6	Tests the MC immediate data path, MCH access to test multiplexer, buffered bidirectional gating register parity bits, and path to the CC error register. [PR Name=DL:CC06]
7	Tests the MC address sequencer, verifies basic address path for unconditional branch and nobranch. [PR Name=DL:CC07]
8	Tests the MC address sequencer, conditional jump logic, opcode jam path, MC address stack, INT command to MCH, set interrupt set, and interrupt mask registers. [PR Name=DL:CC08]
9	Performs the address and memory verification of UN 28 ROM in CU frame slot 0. (Requires equipage bits in ECD.) [PR Name=DL:CC09]
10	Performs the microstore address bus parity tests. [PR Name=DL:CC10]
11	Tests the HSR, PSW, and SSR. [PR Name=DL:CC11]
12	Tests the PPR. [PR Name=DL:CC12]

13	Tests the gate through the DMU and the byte rotate. [PR Name=DL:CC13]
14	Tests the DMU bit rotate. [[PR Name=DL:CC14]
15	Tests the ALU matcher. [[PR Name=DL:CC15]
16	Tests the DMU Q-register. [[PR Name=DL:CC16]
17	Tests the DMU X or Z flag and ONES. PR Name=DL:CC17]
18	Tests the DMU general registers. [[PR Name=DL:CC18]
19	Tests the ALU and gating paths. [[PR Name=DL:CC19]
20	Tests the 24-bit mode. [[PR Name=DL:CC20]
21	Tests the DMU loop-around. [[PR Name=DL:CC21]
22	Tests the temporary and firmware registers. [PR Name=DL:CC22]
26	Performs the MC privileged PROM tests. PR Name=DL:CC26]
27	Performs the MC privileged PROM tests. [PR Name=DL:CC27]
28	Performs the MC privileged PROM tests. [PR Name=DL:CC28]
30	Tests the writable microstore: BGB, microstore data bus, and microstore address bus access. Tests 4K writable microstore (UN48) or 16K writable microstore (UN248) in CU frame slot 1. (Requires equipage bits in ECD.) [PR Name=DL:CC30]
31	Writable microstore control logic. Tests 4K writable microstore (UN48) or 16K writable microstore (UN248) in CU frame slot 1. (Requires equipage bits in ECD.) [PR Name=DL:CC31]
32	*(Demand, REX, and DEX phase.)* Tests the 4K writable microstore (UN48) in CU frame slot 1. (Requires equipage bits in ECD.) [PR Name=DL:CC32]
33	Tests the writable microstore: BGB, microstore data bus, and microstore address bus access. Tests 4K writable microstore (UN48) or 16K writable microstore (UN248) in CU frame slot 2. (Requires equipage bits in ECD.) [PR Name=DL:CC33]
34	Tests the writable microstore control logic. Tests 4K writable microstore (UN48) or 16K writable microstore (UN248) in CU frame slot 2. (Requires equipage bits in ECD.) [PR Name=DL:CC34]
35	*(Demand, REX, and DEX phase.)* Performs the address and memory test of the 4K writable microstore (UN48) or 16K writable microstore (UN248) in CU frame slot 2. (Requires equipage bits in ECD.) [PR Name=DL:CC35]
36	Tests the writable microstore: BGB, microstore data bus, and microstore address bus access. Tests 4K writable microstore (UN48) or 16K writable microstore (UN248) in CU frame slot 3. (Requires equipage bits in ECD.) [PR Name=DL:CC36]
37	Tests the writable microstore control logic. Tests 4K writable microstore (UN48) or 16K writable microstore (UN248) in CU frame slot 3. (Requires equipage bits in ECD.) [PR Name=DL:CC37]
38	*(Demand, REX, and DEX phase.)* Performs the address and memory test of the 4K writable microstore (UN48) in CU frame slot 3. (Requires equipage bits in ECD.) [PR Name=DL:CC38]
39	Tests the DMU parity. [PR Name=DL:CC39]
40	Tests the SCR/store control field of microinstruction register to SCR.[PR Name=DL:CC40]
41	Tests the SDR, SIR, and IB. [PR Name=DL:CC41]
42	Tests the SAR and PAR. [PR Name=DL:CC42]
43	Tests the IB parity circuit. [PR Name=DL:CC43]
44	Tests the address increment and parity predict. [PR Name=DL:CC44]
45	Tests the address increment (SAR only.) [PR Name=DL:CC45]
46	Tests the SIR path to halfword multiplexer to IB. [PR Name=DL:CC46]
47	Tests the SIR path to halfword multiplexer to IB. [PR Name=DL:CC47]
48	Tests the SIR path to halfword multiplexer to IB. [PR Name=DL:CC48]
49	Tests the SIR path to halfword multiplexer to IB. [PR Name=DL:CC49]
52	Tests the A and B select and rotate amount multiplexer. [PR Name=DL:CC52]
53	Tests the mask ROM. [PR Name=DL:CC53]
54	Tests the FLZ. [PR Name=DL:CC54]
55	Tests the interrupt registers and logic. [PR Name=DL:CC55]
56	Tests the timers (includes CL_PT MCH command check). [PR Name=DL:CC56]
57	Tests the CDR. [PR Name=DL:CC57]
58	Tests CC I/O bus sanity. [PR Name=DL:CC58]
59	*(Demand phase only.)* Before running this phase, any units that are causing external error signals should be repaired. Also, do not execute these tests unless all CU units have been diagnosed or the CU has been in service since the last time power was restored to the frame. This tests the CC interrupt logic circuits connected to units other than the CC. [PR Name=DL:CC59]
60	Tests error response logic. [PR Name=DL:CC60]
61	Tests the EAI. The following is displayed: **PRM_z 0123 4567 89AB CDEF xx xx xx** **PRM_z 0000 0000 0000 0000 xx xx xx** **PRM_z FFFF FFFF FFFF FFFF xx xx xx** [PR Name=DL:CC61]
62	Performs the off-line MCH master side tests. [PR Name=DL:CC62]
70	Performs the address and memory verification of the UN28 (ROM) in CU frame slot 2. (Requires equipage bits in ECD.) [PR Name=DL:CC70]

71	Performs the address and memory verification of the UN28 (ROM) in CU frame slot 2. (Requires equipage bits in ECD.) [PR Name=DL:CC71]
93	*(Demand and DEX phase.)* Tests the EAI lamp display (located next to the power switch on the CU) and the ability of the EAI EAI to transmit PRMs. A series of PRMs appear on the EAI display page and is printed on the ROP. The lamps on the EAI display are cycled through the specific pattern for that phase as follows: **PRM_z 0123 4567 89AB CDEF xx xx xx** **PRM_z AAAA AAAA AAAA AAAA xx xx xx** **PRM_z 5555 5555 5555 5555 xx xx xx** **PRM_z EEEE EEEE EEEE EEEE xx xx xx** **PRM_z 1111 1111 1111 1111 xx xx xx** **PRM_z 0000 0000 0000 0000 xx xx xx** **PRM_z FFFF FFFF FFFF FFFF xx xx xx** The following pattern should now be observed: Digits 0 through F are sequenced on the hexadecimal digit display. The sequence start switch 0-F-0 to warn you that this part of the phase is beginning. Next, each LED lights and then goes off in a pattern running down the display. Later lamp flash may occur and should be ignored. If patterns do not occur, the test failed. Lamp display failures indicate the EAI (TN11) is defective. A PRM failure may be due to a defective EAI or a defective MCRT controller (TN83) in the IOP to which the affected MCRT or ROP is connected. Since this failure is indicated visually, it may run ATP in spite of display faults. All forced states on the EAI must be cleared before this phase is run. This is done by activating key "14" on the EAI page. [PR Name=DL:CC93 or CC90]

Table 5.1-5 Diagnostic Phase Descriptions for CU CH in the 3B20D (AM) (Models 2 and 3)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the DSCH-I/O bus interface. [PR Name=DL:DSCH01]
2	Performs the data register (FIFO) tests. [PR Name=DL:DSCH02]
3	Performs the DSCH error tests. [PR Name=DL:DSCH03]
8	Tests the port 0 selection, interrupts, and service requests. [PR Name=DL:DSCH08]
9	Tests the port 1 selection, interrupts, and service requests. [PR Name=DL:DSCH09]
10	Tests the port 2 selection, interrupts, and service requests. [PR Name=DL:DSCH10]
11	Tests the port 3 selection, interrupts, and service requests. [PR Name=DL:DSCH11]
12	Tests the port 4 selection, interrupts, and service requests. CATP completes when a CNI ring with DLNs is equipped on this channel. [PR Name=DL:DSCH12]
13	Tests the port 5 selection, interrupts, and service requests. [PR Name=DL:DSCH13]
14	Tests the port 6 selection, interrupts, and service requests. [PR Name=DL:DSCH14]
15	Tests the port 7 selection, interrupts, and service requests. [PR Name=DL:DSCH15]
16	Tests the port 8 selection, interrupts, and service requests. [PR Name=DL:DSCH16]
17	Tests the port 9 selection, interrupts, and service requests. [PR Name=DL:DSCH17]
18	Tests the port 10 selection, interrupts, and service requests. [PR Name=DL:DSCH18]
19	Tests the port 11 selection, interrupts, and service requests. [PR Name=DL:DSCH19]
20	Tests the port 12 selection, interrupts, and service requests. [PR Name=DL:DSCH20]
21	Tests the port 13 selection, interrupts, and service requests. [PR Name=DL:DSCH21]
22	Tests the port 14 selection, interrupts, and service requests. [PR Name=DL:DSCH22]
23	Tests the port 15 selection, interrupts, and service requests. [PR Name=DL:DSCH23]
24	Performs the port 0 DSCH-DBS communication tests.[PR Name=DL:DSCH24]
25	Performs the port 1 DSCH-DBS communication tests. [PR Name=DL:DSCH25]
26	Performs the port 2 DSCH-DBS communication tests. [PR Name=DL:DSCH26]
27	Performs the port 3 DSCH-DBS communication tests. [PR Name=DL:DSCH27]
28	Performs the port 4 DSCH-DBS communication tests. [PR Name=DL:DSCH28]
29	Performs the port 5 DSCH-DBS communication tests. [PR Name=DL:DSCH29]
30	Performs the port 6 DSCH-DBS communication tests. [PR Name=DL:DSCH30]
31	Performs the port 7 DSCH-DBS communication tests. [PR Name=DL:DSCH31]
32	Performs the port 8 DSCH-DBS communication tests. [PR Name=DL:DSCH32]
33	Performs the port 9 DSCH-DBS communication tests. [PR Name=DL:DSCH33]
34	Performs the port 10 DSCH-DBS communication tests. [PR Name=DL:DSCH34]
35	Performs the port 11 DSCH-DBS communication tests. [PR Name=DL:DSCH35]
36	Performs the port 12 DSCH-DBS communication tests. [PR Name=DL:DSCH36]
37	Performs the port 13 DSCH-DBS communication tests. [PR Name=DL:DSCH37]
38	Performs the port 14 DSCH-DBS communication tests. [PR Name=DL:DSCH38]
39	Performs the port 15 DSCH-DBS communication tests. [PR Name=DL:DSCH39]
40	*(Demand and DEX phase.)* This phase tests data communication between the CU CH (in the CU) and the BIC (in a DFC or IOP). Specify the DFC or IOP in the DGN input message as a helper unit; use DFC 0, DFC 1, IOP 0, and IOP 1. The unit must be OOS when the diagnostic is run. [PR Name=DL:DSCH40]
44	*(Demand phase only.)* This phase tests reading the normal bootstrap data from the disk into main store. Either DFC 0 or DFC 1 must be OOS for this phase. Run this phase if it is suspected a particular CU and DFC

	combination does not boot. [PR Name=DL:DSCH44]

Table 5.1-6 Diagnostic Phase Descriptions for CU CSU in the 3B20D - Model 1

PHASE	DESCRIPTION/WHAT IS TESTED
1	Performs access to cache memories and kernel/interrupt stack enable tests. [PR Name=DL:CSU01]
2	Performs cache memory match tests. [PR Name=DL:CSU02]
3	Tests the hit/miss matchers (ATBA to tags A and B). [PR Name=DL:CSU03]
4	Tests the hit/miss matchers (ATBB to tags A and B). [PR Name=DL:CSU04]
5	Tests the hit/miss matchers (ATBA to tags C and D). [PR Name=DL:CSU05]
6	Tests the hit/miss matchers (ATBB to tags C and D). [PR Name=DL:CSU06]
7	Tests the select enable logic. [PR Name=DL:CSU07]
8	Tests the write tag control logic (tags A and B). [PR Name=DL:CSU08]
9	Tests the write tag control logic (tags C and D). [PR Name=DL:CSU09]
10	Tests the SAT interface (ATBA to tags A and C). [PR Name=DL:CSU10]
11	Tests the SAT interface (ATBB to tags A and C). [PR Name=DL:CSU11]
12	Tests the tag parity generators. [PR Name=DL:CSU12]
13	Tests the tag parity checkers. [PR Name=DL:CSU13]
14	Tests the hit and miss counters. [PR Name=DL:CSU14]
15	Tests the cache store write control logic. [PR Name=DL:CSU15]
16	Tests the cache store write control logic. [PR Name=DL:CSU16]
17	Tests the error check circuits on the cache memory board. [PR Name=DL:CSU17]
18	*(Demand, REX, and DEX phase.)* Exercises the mechanism that writes off-line main store values to the cache. Can be run whenever CU CC, CU SAT, CU CSU, and CU MASC tests pass, but trouble is suspected in those areas. This should be run with the RAW option. While running, a selection of memory addresses are accessed using various modes. Upon completion, the contents of main memory, ATBs, and cache are compared. If no differences (errors) are found, test continues. If no errors, phase runs for 40 seconds. [PR Name=DL:CSU18]
90	*(Demand phase.)* This phase is the same as phase 18, except that it runs for 40 minutes if no fault is found. This phase can be run whenever an intermittent or data-dependent fault is suspected. Always run this phase with the RAW option. [PR Name=DL:CSU90]

Table 5.1-7 Diagnostic Phase Descriptions for CU CSU in the 3B20D - Models 2 and 3

PHASE	DESCRIPTION/WHAT IS TESTED
1	Access to cache memories and interrupt stack enable tests. [PR Name=DL:CSU01]
2	Cache tag and cache store memory match tests. [PR Name=DL:CSU02]
3	Hit/miss matchers (ATBA to tags A and B). [PR Name=DL:CSU03]
4	Hit/miss matchers (ATBB to tags A and B). [PR Name=DL:CSU04]
5	Hit/miss matchers (ATBA to tags C and D). [PR Name=DL:CSU05]
6	Hit/miss matchers (ATBB to tags C and D). [PR Name=DL:CSU06]
7	Hit/miss matchers (ATBA to tags E and F). [PR Name=DL:CSU07]
8	Hit/miss matchers (ATBB to tags E and F). [PR Name=DL:CSU08]
9	Hit/miss matchers (ATBA to tags G and H). [PR Name=DL:CSU09]
10	Hit/miss matchers (ATBB to tags G and H). [PR Name=DL:CSU10]
11	Select enable logic. [PR Name=DL:CSU11]
12	Cache tag memory write control logic (tags A and B). [PR Name=DL:CSU12]
13	Cache tag memory write control logic (tags C and D). [PR Name=DL:CSU13]
14	Cache tag memory write control logic (tags E and F). [PR Name=DL:CSU14]
15	Cache tag memory write control logic (tags G and H). [PR Name=DL:CSU15]
16	ATBA relocation address to tag memory mod A and E. [PR Name=DL:CSU16]
17	ATBA relocation address to tag memory mod B and F. [PR Name=DL:CSU17]
18	ATBA relocation address to tag memory mod C and G. [PR Name=DL:CSU18]
19	ATBA relocation address to tag memory mod D and H. [PR Name=DL:CSU19]
20	Address and data parity generators. [PR Name=DL:CSU20]
21	Address and data parity checkers (tags A, B, C, and D). [PR Name=DL:CSU21]
22	Address and data parity checkers (tags E, F, G, and H). [PR Name=DL:CSU22]
23	Cache store write control logic - stack write and write update operations (all tags; A, B, C, D, E, F, G, and H). [PR Name=DL:CSU23]
24	Cache store write control logic - normal read stack read and test cache mods updated at store complete time (all tags; A, B, C, D, E, F, G, and H). [PR Name=DL:CSU24]
25	Error check circuits on cache memory board. [PR Name=DL:CSU25]
26	*(Demand, REX, and DEX phase.)* Cache exercise test (40 seconds). Run when CC, SAT, cache, and main store tests pass but a trouble is still suspected in one of these areas. A selection of memory address are accessed using various modes. Then the contents of main memory ATBs, and cache are compared. If no differences are found, the test continues. Differences are reported as errors. If no errors are found, this phase runs for 40 seconds. Always run this phase with the RAW option. [PR Name=DL:CSU26]
90	*(Demand phase.)* Cache exercise test (40 minutes). Run when an intermittent or data dependent fault is suspected. Same as phase 26 except runs more extensive and longer tests. Always run this phase with the

	RAW option. [PR Name=DL:CSU90]

Table 5.1-8 Diagnostic Phase Descriptions for CU DMA in the 3B20D

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the DMA CC I/O bus interface. [PR Name=DL:DMA01]
2	Performs the status tests. [PR Name=DL:DMA02]
3	Performs the RAM/register tests. [PR Name=DL:DMA03]
4	Performs the sequencer tests. [PR Name=DL:DMA04]
5	Tests the request priority circuit. [PR Name=DL:DMA05]
6	Performs the store address tests. [PR Name=DL:DMA06]
7	Performs the store data tests. [PR Name=DL:DMA07]
8	Performs the DMA error tests. [PR Name=DL:DMA08]
9	Performs the DMA/Cache interface tests (CACO). [PR Name=DL:DMA09]
10	Performs the DMA/Cache interface tests (CAC1). [PR Name=DL:DMA10]
11	Tests MASU priority and arbitration functions. [PR Name=DL:DMA11]

Table 5.1-9 Diagnostic Phase Descriptions for CU MASC in the 3B20D

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the inactive state of errors B/C and basic MASC response. [PR Name=DL:MASC01]
2	Tests the address loop-around. [PR Name=DL:MASC02]
4	Performs the data communication tests. [PR Name=DL:MASC04]
5	Tests the parity circuit (data, address, control tests, and halfword and byte decoding). [PR Name=DL:MASC05]
6	Performs the maintenance commands, microstore time-out, microinterrupt, and store go-error tests. [PR Name=DL:MASC06]
7	Performs the MASC memory array response tests. [PR Name=DL:MASC07]
8	Performs the refresh rate tests. [PR Name=DL:MASC08]
9	Performs the MASC timing chain tests. [PR Name=DL:MASC09]
10	Performs the special memory operations and array parity tests (main store array 0). [PR Name=DL:MASC10]
11	Tests the destination and source wait states. [PR Name=DL:MASC11]
12	Performs single-bit hamming correction tests. [PR Name=DL:MASC12]
13	Performs the double-bit error (hamming) tests. [PR Name=DL:MASC13]
14-28	Performs the same as phase 10 (for memory store arrays 1-15). [PR Name=DL:MASC14-DL:MASC28]
29	Tests the address loop-around through main store update (duplex mode). [PR Name=DL:MASC29]
30	Tests the data communication tests through main store update (duplex mode). [PR Name=DL:MASC30]
31	Tests the control lead parity and other store error tests through main store update (duplex mode). [PR Name=DL:MASC31]
32	Performs the microstore error B/C tests. [PR Name=DL:MASC32]
33	*(Demand and DEX phase.)* This phase applies memory patterns and access tests to the main memory. [PR Name=DL:MASC33]
34	*(Demand and DEX phase.)* This phase applies memory patterns and access tests to the main memory. [PR Name=DL:MASC34]
35	Performs the memory data pattern tests. [PR Name=DL:MASC35]
36	*(Demand and DEX phase.)* This phase applies memory patterns and access tests to the main memory. [PR Name=DL:MASC36]
37	Tests the ability to trap a failing address on errors A, C, and D. [PR Name=DL:MASC37]
38	Tests to ensure that the CC and MASC can fetch and execute instructions. [PR Name=DL:MASC38]
39	Performs the update mode and refresh data parity check functional tests. [PR Name=DL:MASC39]
40	*(Demand and DEX phase.)* This phase applies memory patterns and access tests to the main memory. [PR Name=DL:MASC40]
41	*(Demand phase only.)* Update mode and refresh data parity tests to entire main memory. [PR Name=DL:MASC41]
42	Tests MASU priority and arbitration functions. [PR Name=DL:MASC42]
93	*(Demand, REX, and DEX phase.)* Tests main and duplicate refresh address counters. [PR Name=DL:MASC93]
95	*(Demand phase only.)* Applies memory patterns and access tests to the main memory. Limits are allowed to be set at run time. [PR Name=DL:MASC95]
96	*(Demand, DEX, and REX phase.)* Tests update mode and refresh data parity to all main memories. Limits are allowed to be set at run time. [PR Name=DL:MASC96]

Table 5.1-10 Diagnostic Phase Descriptions for CU SAT in the 3B20D

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the SCR control flip-flops. [PR Name=DL:SAT01]
2	Tests the ATB access and parity. [PR Name=DL:SAT02]
3	Tests the ATB memory. [PR Name=DL:SAT03]
4	Tests the counter and invalidate circuit. [PR Name=DL:SAT04]

5	Tests the address multiplexer. [PR Name=DL:SAT05]
6	Tests the write control circuit. [PR Name=DL:SAT06]
7	Tests the ATB hit and ATB miss logic. [PR Name=DL:SAT07]
8	Tests the protection circuit. [PR Name=DL:SAT08]
9	Tests the matchers. [PR Name=DL:SAT09]
10	Tests the main store interface. [PR Name=DL:SAT10]

Table 5.1-11 Diagnostic Phase Descriptions for CU UC in the 3B20D

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the BGB - access and enable. [PR Name=DL:UC01]
2	Performs the access matcher, address leads, and read/write tests. [PR Name=DL:UC02]
3	Performs the block address matcher, address leads, and read/write tests. tests. [PR Name=DL:UC03]
4	Performs the address matcher, address leads, and read/write tests. [PR Name=DL:UC04]
5	Performs the unit identification matcher, address leads, and read/write tests. [PR Name=DL:UC05]
6	Performs the data matcher, address leads, and read/write tests. [PR Name=DL:UC06]
7	Performs the event and transfer trace counters and the read/write tests. [PR Name=DL:UC07]
8	Performs the transfer trace access path unit identification buffers tests. [PR Name=DL:UC08]
9	Performs the trace memory and read/write tests. [PR Name=DL:UC09]
10	Performs the trigger function in freeze mode tests. [PR Name=DL:UC10]
11	Performs the block address matcher adder tests. [PR Name=DL:UC11]
12	Performs the trigger functions in run mode without match conditions. [PR Name=DL:UC12]
13	Performs the access matcher run mode tests. [PR Name=DL:UC13]
14	Performs the data matcher run mode tests. [PR Name=DL:UC14]
15	Performs the address matcher virtual address leads (SAR), run mode tests. [PR Name=DL:UC15]
16	Performs the address matcher physical address leads cache address A bus - run mode tests. [PR Name=DL:UC16]
17	Performs the address matcher physical address leads cache address B bus - run mode tests. [PR Name=DL:UC17]
18	Performs the unit identification matcher and transfer trace run mode tests. [PR Name=DL:UC18]
19	Performs the trigger functions in run mode with match conditions. [PR Name=DL:UC19]
20	Performs the transfer trace run mode tests. [PR Name=DL:UC20]
90	*(Demand phase only.)* Run this phase to test the external output of trigger function 0 and the external inputs to trigger functions 1, 2, and 3. To run this phase, clip pin 400 to pin 405 on the backplane at the UC slot. [PR Name=DL:UC90]
91	*(Demand phase only.)* Run this phase to test the external output of trigger function 1 and the external inputs to trigger functions 0, 2, and 3. To run this phase, clip pin 401 to pin 405 on the backplane at the UC slot. [PR Name=DL:UC91]
92	*(Demand phase only.)* Run this phase to test the external output of trigger function 2 and the external inputs to trigger functions 0, 1, and 3. To run this phase, clip pin 402 to pin 405 on the backplane at the UC slot. [PR Name=DL:UC92]
93	*(Demand phase only.)* Run this phase to test the external output of trigger function 3 and the external inputs to trigger functions 0, 1, and 2. To run this phase, clip pin 403 to pin 405 on the backplane at the UC slot. [PR Name=DL:UC93]

Table 5.1-12 Diagnostic Phase Descriptions for CU CC in the 3B21D

PHASE	DESCRIPTION/WHAT IS TESTED
1	Performs on-line MCH master side tests. [PR Name=DL:CC01]
2	Performs the MCH slave communication tests. [PR Name=DL:CC02]
3	Performs the MCH slave command tests. [PR Name=DL:CC03]
4	Performs microstore address (MSA) and microstore data (MSD) registers in off-line MCH. [PR Name=DL:CC04]
5	Performs BIST and boundary scan tests on CC pack. [PR Name=DL:CC05]
6	Performs the individual application specific integrated circuit (ASIC) BISTs on CC packs. [PR Name=DL:CC06]
7	Performs the microcontrol (MC) clock circuit tests, microinstruction register (MIR), and MC parity tests. [PR Name=DL:CC07]
8	Tests the MC immediate data path, MCH access to test multiplexer, buffered bidirectional gating register (BGR) parity bits, and path to the central control error.[PR Name=DL:CC08]
9	Tests the MC address sequencer, verifies basic address path for unconditional branch and no branch. [PR Name=DL:CC09]
10	Tests the MC address sequencer, conditional jump logic and MC address stack. [PR Name=DL:CC10]
11	Performs verification on read-only memory (ROM) in microstore. [PR Name=DL:CC11]
12	Performs the microstore address bus parity tests. [PR Name=DL:CC12]
13	Verifies the status register. [PR Name=DL:CC13]
14	Tests the pulse point register. [PR Name=DL:CC14]
17	Tests gate through data manipulation unit (DMU) and barrel shifter to rotate bit function. [PR Name=DL:CC17]
19	Tests the arithmetic logic unit (ALU) matcher.[PR Name=DL:CC19]

20	Tests the DMU Q-register. [PR Name=DL:CC20]
21	Tests the DMU X or Z flag and ONES. [PR Name=DL:CC21]
22	Tests the DMU general registers. [PR Name=DL:CC22]
23	Tests the ALU and gating paths. [PR Name=DL:CC23]
24	Tests the 24-bit mode. [PR Name=DL:CC24]
25	Tests the DMU loop-around. [PR Name=DL:CC25]
26	Tests the temporary and firmware registers. [PR Name=DL:CC26]
29	Performs the MC privileged bits tests. [PR Name=DL:CC29]
31	Performs the MC privileged bits tests. [PR Name=DL:CC31]
32	Tests the writable microstore: bidirectional gating bus (BGB), microstore data bus, and microstore address bus access. [PR Name=DL:CC32]
33	Tests the writable microstore: BGB, microstore data bus, and microstore address bus access. [PR Name=DL:CC33]
34	Tests the demand only writable microstore: BGB, microstore data bus, and microstore address bus access. [PR Name=DL:CC34]
35	Tests the DMU parity check. [PR Name=DL:CC35]
38	Tests the store control register (SCR). [PR Name=DL:CC38]
39	Tests the store data register (SDR), store instruction register (SIR), and instruction buffer (IB). [PR Name=DL:CC39]
40	Tests the store address register (SAR) and program address register (PAR). [PR Name=DL:CC40]
41	Tests the IB parity circuit. [PR Name=DL:CC41]
42	Tests the address increment and parity predict. [PR Name=DL:CC42]
44	Tests the SIR path to halfword multiplexer to IB. [PR Name=DL:CC44]
45	Tests the SIR path to IB halfword multiplexer.[PR Name=DL:CC45]
46	Tests the SIR path to path to halfword multiplexer to IB. [PR Name=DL:CC46]
47	Tests the SIR to halfword multiplexer to IB. [PR Name=DL:CC47]
50	Tests the A and B select and rotate amount multiplexer. [PR Name=DL:CC50]
51	Tests the linecard register for masking out errors noted by the ERROR register (MASK). [PR Name=DL:CC51]
52	Tests the find-low-zero (FLZ) of DMU. [PR Name=DL:CC52]
53	Tests the interrupt registers and logic. [PR Name=DL:CC53]
54	Tests the timers. [PR Name=DL:CC54]
55	Tests the channel data register. [PR Name=DL:CC55]
58	Tests central control input/output (CCIO) bus sanity. [PR Name=DL:CC58]
59	Performs the off-line MCH master side tests. [PR Name=DL:CC59]
60	Tests other unit interrupt (demand only). [PR Name=DL:CC60]
61	Tests error response logic. [PR Name=DL:CC61]
64	Tests the emergency action interface. [PR Name=DL:CC64]
65	Tests the EAI commands and display tests (demand only). [PR Name=DL:CC65]
68	Tests the SCR and store address translator (SAT) control bits. [PR Name=DL:CC68]
69	Tests the address translation buffer (ATB) access and parity. [PR Name=DL:CC69]
70	Tests the ATB memory. [PR Name=DL:CC70]
71	Tests the counter and invalidate circuit. [PR Name=DL:CC71]
72	Tests the SAT address multiplier. [PR Name=DL:CC72]
73	Tests the ATB write control logic. [PR Name=DL:CC73]
74	Tests the ATB hit and miss logic. [PR Name=DL:CC74]
75	Tests the ATB protection logic. [PR Name=DL:CC75]
76	Tests the ATB matching of duplicate circuits.[PR Name=DL:CC76]
77	Tests the main store interface[PR Name=DL:CC77]
80	Tests the access to cache memories. [PR Name=DL:CC80]
81	Tests the cache tag and cache memory match. [PR Name=DL:CC81]
82	Tests the hit/miss matcher. [PR Name=DL:CC82]
83	Tests the write enable logic. [PR Name=DL:CC83]
84	Tests the ATB relocation address tag memory. [PR Name=DL:CC84]
85	Tests the address and data parity generator. [PR Name=DL:CC85]
86	Tests the address and data parity checker. [PR Name=DL:CC86]
87	Tests the cache store write control logic.[PR Name=DL:CC87]
88	Tests the cache error check circuitry. [PR Name=DL:CC88]
89	Tests the cache exercise (REX). [PR Name=DL:CC89]
90	Test the phase cache exercise (demand only).

Table 5.1-13 Diagnostic Phase Descriptions for CU DCI in the 3B21D

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the dual serial channel (DSCH) with the duplex dual serial bus selector (DDSBS) interface. [PR Name=DL:DCI01]
2	Tests the DDSBS with the BIC interface. [PR Name=DL:DCI02]
3	Tests the BIC with the peripheral interface controller (PIC) interface. [PR Name=DL:DCI03]

Table 5.1-14 Diagnostic Phase Descriptions for CU DFCS in the 3B21D

PHASE	DESCRIPTION/WHAT IS TESTED

1	Tests the demand-only phase with the BIST boundary scan. [PR Name=DL:DFCS01]
2	Tests the DDSBS interface and the DDSBS/BIC interface.[PR Name=DL:DFCS02]
3	Tests BIC to the PIC interface. [PR Name=DL:DFCS03]
4	Tests the central processing unit (CPU) Test 1. [PR Name=DL:DFCS04]
5	Tests to verify the ROM contents. [PR Name=DL:DFCS05]
6	Performs the Test 1-MB static random access memory (SRAM). [PR Name=DL:DFCS06]
7	Performs the host adapter register test. [PR Name=DL:DFCS07]
8	Performs the WE32104 direct memory access controller (DMAC) test. [PR Name=DL:DFCS08]
9	Performs the dual universal asynchronous receiver/transmitter (DUART) test. [PR Name=DL:DFCS09]
10	Tests the system timing controller (STC).[PR Name=DL:DFCS10]
11	Performs the small computer system interface (SCSI) protocol controllers tests on both SCSI buses. [PR Name=DL:DFCS11]
12	Tests only differential type devices attached to the bus. [PR Name=DL:DFCS12]
13	Tests the bus reset capability. [PR Name=DL:DFCS13]
14	Performs the demand exercise (DEX) bit wise independent test for host adapter (HA) FIFO. [PR Name=DL:DFCS14]
15	Tests the interface to nonactive CU (demand only). [PR Name=DL:DFCS15]
90	Performs demand only test and the bus loop test. [PR Name=DL:DFCS90]

Table 5.1-15 Diagnostic Phase Descriptions for CU DMA in the 3B21D

PHASE	DESCRIPTION/WHAT IS TESTED
1	Performs the BIST/boundary scan tests. [PR Name=DL:DMA01]
2	Tests the DMA/CCIO bus interface. [PR Name=DL:DMA02]
3	Performs the status tests. [PR Name=DL:DMA03]
4	Performs the random access memory (RAM) register tests. [PR Name=DL:DMA04]
5	Performs the sequencer tests. [PR Name=DL:DMA05]
6	Tests the request priority circuit. [PR Name=DL:DMA06]
7	Performs the store address tests. [PR Name=DL:DMA07]
8	Performs the store data tests. [PR Name=DL:DMA08]
9	Performs the DMA error tests. [PR Name=DL:DMA09]
10	Performs the DMA/CCIO bus interface (demand only). [PR Name=DL:DMA10]
11	Perform the DMA/Cache interface tests. [PR Name=DL:DMA11]
13	Perform the MASU priority and arbitration tests. [PR Name=DL:DMA13]

Table 5.1-16 Diagnostic Phase Descriptions for CU DMCH in the 3B21D

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the direct IO bus interface. [PR Name=DL:DMCH01]
2	Performs the data register FIFO tests. [PR Name=DL:DMCH02]
3	Performs the error tests. [PR Name=DL:DMCH03]
4	Tests the quad word transfer. [PR Name=DL:DMCH04]
10	Performs the Port 0 selection, interrupt, and service requests. [PR Name=DL:DMCH10]
11	Performs the Port 1 selection, interrupt, and service requests. [PR Name=DL:DMCH11]
12	Performs the Port 2 selection, interrupt, and service requests. [PR Name=DL:DMCH12]
13	Performs the Port 3 selection, interrupt, and service requests. [PR Name=DL:DMCH13]
20	Performs the Port 0 DSCH/DDSBS communication tests. [PR Name=DL:DMCH20]
21	Performs the Port 1 DSCH/DDSBS communication tests. [PR Name=DL:DMCH21]
22	Performs the Port 2 DSCH/DDSBS communication tests. [PR Name=DL:DMCH22]
23	Performs the Port 3 DSCH/DDSBS communication tests. [PR Name=DL:DMCH23]

Table 5.1-17 Diagnostic Phase Descriptions for CU IOP in the 3B21D

PHASE	DESCRIPTION/WHAT IS TESTED
1	Performs the BIST/boundary scan for the demand-only phase. [PR Name=DL:IOP01]
2	Tests the DSCH with the DDSBS interface. [PR Name=DL:IOP02]
3	Tests the DDSBS with the BIC interface and BIC circuitry excluding PIC interface. [PR Name=DL:IOP03]
4	Tests the BIC with the PIC interface using PIC resident firmware. [PR Name=DL:IOP04]
5	Tests the BIC with the PIC communication. [PR Name=DL:IOP05]
6	Tests the PIC microstore data validity and microstore parity checker. [PR Name=DL:IOP06]
7	Tests the PIC microsequencer. [PR Name=DL:IOP07]
8	Tests the PIC register and ALU. [PR Name=DL:IOP08]
9	Tests the PIC source/destination decoders. [PR Name=DL:IOP09]
10	Tests the PIC internal registers. [PR Name=DL:IOP10]
11	Tests the PIC interrupt circuitry. [PR Name=DL:IOP11]
12	Tests the PIC RAM and sequencer. [PR Name=DL:IOP12]
13	Tests the input/output microprocessor interface (IOMI) hardware. [PR Name=DL:IOP13
15	Tests the IOMI power control circuitry peripheral controller community power converter/monitor. [PR Name=DL:IOP13]
16	Tests the interface with the nonactive CU for the demand-only phase. The nonactive CU must be specified as the helper unit, and must be OOS and ATP. [PR Name=DL:IOP16]

Table 5.1-18 Diagnostic Phase Descriptions for CU MASC in the 3B21D

PHASE	DESCRIPTION/WHAT IS TESTED
1	Executes the memory controller (MCERT) "power-on" initial test. [PR Name=DL:MASC01]
2	Performs the boundary scan test. [PR Name=DL:MASC02]
3	Tests the basic response from MM circuit. [PR Name=DL:MASC03]
4	Performs the address loop-around test. [PR Name=DL:MASC04]
5	Performs the data path test. [PR Name=DL:MASC05]
6	Tests store error A. [PR Name=DL:MASC06]
7	Performs the maintenance command test. [PR Name=DL:MASC07]
8	Performs store B and C tests. [PR Name=DL:MASC08]
11	Performs the destination and source wait state tests. [PR Name=DL:MASC11]
12	Performs the single-bit hamming tests. [PR Name=DL:MASC12]
13	Performs the double-bit error (hamming) tests. [PR Name=DL:MASC13]
14	Tests the address trap logic. [PR Name=DL:MASC14]
15	Performs the arbiter RAM testing. [PR Name=DL:MASC15]
20	Performs the short march test to Bank 0. [PR Name=DL:MASC20]
21	Performs the short march test to Bank 1. [PR Name=DL:MASC21]
22	Performs the short march test to Bank 2. [PR Name=DL:MASC22]
23	Performs the short march test to Bank 3. [PR Name=DL:MASC23]
24	Performs the short march test to Bank 4. [PR Name=DL:MASC24]
25	Performs the short march test to Bank 5. [PR Name=DL:MASC25]
26	Performs the short march test to Bank 6. [PR Name=DL:MASC26]
27	Performs the short march test to Bank 7. [PR Name=DL:MASC27]
30	Performs the memory operations and parity tests to Bank 0. [PR Name=DL:MASC30]
31	Performs the memory operations and parity tests to Bank 1. [PR Name=DL:MASC31]
32	Performs the memory operations and parity tests to Bank 2. [PR Name=DL:MASC32]
33	Performs the memory operations and parity tests to Bank 3. [PR Name=DL:MASC33]
34	Performs the memory operations and parity tests to Bank 4. [PR Name=DL:MASC34]
35	Performs the memory operations and parity tests to Bank 5. [PR Name=DL:MASC35]
36	Performs the memory operations and parity tests to Bank 6. [PR Name=DL:MASC36]
37	Performs the memory operations and parity tests to Bank 7. [PR Name=DL:MASC37]
38	Tests the address loop-around through main store update (duplex mode). [PR Name=DL:MASC38]
39	Tests the data loop-around through main store update (duplex mode). [PR Name=DL:MASC39]
40	Performs the main store update control and error tests. [PR Name=DL:MASC40]
41	Performs the memory data pattern tests. [PR Name=DL:MASC41]
42	Tests the fetch/execute instruction from main store. [PR Name=DL:MASC42]
43	Performs the function testing of update mode and refresh data parity checks parity checks (some memory locations). [PR Name=DL:MASC43]
45	Performs the memory data to March pattern tests. [PR Name=DL:MASC45]
46	Performs the memory data to March pattern tests. [PR Name=DL:MASC46]
48	Performs the memory data pattern tests using byte, half, and read-modify-write commands. [PR Name=DL:MASC48]
50	*(Demand Phase only.)* Performs the memory data to March pattern tests. [PR Name=DL:MASC50]
51	*(Demand Phase only.)* Performs the memory data to March pattern tests. [PR Name=DL:MASC51]
52	*(Demand Phase only.)* Performs the memory data to March pattern tests. [PR Name=DL:MASC52]
53	*(Demand Phase only.)* Performs the memory data to March pattern tests. [PR Name=DL:MASC53]
95	*(Demand Phase only.)* Performs the run user-specified to March pattern tests. [PR Name=DL:MASC95]
96	Performs the function testing of update mode and refresh data parity checks (all memory locations). User may specify test parameters. [PR Name=DL:MASC96]

Table 5.1-19 Diagnostic Phase Descriptions for CU MHDS in the 3B21D

PHASE	DESCRIPTION/WHAT IS TESTED
1	Performs the SCSI moving head disk test. [PR Name=DL:MHDS01]

Table 5.1-20 Diagnostic Phase Descriptions for CU MT in the 3B21D

PHASE	DESCRIPTION/WHAT IS TESTED
1	Diagnose the SCSI Device identified in the command: (a) Reset and verify reset condition. (b) Execute the built-in, self-test of the tape unit. [PR Name=DL:MT01]
90	Verify read/write of blocked data to tape. (Writable tape must be installed). [PR Name=DL:MT90]
91	Verify write protection mechanism of the tape unit. (Write protected tape must be installed). Phase mt90 must be successfully executed before this phase. [PR Name=DL:MT91]

Table 5.1-21 Diagnostic Phase Descriptions for CU MTC in the 3B21D

PHASE	DESCRIPTION/WHAT IS TESTED
1	Performs the SCSI tape test. [PR Name=DL:MTC01]
90	Performs the SCSI demand-only test for read/write. [PR Name=DL:MTC90]
91	Performs the SCSI demand-only test for write protect. [PR Name=DL:MTC91]

Table 5.1-22 Diagnostic Phase Descriptions for CU UC in the 3B21D

PHASE	DESCRIPTION/WHAT IS TESTED
1	Performs the bidirectional gating bus access and enable. [PR Name=DL:UC01]
2	Performs the access matcher, address leads, and read/write test. [PR Name=DL:UC02]
3	Performs the block address matchers, address leads, and read/write test. [PR Name=DL:UC03]
4	Performs the address matcher, address leads, and read/write test. [PR Name=DL:UC04]
5	Performs the unit identification matcher, address leads, and read/write test. [PR Name=DL:UC05]
6	Performs the data matcher, address leads, and read/write test. [PR Name=DL:UC06]
7	Performs the event and trace memory addresses counters, and read/write test. [PR Name=DL:UC07]
8	Performs the transfer trace memory access path unit identification buffers test. [PR Name=DL:UC08]
9	Performs the trace memory and read/write test. [PR Name=DL:UC09]
10	Performs the trigger functions in freeze mode tests. [PR Name=DL:UC10]
11	Performs the trigger functions in run mode without match conditions. [PR Name=DL:UC11]
12	Performs the access matcher and run mode tests. [PR Name=DL:UC12]
13	Performs the data matcher and run mode tests. [PR Name=DL:UC13]
14	Performs the address matcher, virtual address bus (store address register), and run mode tests. [PR Name=DL:UC14]
15	Performs the address matcher, physical address bus, and run mode tests. [PR Name=DL:UC15]
16	Performs the unit identification matcher and run mode tests. [PR Name=DL:UC16]
17	Performs the trigger functions in run mode with match conditions. [PR Name=DL:UC17]
18	Performs the transfer trace and run mode tests. [PR Name=DL:UC18]
19	Performs the trace memory read/write indicator bit test. [PR Name=DL:UC19]
90	Performs the demand-only phase with special procedure. External input and external output trigger function 0.
91	Performs the demand-only phase with special procedure. External input and external output trigger function 1.
92	Performs the demand-only phase with special procedure. External input and external output trigger function 2.
93	Performs the demand-only phase with special procedure. External input and external output trigger function 3.

Table 5.1-23 Diagnostic Phase Descriptions for DFC - Model 1

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the DSCH-DDSBS interface. [PR Name=DL:DFC01]
2	Tests the DDSBS-BIC interface and BIC circuitry. Excludes the PIC's interface. [PR Name=DL:DFC02]
3	Tests the BIC-PIC interface using PIC resident firmware. [PR Name=DL:DFC03]
4	Tests the BIC-PIC communication. [PR Name=DL:DFC04]
5	Tests the PIC microstore data validity and microstore parity checker. [PR Name=DL:DFC05]
6	Tests the PIC microsequencer. [PR Name=DL:DFC06]
7	Tests the PIC register and ALU. [PR Name=DL:DFC07]
8	Tests the PIC source/destination decoders. [PR Name=DL:DFC08]
9	Tests the PIC internal registers. [PR Name=DL:DFC09]
10	Tests the PIC interrupt circuitry. [PR Name=DL:DFC10]
11	Tests the PIC RAM and sequencer. [PR Name=DL:DFC11]
12	Parallel/serial data interface and MHD control source and destination decoders. [PR Name=DL:DFC12]
13	MHD control register. [PR Name=DL:DFC13]
15	*(Demand phase.)* Tests the interface with the off-line CU. Off-line CU must be specified as a helper unit, and it must be OOS and ATP before running this phase. [PR Name=DL:DFC15]

Table 5.1-24 Diagnostic Phase Descriptions for DFC - SCSI

PHASE	DESCRIPTION/WHAT IS TESTED
1	DSCH-DDSBS interface. [PR Name=DL:DFCS01]
2	DDSBS-BIC interface and BIC circuitry excluding HA CI. No BIC FIFO buffer memory testing. [PR Name=DL:DFCS02]
3	BIC-HA CI using HA resident firmware. [PR Name=DL:DFCS03]
4	WE32100 CPU test. [PR Name=DL:DFCS04]
5	Verifies ROM's contents. [PR Name=DL:DFCS05]
6	Test 1 MB SRAM. [PR Name=DL:DFCS06]
7	HA register tests. [PR Name=DL:DFCS07]
8	WE32104 DMAC test. [PR Name=DL:DFCS08]
9	DUART test. [PR Name=DL:DFCS09]
10	STC test. [PR Name=DL:DFCS10]
11	SCSI protocol controllers test. Tests both SCSI buses. [PR Name=DL:DFCS11]
12	Test (validate) only differential type devices attached to buses. [PR Name=DL:DFCS12]
13	Test ability of SCSI devices to recognize and acknowledge bus reset. [PR Name=DL:DFCS13]
14	*(Demand and DEX phase.)* Bit-wise independence test for the HA FIFO buffer memory. [PR Name=DL:DFCS14]
15	*(Demand only phase.)* Tests the interface with the STBY CU. The STBY CU must be specified as the helper

	unit, and must be OOS and ATP before running this phase. [PR Name=DL:DFCS15]
90	*(Demand phase.)* SCSI bus loop test. This phase requires that existing cables from the DFC be disconnected and the loop-around cable be connected between the two buses where they connect to the DFC before running the phase. [PR Name=DL:DFCS90]

Table 5.1-25 Diagnostic Phase Descriptions for DUIC

PHASE	DESCRIPTION/WHAT IS TESTED
1	Request isolate, control signal, and control signal acknowledge from the PIC. [PR Name=DL:DUIC01]
2	Read/write access of DAM. [PR Name=DL:DUIC02]
3	DAM parity checker. [PR Name=DL:DUIC03]
4	Microdiagnostic. [PR Name=DL:DUIC04]
5	*(Demand only phase.)* Loopback mode. The DUIs must be equipped. [PR Name=DL:DUIC05]
6	*(Demand only phase.)* Send-frames mode. The DUIs must be equipped. [PR Name=DL:DUIC06]

Table 5.1-26 Diagnostic Phase Descriptions for IOP

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the DSCH-DDSBS interfaces. [PR Name=DL:IOP01]
2	Tests the DDSBS - BIC interface and BIC circuitry. Excludes the PIC. [PR Name=DL:IOP02]
3	Tests the BIC-PIC interface, using the PIC resident firmware. [PR Name=DL:IOP03]
4	Tests the BIC-PIC communications. [PR Name=DL:IOP04]
5	Tests the PIC microstore data validity and microstore parity checker. [PR Name=DL:IOP05]
6	Tests the PIC microsequencer. [PR Name=DL:IOP06]
7	Tests the PIC and ALU. [PR Name=DL:IOP07]
8	Tests the PIC source/destination decoders. [PR Name=DL:IOP08]
9	Tests the PIC internal registers. [PR Name=DL:IOP09]
10	Tests the PIC interrupt circuitry. [PR Name=DL:IOP10]
11	Tests the PIC RAM and sequencer. [PR Name=DL:IOP11]
12	Tests the I/O microprocessor interface hardware. [PR Name=DL:IOP12]
13	Tests the I/O microprocessor interface power control circuitry peripheral controller community power converter/monitor. [PR Name=DL:IOP13]
15	*(Demand phase only.)* Tests the interface with the off-line CU. The off-line CU must be specified as a helper unit and it must be OOS and ATP. [PR Name=DL:IOP15]

Table 5.1-27 Diagnostic Phase Descriptions for MHD-Model 1

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the parallel/serial data interface and the MHD control source and destination decoders. [PR Name=DL:MHD01]
2	Tests MHD control register. [PR Name=DL:MHD02]
3	Tests the parallel/serial data interface. [PR Name=DL:MHD03]
4	Tests the MHD control, disk select, and driver enable. [PR Name=DL:MHD04]
5	Tests the MHD clock. A fully formatted disk must be mounted and spinning on the drive under test. [PR Name=DL:MHD05]
6	Tests the read/write circuitry and error correction circuitry. A fully formatted disk pack must be mounted and spinning on the drive under test. [PR Name=DL:MHD06]
7	Tests the seek, seek error detection, servo offset, and fault detection circuitry of the drive. A fully formatted disk pack must be mounted and spinning on the drive under test. [PR Name=DL:MHD07]
8	Tests data transfer between CU and drive. A fully formatted disk pack must be mounted and spinning on drive under test. [PR Name=DL:MHD08]

Table 5.1-28 Diagnostic Phase Descriptions for MHD-SCSI

PHASE	DESCRIPTION/WHAT IS TESTED
1	Diagnoses SCSI disk via self-tests of SCSI device controller buffer and read/write access to the MHD maintenance area. [PR Name=DL:MHDS01]

Table 5.1-29 Diagnostic Phase Descriptions for MTC

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the request isolate control signal and the control signal acknowledge from the PIC. [PR Name=DL:MTC01]
2	Tests the read/write access of the DAM. [PR Name=DL:MTC02]
3	Tests the DAM parity checker. [PR Name=DL:MTC03]
4	Tests the microdiagnostic. [PR Name=DL:MTC04]
5	*(Demand phase only.)* Tests the tape transport. A fully formatted diagnostic test tape (J-1P059AB-1 List 1M1) must be mounted on the tape transport under test. With prolonged use, the diagnostic test tape can become

	worn and cause STF results in this phase. Sometimes moving the load point (BOT) a few feet farther into the tape reel and formatting the tape at the new load point temporarily corrects STF results caused by worn tape. To format a diagnostic tape: 1. Mount a 200-foot tape with a write enable ring on an in-service MT. 2. Press the "LOAD" button. This should move the tape to the load point (BOT). 3. Press the "ON LINE" button. The ON LINE light should go on. 4. Enter the command as follows, where "c" is the MT unit number. Enter: **COPY:TAPE:DATA.TEST,TD="/dev/mtc8";** [PR Name=DL:MTC05]

Table 5.1-30 Diagnostic Phase Descriptions for MTTYC

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the request isolate control signal and the control signal acknowledge from the PIC. [PR Name=DL:MTTYC01]
2	Tests the read/write access of the DAM. [PR Name=DL:MTTYC02]
3	Tests the DAM parity checker. [PR Name=DL:MTTYC03]
4	Tests the microdiagnostic. [PR Name=DL:MTTYC04]

Table 5.1-31 Diagnostic Phase Descriptions for SCSDC

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the request isolate control signal and acknowledge from PIC. [PR Name=DL:SCSDC01]
2	Tests the read/write access of the DAM. [PR Name=DL:SCSDC02]
3	Tests the DAM parity checker. [PR Name=DL:SCSDC03]
4	Tests the microdiagnostic. [PR Name=SCSDC04]

Table 5.1-32 Diagnostic Phase Descriptions for SDLC

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the request isolate control signal and the control signal acknowledge from the PIC. [PR Name=DL:SDLC01]
2	Tests the read/write access of the DAM.[PR Name=DL:SDLC02]
3	Tests the DAM parity checker. [PR Name=DL:SDLC03]
4	Tests the microdiagnostic. [PR Name=SDLC04]

Table 5.1-33 Diagnostic Phase Descriptions for TTYC

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the request isolate control signal and the control signal acknowledge from the PIC. [PR Name=DL:TTYC01]
2	Tests the read/write access of the DAM. [PR Name=DL:TTYC02]
3	Tests the DAM parity checker. [PR Name=DL:TTYC03]
4	Tests the microdiagnostic. [PR Name=DL:TTYC04]

5.2 COMMUNICATION MODULES

5.2.1 INTRODUCTION

This section contains information about the Global Messaging Server (GMS) which consists of the Communication Module Model 1 (CM1), Communication Module Model 2 (CM2 or CM2C), or Communication Module Model 3 (CM3). Typical Communication Modules (CMs) and their respective units are described and illustrated.

For diagnostic execution input message and POKE command source information, refer to the following *5ESS*® switch Information Products (IPs):

- 235-105-110, *System Maintenance Requirements and Tools*
- 235-105-210, *Routine Operations and Maintenance Procedures*
- 235-105-220, *Corrective Maintenance Procedures*
- 235-600-700, *Input Messages*
- 235-600-750, *Output Messages*.

5.2.2 COMMUNICATION MODULE MODEL 1 - J5D001C/J5D006C

Communication Module Model 1 (CM1) consists of four cabinets. There are two Time-Multiplexed Switch (TMS) cabinets (0 and 1) and two Message Switch (MSGS) cabinets (0 and 1). Equipment in TMS cabinet 0 and MSGS cabinet 0 is duplicated in TMS cabinet 1 and MSGS cabinet 1, respectively. The cabinets operate as active major and active minor.

The TMS units terminate Switching Module (SM) Network Control Timing links and are responsible for space switching the time slots.

The MSGS units have timing and process control messages for the SMs.

Figure 5.2-1 illustrates the CM1 cabinets and their contents.

A Communication Module Processor (CMP), in the form of two circuit packs, is added to the Community 1 Message Switch Peripheral Unit (MSPU).

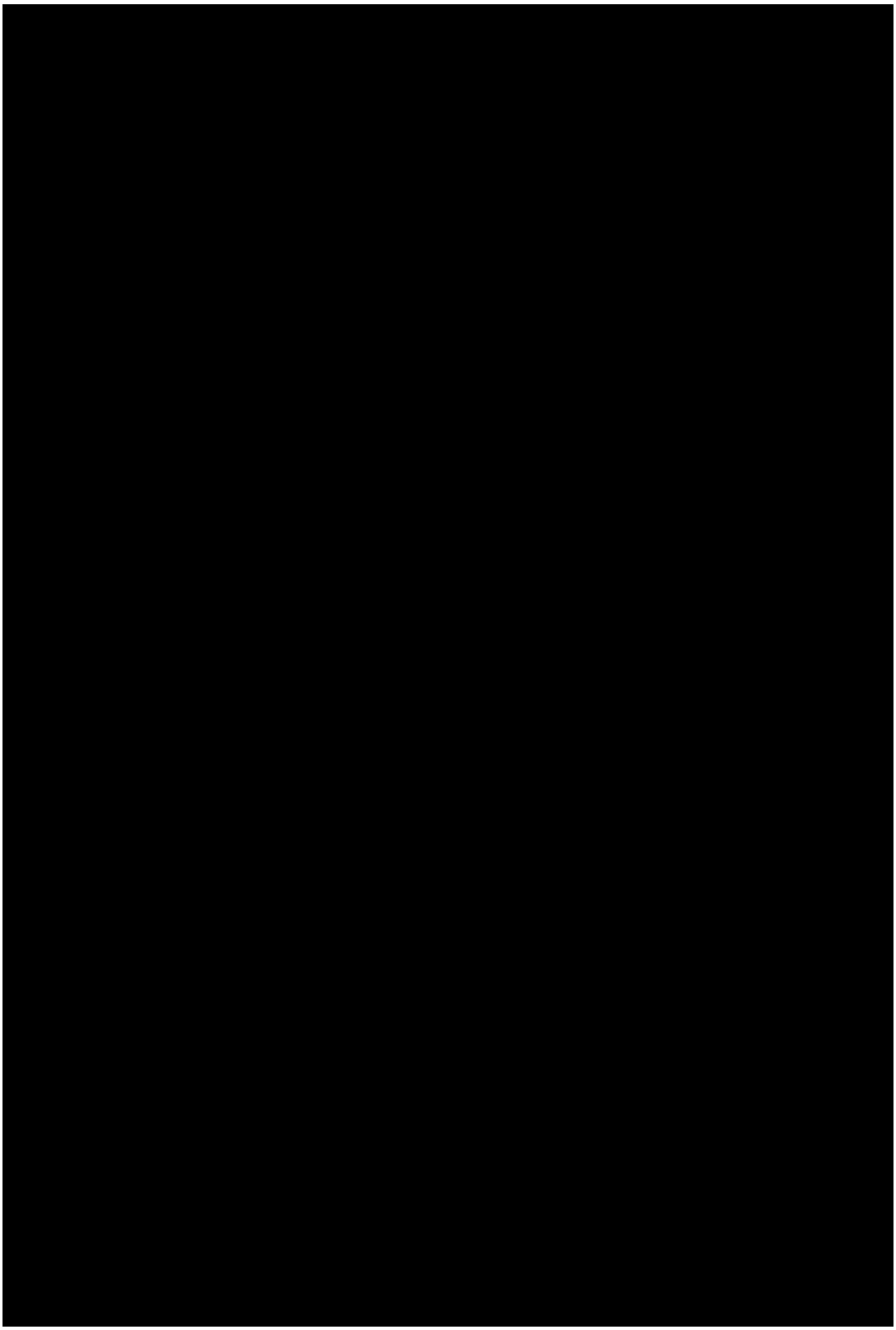

Figure 5.2-1 Communication Module Model 1

5.2.3 COMMUNICATION MODULE MODEL 2 - J5D020A-1

Communication Module Model 2 (CM2) consists of at least two cabinets (5 and 6) and as many as 12 cabinets (0 through 11). Cabinets 5 and 6 represent the basic CM2 and are duplicates.

A CM2 complex is divided into side 0 and side 1; added CM2 cabinets must be supplied in duplicated pairs, one for side 0 and one for side 1. Any CM2 cabinets added to the basic complex are positioned adjacent to cabinets 5 and 6 with side 0 cabinets descending in order from 4 to 0 and side 1 cabinets ascending in order from 7 to 11.

The two basic cabinets (5 and 6) are J5D020A-1. Added cabinets (0 to 4 and 7 to 11) are J5D020B-1. Figure 5.2-2 illustrates the basic CM2 (cabinets 5 and 6) and the respective units contained in the module.

Figure 5.2-3 illustrates the numbering scheme for a fully equipped CM2 configuration containing 12 cabinets (0 to 11).

A Communication Module Processor Unit (CMPU), in the form of CMPU units, is added to the CM2.

The optional Quad-Link Packet Switch (QLPS) release resides in CM2.

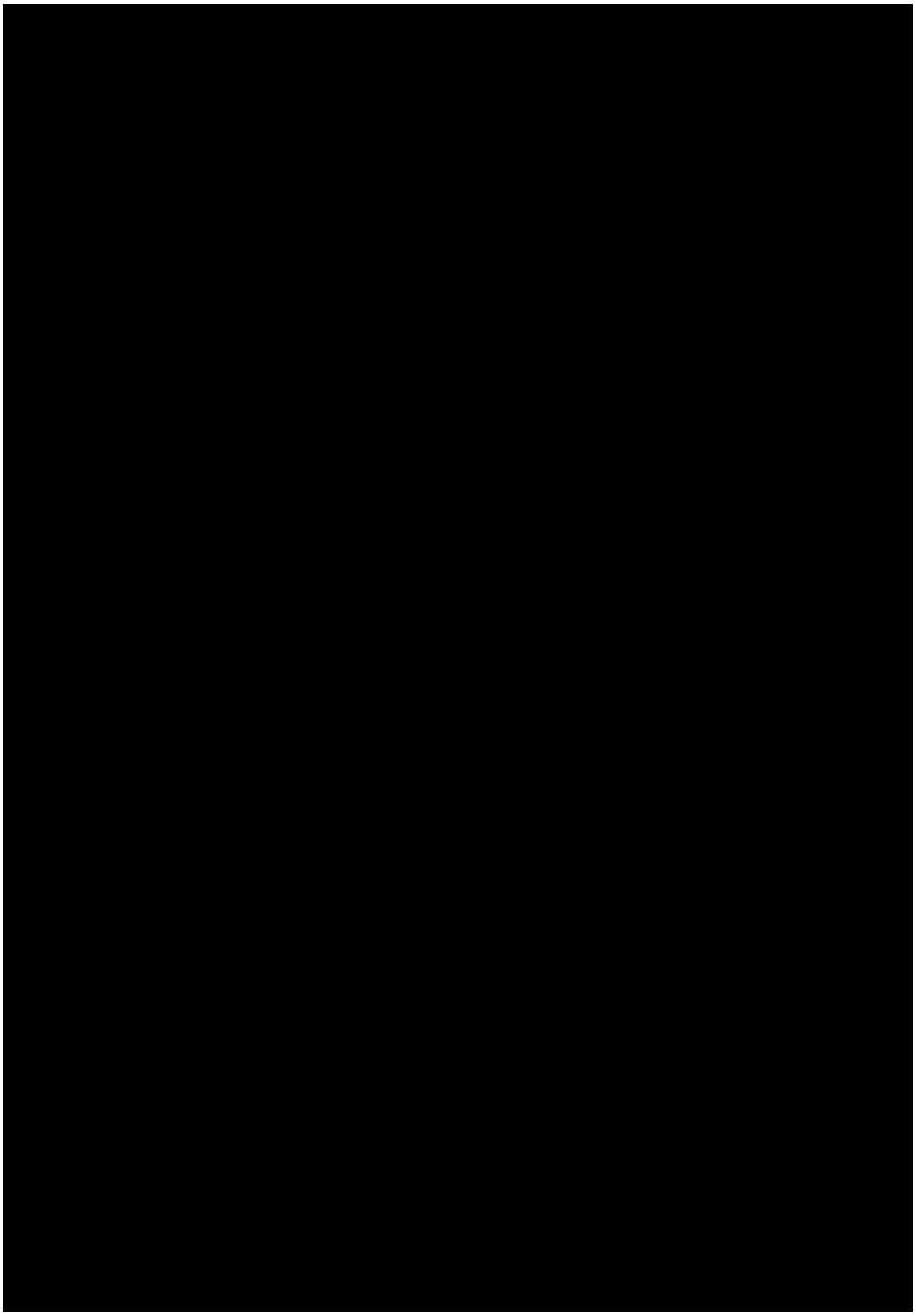

Figure 5.2-2 Communication Module Model 2 - J5D020A-1

Figure 5.2-3 Communication Module Model 2 (Fully Equipped)

5.2.4 COMMUNICATION MODULE MODEL 2 COMPACT

The Communication Module Model 2 Compact (CM2C) consists of the following three shelves:

- Two Communication Module Units (CMU) shelves - J5D020AJ-5
- One Communication Module Processor Unit (CMPU) shelf - J5D020AF-1

Figure 5.2-4 illustrates the CM2C and its respective units.

The CM2C shelves must be housed in either a Switching Module Controller (SMC) or a Line and Trunk Peripherals (LTPs) cabinet, and the cabinet must be located immediately to the left of the Administrative Module (AM). Of the two Local Switching Modules (LSMs) that the CM2C may be equipped with, only one, at most, can be an SM-2000.

The CM2C has the following limitations:

- Supports a maximum of two Switching Modules: an LSM, a Host Switching Module (HSM), an Optically Remoted Module (ORM), or a Two-Mile Optically Remoted Module (TRM).
- Supports a maximum of six Remote Switching Modules (RSMs).
- Supports a maximum of two Module Message Processors (MMPs).
- Supports a maximum of three Network Clock (NCLK) references.
- Supports a maximum of four Time-Multiplexed Switch (TMS) links.
- Supports only one single fabric configuration.
- Supports a maximum of one SM-2000.
- Does not support the Quad-Link Packet Switch (QLPS).

The CM2C configuration requires a 3B21D computer in the AM.

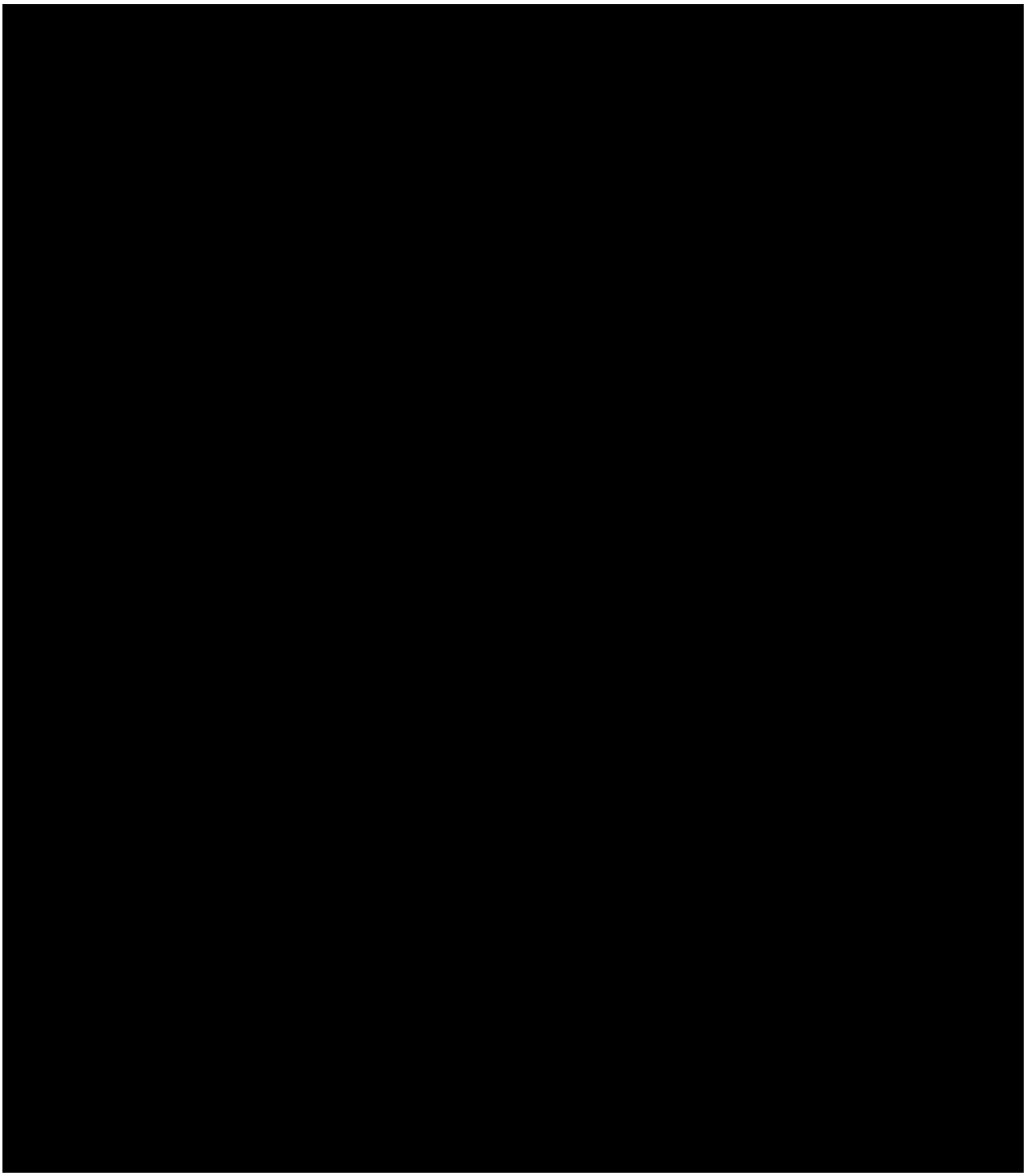

Figure 5.2-4 CM2C and CMPU Cabinet

5.2.5 COMMUNICATION MODULE MODEL 3 (CM3)

The CM3 consists of a single shelf (minimum configuration) or a full Time-Multiplexed Switch (TMS) (maximum configuration) in one cabinet. The single shelf configuration, shown in Figure 5.2-5 , consists of one Communication Module Unit Model 2 (CMU2) (J5D020C01) for side 0 and one CMU2 for side 1. The CMU2 provides the following:

- Message switch functions to terminate 192 odd and 192 even control time slots

- Functions performed by the Foundation Peripheral Controller (FPC), Communication Module Processor (CMP), Module Message Processor (MMP), Pump Peripheral Controllers (PPCs), and Quad Link Packet Switch Gateway Processor (QGP)
- Network Clock (NCLK3) and Stratum 2 Oscillator functions, including terminations for network clock external references
- Switch fabric functions including test functions, central processor intervention, Quad Link Packet Switch (QLPS) switching, message link interface to message switch, and 40 optical paddleboard positions. Note that for Network Control and Timing 2 (NCT2) links, every other paddleboard position must be vacant. Therefore for NCT2 links, the CMU2 may be equipped with a maximum of 20 paddleboards with each paddleboard supporting one even and one odd NCT2 link, for a total of 20 even and 20 odd NCT2 links.

The full TMS configuration, shown in Figure 5.2-6 , requires one CMU2 and three Time-Multiplexed Switch Units Model 4 (TMSU4s) (J5D020C01) for side 0 and one CMU2 and three TMSU4s for side 1. Each TMSU4 shelf provides an additional 48 optical paddleboard positions, supported by 2 Time-Multiplexed Switch Expansion (TMSX) circuit packs. For NCT2 links, every other paddleboard position must be vacant. Therefore for NCT2 links, each TMSU4 supports a maximum of 24 paddleboards with each paddleboard supporting one even and one odd NCT2 link, for a total of 24 even and 24 odd NCT2 links. The full TMS configuration supports a total of 92 even and 92 odd NCT2 links for each side. Note that the TMSU4 optical paddleboard positions may not be equipped unless the supporting TMSX circuit packs are equipped.

Both configurations have one modular fuse and filter unit (J5D003FJ-1) at the top of the CM3 cabinet (J5D020C01) and a fan unit (J5D003FT-1) at the bottom of the cabinet. The units are placed back to back within the cabinet with side 0 facing the front and side 1 facing the rear.

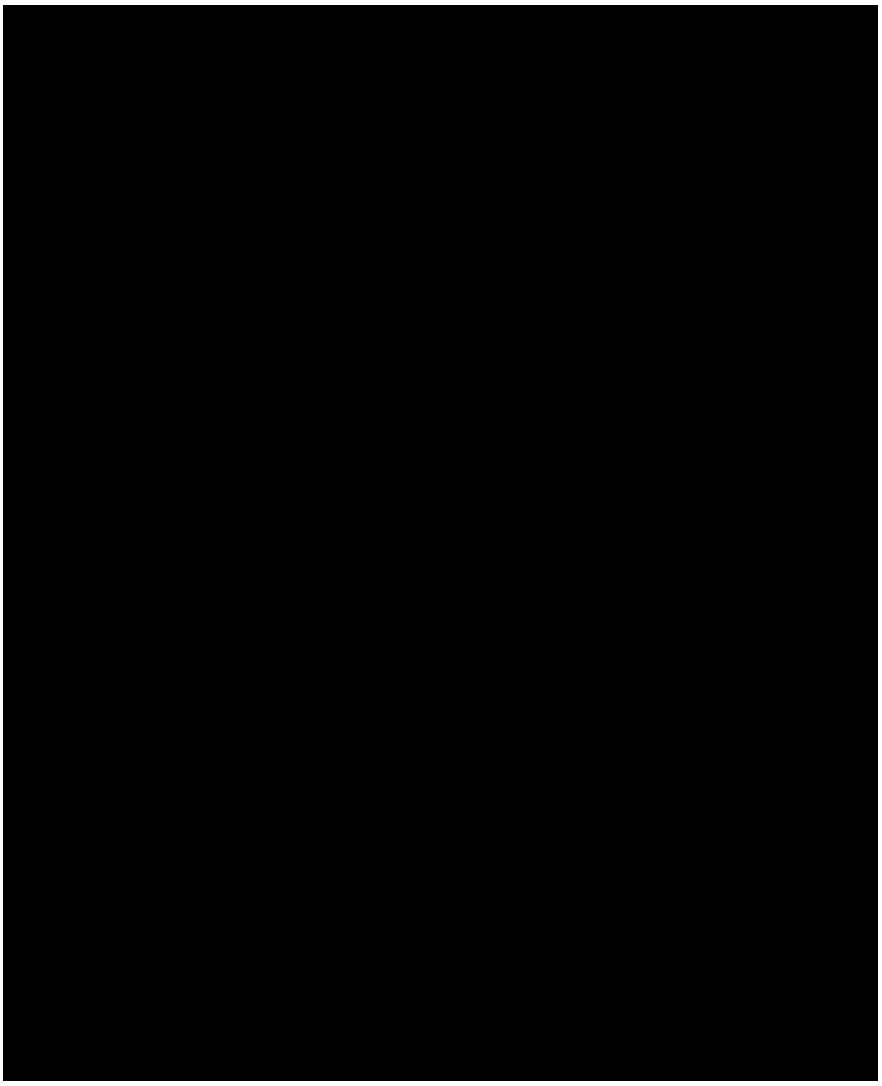

Figure 5.2-5 CM3 - Minimum Configuration

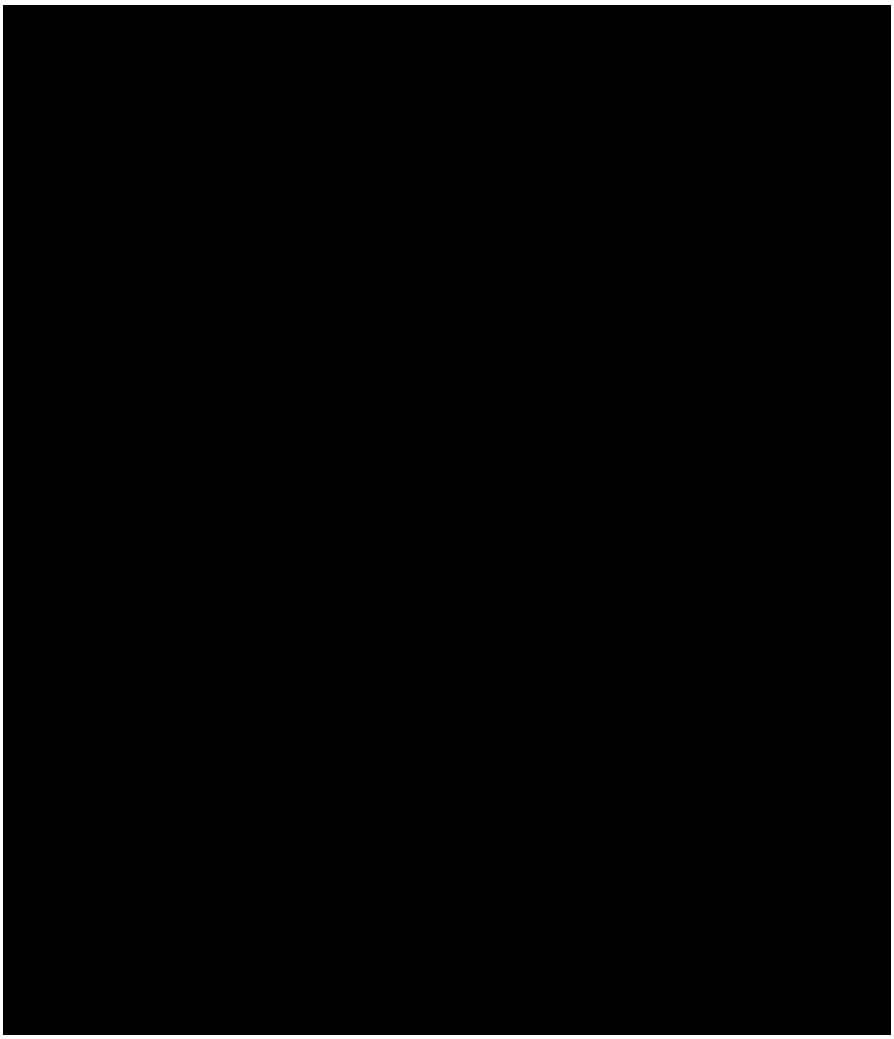

Figure 5.2-6 CM3 - Maximum Configuration

5.2.6 COMMUNICATION MODULE PROCESSOR UNIT - J5D020AF-1

The Communication Module Processor Unit (CMPU) is added to the Communication Module Model 2 (CM2). The CMPU is also part of the CM2C. Its major functions are to perform Recent Change and Call Processing in the Administrative Module.

The CMPU is a single-shelf unit, one of which is located in CM2 cabinets 5 and 6. Each unit is divided into side A and side B; each side supports up to two communities, 0 and 1. Only four circuit packs are used in the present configuration and they are in side B for Community B0. In the CM2C, the CMPU is a single-shelf unit that contains both side 0 and side 1.

The CMPU is used in the CM2C. The CMPU side 0 is in Community A0 and CMP side 1 is in Community B0.

The Communication Module Processor (CMP) uses the TN1368 core circuit pack which contains 4 MB of Dual Dynamic Random Access Memory (DDRAM) and 0.75 MB of Static Random Access Memory (SRAM). The TN1800 core circuit pack, which has 16 MB of DDRAM and 3 MB of SRAM replaces the TN1368 core circuit pack. TN1800 applies to both CM2/CM2C.

Figure 5.2-7 illustrates the location of the CMPU in the CM2 and the circuit packs in it. Refer to Figure 5.2-4 which illustrates the location of the CMPU in the CM2C and the circuit packs in it.

In the *5ESS*® switch, the CMPU shelf has been divided into two communities, 0 and 8; 0 is the CMP side (side B) of the shelf for CMPs and 8 is the Quad-Link Packet Switch Gateway Processor (QGP) side (side A) of the shelf for Quad-Link Packet Switch Gateway Links (QGLs.) The QGP community is optional. Figure 5.2-8 shows a typical QGPs (4QGP) network configuration.

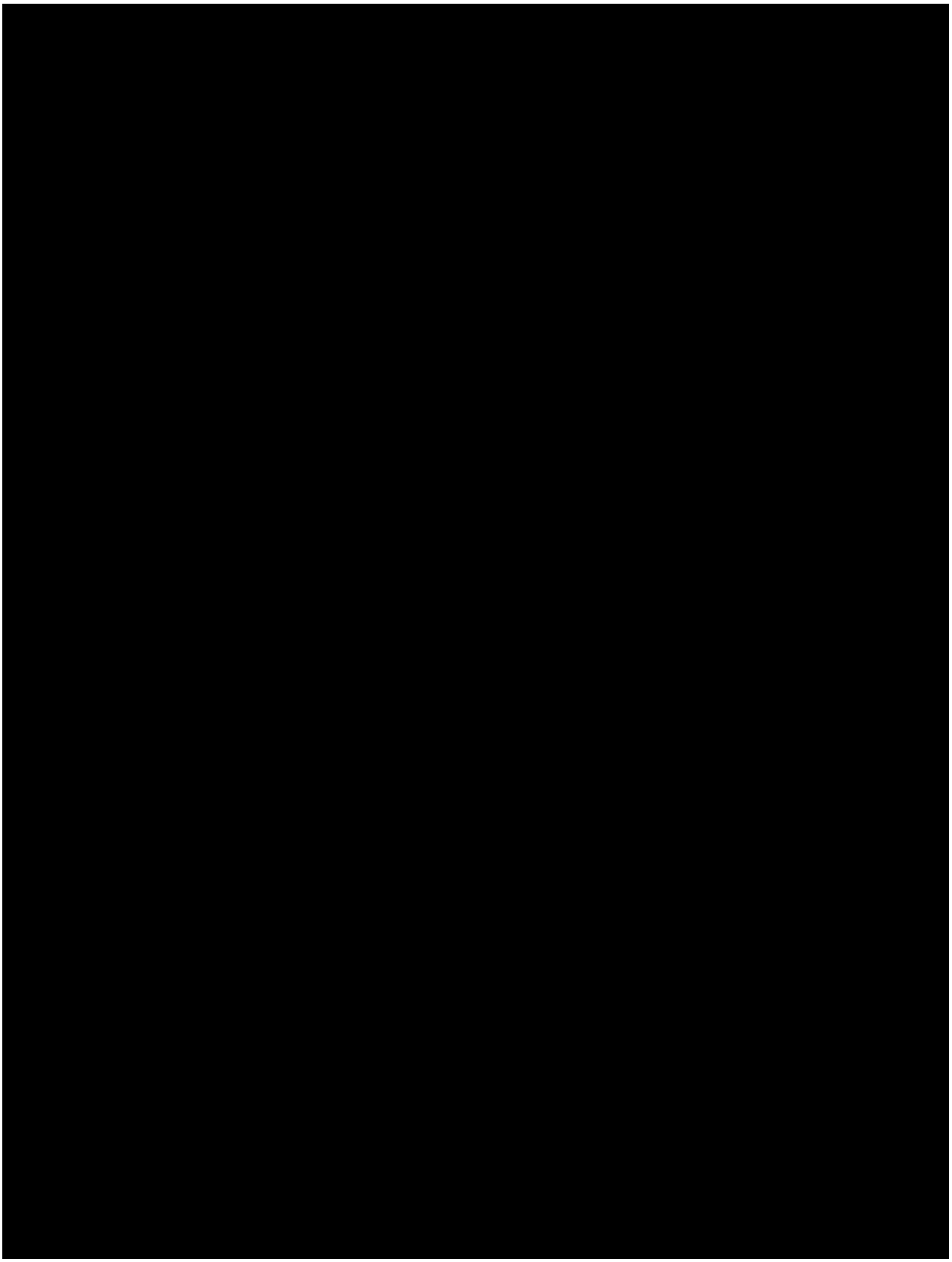

Figure 5.2-7 Communication Module Processor Unit, - J5D020AF-1

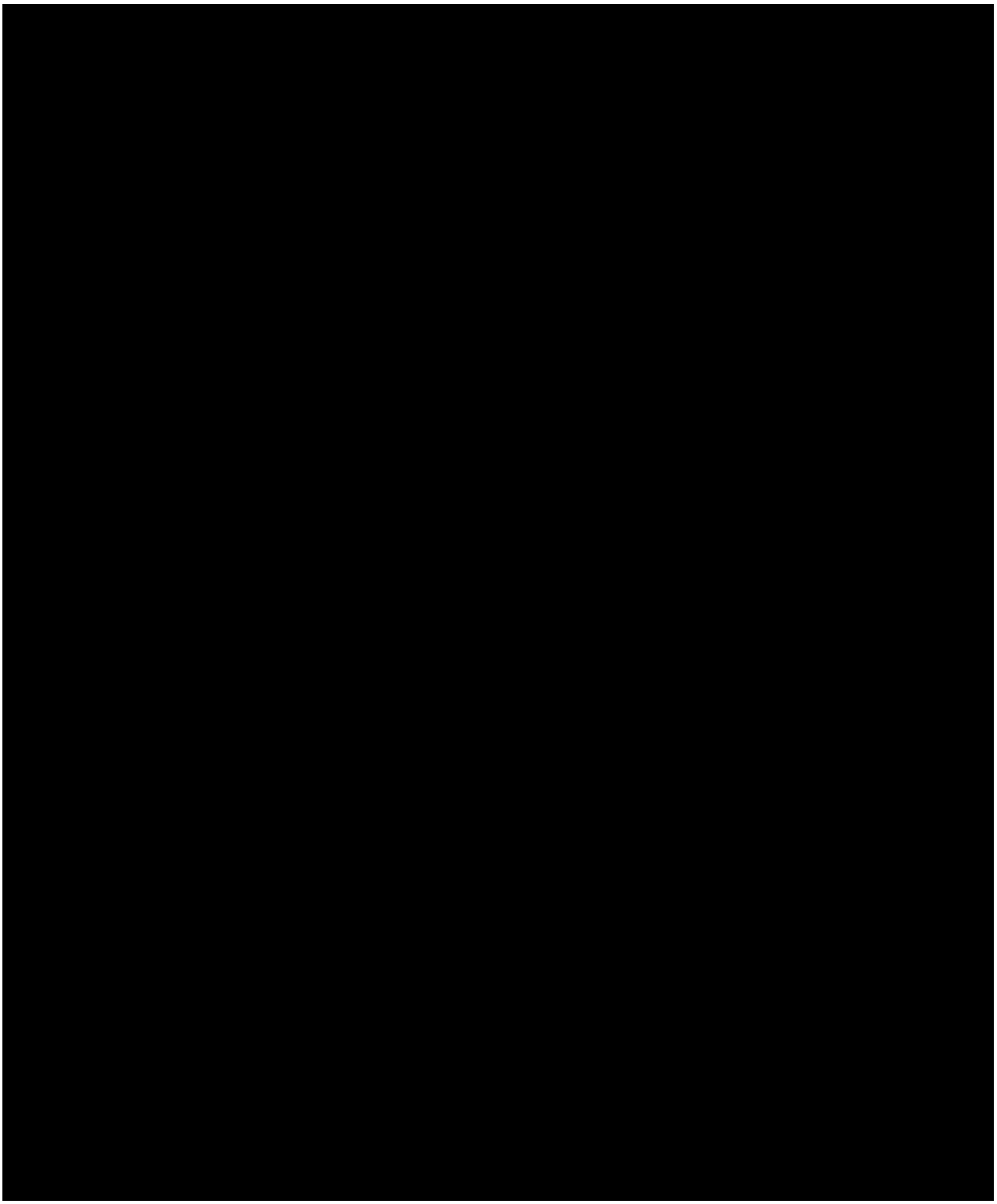

Figure 5.2-8 Communication Module Processor Unit with Optional QGP - J5D020AF-1

5.2.7 COMMUNICATION MODULE UNIT - J5D020AJ-5

The Communication Module Unit (CMU) is the basic unit of the CM2C. CMU sides 0 and 1 are located at Equipment Location (EQL) positions 45 and 53, respectively, in either the SMC or an LTP cabinet, which must be located immediately to the left of the AM.

The CMU consists of the following function blocks:

- The KBN10 board has the Message Switch Controller Unit □ Model 3 (MSCU3). This board is also used in the CM2s MSCU3.
- The TN856C and UN173 boards are Foundation Peripheral Controllers (FPCs). These boards are also in the CM2s FPC.
- The TN856C and TN886 boards are the Pump Peripheral Controllers (PPCs). These boards are the same ones used as the CM2's PPC.
- The TN856C and TN870 boards are the Module Message Processor (MMP). These boards are the same ones that are used as the CM2s MMP.
- The UN187 board is the message interface controller. This board is the same one used in the CM2.
- The TN1276 and TN1274B, along with either the TN1284B or TN1286B boards, are the Network Clock (NCLK). These boards are the same ones used as the CM2s NCLK2.
- The TMS function is provided by the TN1812, TN1813, and TN1830 boards. These boards are new with the CM2C.

All of the above mentioned units in the CMU are powered by a single power supply, except for the network clock oscillator which has its own power supply as it does in the CM2.

5.2.8 COMMUNICATION MODULE UNIT 2 (CMU2) - J5D020C01

The CMU2 shelves are located at vertical EQL 24F (side 0) and 24R (side 1). Each shelf contains five circuit packs, cabling for each side, and 40 paddleboard positions (up to 20 of which can be used for optical paddleboards for NCT2 links connection). Each CMU2 (one for side 0 and one for side 1) contains the following:

- One message switch (MSGS) pack (MMD100)
- One Network Clock and Control (NCC) pack (MMD101)
- One Oscillator pack (MMB100)
- Two Time-Multiplexed Switch Foundation (TMSF) packs (MMC100)
- Up to 20 optical paddleboards for NCT2 links connection. (Note that each optical paddleboard supports one even and one odd NCT2 link.)

5.2.9 COMMUNICATION MODULE CONTROL UNIT - J5D020AA-1

The Communication Module Control Unit (CMCU) is provided only in the two basic Communication Module (CM) cabinets, 5 and 6, and is located at EQL position 28 only. Unit 0 is in cabinet 5 and unit 1 is in cabinet 6.

The three main functions of the CMCU are as follows:

(1) To provide timing for the switch. The type of oscillator pack (TN1284 or TN1286) and microcode of the TN1276 determines the type of office Network Clock as Stratum 2 or Stratum 3.

(2) To control the switching of the Time-Multiplexed Switching Unit - Model 2 (TMSU2) fabric. EQLs 170 and 178 are used only in Dual Fabric arrangements.

(3) To regulate the control time slots between the link interface packs of the TMSU2 or TMSU3 and the Module Message Processors (MMPs) located on the Message Switch Peripheral Unit - Model 3 (MSPU3) or the PPC located on the MSCU2.

The UN310 (EQL 116) is used only when no growth cabinets are supplied. The UN310 circuit pack performs the Emitter-Coupled Logic Bus (EBUS) function when no CM growth cabinets are equipped.

Figure 5.2-9 illustrates the location of the CMCU2 in the basic module and the circuit packs contained in the unit.

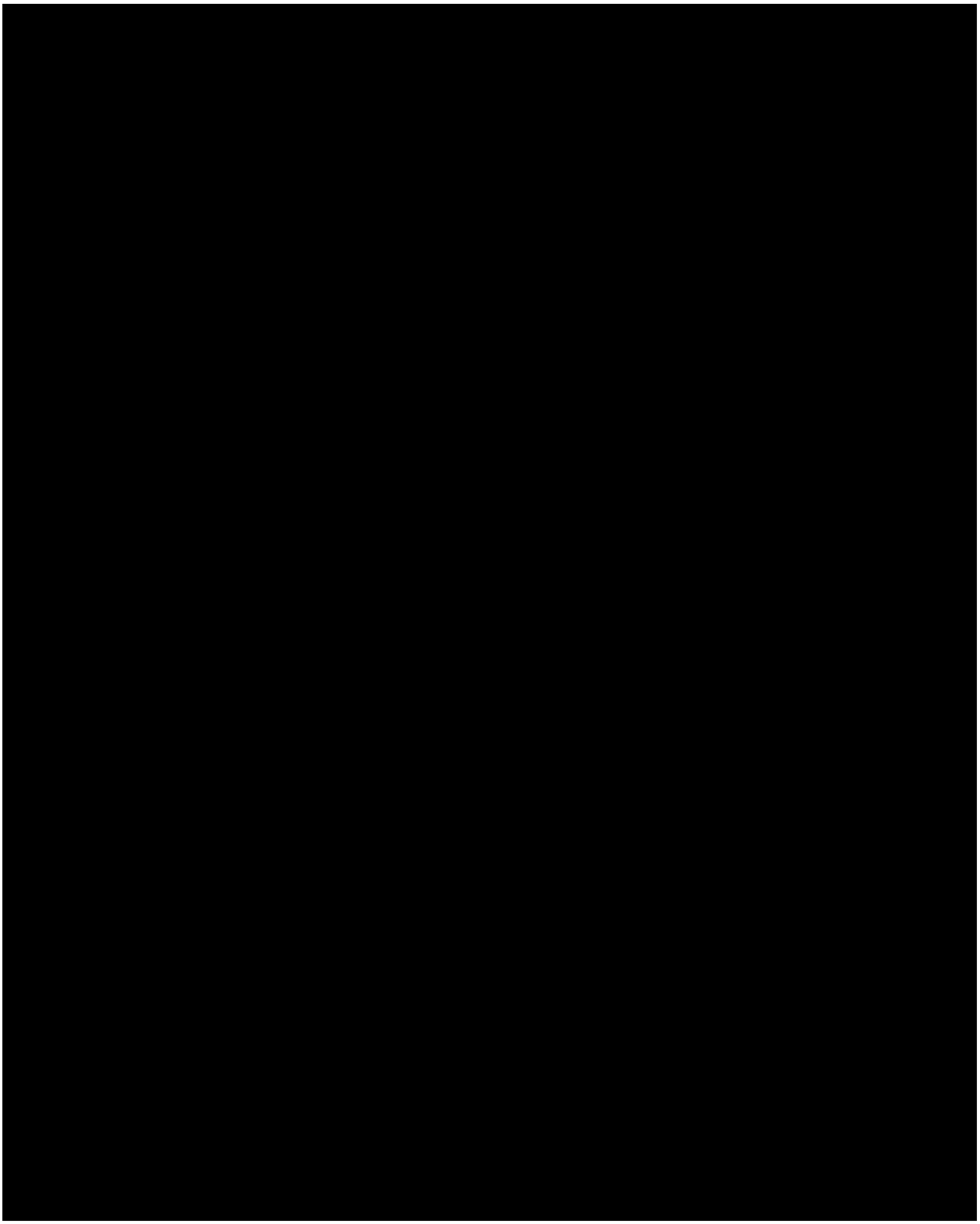

Figure 5.2-9 Communication Module Control Unit - J5D020AA-1

5.2.10 EMITTER-COUPLED LOGIC BUS (EBUS) - J5D020AE-1

The Emitter-Coupled Logic Bus (EBUS) originates from the CMCU and provides the metallic path which the CMCU uses to communicate with every TMSU2. The EBUS (J5D020AE-1) is a single-shelf unit that distributes clock and data to/from all switch units in the TMS. The EBUS unit connects the TMSUs with the

time-multiplexed switch controller circuit located in the CMCU.

The EBUS shelf is located only in growth cabinets (0-4 and 7-11) in vertical location 28. Table 5.2-1 lists the circuit packs that make up the EBUS. See J5D020B-2 (CM cabinet) for specific circuit pack equipage and locations. For offices equipped with a two-cabinet CM2, the EBUS function is performed by circuit pack UN310 located in the CMCU shelf.

Table 5.2-1 EBUS Circuit Packs

CIRCUIT PACK NUMBER	CIRCUIT PACK NAME	CABINETS CONTAINING EBUS CIRCUIT PACKS
UN197	Multiplex Control	All growth cabinets (0-4 and 7-11).
UN198	Loop Board	Cabinets 4, 2, or 0; and cabinets 7, 9, or 11 when previous cabinets are the last CM cabinet.
UN310	Data End Tap Board	Cabinets 4 and 7 in a growth cabinet office. (The UN310 is equipped in the CMCU shelf in a two-cabinet CM2.)
UN311	Data End Board	Cabinets 0-3 and 8-11.
UN312	Clock End Tap Board	Cabinets 4 and 7.
UN313	Clock Tap	Cabinets 0-3 and 8-11.
UN500	Transmit Data Repeater	Cabinets 1, 3, 8, and 10.
UN501	Transmit Control Repeater	Cabinets 1, 3, 8, and 10.
UN503	Receive Data Repeater	Cabinets 0, 2, 9, and 11.
UN504	Receive Control Repeater	Cabinets 0, 2, 9, and 11.

5.2.11 MESSAGE INTERFACE CLOCK UNIT - J5D006ED-1

The Message Interface Clock Unit (MICU) is a single-shelf assembly containing timing and control time slot interface circuit packs. The MICU can interface up to four communities of Module Message Processors (MMPs). Each community is cross-coupled to the mate MICU.

The network clock is configured in the active/standby arrangement. The standby clock receives timing from the active clock, and the active clock receives timing from an oscillator board equipped within the MICU.

Figure 5.2-10 illustrates the MICU and the circuit packs in it.

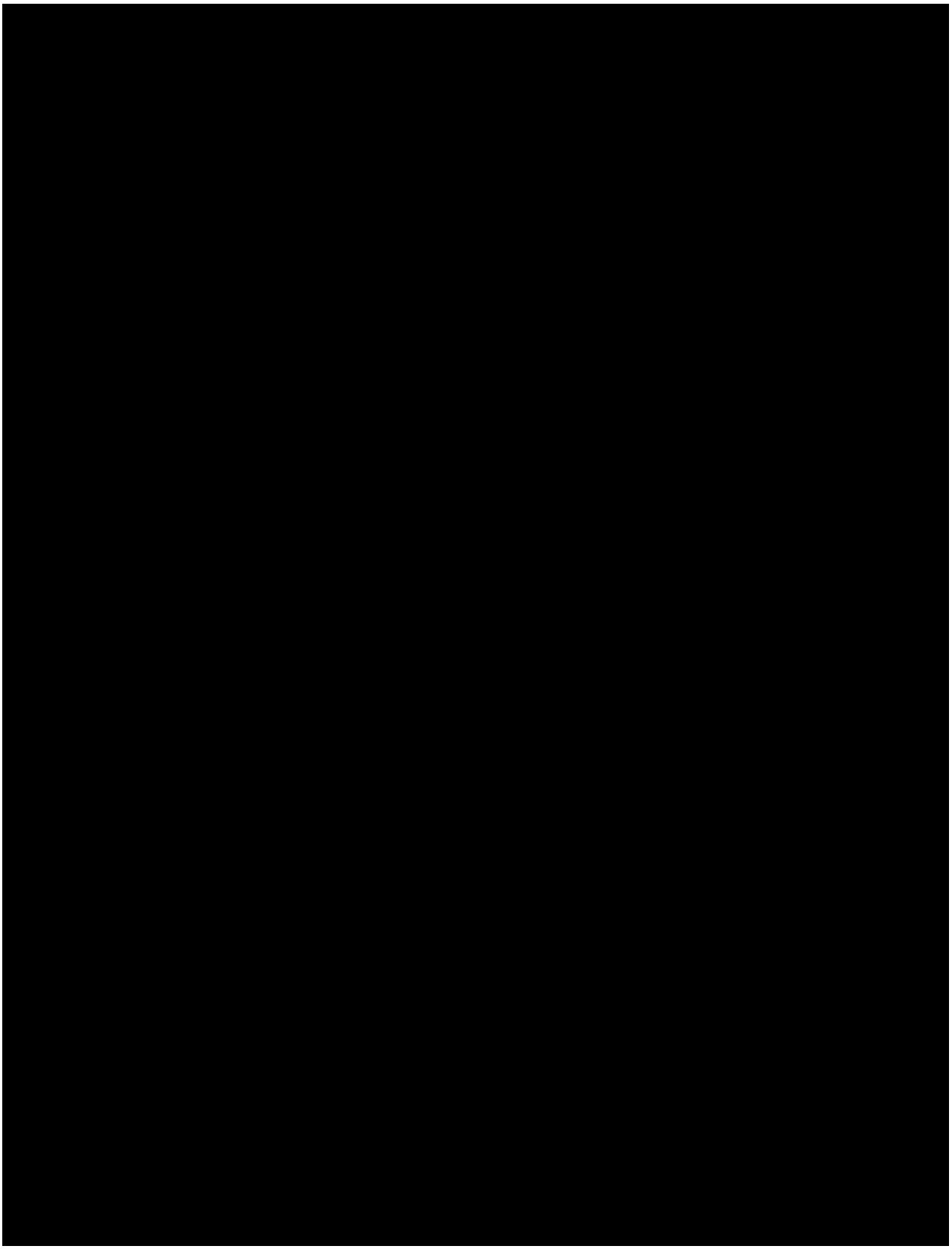

Figure 5.2-10 Message Interface Clock Unit - J5D006ED-01

5.2.12 MESSAGE SWITCH CONTROL UNITS

5.2.12.1 Message Switch Control Unit (MSCU) - J5D006AB-1

The Message Switch Control Unit (MSCU) is located at EQL 45 in the Communications Module 1 (CM1) Message Switch (MSGS) cabinet 1. Functionally, the unit is divided into two areas: Power Control and Power Converters, and Message Switch Control.

Figure 5.2-11 illustrates the location of the MSCU in MSGS cabinet 1 and the respective circuit packs in the unit.

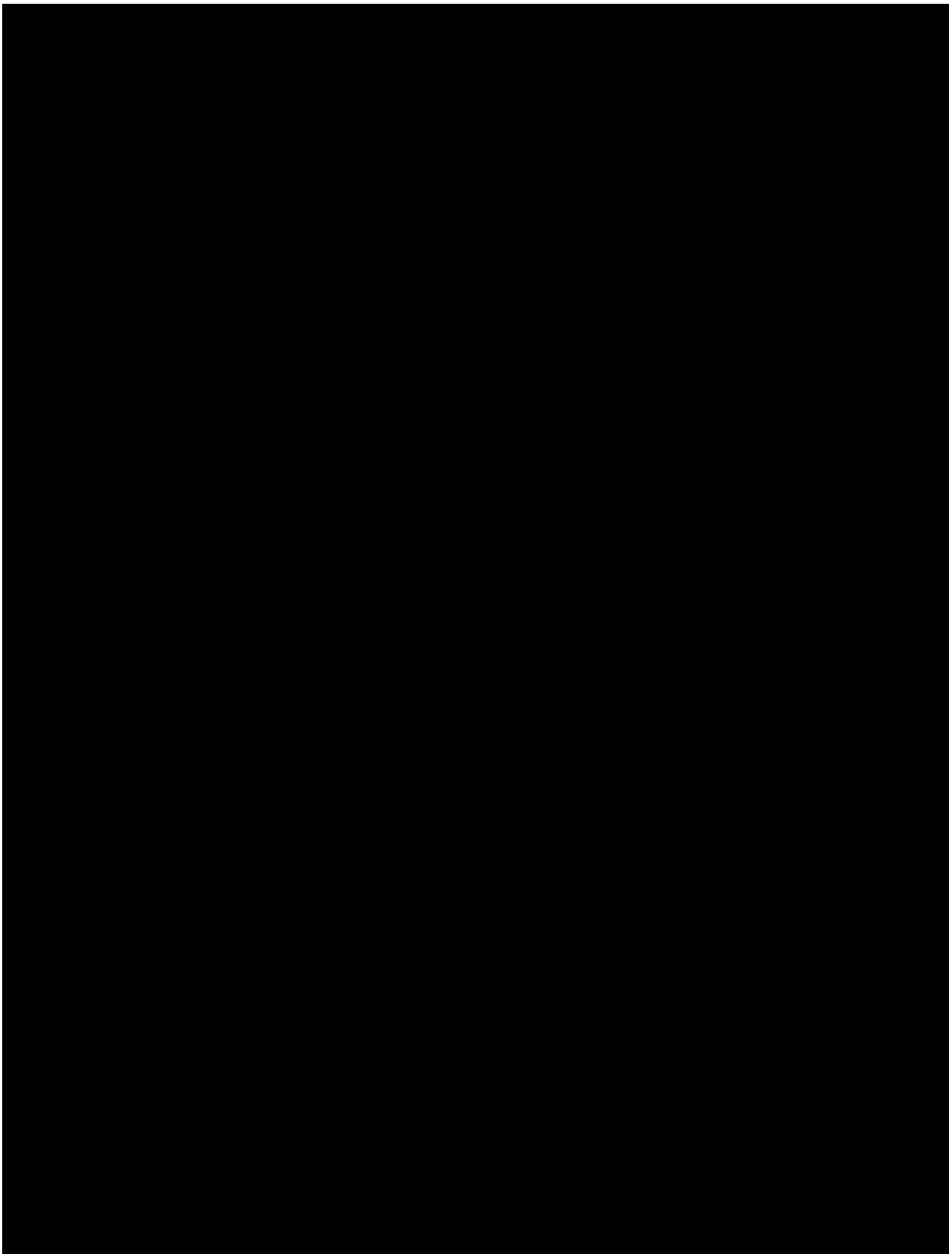

Figure 5.2-11 Message Switch Control Unit - J5D006AB-1

5.2.12.2 Message Switch Control Unit Model 2 - J5D020AB-1

The Message Switch Control Unit - Model 2 (MSCU2) is located at EQL 45 in Communications Module Model 2 (CM2), cabinets 5 and 6. Functionally, the unit is divided into four areas: Power Control and Power Converters, Pump Peripheral Controllers (PPCs), Foundation Peripheral Control (FPC), and Message Switch Control. The MSCU provides the interface between the Administrative Module (AM) and the MMPs. The MSCU is a single-shelf unit primarily equipped with the following circuit packs:

- Peripheral Interface Controller Model 2
- Input/Output Microprocessor Interface (IOMI)
- Duplex Dual Serial Bus Selector
- Pumpable Micro Control Store
- Bus Interface Controller (BIC).

The unit provides four basic functions as described as follows:

(1) Reformats data received from the AM or Communication Module Processor Unit (CMPU) and transmits it to the other units in the cabinet.

(2) Reformats data received from other units in the cabinet and transmits it to the AM or CMPU.

(3) Interprets destination codes of incoming control time slots and switches the control time slots to the AM or another Switching Module (SM).

(4) Provides control of the other units in the CM2 cabinet.

Figure 5.2-12 illustrates the location of the MSCU2 in the CM cabinets 5 and 6 and the respective circuit packs in the unit.

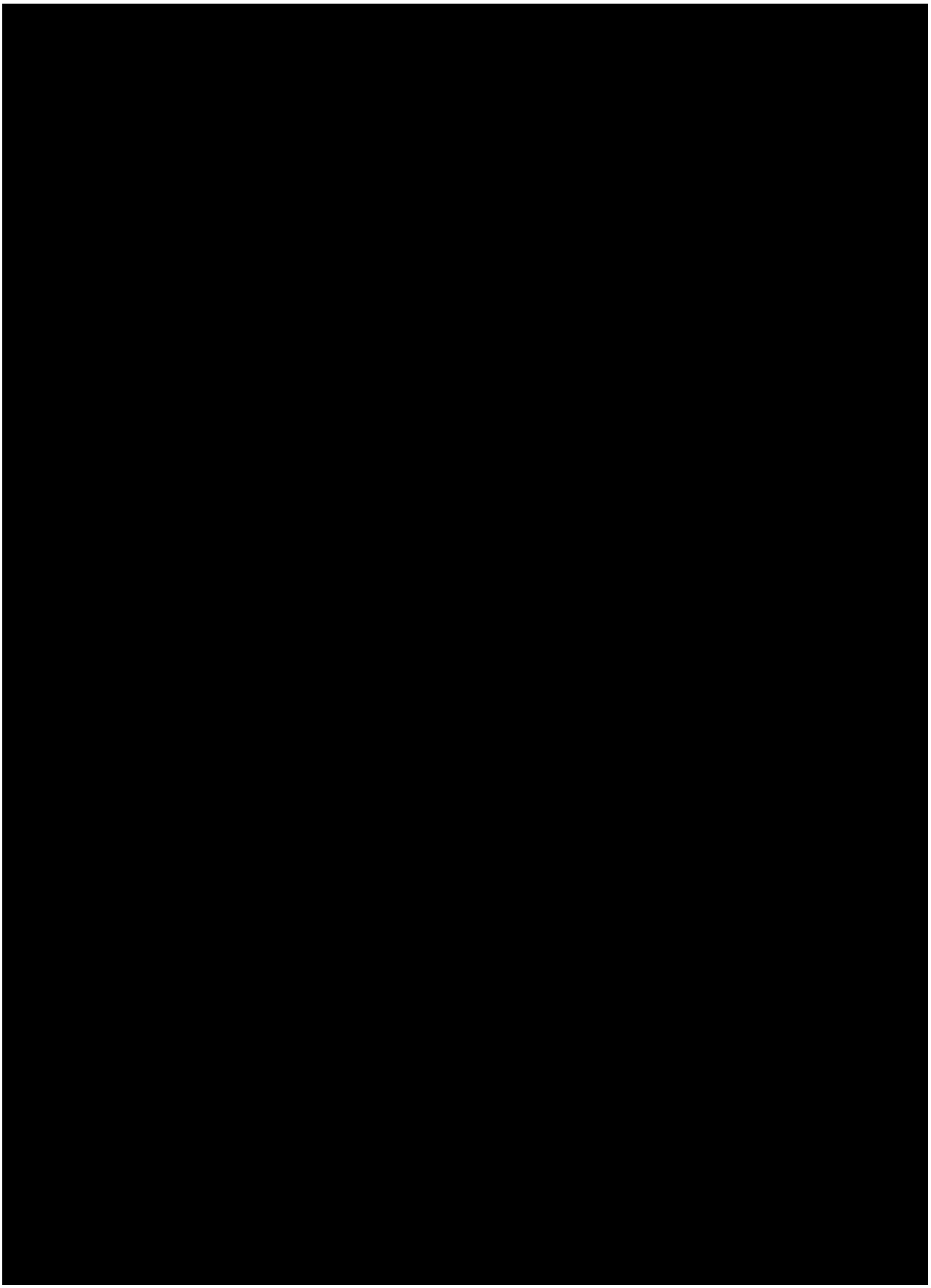

Figure 5.2-12 Message Switch Control Unit Model 2 - J5D020AB-1

5.2.12.3 Message Switch Control Unit Model 3 - J5D020AH-5

The Message Switch Control Unit - Model 3 (MSCU3) controls message transfers among the Administrative Module (AM) and as many as 14 peripheral control communities, each consisting of one to four peripheral controls. A Peripheral Controller (PC) can be a Module Message Processor (MMP), Foundation Peripheral Control (FPC), Pump Peripheral Controller (PPC), or Communication Module Processor (CMP). The community with the FPC and PPC is limited to two PCs and is contained within the MSCU3. Message transfers are accomplished under the control of a bit-slice processor on the Input/Output Processor 2 (IOP2)/Message Switch Control 3 (MSC3) circuit pack.

The MSCU3 provides the following functions:

- Performs the serial-to-parallel conversion of data received from the AM and the parallel-to-serial conversion of data transmitted to the AM.
- Provides one to four Input/Output Microprocessor Interfaces (IOMIs) to interface the IOP2/MSC3 with the MMPs, FPC, and PPC.
- Provides control to transfer data among MMPs or between the AM and MMPs.
- Provides control to transfer data between the AM and the FPC or PPC.
- Performs self-diagnostics that are resident in IOP2/MSC3 firmware.
- Provides control and diagnostic access for the Dual Message Interface (DMI), Network Clock (NCLK), and Time-Multiplexed Switch Model 2 (TMS2) via the FPC.
- Provides a PPC for loading the Switching Module (SM) with data at 192 kbps.
- Provides both manual and AM control of the MSCU3 from an in-service/out-of-service point of view.

The MSCU3 can be equipped with up to three additional external IOMIs to provide additional communities.

5.2.12.3.1 Message Switch Peripheral Processor

The Message Switch Peripheral Processor (MSPP) is the controlling circuit pack of all message switch peripheral controller applications. It is a single-board processor with an interface through an IOMI bus to the IOP2/MSC3 as well as an interface to application boards needed for each specific function. The MSPP contains a 16-bit microprocessor, 128 KB of Dynamic Random Access Memory (DRAM), 8 KB of Static RAM (SRAM), 16 KB of Erasable Programmable Read-Only Memory (EPROM), and clock circuits to ensure its own sanity and to provide needed timing to application boards.

5.2.12.3.2 Foundation Peripheral Controller

The Foundation Peripheral Controller (FPC) provides the interface for rapid pumping on the SM. Data are pumped from the disk in the AM through the IOP2/MSC2 to the PPC through the on-board IOMI bus. The PPC then sends the data to the CMCU through a Message Interface Bus (MIB). The CMCU sends the data to the TMS2 where it is distributed to the destination SM via a Network Control and Timing (NCT) link.

5.2.12.3.3 Control and Display

The Control and Display (C&D) circuit packs run in-service/out-of-service control and the alarming of the power converters. The MSCU3 uses two C&D circuit packs; one provides manual and AM control of the FPC, PPC, and their associated MSPPS, and the other provides manual and AM control of the IOP2/MSC3 and the IOMIs. The AM monitors the C&D circuit packs for fuse alarms, power status (alarms, manual off, and power on) and requests for OOS.

5.2.12.3.4 Power Converter - 495FB

The converter changes a nominal -48 volt input to a well-regulated +5 volt output for applications in the MSCU3 circuits. The power unit is pulse-width controlled for regulation, self-oscillating, and operates at a fixed frequency. The 495FB provides +5 volts at 250 watts. The MSCU3 uses two converters; one provides power for the FPC, PPC, and their associated MSPPs, and the other provides power for the IOP2/MSC3 and the IOMIs.

Figure 5.2-13 shows the layout of the MSCU3 circuit packs.

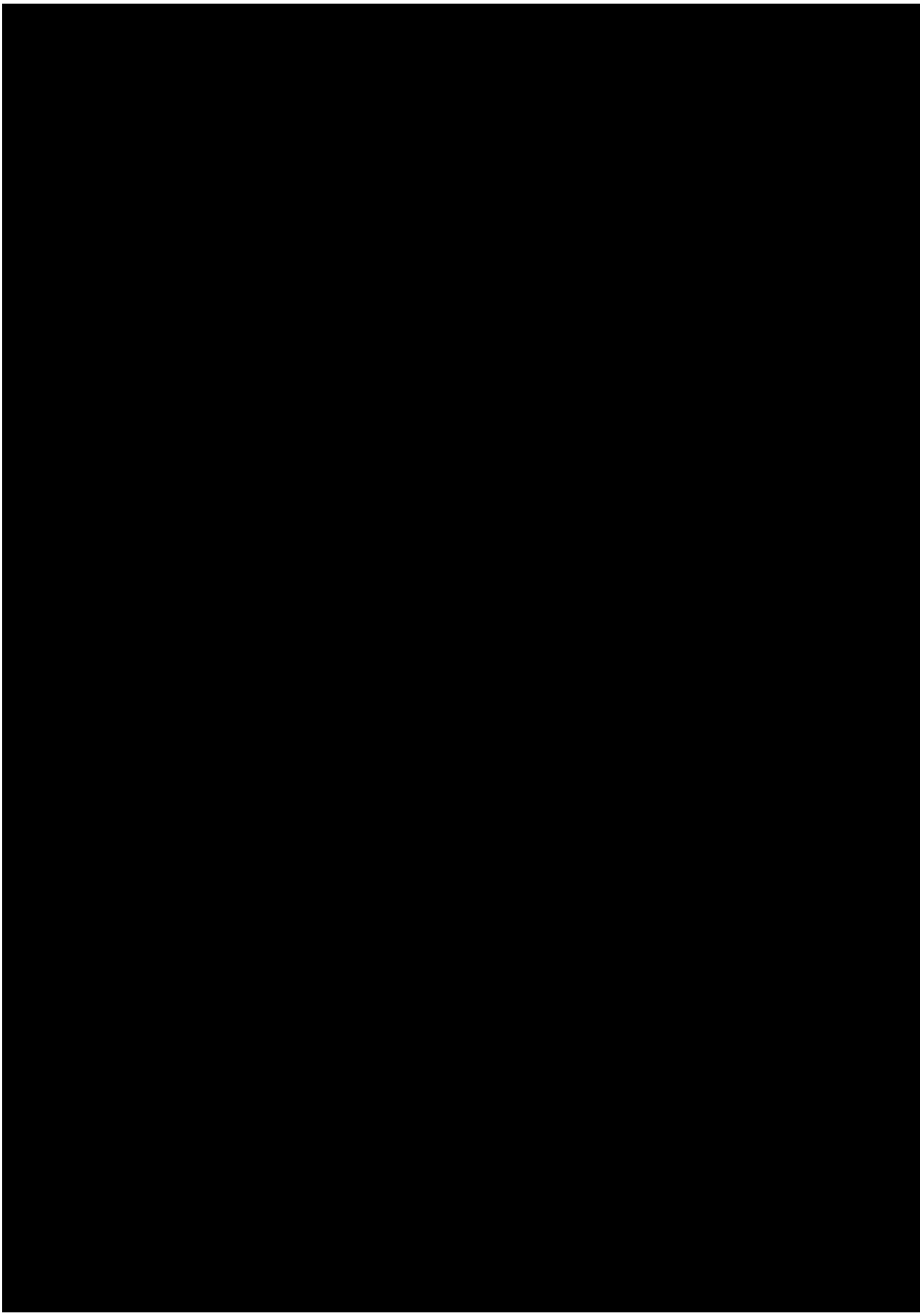

Figure 5.2-13 Message Switch Control Unit Model 3 - J5D020AH-5

5.2.13 QUAD-LINK PACKET SWITCH NETWORK

For the CM2, an optional message switch, the Quad-Link Packet Switch (QLPS), is available to support the higher message traffic of the SM-2000 and the *5ESS*® switch. For the CM3, the QLPS functionality is incorporated into the TMSF circuit pack and is not optional.

The QLPS is essentially a high-speed tandem message switch designed to support the increased message traffic from the SM-2000 and its Message Handler (MH) due to the higher volume of calls. The QLPS communicates with the existing *5ESS*® switch Message Switch (MSGS) through a QLPS Gateway Processor (QGP). The MSGS supports the SM and SM-2000 without QLPS, but to effectively use the higher call capacity of the SM-2000, the eventual addition of the QLPS is recommended.

The QLPS has the following significant impacts:

- The QLPS enables a capacity increase of the *5ESS*® switch to one million completed Plain Old Telephone Service (POTS) calls per hour.
- The QLPS gives the *5ESS*® switch the ability to handle the increased message traffic generated by the message-intensive, distributed-intelligence architecture of the Advanced Intelligent Network.

The QLPS network is an overlay network which provides high- bandwidth/low-latency message transport between an SM-2000 and other SM-2000s, between an SM-2000 and SMs, the Administrative Module (AM), Communication Module Processor (CMP), Direct Link Node (DLN) via the MSGS Peripheral Interface Controller (PIC), and the Foundation Peripheral Controller (FPC). The QLPS network increases the bandwidth for Operating System for Distributed Switching (OSDS) messages from 48 kbps to 896 kbps.

The QLPS network is composed of the following elements: Quad Link Packet Switch (QLPS), QLPS Gateway Processor (QGP), QLPS-QGP Link and, for CM2, the Quad-Link Interface Model 2 (QLI2). It also includes a new message handler used as a link to the SM-2000.

For the CM2, Figure 5.2-8 illustrates the circuit pack locations for the QGP and QGL, while Figures 5.2-19 and 5.2-20 illustrate the circuit pack locations for the Foundation Link Interface (FLI), QLI, QLI2, and QLPS circuit packs. As noted earlier for the CM3, the QLPS functionality is built into the TMSF circuit pack of the CMU2.

5.2.13.1 Quad-Link Packet Switch

The QLPS is the hub of a ``star network.'' Its purpose is to assemble frames [encapsulate the actual Operating System for Distributed Switching (OSDS) Common Channel Signaling (CCS) Messages] received from network endpoints, verify basic frame integrity, determine the destination, and store those frames until delivery to the destination can be accomplished.

5.2.13.2 Quad-Link Gateway Processor

The QLPS Gateway Processor (QGP) is a Message Switch (MSGS) subdevice, which provides access to/from an MSCU and the QLPS via a QLPS Gateway Link (QGL). The QGP provides QLPS with an interface to the existing *5ESS*® switch communications foundation. Messages received at the QGP can be transmitted to the AM, CMP, DLN, FPC SMs or into the appropriately addressed QLPS network, and the SM-2000.

NOTE: For the CM2, the QLPS network may be equipped with 0, 1 or 2 QGPs per MSGS side; depending on the QGP configuration, there may 0, 2 or 4 QGLs per QGP. For the CM3, the 2-QGP configuration is always used, one QGP on each MSGS side.

5.2.13.3 Message Handler

The Message Handler (MH) provides access from the SM-2000 CORE40 to the QLPS network. The connection between the MH and QLPS is via a nailed-up ``pipe'' through the Time-Multiplexed Switch/Time Slot Interchanger (TMS/TSI).

5.2.13.4 QLPS-QGP Link

The QLPS-QGP Link provides the interconnection of the QGP and QLPS via dedicated electrical connections. Each complex of QGPs on a MSGS has four QGL connections, one to each QLPS.

The connection between the MH and the QLPS is via a nailed-up ``pipe'' through the TMS/TSI.

5.2.13.5 Quad-Link Interface Model 2

The Quad-Link Interface Model 2 (QLI2) circuit pack plugs into the Communications Module Model 2 (CM2) and provides the Network Control and Timing 2 (NCT2) interface between the CM2 and the SM-2000. The QLI2s plug into any existing Quad-Link Interface (QLI) slot in the TMS, except for the Foundation Link Interface (FLI) slot, which is reserved for the TN883. CM2s equipped with QLI2s support both single- and dual-fabric configurations. For the CM3, the QLPS functionality is incorporated into the TMSF circuit pack of the CMU2.

5.2.14 MESSAGE SWITCH PERIPHERAL UNITS

5.2.14.1 Message Switch Peripheral Unit (Community 1) - J5D006AD-1

The Message Switch Peripheral Unit Model 2 (MSPU2) is in Equipment Location (EQL) 53 in all Communication Module Model 1 cabinets. The main function of the MSPU2 is to process the control time slots and send them to the Message Switch Control Unit (MSCU) for switching to the Administrative Module (AM) or to other Switching Modules (SMs). Each MSPU is identified by a unique community number (1, 2, or 3) plus an optional MSPU if desired.

The Communication Module Processor Unit (CMPU) has been added in the form of two circuit packs, TN1369 and TN1368. Details for adding the Communication Module Processor (CMP) are shown in drawing ED-5D687-30.

Figure 5.2-14 illustrates the location of the MSPUs in CM cabinet 1 and the respective circuit packs in the unit, including the CMP.

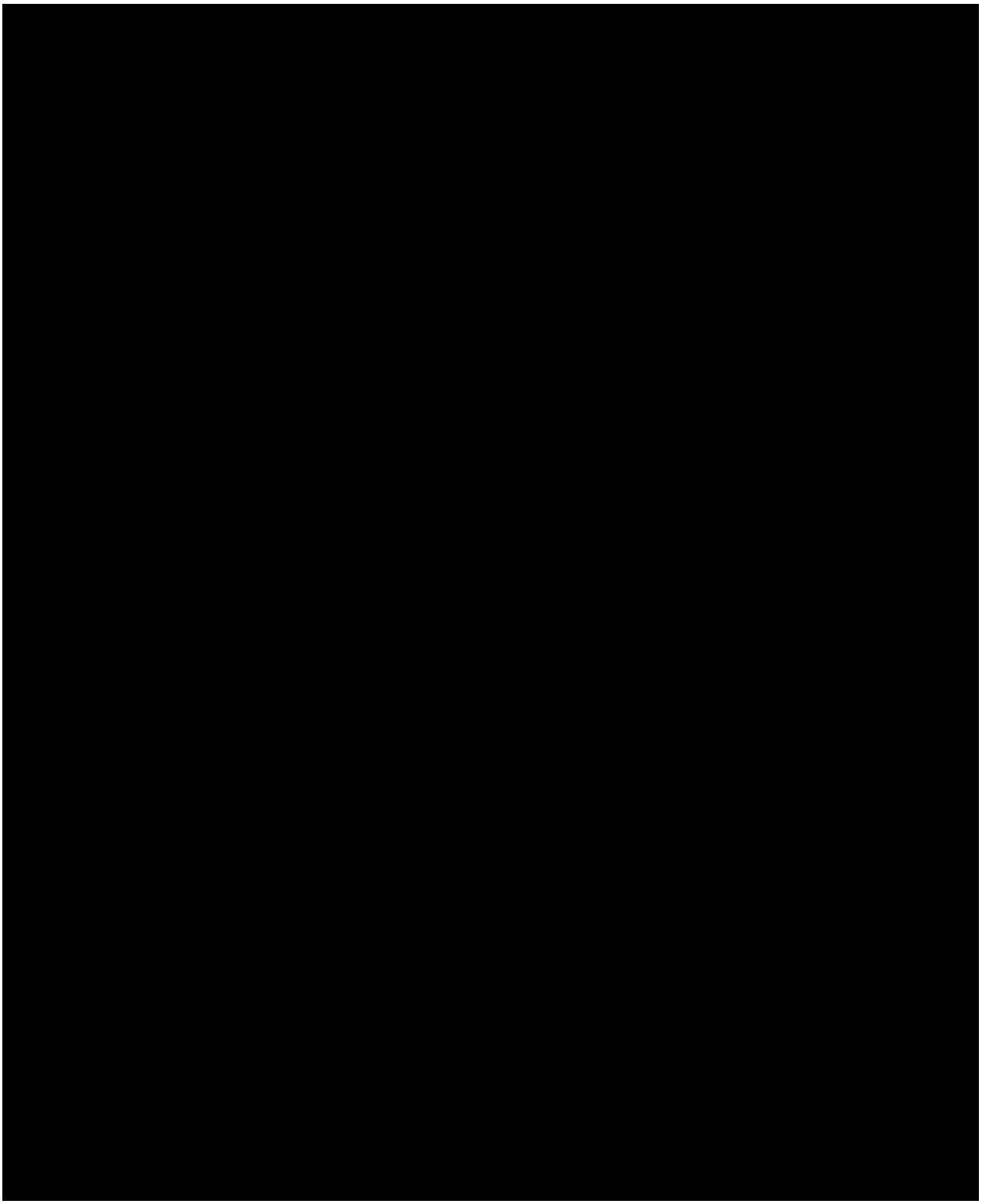

Figure 5.2-14 Message Switch Peripheral Unit Model 2 - J5D006AD-1

5.2.14.2 MSPU (Communities 2 and 3) - J5D006AB-1

The Message Switch Peripheral Units (MSPU) provided for Communities 2 and 3 are located in EQLs 28 and 36, respectively, in the Message Switch Cabinet.

The main purpose of the two MSPUs is to provide switching control for the Module Message Processors

(MMPs) assigned to Switching Modules (SMs). The Community 2 MSPU handles even numbered MMPs (0, 2, 4, and 6) assigned to SMs 1 through 32. The Community 3 MSPU handles odd numbered MMPs (1, 3, 5, and 7) assigned to the same SMs.

The MSPU connects directly to the Input/Output Microprocessor Interface (IOMI) located in the MSCU and also with the Dual Message Interface (DMI) located in the CMCU.

Figure 5.2-15 illustrates the location of the MSPUs in the CM cabinet 1 and the respective circuit packs in the units.

Figure 5.2-15 Message Switch Peripheral Unit - Communities 2 & 3 - J5D006AB-1

5.2.14.3 MSPU3 - J5D020AC-1

The Message Switch Peripheral Unit Model 3 (MSPU3) is fixed located in EQL 53 in all Communication Module Model 2 (CM2) cabinets. The main function of the MSPU3 is to process the control time slots and send them to the Message Switch Control Unit Model 2 (MSCU2) for switching to the Administrative Module (AM) or to other Switching Modules (SMs). Each MSPU3 is identified by a unique community number.

Each community mounts four Module Message Processors (MMPs). Each MMP processes control time slots for eight SMs. The MMPs can be equipped in Service Groups 0 and 1 (dual MMP arrangement).

Table 5.2-2 identifies the community assignments to cabinets for a fully equipped 12-cabinet office.

Figure 5.2-16 illustrates the location of the MSPU3 in CM cabinets 5 and 6 and the respective circuit packs in the unit.

Table 5.2-2 Community/Cabinet Assignments

SIDE 0 DUAL				SIDE 1 DUAL			
CM2 CABINET	MSPU3 COMMUNITY	SERVICE GROUP	MMPs	CM2 CABINET	MSPU3 COMMUNITY	SERVICE GROUP	MMPs
5	2	0	00,02, 04,06	6	3	0	01,03, 05,07
	3	1	01,03, 05,07		2	1	00,02, 04,06
4	4	0	08,10, 12,14	7	5	0	09,11, 13,15
	5	1	09,11, 13,15		4	1	08,10, 12,14
3	6	0	16,18, 20,22	8	7	0	17,19, 21,23
	7	1	17,19, 21,23		6	1	16,18, 20,22
2	11	0	24,26, 28,30	9	10	0	25,27, 29,31
	10	1	25,27, 29,31		11	1	24,26, 28,30
1	13	0	32,34, 36,38	10	12	0	33,35, 37,39
	12	1	33,35, 37,39		13	1	32,34, 36,38
0	15	0	40,42, 44,46	11	14	0	41,43, 45,47
	14	1	41,43, 45,47		15	1	40,42, 44,46

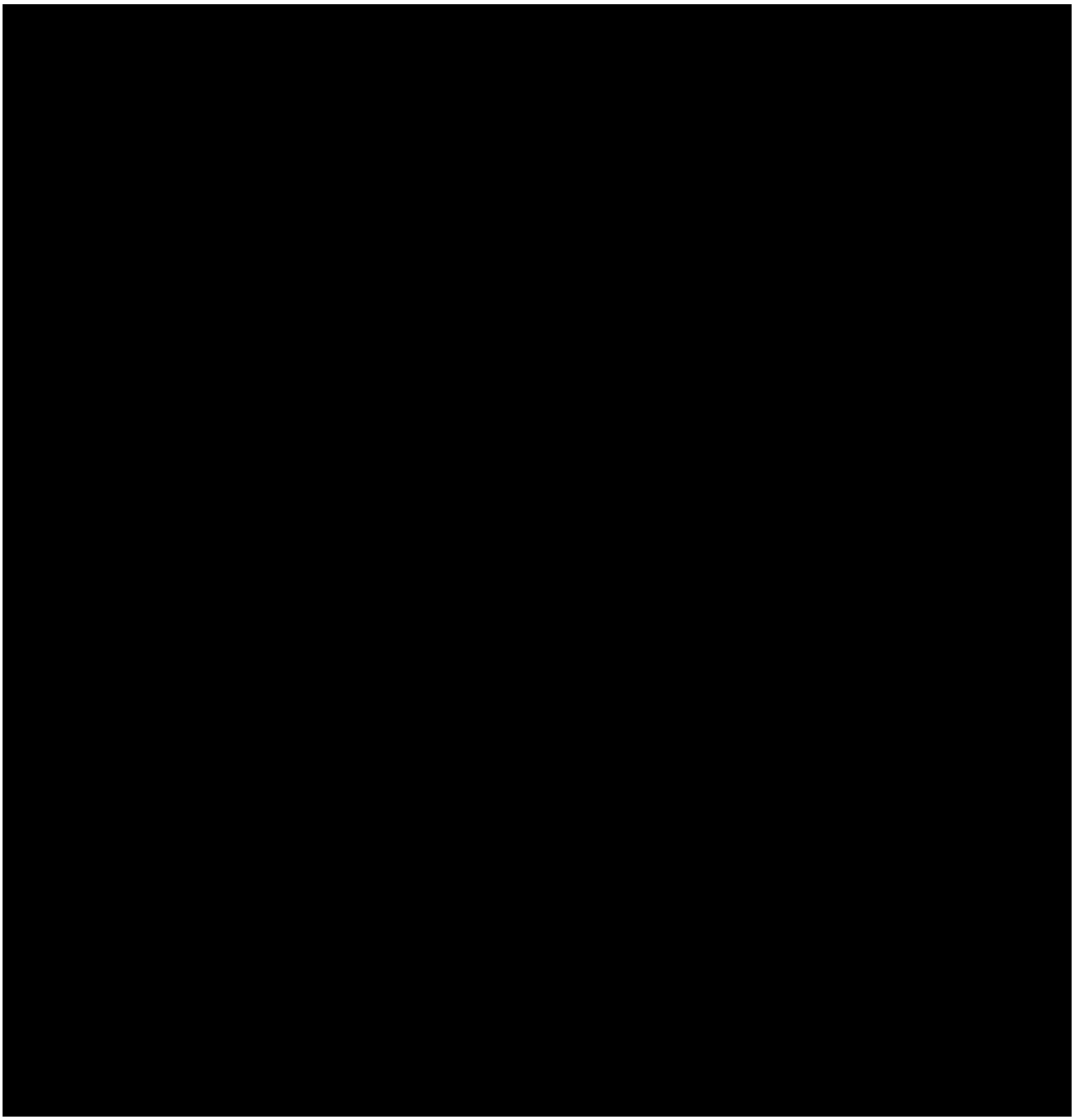

Figure 5.2-16 Message Switch Peripheral Unit - J5D020AC-1

5.2.15 TIME-MULTIPLEXED CONTROL UNIT - J5D001AA-1

The Time-Multiplexed Control Unit (TMCU) is a single-shelf assembly that terminates Network Control and Timing (NCT) links from the Message Interface Clock Unit (MICU) and is equipped with the overall control circuit packs for the Time-Multiplexed Switch (TMS). Positions are provided for seven control and interface packs in addition to space for two power converters.

Figure 5.2-17 illustrates the TMCU and its associated circuit packs.

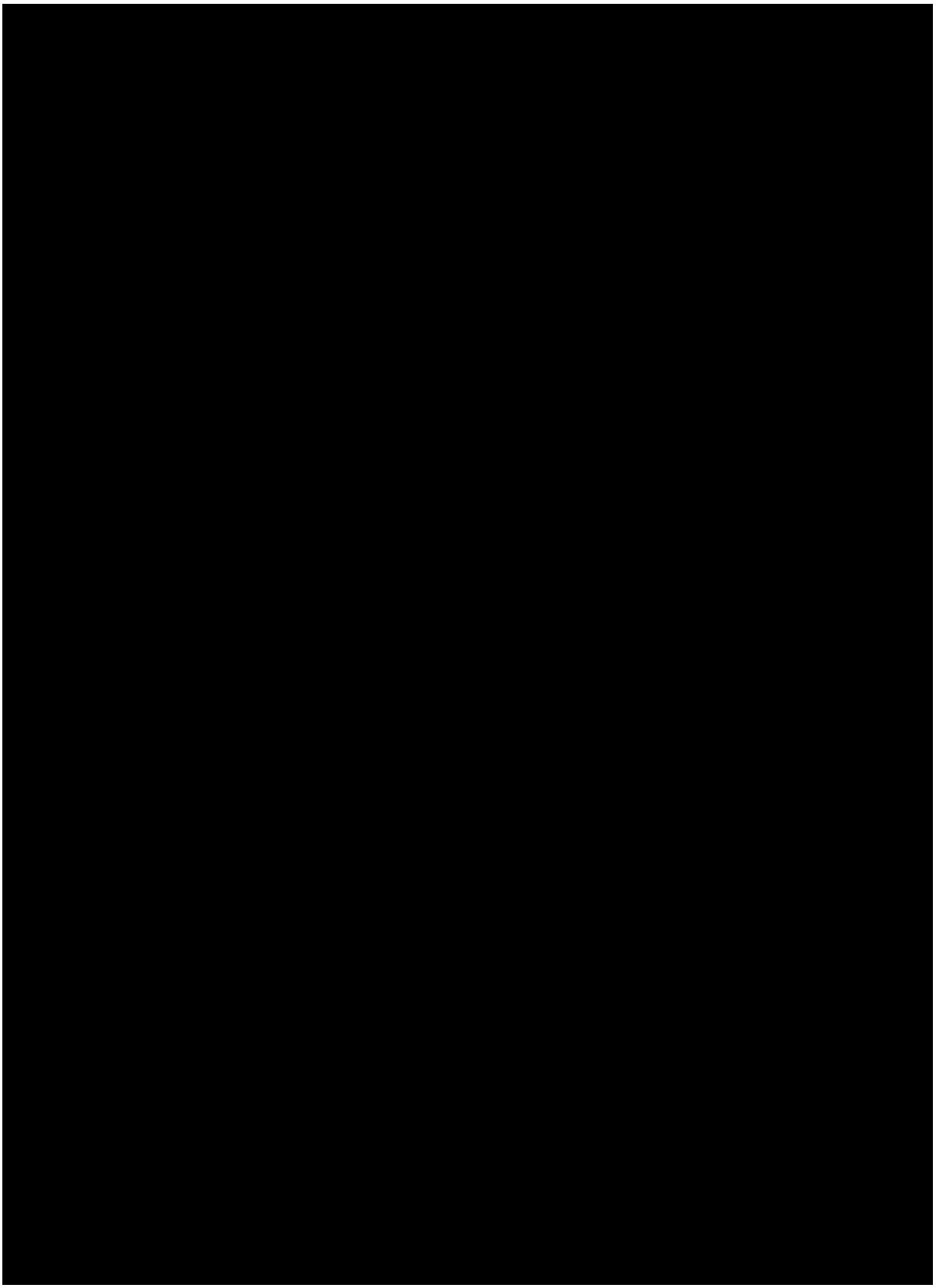

Figure 5.2-17 Time-Multiplexed Control Unit - J5D001AA-1

5.2.16 TIME-MULTIPLEXED SWITCH UNITS

5.2.16.1 Time-Multiplexed Switch Unit - J5D001AB-1

The Time-Multiplexed Switch Unit (TMSU) is a two-shelf assembly that contains the fabric, fanout, and interface circuit packs to provide control and data paths to the appropriate Switching Modules (SMs).

The TMSUs are arranged in an even and odd configuration to serve the associated Network Control and Timing (NCT) links. Positions are provided for 27 circuit packs in the TMSU. Four positions are provided for power converters.

Each link interface is capable of interfacing two NCT links and a fully equipped shelf unit can handle up to 32 links. The Time-Multiplexed Switch (TMS) fabric is expanded in four-link increments that are implemented by inserting the 32 or 34 fabric boards. Two fully equipped shelves provide a 32-by-32 TMS.

Figure 5.2-18 illustrates the TMSU and its associated circuit packs.

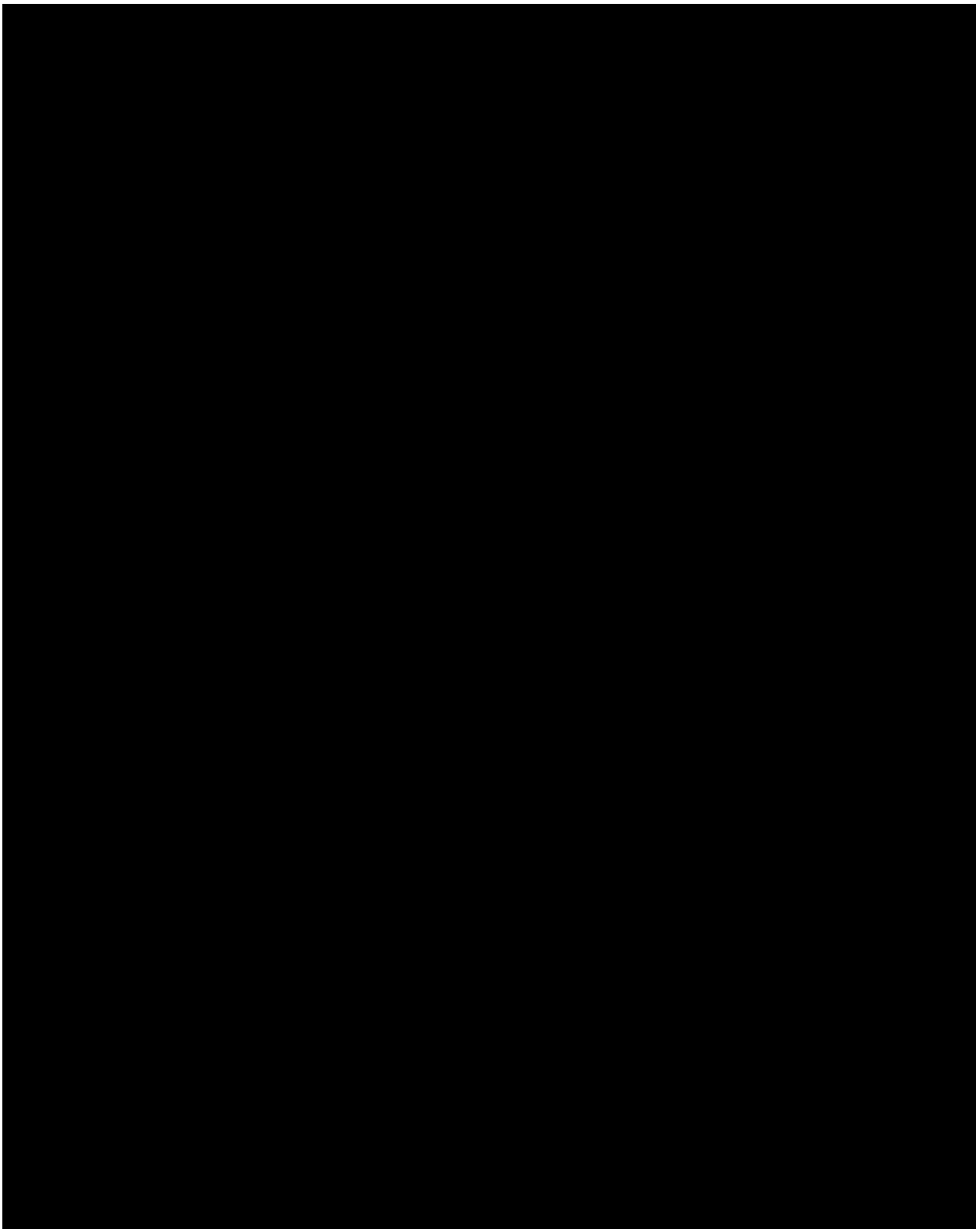

Figure 5.2-18 Time-Multiplexed Switch Unit - J5D001AB-1

5.2.16.2 TMSU Model 2 - J5D020AD-1 and Model 3 - J5D020AG-1

A basic Communication Module (CM) contains at least one Time-Multiplexed Switch Unit Model 2 (TMSU2) or Model 3 (TMSU3) mounted at EQL 36. The TMSU2 and TMSU3 are functionally identical, but the

TMSU3 has fewer physical components. If a second TMSU is required, mount it at EQL 19. Mount a plenum at EQL 19 if a second TMSU is not required. Side 0 and side 1 (cabinets 5 and 6) are equipped identically. Figure 5.2-19 illustrates the TMSU2 unit and the circuit packs in it. Figure 5.2-20 illustrates the TMSU3 unit and the circuit packs in it.

The TMSU primarily consists of the following circuit packs:

- Control and display
- Quad-Link Interface (QLI)
- Quad Link Packet Switch (QLPS)
- Quad Link Interface Model 2 (QLI2)
- Shelf utility board
- Fabric
- Fabric control.

The number of TMSUs required depends upon the number of Switching Modules (SMs) in the office and the TMSU arrangement as to single or dual fabric. Fabric arrangement determination is required in order to correctly assign SM links to the CM. Once the TMSU fabric structure is established (single or dual), all later added TMSUs must be of the same arrangement. A particular Communication Module Model 2 (CM2) frame cannot mix TMSU2 and TMSU3 models; both TMSUs must have the same model number if they are mounted in the same cabinet.

One of the main functions of the TMSU is to terminate (switch) NCT links to and from SMs. Cables carrying input from SMs are connected to optical transceivers located in the line interface area, EQLs 032 through 088. The optical transceiver connectors mount on the TMSU backplane.

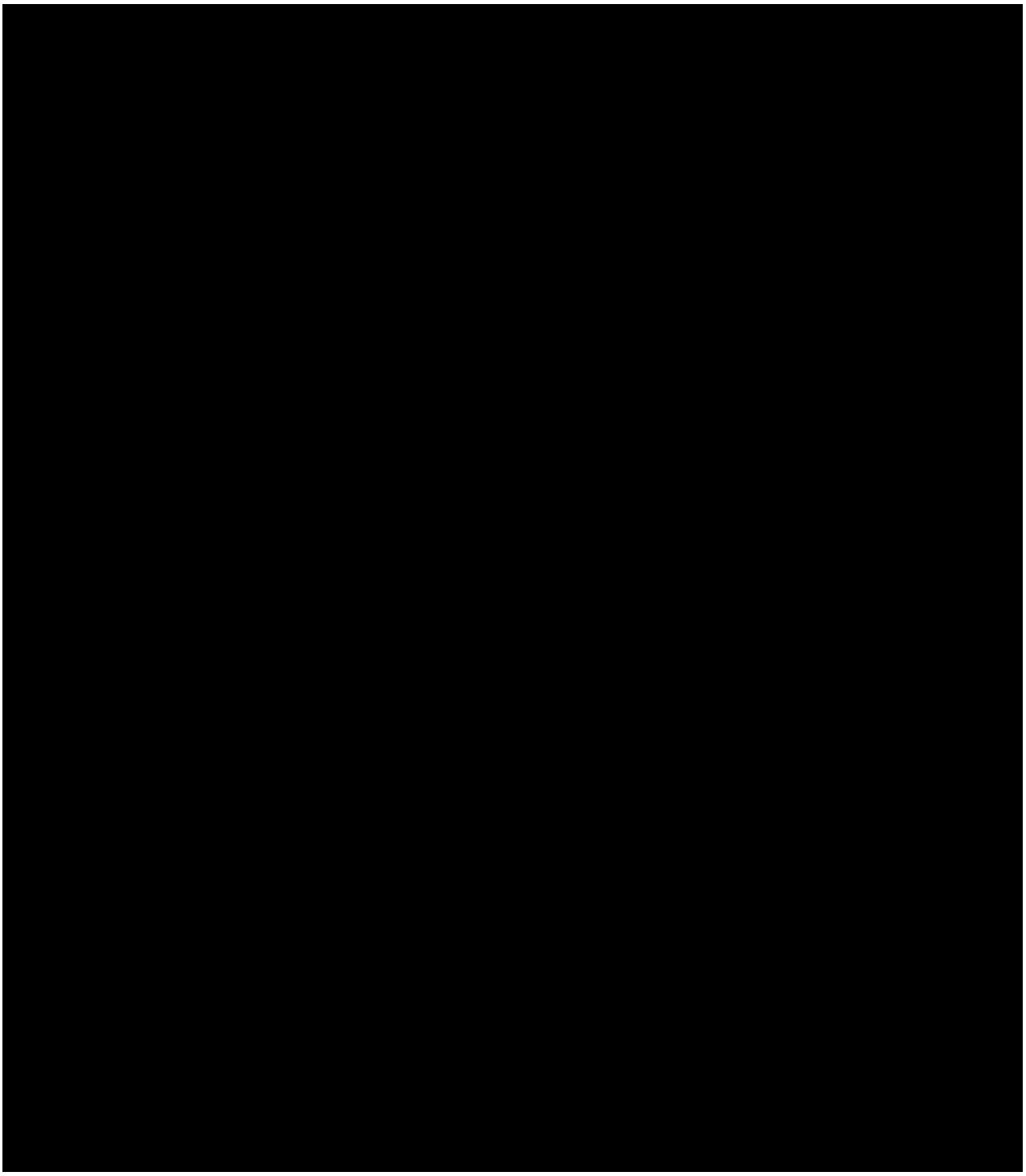

Figure 5.2-19 Time-Multiplexed Switch Unit Model 2 - J5D020AD-1

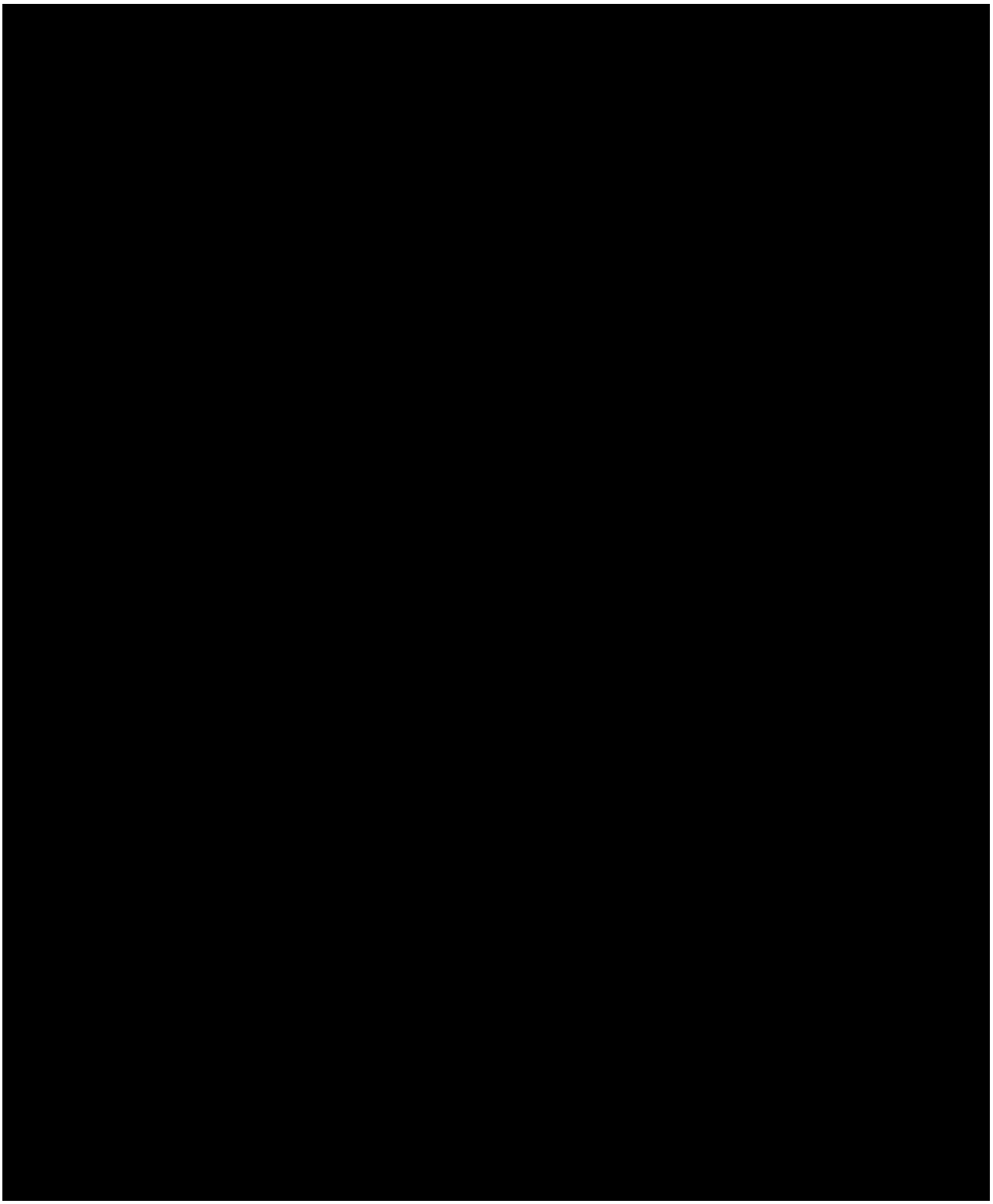

Figure 5.2-20 Time-Multiplexed Switch Unit Model 3 - J5D020AG-1

Figure 5.2-21 illustrates the interface between SMs and CMs by circuit pack functions.

Figure 5.2-21 SM/CM Interface

5.2.16.2.1 Single Fabric Termination Arrangement

If the termination arrangement is Single Switching Fabric, up to 94 SMs can be terminated using six CM cabinets; 5, 4, and 3 on side 0 and 6, 7, and 8 on side 1. Table 5.2-3 lists the cabinet and shelf assignments for the 94 SMs.

Details on how to terminate NCT links from SMs to the TMSU2 for a single fabric arrangement are shown on ED5D500-21, Table AA. A portion of the table, listing up to 30 SMs, appears in Tables 5.2-4 and 5.2-5 . Table 5.2-4 provides information for termination of NCT links on assigned SMs. The table is divided into half, with NCT links OA (even time slots) and OB (odd time slots) connected to CM2, side 1. The direct connections are between the selected SM Module Controller and Time Slot Interchanger Unit (MCTU) Dual Link Interface (TN1077E) and transmitters and receivers at specific SM locations. Note that SM numbers are not entered on the table. These assignments are made locally. Table 5.2-4 shows the three most popular SMC units: TSIU2, MCTU, and MCTU2.

Table 5.2-5 shows how SM NCT links terminate on the TMSU transceivers. Looking at the table columns from the left, the first column shows SM numbering, the second column shows the nine-digit EQL identification for CM2 side 0 and the third column shows the EQL identification for CM2 side 1. The nine-digit EQL number is defined as follows:

- Digit 1 = CM2 cabinet number (can be two digits)
- Digits 2 and 3 = Inches shelf is from floor (36 or 19)
- Digits 4, 5, and 6 = Circuit pack position in unit (EQL) (088 to 032)
- Digit 7 = Column

- Digits 8 and 9 = Row.

The top section of the table shows how the NCT links are connected to the transceivers. A designated cable connects an EQL in the SM to an EQL in the CM2.

The Foundation Link Interface (FLI) circuit pack (TN883) terminates SM1, with both odd and even NCT links connected to one 1A transceiver. A total of 512 time slots are handled. Quad-Link Interface (QLI) circuit packs, TN888, can terminate four NCT links, both odd and even, and handle 1024 time slots through two 1A transceivers. The TN883 FLI circuit packs appear only in CM cabinets 5 and 6. Refer to Figure 5.2-22 for the termination to the 1A transceiver.

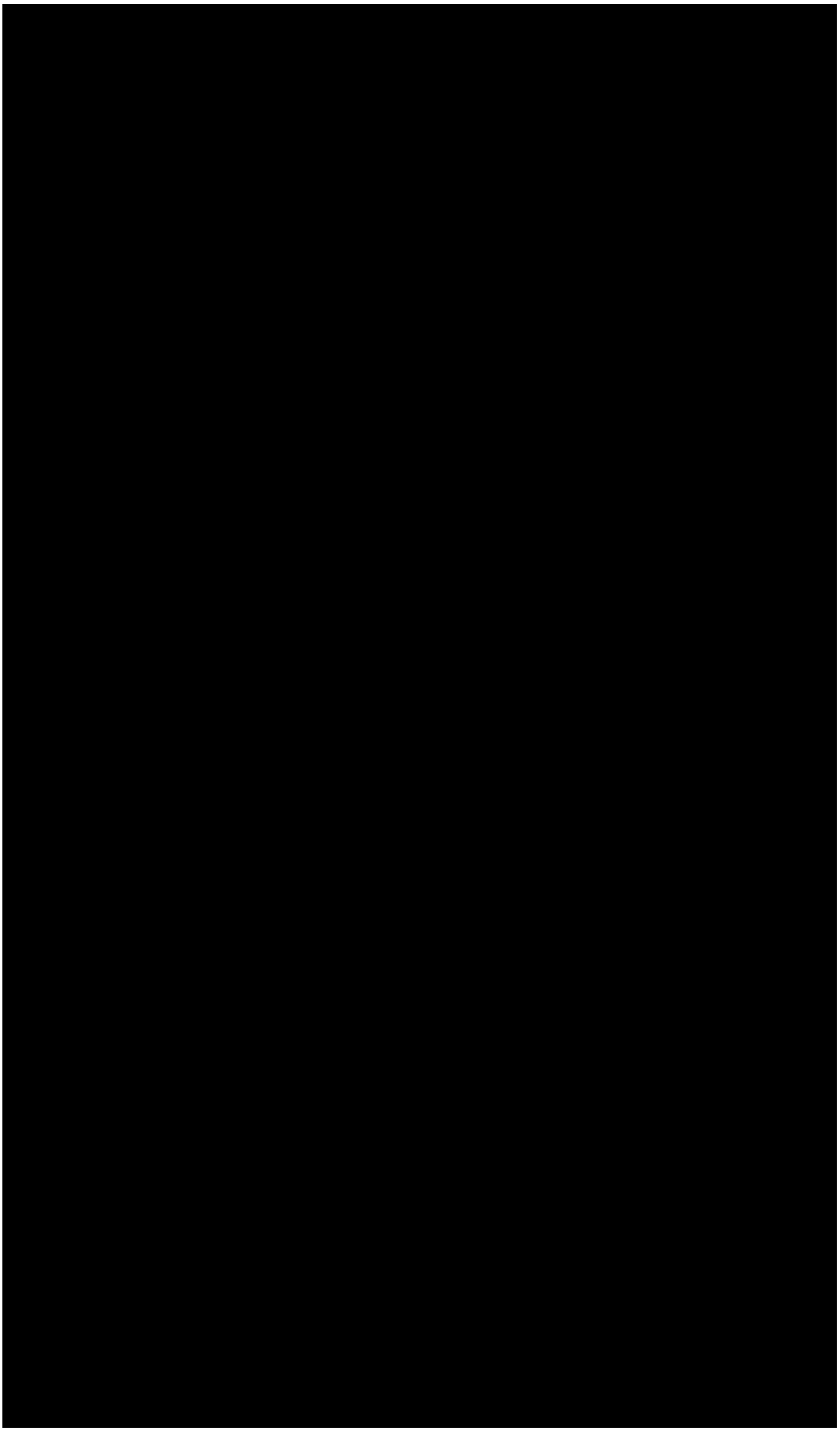

Figure 5.2-22 1A Transceiver

Table 5.2-3 SM Cabinet and Shelf Assignments for the 94 SMs

CM2 CABINET	TMSU2 SHELF	SWITCHING MODULES
5 & 6	36	SM1 to SM15
5 & 6	19	SM16 to SM30
4 & 7	36	SM31 to SM46
4 & 7	19	SM47 to SM62
3 & 8	36	SM63 to SM78
3 & 8	19	SM79 to SM94

Table 5.2-4 NCT Link Terminations on SMS

	EVEN NCT LINK		ODD NCT LINK		EVEN NCT LINK		ODD NCT LINK	
Cable Desig.	**JL9**	**JL11**	**JL13**	**JL15**	**JL10**	**JL12**	**JL14**	**JL16**
NCT Links	**OA**		**OB**		**1A**		**1B**	
	XMTR	**REC**	**XMTR**	**REC**	**XMTR**	**REC**	**XMTR**	**REC**
SM ( ) SMC TSIU2 (TN 877)	145-084-132	145-084-145	145-084-113	145-084-100	145-100-132	145-100-145	145-100-113	145-100-100
SM ( ) SMC 1 MCTU (TN 1077)	136-084-332	136-084-345	136-084-313	136-084-300	136-098-332	136-098-345	136-098-313	136-098-300
SM ( ) SMC 1 MCTU2 (TN 1077E)	119-156-332	119-156-345	119-156-313	119-156-300	128-156-332	128-156-345	128-156-313	128-156-300

Table 5.2-5 SM NCT Link Terminations on TMSU Transceivers

CM2 PORTS								
	CM2 SIDE 0				CM2 SIDE 1			
SM NO.	**REC1 A**	**XMT1 C**	**REC2 B**	**XMT2 D**	**REC1 A**	**XMT1 C**	**REC2 B**	**XMT2 D**
SM1	536-088-145				636-088-145			
SM2	536-080-145				636-080-145			
SM3	536-080-113				636-080-113			
SM4	536-072-145				636-072-145			
SM5	536-072-113				636-072-113			
SM6	536-064-145				636-064-145			
SM7	536-064-113				636-064-113			
SM8	536-056-145				636-056-145			
SM9	536-056-113				636-056-115			
SM10	536-048-145				636-048-145			
SM11	536-048-113				636-048-113			
SM12	536-040-145				636-040-145			
SM13	536-040-113				636-040-113			
SM14	536-032-145				636-032-145			
SM15	536-032-113				636-032-113			
SM16	519-088-145				619-088-145			
SM17	519-080-145				619-080-145			
SM18	519-080-113				619-080-113			
SM19	519-072-145				619-072-145			
SM20	519-072-113				619-072-113			
SM21	519-064-145				619-064-145			
SM22	519-064-113				619-064-113			

SM23	519-056-145	619-056-145
SM24	519-056-113	619-056-115
SM25	519-048-145	619-048-145
SM26	519-048-113	619-048-113
SM27	519-040-145	619-040-145
SM28	519-040-113	619-040-113
SM29	519-032-145	619-032-145
SM30	519-032-113	619-032-113

5.2.16.2.2 Dual Fabric Termination Arrangement

If the termination arrangement is Dual Switching Fabric, up to 190 SMs can be terminated using 12 CM cabinets; 5 to 0 on side 0 and 6 to 12 on side 1. Table 5.2-6 lists the cabinet and shelf assignments for the 190 SMs.

Figure 5.2-3 illustrates the CM2 fully loaded with 12 cabinets.

Table 5.2-6 SM Cabinet and Shelf Assignments for the 190 SMs

CM2 CABINET	TMSU2 SHELF	SWITCHING MODULES
5 & 6	36 & 19	SM 1 to 30
4 & 7	36 & 19	SM 31 to 62
3 & 8	36 & 19	SM 63 to 94
2 & 9	36 & 19	SM 95 to 126
1 & 10	36 & 19	SM 127 to 158
0 & 11	36 & 19	SM 159 to 190

Even NCT links for each SM terminate on shelf 36 and odd links terminate on shelf 19. If QLPS is present, Network 0 is shelf 36; Network 1 is located on shelf 19. The QLPS circuit pack must be in the same slot number. A Foundation Link Interface (FLI) circuit pack (TN883) terminates even NCT links for SM1 and SM2 on two CM2 1A transceivers. The NCT links for the remaining SMs terminate on Quad Link Interface (QLI) circuit packs (TN888), with even links on shelf 36 and odd links on shelf 19. CM2 cabinets 5 and 6 can terminate up to 30 SMs in the dual fabric arrangement. Note that FLI circuit packs appear only in cabinets 5 and 6.

Details on how to terminate NCT links from SMs to the CM2 TMSU2 are shown on ED-5D500-21, Tables AB and AB-1. Portions of these tables appear in Tables 5.2-4 and 5.2-7 . Table 5.2-4 , describing single fabric arrangements, also applies to dual fabric arrangements.

Table 5.2-7 is a two-part table, one part lists odd numbered SM to CM connections and the other part lists even numbered SM to CM connections.

Table 5.2-7 Odd- and Even-Numbered SM to CM Connections

ODD-NUMBERED CM2 PORTS				
	CM2 SIDE 0		CM2 SIDE 1	
SM NO.	REC1 A AND XMT1 C	REC1 A AND XMT1 C	REC1 A AND XMT1 C	REC1 A AND XMT1 C
SM1	536-088-145	519-088-145	636-088-145	619-088-145
SM3	536-080-145	519-080-145	636-080-145	619-080-145
SM5	536-080-113	519-080-113	636-080-113	619-080-113
SM7	536-072-145	519-072-145	636-072-145	619-072-145
SM9	536-072-113	519-072-113	636-072-113	619-072-113
SM11	536-064-145	519-064-145	636-064-145	619-064-145
SM13	536-064-113	519-064-113	636-064-113	619-064-113
SM15	536-056-145	519-056-145	636-056-145	619-056-145
SM17	536-056-113	519-056-113	636-056-113	619-056-113
SM19	536-048-145	519-048-145	636-048-145	619-048-145
SM21	536-048-113	519-048-113	636-048-113	619-048-113
SM23	536-040-145	519-040-145	636-040-145	619-040-145
SM25	536-040-113	519-040-113	636-040-113	619-040-113
SM27	536-032-145	519-032-145	636-032-145	619-032-145
SM29	536-032-113	519-032-113	636-032-113	619-032-113
EVEN-NUMBERED CM2 PORTS				
	CM2 SIDE 0		CM2 SIDE 1	
SM NO.	REC2 B AND XMT2 D	REC2 B AND XMT2 D	REC2 B AND XMT2 D	REC2 B AND XMT2 D
SM2	536-088-145	519-088-145	636-088-145	619-088-145
SM4	536-080-145	519-080-145	636-080-145	619-080-145

SM6	536-080-113	519-080-113	636-080-113	619-080-113
SM8	536-072-145	519-072-145	636-072-145	619-072-145
SM10	536-072-113	519-072-113	636-072-113	619-072-113
SM12	536-064-145	519-064-145	636-064-145	619-064-145
SM14	536-064-113	519-064-113	636-064-113	619-064-113
SM16	536-056-145	519-056-145	636-056-145	619-056-145
SM18	536-056-113	519-056-113	636-056-113	619-056-113
SM20	536-048-145	519-048-145	636-048-145	619-048-145
SM22	536-048-113	519-048-113	636-048-113	619-048-113
SM24	536-040-145	519-040-145	636-040-145	619-040-145
SM26	536-040-113	519-040-113	636-040-113	619-040-113
SM28	536-032-145	519-032-145	636-032-145	619-032-145
SM30	536-032-113	519-032-113	636-032-113	619-032-113

5.2.16.3 Time-Multiplexed Switch Unit Model 4 (TMSU4) (J5D020C01)

A total of six TMSU4s (each consisting of two Time-Multiplexed Switch Expansion (TMSX) packs and up to 24 optical paddleboards for NCT2 links are equipped in the maximum CM3 configuration (three shelves per side), as shown in Figure 5.2-23 . Note that the TMSU4 has 48 paddleboard positions, but when providing connections for NCT2 links, a maximum of 24 paddleboards may be equipped with each paddleboard connecting 2 NCT2 links, one even and one odd. The TMSU4s are located at vertical EQLs as follows:

- TMSU4 shelf 1: 35F (side 0), 35R (side 1)
- TMSU4 shelf 2: 45F (side 0), 45R (side 1)
- TMSU4 shelf 3: 55F (side 0), 55R (side 1).

The TMSU4 provides the termination capacity for 24 NCT2 link pairs (24 even and 24 odd). In the receive direction, these links are multiplexed together at a higher speed and connected to the Time-Multiplexed Switch Foundation (TMSF) packs on the CMU2 shelf. In the transmit direction, 24 links are passed from the TMSF pack and converted into NCT2 link format.

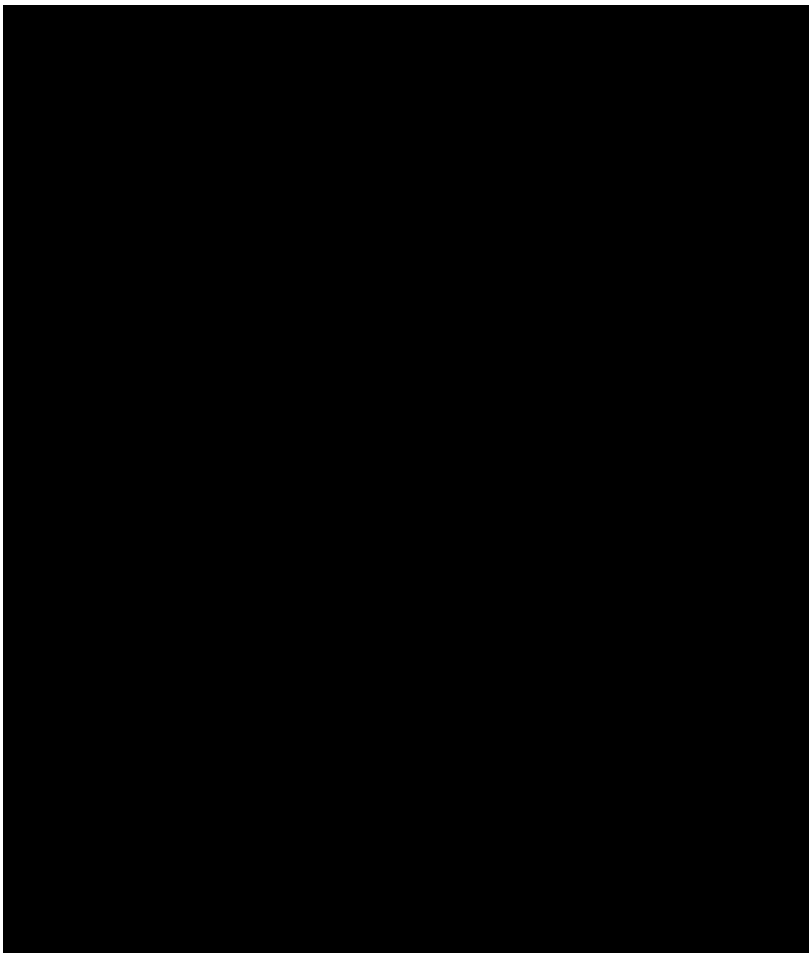

Figure 5.2-23 CM3 Cabinet Layout

5.2.17 DIAGNOSTIC PHASE DESCRIPTIONS

This section contains the diagnostic phase descriptive information (in the form of tables) for the CM hardware (units/circuits) of the *5ESS*® switch. The entries closely follow those used on the MCC display pages and input/output messages.

The entry [PR Name=*xxxxxxxx*] in the DESCRIPTION/WHAT IS TESTED column in a mnemonic reference to the appropriate diagnostic PR (program listing).

The following is a list of the diagnostic phase tables:

- Table 5.2-8 , Diagnostic Phase Descriptions for CMP
- Table 5.2-9 , Diagnostic Phase Descriptions for FPC (CM1)
- Table 5.2-10 , Diagnostic Phase Descriptions for FPC (CM2)
- Table 5.2-11 , Diagnostic Phase Descriptions for LI
- Table 5.2-12 , Diagnostic Phase Descriptions for MI (CM1)
- Table 5.2-13 , Diagnostic Phase Descriptions for MI (CM2)
- Table 5.2-14 , Diagnostic Phase Descriptions for MMP (CM1)
- Table 5.2-15 , Diagnostic Phase Descriptions for MMP (CM2)

- Table 5.2-16 , Diagnostic Phase Descriptions for MSCU (CM1)
- Table 5.2-17 , Diagnostic Phase Descriptions for MSCU (CM2)
- Table 5.2-18 , Diagnostic Phase Descriptions for NC (CM1)
- Table 5.2-19 , Diagnostic Phase Descriptions for NC (CM2)
- Table 5.2-20 , Diagnostic Phase Descriptions for PPC (CM1)
- Table 5.2-21 , Diagnostic Phase Descriptions for PPC (CM2)
- Table 5.2-24 , Diagnostic Phase Descriptions for TMS (CM1)
- Table 5.2-25 , Diagnostic Phase Descriptions for TMS (CM2).

Table 5.2-8 Diagnostic Phase Descriptions for CMP

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests interface between the MSCU (IOMI) and TN1368/TN1800 core board. [PR Name=AM:DNC3BPIP]
2	Tests IP side (including DAM, DRAMs) of TN1368/TN1800 core board. [PR Name=AM:DNC3BPIP and CMP:DNPH3PIP_I]
3	Tests the AP side of the TN1368/TN1800 core board. [PR Name=AM:DNC3BPI and CMP:DNPH3PIP_A]
4	Tests AP-side interface of the TN1368/TN1800 core board to the TN1369 external memory board. [PR Name=AM:DNC3BPIP and CMP:DNPH3PIP_A]
5	Tests memory pump of the TN1368/TN1800 and TN1369. [PR Name=AM:DNC3BIP and CMP:DNPH3PIP_I]
11	*(Demand phase only.)* More exhaustive tests of memory devices on TN1368/TN1800 and TN1369 boards. This phase should be run when there are reports of CMP memory errors but the normal CMP diagnostic phases above run ATP. [PR Name=AM:DNC3BPIP and CMP:DNPH3PIP_A]
12	*(Demand phase only.)* Runs same test sequences as phase 2 except each sequence is run as a separate segment to provide more data on failures. Used primarily in the factory where data may help in component-level fault isolation. [PR Name=AM:DNC3BPIP and CMP:DNPH3PIP_I]
13	*(Demand phase only.)* Runs same test sequences as phase 3 except each sequence is run as a separate segment to provide more data on failures. Used primarily in the factory where data may help in component-level fault isolation. [PR Name=AM:DNC3BPIP and CMP:DNPH3PIP_A]
14	*(Demand phase only.)* Runs same test sequences as phase 4 except each sequence is run as a separate segment to provide more data on failures. Used primarily in the factory where data may help in component-level fault isolation. [PR Name=AM:DNC3BPIP and CMP:DNPH3PIP_A]
15	*(Demand phase only.)* Runs same test sequences as phase 5 except each sequence is run as a separate segment to provide more data on failures. Used primarily in the factory where data may help in component-level fault isolation. [PR Name=AM:DNC3BPIP and CMP:DNPH3PIP_I]

Table 5.2-9 Diagnostic Phase Descriptions for FPC CM1

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the interface between the MSCU (UN25) and the microprocessor board (TN856) of the FPC. [PR Name=AM:DNC3BFPC]
2	Tests the microprocessor board (TN856) of the FPC. [PR Name=FPC:DNCFP22-25 and AM:DNC3BFPC]
3	Tests the application board (UN173) of the FPC. [PR Name=FPC:DNCFP32-35 and AM:DNC3BFPC]

Table 5.2-10 Diagnostic Phase Descriptions for FPC CM2

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the interface between the MSCU (UN25) and the microprocessor board (TN856) of the FPC. [PR Name=AM:DNC3BFPC]
2	Tests the controller board (TN856) of the FPC. [PR Name=AM:DNC3BFPC and FPC:DNCFP22-25]
3	Tests the application board (UN173) of the FPC. [PR Name=AM:DNC3BFPC and FPC:DNCFP32-35]

Table 5.2-11 Diagnostic Phase Descriptions for LI

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the communication interface between the FPC and LI, and the ability to read and write the LI control

	registers. [PR Name=FPC:DNCL01]
2	Tests the A and B links framing, transmit and receive parity, the parity to/from the FPC, and the phase lock loop clock slip. [PR Name=FPC:DNCL02]
3	Tests the A and B link receive message time slot parity, and the A and B link transmit message time slot parity. [PR Name=FPC:DNCL03]

Table 5.2-12 Diagnostic Phase Descriptions for MI (CM1)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests interface from host FPC to MI under test, major buses between MI boards, and access of common registers. [PR Name=FPC:DNCMI1]
2	Tests the time slot switching functions of the TN861 board. [PR Name=FPC:DNCMI2]
3	Tests the CPI time slot matching functions of the TN861 board. [PR Name=FPC:DNCMI3]
4	Tests the clocking functions of the TN860 and TN859 boards. [PR Name=FPC:DNCMI4]
5	Tests TN862 clocking, the TN861 gate array, MI interrupt lead to the FPC, and CDAL link to the opposite FPC. [PR Name=FPC:DNCMI5]
6	Tests the CPI loopback and MIBs from the PCs. [PR Name=FPC:DNCMI6]

Table 5.2-13 Diagnostic Phase Descriptions for MI (CM2)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests interface from host FPC to MI under test and major buses between MI boards, and access of source registers. [PR Name=FPC:DNCDMI01]
2	Tests all clocks. [PR Name=FPC:DNCDMI02]
3	Tests time slot switching control and memory and MIB parity by using associated PPC/MMPs as host circuit. [PR Name=FPC:DNCDMI03]
4	Tests the CPI time slot matching functions of the UN187 board. [PR Name=FPC:DNCDMI04]
5	Tests local transmission of the CPI diagnostic message. [PR Name=FPC:DNCDMI05]
6	Tests external transmission of CPI diagnostic messages using TMS. [PR Name=FPC:DNCDMI06]
7	*(Demand phase only.)* Tests the MIBs by using the PPC/MMPs as host circuits. Both PPC/MMPs are automatically removed and restored during this phase. [PR Name=FPC:DNCDMI07, MMP:DNC2MMP52-57, and PPC:DNCPPC42-43]

Table 5.2-14 Diagnostic Phase Descriptions for MMP (CM1)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests interface between microprocessor board of the MMP and MSCU (UN25). [PR Name=AM:DNC3BMMP]
2	Tests microprocessor board (TN856) of the MMP. [PR Name=MMP:DNCMMP22-25 and AM:DNC3BMMP]
3	Tests application board (UN170) of the MMP. [PR Name=MMP:DNCMMP32-34 and AM:DNC3BMMP]
4	Tests application board (TN858A) of the MMP. [PR Name=MMP:DNCMMP42-44 and AM:DNC3BMMP]
5	Tests application board (TN858B) of the MMP. [PR Name=MMP:DNCMMP52-56 and AM:DNC3BMMP]
6	*(Demand phase only.)* Tests MMP's interfaces to both sides of ONTC (if in-service). Use only when fault recovery reports MMP troubles but diagnostics is ATP. [PR Name=MMP:DNCMMP62-63 and AM:DNC3BMMP]

Table 5.2-15 Diagnostic Phase Descriptions for MMP (CM2)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the interface between the MSCU (UN25) and the microprocessor board of the MMP. [PR Name=AM:DNC3BMMP]
2	Tests the microprocessor board (TN856) of the MMP. [PR Name=AM:DNC3BMMP and MMP:DNC2MMP22-25]
3 **a**	Tests application board (TN870) of the MMP. [PR Name=AM:DNC3BMMP and MMP:DNC2MMP32-36]
4 **a**	Tests application board (TN870) of the MMP and MIB from that MMP by looping data at the TMS. [PR Name=AM:DNC3BMMP and MMP:DNC2MMP42-47]

Notes:

a. In a dual MMP configuration, the opposite MMP from that being diagnosed is automatically removed and restored during this phase. This happens because data is delivered over the MIB, and that MMP must be removed.

Table 5.2-16 Diagnostic Phase Descriptions for MSCU (CM1)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the interface between the DDSBS and DSCH - TN69 and UN9. [PR Name=AM:DNCMSCU]
2	Tests interface between BIC and DDSBS - TN70 and TN69. [PR Name=AM:DNCMSCU]
3	Tests BIC and BIC/PIC interface - TN70 and TN61. [PR Name=AM:DNCMSCU]
4	Tests the PIC - TN61, TN84A and B. [PR Name=AM:DNCMSCU]
5	Tests the IOMIs - UN25, TN61, TN84A and B. [PR Name=AM:DNCMSCU]

6	Tests the interface between the IOMIs and the PC communities - UN25 and TN856. [PR Name=AM:DNCMSCU]

Table 5.2-17 Diagnostic Phase Descriptions for MSCU (CM2)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the PSM boards - SN516, 495FB, and UN33. [PR Name=AM:DNCMSCU]
2	Tests the DDSBS TN69. [PR Name=AM:DNCMSCU] With MSCU3, the TN69 board is replaced with the KBN10 board.
3	Tests the BIC-TN70. [PR Name=AM:DNCMSCU] With MSCU3, the TN70 board is replaced with the KBN10 board.
4	Tests the BIC and BIC/PIC interfaces - TN70 and UN178. [PR Name=AM:DNCMSCU] With MSCU3, the TN70 and UN178 boards are replaced with the KBN10 board.
5	Tests the PIC-UN178 and UN199. [PR Name=AM:DNCMSCU] With MSCU3, the UN178 and UN199 boards are replaced with the KBN10 board.
6	Tests the interface between the IOMIs and the PIC and the power circuitry of the IOMIs-UN25 and UN178. [PR Name=AM:DNCMSCU] With MSCU3, the UN25 and UN178 boards are replaced with the KBN10 board.
7	Tests the interface between the IOMIs and the PC communities - UN25 and TN856. [PR Name=AM:DNCMSCU] With MSCU 3, the UN25 board is replaced with the KBN10 board.

Table 5.2-18 Diagnostic Phase Descriptions for NC (CM1)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the communication interface between the host FPC and NC, and the CLRT subunit on the controller board. [PR Name=FPC:DNCNC01]
2	Tests the CCB subunit on the controller board. [PR Name=FPC:DNCNC02]
3	Tests the microprocessor portion of the controller board. [PR Name=FPC:DNCNC03]
4	Tests the synchronizer board of the NC - (TN245 or TN249). [PR Name=FPC:DNCNC04]
5	Tests the DPLL board and the operation of the NC in its entirety. [PR Name=FPC:DNCNC05]

Table 5.2-19 Diagnostic Phase Descriptions for NC (CM2)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the communication interface between the host FPC and NC, and the CLRT subunit on the controller board. [PR Name=FPC:DNC2NC01]
2	Tests the CCB subunit on the controller board. [PR Name=FPC:DNC2NC02]
3	Tests the microprocessor portion of the controller board. [PR Name=FPC:DNC2NC03]
4	Tests the synchronizer boards (0 and 1) of the NC. [PR Name=FPC:DNC2NC04]
5	Tests the DPLL board and the operation of the NC in its entirety. [PR Name=FPC:DNC2NC05]
6	*(Demand phase.)* Determine what hardware units are causing phase 5 to CATP. [PR Name=FPC:DNC2NC06]

Table 5.2-20 Diagnostic Phase Descriptions for PPC (CM1)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the interface between the MSCU (UN25) and the microprocessor board of the PPC. [PR Name=AM:DNC3BPPC]
2	Tests the microprocessor board (TN856) of the PPC. [PR Name=PPC:DNCPPC22-25 and AM:DNC3BPPC]
3	Tests the application board (TN886) of the PPC. [PR Name=PPC:DNCPPC32-38 and AM:DNC3BPPC]
4	Tests the MIBs by looping data out of PPC via MIB through MI 0, LI 0, TMS 0 and back. [PR Name=PPC:DNCPPC42-43 and AM:DNC3BPPC]

Table 5.2-21 Diagnostic Phase Descriptions for PPC (CM2)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the interface between the MSCU (UN25) and the microprocessor board of the PPC. [PR Name=AM:DNC3BPPC]
2	Tests the microprocessor board (TN856) of the PPC. [PR Name=PPC:DNCPPC22-25 and AM:DNC3BPPC]
3	Tests the application board (TN886) of the PPC. [PR Name=PPC:DNCPPC32-38 and AM:DNC3BPPC]
4	Tests the MIBs by looping data out of PPC via MIB through MI 0 and TMS 0 and back. In a dual PPC configuration, the opposite side PPC from that being diagnosed is automatically removed and restored. This happens because data is delivered over the MIB and that PPC must be removed. [PR Name=PPC:DNCPPC42-43 and AM:DNC3BPPC]

Table 5.2-22 Diagnostic Phase Descriptions for QGP

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests power, interface between MSCU and QGP processor board; RAM that both MSCU and QGP IP can access (DAM)
2	Tests QGP IP processor.
3	Tests QGP AP processor.
4	Tests interface between QGP processor board and QGP link board; QGP link and QGL cable.
5	Tests verifies that QGP can be pumped.

Table 5.2-23 Diagnostic Phase Descriptions for QLPS

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests interface between TMS controller and QLPS board; BIST; registers; error propagation.
2	Tests error detection (with and without sending packets through the TMS fabric).
3	Tests RX detection of Level 2 errors; miscellaneous; QGL connectivity; Packet RAM (PRAM); Routing RAM (RR); stress testing (lots of packets); tests to check TMS fabric between QLPS and all other QLI/QLI2 boards in TMS.

Table 5.2-24 Diagnostic Phase Descriptions for TMS (CM1)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the power and access to the TMS interface and verifies communication to TMS through the TMS interface (TN269). [PR Name=FPC:DNCTM01]
2	Tests the TMS controller boards (TN269, TN268, and TN265). [PR Name=FPC:DNCTM02]
3	Tests the TMS controller's RAM, PROM, and microprocessor circuitry (TN268). [PR Name=FPC:DNCTM03]
4	Tests the TMS maintenance board (TN265). [PR Name=FPC:DNCTM04]
5	Tests the TMS interface to the host FPC and the interface to the microprocessor (TN269). [PR Name=FPC:DNCTM05]
6	Tests the TMS interface (TN269), the TMS clock board (TN270), and the TMS maintenance flip-flop. [PR Name=FPC:DNCTM06]
7	Tests the bidirectional serial data link and the error source lead between the TMS interface (TN269) and the test board (TN267). [PR Name=FPC:DNCTM07]
8	Tests the test board (TN267) ESR and the test generating circuitry. [PR Name=FPC:DNCTM08]
9	Tests the bidirectional serial data link and the error source lead between the TMS interface (TN269) and the message link interface (TN252). [PR Name=FPC:DNCTM09]
10	Tests the message link interface's ability to detect control parity and bad board IDs, as flagged on the message link interface ESR. [PR Name=FPC:DNCTM10]
11	Tests the bidirectional serial data link and the error source lead between the TMS interface (TN269) and the shelf interface (TN244). [PR Name=FPC:DNCTM11]
12	Tests the TMS shelf interface (TN244). [PR Name=FPC:DNCTM12]
13	Tests the bidirectional serial data link between the shelf interface (TN244) and the fabric (TN242) and the error source lead from the fabric to the shelf interface. [PR Name=FPC:DNCTM13]
14	Tests the bidirectional serial data link between the shelf interface (TN244) and the link interface (TN243) and the error source lead from the link interface to the shelf interface. [PR Name=FPC:DNCTM14]
15	Tests the ESRs, error source lead, and memory of the fabric (TN242). [PR Name=FPC:DNCTM15]
16	Tests the link interface's (TN243) ability to detect control parity and bad board IDs. [PR Name=FPC:DNCTM16]
17	Tests the message interface (TN252) and link interface boards (TN254) by sending various data patterns via the test board (TN267). [PR Name=FPC:DNCTM17]
18	Tests are the same as phase 17. [PR Name=FPC:DNCTM18]
19	Tests are the same as phase 17. [PR Name=FPC:DNCTM19]
20	Tests are the same as phase 17. [PR Name=FPC:DNCTM20]
21	Tests the fabric data paths for switch half A (TN252 and TN243). [PR Name=FPC:DNCTM21]
22	Tests the fabric data paths for switch half B (TN252 and TN243). [PR Name=FPC:DNCTM22]
23	Tests the message link interface's (TN252) fabric (TN242) and fan-out (UN74). [PR Name=FPC:DNCTM23]
24	Tests optical link receiver on message link interface (TN252). [PR Name=FPC:DNCTM24]
25	(*Manual diagnosis only*.) Tests the NCT links to the local TRCU (TN1344) circuits that interface links to ORMs. [PR Name=FPC:DNCTMS25]
27	*(Demand phase for factory or growth testing only.)* Tests the NCT link receivers and transmitters. Requires fiber loop-around straps installed either at the TMS end or the SM end of the NCT link. [PR Name=FPC:DNCCLN3]

Table 5.2-25 Diagnostic Phase Descriptions for TMS (CM2)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the PSM boards and the interface between the FPC and the TMS2. [PR Name=FPC:DNC2TMS01]
2	Tests the operation of the TMS2 controller (TN884, UN183, and TN881) and test the controllers CIC unit towards switching units. [PR Name=TMS:DNC2TMS02, and FPC:DNC2FTMS02]

3	Tests communications between the controller and all UN182, KBN2, TN883, and TN888 boards and their registers. [PR Name=TMS:DNC2TMS03 and FPC:DNC2FTMS03] For the CM2C, the UN182, KBN2, TN883 and TN888 boards are changed to the TN1812 and TN1830 boards.
4	Tests error detecting, propagational masking in KBN1/KBN5, KBN2, TN883, and TN884 boards. [PR Name=TMS:DNC2TMS04 and FPC:DNC2FTMS04] For the CM2C, the KBN1/KBN5, KBN2, TN883 and TN884 boards are changed to the TN1813 and TN1830 boards.
5	Tests data paths in switch units using test function. [PR Name=TMS:DNC2TMS05 and FPC:DNC2FTMS05]
6	Tests AUTISS function, KBN2 sequencing, and all fabric paths. [PR Name=TMS:DNC2TMS06, and FPC:DNC2FTMS06]
11	*(Demand phase for factory or growth testing only.)* Tests the NCT link receivers and transmitters. Requires fiber loop-around straps installed at the TMS end or SM end of the NCT link. [PR Name=TMS:DNC2TMS11 and FPC:DNC2FTMS11]
12	Tests the TMS fabric load/stress test. [PR Name=TMS:DNC2TMS12, and FPC:DNC2FTMS12]
13	*(Demand phase for factory or growth testing only.)* Tests NCT link receivers/transmitters. All links must have loop-around straps installed at the TMS or SM end of the NCT links. All links are tested concurrently. This phase is a more exhaustive test then phase 11. [PR Name=TMS:DNC2TMS13 and FPC:DNC2FTMS13]
14	*(Demand phase to be run when an earlier phase fails with Note No. 36 in its Suspected Faulty Equipment List.)* Does sectionalized testing of the E-bus circuits to produce a more accurate Suspected Faulty Equipment List. [PR Name=TMS:DNC2TMS14 and FPC:DNC2FTMS14]
15	A manual diagnostic phase that does NCT link loop-around tests from the TMS link board (TN888) to the local TRCU (TN1344) circuits interfacing links to ORMs. [PR Name=TMS:DNC2TMS15 and FPC:DNC2FTMS15] For the CM2C, the TN888 board is changed to the TN1830 board.

5.3 SWITCHING MODULES

5.3.1 INTRODUCTION

This section contains maintenance support information about the various Switching Module (SM) configurations. While there is no ``typical'' SM (because of differences among local office requirements), basic modules are presented to provide reasonable coverage.

Figures 5.3-1 and 5.3-2 consecutively illustrate an SM and a loaded SM.

Units within the SM are identified by model numbers (J-drawings) usually stamped on the plastic strip mounted on the cabinet frame above the unit. If the number is not present, get it from office records and apply it to the strip for future reference.

For diagnostic execution input message and POKE command source information, refer to the following IPs:

- 235-105-110, *System Maintenance Requirements and Tools*
- 235-105-210, *Routine Operations and Maintenance Procedures*
- 235-105-220, *Corrective Maintenance Procedures*
- 235-600-700, *Input Messages*
- 235-600-750, *Output Messages*.

The change in standard media for the Program Listings from microfiche to on-line makes it necessary to clarify our terminology. The use of the PR FUNCTION NAME reference used in the microfiche listings does not apply to the on-line listings. When using the on-line listings, the FUNCTION NAME reference is used in conjunction with the search for information on specific functions.

The program listings available via networked service are referred to as the 235-410-220, *Web and Media Management (WMM) Access to On-Line Program Listings*. This IP is actually a dial-up service that allows the user to choose from a menu of selections which includes queries that allow a user to view the source code in the *5ESS*® switch. This access is proprietary and the appropriate nondisclosure agreements must be signed before it can be provided.

NOTE: Program listings were provided via microfiche and networked service. To print out pages, a viewer or a printer is required.

The on-line listings which record the software are similar to the microfiche listings but are ***not*** identical in format or content. The layout of the directory structure for the listings is similar to that used by the software developers. Breakpoints, disassemblies, and header files are left as individual files facilitating access via on-line editors. Authorized customers access the on-line listings via WMM and a login/password process. The on-line listings contain program listings for multiple software releases. The number of software releases available is consistent with the *5ESS*® switch Software Support Product Policy.

NOTE: At the time of printing, there was no conversion for the AM diagnostic products. The following rules for using the on-line listings are for the SM and Communication Module (CM) only.

The general rule to convert the PR name to the MODULE PRODUCT NAME is to remove the processor name and colon then make all characters lowercase except the first two. The processor being the first field (AM or CM or SM). This is true for SM products.

Example: SM:DNFABEX converts to DNfabex

CM diagnostic names are different, having DNC as the first three characters and, in this case, change all characters to lowercase except the first three. However, some CM products are 3B-related, in which case the first five characters are DNC3B, all in uppercase.

Example: CM:DNC2NC03 converts to DNC2nc03
AM:DNC3BFPC converts to DNC3Bfpc

Customers with login access to the on-line listings can refer to 235-600-510, *Software Analysis Guide*, for the login procedure and basic usage information. Customers can also call the Lucent Electronic Media Networked Service Group at 800-225-4672 for assistance.

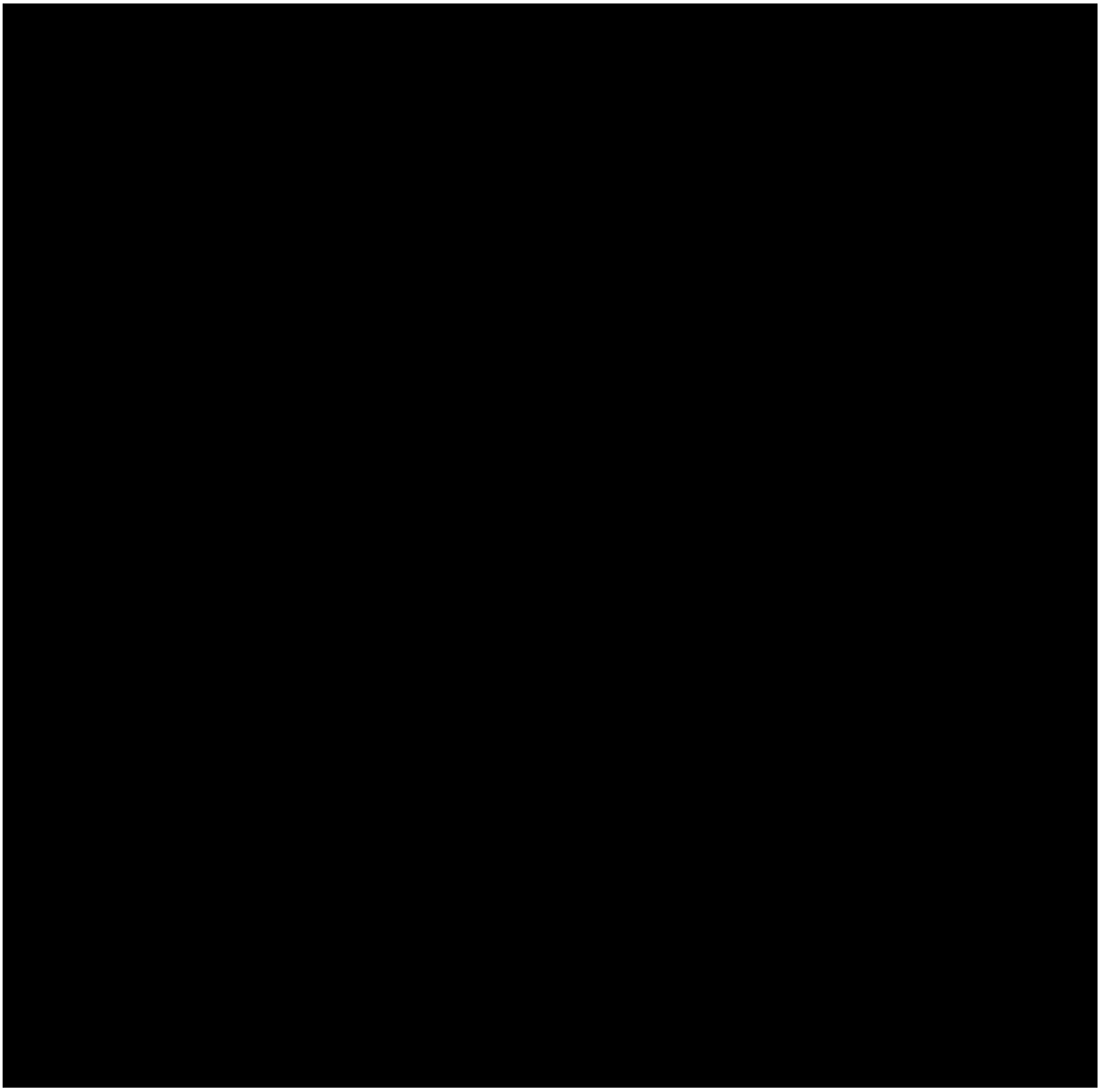

Figure 5.3-1 Switching Module

Figure 5.3-2 Loaded Switching Modules

5.3.2 SWITCHING MODULE-2000

The major component of the *5ESS*® switch is the Switching Module-2000 (SM-2000). Architecturally identical to today's SM, the SM-2000 greatly expands the bandwidth available in the switch while providing additional call processing power and memory capacity needed for its effective use and the ability to terminate more peripherals than a SM.

The SM-2000 is required to permit the installation of SM peripherals in the aisles adjacent to the Switching Module Controller (SMC) cabinet. Because this increased capacity needs more power than a standard 48-kbps communications link can handle, the Quad-Link Packet Switch (QLPS) message network was designed to provide for the higher message capacity required by the SM-2000 and its peripherals. The following are the SM-2000 major components:

- A growable Time Slot Interchange Unit - Model 4 (TSIU4), can be grown to 30K time slots compared with 512 network time slots of the existing SM. This enables enhanced support of the large-scale applications of wideband data switching, as well as continued support of narrowband services. Growth is in response to total bandwidth demand in increments of 3092 peripheral terminations [Digital Signal level 0s (DS0s)]. Also, the fabric is configurable, providing additional network capacity toward the periphery of the switch or toward the internal network, as required. This flexibility permits a tailoring of bandwidth capacity. The internal network side of the Time Slot Interchanger (TSI) is served by expanded Network Control and Timing Model 2 (NCT2) links. These NCT2 links grow with the TSI in increments of 1024 network terminations (DS0s) up to a maximum of 2048 network time slots per TSI slice (TSIS).

- The more sophisticated switching fabric of the SM-2000 is supported by a higher capacity Switching

Module Processor (SMP). Based on the *Motorola*® MC68040 microprocessor, the CORE40 has a significant increase in call processing capacity over the current SMP20. This means that the SM-2000 can support up to 27,520 (43 x 640) analog lines at 10:1 concentration or 10,752 digital trunk applications.

- The Switching Module Processor Unit - Model 4 (CORE40) complex also includes the Message Handler (MH), a separate processor responsible for all interprocessor messages for the SM-2000. Coupled with an expanded message channel on the NCT2 links of 800 kilobits per second (kbps), the MH comprises the SM-2000 portion of an enhanced message switching architecture.
- A larger NCT2 which can be added incrementally to an individual SM-2000 and is fully compatible with the existing Communication Module Model 2 (CM2) and NCT links on existing SMs. An SM-2000 can coexist on a switch with local and remote SMs.
- The Digital Service Unit - Model 3 (DSU3) is used to provide the Local Digital Service Unit Function (LDSUF). The Global Digital Services Functions (GDSFs) are also provided by the DSU3.

Peripheral units supported in SM-2000 are as follows:

- Digital Service Circuits (DSC3) - Local Digital Service Unit Function (LDSUF)
- Digital Line/Trunk Unit - Model 2 (DLTU2)
- Line Unit 3 (LU3)
- Digital Network Unit-SONET (DNU-S)
- Peripheral Control and Timing (PCT) Data Exchanger Unit (PDXU)
- Multiplex Access Interface Unit (XAIU)
- Peripheral Control and Timing (PCT) Line and Trunk (virtual) Unit (PLTU)
- Modular Metallic Service Unit (MMSU) (EXM-2000 only)
- Directly Connected Test Units (DCTUs) (EXM-2000 only).

The SM-2000 can be equipped with 32-megabyte (MB) memory boards or 64-MB boards (TN1806). The 64-MB boards can be used with the 32-MB boards on the same SM-2000, thus providing ease of maintenance and provisioning flexibility.

Figure 5.3-3 shows the basic SM-2000 frame and unit layout. Figure 5.3-4 illustrates the transmission interfaces for remote operation of the SM-2000, Figure 5.3-5 shows the TSI link to DX backplane connections, Figure 5.3-6 shows a backplane view of the TSIU4, and Figure 5.3-7 shows the layout of the DSU3.

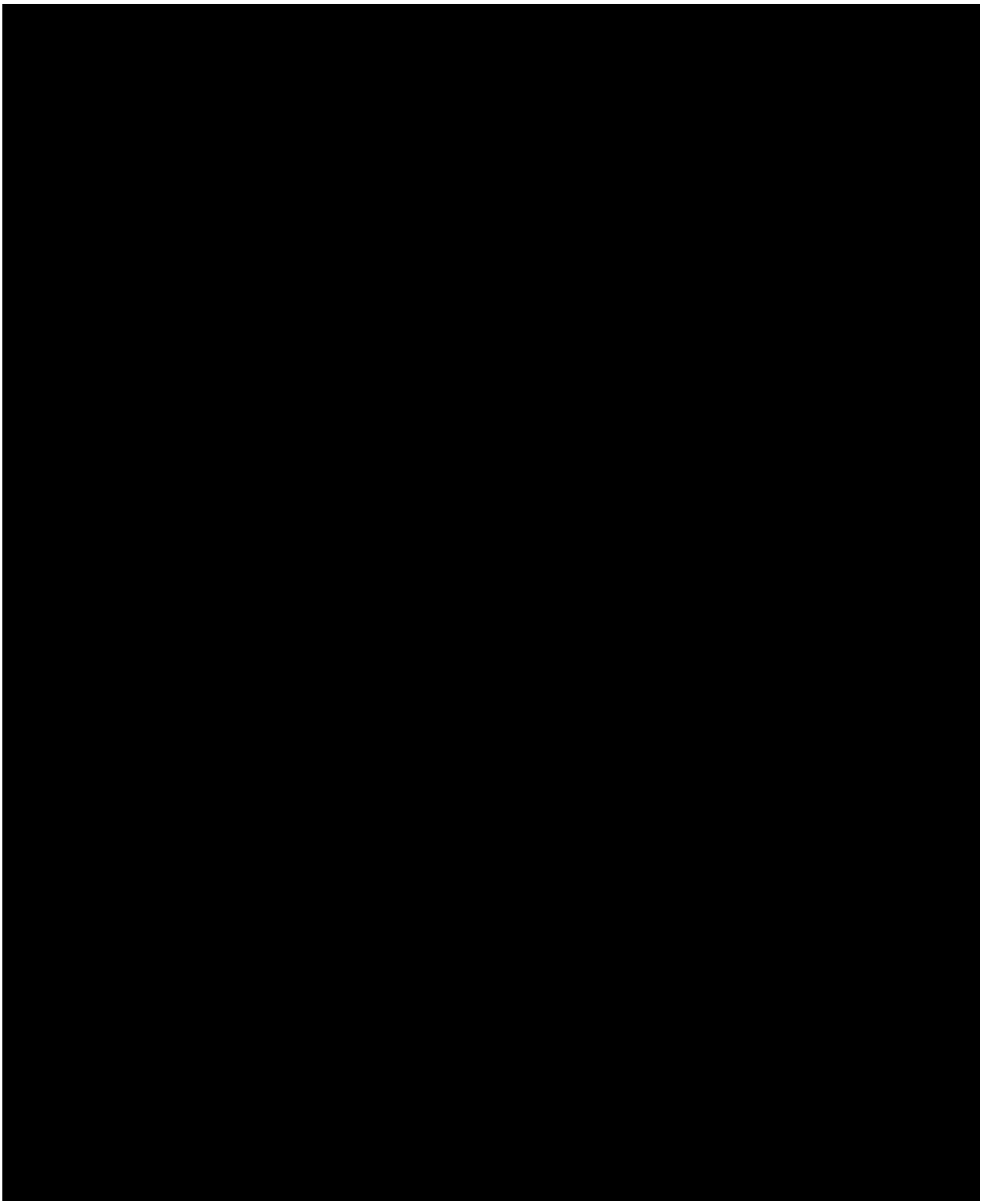

Figure 5.3-3 Basic SM-2000 Frame and Unit Layout Basic SM-2000 Frame and Unit Layout

Figure 5.3-4 Transmission Interface for Remoting the SM-2000 Transmission Interface for Remoting the SM-2000

Figure 5.3-5 TSI Link to DX Backplane Connections TSI Link to DX Backplane Connections

Figure 5.3-6 TSIU4 Backplane TSIU4 Backplane

Figure 5.3-7 DSU3 Layout DSU3 Layout

5.3.2.1 TR303 on DNU-S

Previous generation Digital Loop Carrier (DLC) systems, designed to the TR-008 interface have supported a DS1 (Digital Signal Level 1) level interface to the Central Office Terminal. The Digital Carrier Line Unit (DCLU) and Integrated Digital Carrier Unit (IDCU) were developed to terminate DS1 based DLC systems directly on the *5ESS*® switch.

Next Generation Digital Loop Carrier (NGDLC) systems that are being deployed today are being designed to the TR-303 interface. While they may still support DS1 access, Synchronous Optical Network (SONET) Optical Carrier 3 (OC-3) access is more common. In order to terminate an NGDLC system on an IDCU, the customer must either run copper to support a DS1 interface or provide a SONET multiplexer in the Central Office (CO) to extract DS1s from the OC-3.

The following two configurations are under consideration:

1) TR-303 through EC-1 intraoffice interfaces
2) TR-303 OC-3 interoffice interfaces over SONET rings.

In the two configurations, both asynchronous and byte synchronous mapped Virtual Terminals (VTs) are supported using the hybrid Time Slot Management Channel / Embedded Operations Channel (TMC/EOC) for call processing and Operations, Administration, Maintenance, and Provisioning (OAM&P) control. Note that the Common Signaling Channel (CSC) implementation and DS1 protection switching are NOT requirements for this feature.

This feature provides a platform for future evolution of TR-303. In particular, TR-303 Feature Set C provides more integration of SONET compatible RDTs directly into the switch.

One DNU-S (TR-303) will terminate SONET trunks and lines [both analog and Integrated Services Digital Network (ISDN)]. One DNU-S supports approximately 30,000 lines in an area (floor space) of 25 square feet (includes the SM-2000 cabinet).

5.3.2.2 Voice Frequency Data Enhancement (VFDE)

The *5ESS*® switch implementation of TR-303 utilizes the hybrid signaling method to detect off-hook, on-hooks, and flashes along with standard Time-Slot Management Channel (TMC) message set for lines served by a TR-303 Remote Digital Terminal (RDT). This feature will enhance the TMC message set to contain nonstandard messages that will be used to allow 64KB clear channel use of a Digital Signal Level 0 (DS0) once a call has been set up. These new messages will be used to switch between clear channel mode and robbed bit mode for each individual call. This new messaging scheme will provide interoperability with RDTs that do not support these new messages.

The VFDE is operational on both the IDCU, DNU-S, and TR-303 platforms. When activated, the VFDE applies to all analog calls to/from single party Plain Old Telephone Service (POTS) lines, Wide Area Telecommunications Service (WATS) lines, and Ground Start Private Branch Exchange (PBX) lines. This new signaling mechanism will be published in 235-900-308, *5ESS*® *Switch TR-NWT-000303 Interface Specification*.

5.3.2.3 TSIU - Model 4

5.3.2.3.1 General

The TSIU4 consists of two shelves: an 8-inch high shelf which houses the power converters for the unit, the Time Slot Interchange Common (TSICOM) circuit packs, and the Data Expander (DX) [Peripheral Interface Data Bus (PIDB) Expansion] circuit packs plus a 16-inch high shelf which houses the Time Slot Interchange Slices (TSIS) circuit packs. This unit uses 9-inch deep boards for both shelves as opposed to the 13-inch boards used throughout the *5ESS*® switch. This provides more space in the back of the unit for Network Link Interfaces (NLIs) and Electrical Network Link Interfaces (ENLIs) and forced air cooling of these boards without modifying the fan unit.

The TSIU4 uses a single backplane for the entire two-shelf, two service groups unit. Two power converters per TSI/DX service group are required. The second power converter needs to be installed whenever the number of TSIS circuit packs is four or more or whenever the number of DX circuit packs equals six. One TSICOM, 10 TSIS and 6 DX circuit packs are allowed per service group. TSI service groups are split left and right and a single backplane is used for both service groups of TSI/DX. The mapping of the TSI links to the DX.

5.3.2.3.2 Time Slot Interchange Common

The Time Slot Interchange Common (TSICOM) provides the control interface to the SMP and is responsible for the synchronization timing for the SM. The TSICOM contains a stratum 4 clock for the SM. This supports the digital trunks when the SM-2000 operates as a stand-alone unit.

5.3.2.3.3 DX - PIDB Expansion

The DX board converts one TSI link into 24 PIDBs using all the time slots of the TSI link. The DX is a standard board that inserts through the front of the TSI unit. A maximum of six boards is located in the shelf immediately above the TSIS circuit packs. The TSI link for the DX may be connected either by a cable from the TSI or through the backplace traces and paddleboards.

5.3.2.3.4 Time Slot Interchange Slices

The Time Slot Interchange Slices (TSIS) circuit packs occupy the second, double-grid shelf in the TSIU4. Each TSIS circuit pack sends the data it receives from its TSI link to the first TSIS circuit pack. The first TSIS circuit pack stores all the time slots that arrive at the TSI in its TSI RAMs and sends it to the second TSIS circuit pack and so forth. The TSIS circuit packs provide four duplex TSI links. The maximum number of TSIS circuit packs that can be installed is 10. Each TSIS circuit pack terminates four TSI links.

5.3.2.4 TSIU4 (SM-2000) Version 2

The TSIU4 Version 2 (TSIU4-2), Figure 5.3-8 , provides exactly the same functionality as TSIU4 but in a different unit configuration. TSIU4-2 will still be a two-shelf duplex unit, but will use two separate backplanes in place of a single, triple-high backplane. The upper shelf is a standard 8-inch high by 13-inch deep 132-type housing, which contain one Power Converter and up to six Extended Data Expansion (XDX) (UN553) circuit packs per service group. The left side of the shelf is designated Service Group 0 (SG0) and the right side is designated Service Group 1 (SG1).

The lower shelf is a double high 500-type housing, 16 inches high and 10 inches deep, containing two Power Converters and two TSICOM packs (UM74C) stacked vertically on the left-hand side of the unit, as viewed from the front. The lower pair is in SG0; the upper pair is in SG1. The right side of the shelf contains up to 10 TSIS (KLU1B) packs per service group, with SG0 to the left and SG1 to the right of the center stiffing plate.

A minimally equipped TSIU4-2 service group contains:

- One 410AA and one 486AA Power Converter
- TSICOM (UM74C)
- One TSIS (KLU1B)
- One XDX (UN553)
- Two Control Bus Terminator (CBT) paddle boards
- One Control Time Slot Number Select (CTSNS) paddle board.

Figure 5.3-8 TSIU4 Version 2

5.3.2.5 Bidirectional Fan Unit

The SMC cabinet uses a six-fan unit with three fans mounted at the front and three fans mounted on the rear of the frame. This center-mounted unit has three fans blowing up and three fans blowing down as illustrated in Figure 5.3-3 . The fan unit contains two filters, one for each set of fans. Temperature sensors control the fans letting them operate at a quieter, lower speed under normal operating conditions. As the office temperature increases, the fans automatically adjust to provide adequate cooling.

5.3.2.6 Switching Module Processor

5.3.2.6.1 General

The Switching Module Processor (SMP) is the primary intelligence of the SM and refers to a duplex unit with the CORE40 memory subsystem. The SMP is based on either the *Motorola*® MC68040 (CORE40) or the *Motorola*® MC68060 (CORE60) microprocessor. The expanded capabilities of the CORE60 processor is the only difference from the CORE40 unit. The components of the SMP include the Application Controller (APC), the CORE40 memory, Message Handler (MH), Bus Service Node (BSN), Control Interface (CI), and Packet Interface (PI).

5.3.2.6.2 Application Controller

The Application Controller (APC) provides the Subunit Interface Bus (SUIB) and Serial TSI Control Links

(STCL). The board also connects to a TSI link and distributes its data to the message handlers. It contains application-specific interfaces between the processor unit and other SM hardware.

5.3.2.6.3 Message Handler

The Message Handler (MH) provides access from the CORE40 to the QLPS network and can terminate several message links that consist of time slots embedded in the links which are used to carry messages to and from the SMP. The MH terminates 32 time slots for messages. The Control Time Slots (CTS) and QLPS are the communication types to be handled by the MH and terminates High-Level Data Link Control (HDLC)-encapsulated messages carried in the payload time slots of the TSI.

5.3.2.7 Digital Service Unit - Model 3

5.3.2.7.1 General

The Digital Service Unit - Model 3 (DSU3) shelf houses the Digital Service Circuit - Model 3 (DSC3) circuit packs. There are a total of 18 slots in six fuse groups (of three boards each) in this unit. The unit's design provides backplane connections for all adjacent slots for multiple board services such as the RAF and announcement memory. For reliability, it is desirable to spread the DSC3s across fuse groups to avoid the loss of all three DSC3s to a single fuse failure. Refer to Figure 5.3-7 .

5.3.2.7.2 Digital Services Circuit - Model 3

The DSC3 provides four times the capacity of the DSC used in the SM. It also provides the Local Digital Service Function (LDSF). Each DSC3 circuit pack comprises a service group and has four duplex PIDBs for a total of 128 time slots of data and a duplex Peripheral Interface Control Bus (PICB) for control. A minimum of two DSC3s is required for reliability. Each DSC3 circuit pack is powered separately through an on-board power converter. The DSC3 does not support the implementation of the Service Announcement System (SAS). The SAS units for the *5ESS*® switch are on the DSU2 units in an SM or SM-2000 cabinet.

5.3.3 SWITCHING MODULE PROCESSOR UNIT - MODEL 5

The Switching Module Processor Unit - Model 5 (SMPU5) implements the SM-2000 SMP functionality in a different unit configuration. The SMPU5 development consists of three basic pieces: a new backplane which integrates DSC3 functions into the unit, a CORE60 processor board with additional integrated DRAM, and an APC board. None of these changes affect any of the TSI, its interfaces, or the SU Input/Output (I/O) interfaces with the SMP. A detailed list of all the hardware changes follows.

5.3.3.1 Unit

The SMPU5 unit is capable of supporting all SM-2000 configurations supported by SMPU4, and in particular the Very Compact Digital Exchange (VCDX). The differences between SMPU4 and SMPU5 are the equipment locations which will change for most/all boards. SMPU5 uses a single, combined power/control and display board per side; there are DSC3 slots in SMPU5; and there are only two memory slots, per side, in SMPU5. Refer to Figure 5.3-9 .

Two memory slots provide for sufficient memory growth given the currently available 32 megabytes (MB) and 64-MB memory boards. With a 128M CORE60MM board and 2, 64M memory boards, a total of 256 MB could be equipped in the SMPU5 without further development. The SMPU5 will support CORE60 with 64 MB and CORE66 will support the faster version of CORE60 with 64 MB.

The CORE60 operating at 60 MHz is designed to improve the processor performance and provide two CORE RAM configurations of either 64 MB (UN594) or 128 MB (UN588). The 64-MB CORE60MM (UN594) is supported on SMPU4 for software release 5E12. The 128-MB CORE60MM (UN588) is supported on SMPU5 for software release 5E12. The 128-MB CORE60MM (UN588) will be used for all newly shipped SMPU5 offices.

5.3.3.2 Power, Control, and Display

The Power, Control, and Display (PCD) will provide a 5 V output supply only. However, the SMPU backplane is designed to support boards which utilize onboard 3.3 V power supplies. As 3.3 V use becomes more prevalent on the CORE and MEM boards, the need to tie these converters into the +5 V alarm/detection and auto-shutdown capability provided by the PCD becomes apparent. Therefore, a single wire bus will be provided in the backplane from the PCD to the CORE and MEM slots. Future CORE and/or MEM designs may use this bus to indicate to the PCD that an internal 3.3 V power failure has occurred so the PCD can report and act on the power fault appropriately. The initial PCD design will investigate design requirements needed to provide this function but will not be required to implement this capability. A combined PCD board developed for the SMPU5 cannot be used by the existing SM-2000 with SMPU5.

5.3.3.3 Cable

The current cables used for all SMPU5 shelf 0 to shelf 1 update bus interconnects (that is, BSN and MH/MHEIB update bus cables) are integrated into the backplane.

5.3.3.4 CORE60MM

The CORE60MM design will be based on the UN560 (CORE60) design and will retain all of its functionality. As a goal, the new CORE60MM will have minimal impact to the *5ESS*® switch. The primary switch impacting area of the new CORE60MM design will be the growth of the onboard memory to a maximum equipage of 128 megabytes.

Three board codes will be created from a single AM version of the CORE60MM: a 64-MB board, a 96-MB board, and a 128-MB board. A given board code will dictate the number of DRAMs which are populated on the board in order to attain that codes particular DRAM density. In addition, the hardware will indicate to switch the amount of onboard memory.

5.3.3.5 Application Controller

The intent of the new Application Controller (APC) hardware is to be fully interchangeable with the current versions of the UN560 and UN539 boards. This means that the new APC boards can be equipped in the SMPU4, SMPU5, or Asynchronous Transfer Mode (ATM) units. Likewise, the current versions of the UN560 and UN539 can be equipped in the SMPU5 unit.

Figure 5.3-9 Switching Module Processor Unit - Model 5 Switching Module Processor Unit - Model 5

5.3.4 EXTENDED SWITCHING MODULE 2000

5.3.4.1 General

The Extended Switching Module 2000 (EXM-2000) feature provides optical remote control for an SM-2000 via Transmission Rate Converter Unit - Model 2 (TRCU2) equipment. The EXM-2000 supports the same functions and operations as the local SM-2000.

The EXM-2000 has a maximum of 24 Electrical Network Link Interfaces (ENLIs) per each side of the EXM-2000. An ENLI is the hardware which terminates Network Control and Timing links. A minimum of two primary ENLIs per EXM-2000 side (a total of four primary ENLIs per EXM-2000) must be installed. The ENLI can be terminated to up to six fully equipped TRCU2 units at each end. Each TRCU2 requires two ENLIs per EXM-2000. The ENLI terminates 256 time slots while an NLI terminates only 512 time slots.

5.3.4.2 Electrical Network Link Interface

The ENLI terminates one bi-directional electrical link to the TRCU2. This link is identical to that used between the DLI and TRCU2. It provides an optically remote SM-2000 without any modifications to the TRCU2.

5.3.5 TRANSMISSION RATE CONVERTER UNIT (TRCU3)

5.3.5.1 General

The TRCU3 supports the conversion of Network Control Timing / Network Control Timing Model 2 (NCT/NCT2) *5ESS*® switch signals into SONET (STS1), and provides the capability to remote an EXM-2000 or an Optically Remote Module (ORM) for 5E applications. The TRCU3 is replacing TRCU2 , and improving the available network time slots for an EXM-2000. TRCU3 is being implemented using NCT packs for ORM and NCT2 packs for EXM-2000 in a Digital Data Multiplexer 2000 (DDM-2000) shelf which occupy a DS3 function slot.

5.3.5.2 Detailed Description

The major difference with the EXM-2000 with the TRCU2 and the TRCU3 is the network components. The EXM-2000 with the TRCU2 network connection is limited to 512 Time Slots (TSs)/Network Link Pair. The TRCU connection provides network connection supporting 1024 TSs/Network Links Pair. While the TSI has the same capacity, there are fewer network side TSs available with the TRCU2. Both the TRCU2 and TRCU3 can be used to support an EXM-2000. When an existing EXM-2000 with TRCU2 needs to grow, it will be able to grow TRCU3s along side the existing TRCU2s. In a mixed configuration, the TRCU2s must be equipped before the TRCU3s.

The TRCU3 is made up of the following:

- Synchronous Timing Generator (TGS) – Two circuit packs (4 inches high). Provides timing.
- Optical Line Interface Unit (OLIU) – Multiplexes STS1 signals into OC-3/OC-12.
- NCT1 or NCT2 – Terminates NCT or NCT2 links from the *5ESS*® switch, converts NCT/NCT2 signals into STS1.
- Overhead Controller (OHCTL) – Provides SONET overhead to the OLIU.
- System Controller (SYSCTL) – Provides control of other circuit packs within the TRCU3.
- User Panel – Provides information and control functions.

5.3.5.3 Functional Description

The following functions are provided on the TRCU3:

- The TRCU3 unit equipped with the NCT packs will be used for remoting ORM.
- The NCT function pack terminates one 256 time slot NCT link.
- The TRCU3 unit equipped with NCT2 packs will be used to remote EXM-2000s.

The units that make up the TRCU3 provide the following functions:

- TGS – Provides timing for the TRCU3 shelf. Also provides a reference signal for network synchronization.
- OLIU – Interface with the OC-3/OC-12 optical.
- NCT1/NCT2 – Terminates one NCT or one NCT2 link per board from the TMS, ORM, or EXM-2000. Converts NCT or NCT2 signal into SONET STS1.
- OHCTL – Used in conjunction with the SYSCTL circuit pack. Provides overhead channel interface for the system.
- SYSCTL – Main System Controller in the system. Used in conjunction with the OHCTL circuit pack. Control over all shelf functions and provides all user interfaces into the system.
- User Panel – Allows CIT tasks to be performed. Provides information and control functions.

5.3.5.4 Configuration

At the host office, the TRCU3 will reside in a miscellaneous cabinet next to the Communication Module 2 (CM2). At the remote location, the TRCU3 will reside in the Switch Module Cabinet (SMC) for an ORM and the Line and Trunk Peripheral (LTP) cabinet for an EXM-2000. Each of the new circuit packs provides termination for NCT/NCT2 links and maps NCT/NCT2 signals into STS1, SONET. The following distinctions should be noted:

- The TRCU3 is equipped with NCT packs when used for remoting ORM.
- The NCT function pack terminates one 256 time slot NCT link.
- The TRCU3 is equipped with NCT2 packs when used to remote EXM-2000s.
- The NCT2 function pack terminates one 512 time slot NCT2 link.
- The NCT packs will terminate NCT links from the CM2 or the ORM.
- The NCT2 packs will terminate NCT2 links from the CM2 or the EXM-2000.

5.3.5.5 Shelf and Pack Layout

The TRCU3 feature includes new circuit packs that will support the conversion of NCT/NCT2 *5ESS*® switch signals into STS1. These new circuit packs will be used along with packs derived from the DDM-2000 OC-3 multiplexer creating a new unit called TRCU3. The TRCU3 circuit packs consist of the following:

- NCT1/NCT2 circuit packs – The NCT1 (BNP1) or NCT2 (BNP2) circuit packs terminate the NCT or

NCT2 links from the TMS, DLI, or NLI. The BNP1/BNP2 converts the NCT/NCT2 links into SONET STS1 electrical signals. In the opposite direction, the SONET STS1 electrical signals are converted to NCT/NCT2 links.

- OLIU – The OLIU multiplexes the SONET STS1 electrical signals and SONET overhead signals into OC-3 or OC-12 transmission to the remote office which contains the ORM or EXM-2000. In the opposite direction, the OLIU demultiplexes the OC-3 or OC-12 signal back into SONET STS1 and SONET overhead. Intrashelf control is provided by SYSCTL.

- TGS – The TGS provides timing to NCT1 (BNP1)/NCT2 (BNP2) and OLIU circuit packs. Control is provided by SYSCTL.

- SYSCTL – SYSCTL provides control and monitoring of all circuit packs in the TRCU3. It communicates with the OHCTL through a dedicated bus via dual port RAM. The SYSCTL provides front and rear S-232D interfaces to a Craft Interface Terminal (CIT) for local craft interface.

- OHCTL – OHCTL accesses the SONET Data Communications Channel (DCC) through the OLIU and processes the OSI 7-layer protocol as specified for the DCC. The OHCTL also provides an x.25/TL-1 gateway interface for access to remote Operation Support (OS) Systems and a 10-base LAN interface for extending the DCC to a colocated SNC-2000 EMS or to other colocated SONET network elements.

For each TRCU3 path, there is one additional time slot required for special control purposes. One time slot, referred to as the Control Time Slot (CTS) is used for messaging with ORM. The additional time slot, referred to as the Transmission Control Time Slot (TCTS), is used with both ORMs and EXM-2000s. Because of the control time slot, the number of ORMs in an office is limited to 120. As a result of these time slot restrictions, an ORM cannot use two traffic bearing time slots with each link, and an EXM-2000 cannot use one.

The mapping of network control and timing signals are performed by the NCT/NCT2 circuit packs of the TRCU3 proceeds independently of the host or remoted switch. The TRCU3 circuit packs are listed in Figure 5.3-10

Figure 5.3-10 Transmission Rate Converter Unit Model 3 Transmission Rate Converter Unit Model 3

5.3.6 DIGITAL NETWORK UNIT-SONET - J5D003FR-1

5.3.6.1 General

The SM-2000 also supports the Digital Network Unit-SONET (DNU-S), which provides an STSX-1 trunk interface. It is a high-capacity, digital, trunk-termination vehicle which can support up to 8,064 trunks via a new SONET STS-1 interface.

The DNU-S interface to the SM-2000 Time Slot Interchange (TSI) is via new optical Peripheral Control and Timing (PCT) links. These links are 65.536 Mbps and replace the Peripheral Interface Data Bus (PIDB) and Peripheral Interface Control Bus (PICB) interfaces currently used by existing Switching Module (SM) peripherals; for example, Line Units (LU)s, Digital Line and Trunk Units (DLTUs), etc.

The DNU-S interface to the network is via electrical STS1 STSX-1 links. This interface is a standard SONET interface and, as such, is compatible with transmission equipment that supports the STS1 interface, including the Digital Access and Cross Connect System IV - 2000 (DACS-2000) and the Dual Digital Multiplexer-2000 (DDM-2000).

The DNU-S, as a *5ESS*® switch peripheral, provides complete Operations, Administration, and Maintenance (OA&M) and provisioning functions. This includes capabilities such as Recent Change/Verify (RC/V), Performance Monitoring, Call Trace, Alarming, etc.

Initially, the DNU-S is capable of supporting 12 STSX-1 high-speed trunk interfaces. Each STSX-1 can support 672 DS0s.

The DNU-S is in the Line Trunk Peripheral (LTP) cabinet of the SM-2000 and can accommodate two DNU-S units, one above and one below the center-mounted bidirectional fan unit.

The DNU-S is a double-high (16-inch) shelf unit which fits into the new *5ESS*® switch cabinet. The DNU-S unit uses a single backplane for the entire unit and uses 16- by 13-inch KLW-coded circuit boards. Common Optical Termination (COT) and STSX-1 Link Interface (SLI) paddleboards connect to the rear of the backplane.

The unit is divided into two mirror-imaged data groups around the duplexed Common Control (CC) circuit packs located at the center of the unit. In simplex mode, each CC can control both data groups. Each data group contains duplexed Common Data (CD) and STSX-1 Facility Interface (SFI) packs and the engineered number of simplex service Transmission Multiplexer (TMUX) packs plus one spare TMUX (TMUX-S) for protection. The amount of TMUX packs used in each data group is dependent on the number of STX-1 transmission links that are terminated onto the DNU-S.

Table 5.3-1 provides the quantities of DNU-S components required.

Table 5.3-1 DNU-S Engineering Quantities

ELEMENT	MAX SERV EQUIP	MIN OPER EQUIP	MIN SERV EQUIP	DESCRIPTION
Message Handler (MH)	2	2 **a**	2	SM-2000 Unit 32 Time Slots.
DNU-S Unit	8 **b**	1	1	SM-2000 Peripheral Capacity: 8064 Trunks.
PCT Links (Duplicated)	24	2	2	Interface to SM-2000 1-6 pair per Data Group
PCT Link Interface (PLI) (Duplicated)	24	2	2	Paddleboard on SM-2000. One per PCT link.
Common Control (CC) (Duplicated)	2	2	2	DNU-S Processor. One pair per DNU-S Unit.
Common Data (CD) (Duplicated)	4	2	2	One pair per Data Group.
Common Optical Paddleboard on DNU-S	24	2	2	Termination (COT). One per PCT link.

(Duplicated)				
Transmission Multiplexer (TMUX)	14	1	2	One Spare and 1-6 Active per Data Group.
STSX-1 Facility Interface (SFI) (Duplicated)	4	2	2	One pair per Data Group.
STSX-1 Link Interface (SLI)	12	0	1	Paddleboard. One per STSX-1 Link.
STSX-1 Link	12	0	1	Interface to Transmission. 1-6 per Data Group.
STE/STS1	12	0	1	1 per STSX-1.
VT1.5/DSI	28 x 12	0	1	1-28 per STSX-1.

Notes:

a. A second MH is required for DNU-S. If the SM-2000 does not support a DNU-S, it only needs one MH.

b. Release 1 must support up to four DNU-Ss.

5.3.6.2 Common Control

The DNU-S contains two CC circuit packs which implement a duplex unit controller that operates in an active/standby mode and performs the following functions:

- Terminates the communication and control channels that originate from the SM-2000 CORE40 and are interfaced via the PCT links and Common Data (CD) circuit packs.
- Supervises unit initialization, maintenance, and diagnostics.
- Implements and handles the control interfaces to all DNU-S circuits.
- Provides nonvolatile storage of CC and TMUX control programs in flash memory.

5.3.6.3 Common Optical Terminator

The Common Optical Termination (COT), 982TN, terminates the optical fibers for one side of a duplex PCT link and performs optical-to-electrical and electrical-to-optical conversion of data and control information received by and transmitted over the PCT link interface with the SM-2000. The DNU-S may be equipped with up to 24 COT paddleboards.

5.3.6.4 Common Data

The DNU-S may be equipped with either two or four Common Data (CD) packs with two packs in each data group. The two packs in each data group are designated as "mates." For example, CD00 and CD01 are mate CDs; CD10 and CD11 are mate CDs.

The mate CDs in each data group can terminate up to six duplicated PCT links with side 0 for each duplicated link terminating on one CD and side 1 terminating on the other CD. The mate CDs in each group operate active/standby.

The CDs logically terminate the PCT links and perform rate conversion, selection, and multiplexing/demultiplexing functions that are associated with the passage of data and control information between the PCT links and internal interfaces with other packs in the unit.

The CD performs specific functions, which include:

- Interfaces with up to six normally active Transmission Multiplexer (TMUX) packs, where each terminates one STSX-1 link and mapping data and signaling information among the TMUXs and up to six PCT links with the STS1 information for each TMUX mapped onto one PCT link.
- Interfaces with a spare TMUX pack and supports TMUX pack sparing capabilities.

- Converts data and signaling information between the PCT link format and the Bi-Peripheral Interface Data Bus (BPIDB) format used internal to the DNU-S to pass information between the TMUX and CD packs.
- Extracts and inserts unit control information on PCT link 000/001 and implements the Peripheral Control and Maintenance Bus (PCAMB) interface to the CCs (in CD data group 0 only.)
- Extracts and inserts the SONET Section Data Communications Channel (DCC), line DCC, section orderwire, and low orderwire information on the PCTs.
- Derives system reference timing from the *5ESS*® switch and sources synchronization timing to the rest of the DNU-S.

5.3.6.5 Transmission Multiplexer

The Transmission Multiplexer (TMUX) provides the format conversion of data between one STSX-1 link and 14 BPIDB structures, including the mapping of data time slots between the two formats and signaling bit conversion.

The DNU-S may be equipped with up to 14 TMUX packs. In each data group, the TMUXs implement an N+1 sparing arrangement with up to six active TMUXs and one spare that can be switched into service in place of any of the active TMUXs.

The TMUX also performs functions associated with terminating the STS1 SONET and facility overhead, including the following:

- Terminates STS1 line and section overhead.
- Terminates STS1 path overhead and extracts Virtual Tributary (VT).
- Frames and extracts DS1.
- Detects DS1 facility alarms.
- Checks DS1 Cyclic Redundancy Code (CRC).
- Initial collection of STS1 and DS1 performance monitoring data.
- Facilitates data alignment to the system clock.

5.3.6.6 STSX-1 Facility Interface

The DNU-S may be equipped with two to four STSX-1 Facility Interface (SFI) packs with two in each data group. Each pair of SFI packs implements a duplicated electrical interface for six STSX-1 links. The SFI implements STSX-1 line drivers and receivers, Bipolar 3-Zero (B3SZ) encoding and decoding, and connects each of the six STSX-1 links to either one active or the spare TMUX.

5.3.6.7 STSX-1 Link Interface

The DNU-S may be equipped with up to 12 SLI paddleboards with each board terminating one STSX-1 link. The SLI is a passive circuit that contains a splitting transformer for coupling the received STSX-1 signal to two SFI circuit packs and another transformer that couples the STSX-1 transmit signal from two SFIs to the facility.

Figure 5.3-11 shows the DNU-S in a cabinet with two units.

Figure 5.3-11 Digital Network Unit-SONET Physical Configuration with Two Units per Cabinet
Digital Network Unit-SONET Physical Configuration with Two Units per Cabinet

5.3.7 ANALOG TRUNK UNIT - J5D003AC-1

The Analog Trunk Unit (ATU) is a single-shelf unit that can be mounted in any vacant shelf position in the Switching Module Control cabinet or any of the Line Trunk Peripheral cabinets. Functionally, it provides termination for interoffice trunks and trunks to operator positions and announcement machines.

The unit is divided into two Service Groups, 0 and 1, each group containing a Common Circuit Pack Area and a Trunk Circuit Pack Area. There are nine different trunk circuit packs available for use, depending on the trunk circuit functions. The packs are listed in Figure 5.3-12 .

Figure 5.3-12 shows where the ATU is located in the Switching Module Control Cabinet and its respective circuit packs in the unit.

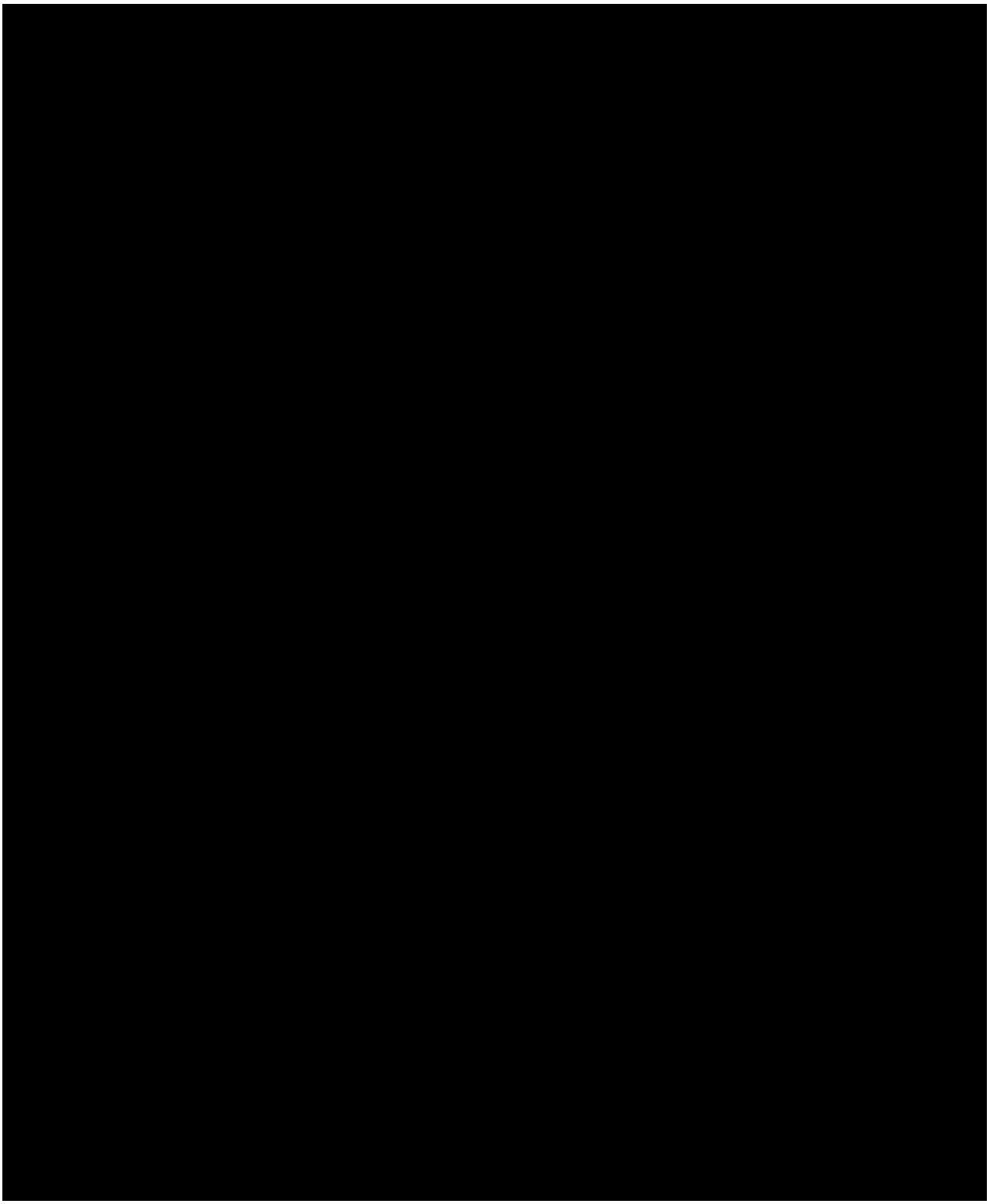

Figure 5.3-12 Analog Trunk Unit - J5D003AC-1

5.3.8 COMMON SHELF UNIT - J5D004AG-1

The Common Shelf Unit (CSU) is a single-shelf unit located in the top of the Integrated Service Line Unit (ISLU). Its purpose is to support all the equipment mounted in the ISLU drawer shelf units. The CSU is divided into Service Group 0 on the left and Service Group 1 on the right. Normally, both sides are active except for the Common Control circuit packs which always operate in active/standby.

Figure 5.3-13 illustrates the location of the CSU and the respective circuit packs in the unit.

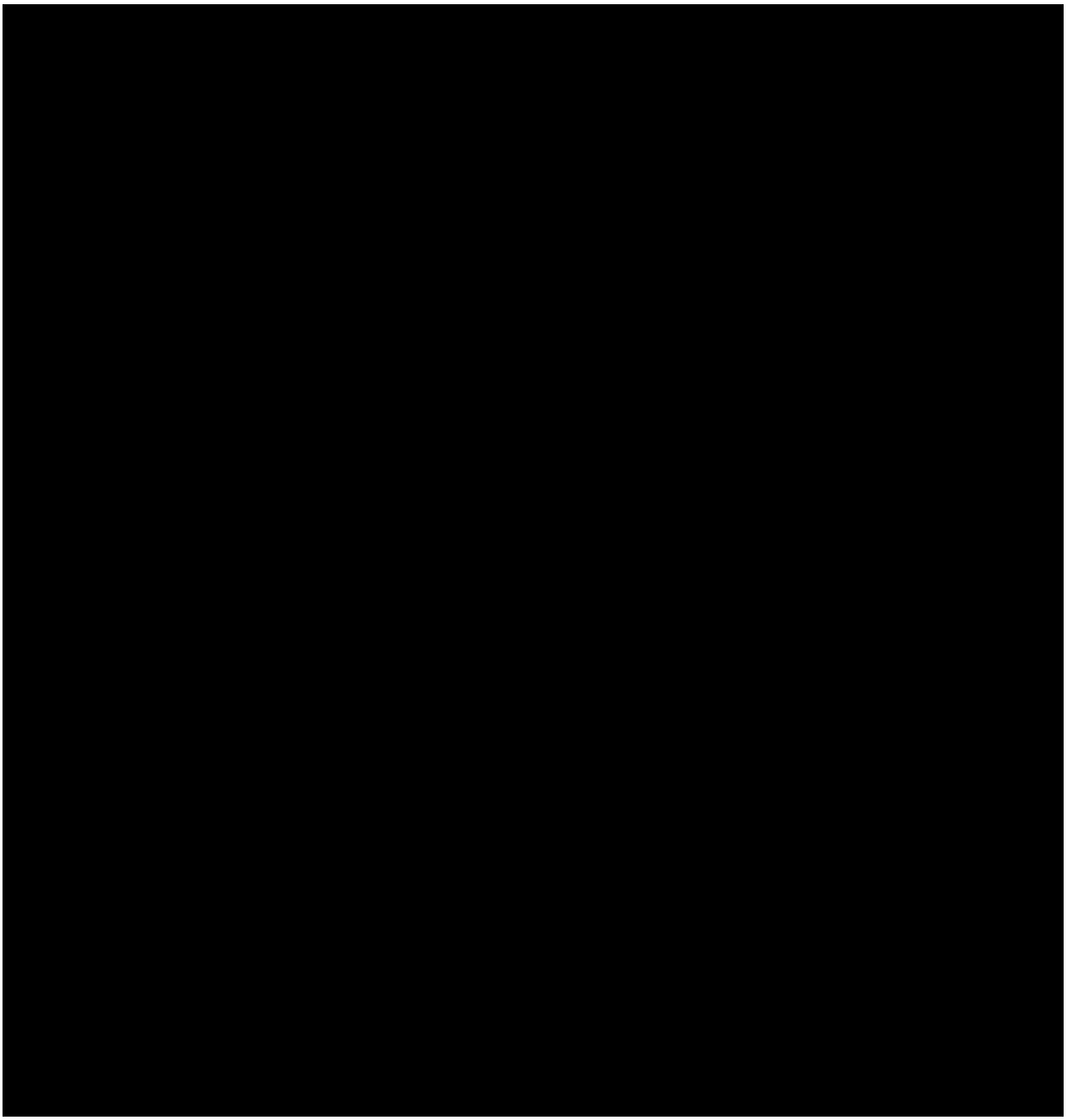

Figure 5.3-13 Common Shelf Unit - J5D004AG-1

5.3.9 DIGITAL CARRIER LINE UNITS - MODEL 2 - J5D003AR-2 (BASIC) AND J5D003AS-2 (SUPPLEMENTARY)

The basic Digital Carrier Line Unit (DCLU) is a two-shelf unit used to interface with *SLC*® 96 carrier. It is divided into Service Group 0 (lower shelf) and Service Group 1 (upper shelf).

The number of Digital Facility Interface (DFI) circuit packs (ANN4) required is variable depending on the number of *SLC*® carrier remote terminals involved and their use with *SLC*® carriers operating in Mode I or Mode II.

NOTE 1: Mode I (unconcentrated): Each *SLC*® carrier remote terminal requires five T1 lines; four working and one protecting. The 96 subscribers, at a remote location, are converted into a digital format and sent to the switch office by T1 lines (24 channels x 4 T1 lines = 96 + 1 backup T1 lines).

NOTE 2: Mode II (concentrated): Each *SLC*® remote terminal requires three T1 lines; two working and one protecting. The 96 subscribers, at a remote location, are converted into a digital format. These subscribers are also concentrated 2:1 and sent to the switch by T1 lines (24 channels x 2 T1 lines = 48 + 1 backup T1 lines).

The basic DCLU serves up to six concentrated (Mode II) *SLC*®-96 carrier remote terminals. When service for six unconcentrated (Mode I) terminals is required, use a supplementary DCLU.

The supplementary DCLU (J5D003AS-2) is a single-shelf unit which must be mounted directly above the basic DCLU.

The circuit packs ANN4 located in positions 027 through 067 (5) are associated with Service Group 0 and circuit packs ANN4 in positions 129 through 169 (5) are associated with Service Group 1.

Figure 5.3-14 illustrates the location of the basic DCLU in the Switching Module Line Peripheral Unit and the respective circuit packs in the unit.

Figure 5.3-15 illustrates the location of the supplementary DCLU in the Switching Module Line Peripheral Unit and the circuit packs in it.

NOTE: *SLC*® carrier remote terminals which are connected by fiber optic facilities do not require protect lines. Protection is built into the fiber optic facilities.

Table 5.3-2 lists equalizer circuit packs from which an appropriate selection can be made, dependent on hookup distance to DXA and cable type.

Table 5.3-2 Equalizer Table

CIRCUIT PACK	DISTANCE TO DSX-1 BAY 607C CABLE	DISTANCE TO DSX-1 BAY 1249 CABLE
SN215	001' to 133'	001' to 090'
SN216	134' to 267'	091' to 180'
SN217	268' to 400'	181' to 270'
SN218	401' to 533'	217' to 360'
SN219	534' to 665'	362' to 450'

Figure 5.3-14 Basic Digital Carrier Line Unit - Model 2 - J5D003AR-2

Figure 5.3-15 Supplementary Digital Carrier Line Unit - J5D003AS-2

5.3.10 DIGITAL LINE AND TRUNK UNITS

5.3.10.1 Digital Line Trunk Unit - J5D003AD-1

The Digital Line Trunk Unit (DLTU) is a single-shelf unit that can be mounted in any Line Trunk Peripheral cabinet in shelf position 1 through 6. It can also be mounted in any vacant shelf (1, 5, or 6) of the Switching Module Control cabinet.

The main function of the DLTU is to provide direct interfacing with digital transmission facilities. Because of time slot restrictions, a host switching module can have a maximum of two fully equipped DLTUs.

The DLTU can mount up to 10 Digital Facility Interface (DFI) packs, ANN3B, or ANN5B.

The ANN3B pack must connect with other offices when using direct digital trunking (T1 facilities). Use the ANN5B pack when connecting to the umbilical T1 facilities of a remote switching module.

Figure 5.3-16 illustrates the location of the Digital Line Trunk Unit and the respective circuit packs in the unit.

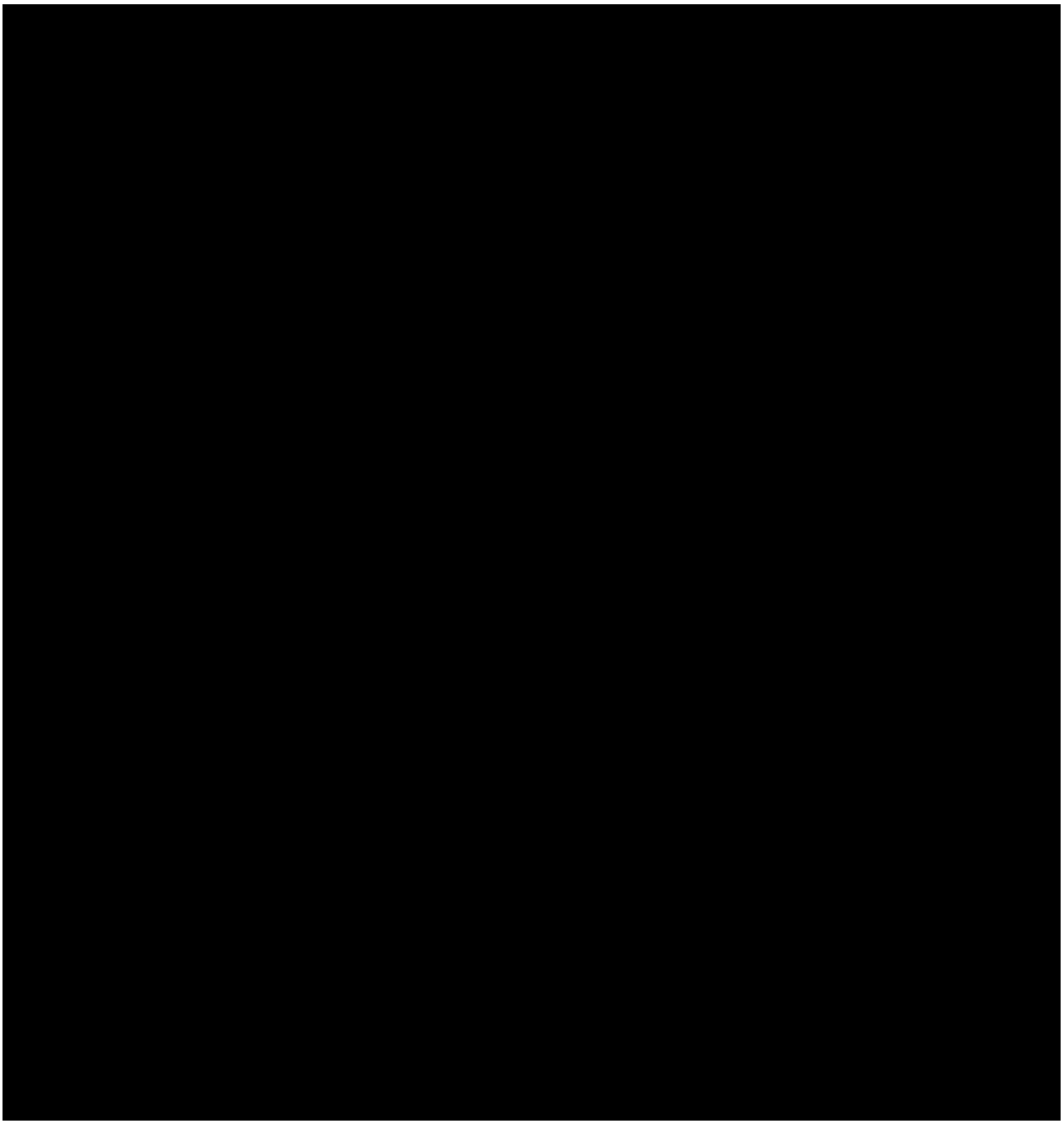

Figure 5.3-16 Digital Line Trunk Unit - J5D003AD-1

5.3.10.2 Digital Line Trunk Unit - Model 2 - J5D024AA-1

The Digital Line Trunk Unit - Model 2 (DLTU2) is a single-shelf unit that can be mounted in any Line Trunk Peripheral cabinet in shelf position 1 through 6. It can also be mounted in any vacant shelf of the Switching Module Control cabinet.

The DLTU2 can mount up to 10 Digital Facility Interface (DFI) packs, TN1611 or TN1612, each capable of terminating two T1 lines. The TN1611 (DFI2-T) packs are used for trunks, and the TN1612 (DFI2-R) packs interface with remote SMs.

The main function of the DLTU2 is to provide interfacing with digital transmission facilities. Because of time slot restrictions, a host switching module can have a maximum of one fully equipped DLTU2s.

Figure 5.3-17 illustrates the location of the DLTU2 and its respective circuit packs.

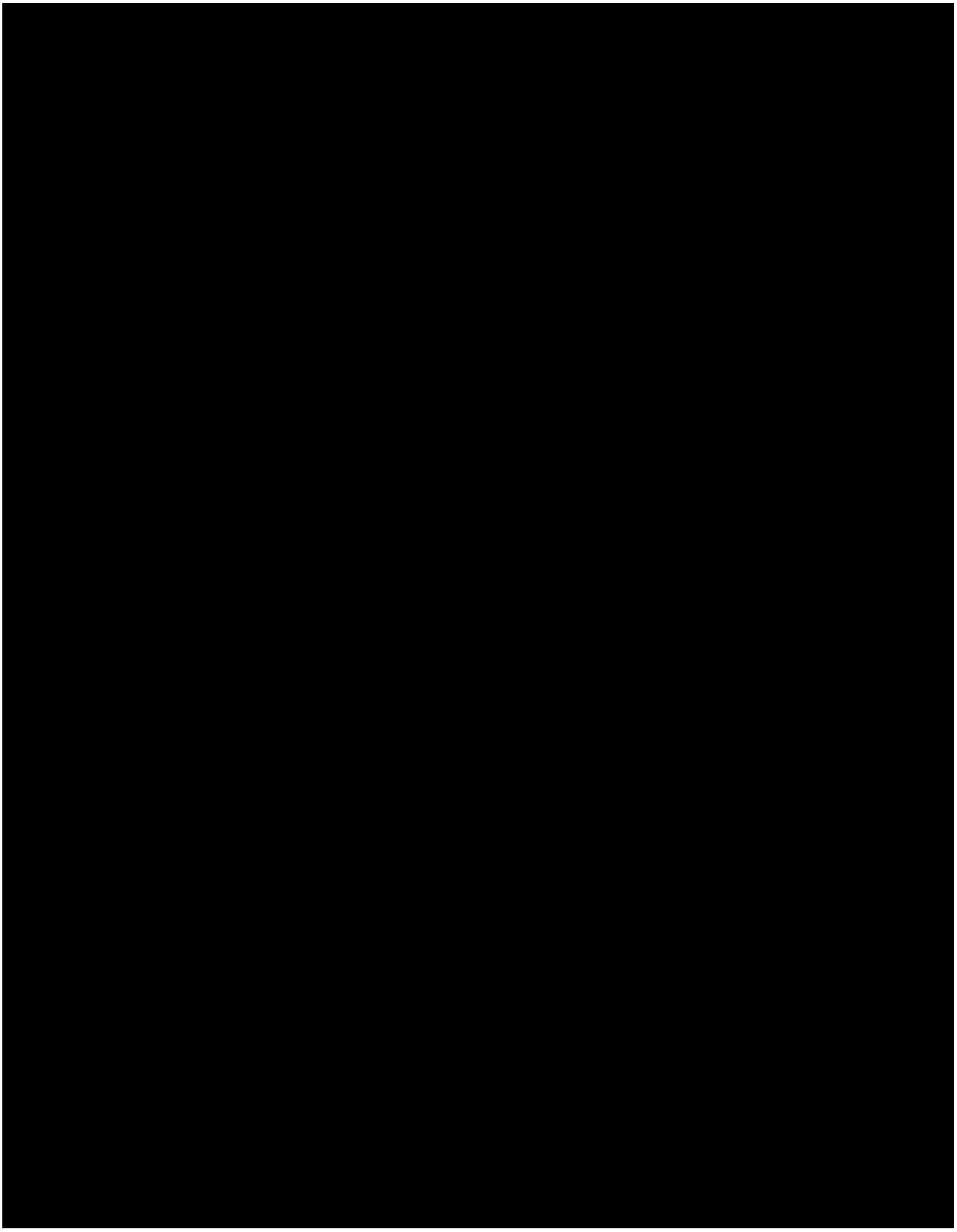

Figure 5.3-17 Digital Line Trunk Unit - Model 2

5.3.10.3 Echo Canceling Service Unit

The Echo Canceler exists on 30 channel export DFI facilities in international. Porting of Echo Canceler to the U.S. means it will be ported for 24 channel DFI/DF2 facilities. For dual facility DFIs, each facility has Echo Canceler 5 (EC5) circuit pack associated with it.

5.3.10.3.1 Audits

Audits (AU) support the Echo Canceler Service Unit (ECSU) in the U.S. by porting changes to the CKTDATA, CDBCOM, and SCNMSK audits. Changes to the CKTDATA, CDBCOM, and SCNMSK audits include cases to audit the PCEC5 circuit type. Basically, the CKTDATA and CDBCOM audits do the same checks on the PCE5 circuit as the checks done for the PCTI_DFI circuit. The SCNMSK audit does the same checks on the PCE5 circuit as the checks done for the PCDFI circuit.

5.3.10.3.2 Peripheral Control

Peripheral Control (PC) provides the same echo functionality to the U.S. code as it does to the international code. The ECSU is the hardware that provides the echo canceling in the *5ESS*® switch. The signaling unit (CCITT5) part of the ESCU is not supported in the U.S. code.

The ESCU occupies its own shelf space in the switching module. The ECSU is situated between the Time Slot Interchange Unit and the Digital Line Trunk Unit. An ECSU may contain several EC5 boards. Each EC5 interfaces with a DFI in the DLTU. A particular EC5 provides echo canceling for the channels of the interfacing DFI. Figure 5.3-18 shows the physical layout of an ESCU.

Figure 5.3-18 Echo Canceler Service Unit

The ECSU and DLTU require the same service request treatment because EC5 has the same CCB structure as a DFI. They are companion circuits, and the EC5 has the same CCB structure for peripheral fault recovery and unexpected activity or unused registers. The canceler control code is comprised of the

primitive LPec_cntl() and the global header PCec_cntl, which is used to specify whether enabling or disabling of the Echo Canceler is desired.

If more information is required for the ECSU, refer to 235-200-100, *5ESS® Switch FLEXENT™/AUTOPLEX® Wireless Networks Applications OA&M Manual*.

5.3.11 DIGITAL SERVICE UNITS

5.3.11.1 Introduction

The Digital Service Unit (DSU) was developed with flexible hardware so that both local and global DSUs are served by a common, optional plug-in unit. As a result of transitions brought about by software releases, there are at least five versions of the DSU in use, including Model 2.

Table 5.3-3 lists the versions by ``J" drawing number.

Table 5.3-3 Digital Service Units

J DRAWING	FIGURE NUMBER	UNIT NAME
J5D003AE-1	5.3-19	GLOBAL DSU
J5D003AE-1	5.3-20	LOCAL DSU
J5D003AE-1	5.3-21	LOCAL DSU (modified)
J5D003EA-1	5.3-22	DSU-MODEL 2
J5D003EA-1	5.3-23	DSU-MODEL 2 (RAF)

5.3.11.2 Global Digital Service Unit - J5D003AE-1

The Global Digital Service Unit (GDSU) is a single-shelf unit that can be mounted in any vacant shelf position in the Switching Module Control cabinet or any of the Line Trunk Peripheral cabinets. Functionally, it houses low-usage, low-level service circuits, Transmission Test Facility (TTF), and conference circuits.

The unit is divided into two Service Groups, 0 and 1, each independent of the other. A service group can mount up to eight digital service circuit packs.

Figure 5.3-19 illustrates the Global Digital Service Unit and the respective circuit packs in it.

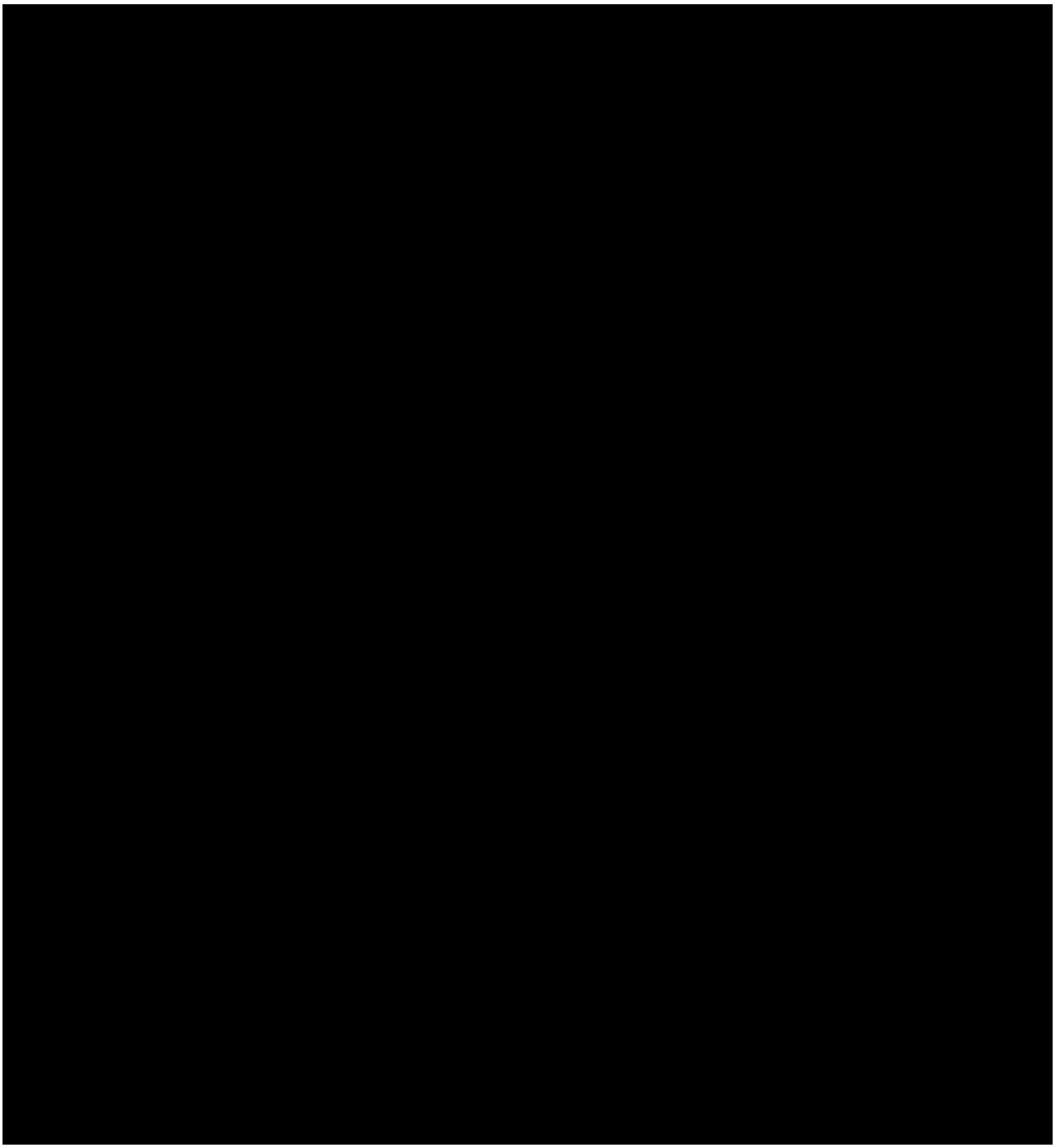

Figure 5.3-19 Global Digital Service Unit - J5D003AE-1

5.3.11.3 Local Digital Service Unit - J5D003AE-1

The Local Digital Service Unit (LDSU) is a single-shelf unit that normally mounts directly above the Module Controller Time Slot Interchanger Unit in the Switching Module Control cabinet. The unit is divided into two Service Groups, 0 and 1, each independent of the other.

Functionally, the LDSU contains low-level service circuits that require high usage, such as audible ring, busy tone, high tone, multifrequency tones, and touch tone.

Electronic offices sometimes connect with Panel and Crossbar offices. If this is the case, revertive pulsing may be required; replace the Digital Service Circuit (TN133) in locations 088 and 178 with a Revertive

Pulsing Transceiver (TN853) pack.

Figure 5.3-20 illustrates the LDSU and the circuit packs in it.

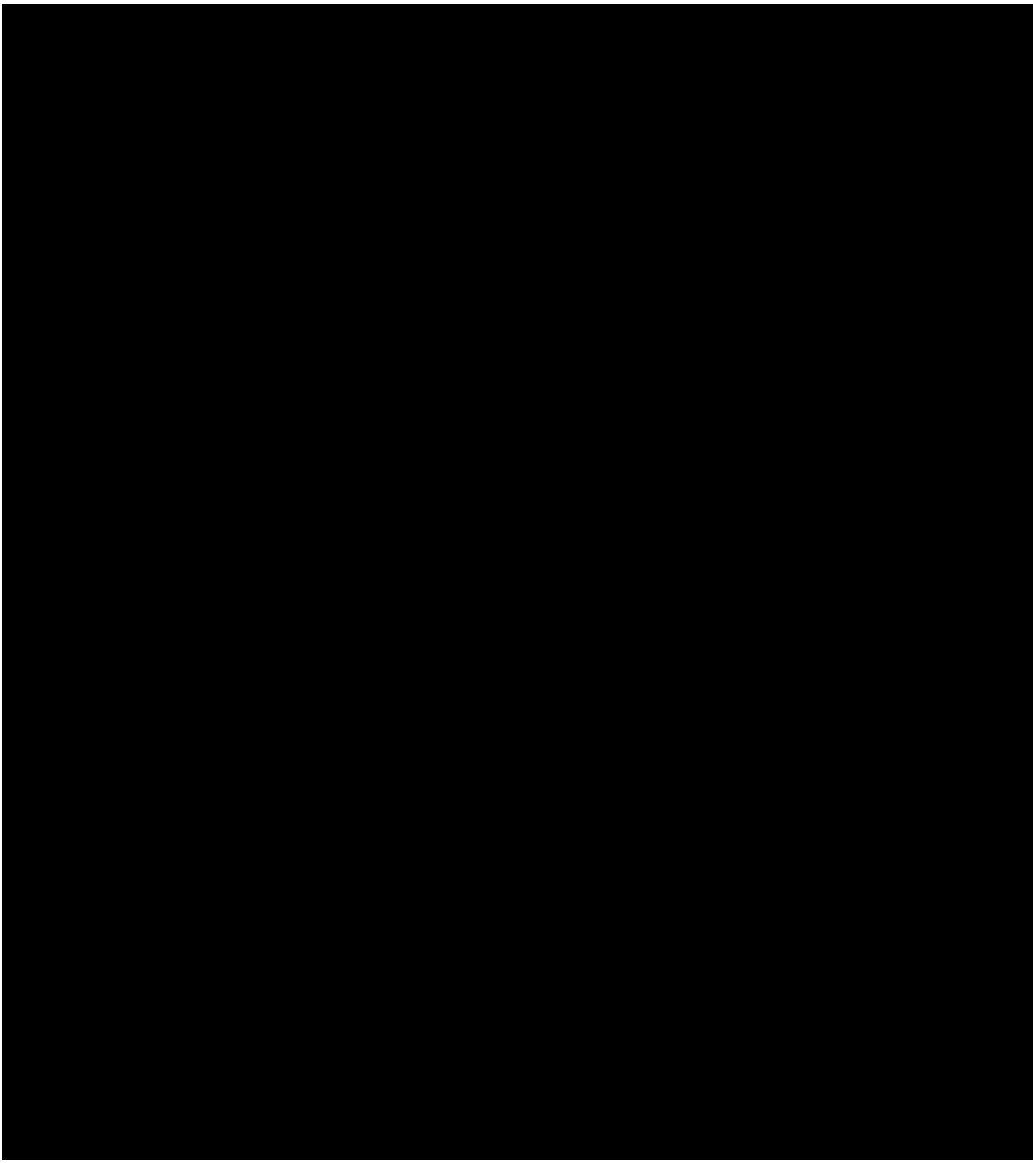

Figure 5.3-20 Local Digital Service Unit - J5D003AE-1

5.3.11.4 Local Digital Service Unit (Modified) - J5D003AE-1

The Local Digital Service Unit (Modified) (LDSUM) replaces all the Universal Tone Decoders (TN133), Universal Tone Generators (TN132), and Common Digital Service Units (TN128) in the LDSU with a single Digital Service Circuit (TN1637).

This version provides the LDSU with the functional capability supplied in the later available Model 2 DSU. Service Groups 0 and 1 are still present, each independent of the other.

Figure 5.3-21 illustrates the LDSUM and its circuit packs.

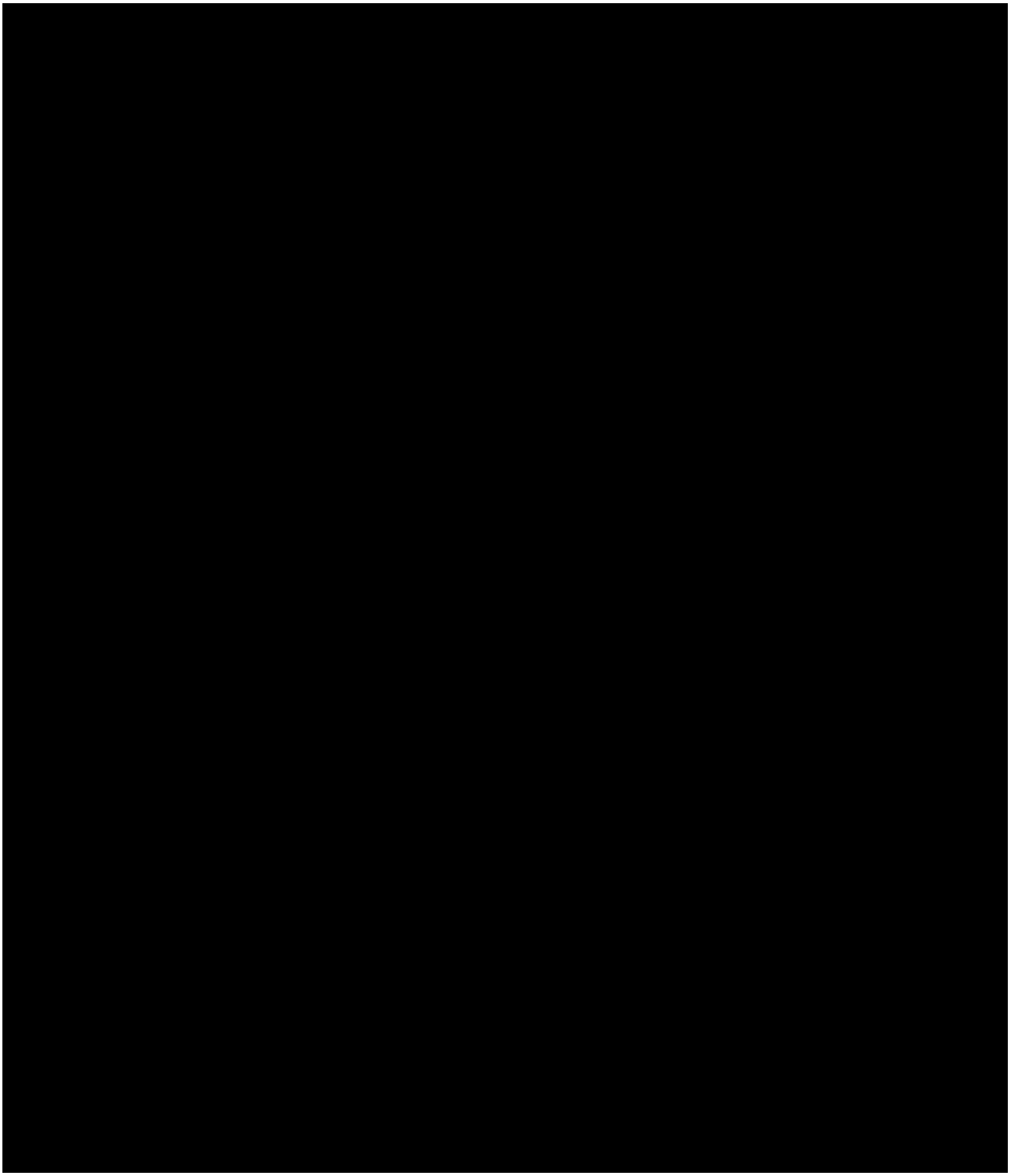

Figure 5.3-21 Local Digital Service Unit (Modified) - J5D003AE-1

5.3.11.5 Digital Service Unit - Model 2 - J5D003EA-1

The Digital Service Unit - Model 2 is a single-shelf unit divided into two Service Groups, 0 and 1, each

independent of the other.

Figure 5.3-22 illustrates the location of the DSU2 and the respective circuit packs in the unit.

Figure 5.3-23 illustrates the ISDN-accommodated unit and the circuit packs in it.

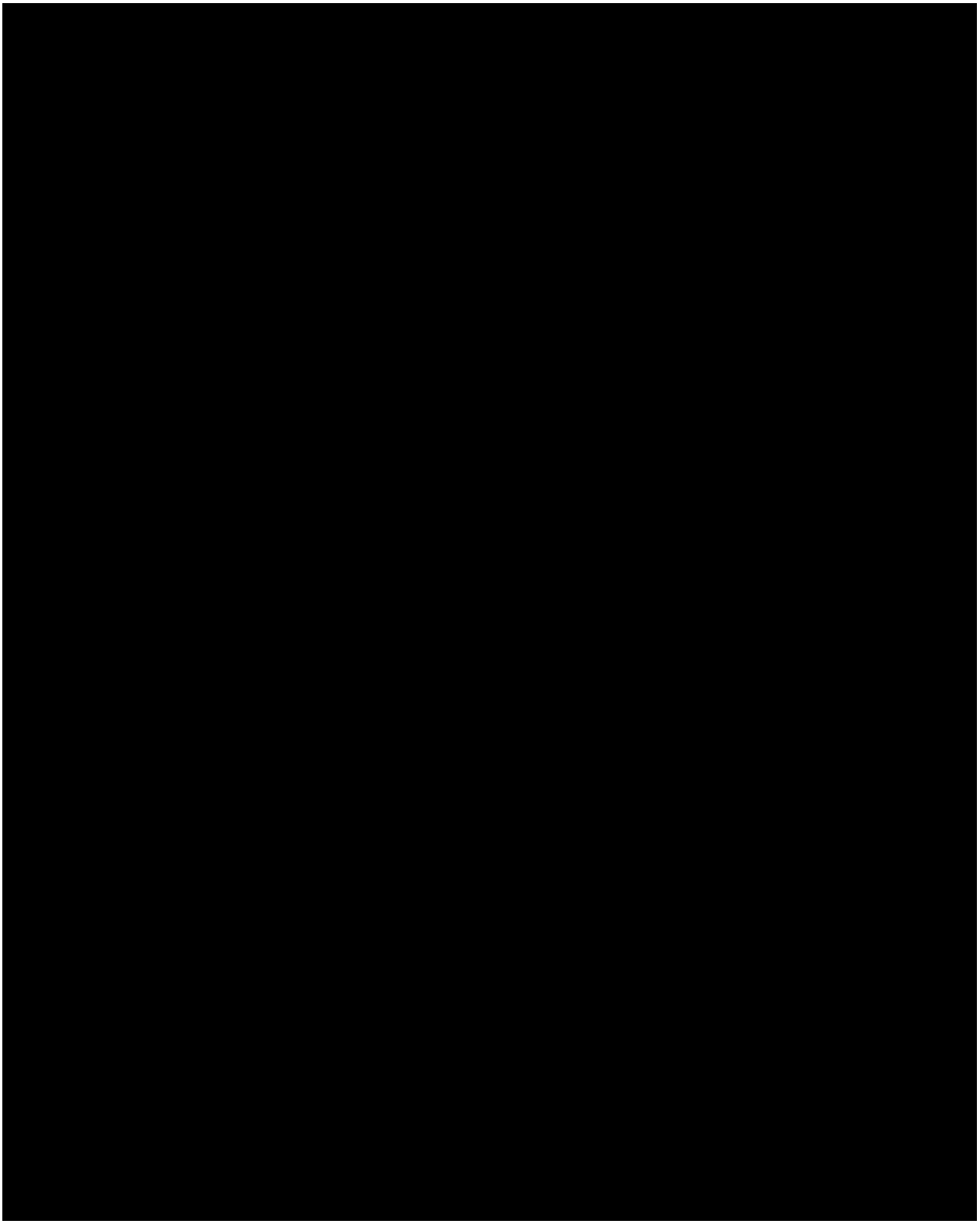

Figure 5.3-22 Digital Service Unit - Model 2 - J5D003EA-1

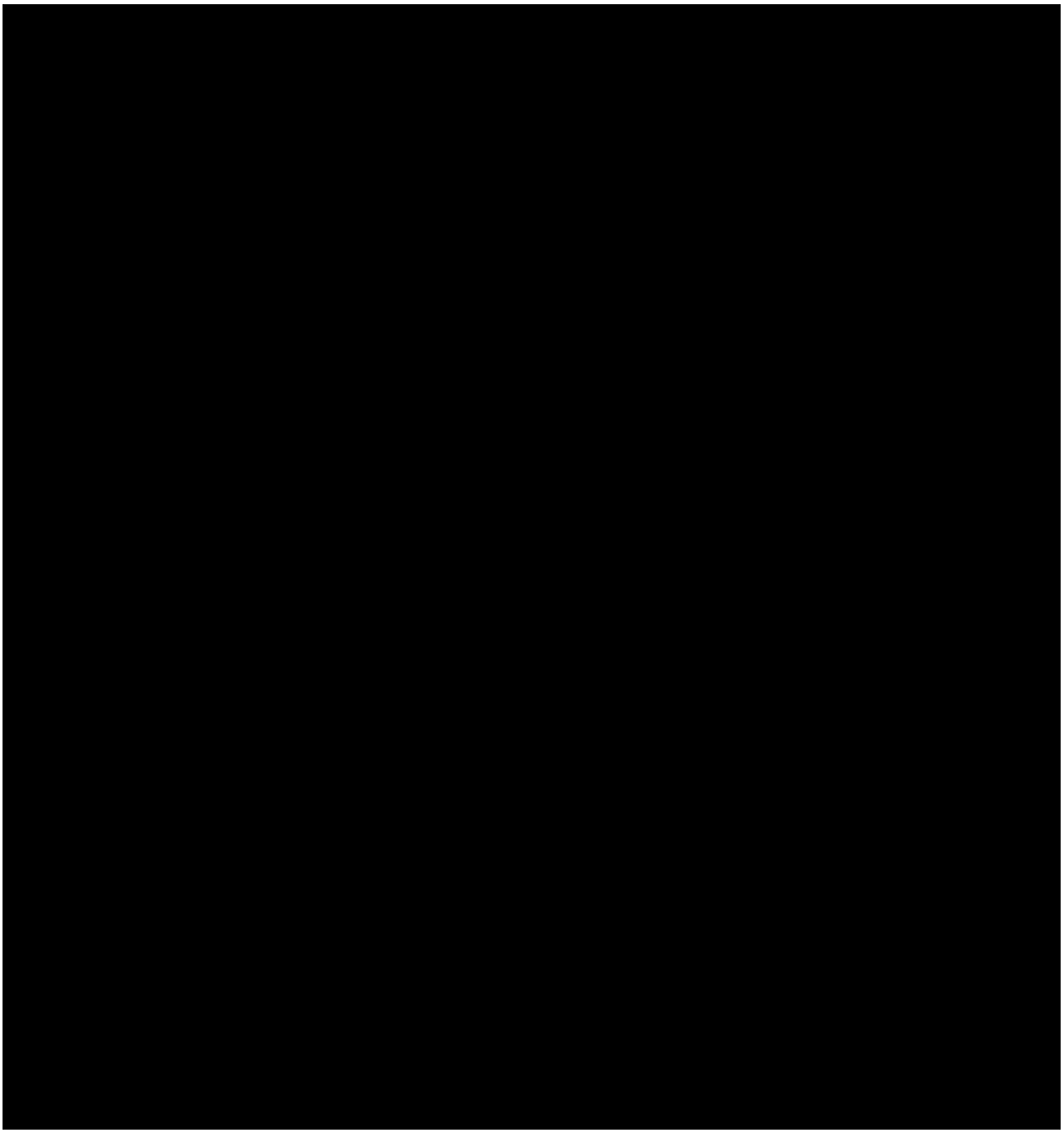

Figure 5.3-23 DSU - Model 2 - Peripheral - J5D003EA-1

5.3.12 RECORDED ANNOUNCEMENT FUNCTION DSU2

The Recorded Announcement Function (RAF) lets more than one caller be connected to a single RAF circuit that broadcasts a particular General Recorded Announcement (GRA). For each GRA broadcast, at least one of the 32 circuits in an RAF unit is needed. If more callers are to be connected to the announcement than a single RAF circuit can handle, then more RAF circuits in the same or other RAF units must be assigned to broadcast the same announcement.

Figure 5.3-23 shows the location of RAF functions in the DSU2.

5.3.13 COMBINED SERVICE UNIT (CSU) - J5D003FS-1

The Combined Services Unit (CSU) applies only to the SM (not the SM-2000). The CSU combines the DLTU2, MMSU, DSU2-SAS, and GDSF into one shelf.

The new CSU is compatible with existing units DLTU2, DSU2-RAF2, and GDSU in the same office, the same SM, or in different SMs. The MMSU in the repackaged version will have only one service group, thereby making it incompatible with the standard MMSU which has two service groups. Therefore, if office growth to conventional configurations necessitates greater metallic services, the standard MMSU will need to be provided and the MMSU portion of the repackaged shelf will have to be degrown. Figure 5.3-24 illustrates the location of the CSU and the respective circuit packs in the unit.

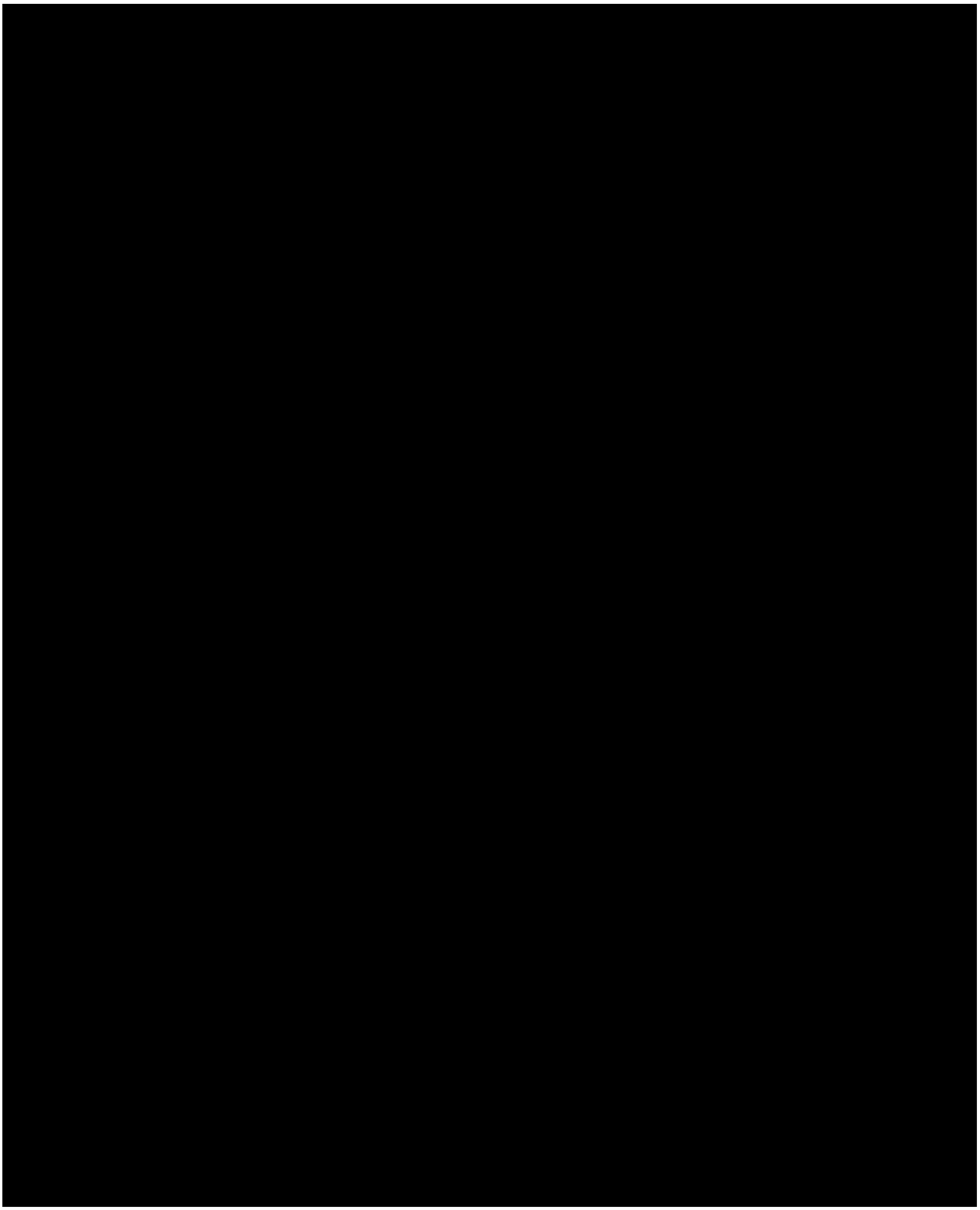

Figure 5.3-24 CSU - Peripheral - J5D003FS-1

5.3.14 SERVICE ANNOUNCEMENT SYSTEM

The Service Announcement System (SAS) and the RAF function operate in a similar way. The difference is that the SAS contains additional functions necessary to support features such as Automatic Collect Call (ACC). These new features require functions such as digit reception, and the recording and playback of a

caller's name on a per-call basis. The SAS provides these new functions in addition to all existing functions currently supported on the RAF.

A SAS unit consists of two major components: a controller board and up to four memory boards. These boards are plug-in compatible with the existing DSU2 and can be placed into any slot of the DSU2 except position 0. A SAS unit is created by placing a controller board in any slot position, except position 0, with at least one but no more then four memory boards in the slots immediately to the right of the controller board.

Like the RAF, the SAS is a global resource. A SAS unit located in a particular DSU2 is accessible from any other SM in the *5ESS*® switch. A SAS unit may be mixed on the same physical DSU2 with other RAF, ISTF, and TTF2 circuit packs.

SAS announcements are defined through Office Dependent Data (ODD) as a series of phrases. These phrases are stored on the memory board(s) in a SAS unit housed in a DSU2. The announcements can be changed by reconfiguring the ODD announcement definitions using the phrases already stored in the SAS unit. The memory board phrases are stored on flash memory devices.

Each SAS unit can provide up to 32 independently phased announcement channels; thus 32 separate announcements can be played or 32 copies of the same announcement can be played simultaneously. Access to any of the 32 channels of a SAS unit provides access to any of the stored announcements of an announcement set. Multiple SAS units can handle the traffic load to the announcements supported by the announcement set.

Figure 5.3-25 shows the coexisting SAS/RAF equipment locations and restrictions.

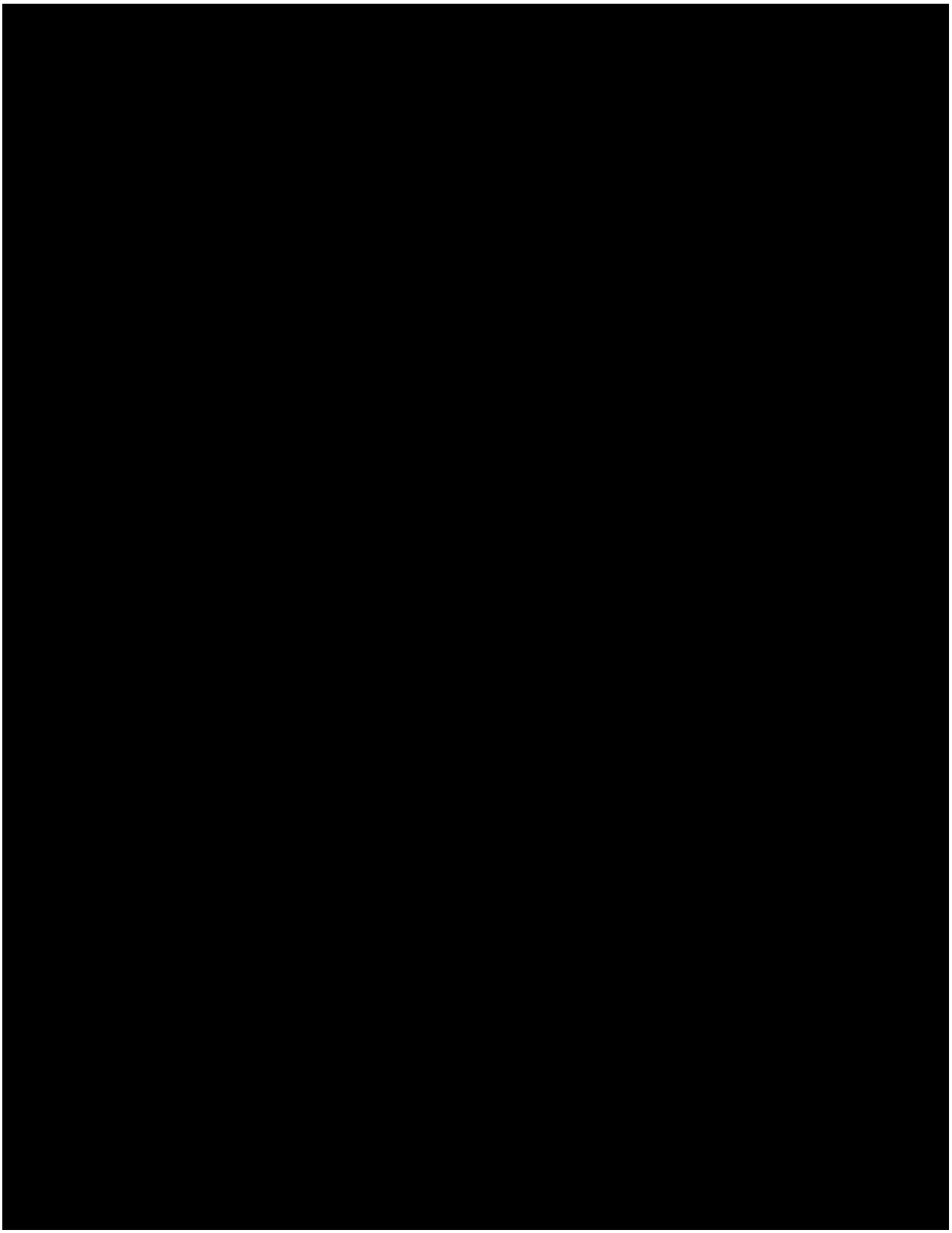

Figure 5.3-25 SAS Equipment Locations and Restrictions

Each service group (SG0, SG1, SG2, and SG3) has one to four memory boards, each having slots for eight flash memory cards. These cards are PCMCIA standard memory cards, which may vary in capacity and can be used in any quantity from one through eight.

5.3.14.1 SAS Controller Board

The SAS Digital Service Circuit (SASDSC) controller board (TN1841) contains the Digital Signal Processors (DSPs) and provides the PICB and PIDB interface to the SM and the interface to the SAS Memory (SASMEM) board(s). Like the RAFDSC, the SASDSC can support up to 32 time slots.

5.3.14.2 SAS Memory Board

Up to four SAS Memory (SASMEM) boards (TN1842) can be installed in a SAS unit. Each SASMEM board can be equipped with up to eight PCMCIA flash memory cards of the same or varying capacity. The 4-MB flash cards provide 422 seconds of speech recording space per card, which yields 3367 seconds of recording space per memory board.

5.3.15 DIRECTLY CONNECTED TEST UNIT - J1P023AM-1

The Directly Connected Test Unit (DCTU) can be a two-, three-, or four-shelf unit, depending on the size and needs of an office. The basic unit always has two shelves: the upper containing the DCTU controller, the control interface, the Equipment Access Network (EAN) circuits, and the power converters; the lower containing the Precision Measuring Unit (PMU).

The DCTU must be mounted at the top of the cabinet. If only a basic unit is initially furnished, reserve space for two additional precision measuring units (PM02 and PM03).

The DCTU performs the following:

- Performs testing of lines and trunks.
- Provides certain central office-related maintenance activities such as DC voltage, resistance and capacitance measurements, and low frequency readings of facilities.

The DCTU is dependent on the switch office for its control functions and metallic paths required to establish connections to facilities requiring the test functions.

Figure 5.3-26 illustrates the location of the Directly Connected Test Unit and the respective circuit packs in the unit.

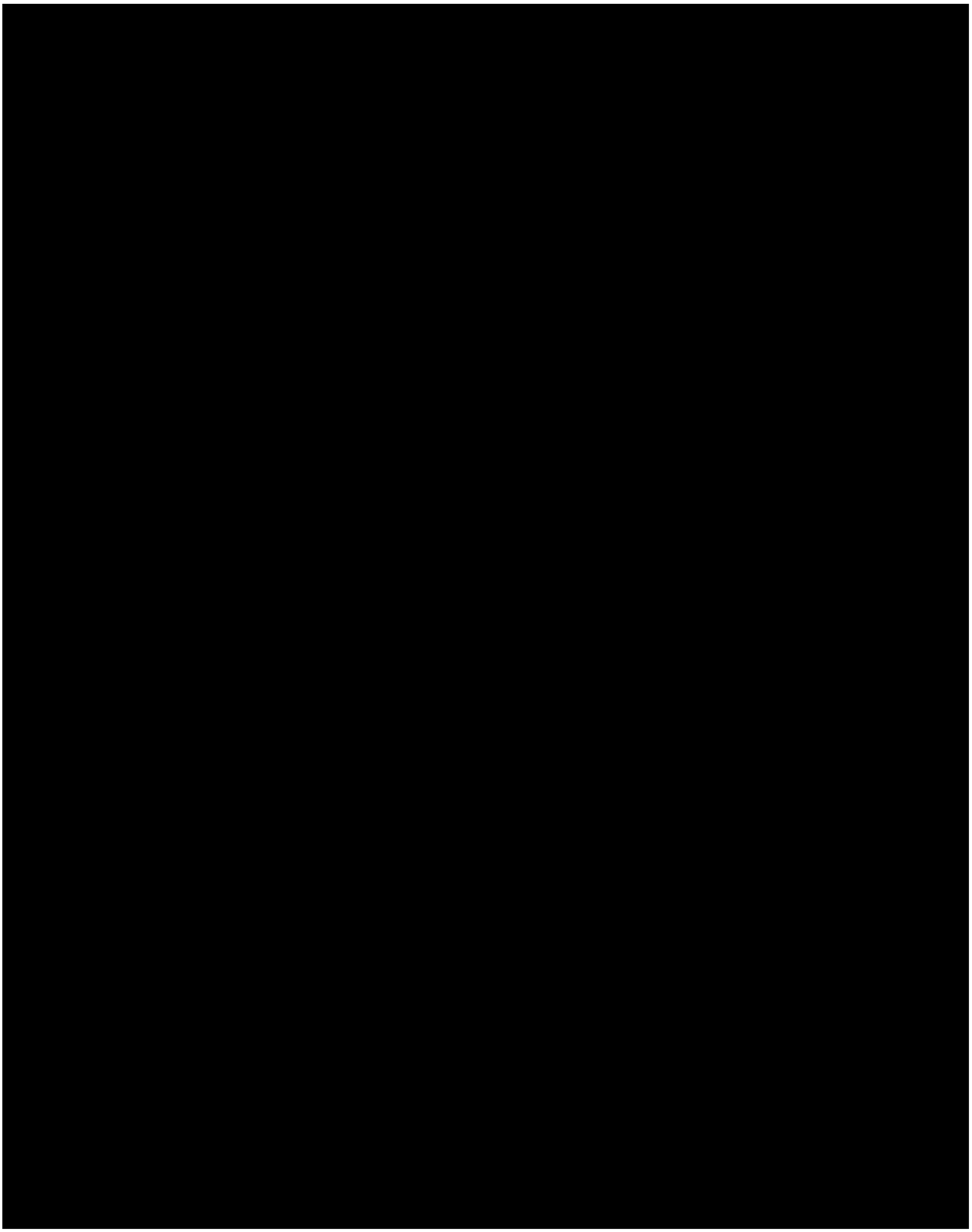

Figure 5.3-26 Directly Connected Test Unit - J1P023AM-1

5.3.16 INTEGRATED SERVICES LINE UNIT

5.3.16.1 Integrated Services Line Unit (ISLU) - J5D004AK-1 SD5D089-01

The Integrated Services Line Unit (ISLU) is a three-and-one-half shelf unit that mounts in a Line Trunk Peripheral (LTP) cabinet at Equipment Location (EQL) 63 to 36. One or two ISLUs can be mounted in an LTP and one can be mounted in the top of the Switching Module Control (SMC) cabinet if space is available. If one ISLU is required in an LTP cabinet, a plenum is mounted in the remaining half space at EQL 36. If two ISLUs are located in an LTP, the second is mounted in EQL 36 to 11 and no plenum is provided. Also with two ISLUs present, no LTP fan unit is required because each ISLU drawer contains its own fan drawer.

The ISLU provides customer interface to the switch for 2-wire analog and 2- or 4-wire digital lines. It supports coin lines with up to 1500 □ DC resistance and noncoin and PBX lines with up to 1600 □ DC. The ISLU handles both analog and digital lines simultaneously.

The ISLUs are numbered 0 and up for each Switching Module (SM). Details for adding an ISLU to an SM are given on SD-5D5012-02, Figure AS 27.

An ISLU contains a Common Shelf Unit (CSU) and from one- to four- drawer shelf units. Figure 5.3-27 illustrates a ``fully equipped'' ISLU containing four-drawer shelf units.

Each drawer unit can mount up to four Line Groups (LGs), 00 through 15. A drawer does not have to contain four LGs before other drawers can be added. A cover is supplied for any ISLU drawer position not occupied.

Each drawer shelf unit is divided into two sides, left and right, when viewed from the front. In each drawer, the first two LGs are mounted on the left side and the next two on the right side. The backplane separates the two sides. Mounted on the front of each drawer is a label identifying the LGs in the drawer. In Figure 5.3-28 , even-numbered LGs are in the lower part of the drawer and odd-numbered LGs are in the upper part.

Each LG comprises three basic areas, which are as follows:

- □ Line Cards (LCs)
- □ Line Group Common Area
- □ Connector Area.

An LG can mount up to 32 LCs (00 to 31). Whether facing the left side or right side of a drawer unit, observe that LCs are ALWAYS numbered from left to right, with LCs 00 to 15 on the lower level and 16 to 31 on the upper level. There are three kinds of LCs that can be used, and an LG can have a mix of all three. A label on the LC pull-out bar identifies each card.

When fully equipped with four LGs, a drawer has a maximum of 128 LCs, 64 on the left side and 64 on the right side. Table 5.3-4 lists the three types of LCs.

One LC is required for each subscriber.

Figure 5.3-28 illustrates the LC location layout within the Line Groups.

The Line Group Common Area consists of two types of circuit packs: the Line Group Controller (LGC), and the Line Group Power (LGP). The double-high packs are always required for each LG. Their location in the LG is illustrated in Figure 5.3-27 .

Located near the rear of each ISLU drawer unit is a connector area used to terminate the flat umbilical cables from the ISLU common shelf. The area also terminates Line Card cabling from a connector panel on the rear of the drawer shelf unit. Each drawer unit has four connector areas, one for each LG. Table 5.3-5 lists typical connector areas with jack number functions.

5.3.16.2 Integrated Services Line Unit 2 (ISLU2) - SD5D192-01

The operation of the ISLU2 is identical to ISLU and transparent with respect to the operation of the ISLU. However, for service purposes, the two units are different. The ISLU2 contains individual line circuits in packs of eight circuits a piece. Thus, at the pack level all eight lines must be installed or removed simultaneously. To work on individual circuits at the line level, the entire pack must be removed.

A simplified block diagram of the ISLU2 physical configuration is shown in Figure 5.3-29 . The ISLU2 is configured with one common shelf and one, two, three, or four line shelves. A plenum is required when only one line shelf is equipped. As a four-shelf unit, ISLU2 consists of a common shelf and three line shelves. As a five-shelf unit, ISLU2 consists of a common shelf and four line shelves.

The ISLU2 common shelf contains the Common Control Processor (CCP), Common Control Interface (CCI), and Common Data (CD) circuit packs which control the flow of data and control information between the line circuits and the rest of the SM. There are two CCP/CCI pairs which form duplex Common Control (CC) service groups which operate in active/standby mode. There are two CD service groups, with two CD packs in each service group. The CD service groups may be operated in either active/active or active/standby modes.

The ISLU2 common shelf may also be equipped with zero through four Metallic Access Network (MAN) circuit packs and zero through six High Level Service Circuits (HLSC). These circuit packs support metallic access to line circuits and subscriber lines for testing and/or sparing.

The type and number of MAN and HLSC circuit packs equipped in a unit are engineered according to the different types of lines and number of each type equipped and the amount of traffic anticipated.

In ISLU2, the line circuits are partitioned into 16 line groups, with up to 64 lines in each line group. From an exchange technician perspective, each line circuit in the unit is identified by a unique line group-line pack-line circuit designation. This designation is determined by the specific ISLU2 shelf and slot in which the line pack is plugged and the relative position of the line circuit on the line pack.

In the ISLU2 design, eight line circuits and associated power and control circuitry are implemented on each pack. All line circuits equipped on a line pack are always the same type; that is, U, T, W, or Z.

NOTE: At present, the Z interface line circuits are not supported in ISLU2.

Up to eight line packs of any type may be equipped in an LG in any combination. Since lines are equipped eight lines per pack, hardware growth/conversion must be done on an eight-line basis. Note also that although the LG control architecture will support up to 64 lines of any type, care must be taken when equipping ISDN LCs to ensure that an LG is not overloaded in terms of traffic capacity.

NOTE: Cabling has to be compatible with the pack type. If the Technician is familiar with ISLU and has been equipping the cabling for T packs, then the packs can be mixed and matched on a single ISLU, with 100 percent utilization of LCs. In ISLU2 the packs cannot be interchanged without a coordinated cabling change. ISLU2 requires that specific cabling be engineered to support ``U'' or ``T'' DSLs.

5.3.16.3 Comparing ISLU2 to (R)ISLU

The ISLU2 hardware architecture is based mainly on the hardware architecture of the existing (R)ISLU. The ISLU2 differs from ISLU in the following key areas:

- The ISLU2 can support a maximum of 1024 lines, twice as many as ISLU. The line circuits are partitioned into 16 LGs. Each LG can be equipped with up to 64 lines, as compared to the 32 lines per LG maximum for ISLU.

- In ISLU2, all line group circuitry is implemented on N-sized circuit packs that are equipped in shelves, eliminating the drawer hardware and smaller KCB and KCD packs used in ISLU. In the present design,

eight line circuits are implemented on each pack. Line Group Control (LGC) and Line Group Power (LGP) functionality is distributed across the associated line packs. There are no separate LGC and LGP packs.

- In ISLU2, the Common Data (CD) circuit packs support a modified Line Interface Data Bus (LIDB) architecture, 64 lines per LG, and distributed LGC function.
- The Common Control Processor (CCP) and Common Control Interface (CCI) circuit packs are available for ISLU2. The ISLU2 CCP has a powerful microprocessor and more RAM than the CCP for ISLU. The ISLU2 CCI also supports the new Common Control (CC) processor bus structure. It will also have an additional Control Sequencer (CS) device that will be used in implementing control capabilities for handling up to 64 lines per LG.
- The Metallic Access Network (MAN) circuit pack is available for ISLU2. The metallic access structure implemented using the MAN pack supports the following enhanced capabilities:
  - A sparing architecture that provides less degradation in ringing and metallic testing capabilities when sparing is active, as compared to ISLU.
  - Cleaner metallic test access paths containing no active components and the ability to insert or remove additional capacitance.
  - Metallic access that supports testing at Digital Subscriber Line (DSL) transmission signal frequencies.
  - The ability to metallically isolate line packs from access buses for improved fault sectionalization.

Table 5.3-4 Line Card Characteristics

CARD	T	U	Z
Circuit Pack	KCB7	KCB17 **a**	KCB6 or KCB6B
Facility Type	4-Wire DSL	2-Wire DSL	Analog
Line Format			Analog
Rate	144 kbps 64 kbps X 2 B Channels 16 kbps X 1 D Channel		
Switching Method	B Channel - Voice: Circuit Switched Only Data: Circuit or Packet Switched D Channel - Data: Packet Switched Only		Circuit Switched Only
Cable Loop Loss	6 dB @ 96 kHz	42 dB @ 40 kHz	-
Outside Plant Protection	No	Yes	Yes
Standard	TSS	*ANSI* **b**	Lucent

Notes:

a. When a KCB17 pack is mounted, the LG power pack must be A553B.

b. Registered trademark of American National Standards Institute, Inc.

Figure 5.3-27 Integrated Service Line Unit - J5D004AK-1

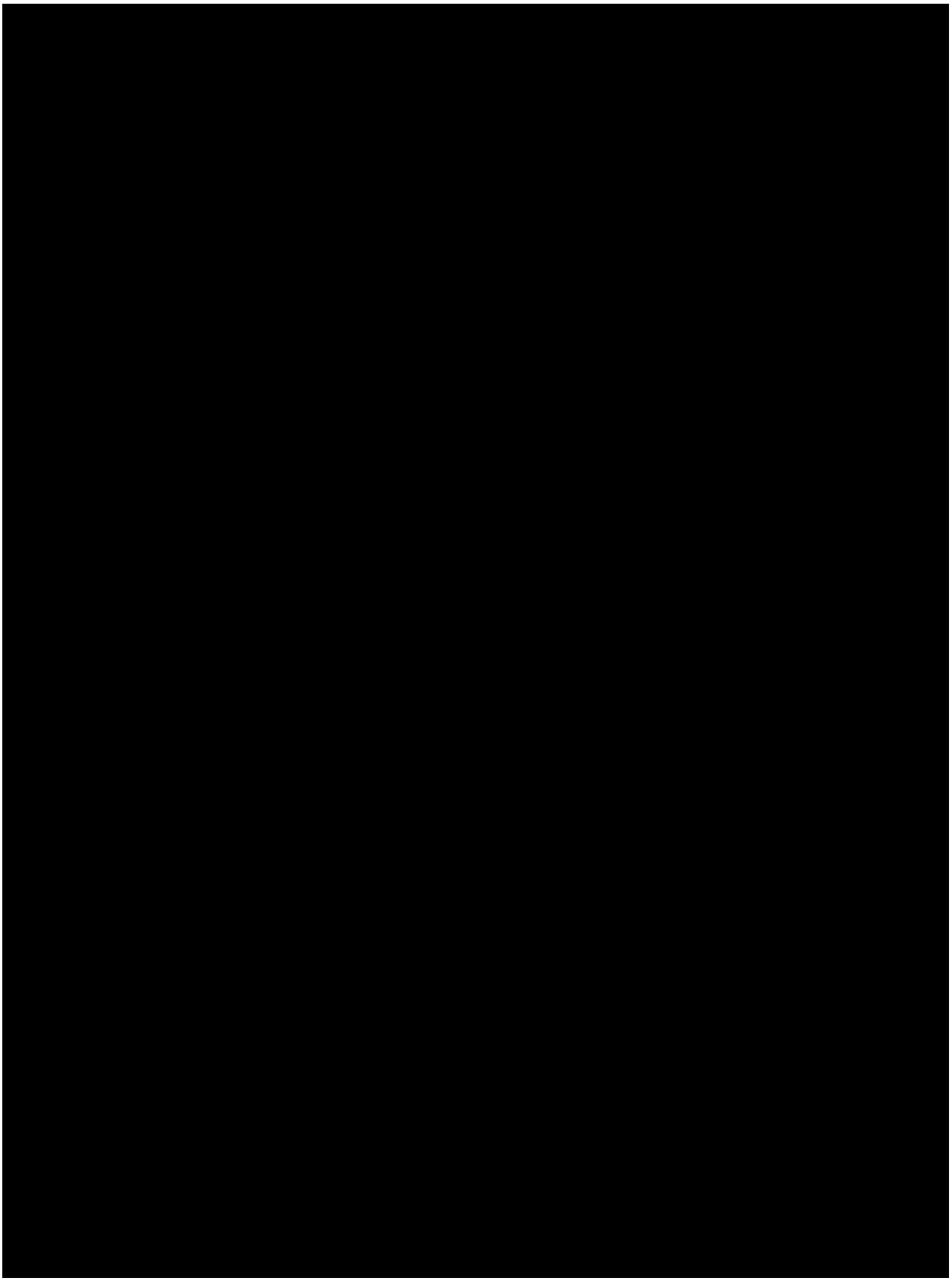

Figure 5.3-28 ISLU Line Groups 2 and 3 (Line Cards)

Table 5.3-5 ISLU Connectors

CONNECTORS	LINE CARDS	LEADS
J1 **a**	00 to 15	TIP and RING
J2 **a**	00 to 15	TIP1 and RING1
J3 **a**	16 to 31	TIP and RING
J4 **a**	16 to 31	TIP1 and RING1
J5	Metallic test bus leads, ringing leads, and spare bus leads (common shelf)	
J6	Line Interface Data Bus (LIDB) (common shelf)	
J7	Power leads and power distribution (common shelf)	
Loc 030 (Left side)	Fan unit termination	
Loc 199	Fan unit termination	

Notes:

a. Connectors J1 to J4 provide termination of the tip and ring cables for the Line Cards (LCs) to the connector panel located on the rear of the ISLU drawer.

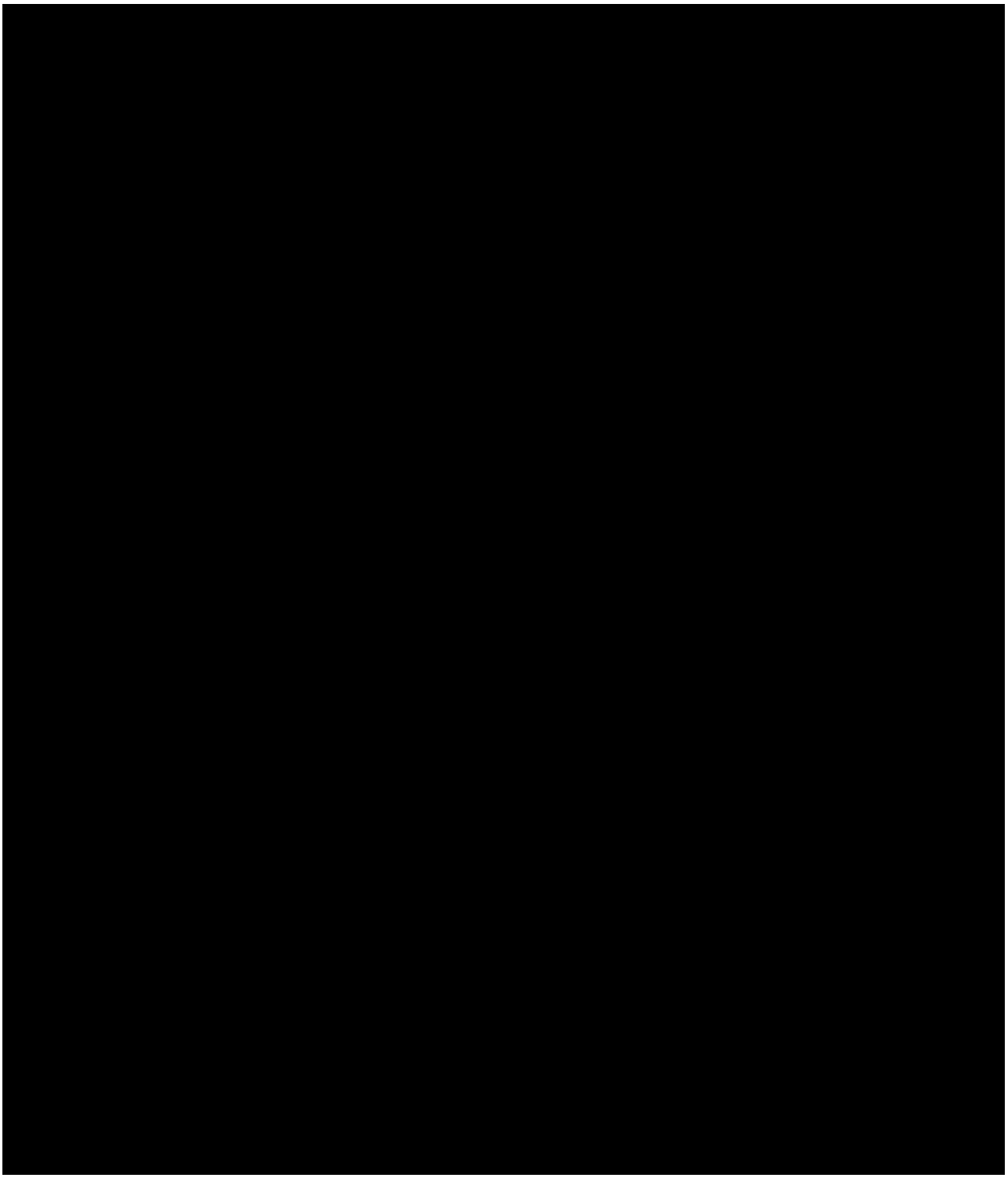

Figure 5.3-29 Integrated Service Line Unit 2 Layout

5.3.17 PARALLEL PUMP WITH CI2

The Parallel Peripheral pump for all peripherals pumped through Peripheral Interface Control Buses (PICBs) are modified to take advantage of the multicast capability offered by the Control Interface 2 (CI2) for peripherals behind the same CI2. For peripherals behind CI2 or multiple CI2s, asynchronous writes are used which allow the SMP to issue multiple CI orders to different CIs without waiting for the ASW. This allows the ASW to write a number of CI orders in the time it takes to write one currently. If these peripherals are equipped behind as few CI2s as possible, at most six CI2s are needed [for 62 Integrated Services Line

Units (ISLUs) or Remote Integrated Services Line Units (RISLUs), with 11 ISLUs or RISLUs per CI2]. Using the multicast and asynchronous Input/Output (I/O) all of these can be pumped in the time it takes to pump a single ISLU or RISLU, [approximately 14.1 seconds for ISLU(2) and 150 seconds for RISLU(2)s].

The peripheral offline pump is also modified to use multicast to improve its performance. Since multicast uses a special PICB number to perform CI operations, this should neither impact any operational actions nor cause side effects from maintenance interrupts. However, asynchronous CI operations are not used by the peripheral offline pump to avoid any side effects; for example, resulting from maintenance interrupts.

5.3.18 LINE UNITS - MODEL 2 (J5D004AC-2) AND MODEL 3 (J5D004AD-2)

Line Units 2 and 3 are two-shelf units that can be located in any available shelf location in any Line Trunk Peripheral cabinet.

The Line Unit provides an interface between customer lines and the Time Division Switching Network. Its two main functions are to provide subscriber line concentration and ``BORSCHT'' functions. The functions are defined as follows:

- **Concentration**: Refers to a relationship between subscriber terminations and time slot assignments. A fully assigned grid serves for 64 subscribers, terminated in two, half-grid circuit packs, each pack serving 32 subscribers. The total number of subscribers assigned to a Line Unit is office engineered and dependent on the number of grids equipped. Line Units 2 and 3 can terminate up to 640 subscribers.

  Table 5.3-6 illustrates the subscriber/time slot ratio.

- **BORSCHT**: service group functions contained in this coded reference are described as follows:

  B - Battery feed, including all needed DC-to-DC converters for generating required voltages.

  O - Overvoltage protection for power crosses, lightning surges, etc.

  R - Ringing, coin control and other high-level service circuit functions.

  S - Supervisory functions, such as on-hook/off-hook detection, call origination, dial pulses, ring trip, etc.

  C - CODE C or code/decode analog-to-digital and digital-to-analog conversion.

  H - Hybrid or 2-wire to 4-wire coupling and vice versa.

  T - Test access to the Metallic Test Bus (MTB).

Line Units, Models 2 and 3 are illustrated in Figures 5.3-30 and 5.3-31 . Model 2 J5D004AC-2 has subscriber to time slot ratios of 4:1, 6:1 and 8:1. Model 3 J5D004AD-2 has ratios of 4:1, 6:1, 8:1, and 10:1.

Half-grid circuit packs (such as TN1048) are selected locally to satisfy secondary protection needs. The three types that may be selected from are TN1048, TN838, and TN1058. Both TN1048 and TN838 are shown in the figures as typical.

The KTU4 (Common Control, Data, and Power Board) replaces the 4996B and UN322 that are used in LU3, while KTU6, an alternate to KTU4, provides an additional redundant 48 V power supply and acts as a single Line Unit from either feeder. This alternate circuit pack is helpful if the wrong fuse is accidentally pulled. The alternate KTU8 High Level Service Circuit (HLSC) board has the functions of three TN844s; the KTU9 has the functions of two TN844s.

Table 5.3-6 Subscriber/Time Slot Assignments

NO. SUBS.	NO. GRIDS	TIME SLOTS OUT	RATIO
256	0 to 3	64	4:1
384	0 to 5	64	6:1
512	0 to 7	64	8:1
640	0 to 9	64	10:1

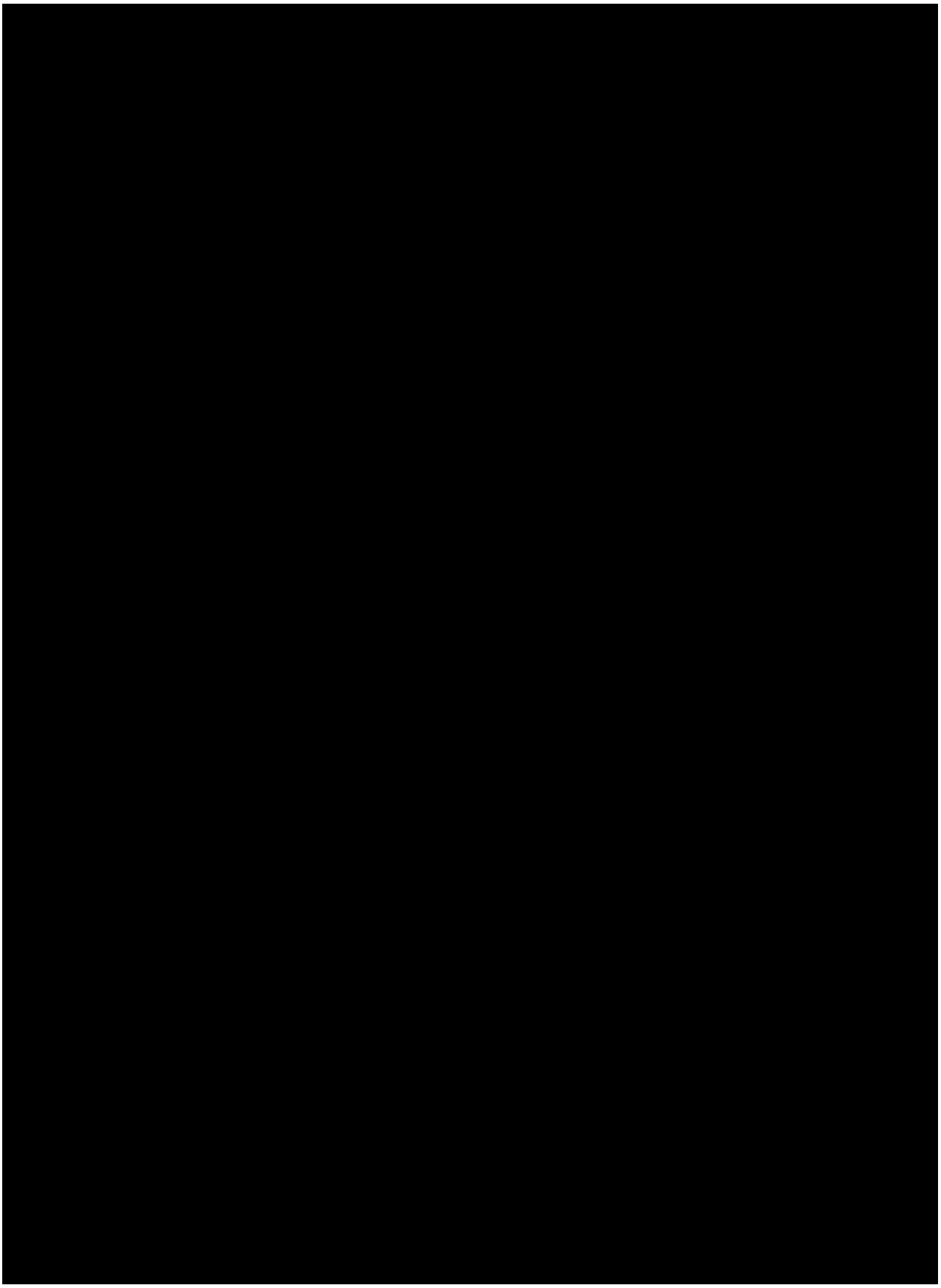

Figure 5.3-30 Line Unit Model 2 - J5D004AC-2

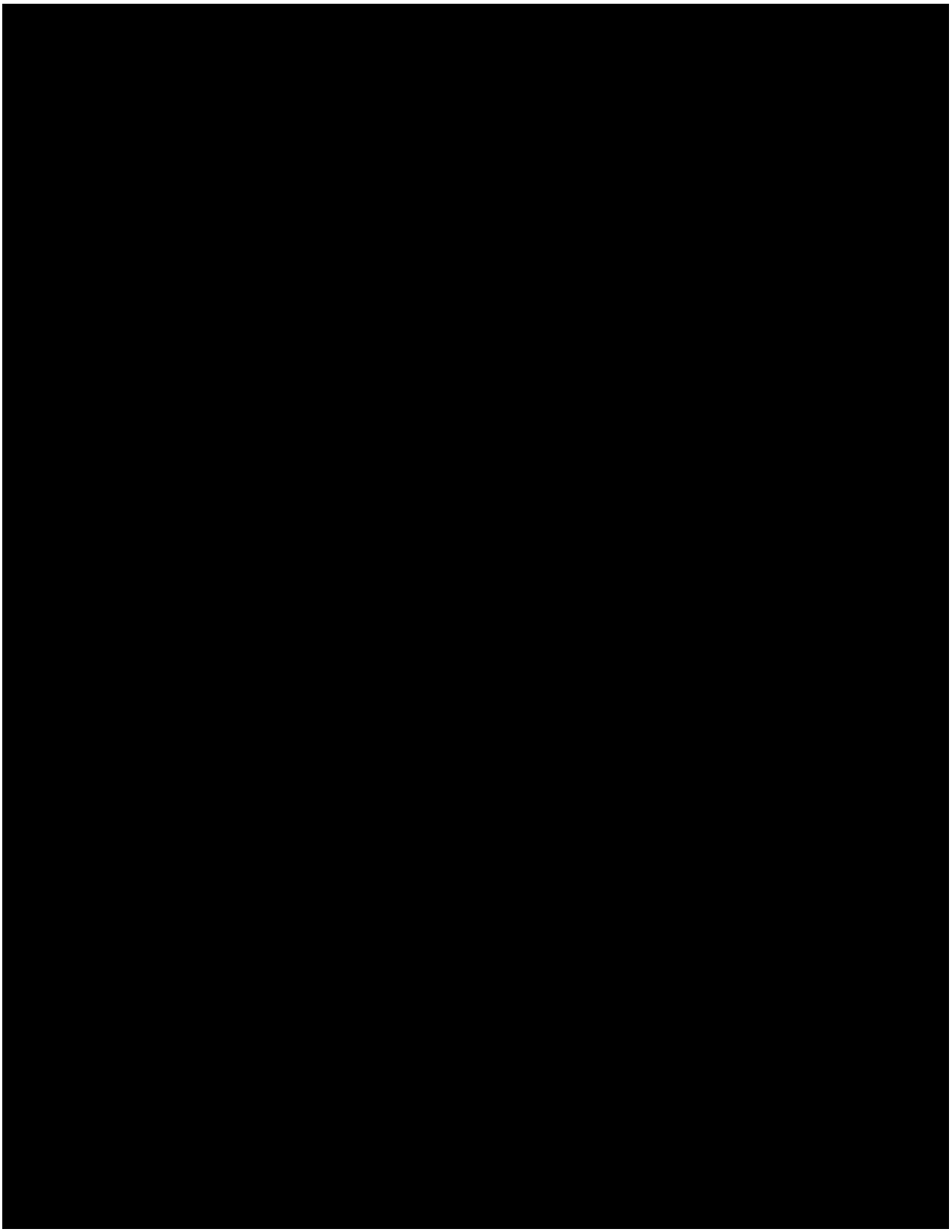

Figure 5.3-31 Line Unit Model 3 - J5D004AD-1

5.3.19 ACCESS INTERFACE UNIT

The Access Interface Unit (AIU) is a new unit that provides functionality found in Line Units and ISLUs

previously described. All common equipment is centralized on a single Common Data and Control (COMDAC) circuit pack, one for each service group. All remaining packs are Application Packs (APs). In the initial release of AIU the only application packs supported are Line Packs (LPs), Ringing Generators (RGs).

The COMDAC provides a control interface between the SMP and the application packs. In addition, the COMDAC contains a space switch providing a mapping and concentration function of the time slots from the APs onto the PIDBs. The two COMDACs normally operate in an active-active mode, where each COMDAC serves half the APs. The APs provide the interface to subscriber lines. The AIU provides an LP for the analog (Z) interface and another LP for the analog interface with 12/16 kHz PPM. The POTS Z-pack supports 32 lines with per-line Codec functionality. The PPM AP supports up to 24 lines. Each of the LPs provides a time switch allowing any line circuit to be connected to any time slot on the AP-COMDAC data bus.

The ISDN ``U'' Application Pack provides Basic Rate Access (BRA)/Basic Rate Interface (BRI) and can be provisioned with up to two 64 Kbps ``B channels'' and one 16 Kbps ``D channel.''

5.3.19.1 Application Pack

Any type of Application Pack may be equipped in any Application Pack position within the unit. Thus, the physical backplane interface is the same for each AIU Application Pack. Each type of Application Pack provides a self-ID feature that contains the pack code and serial number.

5.3.19.2 Data Interface

The data interface format is 32 time slots of 16 bits each (4.096 MHz). This interface consists of a 4.096 MHz clock signal, a Frame sync, data up (towards the COMDAC), and data down (towards the Application Pack). Each Application Pack slot has its own data interface.

The Application Packs contain elastic stores (or their equivalent) to send and receive data to and from either COMDAC (both operating at the same frequency, but possibly at different phases) on any of the 32 time slots.

5.3.19.3 Control Interface

The control interface for the Application Packs is through a 256K bit Universal Asynchronous Receiver Transmitter (UART). The interface between the Application Pack and each COMDAC consists of the following signals:

- Clock
- Sync
- Data up (toward the COMDAC)
- Data down (toward the Application Pack)
- Control up (toward the COMDAC)
- Control down (toward the Application Pack)
- Select
- Reset

Application Packs have the capability to loop back any time slot for test purposes.

5.3.19.4 Ringing

The POTS analog line AP has two ringing inputs, selected by a register bit written through a UART message. Ring trip is per line.

NOTE: AIU does not support multiparty ringing or multiparty lines. The reason the AIU does not support multiparty lines is due to the way the ringing bus is designed.

5.3.19.5 Metallic Test

Application Packs have access to only one Metallic Test Bus (MTB). Each COMDAC has an incoming MTB, but only one will connect its MTB to the internal general purpose bus. The POTS Line Pack hardware design supports both test in and test out, which can be provided simultaneously with two general purpose buses for use in the *SLC*®-2000 application.

If the R/EAIU is beyond metallic testing range (3000 ohms), or no metallic pair is available to test, an AP for the remote site should be considered. The AIU can be equipped with an Application Test Pack that performs SLIM-2 like test functions. It is controlled from the Remote Common Data and Control (RCOMDAC) and provides integrated testing with the rest of the *5ESS*® switch. A Test Application Pack can provide testing capability for up to eight RAIUs at the same logical remote site (the logical remote site is defined in the ODD). Only one Test Application Pack may be equipped per logical remote site. Multiple logical remote sites may be physically colocated. If a test pack is not equipped, external test equipment may also be considered.

5.3.19.6 POTS

The Analog Line Packs provide a tip and ring interface to analog subscriber lines, which includes the BORSCHT functions. The BORSCHT functions provided by the line circuits are battery feed, overvoltage protection, ringing access and ring trip, supervision, CODEC [Analog to Digital (A-to-D) and Digital to Analog (D-to-A) conversion], hybrid (4-wire to 2-wire conversion), and loop testing access.

The Z Line Packs (POTS) support 32 subscriber line interface circuits per pack. If ISDN customers are supported, D channel access and B channel support must be provisioned before other customers will have access.

5.3.19.7 PPM

In addition to the POTS analog interface, special Line Packs to support 12 kHz and 16 kHz Periodic Pulse Metering (PPM) are provided. These packs generate the PPM tones, provide the capability to diagnose the PPM hardware, and support the same BORSCHT functions as the POTS lines.

Coin packs terminate up to 16 analog coin or POTS customers. If more than one coin pack is equipped, balancing the coin packs between odd and even pack positions is recommended. This will equalize path hunting between major and minor RCOMDAC circuit packs.

Figure 5.3-32 illustrates the location of the Access Interface Unit in the Switching Module Control cabinet and the respective circuit packs in the unit.

5.3.19.8 Power

Each AIU circuit pack converts -48 volts to +5 volts (or other required voltages) locally.

Each AIU circuit pack has a surface mount (nonfield replaceable) fuse on its incoming -48 volts. This fuse is not intended to replace the fuse/filter unit, but only to prevent flame and smoke in case of a component failure on the circuit pack.

AIU uses the standard *5ESS*® switch Fuse/Filter Unit (FFU) to distribute -48 volts.

Figure 5.3-32 Access Interface Unit

5.3.20 ASYMMETRIC DIGITAL SUBSCRIBER LINE (ADSL)

5.3.20.1 Basic Description

Asymmetric Digital Subscriber Line (ADSL) provides combined broadband data and narrowband telephony service for subscribers on the *5ESS*® switch by using the *ANSI* standard T1.413 ADSL specification. This technique puts the broadband data on the same subscriber loop through the use of Discrete MultiTone (DMT) modulation at frequencies above 4 kHz. Splitters at both ends of the loop separate the narrowband and broadband signals. The broadband data is carried in the form of ATM cells on Permanent Virtual Circuits (PVCs).

5.3.20.2 Configuration

The AIU cabinet has space for six shelves, three in the front and three in the back. The configuration chosen for ADSL has two OEM ADSL shelves and one Lucent POTS shelf in the front of the cabinet, and three OEM ADSL shelves in the back. The ADSL shelf has 18 slots for Line Cards, but only 16 are used. Two slots are left empty. The OEM shelf provides terminations for alarms (six outputs and two inputs), but these are not used. All alarm information is transported through the Element Manager.

The top shelf is identical to the middle shelf with respect to the circuit pack configurations. It should be

noted that the ADSL unit is dedicated to the ADSL application described. This means that it cannot be converted to a full AIU (non-ADSL) application by only changing out the AP types. The tip/ring cabling to the MDF is different between the types of units and is not easily interchangeable. A cabling harness, connected between the MDF cable and circuit packs, is also required in the ADSL application.

5.3.21 EXPANSION ACCESS INTERFACE UNIT □ (EAIU)

5.3.21.1 General

The Expansion Access Interface Unit (EAIU) is similar to the AIU except it can be colocated with the Host SM/SM-2000, ORM/EXM2000, or it can be remotely located by itself. The distance between the EAIU and the SM-2000 can be up to 300 miles. The actual distance will vary depending on the transmission equipment used for remoting.

5.3.21.2 Detailed Description

The EAIU has the same major components as the AIU, except it uses a Remote Common Data and Control (RCOMDAC DAC624) circuit pack.

The EAIU performs its function by multiplexing the DS1 signals from the RCOMDAC pair into the Synchronous Transport Signal Level 1 (STS1) signal. Testing capabilities are provided through connection to the MTB.

5.3.21.2.1 Components for EAIU

RCOMDAC EAIU □ The RCOMDAC provides a DS1 signal over the T1 facilities that is multiplexed into an STS1 signal. Each RCOMDAC can have up to 6 T1 facilities (12 T1s per EAIU). The STS1 from the T1 facility is terminated to a Digital Network Unit- Synchronous Optical Network (SONET) (DNU-S) associated with the SM-2000.

Subscriber Lines □ The APs provide the interface for analog and ISDN subscriber lines and ringing generators. Any type of AP can be installed in any AP slot to provide a flexible mixture of analog and ISDN lines, if necessary. This arrangement also makes it easy for subscribers to migrate from an analog to an ISDN line. Each type of Application Pack will provide a self-ID feature that will contain the pack code and serial number.

The types of APs used in the AIU or the EAIU area:

- LPZ100: Provides Plain Old Telephone Service (POTS) Z interface for up to 32 analog subscriber lines.
- LPC100: Provides coin phone or POTS interface for up to 16 analog subscriber lines.
- LPU116: Provides ISDN American National Standards Institute (ANSI) U interface for up to 16 digital subscriber lines.
- RGP100: Provides ringing generation for analog subscriber lines. Two packs service up to three AIUs.
- TAP100: Provides integrated metallic testing (that is, SLIM functionality) at remote sites (EAIU) more than 3000 ohms from the Modular Metallic Service Unit (MMSU).

5.3.21.3 Functional Description

The Access Interface Unit (AIU) and Expansion Access Interface Unit (EAIU) consists of two types of circuit packs:

- Common Data and Control (COMDAC) □ provides common control functions and the interface to the

switch.

- Application Packs provide the interface to the subscriber lines. The interface to the subscriber lines can be provided by using the appropriate Application Pack. The Application Packs differ for digital, analog, or coin.

The COMDAC an various combinations of Application Packs are combined to provide local customers interface to the *5ESS*® switch switching module for analog and 2-wire ISDN lines. The AIU terminates up to 640 analog lines or 320 two-wire ISDN lines. It concentrates these lines based on the customer traffic load, the method of engineering, and the engineered blocking factors that have been applied.

In addition to terminating lines and providing line concentration, the unit performs origination scanning, BORSCHT functions [battery feed, overvoltage protection, ringing, supervisory functions, analog/digital (CODEC) conversion, 2-wire to 4-wire conversion (hybrid]), test access], and accepts voice and data connections simultaneously over the same telephone lines.

Each of the Line Packs provide a time switch allowing any line circuit to be connected to any time slot on the Application Pack-COMDAC to connect the data bus to on a per time slot basis.

5.3.21.3.1 RCOMDAC Circuit

The RCOMDAC (DAC624) circuit pack provides a Digital Signal Level 1 (DS1) between the AIU and the switch. Each RCOMDAC circuit provides up to 6 duplicated DS1 signals, therefore a RCOMDAC pair (DAC624 0 and 1) will provide up to 12 DS1 signals per EAIU. The DS1 signals, up to 28, are multiplexed into an STS1 signal. The STS1 signal is terminated on a Digital Network Unit-SONET (DNU-S). The DNU-S provides a Peripheral Control and Timing link interface to SM-2000 Module Controller/Time Slot Interchanger (MCTSI). The EAIU control channel is bundled with 23 other data channels to make up the 24 channel DS1-0 signal. The PCT link delivers the DS1 signal to the TSI link and the TSI. At the TSI, the control channel is routed to the Message Handler 1(MH1) where the control information is formatted into a pseudeo-PICB and routed to the Switching Module Processor (SMP).

5.3.21.3.2 Application Packs

The line Application Packs are common to the AIU and the EAIU.

The following functionality is common to all Application Packs providing line terminations.

The data interface format for Application Packs consists of 32 time slots of 16 bits each. The interface between the Application Packs and the COMDAC consist of the following signals:

- PCM Clock
- PCM Synchronization
- PCM Data (AP up/down to COMDAC)
- AP Control (AP up/down to COMDAC)
- AP Select
- AP Reset.

The SM selects the time slot to be used and then sets up the COMDAC and the Application Packs. The COMDAC concentrator connects a given time slot from any Application Pack to the same time slot on any of the Time Slot Groups (TSGRPs). The Application Packs can connect any incoming line to any of the 32 time slots.

Application Packs have one red LED located on the faceplate. This red LED is used as a diagnostic tool to annunciate various conditions of self-test, such as reset, power-up, and software control. A constantly lit LED (no flashing) means a fault condition exists with the pack.

5.3.21.4 Configuration

The Access Interface Unit (AIU) is a simplex unit made up of two service groups. Each service group has a Common Data and Control (COMDAC) pack.

The AIU is engineered for a line concentration ratio of anywhere from 2:1 to 10:1.

The COMDAC packs operate in active-active mode to share the call load.

The even-numbered Application Packs are assigned to COMDAC 0 and the odd-numbered Application Packs are assigned to COMDAC 1. However, each Application Pack has access to both COMDACs should one COMDAC become overloaded or go out of service.

Should one COMDAC go out of service, the line concentration ratio would double.

5.3.21.5 Shelf and Pack Layout

AIUs/EAIUs are housed in a dedicated Line Trunk Peripheral (LTP) cabinet. No other units are installed in a cabinet housing AIUs/EAIUs. AIUs/EAIUs are installed in standard building blocks of two or three, mounted one above the other. One AIU/EAIU building block fits into a standard LTP cabinet. Two AIU/EAIU blocks fit into a Front Access Cabling (FAC) cabinet, one facing the equipment aisle and one facing the wiring aisle.

5.3.22 MULTIPLEX ACCESS INTERFACE UNIT (XAIU)

The XAIU has the functionality of the AIU in the SM-2000, but it is capable of being used as a local AIU only. Thus, any of the remote applications (such as EAIU or RAIU) are not supported with the XAIU. The XAIU supports the same application packs as are already defined for the AIU. The key feature of the XAIU is that it drastically reduces the AIU installation time by eliminating the installation associated with the Peripheral Interface Control Buses (PICBs) and Peripheral Interface Data Buses (PIDBs). The XAIU replaces all the PIDB/PICB cables to an entire cabinet with two fiber optic pairs, or Peripheral Control and Timing (PCT) links. Because of the PCT links, the XAIU can be located up to 2000 cable feet from the SM-2000 as opposed to 28 cable feet with the PIDB/PICB links.

The hardware components associated with the XAIU feature are:

- PCT Data Exchanger Unit (PDXU)
- XAIU.

The PDXU consists of two PCT Data Exchanger (PCTDX) circuits, each containing one Peripheral Link Interface (PLI) paddle board, a PCT fiber pair, and one Fiber Common Data (FCD) circuit pack. The FCD pack terminates the PCT fiber optic links and distributes data to the XAIU shelves in the cabinet.

The XAIU is an AIU which resides in an XAIU cabinet. It uses a Quad PIDB COMDAC (QCOMDAC) which provides the interface and control between the FCD and the application circuit packs. The QCOMDAC is functionally similar to the RCOMDAC, except that the QCOMDAC does not have the capability to terminate E1/DS1 facilities.

The XAIU cabinet differs from the local AIU and EAIU cabinets in that it has two FCD packs in the lower rear of the cabinet. The FCD packs are contained in a housing which is part of the PDXU. This unit supports two fiber pairs per cabinet, with each fiber pair carrying either a full PCT link or one-half PCT link. A full PCT link consists of 768 time slots or 24 Time Slot Groups (TSGRPs) at 32 time slots per group, and

one-half PCT link has 384 time slots or 12 TSGRPs at 32 time slots per group.

The following basic cabinet configurations are available:

- A low traffic configuration with two one-half PCT PDXUs serving up to six XAIUs in the cabinet. Each XAIU in the cabinet may have up to two TSGRP pairs.
- A high traffic configuration with two full PCT PDXUs serving up to four XAIUs in the cabinet. Each XAIU in the cabinet may have up to six TSGRP pairs.

5.3.23 MEMORY EXPANSION UNIT - J5D003BH-1

The Memory Expansion Unit (MEU) is a single-shelf unit which MUST be mounted in the Switching Module Control (SMC) cabinet, shelf 1. The unit is divided into two Module Controller Time Slot Interchange (MCTSI) controllers, 0 and 1, with 0 to the left and 1 to the right.

The main function of the MEU is to expand the memory area of the Module Controller and Time Slot Interchanger (TSI) Unit (MCTU). Addition of the MEU increases the maximum MCTU memory capacity from 10 to 16 MB. Since the SMP12 or SMP23 units can be equipped with either 2-MB (TN56) or 4-MB (TN2012) memory boards, the MEU increases the maximum MCTU memory capacity to 24 MB (12 x 2 MB) (TN56s) or 32 MB (12 x 4 MB - but limited to a maximum addressability of 32 MB) (TN2012).

The type and number of memory circuit packs (TN56 or TN2012) depends on the processor in the MCTU. The memory packs in the MEU must be the same as the memory boards in the MCTU. The MEU is only valid on MCTUs that support SMP12 or SMP23 Module Processors. The MEU is not supported on MCTUs with SMP23CDM Module Processors.

Figure 5.3-33 illustrates the location of the Memory Expansion Unit in the Switching Module Control cabinet and the respective circuit packs in the unit.

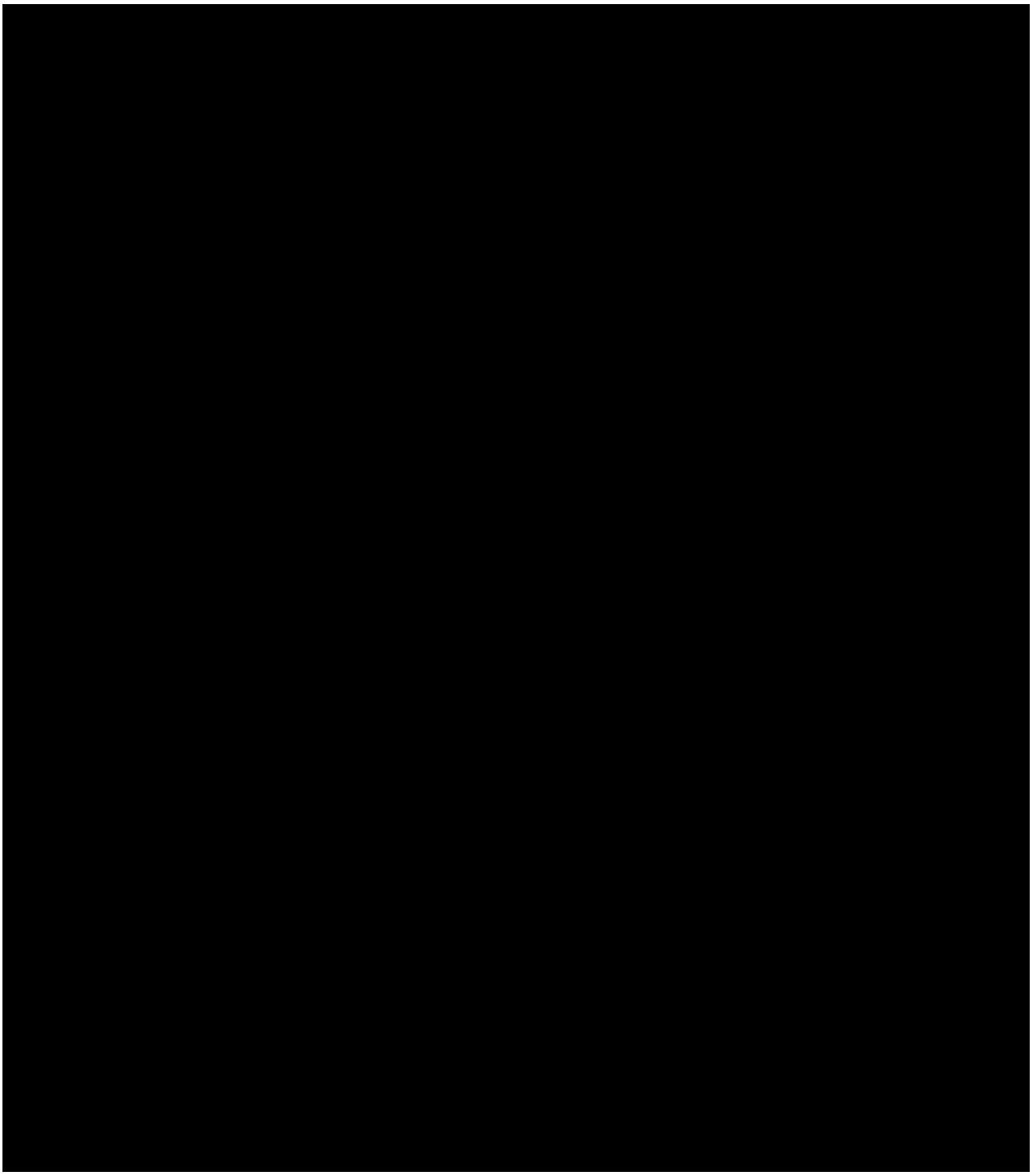

Figure 5.3-33 Memory Expansion Unit - J5D003BH-1

5.3.24 SMP23 WITH CORE DRAM

The SMP23CDM core board (TN1423) can be used in SMP23 or SMP12 units to replace the TN1407(B) or TN1397 microprocessor core boards, respectively. The TN1423 provides 32 MB of DRAM on the microprocessor core board, which removes the need of using an MEU shelf and extra memory boards to reach maximum equipage. Although the SMP23CDM core board is capable of addressing up to 128 MB, the bootstrapper board and the size of the update bus currently limit duplex operation of the MCTSI to 32 MB.

The SMP23CDMX is an extension of the SMP23CDM Module Processor. The conversion of a SMP23CDM to a SMP23CDMX involves adding an Update Bus Cable, a new bootstrapper board, the code to support it, and possibly changing the memory controller boards. The SMP23CDMX was introduced as part of the 5E12(1) software release. The SMP23CDMX supports 32 MB of DRAM on the microprocessor core board and up to five 4-MB TN2012s on the MCTU shelf. This means that the maximum memory equipage of a SMP23CDMX is 52 MB [32 MB DRAM + (5 x 4 MB)]. Table 5.3-7 shows the configuration of the component boards.

Table 5.3-7 SMP23 Components

FUNCTION	SMP23CDM	SMP23CDMX
Microprocessor Core Board	TN1423(B)	TN1423(B)
Communications Boards	TN1617/TN872	TN1617/TN872
Processor Core Support Board	TN1533	TN1533
RAM/ROM Board	TN874B	TN874B
Bootstrapper Board [a]	TN878	TN1418
Memory Controller Board	TN1408(B)/TN1527	TN1408(B)
Noncore Board Memory Board	NONE	TN2012

Notes:

a. The TN878 can only be used for applications requiring 32 MB or less of memory.

5.3.25 MODULE CONTROLLER TIME SLOT INTERCHANGER UNITS

5.3.25.1 Module Controller Time Slot Interchanger - J5D003EC-1

The Module Controller Time Slot Interchanger Unit (MCTU) is a two-shelf unit fixed located on shelf 2 and 3 of the Switching Module Control cabinet. It is divided into two sections with controller 0 at the left and controller 1 at the right. The controllers operate in an active/standby mode with circuit packs duplicated in the two controllers. All circuit packs in Module Controller 0 are duplicated in Module Controller 1 except the bootstrapper pack (TN878 or TN1418).

The MCTU does the following:

- Provides interfaces with Network Control and Timing (NCT) links.
- Provides an interface with the intra-switching module to transmit control information from the Switching Module Processor.
- Provides an interface with the intra-switching module for Pulse-Code Modulation (PCM) data.
- Provides call processing, call supervision, and maintenance functions.
- Provides Switching Module Processor controlled time-division switching.
- Provides an interface between the Switching Module Processor and the Network Control Timing links message time slots.
- Preprocesses signaling and control bits of time-slot data and provides Switching Module Processor access to the bits.

The TN874B Module Processor pack is software-release sensitive.

Figure 5.3-34 illustrates the location of the Module Controller Time Slot Interchanger Unit and the respective circuit packs in the unit.

Figure 5.3-34 Module Controller Time Slot Interchanger - J5D003EC-1

5.3.25.2 Module Controller Time Slot Interchanger - Model 2 - J5D003LA-1

The Module Controller Time Slot Interchanger Model 2 (MCTU2) is a two-shelf unit fixed located on shelves 1 and 2 of the Switching Module Control cabinet. It is divided into two sections with controller 0 at the bottom and controller 1 at the top. The controllers operate in an active/standby mode with circuit packs duplicated in the two controllers. All circuit packs in Module Controller 0 are duplicated in Module Controller 1.

The TN833 circuit pack located at EQL 168 handles the Local Digital Service Unit functions. This eliminates a need for 003EAI DSU2 serving local functions for a DSU2 shelf.

The MCTU2 does the following:

- Interfaces with Network Control and Timing Links.
- Sends/receives control orders from the peripheral units in the SM, using the PICB information from the Switching Module Processor.
- Sends/receives pulse-code modulation data from the peripheral unit in the SM, using the PICB.
- Preprocesses signaling and control bits of time-slot data and provides Switching Module Processor access to the bits. Memory unit assignments are sensitive toward software releases.
- Provides interface with the PSU.

Figure 5.3-35 illustrates the location of the Module Controller Time Slot Interchanger - Model 2 and the respective circuit packs in the unit.

Figure 5.3-35 Module Controller and Time Slot Interchanger - Model 2 - J5D003LA-1

5.3.25.3 Module Controller and Time Slot Interchanger - Model 3 - J5D003LB-1

The Modular Controller and Time Slot Interchange Unit, Model 3 (MCTU3) combines several circuit packs into one and reduces the MCTU2 from two shelves to one. The MCTU3 will require a new shelf/backplane, a new core board (SB20CORE), and a new combined power control and display pack. The existing TSIU3 together with the DIs, CIs, or the new CI2s and peripherals will be used. All SM configurations including Local Switching Module (LSM), RSM, ORM for *5ESS*® switch, and *5ESS*® switch CDX will be supported. The MCTU3 feature is particularly beneficial to the *5ESS*® switch VCDX because the SB20CORE board contains most of the hardware to support the Ethernet interface. A paddleboard located on the backplane of the MCTU3 will provide the physical interface to the Ethernet interface and handles the CPI message interface between the workstation and the SB20CORE.

The functionality of the MCTU3 is identical to MCTU2 with customer benefits listed below:

- The MCTU3 provides more than a 10 percent increase in SM Processor capacity without the need of a Data Cache (UN520 as required by MCTU2).
- MCTU3 consumes 50 percent less power than MCTU2.
- MCTU3's predicted reliability is 35 percent better than MCTU2.
- The reduction in circuit pack codes means that fewer codes need to be spared.

- MCTU3 fits in one shelf; MCTU2 requires two shelves.

Figure 5.3-36 illustrates the location of the Module Controller and Time Slot Interchanger - Model 3.

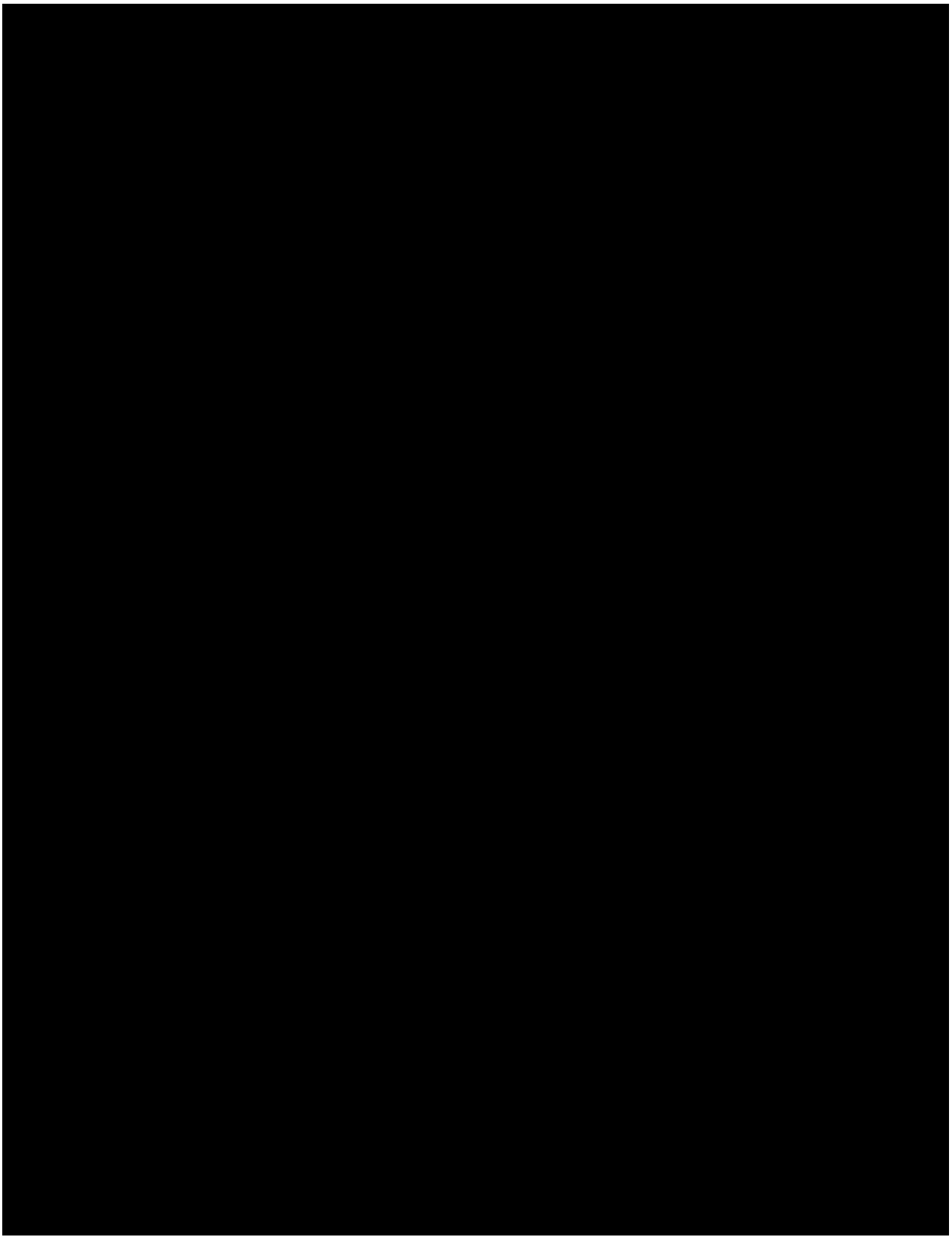

Figure 5.3-36 Module Controller and Time Slot Interchanger - Model 3 - J5D003LB-1

5.3.26 MODULAR METALLIC SERVICE UNIT - J5D003BD-1

The Modular Metallic Service Unit (MMSU) is a one- to four-shelf unit that can be located in shelf positions one through six in a Line Trunk Peripheral (LTP) cabinet. Put the basic MMSU in shelf space one to three, with supplemental units (up to 03) mounted above in ascending order. The MMSU may also be mounted in any available vacant location in the Switching Module Control cabinets.

Each unit is divided into two duplicate service groups, SG0 and SG1. Each shelf requires two power units (494LA) at locations 010 and 098, respectively. Only the basic shelf requires common packs TN879B at positions 018 and 106.

Each service group can mount up to 32 service packs (SG0 - EQL 026 to 081 and SG1 - EQL 114 to 170). The type of pack in each position varies from office to office.

One of the main functions of the MSSU is to establish a metallic test path through the office, thereby connecting lines or trunks to test positions and designated test equipment.

When a TN138 pack is mounted in SG0 (at 026, 034 and 042) and SG1 (at 114, 122 and 130), an additional TN138 pack is required at 090 and 178. When there are no TN138 packs in a service group, position 090 contains a ground shield.

Circuit packs assigned to Automatic Line Insulation Tests are selected to accommodate local area humidity conditions. The packs available are TN328B, TN329B, and TN330B. The packs are located at EQL 050 and 138.

A SLIM2 board (TN1422) is an optional board to insert in the MMSU. The SLIM2 performs measurements on analog and digital subscriber lines as well as analog trunks. It will measure the metallic characteristics of the line/trunk such as voltages, insulation resistances, and capacitances. SLIM2 can be operated in both Operator Mode (TLWS 5700 page, similar to the DCTU page) and Routine Mode (recent change driven, similar to the ALIT).

Figure 5.3-37 illustrates an example location of the SLIM2 board in the Modular Metallic Service Unit area of the Line Trunk Peripheral cabinet and location of the respective circuit packs in the unit. The MMSUs and associated growth units are engineered to specific office requirements; therefore, the configurations are typical and nonrestrictive.

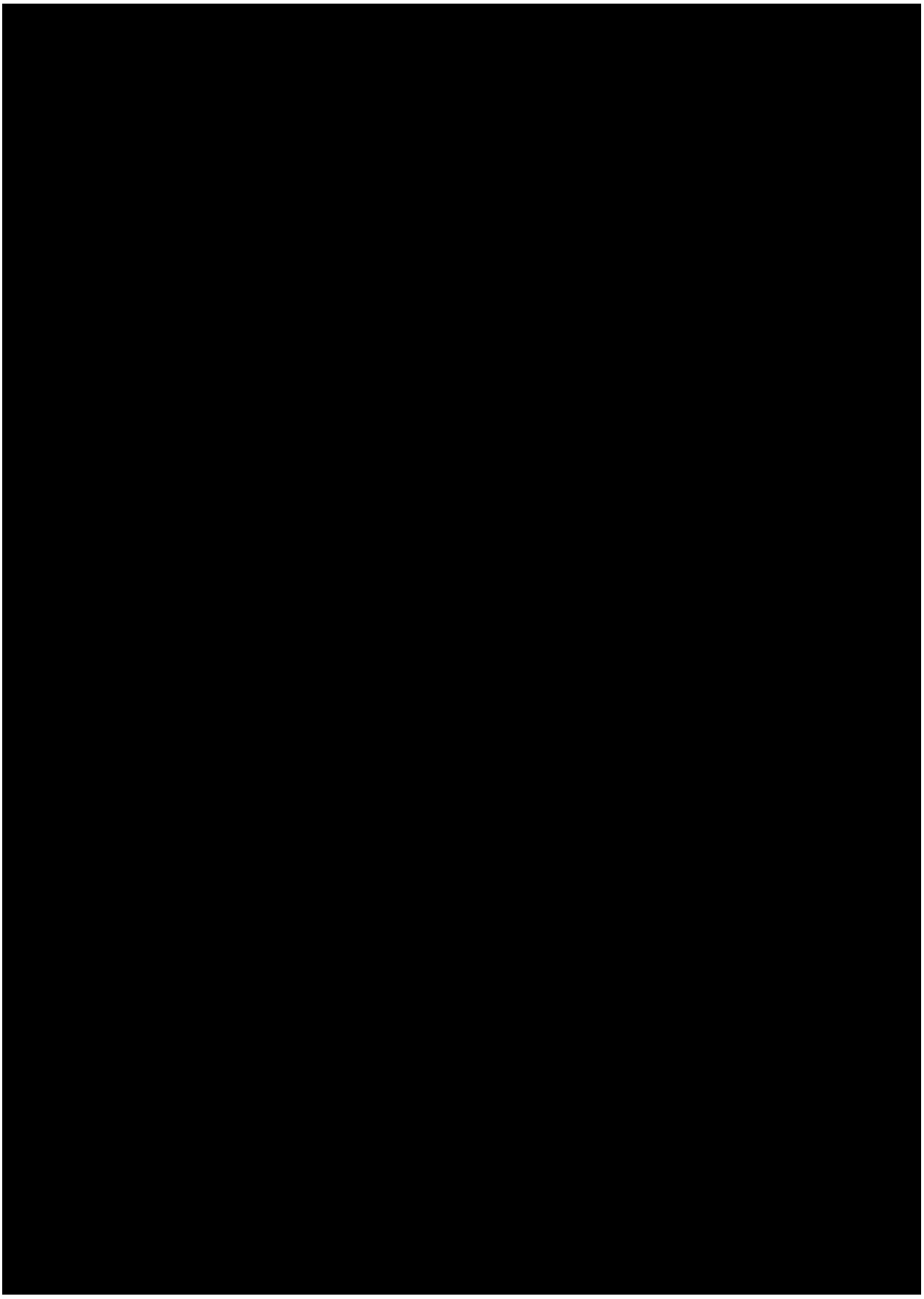

Figure 5.3-37 Modular Metallic Service Unit - J5D003BD-1

5.3.27 PACKET SWITCH UNIT - J5D003BL-1

The Packet Switch Unit (PSU) is made of one to five shelf units mounted in any Line Trunk Peripheral (LTP) cabinet. The PSUs can also be mounted in Switching Module Control (SMC) cabinets but only in shelves three and four when the space is available.

The primary function of the PSU is to provide processing to support packet signal messages, Operator Services Position System (OSPS) operator data messages, and packet data switching.

The basic PSU (0) is always required in an SM containing an Integrated Service Line Unit (ISLU) that services digital subscribers. The basic PSU is also required for SMs that mount a Digital Line Trunk Unit (DLTU) connected to T1 lines that handle Integrated Services Data Network (ISDN) traffic (primary rate users).

The assignment of protocol handler circuit packs (up to 16) is software-release sensitive. The protocol handler communicates over the packet bus to the SMP and to other protocol handlers and provides a local environment to support distributed processing.

The basic PSU can support four additional growth units. The growth units are mounted above the basic unit in ascending numerical order from 01 through 04. The number of PSU shelves for an office is determined by the number of digital subscribers present. Only one PSU can mount in an SM.

Figure 5.3-38 illustrates the location of the PSU.

Table 5.3-8 identifies the respective circuit packs in the PSU.

NOTE: If an SM requires a PSU, either a PSU or Packet Switch Unit Model 2 (PSU2) can be used. If an SM-2000 requires a PSU, only a PSU2 can be used.

A second PSU2 unit can physically support up to a combination of 80 Protocol Handler 4's (PH4s), Protocol Handlers for Voice (PHVs), PH22, PHV4, PHV5, and spares. However, time slot engineering may limit specific configurations to less than 80. Refer to 235-200-100, *5ESS® Switch FLEXENT™/AUTOPLEX® Wireless Networks Applications OA&M Manual*, for additional information on the PSU2 units.

Figure 5.3-38 Packet Switch Unit - J5D003BL-1

Table 5.3-8 PACKET SWITCH UNIT CIRCUIT PACKS

PSU TYPE	PROTOCOL HANDLER CIRCUIT PACKS
PSU	TN1366, TN1367, TN1081
PSU2	TN1844,TN1856, TN1862, TN1845, TN1367C, TN1867, TN1846
PSU TYPE	**FANOUT CIRCUIT PACKS**
PSU1	Control Fanout TN1082/MC5D102A1, TN1082B/MC5D102A1B, TN1082B/MC5D123A1B
PSU2	TN1843, UN399, UN348B, UN348/MC5X701A1, UN592

5.3.28 SS7-PSU ON SM/EXM-2000

The introduction of SM-based SS7 (Signaling System 7) signaling on the SM-2000/ EXM-2000 allows basic subscriber features and services that require SS7 signaling to continue intra-module operation in the event the SM-2000/EXM-2000 loses communication with the host and goes into stand-alone operation (if provisioned for stand-alone). The SM-based SS7 signaling platform is provided by the addition of an SS7 Packet Switch Unit (PSU) to the switching module. For switching modules like the SM-2000 and EXM-2000, an SS7 PSU can be added and SS7 signaling links terminated to it to provide stand-alone processing if desired.

This feature consists of the following core elements:

(1) It provides the SM-based SS7 Message Transfer Part (MTP) and Signaling Connection Control Part (SCCP) signaling platform (SS7-PSU) on the SM, RSM ORM (Optically Integrated Remote Switching Module), and (local) SM-2000 and EXM-2000 switching modules in the *5ESS*® switch.

(2) It allows both the (AM-based) Common Network Interface (CNI) and (SM-based) SS7-PSU signaling

platforms to co-exist in the same host office.

Those switching modules equipped with an SS7 PSU and terminating SS7 signaling links are designated as Global Switching Modules (GSMs). All SS7 signaling on the GSM is handled by its SS7 PSU. In this phase of bringing SM-based signaling to the *5ESS*® switch, the SS7 PSU supports only trunk groups terminated on the GSM. In essence, the GSM emulates a single SM office, and up to 16 GSMs are supported per *5ESS*® switch.

The SM-based SS7 signaling is necessary for Very Compact Digital Exchange (VCDX) offices since CNI, AM, and CM do not exist. CNI and SS7 on PSU may co-exist. The *5ESS*® switch, uses PH3 to terminate the SS7 signaling links onto the VCDX and non-VCDX offices. A signaling link arrives as a timeslot either on a 24-channel T1 facility terminating in a Digital Line and Trunk Unit 2 (DLTU2) or on a Digital Networking Unit-Sonet (DNU-S). The SS7 on PSU provides:

- Transaction Capabilities Application Part (TCAP)
- Integrated Services User Part (ISUP).

On the non-VCDX offices, if a Switching Module is equipped as a GSM, an ISUP trunk group or TCAP service can be provisioned by the customer to use either CNI or an SS7 PSU for message transport. This will provide a means for the service provider to transition signaling from CNI to the SS7 PSU for normal and stand-alone operation over time rather than being flash cut.

5.3.29 INTEGRATED DIGITAL CARRIER UNIT

5.3.29.1 Integrated Digital Carrier Unit - J5D003FL-1

The Integrated Digital Carrier Unit (IDCU) is an interface on the SM that provides integrated access to Digital Loop Carrier (DLC) systems. In addition to terminating TR-008 systems (POTS and other switched services), the IDCU supports TR-303 integrated DLC (IDLC) systems (POTS, switched, and ISDN), as well as PUB 43801 (nonswitched and nonlocally switched services) interfaces. The initial offering of this hardware provides the first phase of a TR-303 implementation.

The IDCU provides an open interface as described in Telcordia Technologies, Inc. TR-TSY-000303 to support concentrated Integrated Services Digital Network (ISDN). This feature supports the following Remote Terminals (RTs):

- *SLC*® 96 Carrier System Remote Terminals
  - Mode I
  - Mode II.
- *SLC*® Series 5 Carrier System Remote Terminals
  - Feature Package 303G (FP303G): TR-008 Mode I, TR-008 Mode II, or TR-303 interface (with concentrated ISDN)
  - Feature Package B (FPB)
  - Enhanced Feature Package B (FPB+) Mode I
  - Enhanced Feature Package B (FPB+) Mode II.

- Large Remote Digital Terminals (RDTs)
  - TR-008 Mode
  - TR-303 Mode
  - TR-008 Compatible RTs.
- TR-303 Compliant RTs.

IDCU TR-303 Industry Standard 96 Line RDT Interface was the *5ESS*® switch's first Product Release of the TR-303 Industry Standard 96 Line RT Interface. It implements the IDCU with the *SLC*® Series 5 carrier system remote terminal equipped with FP303G. The *5ESS*® switch's implementation of TR-303 is described in 235-900-308, *Integrated Digital Carrier Unit TR-TSY-000303 Interface Specification*. The TR-303 options implemented with the IDCU are identified and the implementation details needed to build the interface (matched to Telcordia Technologies Inc. TR-303, Revision 4) are included in this document.

If an IDCU interfaces with TR-303 RDTs, the IDCU requires a PSU(2). If an IDCU only interfaces with TR-008 RDTs, a PSU2 is not required. See Section 5.3.20 for more information on PSU2.

The IDCU TR-303 large RDT interface can support up to 2048 lines. This is significantly larger than the small RDT interface which supports up to 96 lines. Additionally, the large RDT interface can support up to 28 DS1 interfaces compared with the 5 DS1 interfaces supported in the small RDT interface. The *5ESS*® switch supports both the small and large TR-008 and TR-303 interface.

The Integrated Digital Carrier Unit (IDCU) is a single-shelf peripheral unit. The IDCU shelf is divided into two service groups (SGs) [that is, SG 0 and SG 1] that operate in an "active/standby" configuration. Figure 5.3-39 shows the IDCU shelf layout. The IDCU contains four or five duplicated circuit packs (that is, Power Converter with Display and Control (PCDC), Common Control Processor (CCP), PIDB Transmission Interface (PTI) and Loopside Interface (LSI0, LSI1). The IDCU also contains one or two common packs, Electrical Line Interface (ELI0 and ELI1). The LSI1 and ELI1 are optional.

The IDCU connects within the SM via Peripheral Interface Control Bus (PICB), Peripheral Interface Data Bus (PIDB) and Directly Connected Interface Data Bus (DPIDB). The DS1 cables connect to it from the Digital Cross-Connect (DSX) bay. The SM-2000 supports up to 34 IDCU peripheral units with unit numbers from 0 to 42. This maximum number can only be reached if other peripherals are not also maximally installed.

5.3.29.2 PIDB Transmission Interface

The PIDB Transmission Interface (PTI) contains a time slot interface that can connect any DS1 time slot to any time slot on the PIDBs, to the SM TSIU, or on the DPIDBs to the PSU. The PTI provides a signal processing function which monitors incoming signaling to detect originations and transmits idle signaling.

5.3.29.3 Loopside Interface

Each Loopside Interface (LSI) terminates 20 DS1s. Two fully duplicated LSIs are required to equip an IDCU. The LSI frames on each of the DS1s convert it to a PIDB-like format on the internal bus to the PTI. It also collects DS1 performance-monitoring data and detects DS1 failures and alarms.

5.3.29.4 Electrical Line Interface

The Electrical Line Interface (ELI) splits the received DS1 signals to active/standby LSIs and combines the transmitted DS1 signals; each ELI can handle 20 DS1s. The units are not duplicated because they contain only passive components and a single fault can affect only one DS1.

Figure 5.3-39 IDCU Shelf Layout - J5D003FL-1

5.3.30 Peripheral Control and Timing Line and Trunk Unit (PLTU)

The Peripheral Control and Timing Facility Interface (PCTFI) provides the *5ESS*® switch with the capability to interface to access services and transport products. The PCTFI is implemented by using the 65.536 Mbps Peripheral Control and Timing (PCT) link(s) from the SM-2000 TSI to directly terminate a variety of peripheral unit types and applications onto the *5ESS*® switch. The PCTFI is supported by a ``virtual unit'' (implemented in software), called the Peripheral Control and Timing (PCT) Line and Trunk Unit (PLTU). From a hardware perspective, the PCTFI connects through an optical paddle board (BKD10) to the TSI backplane. The customer terminations supported on this interface appear at the TSI on the PCT link as shown in Figure 5.3-40 . Therefore, an intervening peripheral unit, such as the DNU-S, is not required.

Figure 5.3-40 PCT Facility Interface Switching Ports

5.3.31 DIAGNOSTIC PHASE DESCRIPTIONS

This section contains the diagnostic phase descriptive information (in the form of tables) for the SM hardware (units/circuits) of the *5ESS*® switch. The entries closely follow those used on the MCC display pages and input/output messages.

The entry [PR Name=*xxxxxxxx*] in the DESCRIPTION/WHAT IS TESTED column in a mnemonic reference to the appropriate diagnostic PR (program listing).

The following is a list of the diagnostic phase tables:

- Table 5.3-9 , Diagnostic Phase Descriptions for AIUCOMDAC
- Table 5.3-10 , Diagnostic Phase Descriptions for AIULC
- Table 5.3-11 , Diagnostic Phase Descriptions for AIULP-U

- Table 5.3-12 , Diagnostic Phase Descriptions for AIULP-Z
- Table 5.3-13 , Diagnostic Phase Descriptions for AIURG
- Table 5.3-14 , Diagnostic Phase Descriptions for AIUTSGRP
- Table 5.3-15 , Diagnostic Phase Descriptions for ALIT
- Table 5.3-16 , Diagnostic Phase Descriptions for ASC
- Table 5.3-17 , Diagnostic Phase Descriptions for BTSR
- Table 5.3-18 , Diagnostic Phase Descriptions for CC (DNU-S)
- Table 5.3-19 , Diagnostic Phase Descriptions for CD (DNU-S)
- Table 5.3-20 , Diagnostic Phase Descriptions for CDFI/RDFI
- Table 5.3-21 , Diagnostic Phase Descriptions for CDI
- Table 5.3-22 , Diagnostic Phase Descriptions for DCLU
- Table 5.3-23 , Diagnostic Phase Descriptions for DCTUCOM
- Table 5.3-24 , Diagnostic Phase Descriptions for DCTUPORT
- Table 5.3-25 , Diagnostic Phase Descriptions for DFI
- Table 5.3-26 , Diagnostic Phase Descriptions for DFI2
- Table 5.3-27 , Diagnostic Phase Descriptions for DFIH
- Table 5.3-28 , Diagnostic Phase Descriptions for DFTAC
- Table 5.3-29 , Diagnostic Phase Descriptions for DIST
- Table 5.3-30 , Diagnostic Phase Descriptions for DLI
- Table 5.3-31 , Diagnostic Phase Descriptions for EAN
- Table 5.3-32 , Diagnostic Phase Descriptions for GDSF
- Table 5.3-33 , Diagnostic Phase Descriptions for GDSUCOM
- Table 5.3-34 , Diagnostic Phase Descriptions for GDXACC
- Table 5.3-35 , Diagnostic Phase Descriptions for GDXC
- Table 5.3-36 , Diagnostic Phase Descriptions for GDXCON
- Table 5.3-37 , Diagnostic Phase Descriptions for GRID/GRIDBD (SM)
- Table 5.3-38 , Diagnostic Phase Descriptions for GRID/GRIDBD EXERCISE (SM)
- Table 5.3-39 , Diagnostic Phase Descriptions for GRID/GRIDBD PATH TEST (SM)
- Table 5.3-40 , Diagnostic Phase Descriptions for HDFI
- Table 5.3-41 , Diagnostic Phase Descriptions for IDCU

- Table 5.3-42 , Diagnostic Phase Descriptions for ISLUCC
- Table 5.3-43 , Diagnostic Phase Descriptions for ISLUCD
- Table 5.3-44 , Diagnostic Phase Descriptions for ISLUHLSC
- Table 5.3-45 , Diagnostic Phase Descriptions for ISLULC (T-Card)
- Table 5.3-46 , Diagnostic Phase Descriptions for ISLULC (U-Card)
- Table 5.3-47 , Diagnostic Phase Descriptions for ISLULC (Z-Card)
- Table 5.3-48 , Diagnostic Phase Descriptions for ISLULGC
- Table 5.3-49 , Diagnostic Phase Descriptions for ISLUMAN
- Table 5.3-50 , Diagnostic Phase Descriptions for ISLURG
- Table 5.3-51 , Diagnostic Phase Descriptions for ISTF
- Table 5.3-52 , Diagnostic Phase Descriptions for LDSF
- Table 5.3-53 , Diagnostic Phase Descriptions for LDSU
- Table 5.3-54 , Diagnostic Phase Descriptions for LDSUCOM
- Table 5.3-55 , Diagnostic Phase Descriptions for LUCHAN/LUCHBD
- Table 5.3-56 , Diagnostic Phase Descriptions for LUCOMC (LU1)
- Table 5.3-57 , Diagnostic Phase Descriptions for LUCOMC (LU2 and LU3)
- Table 5.3-58 , Diagnostic Phase Descriptions for LUHLSC (LU1)
- Table 5.3-59 , Diagnostic Phase Descriptions for LUHLSC (LU2 and LU3)
- Table 5.3-60 , Diagnostic Phase Descriptions for MA
- Table 5.3-61 , Diagnostic Phase Descriptions for MAB
- Table 5.3-62 , Diagnostic Phase Descriptions for MCTSI (SMP 1/12/23)
- Table 5.3-63 , Diagnostic Phase Descriptions for MCTSI (SMP 20)
- Table 5.3-64 , Diagnostic Phase Descriptions for MCTSI SM-2000
- Table 5.3-65 , Diagnostic Phase Descriptions for MCTSI (MCTU3)
- Table 5.3-66 , Diagnostic Phase Descriptions for MSUCOM
- Table 5.3-67 , Diagnostic Phase Descriptions for MTIB
- Table 5.3-68 , Diagnostic Phase Descriptions for MTIBAX
- Table 5.3-69 , Diagnostic Phase Descriptions for NLI
- Table 5.3-70 , Diagnostic Phase Descriptions for OIU
- Table 5.3-71 , Diagnostic Phase Descriptions for PCTFI

- Table 5.3-72 , Diagnostic Phase Descriptions for PDLI
- Table 5.3-73 , Diagnostic Phase Descriptions for PMU
- Table 5.3-74 , Diagnostic Phase Descriptions for PROTO
- Table 5.3-75 , Diagnostic Phase Descriptions for PSUCOM
- Table 5.3-76 , Diagnostic Phase Descriptions for PSUPH
- Table 5.3-77 , Diagnostic Phase Descriptions for PSUPH-ATM
- Table 5.3-78 , Diagnostic Phase Descriptions for PSUPH-VOICE
- Table 5.3-79 , Diagnostic Phase Descriptions for RAF
- Table 5.3-80 , Diagnostic Phase Descriptions for RAU
- Table 5.3-81 , Diagnostic Phase Descriptions for RCLK
- Table 5.3-82 , Diagnostic Phase Descriptions for RLI
- Table 5.3-83 , Diagnostic Phase Descriptions for RRCLK
- Table 5.3-84 , Diagnostic Phase Descriptions for RUCI
- Table 5.3-85 , Diagnostic Phase Descriptions for RVPT
- Table 5.3-86 , Diagnostic Phase Descriptions for SAS
- Table 5.3-87 , Diagnostic Phase Descriptions for SCAN
- Table 5.3-88 , Diagnostic Phase Descriptions for SDFI
- Table 5.3-89 , Diagnostic Phase Descriptions for SFI (DNU-S)
- Table 5.3-90 , Diagnostic Phase Descriptions for SLIM
- Table 5.3-91 , Diagnostic Phase Descriptions for TAC
- Table 5.3-92 , Diagnostic Phase Descriptions for TEN/TUCHBD
- Table 5.3-93 , Diagnostic Phase Descriptions for TMUX (DNU-S)
- Table 5.3-94 , Diagnostic Phase Descriptions for TTFCOM
- Table 5.3-95 , Diagnostic Phase Descriptions for UCONF
- Table 5.3-96 , Diagnostic Phase Descriptions for UTD
- Table 5.3-97 , Diagnostic Phase Descriptions for UTG.

Table 5.3-9 Diagnostic Phase Descriptions for AIUCOM (COMDAC)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the PICB (Control) interface.[PR Name=***N/A***]
2	Tests circuitry on the COMDAC. [PR Name=***N/A***] ***NOTE:*** For RCOMDACs, a failure in segment 20 indicates a problem with the RCOMDAC or BZ-RS. A TLP note provides additional information for finding the problem.

	For more information, see 241-500-009, *BZ-RS User Guide*, which was delivered with the BZ-RS. The document can also be ordered from the Lucent Learning Organization (formerly Customer Information Center).
3	Tests the control/data integrity to each equipped and ACT application pack. If an application pack is OOS, the tests for that application pack are skipped. This phase also runs the COMDAC resident diagnostics. [PR Name=***N/A***]

Table 5.3-10 Diagnostic Phase Descriptions for AIULC

PHASE	DESCRIPTION/WHAT IS TESTED
1000	Verifies the LC functionality by requesting the application pack firmware to run tests on the circuits, including PCM path tests between the LC and the controlling COMDAC. [PR Name=***N/A***]

Table 5.3-11 Diagnostic Phase Descriptions for AIULP-U (U-Interface)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies the control data flow between the line pack (LP) and both Common Data and Control (COMDAC) controllers and runs the LP resident diagnostics.
2	Verifies the PCM data paths between the LP and both COMDACs.
3	Performs metallic GPB Bus Interface Tests. For each test, the reply will contain the bus under test (LPEO or LPBL) and the expected state of the bus (open or closed). This provides sufficient information to determine if the LP relays are operating properly from voltage measures made with the COMDAC A/D circuit.
1000	Tests ISDN line circuits on an LP. This phase is requested the following ways: □ Individual LC diagnose request (manual or fault recovery) □ LP board level diagnostic with all circuits being diagnosed □ REX request which can have multiple circuits being diagnosed at once.

Table 5.3-12 Diagnostic Phase Descriptions for AIULP-Z (Z-Interface)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies the control data flow between the LP (line pack) and both Common Data and Control (COMDAC) controllers and runs the LP resident diagnostics. [PR Name=***N/A***]
2	Verifies the PCM data paths between the LP and both COMDACs. [PR Name=***N/A***]
3	Verifies the LP metallic test buses and associated relays including the paths (GPB0/1) from the COMDAC to the LP. [PR Name=***N/A***] ***Note:*** The LP metallic bus structure is likely to vary between specific LP types.
4	Run for Z-POTS circuit packs only. Verifies the LP's connection to the ring generator (RG) buses. Also verifies that the LP can be isolated from the RG buses. [PR Name=***N/A***]
1000	Verifies the LC functionality by requesting the application pack firmware to run tests on the circuits, including PCM path tests between the LC and the controlling COMDAC.

Table 5.3-13 Diagnostic Phase Descriptions for AIURG

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies the control data flow between the RG (application pack) and both COMDACs and runs the RG firmware diagnostics. [PR Name=***N/A***]
4	Verifies the RG's isolation relay, programmability, and the ringing bus connections to each AIU it is assigned. At least one in-service COMDAC is required for this phase, or the phase completion status is NTR (no tests run). [PR Name=***N/A***]

Table 5.3-14 Diagnostic Phase Descriptions for AIUTSGRP

PHASE	DESCRIPTION/WHAT IS TESTED
100	Tests the TSGRP (data) interface. [PR Name=***N/A***]

Table 5.3-15 Diagnostic Phase Descriptions for ALIT

PHASE	DESCRIPTION/WHAT IS TESTED

1	Tests receive control orders from the MSUCOM sanity test and calibration test. [PR Name=SM:DNALIT]

Table 5.3-16 Diagnostic Phase Descriptions for ASC

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the display and report status of alarms and indicators for the remote site. [PR Name=SM:DNASC]

Table 5.3-17 Diagnostic Phase Descriptions for BTSR

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests access to the BTSR board, verification of registers, and executes internal self-diagnostic of the BTSR. [PR Name=SM:DNBTSR]
2	Functional test of the BTSR (attempts to pump to STBY MCTSI memory). [PR Name=SM: DNBTSR]

Table 5.3-18 Diagnostic Phase Descriptions for CC (DNU-S)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Performs PCT loopback at PCTLI and serial PCAMB loopback at CC. PCT loopback is performed using the PCT loopword time slot. The PCT link loopword time slot is looped back at PCTLI. The PCAMB loopback test is usually done for PCAMBs through both CDs. [PR Name=SM2K:DNUSCC1]
2	Tests the HIFI device's processor-side interface, loopback, internals, and interrupts. [PR Name=SM2K:DNUSCC1]
4	Verifies operation of the DNU-S CCP (DNU-S) processor that includes timers, sanity (Contd) timer, interrupt priority encoder, and the NMIs. It also tests EPROM, I/O write protection, memory write-protection circuits, and address and data parity generators and checkers. [PR Name=SM2K:DNUSCC1]
5	Tests the operation of the two control interface (CI) devices on the CC pack. [PR Name=SM2K:DNUSCC1]
7	Tests fan and fuse alarms, parallel PCAMBs between CC under test and both CDs. Then tests the mate bus, ICB interface and mate hashsum. If there is no active CC, this phase will NTR. The mate bus is tested from the active CC towards the CC under test. The CC under test is initialized into DGN mode before the active CC can access it. [PR Name=SM2K:DNUSCC1]
8	Tests the mate access circuit from the CC under test to the active CC. It verifies that the CC under test can detect mate errors by putting the Active CC in hold and forcing the mate errors. [PR Name=SM2K:DNUSCC1]
9	Requests the DNU-S CC to run a ROM-based memory test for the CC memory. [PR Name=SM2K:DNUSCC1]

Table 5.3-19 Diagnostic Phase Descriptions for CD (DNU-S)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the PCT link(s) between the SM/SM-2000 and the DNU-S. This phase of the CD diagnostic is a common product shared by all PCT-based peripherals. [PR Name=SM2K:DNUSCD1]
2	Tests the Internal Control Bus (ICB) and Peripheral Control Interface (PCI) devices and their interface to the ON-LINE and the STBY CC. Also test the general registers and their interface to the PCIBUS. The clock tracking and generating circuits are also tested in this phase. [PR Name=SM2K:DNUSCD2]
3	Tests the Peripheral Control and Maintenance Bus (PCAMB) interfaces to active and OOS/STBY CC. Both the serial and parallel buses are tested as well as the MCTSI IF sink/source registers that access the PCTLIs. [PR Name=SM2K:DNUSCD2]
4	Tests the 6 PCTLI devices on the CD pack. The PCI between the CD and SM-2000 for each PCT link are also tested. [PR Name=SM2K:DNUSCD2]
5	Tests the BPIDBs to the TMUXs. [PR Name=SM2K:DNUSCD2]

Table 5.3-20 Diagnostic Phase Descriptions for CDFI/RDFI

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests CI/CLRT integrity. [PR Name=SM:DNDFIG1]
2	Tests CCB integrity. [PR Name=SM:DNDFIG1]
3	Tests □C integrity. [PR Name=SM:DNDFIG1]
4	Tests maintenance buffer integrity. [PR Name=SM:DNDFIG2]
5	Tests LSI exercises I. [PR Name=SM:DNDFIG2]
6	Tests LSI exercises II. [PR Name=SM:DNDFIG3]
7	Tests facility alarm clock. [PR Name=SM:DNDFIG3]
9	Tests STBY CI/CLRT check. [PR Name=SM:DNDFIG3]
10	Tests DPR, XPC, FDL integrity. [PR Name=SM:DNDFIG4]
11	Tests T1 clock, T1 status, and RSM reset exercises. [PR Name=SM:DNDFIG4]
12	Tests signaling and PCM data path test (the ACT and STB FIU). [PR Name=SM:DNDFIG4]

Table 5.3-21 Diagnostic Phase Descriptions for CDI

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests loopback register, service request register, ASW register, and ESR. [PR Name=SM:DNCDI]
2	Tests clock errors, data path integrity and data delay circuits. [PR Name=SM:DNCDI]
3	Tests the interface with the STBY MCTSI. If MCTSI is not ACT/STBY, then CATP completes. [PR Name=SM:DNCDI]

Table 5.3-22 Diagnostic Phase Descriptions for DCLU

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the CI/CLRT integrity [PR Name=SM:DNDCLU1]
2	Verifies operation of DFI select register and the "dummy" CLRT. [PR Name=SM:DNDCLU1]
3	Tests operation of the TSSR (Time Slot Select Register). [PR Name=SM:DNDCLU1]
4	Verifies the PIDB to the ACT MCTSI. [PR Name=SM:DNDCLU2]
5	Verifies the interface between the CI/CLRT for STDBY MCTSI and the PIDB to the STDBY MCTSI. [PR Name=SM:DNDCLU2]

Table 5.3-23 Diagnostic Phase Descriptions for DCTUCOM

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the CI/CLRT integrity. [PR Name=SM:DNDCTC]
2	Runs DCTU special diagnostic: CPU test, RAM/ROM tests, GPIB loopback, and arithmetic processor. [PR Name=SM:DNDCTC]
3	Tests the CI/CLRT integrity to STBY MCTSI. [PR Name=SM:DNDCTC]

Table 5.3-24 Diagnostic Phase Descriptions for DCTUPORT

PHASE	DESCRIPTION/WHAT IS TESTED
1	Runs Group J DCTU tests. [PR Name=SM:DNPORT]

Table 5.3-25 Diagnostic Phase Descriptions for DFI

PHASE	DESCRIPTION/WHAT IS TESTED
1 **a**	Tests the active side CI-CLRT. The functions verified: 1. Serial transmission capabilities, including the PICB transmission paths, order start code, order parity, and serial loop back checks. 2. Parallel loop back capabilities, including the subaddresses register, the four subaddress registers, and the Peripheral Control Link (PCL) exercise register. 3. CLRT clear capabilities, including output-piso, the four subaddress registers, and PCL exercise clear. 4. ASW integrity, which includes a check for ASW response and an exercise to check the checker. 5. Status latch control, which verifies status-reread and explicit clear capabilities as well as a status-latch exercise. 6. PSR test, which checks the PSR function and a PSR exercise. [PR Name=SM:DNec5_1] **a**
2 **a**	Tests the mate CI-CLRT communication paths and provides a comprehensive system test for the CLRT. The functions verified: 1. Serial transmission capabilities, including the PICB transmission paths, order start code, order parity, and serial loop back checks. 2. Parallel loop back capabilities, including the subaddress Control Link (PCL) exercise register. 3. CLRT clear capabilities, including output-piso, the four subaddress registers, and PCL exercise clear. 4. ASW integrity, which includes a check for ASW response and an exercise to check the checker. 5. Status latch control, which verifies status-reread and explicit clear capabilities as well as a status-latch exercise. 6. PSR test, which checks the PSR function and a PSR exercise. [PR Name=SM:DNec5_1] **a**
3 **a**	Tests the integrity of the CCB interface. The functions verified: 1. Integrity of the transmission path between CLRT and CCB. 2. CCB Data RAM is accessible both for reading and writing. 3. Flag RAM is accessible both for reading and writing. 4. Decision tree for pinpointing raised flags (activity flags, summary flags) works.

	5. All error reporting mechanisms (address, matching, parity errors) are in working order. 6. That the clear operation visibly works. [PR Name=SM:DNec5_1] **a**
4 **a**	This phase insures that the microprocessor can be brought up from a cold start and that the firmware enters its process schedule routine. The functions verified: 1. Partial check of microprocessor to CCB data access and flag protocol. 2. Sanity time-out indicator (shows that the firmware is cycling in process scheduler). [PR Name=SM:DNec5_1] **a**
5 **a**	This phase tests the PMTG parity walker and the firmware parity error reporting mechanism. It also verifies that the PMTG does not corrupt data passed through it on the active or mate PIDB. The functions verified: 1. The circuit's ability to pass PCM and signaling information at the circuit interface is verified by looping through the PMTG over the active and mate PIDBs. 2. The firmware error reporting mechanism is enabled and verified by detecting transmit and receive errors with the PMTG. 3. The circuit's ability to pass PCM and signaling information through the circuit is verified by looping PCM and signaling information through the companion DFI over the far-end active and mate PIDBs. 4. The PMTG parity walker circuitry is verified by forcing the companion DFI to loose synchronization. [PR Name=SM:DNec5_2] **a**
6	This phase is not used.
7 **a**	This phase verifies that echo cancellation can be disabled using the 2100Hz disabling tone. This phase verifies: 1. The 2100Hz tone recognition and echo cancellation control circuitry. 2. Echo Cancellation and Voice Path Assurance tests. [PR Name=SM:DNec5_2] **a**
8 **a**	*(Demand phase.)* This phase verifies cancellation is performed correctly at the proper loss levels and that the voice path assurance tone is passed without cancellation. ***NOTE:*** The echo cancellation test performed in this phase executes only on the TN1511 EC5s. Phase 7 contains the echo cancellation tests for the TN1825 EC5s.
9	This phase initializes and tests the CI-CLRT communication paths and provides a comprehensive system test for the CLRT. The functions verified: 1. Serial transmission capabilities, including the PICB transmission paths, order start code, order parity, and serial loopback checks. 2. Parallel loopback capabilities, including the subaddress register, the four subaddress registers, and the PCL exercise register. 3. CLRT clear capabilities, including output-piso, the four subaddress registers, and PCL exercise clear. 4. ASW integrity, which includes a check for ASW response and an exercise to check the checker. 5. Status latch control, which verifies status reread and explicit clear capabilities as well as a status latch exercise. 6. PSR test, which checks the PSR function and a PSR test. [PR Name=SM:DNdfig1] **a**
10	Tests the integrity of the CCB. The functions verified: 1. Integrity of the transmission path between CLRT and CCB. 2. CCB Data RAM is accessible both for reading and writing. 3. Flag RAM is accessible both for reading and writing. 4. Decision tree for pinpointing raised flags (activity flags, summary flags) works. 5. All error reporting mechanisms (address, matching, parity errors) are in working order. 6. That the clear operation visibly works. [PR Name=SM:DNdfig1]
11	This phase insures that the microcomputer can be brought up from a cold start and that the firmware enters

	its process schedule routine. The DFI is automatically looped on itself by the firmware as part of the initialization process. [PR Name=SM:DNdfig1]
12	This phase provides a comprehensive check of the Maintenance Buffer and its internal latches. [PR Name=SM:DNdfig2]
13	This phase writes various exercise patterns to the control streams of each of the three LSI devices and checks for the correct response. Interaction among the MB, TF, RS, FR, CCB and the firmware is quite extensive, so this phase should give a good indication of the health of the LSI. [PR Name=SM:DNdfig2]
14	Like the previous phase, this phase writes exercises to the LSI devices. However, these exercises bring up facility alarms that are service affecting. Hence, these exercises must be run out-of-service. Also note that the facility response register in the CCB contains the exercise response. [PR Name=SM:DNdfig3]
15	This phase checks the address and data bus of the microcomputer as well as the integrity of the firmware via the firmware fault flag. [PR Name=SM:DNdfig3]
16	This phase verifies the integrity of the signaling and PCM data paths in the DFI. Both the active and mate PIDB's are checked. [PR Name=SM:DNdfig3]
17	This phase tests the mate-side CI by running the same tests as in Phase 1. The only difference is that the CLRT is now accessed via the mate CI. [PR Name=SM:DNdfig3]
18	Tests the XPC-8 Protocol Controller chip, the Dual Port Ram (DPR), and the internal Facility Data Link (FDL) path. The functions verified: 1. Microcomputer/CCB/DPR interface is working properly. All DPR memory cells can be written and read. 2. Microcomputer/CCB/XPC interface is good. The FDL on the DFI is also checked. [PR Name=SM:DNdfig4]
19	This phase uses the active and standby FIU to test the operation of the T1 Clock and T1 Status leads from the RSM DFI to both FIU sides. [PR Name=SM:DNdfig4]
20	This phase loops PCM and Signaling data from the Active TSI to the looped RSM DFI. [PR Name=SM:DNdfig4]
Notes:	
a.	The first eight test phases are associated with the ECSU. Phase 8 is a demand phase and is only used when DFI under test is equipped with a TN1511 EC5.

Table 5.3-26 Diagnostic Phase Descriptions for DFI 2

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the active side CI-CLRT. The functions verified: 1. Serial transmission capabilities, including the PICB transmission paths, order start code, order parity, and serial loop back checks. 2. Parallel loop back capabilities, including the subaddress register, the four subaddress registers, and the Peripheral Control Link (PCL) exercise register. 3. CLRT clear capabilities, including output-piso, the four subaddress registers, and PCL exercise clear. 4. ASW integrity, which includes a check for ASW response and an exercise to check the checker. 5. Status latch control, which verifies status-reread and explicit clear capabilities as well as a status-latch exercise. 6. PSR test, which checks the PSR function and a PSR exercise. [PR Name=DNec5_1]
2	Tests the mate CI-CLRT communication paths and provides a comprehensive system test for the CLRT. The functions verified: 1. Serial transmission capabilities, including the PICB transmission paths, order start code, order parity, and serial loop back checks. 2. Parallel loop back capabilities, including the subaddress register, the four subaddress registers, and the Peripheral Control Link (PCL) exercise register. 3. CLRT clear capabilities, including output-piso, the four subaddress registers, and PCL exercise clear. 4. ASW integrity, which includes a check for ASW response and an exercise to check the checker. 5. Status latch control, which verifies status-reread and explicit clear capabilities as well as a status-latch exercise.

	6. PSR test, which checks the PSR function and a PSR exercise. [PR Name=DNec5_1]
3	Tests the integrity of the CCB interface. The functions verified: 1. The integrity of the transmission path between CLRT & CCB. 2. The CCB Data Ram is accessible both for reading and writing. 3. The Flag Ram is accessible both for reading and writing. 4. The decision tree for pinpointing raised flags works (activity flags, summary flags). 5. All error reporting mechanisms are in working order (address, matching, parity errors). 6. That the clear operation visibly works. [PR Name=DNec5_1]
4	This phase insures that the microprocessor can be brought up from a cold start and that the firmware enters its process schedule routine. The functions verified: 1. Partial check of up to CCB data access and flag protocol. 2. Sanity time-out indicator (shows that the firmware is cycling in process scheduler). [PR Name=DNec5_2]
5	This phase tests the PMTG parity walker and the firmware parity error reporting mechanism. It also verifies that the PMTG does not corrupt data passed through it on the active or mate PIDB. The functions verified: 1. The circuit's ability to pass PCM and signaling information at the circuit interface is verified by looping through the PMTG over the active and mate PIDBs. 2. The firmware error reporting mechanism is enabled and verified by detecting transmit and receive errors with the PMTG. 3. The circuit's ability to pass PCM and signaling information through the circuit is verified by looping PCM and signaling information through the companion DFI over the far-end active and mate PIDBs. 4. The PMTG parity walker circuitry is verified by forcing the companion DFI to loose synchronization. [PR Name=DNec5_2]
6	The functions verified: That the LST can both transmit and receive 2400 Hz, 2600 Hz and 2400/2600 Hz combined tones for all 30 channels. [PR Name=DNec5_2]
7	This phase verifies that echo cancellation can be disabled using the 2100Hz disabling tone. This phase verifies: 1. The 2100 Hz tone recognition and echo cancellation control circuitry. 2. Echo Cancellation and Voice Path Assurance tests. [PR Name=DNec5_2]
9	This phase verifies the PICB interface between the active/standby MCTSI and the DFI control interface. The PICB interface circuits (parity check, start code check, and ability to force ASW errors) are verified. If the MCTSI is not duplex (ACT/STBY), only the interface to the active processor is tested and the phase completes CATP. [PR Name=DNuci]
10	This phase tests interface functions that are accessible through the module processor (MP) port. This includes testing of the first in - first out (FIFO) registers RAM, RAM parity checker/generator, summary scan registers, error source registers, mailbox registers, and mask registers. [PR Name=DNuci]
11	This phase tests the interface between the MP and local processor (LP) via the universal control interface (UCI) device. The specific tests are summary scan, interrupts and masks for the LP, access to registers, and interrupt in the hardware error source register (ESR) for errors on the LP. [PR Name=DNuci]
12	This phase tests that the microprocessor can be brought up from a cold start and that the firmware enters its process scheduler routine. The sanity time-out indicator is verified, which shows that the firmware is cycling in the process scheduler. A check of the equalizer value leads to the digital signal interface (DSI) is also performed. [PR Name=DNdfid1]
13	This phase checks the response of firmware that runs EPROM and RAM diagnostics. [PR Name=DNdfid1]
14	This phase verifies the integrity of the transceiver (XCVR) uP interface. The transmitter, receive synchronizer,

	and framer functions are checked via demand exercises performed in firmware. This phase also checks the XCVR framer, remote frame alarm, remote multiframe alarm, and receive synchronizer counter functions. The XCVR RAM is checked by running facility side for all the above tests. [PR Name=DNdfid2]
15	This phase verifies the integrity of the signaling and PCM data paths in the DFI. Both the active and standby MCTSI PIDBs are checked. The alternate data RAM is used to source 8-bit PCM data toward the DFI. Signaling bits are supplied by the SP. Since the DFI is looped on itself, the data and signaling bits are sent back to the alternate data RAM where they are verified. [PR Name=DNdfid3]
16	(*TN1612 only*.) This phase tests the XPC (X.25 protocol controller) by writing different patterns to the talk-back channel and verifies a response pattern. With both paths of the RSM DFI looped at the far-end, the talk-back channel is used as a means of checking the XPC. [PR Name=DNdfid3]
17	(*TN1612 only*.) This phase sends PCM data and signaling from the MCTSI to the looped RSM DFI. A single time slot is sourced from the MCTSI and sent through the FIU-DLI to the DFI. Both active and mate FIU-DLI paths are verified. [PR Name=DNdfid3]
18	(*TN1612 only*.) This phase tests the operation of the T1 status leads from the RSM DFI to both FIU sides of an RSM. [PR Name=DNdfid3]

Table 5.3-27 Diagnostic Phase Descriptions for DFIH

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies (if the HDFI is the H1DFI) the PICB interface to the UCI from the ACT/STBY MCTSI. [PR Name=SM:DNUCI]
2	Verifies (on the H1DFI) operation of the UCI chip from the SMP end. [PR Name=SM:DNUCI]
3	Tests (on H1DFI) the UCI interface to LP side. Also verifies communication between the SMP and LP via the UCI and the associated interrupts to the LP. [PR Name=SM:DNUCI]
4	Initializes (on the HDFI) and tests the CI/CLRT communication paths and provides a comprehensive system test for the CLRT. [PR Name=SM:DNDFRI1]
5	Ensures (on the HDFI) the following: 1. The integrity of the transmission path between the CLRT and the CCB. 2. The CCB data RAM and flag RAM are accessible both for reading and writing. 3. The decision tree for pinpointing raised flag works. 4. All error reporting mechanisms are in working order. 5. The clear operation visibly works. [PR Name=SM:DNDFRI1]
6	Ensures that the microprocessor can be brought up from a cold start and that the firmware enters its process schedule routine on the HDFI. It partially checks the microprocessor to CCB data access and flag protocol, sanity time-out indicator, and loop monitor indicator. [PR Name=SM:DNDFRI1]
7	Provides a comprehensive check of the maintenance buffer and its internal latches including the report synchronizer, transmit formatter, framer control and report stream registers, register clear register, ESR, and general purpose latch on the HDFI. [PR Name=SM:DNDFRI1]
8	Writes various exercise patterns to the control streams of each of the three LSI devices on the HDFI and checks for the correct response. Interaction among the MB, TF, RS, FR, CCB, and the firmware is extensive, so this phase gives a good indication of the health of the LSI. [PR Name=SM:DNDFRI2]
9	Writes (like phase 8) exercises to the LSI devices. However, these exercises bring up facility alarms that are service affecting. The TF does not have any facility alarm exercises. [PR Name=SM:DNDFRI2]
10	Checks facility alarm reporting on the HDFI in an indirect manner by taking advantage of the fact that the microprocessor, when functioning properly, reports facility alarms routinely (via firmware). Hence, this phase checks the address and data bus of the microprocessor as well as the integrity of the firmware via the device summary register. [PR Name=SM:DNDFRI2]
11	Verifies the integrity of the signaling and PCM data paths in the HDFI. Both ACT and STBY PIDBs are checked. [PR Name=SM:DNDFRI2]
12	Tests the STBY side CI by running the same tests as in phase 4. The only difference is that the CLRT is now accessed via the STBY CI. [PR Name=SM:DNDFRI2]
13	Tests the XPC (in the HDFI) by writing different patterns to talk back channel and verifying a response of a true data pattern. In H1s, this test is performed for the different number of time slots that can be used for the control channel in the DLI. [PR Name=SM:DNDFRI2]
14	Checks microprocessor EPROM and RAM on the HDFI. [PR Name=SM:DNDFRI2]
15	Ensures that the microprocessor can be brought up from a cold start and that the firmware enters its process schedule routine on the RDFI. It partially checks microprocessor (R1, R2) to CCB (H1, H2) data access and flag protocol and sanity time-out. [PR Name=SM:DNDFRI2]
16	Provides a comprehensive check of the maintenance buffer and its internal latches including receive

	synchronizer, transmit formatter, framer control and report stream registers, register clear register, ESR, and general purpose latch on the RDFI. [PR Name=SM:DNDFRI3]
17	Writes various exercise patterns to the control streams of each of the three LSI devices on the RDFI and checks the correct response. Interaction among the MB, TF, RS, FR, CCB, and the firmware is quite extensive, so this phase should give a good indication of the health of the LSI. [PR Name=SM:DNDFRI3]
18	Writes (like phase 17) exercises to the LSI devices. However, these exercises bring up facility alarms that are service affecting. The TF does not have any facility alarm exercises. [PR Name=SM:DNDFRI3]
19	Checks XPC function in the RDFI. Also checks facility alarm reporting in an indirect manner by taking advantage of the fact that the microprocessor, when functioning properly, reports facility alarms routinely (via firmware). The address and data bus of the microprocessor as well as the integrity of the firmware is checked via the device summary register. [PR Name=SM:DNDFRI4]
20	Verifies the integrity of the signaling and PCM data paths in the RDFI. Both ACT and STBY PIDBs are checked. For one segment, the remote DFI is looped on itself. The looping takes place in the PMTB so that time slot 7 is returned directly to the transmit formatter. For another segment, the RDFI is unlooped and a CD is looped. [PR Name=SM:DNDFRI4]
21	Checks the microprocessor EPROM and RAM on the RDFI using on-board test routines. [PR Name=SM:DNDFRI4]
22	Checks the PMTG functions on the RDFI including the walking parity mask and error registers, control register, and remote loss of clock register. [PR Name=SM:DNDFRI4]
23	Checks the operation of the CI in the R1DFI. The primary responsibility of the CI is to recreate the PICB interface at the remote site in a manner similar to that in the nonremoted application. [PR Name=SM:DNDFRI4]
24	Tests the communication between the SMP and the H1DFI through the PICB bypass FIFO circuit by writing data in various RAM locations in the UCI and verifying that the same data is returned in the corresponding locations. [PR Name=SM:DNDFRI4]

Table 5.3-28 Diagnostic Phase Descriptions for DFTAC

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies board ID and basic register operation. [PR Name=SM:DNDFTAC]
2	Tests junctor network and monitor and talk circuits. [PR Name=SM:DNDFTAC]

Table 5.3-29 Diagnostic Phase Descriptions for DIST

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests send and receive data via MSUCOM operation of relay drivers. [PR Name=SM:DNDIST]

Table 5.3-30 Diagnostic Phase Descriptions for DLI

PHASE	DESCRIPTION/WHAT IS TESTED
1	Active MP to DLI communication and interface tests. [PR Name=SM:DNPDLI1]
2	Performs DLI internal function tests (I). [PR Name=SM:DNPDLI1]
3	Performs DLI internal function tests (II). [PR Name=SM:DNPDLI1]
6	Performs ACT TSI to DLI interface tests. [PR Name=SM:DNPDLI2]
7	Performs STBY MP to DLI interface tests. [PR Name=SM:DNPDLI2]
8	Performs STBY MP SDLC to DLI interrupt and data tests. [PR Name=SM:DNPDLI2]
9	Performs STBY TSI to DLI interface (data loopback) tests. Also tests the STBY TSI to TRCU loopback tests in an ORM. [PR Name=SM:DNPDLI3]
10	Performs switch/monitor tests. [PR Name=SM:DNPDLI3]
11	Performs the TMS NCT link loop-around tests. [PR Name=SM:DNPDLI3]

Table 5.3-31 Diagnostic Phase Descriptions for EAN

PHASE	DESCRIPTION/WHAT IS TESTED
1	Runs Group H DCTU tests. [PR Name=SM:DNEAN]

Table 5.3-32 Diagnostic Phase Descriptions for GDSF

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies the PICB interface from the ACT and STBY MCTSI. [PR Name=SM:DNUCI]
2	Verifies operation of the UCI chip from the SMP end. [PR Name=SM:DNUCI]
3	UCI tests the interface to the LP side. The MC sends messages through the UCI for the LP, upon receipt of the messages, performs the required read and write to the UCI. Then internal read and write to verify interrupts to the LP. [PR Name=SM:DNUCI]
4	Verifies all hardware of the circuit pack and its interface to PICBs and PIDBs. All segments executed by

	resident software have the "LP" prefix; all others use the resident software indirectly.[PR Name=DNds3_4]

Table 5.3-33 Diagnostic Phase Descriptions for GDSUCOM

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests CI with the ACT MCTSI. CATP completes if the MCTSI is not ACT/STBY. [PR Name=SM:DNGDSC1]
2	Tests CI with the STBY MCTSI. NTR completes if the MCTSI is not ACT/STBY. [PR Name=SM:DNGDSC1]
3	Tests the TSSR. [PR Name=SM:DNGDSC1]
4	Tests the parity checkers and generators. [PR Name=SM:DNGDSC2]
5	Tests interrupt registers, DSC parity error, and DSC fault and summary scan. [PR Name=SM:DNGDSC2]
6	Tests data links to/from ACT and STBY MCTSIs (if STBY MCTSI is OOS, then CATP executes). [PR Name=SM:DNGDSC2]

Table 5.3-34 Diagnostic Phase Descriptions for GDXACC

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests initialization. For LU1 - [PR Name=SM:DNAXS1]. For LU2 and LU3 - [PR Name=SM:DNCAXS1]
2	Verifies crosspoints, which make up the 6-by-6 test access network. If cannot test access to all HLSCs (HLSC is busy), then CATP completes. For LU1 - [PR Name=SM:DNAXS1]. For LU2 and LU3 - [PR Name=SM:DNCAXS1].
3	Verifies operation of crosspoints, which make up the 32-by-8 B-LINK access network. If cannot test access to all HLSCs (HLSC is busy), then CATP completes. For LU1 - [PR Name=SM:DNAXS2]. For LU2 and LU3 - [PR Name=SM:DNCAXS1].
4	Verifies operation of crosspoints of the 32 forward/reverse networks associated with the channel circuits in this SG. For LU1 - [PR Name=SM:DNAXS3]. For LU2 and LU3 - [PR Name=SM:DNCAXS2].
5	Verifies access network crosspoints, which connect B-LINKS to the GDX linearization circuit. For LU1 - [PR Name=SM:DNAXS3]. For LU2 and LU3 - [PR Name=SM:DNCAXS2].
6	Verifies operation of the GDX linearization circuit. For LU1 - [PR Name=SM:DNAXS3]. For LU2 and LU3 - [PR Name=SM:DNCAXS2].

Table 5.3-35 Diagnostic Phase Descriptions for GDXC

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests receive control orders from the MSUCOM and performs a compensation. [PR Name=SM:DNMCOMP]

Table 5.3-36 Diagnostic Phase Descriptions for GDXCON

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the load and read data from the source gate array and the alarm mask destination. [PR Name=SM:DNGCTR]
2	Tests the enable checking and reporting circuits. [PR Name=SM:DNGCTR]
3	Tests the power alarm reporting, storing, and inhibiting circuits. [PR Name=SM:DNGCTR]
4	Tests transmission, loading, and reading of data to the concentrator LGs. [PR Name=SM:DNGCTR]
5	Tests circuits that inhibit writes and reads to the concentrator when a multiple enable is detected. [PR Name=SM:DNGCTR]

6	Turns on the network controller lamp for 1 second, then off for 1 second. Test is repeated 7 times, and then the lamp is left on. [PR Name=SM:DNGCTR]

Table 5.3-37 Diagnostic Phase Descriptions for GRID/GRIDBD (SM)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the grid alarm status, verifies the loopable test bit positions of both grid destination gate arrays, initializes all grid crosspoints to their "off" state, and verifies the pseudo alarm capability of the grid to both SG network controllers. For LU1 - [PR Name=SM:DNGRD]. For LU2 and LU3 - [PR Name=SM:DNCGRD].
2	Verifies ability to write and read state of each crosspoint control latch for scan cutoff crosspoints. Actual connect/disconnect state not verified. For LU1 - [PR Name=SM:DNGRD]. For LU2 and LU3 - [PR Name=SM:DNCGRD].
3	Verifies ability to write and read state of each crosspoint control latch for second stage crosspoints. Actual connect/disconnect state of crosspoint are not verified. Also, crosspoint address decoding is tested for the possibility of stuck bits of "do not care" states, which could cause erroneous or multiple operation of crosspoints. For LU1 - [PR Name=SM:DNGRD]. For LU2 and LU3 - [PR Name=SM:DNCGRD].
4	Verifies ability to write and read state of each crosspoint control latch for first stage crosspoints. Actual connect/disconnect states of crosspoints are not verified. For LU1 - [PR Name=SM:DNGRD]. For LU2 and LU3 - [PR Name=SM:DNCGRD].
5	Checks operation of summary scan transition latch programming on the grid. For LU1 - [PR Name=SM:DNGRD]. For LU2 and LU3 - [PR Name=SM:DNCGRD].

Table 5.3-38 Diagnostic Phase Descriptions for GRID/GRIDBD EXERCISE (SM)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the scan cut-off crosspoints and associated scan circuitry on each of the ports. [PR Name=SM:DNFABEX]
2	Tests the first stage crosspoints along the A-LINKS. [PR Name=SM:DNFABEX]
3	Tests the second stage crosspoints along with the B-LINKS. [PR Name=SM:DNFABEX]

Table 5.3-39 Diagnostic Phase Descriptions for GRID/GRIDBD PATH TEST (SM)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests grid portion of the path for a resistive leak to ground. For LU1 - [PR Name=SM:DNLUP2]. For LU2 and LU3 - [PR Name=SM:DNLUP3].
2	Tests the path (grid and loop facility) for a dangerously high voltage (AC and/or DC). For LU1 - [PR Name=SM:DNLUP2]. For LU2 and LU3 - [PR Name=SM:DNLUP3].
3	Tests the path (grid and loop facility) for an extraneous voltage. Also tests loop facility for a resistive leak and short between tip and ring leads. For LU1 - [PR Name=SM:DNLUP2].

	For LU2 and LU3 - [PR Name=SM:DNLUP3].
4	Verifies the scan origination circuit's ability to detect off-hook for 200- and 2500-ohm loops and tests scan cutoff crosspoints for stuck open failures. For LU1 - [PR Name=SM:DNLUP2]. For LU2 and LU3 - [PR Name=SM:DNLUP3].
5	Tests scan cutoff crosspoints for stuck closed failures. For LU1 - [PR Name=SM:DNLUP2]. For LU2 and LU3 - [PR Name=SM:DNLUP3].
6	Tests the first stage crosspoint of the path for stuck open failures. Tip, ring, or failures on both leads are specifically indicated. For LU1 - [PR Name=SM:DNLUP2]. For LU2 and LU3 - [PR Name=SM:DNLUP3].
7	Tests the first stage crosspoint of the path for stuck closed failures. Tip, ring, or failures on both leads are specifically indicated. For LU1 - [PR Name=SM:DNLUP2]. For LU2 and LU3 - [PR Name=SM:DNLUP3].
8	Tests the second stage crosspoint of the path for stuck open failures. Tip, ring, or failures on both leads are specifically indicated. For LU1 - [PR Name=SM:DNLUP2]. For LU2 and LU3 - [PR Name=SM:DNLUP3].
9	Tests the second stage crosspoint of the path for stuck closed failures. Tip, ring, or failures on both leads are specifically indicated. For LU1 - [PR Name=SM:DNLUP2]. For LU2 and LU3 - [PR Name=SM:DNLUP3].
94 **a**	Reverse channel battery is applied, scan cutoff crosspoints are open, and first and second stage crosspoints are closed. For LU1 - [PR Name=SM:DNLUP2]. For LU2 and LU3 - [PR Name=SM:DNLUP3].
95 **a**	Forward channel battery is applied, scan cutoff crosspoints are open, and first and second stage crosspoints are closed. For LU1 - [PR Name=SM:DNLUP2]. For LU2 and LU3 - [PR Name=SM:DNLUP3].
96 **a**	First and second stage crosspoints are closed. Both tip and ring scan crosspoints are open. For LU1 - [PR Name=SM:DNLUP2]. For LU2 and LU3 - [PR Name=SM:DNLUP3].
97 **a**	Ring scan and first and second stage crosspoints are closed. Tip scan crosspoint is open. For LU1 - [PR Name=SM:DNLUP2]. For LU2 and LU3 - [PR Name=SM:DNLUP3].
98 **a**	Tip scan and first and second stage crosspoints are closed. Ring scan crosspoint is open. For LU1 - [PR Name=SM:DNLUP2].

	For LU2 and LU3 - [PR Name=SM:DNLUP3].
99 **a**	Both tip and ring scan crosspoints and the first and second stage crosspoints are closed. For LU1 - [PR Name=SM:DNLUP2]. For LU2 and LU3 - [PR Name=SM:DNLUP3].
Notes:	
a. Phases 94-99 hold a path up to 15 minutes allowing testing of grid and loop characteristics with special instrumentation or procedures. The HLSC is never used in the hold tests but the channel battery is used for some phases.	

Table 5.3-40 Diagnostic Phase Descriptions for HDFI

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the CI/CLRT integrity. [PR Name=SM:DNDFIG1]
2	Tests CCB integrity. [PR Name=SM:DNDFIG1]
3	Tests □C integrity. [PR Name=SM:DNDFIG1]
4	Tests maintenance buffer integrity. [PR Name=SM:DNDFIG2]
5	Tests LSI exercises I. [PR Name=SM:DNDFIG2]
6	Tests LSI exercises II. [PR Name=SM:DNDFIG3]
7	Tests facility alarm check. [PR Name=SM:DNDFIG3]
8	Tests transmit and receive signaling and PCM data paths. [PR Name=SM:DNDFIG3]
9	Tests STBY CI/CLRT check. [PR Name=SM:DNDFIG3]
10	Tests DPR, XPC, and FDL integrity. [PR Name=SM:DNDFIG4]

Table 5.3-41 Diagnostic Phase Descriptions for IDCU

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies the PICB interface from the active and standby MCTSI. [PR Name=SM:DNUCI]
2	Verifies operation of the CCP (Common Control Processor) UCI (Unified Control Interface) chip from the SMP end. [PR Name=SM:DNUCI]
3	Tests the LP (Local Processor) of the CCP UCI. The MC (module controller) sends messages through the UCI for the LP, which upon receipt of the messages, performs the required reads and writes to the UCI, and internal reads and writes to verify interrupts to the LP. [PR Name=SM:DNUCI]
4	Verifies operation of the timers, sanity timer, processor interrupts, and NMIs. It also tests EPROM, I/O write protection circuits, and address and data parity generators and checkers. [PR Name=SM:DNIDCOM]
5	Verifies the control interface between the PTI (PIDB Transmission Interface) control logic and all PTI VLSI devices: PRF (PIDB Receive Formatter), TSI (Timeslot Interchanger), SP (Signal Processor), and CI (Control Interface). The VLSI devices are tested to the extent possible (e.g. alarms, BIST, etc.) without using the data paths. The interrupt masking and clock selection/detection circuitry is also tested. [PR Name=SM:DNIDCOM]
6	Verifies the functionality of the PTI internal data paths and interconnection of the PRF, SP, and TSI devices. All modes of SP signaling state change detection are tested. [PR Name=SM:DNIDCOM]
7	This phase tests the mate access bus by verifying communication from the ACT CCP to the CCP under test with the side under test in hold. A mate memory hashsum check is also performed. [PR Name=SM:DNIDCOM]
8	This phase tests the mate access bus by verifying communication from the CCP under test to the ACT CCP with the ACT CCP put in hold. The PTI mate clock selection and LSI DSI driver enable/override circuits are also tested in this phase. [PR Name=SM:DNIDCOM]
9	This phase verifies all (D)PIDB connections and associated (D)PIDB interface circuitry.
10	This phase runs a memory test on the CCP memory (RAM). [PR Name=SM:DNIDCOM]
21	Verifies the ICB (Internal Control Bus) interface from the PTI to the LSI (Loop Side Interface) pack. [PR Name=SM:DNLSI1]
22	Verifies operation of the LSI UCI chip from the PTI end. [PR Name=SM:DNLSI1]
23	Tests the LP of the LSI. The CCP sends messages through the UCI for the LP, which upon receipt of the messages, performs the required reads and writes to the UCI, and internal reads and writes to verify interrupts to the LP. [PR Name=SM:DNLSI1]
24	This phase runs a memory test on all of the LSI memory (RAM). [PR Name=SM:DNLSI1]
25	Verifies the LSI processor, processor clock, interrupts, timers, sanity timer, 4 MHz clock detector circuit, and EPROM. It also verifies communication from LSI to DLPs (Data Link Processor) and functionality of the DLP, DLP RAM, DLP timers and interrupts, and control to SCC (Serial Communications Controller) devices. Lastly it verifies control to the rest of the devices on the pack such as the transceivers and the timeslot multiplexer/demultiplexer. [PR Name=SM:DNLSI1]
26	Verifies the functionality of the LSI internal data paths and interconnection of the timeslot multiplexer/demultiplexer, transceiver, SCC, and DSI (digital signal interface) devices. [PR Name=SM:DNLSI1]

27	Verifies all IDB (Internal Data Bus) connections and associated IDB interface circuitry. [PR Name=SM:DNLSI1]
28	*(Demand phase only for factory and installation use).* Verifies the LSI switch circuitry mainly that on the DSI device and the sync signals between the two SGs. The LSIs in both SGs must be in the growth state. [PR Name=SM:DNLSI2]
29	*(Demand phase only for factory and installation use).* Verifies the DSI output drivers and the data paths between the LSI and Electrical Line Interface (ELI) along with the output of the ELI. This phase requires a special loopback connector on the backplane, or all facilities looped back at the DSX. The LSIs in both SGs must be in the growth state, or the unit must be duplex failed. [PR Name=SM:DNLSI2]
30	*(Demand phase only for factory and installation use).* Verifies a HITLESS switch can be performed. This phase requires a special loopback connector on the backplane, or all facilities looped back at the DSX. The LSIs in both SGs must be in the growth state. [PR Name=SM:DNLSI2]

Table 5.3-42 Diagnostic Phase Descriptions for ISLUCC

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies the PICB interface from the ACT and STBY MCTSI. [PR Name=SM:DNUCI]
2	Verifies operation of the UCI chip from the SMP end. [PR Name=SM:DNUCI]
3	UCI tests the interface to the LP side. The MC sends messages through the UCI for the LP, which, upon receipt of the messages, performs the required reads and writes to the UCI, and internal reads and writes to verify interrupts to the LP. [PR Name=SM:DNUCI]
4	Verifies operation of the timers in the CC microprocessor sanity timer, PIC, and NMIs. Also tests EPROM, I/O write protection circuits, and address and data parity generators and checkers. [PR Name=SM:DNICC]
5	Verifies operation of the control sequencer on the CC under test. This includes the CS register, the sync circuitry, the CS memory, the CS memory parity generators and checkers, the 2-MHz interface and its error detection and propagation, and the 4-MHz interface and its error detection and propagation. [PR Name=SM:DNICC]
6	Verifies the interface between the CC and peripheral boards. It also verifies operation of the enable controller, ASW controller, and the service request controller. [PR Name=SM:DNICC]
7	Verifies operation of the STBY access bus from the ACT CC to the CC under test. It also verifies peripheral select bit and the CIDB interface to the ACT CD. [PR Name=SM:DNICC]
8	Verifies operation of the STBY access bus from the CC under test to the ACT CC. [PR Name=SM:DNICC]
9	Runs memory test on the CC memory (RAM). [PR Name=SM:DNICC]

Table 5.3-43 Diagnostic Phase Descriptions for ISLUCD

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies the interface between the CD under test and the ACT and STBY CCs. It also tests the peripheral register access controller's service request register and its mask register. [PR Name=SM:DNICD]
2	Tests the parity generators and checkers used in the PCM - MUX for its different control memory banks (A, B, and T). [PR Name=SM:DNICD]
3	Runs a memory test on all the CDs in the PCM - MUX control memory. [PR Name=SM:DNICD]
4	Tests the CIDB interface to the ACT and STBY CC from the CD under test and the corresponding configuration bits. This phase does not perform any test if the CCs are not duplex. [PR Name=SM:DNICD]
5	Verifies multiplexing function of the CD between all PIDBs and equipped LGCs by looping data at the LGC, using on-board signature only. [PR Name=SM:DNICD]
6	Verifies data interface between the CD packs and the ACT/STBY DI and the ACT/STBY DFs. [PR Name=SM:DNICD]

Table 5.3-44 Diagnostic Phase Descriptions for ISLUHLSC

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies communication between the ACT/STBY CCs and the HLSC. Also tests the ability to shut down the power converter on the HLSC and ring trip service request. Finally, it verifies the firmware version. [PR Name=SM:DNIZHSC]
2	Tests internals of the HLSC with self-test routines. [PR Name=SM:DNIZHSC]
3	Tests the HLSC buses 0 and 1 output relays. It also verifies ring trip function and the ability of the HLSC to supply DC voltages. [PR Name=SM:DNIZHSC]

Table 5.3-45 Diagnostic Phase Descriptions for ISLULC (T-Card)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies the CIs to the LC, the function of the maintenance circuitry and its masks, and the directed scanning

	and isolation functions. [PR Name=SM:DNITC]
2	Verifies a test for single bit errors in the time slot comparator and parity of the B and D channels. It also tests the ability of the T-Interface Card to communicate over a path to the TSI. [A duplex path (two time slots at the TSI, the same time slot number on LIDB sides 0 and 1 to the card under test) is set up between the ACT TSI and the T-Interface Card under test. The dual upstream mode of the card is also tested over this duplex path] [PR Name=SM:DNITC]
3	Only runs on ISLULGC diagnosis with LC option requested. Verifies the time slot comparator, the origination and fault scan operation, and the broadcast mode operation. [PR Name=SM:DNITC]

Table 5.3-46 Diagnostic Phase Descriptions for ISLULC (U-Card)

PHASE	DESCRIPTION/WHAT IS TESTED [a]
1	Runs for all sources. Concerned with the control access to the LC through primitive reads and writes provided by ISLU base software. Checks the control path to the LC and checks for proper register access as a foundation to other tests. Also verifies the time slot selection feature of the LC. [PR Name=SM:DNISUC]
2	Runs for all sources. Concerned with the various channel's mode of operation. The GIDB data path, e-bit control, and data parity are examined. Also checks local loopback of data, U-K logic, and verification of the echo canceler. Finally, this phase checks the operation of the spare U-DSL card and the U-DSL card crosspoints via the LG bus, and the ability to spare the LC is examined via the spare bus. [PR Name=SM:DNISUC]
3	Can only be run if the ISLULGC is OOS. The ISLULGC diagnostic must be run with the LC option. Checks broadcast features of the LC and performs fault and summary LG scan tests. Also does a full test of the B and D time slot comparator. [PR Name=SM:DNISUC]
4	*(Demand phase only.)* For the AMI U-Type Interface Card, examines the upstream responses to changes in the downstream N-channel signaling using the NT1. For the *ANSI*® U-Type Interface Card, examines the upstream response to the downstream EOC messages sent to the NT1. For both the AMI and *ANSI*® U-Type Interface Cards, verifies that each channel can transmit/receive without data corruption through loopbacks and a digital source. Each channel is also checked for data integrity. Also does a metallic mismatch test to check for a mismatch between the LC/NT1 installed and the ODD and also a check for a tip and ring open or short. For AMI, checks for a tip and ring reversal. [PR Name=SM:DNISUC]
5	Used only by the *ANSI*® U-Type Interface Card. Runs for all sources except automatic, which is called by fault recovery. Performs tests to check the PM circuitry. [PR Name=SM:DNISUC]
Notes:	
a. Unless otherwise specified, these descriptions are for both the AMI and *ANSI*® U-Type Interface cards. The segment numbers for the AMI cards begins with 4000 and the segment numbers for the *ANSI*® cards begins with 5000.	

Table 5.3-47 Diagnostic Phase Descriptions for ISLULC (Z-Card)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies the CIs to the LC. Also verifies the function of the maintenance circuitry and its masks. Also tests the digital circuitry to the MCTSI and e-bit control. [PR Name=SM:DNIZC1]
2	Tests the DC portion of the LC, which can be tested without closing the tip and ring crosspoints. Also tests spare bus continuity if the card is a spare card. [PR Name=SM:DNIZC1]
3	Tests the remaining DC portion of the LC and the metallic connections to access buses 0 and 1. [PR Name=SM:DNIZC1]
4	Tests the ring trip circuit on the LC. [PR Name=SM:DNIZC1]
5	Performs basic transmission testing in the ISLU. [PR Name=SM:DNIZC3]
6	*(Demand phase only.)* Performs comprehensive transmission tests including auto-out, idle channel noise, receive and transmit filters, balance network, and gain states. [PR Name=SM:DNIZC2]
7	Performs basic time slot comparator check. [PR Name=SM:DNIZC3]
8	*(Demand phase only.)* Runs the tests that may interfere with a PBX if the line is a PBX line. [PR Name=SM:DNIZC2]
9	Runs only if the ISLULGC diagnostic is requested with the LC option. Tests the summary scan, fault scan, and performs a comprehensive time slot comparator check. [PR Name=SM:DNIZC2]

Table 5.3-48 Diagnostic Phase Descriptions for ISLULGC

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies the interface to the LGC from the ACT/STBY major and minor CD. It also tests the internal logic and bit decoding, and verifies the ability to communicate with an LC both GIDBs. [PR Name=SM:DNLGC]
2	Verifies the interface from the LGC to each equipped LC in the SG - not OOS due to a faulty condition. Also,

	each LC in an OOS faulty condition is verified that no directed scan is detected when it is isolated. [PR Name=SM:DNLGC]
3	Verifies the directed, faulty, and summary scan from each equipped LC in the SG - not OOS due to a faulty condition. [PR Name=SM:DNLGC]
4	Verifies operation of the loopback mode for the LGC. In this mode, data and control are looped back to the STBY CC from the LGC under test. [PR Name=SM:DNLGC]

Table 5.3-49 Diagnostic Phase Descriptions for ISLUMAN

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies communication between ACT/STBY CCs and the MAN circuit pack. It also verifies the reset function that de-energizes all relays and associated latches. [PR Name=SM:DNMAN]
2	Tests the MTB relays, test termination relays, ringing generator maintenance relays, and spare relays. Also tests protocol circuit, MTB protection circuit, and verifies that the MAN circuit pack is disconnected from STBY MAN circuit pack on the spare bus. [PR Name=SM:DNMAN]
3	Tests all RG relays on the MAN circuit pack. [PR Name=SM:DNMAN]
4	Tests all relays on the MAN circuit pack associated with HLSCs. [PR Name=SM:DNMAN]
5	*(Demand phase only.)* Verifies that there are no foreign TR shorts and/or voltage potentials connected to the MAN circuit pack and more testing is done on the MTB relays. [PR Name=SM:DNMAN]

Table 5.3-50 Diagnostic Phase Descriptions for ISLURG

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies communication between ACT/STBY CCs. [PR Name=SM:DNIRG]
2	Tests the RG voltages and the following modes: 1. Earth backed with ring on tip lead 2. Earth backed with ring on ring lead 3. Battery backed with ring on ring lead 4. Battery backed with ring on tip lead. Also tests the sources of service request on the RG and verifies that the RGs ringing frequency agrees with that of ODD. [PR Name=SM:DNIRG]
3	Verifies that the RG can output its ringing voltage to each of the four MAN CPs. In addition, the BCF service request is also tested. [PR Name=SM:DNIRG]

Table 5.3-51 Diagnostic Phase Descriptions for ISTF

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests CI with ACT and STBY MCTSI. If STBY MCTSI is OOS, then CATP completes. [PR Name=SM:DNUCI]
2	Tests the internal functions of the UCI chip on the LDSU. [PR Name=SM:DNUCI]
3	Tests the LP-UCI interface. [PR Name=SM:DNUCI]
4	Tests LDSU bus interface to DSU2. [PR Name=SM:DNDSU2]
5	Performs LP tests - interrupt controller, timers, parity, and write protect. [PR Name=SM:DNDSU2]
6	Tests DSPs, SDI, and data to/from LDSU bus. [PR Name=SM:DNDSU2]
8	Performs memory test and operational image pump verification. [PR Name=SM:DNDSU2]

Table 5.3-52 Diagnostic Phase Descriptions for LDSF

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies the PICB interface from the ACT and STBY MCTSI. [PR Name=SM:DNUCI]
2	Verifies operation of the UCI chip from the SMP end. [PR Name=SM:DNUCI]
3	UCI tests the interface to the LP side. The MC sends messages through the UCI for the LP, upon receipt of the messages, performs the required read and write to the UCI. Then internal read and write to verify interrupts to the LP. [PR Name=SM:DNUCI]
4	Verifies all hardware of the circuit pack and its interface to PICBs and PIDBs. All segments executed by resident software have the "LP" prefix; all others use the resident software indirectly.[PR Name=DNds3_4]

Table 5.3-53 Diagnostic Phase Descriptions for LDSU

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests CI with ACT and STBY MCTSI. If STBY MCTSI is OOS, then CATP completes. [PR Name=SM:DNUCI]
2	Tests the internal functions of the UCI chip on the LDSU. [PR Name=SM:DNUCI]

3	Tests the LP-UCI interface. [PR Name=SM:DNUCI]
4	Tests LDSU bus interface to DSU2. [PR Name=SM:DNDSU2] ***For TN1890 only:*** [PR Name=DNds3_4]
5	Performs LP tests - interrupt controller, timers, parity, and write protect. [PR Name=SM:DNDSU2]
6	Tests DSPs, SDI, and data to/from LDSU bus. [PR Name=SM:DNDSU2]
8	Performs memory test and operational image pump verification. [PR Name=SM:DNDSU2]

Table 5.3-54 Diagnostic Phase Descriptions for LDSUCOM

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests CI with the ACT MCTSI. If the MCTSI is not ACT/STBY, then CATP completes. [PR Name=SM:DNLDSC1]
2	Tests CI with the STBY MCTSI. If the MCTSI is not ACT/STBY, then NTR completes. [PR Name=SM:DNLDSC1]
3	Tests the TSSR. [PR Name=SM:DNLDSC1]
4	Tests the parity checkers and generators. [PR Name=SM:DNLDSC2]
5	Tests the interrupt registers, DSC parity error, DSC fault and summary scans. [PR Name=SM:DNLDSC2]
6	Tests data links to/from ACT and STBY MCTSIs. If STBY MCTSI is OOS, then CATP completes. [PR Name=SM:DNLDSC2]

Table 5.3-55 Diagnostic Phase Descriptions for LUCHAN/LUCHBD

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests control to channel circuit. For LU1 - [PR Name=SM:DNCHN]. For LU2 and LU3 - [PR Name=SM:DNCCHN1].
2	Tests DC portion of channel circuit - battery feed, cutoff, scan encoding, loop bias, and power up/down. Initializes all GDX crosspoints associated with the channel under test. For LU1 - [PR Name=SM:DNCHN]. For LU2 and LU3 - [PR Name=SM:DNCCHN1].
3	Tests AC portion of channel circuit - parity bit, CODEC power down, CODEC circuit, hybrid gain, idle channel noise, and CODEC filter balance network. Completes CATP if either the STBY MCTSI or the TTFCOM is OOS. For LU1 - [PR Name=SM:DNCHN]. For LU2 and LU3 - [PR Name=SM:DNCCHN1].
4	Performs more exhaustive test of CODEC. Completes CATP if either the STBY MCTSI or the TTFCOM is OOS. For LU1 - [PR Name=SM:DNCHN]. For LU2 and LU3 - [PR Name=SM:DNCCHN1].
5	Checks the crosspoints associated with the path to the channel being tested. For LU1 - [PR Name=SM:DNCHN]. For LU2 and LU3 - [PR Name=SM:DNCCHN1].

Table 5.3-56 Diagnostic Phase Descriptions for LUCOMC (LU1)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests CI with the MCTSI. Completes NTR if the MCTSI is not ACT/STBY. [PR Name=SM:DNCD]
2	Tests remaining control to registers on COMDAC. Reports CI errors - does not check interface to COMDAC subtending circuits. [PR Name=SM:DNCD]
3	Tests CI with the STBY MCTSI. NTR completes if MCTSI not ACT/STBY. [PR Name=SM:DNCD]
4	Verifies operation of the common data circuit. NTR completes if the MCTSI is not ACT/STBY. [PR Name=SM:DNCD]
5	*(Demand, automatic, or growth phase.)* Tests the interface of COMDAC and its subtending circuits.

	[PR Name=SM:DNCD]

Table 5.3-57 Diagnostic Phase Descriptions for LUCOMC (LU2 and LU3)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests CIs with MCTSI, peripheral sequencer and maintenance register. CATP completes if MCTSI not ACT/STBY. [PR Name=SM:DNCCD1]
2	Tests service request controller. [PR Name=SM:DNCCD1]
3	Tests board - enable multiplexer. [PR Name=SM:DNCCD1]
4	Tests ASW controller. [PR Name=SM:DNCCD1]
5	Tests CI with STBY MCTSI. NTR completes if MCTSI not ACT/STBY. [PR Name=SM:DNCCD2]
6	Tests PIDB interface with ACT and STBY MCTSIs. CATP completes if MCTSI is not ACT/STBY. [PR Name=SM:DNCCD2]
7	*(Demand, automatic, or growth phase only.)* Tests interface of COMDAC with its subtending circuits. [PR Name=SM:DNCCD2]

Table 5.3-58 Diagnostic Phase Descriptions for LUHLSC (LU1)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies basic operations - control of power converter, bridge switch, amplifier detect overcurrent, overvoltage protection and output reversal. [PR Name=SM:DNHLSC1]
2	Tests operation of the MABs. [PR Name=SM:DNHLSC1]
3	*(Demand phase only.)* Generates and detects DC voltages and operation of the voltage flip-flop. [PR Name=SM:DNHLSC2]
4	*(Demand phase only.)* Tests filtered current crosspoints, reset time constant, ring flip- flop and ring trip RG. [PR Name=SM:DNHLSC2]
5	*(Demand phase only.)* Performs DC current generation/detection and the current sensing modes single-ended, differential, and single- ended-times-four. [PR Name=SM:DNHLSC3]

Table 5.3-59 Diagnostic Phase Descriptions for LUHLSC (LU2 and LU3)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests CI to HLSC, runs firmware self-tests and verifies version. [PR Name=SM:DNCHLSC1]
2	Tests HLSC output connections through A and B relays. [PR Name=SM:DNCHLSC1]

Table 5.3-60 Diagnostic Phase Descriptions for MA

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests send and receive data with MSUCOM, generates interrupt to MSUCOM, and operation of relay drivers. [PR Name=SM:DNMAXS]
102	Tests the MTBs for proper operations. This phase test and checks the following: Relay operations in the MA circuit pack that are connected to the MTB. Connections to the TBCU for integrated subscriber loop carriers. [PR Name=SM:DNMAXS]
103	Tests integrated subscriber loop carrier terminations on each RT connected to the MTB. [PR Name=SM:DNMAXS]

Table 5.3-61 Diagnostic Phase Descriptions for MAB

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests access bus and all connecting relays in MSU shelf. [PR Name=SM:DNJUNC]

Table 5.3-62 Diagnostic Phase Descriptions for MCTSI (SMP 1/12/23)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests static RAM, PICs address, data latches access to all boards of IMP, and all equipped memory boards in SMP 1/12/23. Skips PIC test if either DLI is OOS and completes CATP. [PR Name=SM:DNMP1]
2	Processor sanity test, tests dormant logic and parity checkers on TN871/TN1397/TN1407 in SMP 1/12/23. [PR Name=SM:DNMP2]
3	Tests ROM checksum, write protect, stack protect, address decoder, and microcode number on TN874 in SMP 1/12/23. [PR Name=SM:DNMP3]
4	Tests ESRs, sanity and I/O timers, reset handling circuits, status registers, BCR and its shadow register, subunit mismatch error detection, and address decoders on the TN873/TN1533 in SMP 1/12/23. [PR Name=SM:DNMP4]
5	Tests SDLC and DMA circuits, and DLI interface on the TN872 in SMP 1/12/23. Completes CATP if either DLI

	is OOS. [PR Name=SM:DNMP5]
6	Tests TN875/TN1409/TN1527 and all memory boards - row and column parity, hamming and a 2-pass memory test in SMP 1/12/23. [PR Name=SM:DNMP6]
7	*(Demand and Manual phase only, not REX.)* Memory tests - a more exhaustive (8-pass) memory test in SMP 1/12/23. Use when suspected marginal memory board, but normal MCTSI is ATP. [PR Name=SM:DNMP6]
8	Tests the power alarm circuitry on the TN874B and ASC in SMP 1/12/23. [PR Name=SM:DNMP7]
9	Tests the CPI in SMP 1/12/23. Will not perform test if either DLI or any TMS link is OOS and completes CATP. [PR Name=SM:DNMP7]
10	Performs update bus test for SMP 1/12/23. [PR Name=SM:DNMP8]
11	Performs the subunit access test for SMP 1/12/23. [PR Name=SM:DNMP8]
31	Tests TSI - MP interface, TSI control circuitry, control RAMs A-E, ADR, and RCV and TMT TSIs, attenuator ROM, e-bit buffer, and TSI data paths. [PR Name=SM:DNTSI1]
32	Tests TSI - DLI interface. NTR completes if either DLI is OOS. [PR Name=SM:DNTSI2]
51	Tests the SP - mode latch, M-RAM, ignore RAM, and immediate access RAM. [PR Name=SM:DNSP]
52	Tests the SP - FIFO, parity check circuits, ESR, interface to programmable interrupt controller on the TN872, and ready time-out error. [PR Name=SM:DNSP]
61	Tests the DI circuits. [PR Name=SM:DNDI]
62	Tests the DI parity check from peripheral. [PR Name=SM:DNDI]
63	Tests the DI fan-out on TN1377. [PR Name=SM:DNDI]
64	Performs no testing at this time and is reserved for future use. [PR Name=SM:DNDI]
71	Tests CI - MP interface and CI register access. [PR Name=SM:DNCI1]
72	Tests the CI - CI transmit/receive sequencers. [PR Name=SM:DNCI1]
73	CI - tests integrity of PICB paths to/from peripherals. [PR Name=SM:DNCI1]
81	Verifies SUIB interface of the PI. Fundamental communication and error reporting are verified. The port processor and DARAM are not accessed except to initialize them into a noninterfering configuration. [PR Name=SM:DNPI1]
82	Verifies access to full range of DARAM from SUIB side of PI. A complete memory test is provided from port processor side of PI. This phase is only used to verify addressing, the ability to reset memory, the write protect of memory, and auto increment of address register when reading or writing data to the DARAM. [PR Name=SM:DNPI1]
83	Verifies operation of the error correction and detection circuits from SUIB side of DARAM. Also verifies ability to detect and correct single-bit errors and to detect and report multiple-bit errors. [PR Name=SM:DNPI1]
84	Verifies port processor side of the PI. The PI is reset and pumped. Basic communication of PB is verified. If communication looks good, a sanity maze and memory test are run. This phase does not continue its operation if the initial pump fails or if set up of PB from on-line PSUCOM fails. Port processor is in a diagnostic mode. [PR Name=SM:DNPI1]
85	Verifies packet bus from PI to STBY side of PSUCOM. Only attempts test if PSUCOM is in STBY mode. If PSUCOM is OOS, test reports a CATP. The port processor in the PI is in a diagnostic mode during this phase. [PR Name=SM:DNPI1]
90	*(Demand phase only.)* Tests the TN874. Primary use is during software update when TN874 has been changed on one side of the MCTSI and needs to be tested (including the EPROM microcode number and checksum over the code in the EPROMs). [PR Name=SM:DNMP8]

Table 5.3-63 Diagnostic Phase Descriptions for MCTSI (SMP20)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the ACT processor's ability to write and read the STBY via the update bus, the dynamic memory, and the interconnections between circuit packs in an SMP20 (UN515/UN520). [PR Name=SM:DNMC2_1]
2	Verifies sanity for off-line execution, tests STBY module controller, interrupt controller, 10 ms timer, ability for STBY to be awakened and put to sleep, reset and total hold masks, sanity maze, address and data parity checkers, shadow operation register, internal and external cache, processor performance, and cross coupled interrupts/DLI interrupts in SMP20 (UN515/UN520). [PR Name=SM:DNMC2_2]
3	Tests the UN517 board, billing counter, stack protect, 10 ms timer, and verifies the microcode number in SMP20. [PR Name=SM:DNMC2_3]
4	Tests all circuitry on UN516 CS1 board not previously tested in SMP20. Tests ASR, PSRs 1&2, SPR "A"FF, 8255 port hardware, software and global memory ESRs, sanity and I/O timer, reset handling circuitry, BCR, shadow BCR, and MPF circuitry. [PR Name=SM:DNMC2_3]
5	Tests the applications board (UN518), SDLC and DMA circuitry in SMP20. [PR Name=SM:DNMC2_4]
6	Tests the dynamic memory boards, EDC circuits, write protect circuits, memory refresh circuits, dynamic RAM devices, and memory self-test in SMP20 (TN1374, TN1376, and TN1661). [PR Name=SM:DNMC2_5]
7	*(Demand phase only.)* Tests dynamic memory boards by doing reads and writes from software in addition to self-tests in SMP20 (TN1374, TN1376, and TN1661). [PR Name=SM:DNMC2_6]
8	*(Demand phase only.)* Tests RSM lamp circuitry on UN516 (CS1) board and the ASC in SMP20. [PR Name=SM:DNMC2_6]
9	Tests CPR hardware in SMP20. [PR Name=SM:DNMC2_5]

10	Tests the OOS processor's ability to access the ACT side over the update bus, as well as local and STBY side pump DMA activity to memory in SMP20. [PR Name=SM:DNMC2_5]
11	Tests SIB in SMP20. [PR Name=SM:DNMC2_5]
31	Tests TSI - MP interface, TSI control circuitry, control RAMs A-E, ADR, and RCV and TMT TSIs, attenuator ROM, e-bit buffer, and TSI data paths. [PR Name=SM:DNTSI1]
32	Tests TSI - DLI interface. NTR completes if either DLI is OOS. [PR Name=SM:DNTSI2]
51	Tests the SP - mode latch, M-RAM, ignore RAM, and immediate access RAM. [PR Name=SM:DNSP]
52	Tests the SP - FIFO, parity check circuits, ESR, interface to programmable interrupt controller on the TN872, and ready time-out error. [PR Name=SM:DNSP]
61	Tests the DI circuits. [PR Name=SM:DNDI]
62	Tests the DI parity check from peripheral. [PR Name=SM:DNDI]
63	Tests the DI fan-out on TN1377. [PR Name=SM:DNDI]
64	Performs no testing at this time and is reserved for future use. [PR Name=SM:DNDI]
66	Tests interface to the BTSR circuit on the UN518 - the PIDB interface from the DI, and level 6 interrupt to UN516 in SMP20. [PR Name=SM:DNMC2_66]
71	Tests CI - MP interface and CI register access. [PR Name=SM:DNCI1]
72	Tests the CI - CI transmit/receive sequencers. [PR Name=SM:DNCI1]
73	CI - tests integrity of PICB paths to/from peripherals. [PR Name=SM:DNCI1]
81	Verifies SUIB interface of the PI. Fundamental communication and error reporting are verified. The port processor and DARAM are not accessed except to initialize them into a noninterfering configuration. [PR Name=SM:DNPI1]
82	Verifies access to full range of DARAM from SUIB side of PI. A complete memory test is provided from port processor side of PI. This phase is only used to verify addressing, the ability to reset memory, the write protect of memory, and auto increment of address register when reading or writing data to the DARAM. [PR Name=SM:DNPI1]
83	Verifies operation of the error correction and detection circuits from SUIB side of DARAM. Also verifies ability to detect and correct single-bit errors and to detect and report multiple-bit errors. [PR Name=SM:DNPI1]
84	Verifies port processor side of the PI. The PI is reset and pumped. Basic communication of PB is verified. If communication looks good, a sanity maze and memory test are run. This phase does not continue its operation if the initial pump fails or if set up of PB from on-line PSUCOM fails. Port processor is in a diagnostic mode. [PR Name=SM:DNPI1]
85	Verifies packet bus from PI to STBY side of PSUCOM. Only attempts test if PSUCOM is in STBY mode. If PSUCOM is OOS, test reports a CATP. The port processor in the PI is in a diagnostic mode during this phase. [PR Name=SM:DNPI1]

Table 5.3-64 Diagnostic Phase Descriptions for MCTSI SM-2000

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies: □ the sanity of the OOS MCTSI for power (SN410AA/UN589) □ SMP state □ SMP equipage with respect to the database □ capability to perform the accesses across the SMP update bus to the I/OS on CORE (UN540/UN540B/UN560/UN588/UN593/UN594) □ Bus Service Node (BSN; KBN8/KBN8B) □ equipped external memory boards (TN1685/TN1806) □ Application Controller (APC; UN539/UN539B) □ Message Handler (UN538/UN584) □ parity checkers and generators connected to update bus □ interconnections between circuit packs □ SMP error source hierarchy

	□ access to APCO/APCX (UN599/UN555) if equipped. Tests the external memory and its initialization using on-board self-tests. For the UN560, it also tests the internal timer and on-CORE memory and external cache using self-test. [PR Name=SM2000:DNmc4_01]
2	Tests circuits on CORE (UN540/UN540B/UN560/UN588/UN593/UN594) and BSN (KBN8/KBN8B). Verifies: □ power-up reset (exception 0) circuit to and from OOS SMP □ cross coupled processor status signals between ACTive and OOS SMP □ capability to wake-up and stop the OOS processor for off-line execution □ sanity and mate lockout, short ready timeout □ A-FF and loss-of-clock detector □ sanity maze □ cache □ SPFMR operation □ parity checkers and generators on the Local System (LS) bus □ conditional suspend timer □ processor performance □ CRC checks of the generic firmware. For the UN560, UN588, UN593, and UN594, the external cache maintenance modes, internal timers, lock protocol, loss of sync, and write posting buffer are also tested. [PR Name=SM2000:DNmc4_02]
3	Tests circuits on CORE and BSN. Verifies: □ processor status registers □ PICs □ to/from mate interrupt signals between the ACT and OOS SMPs □ control/display circuits (SN516 for SM-2000 with SMPU4/UN589 for SM-2000 with SMPU5) □ sanity timer □ I/O timers □ bus error circuits □ MPF circuits for ACT and OOS SMPs. [PR Name=SM2000:DNmc4_03]
4	Tests the circuits on BSN (KBN8/KBN8B). The BSN is the interface between the LS, RS bus, and SMP update bus. Verifies: □ bus control circuits and shadow bus control □ address □ data

	□ control shadow registers □ BSN write protects □ matchers □ shadow circuits □ parity checkers and generators on the RS bus. [PR Name=SM2000:DNmc4_04]
5	Tests the circuits on APC. Verifies: □ address decoders on APC □ stuck at faults on the APC I/Os □ Bootstrapper DLI interface circuit (BDL) □ Bootstrapper Direct Memory Access (BTSR-DMA) circuits □ Sub Unit Interface Bus (SUIB) □ hardware delay register. If APCO/APCX is equipped, verify register accesses and device BIST. Verifies error detection circuitry to each equipped OCDCOM/XCDCOM (UN651/TN1996). [PR Name=SM2000:DNmc4_05]
6	Tests the circuits on the external memory boards and the circuits associated with on-CORE (UN560/UN588/UN593/UN594) memory. For the UN560, it tests the on-CORE memory circuit, scrubbing, and address comparators on Dynamic Ram Controller. Verifies: □ memory equipage □ address decoder and I/O registers □ different size memory accesses □ refresh circuits □ corr-bit counter and threshold circuits □ Error Detection and Correction (EDC) circuits □ memory self-test logic including the comparators □ pattern matchers □ system address leads □ different self-test modes and its interactions with hardware reset □ NMI. [PR Name=SM2000:DNmc4_06]
7	(*Demand phase only*) Tests the circuits on the external memory boards and the circuits associated with on-CORE (UN560/UN588/UN593/UN594) memory. Verifies self-test inhibit circuit, which prevents the running of the memory board self-test on the ACT side. This phase is a demand phase only, which typically would only be executed on those occasions where the memory self-test is suspect of not finding faulty memory boards or when new memory boards are being grown in the unit. [PR Name=SM2000:DNmc4_07]

8	(*Demand phase only*) Tests the circuits on KBN8/KBN8B, Alarm Status Unit (ASU) paddleboard (9822DU), and Stand Alone Monitor circuit in ASU, when ASU is equipped (EXM2000 configuration). Verifies the ASU equipage and then tests the RSM sanity and stand-alone indicator logic on BSN and SAM in ASU. [PR Name=SM2000:DNmc4_08]
9	Tests the central processor intervention (CPI) circuit on KBN8/KBN8B. [PR Name=SM2000:DNmc4_09]
10	Tests the SMP update bus circuits on CORE and BSN. Verifies the update bus status signals, parity, capability to drive address, data, control signals, various access modes from OOS to ACTive SMP. Tests the operation of mate ready-time-out and internal global system-ready-timeout circuits. [PR Name=SM2000:DNmc4_10]
21	Tests the local processor, on-board RAM, and BRICPIT devices of all equipped MHs (UN538/UN584). Tests the OOS MH interfaces to ACTive SMP and ACTive MH. Includes tests of: □ sanity maze □ MMU □ cache □ interrupts □ interrupt handlers □ parity circuits □ MH update buses. [PR Name=SM2000:DNmc4_21]
22	Tests the SPYDER-T (synchronous/asynchronous protocol data formatter) device functions of all equipped MH boards (UN538). Includes tests of: □ lost clock and sync circuit □ transmit and receive (internal loop-back) □ dynamic configuration □ interrupt (EOL, EOF, and EOB) □ CRC □ parity □ transmit and receive paths. [PR Name=SM2000:DNmc4_22]
23	This phase is used to test the System-Oriented Network Interface Controller (SONIC) device of all equipped Message Handler for Ethernet Interface Boards (MHEIB) boards (UN584). This includes: □ SONIC registers access □ initialization of SONIC Content Addressable Memory (CAM) and SONIC buffer □ internal loopback □ CRC checking □ SONIC interrupt □ SONIC read parity error

	□ Ethernet test to far-end system or hub (if so equipped). [PR Name=SM2000:DNmc4_23]
33	Tests circuits on TSICOM board (UM74/UM74B/UM74C/UM74D): □ Basic TSICOM access from SMP □ TSICOM version check □ SMP to TSICOM interfaces via APC □ function of TSICOM error source/mask register □ function of TSIU4 service request register (with mask) □ function of TSIU4 interrupt source/mask register □ function of the clock-control register and other TSICOM registers □ device self-tests on the TSICOM. This phase also tests TSIU4 unit equipage and all registers on all equipped TSIS boards (KLU1/KLU1B). Tests all registers on all equipped TSIS boards, including access of all equipped TSIS ports. [PR Name=SM2000:DNts_33]
34	Tests each equipped TSIS (KLU1/KLU1B) board, including: □ basic access from the SMP □ diagnostic control and error source/mask registers □ CRC error propagation □ boundary scan self-test □ intra-bound interconnect and cluster tests □ device BIST □ Control Time Slot (CTS) registers □ port equipage and version checks. [PR Name=SM2000:DNts_34]
35	Tests each equipped TSIS (KLU1/KLU1B) board-level self-tests. [PR Name=SM2000:DNts_35]
36	Tests: □ TSIS board interfaces to Interfaces to APC (UN539/UN539B) □ MCP link to TSIS-0 are tested in segment 10 □ reference clock interfaces (either CM-sourced or external references) are tested in segments 50-52 □ the (E)NLI interfaces to the TSI-links are tested in segments 60-69 □ any equipped PLI interfaces to the TSI-links are tested in segments 70-79. ***NOTE:*** PLIs assigned for OXU usage are not tested in this phase. [PR Name=SM2000:DNts_36]
37	Reserved for future use.
38	Performs additional TSIS (KLU1) functional unit-level BIST tests, concentrating on inter-TSIS board

	connections. [PR Name=SM2000:DNts_38]
40	(5E15 and later) Tests the OCDCOM/XCDCOM (UN651/TN1996) if equipped. Tests include: □ on-board BIST □ XDX (UN553) and CI2 (UN71C) equipage □ access □ crosstalk □ interrupt hierarchy □ power scan □ distribute circuitry. If OCDCOM (UN651) is equipped, verify the functions of the clock control register. [PR Name=DNts_40]
43	(5E15 and later) Tests the OXU Peripheral Link Interface (PLI) and Data Peripheral Link Interface (DPLI) hardware. Verifies equipage and register access to the PLI. Verifies equipage and device BIST for the DPLI. [PR Name=DNts_43]
44	Tests all circuits of equipped DX(UM73)/XDX(UN553 in TSIU4-2) boards. Included are: □ initial access test of control RAMs □ board configuration and inter-board crosstalk tests (segments 9 - 11) □ TSICOM to DX/XDX communication tests (segments 20, 21) □ control RAM tests of parity □ rd/mod/write masking and memory tests (segments 30-32) □ board reset □ device BIST tests (segments 40-43). [PR Name=DNts_44]
45	Tests further the DX/XDX boards individually and in looped back configurations. These tests include: □ TSI-link CRC tests (segment 50) □ PIDB parity buffer tests (segment 51) □ fan-out/fan-in tests (segment 60) □ PIDB monitoring of active/standby peripheral sides for valid parity (segment 70) □ multi-access-board PCM-looping test at the DX/XDX PIDB outputs (segment 9975). [PR Name=DNts_45]
46	DX/XDX demand phase not available to craft (this phase requires additional test equipment).
66	Tests circuits on CORE, BSN, APC, and MH-APC interface. Verifies pump data assembler circuit on APC, billing counter clock input, pump circuits on APC-MH interface, APC_MH SPYDER interface. [PR Name=DNmc4_66]
71	Diagnoses the interface between the micro-processor and the CI. At the completion, if no errors have occurred, then the data bus, address bus, and interface registers can be considered operational. Also, the address and data parity generators and checkers are exercised. [PR Name=DNSU_CI1]
72	Diagnoses the internal hardware of the CI as much as possible without attempting to communicate with the peripheral unit over a peripheral interface control bus. Assumes that the interface to the microprocessor is

	operable and that the microprocessor can communicate with all the registers in the CI. If no errors occurred, then all the CI hardware except the selectors and buffers connecting to the peripheral units, interrupt source register, and the interrupt mask registers can be considered operational. [PR Name=DNSU_CI1]
73	Diagnoses the interface between the CI and all equipped and in-service peripheral units. Assumes that the CI can communicate with the module processor. On completion, the balance of all CI hardware used to connect the equipped PICBs with PUs are verified (including, multiplexers, incoming and outgoing buffers, and local and remote interrupt structures. [PR Name=DNSU_CI1]
74	(5E15 and later) Verifies the CI2 (UN71C) to SMP interrupt structure and the broadcast capability to the equipped and in-service peripherals when the parallel pump feature is enabled. This phase completes No Tests Run (NTR) if the pump feature is disabled for all equipped CI2s. [PR Name= DNSU_CI1]
75	(5E15 and later) Diagnoses the OXU/XCDU CI2 boards. Diagnoses the interface between the micro-processor and the CI. At the completion, if no errors have occurred, then the data bus, address bus, and interface registers can be considered operational. Also, the address and data parity generators and checkers are exercised. [PR Name=DNSU_CI2]
76	(5E15 and later) Diagnoses the OXU/XCDU CI2 boards. Diagnoses the internal hardware of the CI as much as possible without attempting to communicate with the peripheral unit over a peripheral interface control bus. Assumes that the interface to the microprocessor is operable and that the microprocessor can communicate with all the registers in the CI. If no errors occurred, then all the CI hardware except the selectors and buffers connecting to the peripheral units, interrupt source register, and the interrupt mask registers can be considered operational. [PR Name=DNci76]
77	(5E15 and later) Diagnoses the OXU/XCDU CI2 boards. Diagnoses the interface between the CI and all equipped and in-service peripheral units. Assumes that the CI can communicate with the module processor. On completion, the balance of all CI hardware used to connect the equipped PICBs with PUs are verified (including, multiplexers, incoming and outgoing buffers, and local and remote interrupt structures. [PR Name=DNci77]
78	(5E15 and later) Diagnoses the OXU/XCDU CI2 boards. Verifies the CI2 (UN71C) to SMP interrupt structure and the broadcast capability to the equipped and in-service peripherals when the parallel pump feature is enabled. This phase completes No Tests Run (NTR) if the pump feature is disabled for all equipped CI2s. [PR Name=DNci78]
81	This is the first phase of the Packet Interface diagnostic; packet interface circuit PI1 (TN-1042) and PI2 (UN395/UN395B) are used to interface the PSIU to the SMP in an ISDN SM. Verifies the SUIB interface of the packet interface and basic communication across the SUIB; also, all register functions (excluding the memory and error correction. The port processor and DARAM are not accessed except to initialize them into a noninterfering configuration. [PR Name=DNpi81]
82	This is the second phase of the Packet interface diagnostic; packet interface circuit PI1 (TN-1042) and PI2 (UN395/UN395B) are used to interface the PSIU to the SMP in an ISDN SM. Verifies access to the full range of DARAM from the SUIB side of the PI. Verifies addressing, the capability to clear the memory, capability to write protect the memory, and the auto increment of the address registers when reading or writing data to the DARAM. [PR Name=DNpi82]
83	***NOTE:*** This phase is for PI1 (TN-1042) only. This phase is not run on PI2 (UN395/UN395B), so PI2 is always ATP. This is the third phase of the Packet Interface diagnostic; packet interface circuit (TN-1042) is used to interface the PSIU to the SMP in an ISDN SM. Verifies the subunit interface bus (SUIB) interface to the PI. Verifies the operation of the error correction and detection circuits from the SUIB side of the DARAM and also, detect and correct single-bit errors and multiple-bit errors. [PR Name=DNpi83]
84	***NOTE:*** This phase is for PI1 (TN-1042) only. This phase is not run on PI2 (UN395/UN395B), so PI2 is always ATP. This is the fourth phase of the Packet Interface diagnostic; packet interface circuit (TN-1042) is used to interface the PSIU to the SMP in an ISDN SM. Verifies the port processor side of the packet interface and the basic communication across the packet bus. The PI is reset and pumped. If communication looks good; a sanity maze and a memory test are run on the PI. The phase does not continue its operation if the initial "pump" fails or if the setup of the packet bus from the on-line PSIUCOM fails. The port processor is in a "diagnostic" mode during this under OSDS in the PI. Communicates with the diagnostic system process through packet bus messages. [PR Name=DNpi84]
85	Verifies the packet bus from the PI to the standby side of the PSUCOM. This phase only attempts the test if the PSUCOM is in a standby mode. If the PSUCOM is in an OOS mode, the test reports a CATP. The port processor in the PI is in a diagnostic mode during this phase. This phase executes for PI1 (TN-1042) and PI2

	(UN395/UN395B). [PR Name=DNPI1]
86	***NOTE:*** This phase is for PI2 (UN395/UN395B) only. This phase is not run on PI1 (TN-1042), so PI1 is always ATP. This phase tests the PI2 system command block in the DSRAM, initiates the ROM resident RAM test for both the DSRAM and LSRAM, and pumps the PI2. This phase executes for the PI2 only. This phase automatically ATPs if PI circuit packs are equipped. [PR Name=DNpi86]
87	Verifies the packet bus from the PI to the standby side of the PSUCOM. This phase only attempts the test if the PSUCOM is in a standby mode. If the PSUCOM is in an OOS mode, the test reports a CATP. The port processor in the PI is in a diagnostic mode during this phase. This phase executes for PI1 (TN-1042) and PI2 (UN395/UN395B). [PR Name=DNpi87]

Table 5.3-65 Diagnostic Phase Descriptions for MCTSI Unit 3 (MCTU3)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests circuits on SB20CORE (KBN17, KBN18, or KBN19). Verifies the sanity of the OOS MCTSI for power, SMP state, SMP equipage with respect to the database, ability to perform the accesses across the SMP update bus. It also verifies parity checkers and generators, Ready Time Out (RTO) detection, and SMP error source hierarchy. Test address aliasing between DRAM, I/O and the QUICC (quad integrated communications controller) device on the SB20CORE. Tests the on-board memory using self-test. [PR Name=SM:DNMC3_1]
2	Tests circuits on SB20CORE. Verifies power-up reset (exception 0) circuit to and from the OOS SMP. Rough test of timers. Verifies cross coupled status signal between ACTive and OOS SMP, ability to wake-up and stop the OOS processor for the off-line execution, sanity and mate lockout. Tests internal address and databus, bus arbiter error, sanity maze, processor performance, I/O accesses with instruction cache enabled, SPFMR operation, A-FF, shadow operations register, ROM checksum. [PR Name=SM:DNMC3_2]
3	Tests circuits on SB20CORE. Verifies processor status registers Verifies the SBPCD (TN1424) functions, write and stack protection, resets, sanity timer, MPF (mate power fail) signal, I/O timers, BCR (Bus Control Register) and shadow BCR, fan alarm verification, bus errors, and the SUIB (sub-unit interface bus). [PR Name=SM:DNMC3_3]
4	Tests parts of the TPC (timers, programmable interrupt controllers) device on SB20CORE. Verifies billing counter, timers, PIC's, to/from mate interrupts signals between ACT and OOS SMP's, DLI interrupts, SDLC parity, DLI register access. [PR Name=SM:DNMC3_4]
5	Tests the QUICC device and its interfaces on SB20CORE. Includes QUICC dual port RAM test, write protection test, hardware and software reset, timer tests, SDLC (synchronous data link controller) transmitter/receiver tests, IDMA [internal (QUICC) direct memory access) tests, and BTSR (Bootstrapper) tests. [PR Name=SM:DNMC3_5]
6	Tests dynamic memory (DRC device, SIMM modules) on SB20CORE. Verifies address decoding, EDC (error detection and correction) circuits, scrubbing, memory refresh. Tests DRAM initialization, and DRAM using self-test. [PR Name=SM:DNMC3_6]
7	*(Demand phase only.)* Tests dynamic memory on SB20CORE. Verifies BIST inhibit logic, which prevents the running of the memory self-test/initialization on the ACT SMP. Verifies internal data lead coupling in the memory complex. [PR Name=SM:DNMC3_7]
8	Verifies the ASU (alarm status unit) equipage and then tests the RSM sanity and stand-alone indicator logic on the SBPCD and the SB20CORE. [PR Name=SM:DNMC3_8]
9	Tests the CPI (Central Processor Intervention) hardware on the SB20CORE by requesting diagnostic CPI messages from the AM (or VCDX workstation) and verifying that each message is received properly. For a VCDX it verifies the CPI paddle board. [PR Name=SM:DNMC3_8]
10	Tests circuits on SB20CORE. Tests the SMP update bus with the OOS SMP as the master. Tests the ability to drive address, data, and control signals across the ACT SMP to OOS SMP data bus. Tests the ability to receive mate status signals. [PR Name=SM:DNMC3_8]
11	Tests QUICC device and its interfaces on the SB20CORE. Verifies the QUICC hardware and software reset. Verifies that the OOS SMP can transfer data via the DMA (direct memory access) over the update bus to the ACT SMP. Verifies that the BTSR, under IDMA control, can transfer data to the ACT SMP and OOS SMP. Verifies that at least one of the QUICC SDMA devices is capable of driving the update bus. Verifies that at least one of the QUICC IDMA devices is capable of driving the update bus. [PR Name=SM:DNMC3_9]
12	Tests the Ethernet controller part of the QUICC device and its interfaces on the SB20CORE. Tests include Ethernet transmitter and receiver operation (loops, external connections to Ethernet paddle board, error detection) and transmission to/reception from the Ethernet medium. [PR Name=SM:DNMC3_9]
13-30	These phases are not used for MCTU3 testing.
31	Tests TSI-DLI interface, TSI control and alternate data RAMs, TSI-SMP interface, all TSI registers, receive

	and transmit TSI RAMs. [PR Name=SM:DNTSI1]
32	Tests TSI-DLI interface. Will complete CATP if either DLI is OOS. [PR Name=SM:DNTSI2]
33-50	These phases are not used for MCTU3 testing.
51	Tests SP-mode latch, M RAM, ignore RAM and immediate access RAM. [PR Name=SM:DNSP]
52	Tests SP-FIFO, parity check circuits, error source register, interface to programmable interrupt controller on the TN1086, and ready time-out error. [PR Name=SM:DNSP]
53-60	These phases are not used for MCTU3 testing.
61	Tests DI. [PR Name=SM:DNDI]
62	Tests parity on PIDBs from PUs. Verifies receivers on PIDB links. [PR Name=SM:DNDI]
63	Tests DI fan-out on TN1377 or TN1524. All PIDBs are checked. [PR Name=SM:DNDI]
64	Tests PIDB driver and receiver on odd DI when PU is OOS. [PR Name=SM:DNDI]
65	This phase is not used for MCTU3 testing.
66	Tests the BTSR circuitry on the SB20CORE. Taking real PIDB data generated in the TSI, this phase verifies that the BTSR loops back true parity from the DI. Also verifies the BTSR to PIDB interface by generating pump data in the TSI. [PR Name=SM:DNMC3_66]
67-70	These phases are not used for MCTU3 testing.
71	Tests parity on PICBs from PUs. Verifies receivers on PICB links. Tests CI-MP interface and CI (UN71/UN71B) register access. [PR Name=SM:DNCI1]
72	Tests CI-CI transmit and receive sequencers (UN71B). [PR Name=SM:DNCI1]
73	CI - tests integrity of control paths to and from all equipped peripherals (UN71/UN71B). [PR Name=SM:DNCI1]
74-80	These phases are not used for MCTU3 testing.
81	Verifies SUIB interface of PI. Fundamental communication and error reporting are verified. In addition, all register functions, excluding memory and error correction, are verified. [PR Name=SM:DNPI1]
82	Verifies access to full range of DARAM from SUIB side of PI. A complete memory test is provided from port processor side of PI. This phase is only used to verify addressing, ability to reset memory, write protect of memory, and auto increment of address register when reading or writing data to DARAM. [PR Name=SM:DNPI1]
83	Verifies operation of error correction and detection circuits from SUIB side of DARAM. It also verifies ability to detect and correct single bit errors and to detect and report multiple bit errors. [PR Name=SM:DNPI1]
84	Verifies port processor side of PI. The PI is reset and pumped. Basic communication of PB is verified. If communication looks OK, a sanity maze and memory test are run on PI. This phase does not continue its operation if initial pump fails or if setup of PB from on-line PSUCOM fails. Port processor is in diagnostic mode during this phase. [PR Name=SM:DNPI1]
85	Verifies packet bus from PI to standby side of PSUCOM. This phase only attempts test if PSUCOM is in STBY mode. If PSUCOM is in an OOS mode, test reports CATP. Port processor in PI is in diagnostic mode during this phase. [PR Name=SM:DNPI1]
86	Verifies 68040 core of a PI2. For a PI, no tests are run. [PR Name=SM:DNPI1]
87	Verifies the packet bus cabling between the PI/PI2 and the PSUCOM. [PR Name=SM:DNPI1]
88-90	These phases are not used for MCTU3 testing.

Table 5.3-66 Diagnostic Phase Descriptions for MSUCOM

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the CI with the MCTSI. [PR Name=SM:DNMSC (for single module office) or SM:DNMMSC (for multimodule office)]
2	Tests CI with the STBY MCTSI. [PR Name=SM:DNMSC (for single module office) or SM:DNMMSC (for multimodule office)]
3	Tests the remote interrupt mask and scan registers, interrupt latches and interrupt polarity bit. [PR Name=SM:DNMSC (for single module office) or SM:DNMMSC (for multimodule office)]

Table 5.3-67 Diagnostic Phase Descriptions for MTIB

PHASE	DESCRIPTION/WHAT IS TESTED
1	Performs end-to-end protocol test of complete interconnect bus. [PR Name=SM:DNMTIB]
2	Performs step-by-step verification of interconnect bus interfaces to MSU shelves. [PR Name=SM:DNMTIB]

Table 5.3-68 Diagnostic Phase Descriptions for MTIBAX

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests send and receive data switch with MSUCOM, interrupts, and operation of relay drivers. [PR Name=SM:DNMTAC]
2	Tests relay connections to all MTIBs. [PR Name=SM:DNMTAC]

Table 5.3-69 Diagnostic Phase Descriptions for NLI

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies the interface of the LI to the active and mate side Time Slot Interchangers, as well as the functionality of various error checks. [PR Name=DNnli_1]
2	Verifies the interface of the LI to the ONTC TMS. [PR Name=DNnli_2]

Table 5.3-70 Diagnostic Phase Description for OIU

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the PCT link, SM-to-PLI interface, and the PLI pack. Interfaces to both sides of the MCTSI.
2	Tests the PCT interface to the circuit under test. The slot position and the PCT physical connection at the circuit under test are tested.
3	Runs self-tests, pack-to-pack communication tests, and the ROM-based RAM tests.
4	Tests the integrity of the facility data (PCM) path from the SMP to the OFI, on all equipped PCT links.
5	*(Demand phase only.)* Tests the external facility loopback on the OFI. Installation of an external loopback is required before running this phase.

Table 5.3-71 Diagnostic Phase Description for PCTFI

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the PCT link, SM-to-PLI interface, and the PLI pack. Interfaces to both sides of the MCTSI.
2	Tests the interface between the TSI IF peripheral registers to the PCT-TE. Both sides of the MCTSI are tested, where applicable.
3	*(Demand phase only.)* Uses the peripheral loopback word to verify the integrity of the data path to the far end. The PLI must have Xmit link looped back onto the Rcv link.

Table 5.3-72 Diagnostic Phase Descriptions for PDLI

PHASE	DESCRIPTION/WHAT IS TESTED
1	ACT MP to DLI communication and interface tests. [PR Name=SM:DNPDLI1]
2	Performs DLI internal function tests. [PR Name=SM:DNPDLI1]
3	Performs DLI internal function tests. [PR Name=SM:DNPDLI1]
6	Performs ACT TSI to DLI interface tests. [PR Name=SM:DNPDLI2]
7	Performs STBY MP to DLI interface tests. [PR Name=SM:DNPDLI2]
8	Performs STBY MP SDLC to DLI interrupt and data tests. Also tests the STBY TSI to DLI data loopback on all time slots. [PR Name=SM:DNPDLI2]
9	Performs STBY TSI to DLI interface (data loopback) tests. Also tests the STBY TSI to TRCU loopback tests in an ORM. [PR Name=SM:DNPDLI3]
10	Performs switch/monitor tests. [PR Name=SM:DNPDLI3]
11	Performs the TMS NCT link tests. CTS is looped back in the TMS. [PR Name=SM:DNPDLI3]

Table 5.3-73 Diagnostic Phase Descriptions for PMU

PHASE	DESCRIPTION/WHAT IS TESTED
1	Runs Group D DCTU tests. [PR Name=SM:DNPMU1]
2	Runs Group E DCTU tests. [PR Name=SM:DNPMU2]
3	Runs Group F DCTU tests. [PR Name=SM:DNPMU3]
4	Runs Group G, Series A through I - DCTU tests. [PR Name=SM:DNPMU4]
5	Runs Group G, Series J through O - DCTU tests. [PR Name=SM:DNPMU5]

Table 5.3-74 Diagnostic Phase Descriptions for PROTO

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests operation of the protocol circuit to a termination circuit. [PR Name=SM:DNPROTO]

Table 5.3-75 Diagnostic Phase Descriptions for PSUCOM

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the PICB communication between the CI and the UCI chip on the CF. [PR Name=SM:DNUCI]
2	Tests the UCI chip on the CF. [PR Name=SM:DNUCI]
3	Tests the LP of the CFs UCI chip. The SMP sends messages for the LP, and when the LP sees the messages, performs the required reads and writes (to verify interrupts to the LP). [PR Name=SM:DNUCI]
4	Tests the CFs LP ESRs and CRC in ROM. [PR Name=SM:DNPS1]
5	Tests the CIB between the CF, PF, and DF. [PR Name=SM:DNPS1]
6	Tests the PB between the CF, the PF, and PI. [PR Name=SM:DNPS1]
7	*(Demand phase for factory and growth testing only.)* Tests all DUARTS in the CF for unequipped shelves. [PR Name=SM:DNPS1]
8	*(Demand phase for factory and growth testing only*.) Tests the internal CF interfaces to all unequipped PFs.

	[PR Name=SM:DNPS1]
9	*(Demand phase for factory and growth testing only.)* Tests the OOS lamps on equipped and growth CFs, PFs, and DFs. The diagnostic cycles through five times, starting by turning all lamps off. [PR Name=SM:DNPS1]
10	Tests the CF2 polling RAM, arbiter, and packet bus between the active and mate PIs via the CF2. (Only executed with the PSU/CF2 pack.)
11	Tests the communication between the CI and the PF. [PR Name=SM:DNPS2]
12	Tests the LPs ROM and the ability of the PF to be reset. [PR Name=SM:DNPS2]
13	Tests the communication between the PF and each of the equipped and growth PHs. [PR Name=SM:DNPS2]
14	Tests the packet arbiter and the packet bus connections through the PF to each equipped PH. [PR Name=SM:DNPS2]
15	*(Demand phase for factory and growth testing only.)* Tests the internal communication path on the PF for each unequipped PH. [PR Name=SM:DNPS2]
16	*(Demand phase for factory and growth testing only.)* Tests the internal communication path on the PF for each unequipped PH. [PR Name=SM:DNPS2]
21	Tests the communication path between the CI and DF via the CF. [PR Name=SM:DNPS3]
22	Tests the LPs ROM for the ability of the DF to be reset. [PR Name=SM:DNPS3]
23	Performs reads and writes on the DFs 8751 bus. [PR Name=SM:DNPS3]
24	Provides a memory test for the DFs parity error buffer. [PR Name=SM:DNPS3]
25	Performs a test on the DFs TSI chip. [PR Name=SM:DNPS3]
26	Tests the data paths on the DF. [PR Name=SM:DNPS4]
27	*(Demand phase for factory and growth testing only.)* Tests the data paths between the DF and the STBY common data board via the DPIDBs. [PR Name=SM:DNPS4]
28	Tests the PLI associated with any DF2 equipped in the PSUCOM under test.
29	Tests the DFTS and PCTLI devices resident on the DF2 circuit pack.
30	Test interdevice connections, timing circuitry and PHDB connections from a DF2 to equipped PHs.

Table 5.3-76 Diagnostic Phase Descriptions for PSUPH

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the interface between the ACT PF and PH under test (TN1081 or TN1367). This includes the CB, and the CB and PB leads. [PR Name=SM:DNPH1]
2	Tests the port processor side of the PH board. [PR Name=SM:DNPH1]
3	Tests the HDLC processor of the PH under test. [PR Name=SM:DNPH1]
4	Tests the DMA processor interfacing with the active and standby PSUCOM. Also, tests the PHDB bus from the PH under test to the active DF and for the TN1366, also test to the standby DF. [PR Name=SM:DNPH2]
5	Tests the interfaces between the STBY PF and PH under test. [PR Name=SM:DNPH2]
90	*(Demand phase only.)* Tests the full range of memory using a high coverage memory algorithm. [PR Name=SM:DNPH2]
91	*(Demand phase only.)* More exhaustive test of the SPORT chips on the TN1081 circuit pack. [PR Name=SM:DNPH2]
92	*(Demand phase only.)* Runs the same test sequences as phase 2 except each sequence is run as a separate segment to provide more data on failures. This phase is expected to be used primarily in the factory where the additional data may help in component-level fault isolation. This phase only applies to a TN1367 PH, a request for it on a TN1086 PH produces an NTR result. [PR Name=SM:DNPH2]
93	*(Demand phase only.)* Runs the same test sequences as phase 3 except each sequence is run as a separate segment to provide more data on failures. This phase is expected to be used primarily in the factory where the additional data may help in component-level fault isolation. This phase only applies to a TN1367 PH, a request for it on a TN1086 PH produces an NTR result. [PR Name=SM:DNPH2]

Table 5.3-77 Diagnostic Phase Descriptions for PSUPH-ATM

PHASE	DESCRIPTION/WHAT IS TESTED [a]
1	Tests the common portions of PBC core40 type circuit packs used in the PSU2. Tests are as follows: Verifies that communication to a PI from SMP is good. Verifies that initial pump of PBC is done. Tests ROM resident memory. Tests interfaces from PSU to PBC. Tests interfaces from PSU to PBC. Runs RAM resident tests of the PBC core.
2	Tests the AMEX as follows: Runs BIST on both the AMEX and on its associated SRAM. Verifies communication between the AMEX and PBMACs. Checks AMEX capability to process cells into packets, and vice-versa, in the various transmit modes. Verifies OAM cell processing. Verifies AMEX ABORT capability.

	Checks AMEX scrubbing function and its capability to compose packets out of a mixed stream of cells. Tests packet bus holdoff capability and remaining registers.
3	Tests the TERMINATOR and TRAC as follows: Verifies functionality of the TRAC. Verifies BIST on the TERMINATOR SRAM. Verifies TERMINATOR-AMEX interface. Checks TERMINATOR's cell transmission ability. Tests TERMINATOR registers. Runs different segments, depending on whether the PHA under test is in point-to-point or central stage ATM-fabric configuration.
4	Tests the PHDB interface and SPI device as follows: Self-tests (BIST) STP device. Tests PHDB interface. Checks SOH/POH manipulations. Verifies PHDB-SOH/POH data interchangeability.
5	*(Demand phase only - Due to optical link instability.)* Causes all tests to be run on the terminator.
6	*(Demand phase only - Due to optical link instability.)* Cause all tests to be run on the terminator. This phase is intended for PHA growth and the optical transmitter to be fiber-optic looped to the optical receiver on the backplane-mounted optical paddle board. If no signal is present on the optical receiver, this phase fails.
	Notes: a. PSUPH PHA (Secure Feature - SFID 224)

Table 5.3-78 Diagnostic Phase Descriptions for PSUPH-VOICE

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the common portions of PBC core40 type circuit packs used in the PSU2. Tests are as follows: Verifies that communication to a PI from SMP is good. Verifies that initial pump of PBC is done. Tests ROM resident memory. Tests interfaces from PSU to PBC. Runs RAM resident tests of the PBC core.
2	Sends messages to the resident code to execute tests on the vocoders and visa devices. Also, tests the visamux device (PHV4) to verify its capabilities and interfaces.
3	Tests the "voice path" of the PHV. Signals are sent to the vocoders compressed and uncompressed by the same vocoder and the return signal is measured.
4	*(Demand phase only.)* This test is run to give more details of phase 1 failures.

Table 5.3-79 Diagnostic Phase Descriptions for RAF

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests CI with ACT and STBY MCTSI. Completes ATP if STBY MCTSI is OOS. [PR Name=SM:DNUCI]
2	Tests the internal functions of the UCI chip on the LDSU. [PR Name=SM:DNUCI]
3	Tests the LP-UCI interface. [PR Name=SM:DNUCI]
4	Tests LDSU bus interface to DSU2. [PR Name=SM:DNDSU2]
5	Performs LP tests - interrupt controller, timers, parity, and write protect. [PR Name-SM:DNDSU2]
6	Tests DSPs, SDI, and data to/from LDSU bus. [PR Name=SM:DNDSU2]
7	Tests RAF memory. [PR Name=SM:DNDSU2]
8	Performs memory test. [PR Name=SM:DNDSU2]

Table 5.3-80 Diagnostic Phase Descriptions for RAU

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the entire RAU in the RSM. [PR Name=SM:DNRAU]

Table 5.3-81 Diagnostic Phase Descriptions for RCLK

PHASE	DESCRIPTION/WHAT IS TESTED
1	Performs CLRT tests. [PR Name=SM:DN2NC1]
2	Performs CCB tests. [PR Name=SM:DN2NC2]
3	Performs controller and oscillator tests. [PR Name=SM:DN2NC3]
4	Performs synchronizer board tests. [PR Name=SM:DN2NC4]
5	Performs DPLL and clock performance tests. [PR Name=SM:DN2NC5]

Table 5.3-82 Diagnostic Phase Descriptions for RLI

PHASE	DESCRIPTION/WHAT IS TESTED
1	ACT MP to DLI communication and interface tests. [PR Name=SM:DNPDLI1]
2	Performs DLI internal function tests (I). [PR Name=SM:DNPDLI1]
3	Performs DLI internal function tests (II). [PR Name=SM:DNPDLI1]
4	ACT CI to FIU communication tests (TN835 and TN618). [PR Name=SM:DNFIU1]
5	STBY CI to FIU communication tests (TN835 and TN618).[PR Name=SM:DNFIU2]
6	ACT TSI to DLI interface tests. [PR Name=SM:DNPDLI2]
7	STBY MP to DLI interface tests. [PR Name=SM:DNPDLI2]
8	STBY MP SDLC to DLI interrupt and data tests. [PR Name=SM:DNPDLI2]
9	STBY TSI to DLI interface (data loop back) tests. [PR Name=SM:DNPDLI3]
10	Power switch/monitor tests. [PR Name=SM:DNPDLI3]
13	Performs the FIU clock circuitry and controller board tests (TN835 and TN618). [PR Name=SM:DNFIU2]
14	Performs the FIU - link A tests (TN834). [PR Name=SM:DNFIU3]
15	Performs the FIU - link B tests (TN834). [PR Name=SM:DNFIU3]
16	Performs the FIU - MUX A tests (TN619). [PR Name=SM:DNFIU4]
17	Performs the FIU - MUX B tests (TN619). [PR Name=SM:DNFIU4]

Table 5.3-83 Diagnostic Phase Descriptions for RRCLK

PHASE	DESCRIPTION/WHAT IS TESTED
1	Checks CI/CLRT through DFI - RCLK PICB, CCB, microprocessor talk back and sanity timer. Diagnostics are resident in the R1DFI firmware. [PR Name=SM:DNRRCLK]
2	Runs RCLK diagnostics that are resident in the RCLK firmware. The RAM and EPROM, the control latches, reference phase registers, DCO, clock generator, and interrupts are checked. [PR Name=SM:DNRRCLK]
3	Tests the RCLK energy detector circuitry with diagnostics resident in RCLK firmware. Also tests clock's reference from each R1DFI and XCPL wire connecting RCLKs. [PR Name=SM:DNRRCLK]

Table 5.3-84 Diagnostic Phase Descriptions for RUCI

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests CI with ACT and STBY MCTSI. If STBY MCTSI is OOS, then CATP completes. [PR Name=SM:DNRUCI]
2	Tests the internal functions of the UCI chip on the LDSU. [PR Name=SM:DNRUCI]
3	Tests the LP-UCI interface. [PR Name=SM:DNRUCI]

Table 5.3-85 Diagnostic Phase Descriptions for RVPT

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests failure alarm circuits on the RVPT board. [PR Name=SM:DNRPT1]
2	Tests TSSR of RVPT pack. [PR Name=SM:DNRPT1]
3	Tests the parity checker and parity generator of the RVPT. [PR Name=SM:DNRPT1]
4	Tests the summary scan register on the RVPT. [PR Name=SM:DNRPT2]
5	Performs run on-board self tests, test overflow bit, and test I/O address and data leads. [PR Name=SM:DNRPT2]
6	Performs loop test calls through RVPT pack. [PR Name=SM:DNRPT2]

Table 5.3-86 Diagnostic Phase Descriptions for SAS

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies control interface with active and mate MCTSI. Will CATP if mate MCTSI is OOS. [PR Name=SM:DNuci_1]
2	Verifies all functions of the SASDSC UCI device that are accessible from the MCTSI. [PR Name=SM:DNuci_2]
3	Tests the SASDSC LP-UCI interface. The diagnostic code is downloaded to the SASDSC via the PICB. [PR Name=SM:DNuci_3]
4	Tests all the hardware components of the SASDSC. [PR Name=SM:DNdsc3_4]
5	Tests SAS memory. [PR Name=SM:DNsas_5]
6	*(Demand phase only.)* Tests the programmability of each of the SASMEM flash cards. [PR Name=SM:DNsas_6]

Table 5.3-87 Diagnostic Phase Descriptions for SCAN

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the MSU scan pack with exception of actually closing the scan points. [PR Name=SM:DNSCAN]
2	*(Demand phase only.)* Tests low state of scan points with no backplane connections. [PR Name=SM:DNSCAN]

Table 5.3-88 Diagnostic Phase Descriptions for SDFI

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests CI/CLRT integrity. [PR Name=SM:DNDFIS1]
2	Tests CCB integrity. [PR Name=SM:DNDFIS1]
3	Tests □C integrity. [PR Name=SM:DNDFIS1]
4	Tests maintenance buffer integrity. [PR Name=SM:DNDFIS2]
5	Tests LSI exercises I. [PR Name=SM:DNDFIS3]
6	Tests LSI exercises II. [PR Name=SM:DNDFIS3]
7	Tests facility alarm clock. [PR Name=SM:DNDFIS3]
8	Tests TSI integrity. [PR Name=SM:DNDFIS4]
9	Tests signaling and PCM data path test. [PR Name=SM:DNDFIS4]

Table 5.3-89 Diagnostic Phase Descriptions for SFI (DNU-S)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the Internal Control Bus (ICB) from both CCs to the SFI, PCI device, the ability to read and write the general registers, the ability to detect PCIBUS errors, and the operation of each SFI reset mode. [PR Name=SM2K:DNUSSFI1]
2	Tests the TSCs, drivers, encoders, receivers, upstream LOS detectors, upstream spare selection and early loopbacks to the spare and service TMUXs. Contains one task dedicated to duplicating the tests performed under PIST. This allows any PIST failures to be reproduced by OOS diagnostics. [PR Name=SM2K:DNUSSFI1]
3	Tests the upstream and downstream relays, downstream LOS, SLI LOS, facility loopback capability, and the SLIs. If the mate SFI is not active, the SLI and second downstream relay (D2) tests are skipped and the phase completes CATP. [PR Name=SM2K:DNUSSFI1]
9	Tests the upstream relay, secondary downstream relay, the service TIDB and the facility loopback capability for facilities in the GROW state using an external loopback manually applied to the SLI. [PR Name=SM2K:DNUSSFI1]

Table 5.3-90 Diagnostic Phase Descriptions for SLIM

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests: The interface between the MSUCOM circuit pack and the SLIM2 The ability to read/write SLIM2 registers The ability to generate/mask service requests and all seems well operation The four FIFO stacks The control FPGA (field programmable gate array) operation. [PR Name=SM:DN2SLM01]
2	*(Demand phase only.)* Tests microprocessor-related hardware like: RAM Pump RAM ROM Sanity timer. [PR Name=SM:DN2SLM02]
3	*(Demand phase only.)* Tests the DSP and DSP-related hardware like the RAM and FPGA interfaces. Background exercises are run on the DSP and microprocessor for a period of time. [PR Name=SM:DN2SLM03]
4	Tests the analog hardware on the SLIM2 circuit pack. Similar to a linesman calling the SLIM2 self-test, but runs more detailed tests to obtain more information about the nature of the defect. [PR Name=SM:DN2SLM04]
5	Uses the SLIM2 to perform a number of functional tests on the test termination on the SLIM2. Line capacitance, distance to open foreign voltage, line insulation, and dial pulse distortion are checked. [PR Name=SM:DN2SLM05]
6	Tests the operation of the four junctor access relays. Each junctor will be connected to the protocol circuit on the common board.[PR Name=SM:DN2SLM06]

Table 5.3-91 Diagnostic Phase Descriptions for TAC

PHASE	DESCRIPTION/WHAT IS TESTED
1	Seizes CDI and finds ACT data side. Interconnects loop outgoing and incoming test circuits, normal battery loop open, and E&M signaling test. Trunk access network is tested in groups of four. Facility test network is tested. [PR Name=SM:DNTAC]
2	Tests initialization of the T&A destination register and analog termination segment. The D/A converters are tested; the test reference and detector are tested; and a test for shorts between the maintenance leads is performed. [PR Name=SM:DNTAC]

Table 5.3-92 Diagnostic Phase Descriptions for TEN/TUCHBD

PHASE	DESCRIPTION/WHAT IS TESTED
1	Performs signaling test for the trunk circuit under test (for example, SN102, SN103, SN104, SN105, etc.). [PR Name= [a]]
2	Performs transmission tests of the trunk circuit. Verifies correct operation of the CODEC, filter, and transformer. Completes CATP if either the STBY MCTSI or the TTFCOM is OOS. [PR Name= [a]]

Notes:

a. The PR having listings for phases 1 and 2 depends on the type of trunk.

Where:

PR NAME = TRUNK TYPE

SM:DNLIN = Loop Start Input
SM:DNLOUT = Loop Start Output
SM:DN2EM = 2-Wire E & M
SM:DN4EM = 4-Wire E & M
SM:DNTLI = Toll Loop Start Input
SM:DNTLO = Toll Loop Start Output
SM:DNT2EM = Toll 2-Wire E & M
SM:DNT4EM = Toll 4-Wire E & M
SM:DNTST = Test Trunk

Table 5.3-93 Diagnostic Phase Descriptions for TMUX (DNU-S)

PHASE	DESCRIPTION/WHAT IS TESTED
1	Verifies the ICB interface (physical connection) from the CC to the TMUX. The ICB interface circuits (parity check, start code check, ability to force ASW errors) and the ability of the mate CC to access the TMUX are verified. [PR Name=SM2K:DNUSTX1]
2	Verifies that all functions in the UCI on the TMUX that are accessible via the CC. This includes the FIFO circuitry. RAM, RAM parity checker/generation, and summary scan/error source/mailbox/mask registers. [PR Name=SM2K:DNUSTX1]
3	Verifies the TMUX interface to the UCI. This includes the summary scan interrupts and masks, access to registers and interrupts in the hardware ESR for errors on the TMUX accesses. [PR Name=SM2K:DNUSTX1]
4	Verifies the microprocessor-related circuitry on the TMUX including byte enables, timers, maskable interrupts and priority encoder, sanity timer, NMI circuitry, bus error circuitry, I/O write protection. RAM write protection, data parity checkers/generators and on-chip cache. [PR Name=SM2K:DNUSTX1]
9	Verifies the RAM on the TMUX. [PR Name=SM2K:DNUSTX1]
11	Verifies the individual SONET devices for read/write parity and protocol errors and the connections of the STS-1 level devices to the VT level devices. Devices that have a built-in, self-test (BIST) are also run. [PR Name=SM2K:DNUSTX2]
12	Verifies the transmission of SONET payloads through the SONET devices on the TMUX. The C1 overhead byte is used first to verify basic connections between devices. Then, different payloads with different signaling modes are looped through both the transmit and receive portions of each device and verified for accuracy. [PR Name=SM2K:DNUSTX2]
14	Verifies the BPIB connections to the CD packs and the TDIB connections to the SFI packs. Parity generation/checking is verified for each link. [PR Name=SM2K:DNUSTX2]

Table 5.3-94 Diagnostic Phase Descriptions for TTFCOM

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests failure alarm and system maintenance functions associated with the interface board.

	[PR Name=SM:DNTFC1]
2	Tests failure alarm and system maintenance functions associated with the processor board. [PR Name=SM:DNTFC1]
3	Tests failure alarm and system maintenance functions associated with the tone generator Digital Signal Processor (DSP) board (TN304 or TN304B). [PR Name=SM:DNTFC1]
4	Tests failure alarm and maintenance functions associated with the measurement. The DSP board fails if the dip switches on TN304 or TN304B are configured incorrectly. [PR Name=SM:DNTFC1]
7	Tests parity check circuit on the interface board. [PR Name=SM:DNTFC1]
8	Tests firmware's ability to generate a summary scan interrupt. [PR Name=SM:DNTFC2]
9	Tests write/read of the firmware's pseudo Time Slot Select Register (TSSR). [PR Name=SM:DNTFC2]
10	Tests parity generator. [PR Name=SM:DNTFC2]
11	Tests the reset function and verifies the TTF's reports. [PR Name=SM:DNTFC2]
12	Tests the TTF tone sources - looped back to the TTF responder. Dummy test - if the CLI is equal to 0. [PR Name=SM:DNTFC2]
13	Tests send and receive paths of each responder and PTC tone detector in the TTF. Dummy test - if the CLI is equal to 0. [PR Name=SM:DNTFC2]
14	Tests AGC function of the PCT tone detector and the operation of the CDA tone detector. Dummy test - if the CLI is equal to 0. [PR Name=SM:DNTFC2]
15	Tests receive path of each TT test function in the TTF. Dummy test - if the CLI is equal to 0. [PR Name=SM:DNTFC2]

Table 5.3-95 Diagnostic Phase Descriptions for UCONF

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests failure alarm circuits. [PR Name=SM:DNCONF1 (for 3-port) or SM:DN6CONF1 (for 6-port)]
2	Test the TSSRs. [PR Name=SM:DNCONF1 (for 3-port) or SM:DN6CONF1 (for 6-port)]
3	Tests the parity checker. [PR Name=SM:DNCONF1 (for 3-port) or SM:DN6CONF1 (for 6-port)]
4	Tests the parity generator. [PR Name=SM:DNCONF2 (for 3-port) or SM:DN6CONF2 (for 6-port)]
5	Performs functional tests, using static data sent from the TSI alternate data RAM. [PR Name=SM:DNCONF2 (for 3-port) or SM:DN6CONF2 (for 6-port)]

Table 5.3-96 Diagnostic Phase Descriptions for UTD

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests failure alarm circuits associated with the UTD. [PR Name=SM:DNCUTD1]
2	Tests the TSSR. [PR Name=SM:DNCUTD1]
3	Tests the parity checker. [PR Name=SM:DNCUTD1]
4	Tests SSR, tone decoder, and read and write control registers. [PR Name=SM:DNCUTD2]
5	Performs functional tests with tones from the UTG looped back to the UTD. [PR Name=SM:DNCUTD2]

Table 5.3-97 Diagnostic Phase Descriptions for UTG

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests the failure alarm circuits. [PR Name=SM:DNUTG1]
2	Tests the TSSR. [PR Name=SM:DNUTG1]
3	Tests the parity generator. [PR Name=SM:DNUTG1]

5.4 COMMON NETWORK INTERFACE

5.4.1 INTRODUCTION

This section describes the Common Network Interface (CNI) ring in the *5ESS*® switch. There are several CNI configurations in each of its two technologies: Small Scale Integration (SSI) and Integrated Ring Node Version 2 (IRN2). The SSI technology has been the standard for all installing rings. The new IRN2 technology was deployed which provides higher reliability and more link terminations. Figure 5.4-1 shows the topology of a typical SSI-based ring.

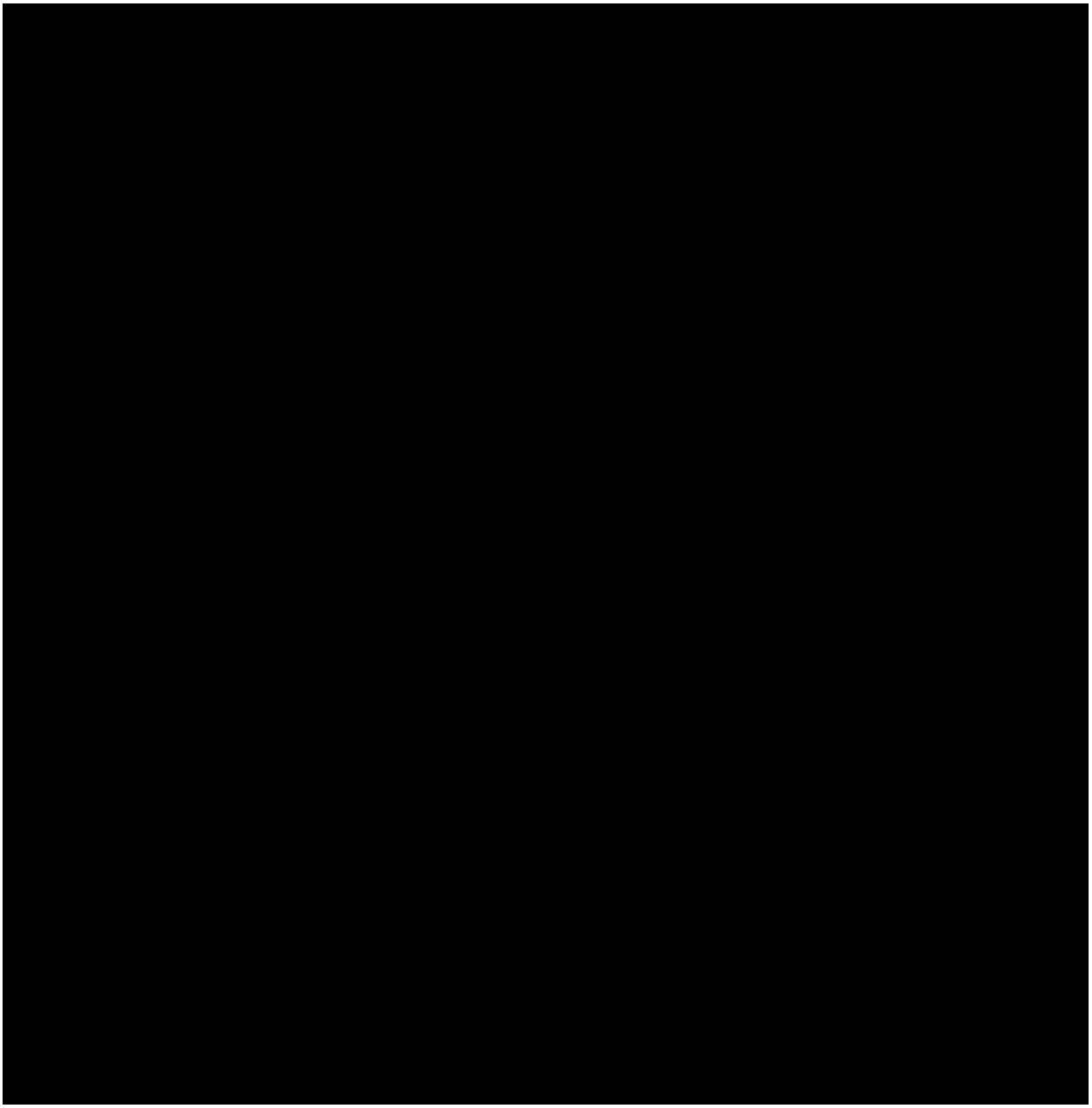

Figure 5.4-1 SSI CNI Configuration

Refer to 235-200-115, *5ESS*®*Switch CNI Common Channel Signaling* for information about the *5ESS*® switch application of Common Channel Signaling (CCS) on the CNI.

For diagnostic execution input message and POKE command source information, refer to the following IPs:

- 235-105-110, *System Maintenance Requirements and Tools*
- 235-105-210, *Routine Operations and Maintenance Procedures*
- 235-105-220, *Corrective Maintenance Procedures*
- 235-600-700, *Input Message Manual*
- 235-600-750, *Output Message Manual*.

5.4.2 SSI RING NODE CABINET

The Ring Node Cabinet is a single cabinet containing a power panel, control panel, shelves for ring nodes, and a fan assembly. There are two types of SSI cabinets. The J3F011C-1 is the original cabinet used for installing offices. The latest cabinet, J3F011C-2, uses the same shelving arrangements but has a different fan unit and alarming capabilities. The following text and figures show the J3F011C-1.

The cabinet is divided into two groups, ring groups 00 and 32, which must be configured identically to provide redundancy.

There are only two types of shelves provided for ring node assignment: J3F011AA and J3F011AC.

There can be up to six shelves equipped, shelves 0-5, configured as follows:

- Shelf positions zero and three always contain a J3F011AA shelf, normally equipped with one Ring Peripheral Controller Node (RPCN) and one Link Node (LN).
- Shelf positions one and four may contain an optional J3F011AA shelf, equipped to hold one Direct Link Node (DLN) and one LN.
- Shelf positions two and five may contain an optional J3F011AC shelf, equipped with three LNs numbered from right to left.

Power is fed to each shelf-mounted node through the J5D003AU-02 fuse/filter panel and is controlled by a 495 FA converter provided for each node except for LN5 which is controlled by packs adjacent to LNs 4 and 6.

A 3-fan assembly is mounted at the bottom of the cabinet for equipment ventilation.

Figure 5.4-2 illustrates a fully equipped CNI cabinet and how the shelves are configured with the optional DLN configurations.

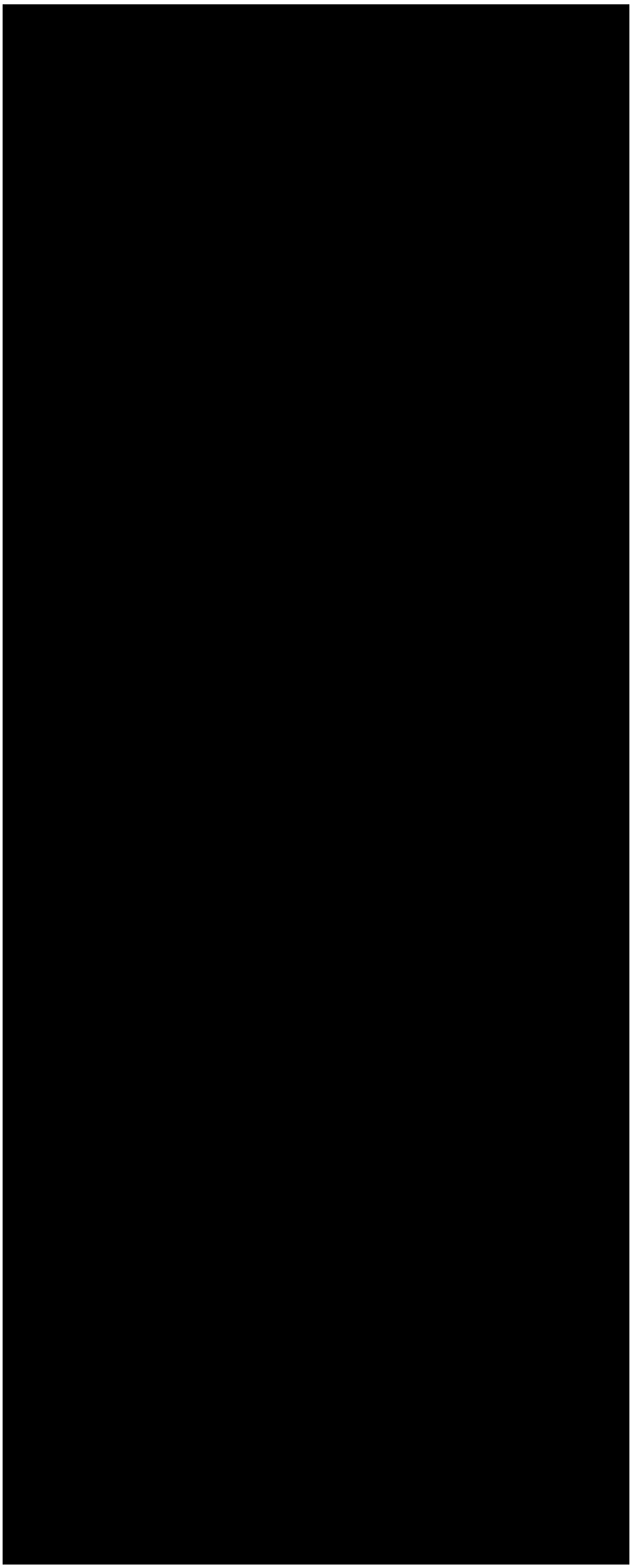

Figure 5.4-2 Fully Equipped SSI CNI Cabinet with Optional DLNs

5.4.3 SSI CNI NODES

Only three kinds of CNI nodes are available for the *5ESS*® switch. There is an optional fourth ring processing node to provide for increased Common Channel Signaling (CCS) capacity requirements. The nodes are described as follows:

- **Ring Peripheral Controller Node (RPCN):** Provides communication between the ring and the Administrative Module (AM). There is an RPCN placed in position 0 of each ring group. Two are always used in the *5ESS*® switch CNI application.

  The RCPN and its circuit packs are illustrated in Figure 5.4-3 .

- **Link Node (LN):** Provides communication between the CNI ring and the CCS network. The LN data speed can be 4.8 kb/s or 56 kb/s. These can be either encrypted or not encrypted. From 2 to 10 LNs can be used in the *5ESS*® switch CNI application.

  The LN and its circuit packs are illustrated in Figure 5.4-4 .

- **Interprocess Message Switch User Node (IUN):** This is not recommended for the *5ESS*® switch. This is an active node on the CNI ring, but it performs no signaling or processing. One use of the IUN, in the *5ESS*® switch application, is to electrically hold a place for a future DLN or LN and provide the foundation of common circuitry on which the DLNs or LNs are built. This avoids ring cabling at the time of growth. The IUN may control an adjacent interframe buffer that is used to connect ring nodes across a physical frame boundary; it is generally a temporary filler during growth or reduction periods. The IUN is not illustrated.

- **Direct Link Node (DLN):** The DLN, an optional node, is for *5ESS*® switches equipped with Communication Module Model 2 (CM2). The DLN relieves the AM of some signaling message processing to support greater CCS processing capacity. When DLNs are used, there are always two required for the *5ESS*® switch.

  The DLN and its circuit packs are illustrated in Figure 5.4-5 .

The *5ESS*® switch CCS7 capacity improvement - DLN30 capability was developed. This CCS7 capacity improvement increases the call capacity in the *5ESS*® switch by replacing the existing SSI nodes on the CNI ring with the newer technology IRNs.

With this capability, the DLN capacity no longer matched the capacity of the switch. Therefore a new DLN, DLN30 was developed. The DLN30 includes a *Motorola*® MC68030 processor and the IRN.

The capability requires a DLN-AP30 replacement for a DLN-AP and a conversion from an SSI-based technology to IRN technology for all the CNI nodes - DLNs, LNs, and RPCNs. It also requires a new IRN eight-node third shelf.

The following DLN30 hardware changes are required to support this feature:

- An AP30 processor board with the *Motorola*® MC68030 chip. It has 16 MB of fixed resident memory that cannot be reengineered.
- A single IRN2 circuit pack which has the current NP, RI0, and RI1 board functions.
- A 3B20D/3B21D Computer Interface (3BI) board.
- A Duplex Dual Serial Bus Selector (DDSBS) board.

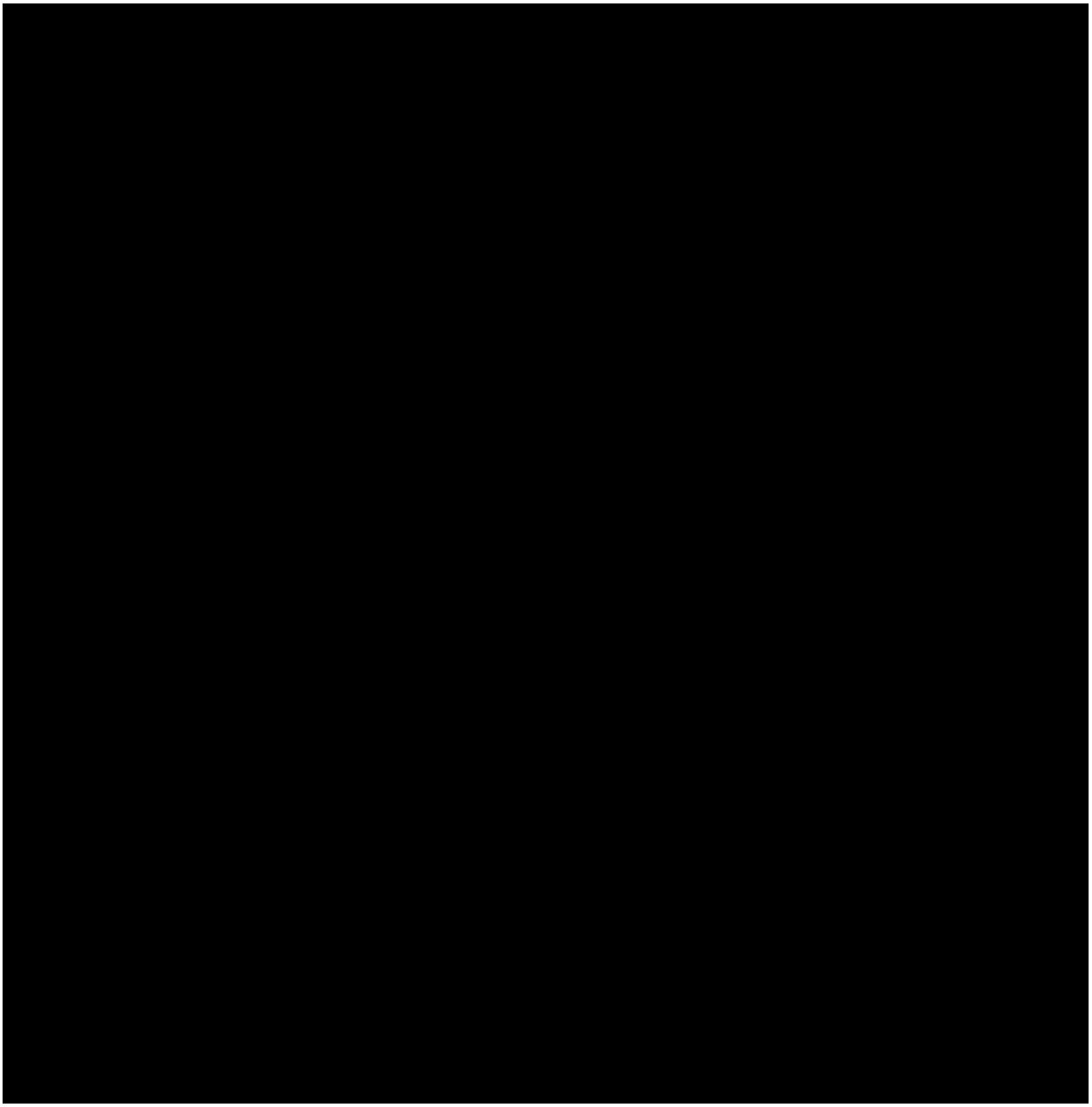

Figure 5.4-3 SSI Ring Peripheral Controller Node

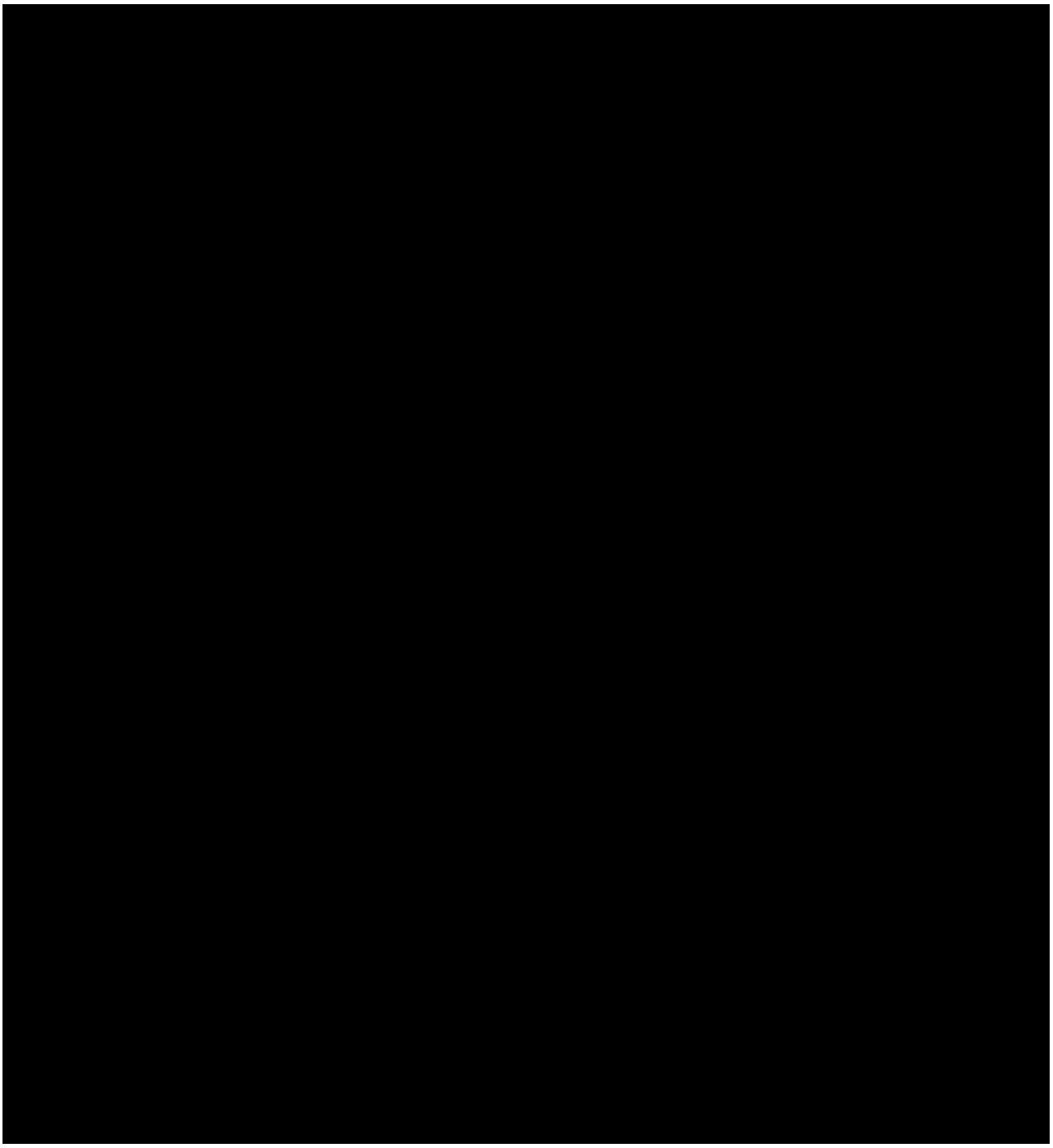

Figure 5.4-4 SSI Link Node

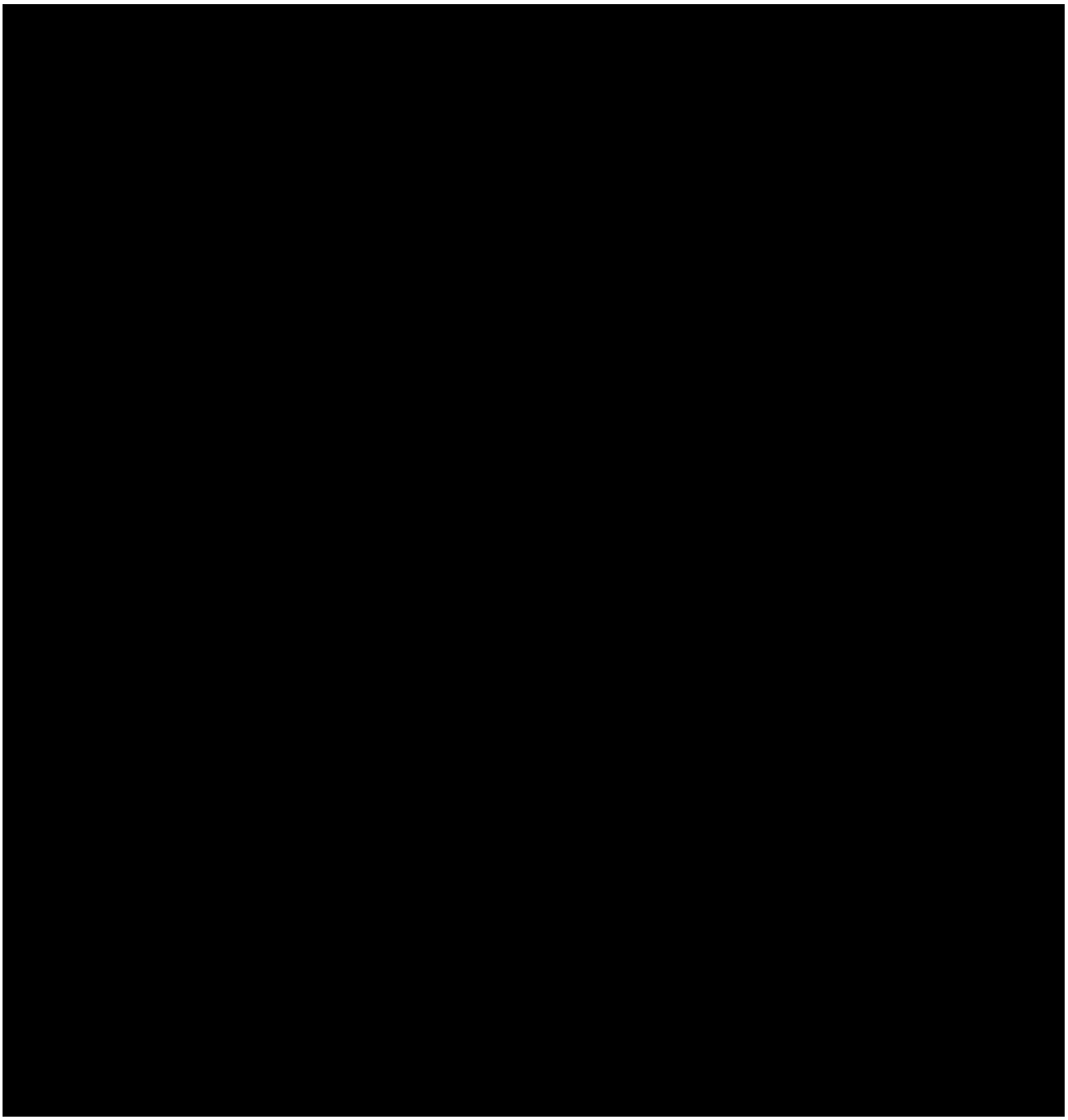

Figure 5.4-5 SSI Direct Link Node

5.4.4 IRN2 RING NODE CABINET

The ring node cabinet is a single cabinet containing a power panel, control panel, shelves for ring nodes, and fan assembly. The IRN2 ring is placed in the J3F011C-2 frame and is only available to offices.

The cabinet is divided into two halves, each containing three groups. Groups 00, 01, and 02 in one half, and groups 32, 33, and 34 in the other half. These two halves must be equipped identically for redundancy.

There are two types of shelves provided for this cabinet: J3F011GC and J3F011GD. The cabinet accommodates up to six shelves and is configured as follows:

- Shelf positions zero and four always contain the J3F011GD shelf. This shelf must have the RPCN and LN4 installed. It may have up to three Link Nodes (LNs) and one Direct Link Node (DLN).

- Shelf positions one, two, five, and six have the J3F011GC shelf. This shelf is optional and is needed only when the existing J3F011GD shelf has been filled. The J3F011GC shelf can contain up to eight LNs.

The Modular Fuse Filter Unit (MFFU) provides power to the cabinet and to the 410AA power converters. There are two power converters per shelf. On the J3F011GD the left-hand converter powers the RPCN and LN-1, while the right converter powers DLN2, LN3, and LN4. For the J3F011GC shelf, the power is split down the middle so that the left-hand converter powers nodes LN1 through LN4 and the right one powers LN5 through LN8. Figure 5.4-6 shows the J3F011GC shelf layout, and Figure 5.4-7 shows the J3F011GD shelf layout.

A six-fan assembly is mounted in the middle of the cabinet with three fans pulling air up for the lower three shelves and three fans pushing air up for the upper three shelves. Figure 5.4-8 illustrates a fully equipped IRN2 CNI cabinet and how the shelves are arranged.

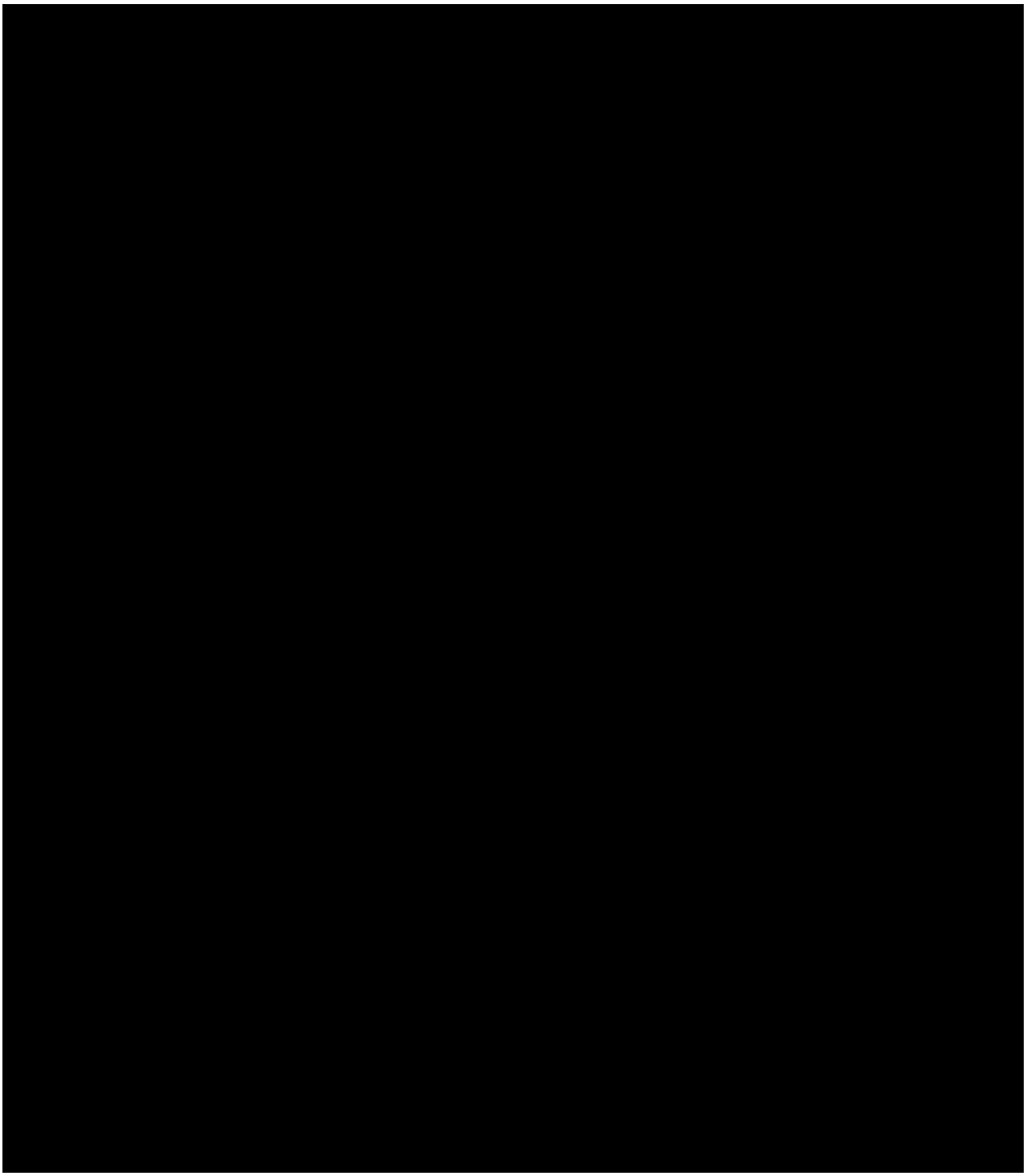

Figure 5.4-6 IRN2 J3F011GC Shelf Unit

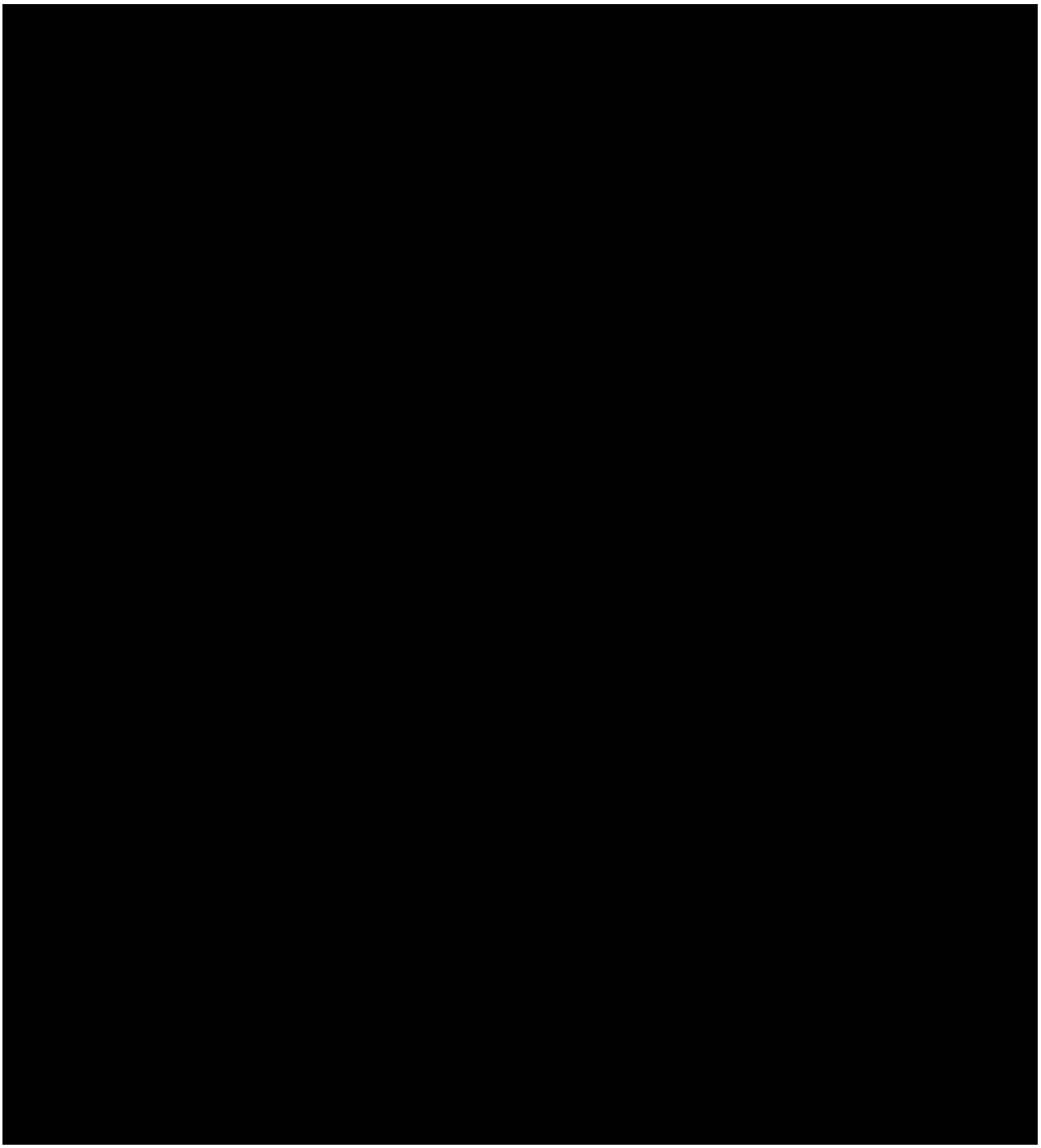

Figure 5.4-7 IRN2 J3F011GD Shelf Unit

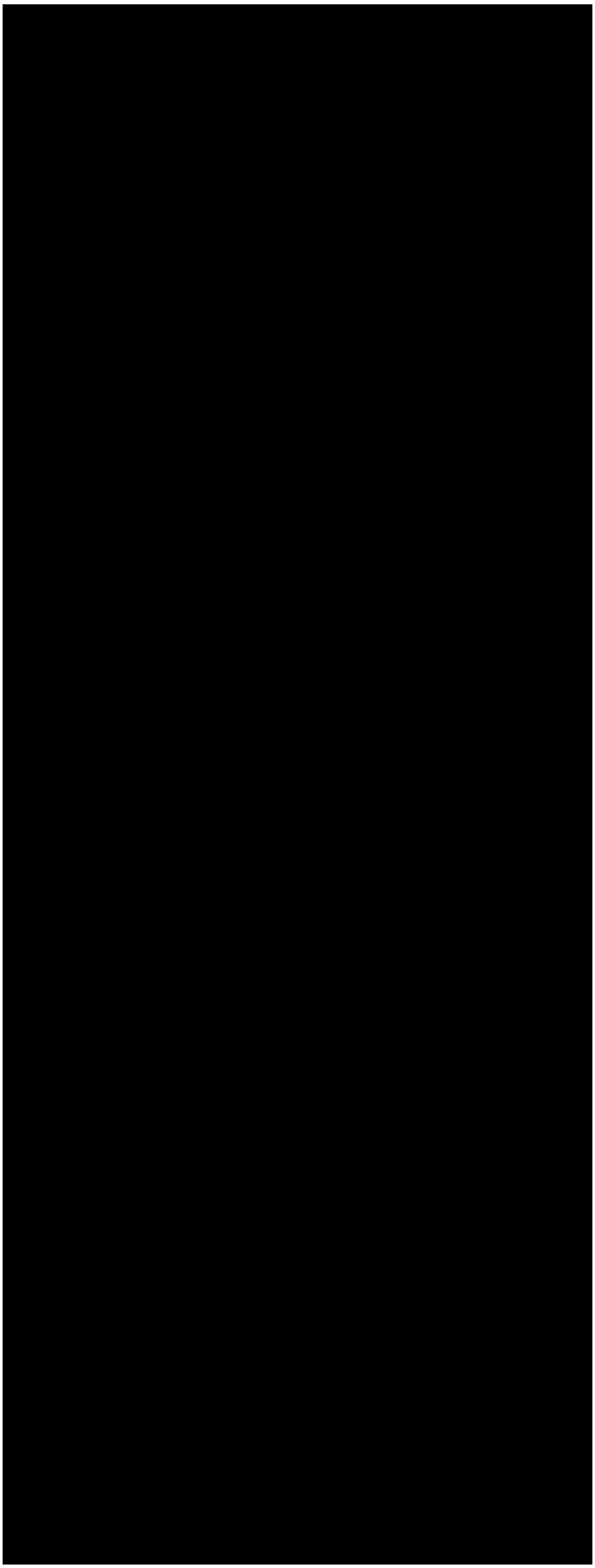

Figure 5.4-8 Fully Equipped IRN2 CNI Cabinet

5.4.5 IRN2 CNI NODES

There are four types of nodes available on the CNI ring. The nodes are described as follows:

- ***Ring Peripheral Controller Node (RPCN):*** There are only two RPCNs per CNI ring. These nodes provide the communication interface to the AM processor through the Duplex Dual Serial Bus Selector (DDSBS).
- ***Link Node (LN):*** The LNs provide communications to the CCS7 signaling. The IRN2 ring uses only TN916 CCS7 nonencrypted links, of which it can support 19 pair.
- ***IMS User Node (IUN):*** The IUN is used only as a ``place holder'' in a live ring to prevent recabling when added signaling capacity is expected in the future. In the SSI ring this was needed because of DLN growth. For IRN2 rings, it is only allowed in the LN-4 position on the J3F011GD shelf and only for rings which converted from SSI to IRN2.
- ***Direct Link Node (DLN):*** The DLN is used to handle CCS7 call processing instead of the AM. The DLN can handle several times the amount of traffic of the AM thus increasing office capacity. There are two DLNs (also known as DLN30s) in a ring. They are required if more than two pair of signaling links are to be installed but cannot be equipped with just one pair.

5.4.6 DIAGNOSTIC PHASE DESCRIPTIONS

This section contains the diagnostic phase descriptive information (in the form of tables) for the CNI hardware (units/circuits) of the *5ESS*® switch. The entries closely follow those used on the MCC display pages and input/output messages.

The entry [PR Name=*xxxxxxxx*] in the DESCRIPTION/WHAT IS TESTED column in a mnemonic reference to the appropriate diagnostic PR (program listing).

The following is a list of the diagnostic phase tables:

- Table 5.4-1 , Diagnostic Phase Descriptions for DLN
- Table 5.4-2 , Diagnostic Phase Descriptions for IUN
- Table 5.4-3 , Diagnostic Phase Descriptions for LN
- Table 5.4-4 , Diagnostic Phase Descriptions for RPCN

Table 5.4-1 Diagnostic Phase Descriptions for DLN

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests RI0 (UN122), RI1 (UN123), IFB-P (TN915), IFB (TN918), and ring bus cable. [PR Name=iun01.1]
2	Tests RI0 (UN122), RI1 (UN123), IFB-P (TN915), IFB (TN918), and ring bus cable. [PR Name=iun02.1]
10	Tests the NP (TN913/TN922), RI0 (UN122), and RI1 (UN123). [PR Name=iun10.1]
11	Tests the NP (TN913/TN922), RI0 (UN122), and RI1 (UN123). [PR Name=iun11.1]
12	Tests RI0 (UN122). CATP completes when more than one node is isolated. [PR Name=iun12.1]
13	Tests RI1 (UN123). CATP completes when more than one node is isolated. [PR Name=iun13.1]
20	Tests the NP (TN913/TN922). [PR Name=iun20.1]
23	Tests the NP (TN913/TN922). [PR Name=iun23.1]
24	Tests the NP (TN913/TN922). [PR Name=iun24.1]
26	Tests the NP (TN913/TN922). [PR Name=iun26.1]
27	Tests the NP (TN913/TN922). [PR Name=iun27.1]
30	Tests interface between the DSCH (UN9 at CU) and the DDSBS (TN69B). [PR Name=iun30.1]
31	Tests the DDSBS (TN69B) and the 3B20D interface (TN914). [PR Name=iun31.1]
32	Tests ability of NP (TN922) to lose sanity and set the interrupt request flag when the 3B20D interface (TN914) has an error. [PR Name=iun32.1]

33	Tests the interface between the 3B20D (TN914) and the NP (TN922). [PR Name=iun33.1]
34	*(Demand phase only.)* Off-line CU to DDSBS (TN69B) tests. [PR Name=iun34.1]
35	Cooperates with the 3B20D driver to test the DMA capability via the 3B20D interface (TN914). [PR Name=iun35.1]
40	Tests the AP (TN1340) Dual Port Memory from the NP side. [PR Name=iun40.1]
41	Tests the AP (TN1340) and sends the results back to the 3B20D computer. [PR Name=iun41.1]
42	Tests between DMA and 3B20D interfaces. [PR Name=iun42.1]

Table 5.4-2 Diagnostic Phase Descriptions for IUN

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests RI0 (UN122), RI1 (UN123), IFB-P (TN915), IFB (TN918), and ring bus cable. [PR Name=iun01.1]
2	Tests RI0 (UN122), RI1 (UN123), IFB-P (TN915), IFB (TN918), and ring bus cable. [PR Name=iun02.1]
10	Tests the NP (TN913/TN922), RI0 (UN122), and RI1 (UN123). [PR Name=iun10.1]
11	Tests the NP (TN913/TN922), RI0 (UN122), and RI1 (UN123). [PR Name=iun11.1]
12	Tests RI0 (UN122). CATP completes when more than one node is isolated. [PR Name=iun12.1]
13	Tests RI1 (UN123). CATP completes when more than one node is isolated. [PR Name=iun13.1]
20	Tests the NP (TN913/TN922). [PR Name=iun20.1]
23	Tests the NP (TN913/TN922). [PR Name=iun23.1]
24	Tests the NP (TN913/TN922). [PR Name=iun24.1]
26	Tests the NP (TN913/TN922). [PR Name=iun26.1]
27	Tests the NP (TN913/TN922). [PR Name=iun27.1]

Table 5.4-3 Diagnostic Phase Descriptions for LN

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests RI0 (UN122), RI1 (UN123), IFB-P (TN915), IFB (TN918), and ring bus cable. [PR Name=iun01.1]
2	Tests RI0 (UN122), RI1 (UN123), IFB-P (TN915), IFB (TN918), and ring bus cable. [PR Name=iun02.1]
10	Tests the NP (TN913/TN922), RI0 (UN122), and RI1 (UN123). [PR Name=iun10.1]
11	Tests the NP (TN913/TN922), RI0 (UN122), and RI1 (UN123). [PR Name=iun11.1]
12	Tests RI0 (UN122). CATP completes when more than one node is isolated. [PR Name=iun12.1]
13	Tests RI1 (UN123). CATP completes when more than one node is isolated. [PR Name=iun13.1]
20	Tests the NP (TN913/TN922). [PR Name=iun20.1]
23	Tests the NP (TN913/TN922). [PR Name=iun23.1]
24	Tests the NP (TN913/TN922). [PR Name=iun24.1]
26	Tests the NP (TN913/TN922). [PR Name=iun26.1]
27	Tests the NP (TN913/TN922). [PR Name=iun27.1]
40	Tests the NP (TN913/TN922), LI (TN916) - not encrypted, and LI (TN917) - encrypted. [PR Name=CBph40.1]
41	Tests the NP (TN913/TN922), LI (TN916) - not encrypted, and LI (TN917) - encrypted. [PR Name=CBph41.1]
47	Tests the NP (TN913/TN922), LI (TN916) - not encrypted, LI (TN917) - encrypted, and TN919 data sets and VFL. [PR Name=CBph47.1]
48	Tests the NP (TN913/TN922), LI (TN916) - not encrypted, LI (TN917) - encrypted, and TN919 data sets and VFL. [PR Name=CBph48.1]

Table 5.4-4 Diagnostic Phase Descriptions for RPCN

PHASE	DESCRIPTION/WHAT IS TESTED
1	Tests RI0 (UN122), RI1 (UN123), IFB-P (TN915), IFB (TN918), and ring bus cable. [PR Name=rpc01.1]
2	Tests RI0 (UN122), RI1 (UN123), IFB-P (TN915), IFB (TN918), and ring bus cable. [PR Name=rpc02.1]
10	Tests the DDSBS (TN69B), DSCH (UN9), and 3B20D interface (TN914). [PR Name=rpc10.1]
11	Tests the 3B20D interface (TN914) and DDSBS (TN69B). [PR Name=rpc11.1]
12	Tests the 3B20D interface (TN914), NP (TN913/TN922), RI0 (UN122), and RI1 (UN123). CATP when more than one node is isolated. [PR Name=rpc12.1]
13	Tests the NP (TN913/TN922) and 3B20D interface (TN914). CATP when more than one node is isolated. [PR Name=rpc13.1]
14	*(Demand phase only.)* Tests the DDSBS (TN69B) and the off-line DSCH (UN09). Completes CATP. [PR Name=rpc14.1]
20	Tests the NP (TN913/TN922). [PR Name=rpc20.1]
23	Tests the NP (TN913/TN922). [PR Name=rpc23.1]
24	Tests the NP (TN913/TN922). [PR Name=rpc24.1]
26	Tests the NP (TN913/TN922). [PR Name=rpc26.1]
27	Tests the NP (TN913/TN922). [PR Name=rpc27.1]
30	Tests the NP (TN913/TN922), RI0 (UN122), and RI1 (UN123). [PR Name=rpc30.1]
31	Tests the NP (TN913/TN922), RI0 (UN122), and RI1 (UN123). [PR Name=rpc31.1]
32	Tests the RI0 (UN122). [PR Name=rpc32.1]
33	Tests the RI1 (UN123). [PR Name=rpc33.1]

6. POWER DISTRIBUTION

6.1 DESCRIPTION

The Power Control Fuse Distribution (PCFD) provides primary power distribution (-48 V DC to all cabinets in the *5ESS*® switch) from whatever source is established.

Secondary distribution (-48 V DC to individual units within cabinets) is provided through cabinet fuse and filter panels to the various units.

Circuits within the units convert the input voltage to the various levels required for system operations (tertiary distribution).

It is a general practice to supply duplicated system components within the switch with power from separate buses to establish independent power supplies for operating reliability.

Secondary power distribution in the Administration Module (AM) is unlike that in the Communication Module (CM) and Switching Module (SM). The AM contains a Power Distribution Unit (PDU) for extra control and protection, while the CM and SM filter and fuse panels distribute the fused power routinely.

Figure 6-1 illustrates the PCFD power distribution.

CAUTION: When performing maintenance procedures on, or affected by, the PCFD, maintenance personnel MUST be alert to any effects on switch operation integrity. Do not attempt ``short cut'' maintenance procedures. Refer to Information Products (IPs) that provide detailed procedures for Routine Maintenance (235-105-210), Corrective Maintenance (235-105-220), and System Recovery (235-105-250).

Figure 6-1 PCFD or GPDF Power Distribution

6.2 POWER DISTRIBUTION FRAME - J86334D-1

The Power Distribution Frame (PCFD) provides redundant, protected direct current to power the switch. The PCFDF receives its power from two to four independent buses terminated at the back of PCFD frame.

The PCFD contains a control panel and from one to four distribution panels. The distribution panels may consist of any combination of fuse panels (pop-up type or high-current type).

Figure 6-2 illustrates a typical PCFD and its components.

The control panel contains an alarm circuit module, two alarm circuit module protection fuses, a charge circuit protection fuse, and a capacitor charge circuit with a charging probe.

A pop-up fuse panel has 48 load fuse positions and associated alarm-indicating fuses and an energy storage capacitor bank (three capacitors per bus) to minimize voltage transients after load fuse operations.

Figure 6-2 illustrates the control panel and a pop-up fuse panel.

When a blown fuse is to be replaced, the power supply capacitor associated with the blown fuse must be charged before a new fuse is installed. Charging the capacitor prevents a sudden high-current surge which may blow the new fuse immediately.

A high-current fuse panel has eight load fuse positions and associated alarm indicating fuses (four load and four alarm indicating per bus) and a filter capacity bank (three capacitors per bus).

Figure 6-3 illustrates the high-current fuse panel.

Figure 6-2 Power Distribution Frame

Figure 6-3 High-Current Fuse Panel

6.3 GLOBAL POWER DISTRIBUTION FRAME - J86334E-1

The Global Power Distribution Frame (GPDF) provides redundant, protected direct current to power the *5ESS*® switch. The GPDF receives its power from two to eight independent buses that are terminated at the back of the GPDF.

Figure 6-4 illustrates a typical GPDF and its components.

A WP92955 (ED83133-30) fuse panel has 48 load fuse positions and associated alarm-indicating Light Emitting Diodes (LEDs) and an energy-storage capacitor bank (two capacitors per bus) to minimize voltage transients after load-fuse operations.

Figure 6-5 shows the alarm panel and WP92955 fuse panel.

Note that when a blown fuse has to be replaced that the power supply capacitor associated with the blown fuse does **not** have to be charged before a new fuse is installed. The GPDF and WP92955 fuses are specially designed to withstand inrush currents.

A high-current fuse panel has eight load fuse positions and associated alarm-indicating fuses (four load and four alarm indicating per bus) and a filter capacity bank (two capacitors per bus.)

Figure 6-6 shows the high-current fuse panel.

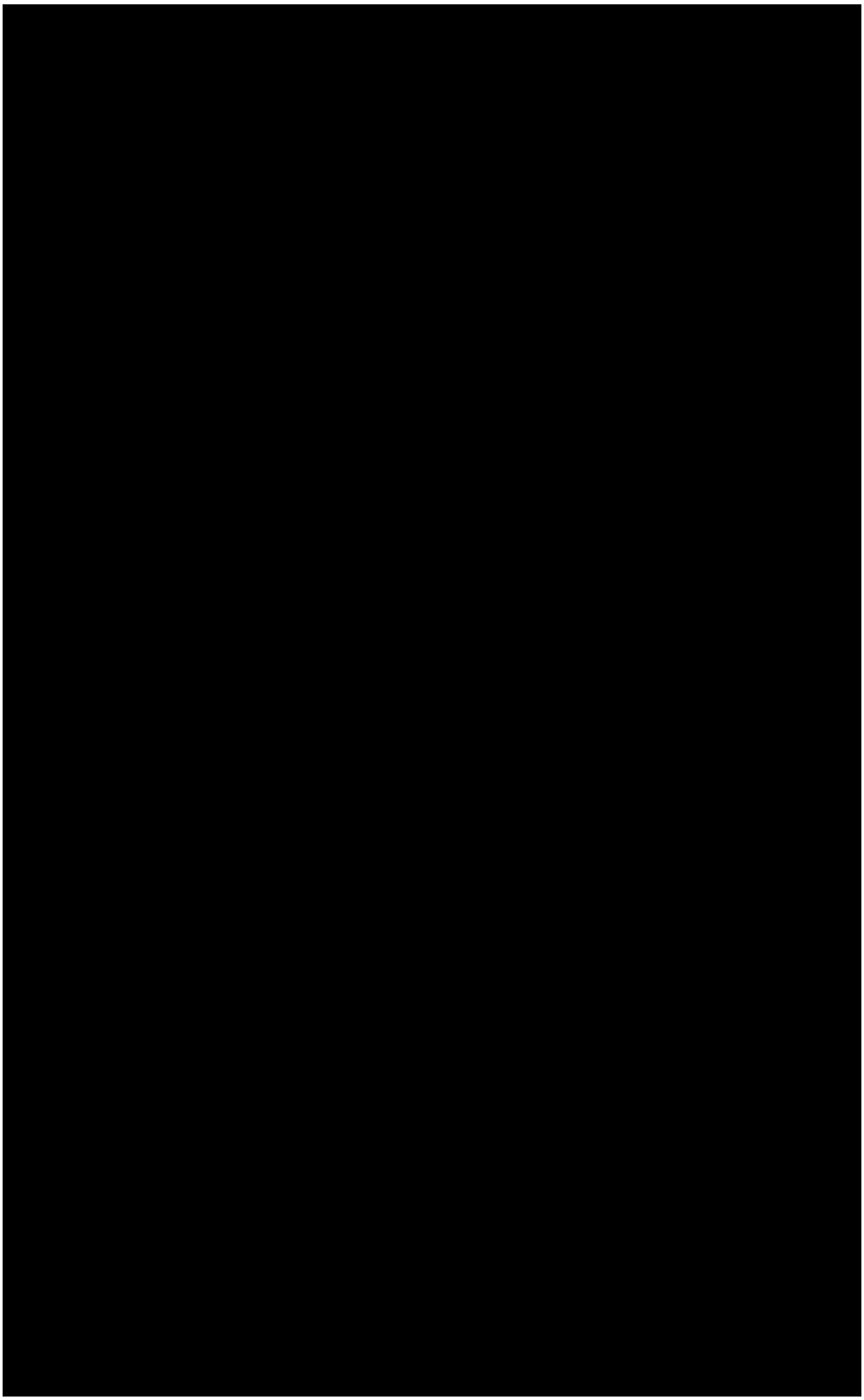

Figure 6-4 Typical Global Power Distribution Frame

Figure 6-5 Alarm Panel and WP92955 Fuse Panel

Figure 6-6 High-Current Fuse Panel (Front View)

GLOSSARY

A-Link
The A-link connects the first- and second-stage switches of the line unit or access link from end office to STP.

Access Editor (ACCED)
The ACCED is an administrative memory module function that controls the freeing and use of terminating number assignments.

Access Interface Unit (AIU)
Provides functionality found in line units and Integrated Service Line Units.

Access Tandem (AT)
An AT is an *ESS*^{TM} switch used to provide carrier access to end offices and possibly to colocated stations to directly control, in stages, the routing of an outgoing tie trunk call through the originating and intermediate switches. The user is said to ``cut-through'' these offices. These trunks are referred to as ``nonsender'' or ``tandem'' tie trunks.

Administration
Administration consists of related functions with the objective of ensuring the overall provision of switch service. Administration includes the assignment of lines and trunks to the system, memory

management, collection of traffic and plant data, provisions for additions and modifications to the switch, service evaluation, and capabilities to control and manage the switch. The primary objective of administration is to assure that the switch delivers a high level of quality service to the subscribing customers. This is accomplished by monitoring and evaluating system performance. Potential problems that cause service deterioration are identified.

Administrative Module (AM)
The AM is the part of the *5ESS*® switch that performs call processing, administration, and maintenance, which cannot be economically distributed to the switching modules. The AM consists of the processor, disk storage, and tape backup units. The AM processor performs the central processing functions, controls the high-speed tape, and the flow of data between the other dedicated processors distributed throughout the remaining units. The processor functions are fully duplicated (except for the port switch) to assure continued processing capability.

All Tests Pass (ATP)
ATP is an indication that all tests have passed in a particular diagnostic or other test.

Analog Trunk Unit (ATU)
The ATU is a single-shelf unit in the Switching Module Control or Line Trunk Peripheral cabinets. It provides termination for interoffice trunks and trunks to operator positions and announcement machines.

Application Controller (APC)
An APC is a component of the switching module processor.

Asynchronous Transfer Mode (ATM)
ATM is a high-bandwidth, fast-packet switching technology that uses fixed length (53-byte) cells to exchange data. The ATM is used to move mass quantities of digital data to remote locations through data nodes.

Attempt
The term attempt refers to a peg count of an effort to use a facility or a circuit. An attempt may be a success or a failure.

Attribute
The term attribute as used here is the title of a column in a data table having a unique name.

Audit (AU)
An AU is a program that ensures reliable service by verifying the software memory for consistency of data. It performs this task by detecting and correcting errors, and recovering lost resources, which increases the efficiency of the system.

Automatic Line Insulation Test (ALIT)
The ALIT is an operations, administration, and maintenance feature that enables routine testing of analog line appearances terminating directly on the switch. It runs tip-to-ring, tip-to-ground, and ring-to-ground leakage tests.

Automatic Message Accounting (AMA)
The AMA is a procedure in which the revenue accounting office processes the automatic accumulation of call data such as calling number, called number, date, time, duration, etc., to render a customer's telephone bill. Magnetic tapes and disks store the information from local and toll calls for billing purposes.

Automatic Message Accounting Teleprocessing System (AMATPS)
The AMATPS is a billing system feature where the switch forwards billing information over a data link to a central automatic message accounting data collection system. The automatic message accounting data collection system interfaces with a revenue accounting office.

Automatic Number Identification (ANI)
The ANI is a feature of a local switching office that automatically identifies the calling party without operator intervention.

B-Link
A B-link is the output from 16 line unit half-grids that are multipled onto 64 different paths.

Basic Rate Interface (BRI)
The BRI is the customer line's interface to the integrated services line unit that combines two B-channels and one D-channel.

Battery Feed, Overvoltage Protection, Ringing, Supervision Coding and Decoding, Hybrid (2-wire, 4-wire Conversion) and Testing (BORSCHT)
BORSCH is a series of test routines provided with and run in the line unit.

Bi-Peripheral Interface Data Bus (BPIDB)
The BPIDB is a data transfer point within the digital network unit - synchronous optical network unit.

Bootstrap
Bootstrap is an initialization action which results in a memory reload and software initialization. The effect is the same as shutting a unit down and restarting it.

Bootstrapper (BSTR)
BSTR is a part of the ``fast pump'' data link that works with the processor update bus to gain access to service module processor memory (see also bootstrap).

Broadcast Warning Message (BWM)
BWM is an obsolete term. See Software Update.

Bus Interface Controller (BIC)
The BIC is a unit that interconnects a duplex bus selector to the microprogrammer controller of the peripheral interface controller.

Bus Service Node (BSN)
The BSN is a component of the switching module processor.

Business and Residence Custom Services (BRCS)
The BRCS software is *5ESS*® switch software that makes revenue generating features available to both business and residential customers.

Business and Residence Customer Services Feature Grouping (BFG)
The BFG function provides group feature assignment to lines. A BFG is a group of features and parameters. A BFG is not a group of directory numbers, terminals or multiline hunt group members, but a BFG may be assigned to any number of directory numbers, terminals, or multiline hunt group members.

BX.25
The BX.25 protocol is the Lucent Technologies version of the Telecommunication Standardization Sector protocol X.25. This protocol is used for exchanging messages between the message switch and the switching module.

Byte
A byte is eight binary digits, or bits; the byte is the basic unit for measuring a computer's memory and storage capacity. Equivalent decimal values are 0 - 255.

Carrier Group Alarm (CGA)
The CGA enables the local switching system to infer the failure of a carrier group from observed call failures on only a few trunks in the trunk group.

Central Control Input/Output (CCIO)
The CCIO is an interface that connects the central processing unit to up to two direct memory access controllers and up to two additional input/output peripherals.

Central Office (CO)
The CO is the switching equipment in a building that provides exchange telephone service for a given location. In some cases, there is more than one CO serving the same area. A CO may include more than one CO code.

Central Office Terminal (COT)
The COT is hardware on the backplane of the digital network unit - synchronous optical network that changes electromechanical signals to analog signals.

Central Processor (CP)
The CP provides the primary control for operating the equipment that directs calls through the central office and aids in detecting and analyzing any faulty equipment involved in this task. In the switch, the administrative module is the central processor.

Central Processor Unit (CPU)
In general terms, the CPU is the area where all calculations take place. In a microcomputer, this is usually the microprocessor chip. In the *5ESS*® switch, it is the administrative module. Other components may have their own independent CPUs.

Central Trunk Test Unit (CTTU)
The CCTU provides central trunk maintenance through a data link. This lets switching control center maintenance personnel perform remote trunk testing from a work station on a local switching office.

Circuit Pack
A circuit pack is a plug-in unit used as a convenient means for assembling, on a single mounting, one or more components such as capacitors, inductors, diodes, resistors, transistors, etc. The components are interconnected to perform one or more circuit functions, such as amplification, gating, timing, etc., required in a circuit. Typically, each circuit pack is a field replaceable unit.

Common Channel Signaling (CCS)
The CCS is an operating capability of the software release that is compatible with the common channel interoffice signaling No. 6, embedded common channel interoffice signaling No. 6, destination common channel interoffice signaling No. 6, common channel signaling 7, and telecommunication standardization sector message protocols and permits the switch to reach the No. 2 signal transfer point network.

Common Control (CC)
The CC circuit packs are two circuit packs in the digital network unit - synchronous optical network which implement a duplex unit controller that operates in active/standby mode. The primary functions of the CC include the termination of message and control channels originating from the switching module-2000 CORE40 and interfaced via the peripheral control and timing links and common data circuit packs; supervision of unit initialization, maintenance and diagnostics; implementation and handling of the control interfaces to all circuits in the digital network unit - synchronous optical network and non-volatile storage of CC and transmission multiplexer control programs in flash memory.

Common Control Processor (CCP)
The CCP routes control messages between the module controller and time slot interchanger and the integrated services line unit circuit packs.

Common Control Switching Arrangement (CCSA)
The CCSA is a switching arrangement is groups of trunks and one or more switching machines used to switch calls in a private leased network. All stations connected in the private network may call one another without using the public toll facilities. In addition, the CCSA provides access to a direct

distance dialing network for network inward calling to the centrex group, directs outward dialing to the direct distance dialing network and other features to the exchange network.

Common Data (CD)
The CD boards are located in the digital network unit - synchronous optical network and logically terminate the PCT links and perform rate conversion, selection and multiplexing/demultiplexing functions associated with passing data and control information between the peripheral control and timing links and internal interfaces with other packs in the unit.

Common Data and Control (COMDAC)
The COMDAC is a component of the access interface unit that provides a control interface between the switching module processor and the application circuit packs.

Common Network Interface (CNI)
The CNI functions as a packet switching system in the signaling network. The CNI is not a stand-alone switching system but requires configuration to an application such as the *5ESS*® switch. The CNI consists of several peripheral processors (ring peripheral controllers and link nodes) serially interconnected and a central processor that performs the basic operating system duties in a distributed input/output processing architecture.

Common Network Interface/Interprocess Message Switch (CNI/IMS)
The CNI/IMS consists of a single switch cabinet that provides two types of ring nodes: ring peripheral controllers and link nodes. The common network interface/interprocessing message switch is connected to the administrative module by way of a dual serial channel and also interfaces with digital data service facilities.

Common Optical Termination (COT)
The COT is a paddle board located on the back of the digital network unit - synchronous optical network board. The COT terminates the optical fibers for one side of a duplex peripheral control and timing link and performs optical-to-electrical and electrical-to-optical conversion of data and control information received and transmitted over the peripheral control and timing link interface with the switching module-2000.

Common Shelf Unit of ISLU (CSU)
The CSU supports all the equipment mounted in the integrated services line unit drawer shelf units.

Common Signaling Channel (CSC)
The CSC is a call processing signaling method (out-of-band).

Communication Link (CLNK)
The CLNK is a logical path of control messages to/from the dual link interface in the switching module from/to the module message processor in the administrative module.

Communication Module (CM)
The CM is hardware that provides the interface between the administrative module and the switching module(s). In a multimodule office, the CM consists of the message switch and the time-multiplexed switch.

Communication Module Control Unit (CMCU)
The CMCU, a part of the communication module model 2, provides message interface and timing facilities used to synchronize the time division network in the time-multiplexed switch via the time-multiplexed switch unit. The CMCU consists of a duplex message interface, network clock model 2, time-multiplexed controller and metallic interface. The CMCU is not used in the communication module 1 configuration (see message interface clock unit).

Communication Module Control Unit-2 (CMCU2)
The CMCU2 is an updated version of the communication module control unit that is physically smaller but has an increased call handling capacity (see also communication module model).

Communication Module Model 1 (CM1)
The CM1 consists of four cabinets. There are two time-multiplexed switch cabinets, and two message switch cabinets. Equipment in time-multiplexed switch cabinet 0 and message switch cabinet 0 is duplicated in time-multiplexed switch cabinet 1 and message switch cabinet 1, respectively.

Communication Module Model 2 (CM2)
The CM2 is an updated version of the communication module that is physically smaller but has an increased call handling capacity. This has been accomplished by use of the new operationally larger time-multiplexed switch model 2 and message switch model 2, now housed in the CM2 cabinet instead of separate time-multiplexed switch and message switch cabinets.

Communications Module Model 2 Compact (CM2C)
The CM2C is for small office applications. The CM2C costs less and requires less floor space than the communication module model 2. The CM2C is housed in 3 shelves of a switching module control cabinet or line trunk peripheral cabinet as opposed to at least 2 communication module cabinets for the communication module model 2.

Communication Module Processor (CMP)
The CMP can be added to the communication module model 2 compact. It is also referred to as the communication module processor unit.

Communication Module Processor Unit (CMPU)
See communication module processor.

Communication Module Unit (CMU)
The CMU is the basic field replaceable unit (circuit pack) of the communication module model 2 compact.

Communication Module Unit Model 2 (CMU2)
The CMU2 is a unit in the Global Messaging Server that houses the message switch, network clock and control, oscillator, time-multiplexed switch foundation, and optical paddle boards.

Component
A component is a server such as a trunk, tone decoder, or service circuit that is a shared resource as opposed to being dedicated.

Concentration Ratio
The concentration ratio is the ratio of the number of lines terminated on the line unit to the time slots available for the line unit (64 time slots per line unit).

Concentrator
A concentrator is a digital switching entity that permits more customers to share common output lines; for example, a 2:1 concentrator permits 48 customers to share the 24-channel capacity of a single T1 line.

Concentrator Group (CG)
The CG is synonymous with line unit pair of concentrators. There may be 4, 6, 8, or 10 concentrators to a line unit.

Constructed Feature
A constructed feature is a feature defined by a switch user (such as the service provider) for their particular needs.

Control and Display (C&D)
The C&D circuit packs run in-service/out-of-service control and the alarming of the power converters.

Control Bus Terminator (CBT)

The CBT is a type of paddle board located in the time slot interchange unit model 2 - version 4.

Control Interface (CI)
The CI, a subunit of the time slot interchange unit, provides an interface and monitors communications between the switching module processor and the interface units and reports errors detected; receives, latches, and reports service requests from interface units to the switching module processor; and distributes control and clock signals to the module peripheral units via the peripheral interface control bus.

Control Interface Model 2 (CI2)
The CI2 is an updated control interface circuit pack.

Control Interface Bus (CIB)
The CIB carries the control messages between the control fanout and the data fanout.

Control Time Slot (CTS)
The CTSs are transmission periods for control signals during multiplexing or demultiplexing.

Control Time Slot Number Select (CTSNS)
The CTSNS is a type of paddle board located in the Time Slot Interchange Unit Model 2 - Version 4.

Control Unit (CU)
See central processor.

Control and Data Interface (CDI)
The CDI provides the trunk unit service group interface through the peripheral interface control bus and peripheral interface data bus to the module controller and time slot interchanger unit.

Customer Premises Equipment (CPE)
CPE is telephone equipment located on the customer's premises.

Cyclic Sequential Search (CSS)
CSS is a path hunt used in the switch call processing software.

Data Base Manager (DBM)
The DBM provides interfaces and access mechanisms between software systems and data in the data base.

Data Expander (DX)
The DX is a circuit board that interfaces peripheral units with the time slot interchanger.

Data Interface
The data interface is a subunit of the time slot interchange unit that provides the interface for the pulse code modulation data, signaling bits, and the clock and time-slot synchronization between the time slot interchanger and the interface units.

Data Link Processor (DLP)
Data Link Processor.

Defense Switched Network (DSN)
The DSN is a private 4-wire telecommunications network used for official business of the Department of Defense and military installations. The DSN incorporates unique features specific to government applications, including the use of *5ESS*® switches as multifunction switches. The DSN has control to permit or limit access to commercial telephone company central office and trunk lines and to restrict commercial access to the DSN as deemed necessary. The terms DSN, Automated Voice Network (AUTOVON), and DSN/AUTOVON are interchangeable when referring to this network.

Derived Data Links (DDL)

DDLs are used to communicate with other remote switching modules in a multimodule remote switching module when in a stand-alone mode.

Dial Pulse (DP)
DP is a method of transmitting digits (address information) between telephone customers and the central office or between central offices. It consists of direct current pulses caused by momentarily opening the loop (usually at 10 ``opens'' per second). The numerical value of each digit is represented by the number of ``opens'' in a train of pulses.

Dial Tone Delay (DTD)
The DTD is the time it takes the switching system to return dial tone to an originating line after the subscriber goes off-hook.

Dictionaries
Dictionaries are contained in a data base in the *5ESS*® switch and provide information such as access type, relation and attribute identifications, number of subattributes, domain identifications, etc., in the memory structure.

Digital Audio Tape (DAT)
The DAT drive uses 4-mm wide tape in 90-, 60- and 30-meter cartridges. The usable storage capacity of the DAT drive varies with the length of tape and recording mode. In a noncompressed mode, the capacity is 650 megabytes for 30 meters; 1300 megabytes for 60 meters; and 2500 megabytes for the 90-meter tape.

Digital Carrier Line Unit (DCLU)
The DCLU terminates the T1 carrier from the *SLC*® 96 carrier systems to the switch.

Digital Cross-Connect (DSX)
The DSX is an internal interface that acts as a central point for cross-connecting, rearranging, patching, and testing digital equipment and facilities.

Dual Digital Multiplexer 2000 (DDM-2000)
Dual Digital Multiplexer 2000.

Digital Equipment Number (DEN)
The DEN is a seven-digit number used in translation to identify the location of a digital line/trunk unit channel so that it may be used.

Digital Facilities Access (DFA)
The DFA is an entry point for digital facilities in a *5ESS*® switch.

Digital Facility Interface (DFI)
The DFI is circuitry in a digital line/trunk unit that terminates a single T1 span line from a T-carrier remote switching module.

Digital Line/Trunk Unit (DLTU)
The DLTU is hardware that terminates digital trunks with switching modules by way of T1 lines.

Digital Line/Trunk Unit Model 2 (DLTU2)
Digital Line/Trunk Unit Model 2.

Digital Loop Carrier (DLC)
The DLC is a term that refers to a class of interfaces that allow line appearances to be remoted via digital facilities such as T1 or E1 to a remote unit with line units.

Digital Network Unit - Synchronous Optical Network (DNU-S)
The DNU-S is an SM-2000 peripheral unit that provides an optical trunk interface. Its primary function is to terminate synchronous optical network facilities and overhead. It converts data and signaling

information between synchronous optical network and peripheral control and timing link format. It provides the *5ESS*® switch interface for interoffice circuit switched trunks (inband and common channel signaling), TR303 digital loop carriers and remote switching modules.

Digital Ordering and Planning System (5 DOPS)
The 5 DOPS is the standard engineering ordering and pricing vehicle for the *5ESS*® switch.

Digital Service Circuit (DSC)
The DSC produces and controls cadenced tone sequences. This function includes timing for tone cadencing, control of tone sequences, and signal processing for tone generation.

Digital Service Circuit - Model 3 (DSC3)
The DSC3 provides four times the capacity of the digital service circuit used in the switching module. It also provides the local digital service function.

Digital Service Unit (DSU)
The DSU is a functional part of the switching module that generates and decodes tones, tests integrated services digital network lines and common channel signaling trunks, and provides recorded announcements for the operator services position system.

Digital Service Unit - Model 2 (DSU2)
The DSU2 is an upgraded replacement for the local digital service unit. The DSU2 performs all tone generation and decoding functions required for call processing, tests common channel signaling trunks, stores recorded announcements, and tests integrated services digital network lines.

Digital Service Unit - Model 3 (DSU3)
The DSU3 is a one shelf unit that can be located in any SM-2000 cabinet. The DSU3 performs both the local and global digital service functions.

Digital Service Unit Bus (LDSUB)
The LDSUB is a data connection terminating the time slot interchanger in the module controller and time slot interchanger unit and the serial data interface circuit on the digital service circuit pack. The LDSUB is the path over which digital tone samples pass to and from the digital service unit - model 2.

Digital Signal Level 0 (DS0)
A DS0 is a single 64 Kbps time slice on a T1 carrier and corresponds to the capacity of one voice frequency equivalent channel. This rate forms the basis for the North American digital multiplex transmission hierarchy. DS0 uses pulse code modulation.

Digital Signal Level 1 (DS1)
A DS1 is a group of 24 digital signal level 0 signals multiplexed together for a rate of 1.544 megabytes per second.

Digital Signal Level 2 (DS2)
A DS2 is a group of 4 digital signal level 1 signals multiplexed together for a rate of 6.312 megabytes per second. The DS2 is equivalent to 96 digital signal level 0 signals.

Digital Signal Level 3 (DS3)
DS3 is a transmission medium that can be fiber-optic or digital radio at a rate of 44.736 megabytes per second.

Digital Signal Processor (DSP)
The DSP is a special microprocessor that performs signal processing operations in the universal tone decoder, universal conference circuit, and transmission test facility.

Digital Universal Conference Service (DUCS)
The DUCS is a three-port or six-port conference circuit capable of conferencing up to three or six parties, respectively.

Direct Link Node (DLN)
The DLN is a node on the common network interface ring for signaling message processing normally done by the administrative module. The DLN is connected with other nodes on the ring by way of the dual ring bus.

Direct Memory Access (DMA)
The DMA circuitry provides direct access to the main store by peripheral units without involving the administrative module.

Direct Memory Access Input/Output (DIO)
Direct Memory Access Input/Output (DIO).

Direct Memory Access Controller (DMAC)
The DMAC provides the controlling circuitry for direct memory access to the main store, bypassing the central processor unit.

Directly Connected Test Unit (DCTU)
The DCTU is connected to each line and trunk to provide a number of required facility tests.

Directory Number (DN)
A DN is a seven-digit telephone number made up of a three-digit central office code and a four-digit station number. It is also called a telephone number.

Discontinued Availability (DA)
A DA rated product is no longer available for purchase.

Disk Drives
A disk drive is a memory storage hardware device that uses magnetic recording on rotating disks. Disk drives provide reliable and flexible mass memory storage for infrequently used programs and data. A single drive, with its controller, makes up a disk unit.

Disk File Controller (DFC)
A DFC is a microprocessor-controlled unit that is programmed to accept tasks from the administrative module and then assigns each task to a disk drive work queue.

Disk Unit (DU)
See Disk Drives.

Disk Unit Package (DUP)
See Disk Drives.

Dual Dynamic Random Access Memory (DDRAM)
Dual Dynamic Random Access Memory.

Dual Link Interface (DLI)
The DLI is a connection from the time slot interchanger to the network control and timing links which inserts control messages between the module processor and the administrative module or other module processors, providing buffering and timing.

Dual Multimodule Processor (DMMP)
The DMMP is an optional feature for hardware expansion, providing greater reliability for full message transfer capacity in communication module - model 2 equipped offices.

Dual Serial Channel (DSCH)
The DSCH bus in the common network interface that provides packet data transfer between the ring peripheral controllers, link nodes and the administrative module.

Dual Serial Channel Computer Interconnect (DCI)

The DCI uses direct memory access over the dual serial channel to perform data transfers of up to 700 kbytes per second.

Dual Tone Multifrequency (DTMF)
DTMF is a method of transmitting digits (address information) from telephone customers to the central office. It consists of sending a simultaneous combination of one of a lower group of frequencies and one of a higher group of frequencies to represent each digit (1 through 0) and symbols (* and #).

Duplex Dual Serial Bus Selector (DDSBS)
The DDSBS permits a connection of two dual serial channels to a single input/output device.

Duplex Message Interface (DMI)
The DMI is circuitry terminating the message interface fuses from the module message processors.

Duplex Multienvironment Real-Time (DMERT)
The DMERT operating system is a software program used by the administrative module.

Dynamic Memory
Dynamic memory is equipment used to magnetically store information which is changed frequently, such as equipment and work status, work queues, etc. Dynamic memory, dynamic data, and dynamic office dependent data are used interchangeably.

Dynamic Random Access Memory (DRAM)
DRAM is random access memory that requires data refreshing periodically to prevent its loss from memory.

E&M Signaling Leads
The E&M signaling leads is a signaling system that derives its name from historical designations of the signaling leads on the circuit drawings covering these systems. The M-lead carries supervisory (and sometimes dial pulse) signals from the switching equipment to the signaling/transmission equipment. The E-lead carries supervisory signals from the signaling/transmission equipment to the switching equipment. As a result, signals from office A to office B leave on the M-lead at office A and arrive on the E-lead at office B.

Echo Canceler 5 (EC5)
Echo Canceler 5.

Electrical Line Interface (ELI)
The ELI splits the received digital signal level 1 signals to active/standby loop side interfaces and combines the transmitted digital signal level 1 signals. Each ELI can handle 20 digital signal level 1 signals.

Electrical Network Link Interface (ENLI)
The ENLI terminates one bi-directional electrical link to the transmission rate conversion unit model 2.

Electronically Erasable Programmable Read-Only Memory (EEPROM)
An EEPROM is a type of erasable programmable read-only memory which can be erased electronically and rewritten without removing the chip or component from its surroundings.

Embedded Operations Channel (EOC)
The EOC is a 64-Kbps channel for operations, administration, and maintenance messages.

Emergency Action Interface (EAI)
The EAI is an interface connecting craft input to the central control for certain maintenance functions.

Emitter-Coupled Logic Bus (EBUS)
The EBUS is the communications path between the communication module control unit and the time-multiplexed switch unit model 2.

End-of-Period (EOP)
The EOP is a statistical term used in engineering that denotes the end of a predetermined engineering period. It is the time between scheduled phases of equipment growth or modification operations.

Engineering and Administration Data Acquisition System (EADAS)
The EADAS is an automated traffic data collection system which collects and summarizes data obtained from central office switches to be used for administrative and engineering purposes.

Enhanced Private Switched Communications Service (EPSCS)
The EPSCS is a private switched network of dedicated facilities providing full duplex communication on all connections. It provides a center from which the customer can exercise, monitor, and control functions relative to the performance of the network.

Equal Access End Office (EAEO)
The EAEO is an *ESS*^{TM} switch used to provide carrier access to colocated stations.

Equal Access Signaling (EAS)
EAS is a signaling method introduced by the carrier interconnect feature.

Equipment Access Network (EAN)
The EAN is a circuit pack which is a distribution node in the upper equipment shelf of the directly connected test unit.

Equipment Location (EQL)
The EQL is expressed as a nine-digit index used to identify the location of a component. See Figure 4-1 for more detailed information.

Erasable Programmable Read-Only Memory (EPROM)
The EPROM is a type of read-only memory that can be erased and rewritten.

Erlang
The term Erlang is a measure of communications traffic intensity representing the full-time use of a communications facility. One Erlang equals 36 centi (hundred) call seconds.

European Digital Signal Level 1 (E1)
A four-wire voice/data trunking facility that carries 30 duplex channels via 64 kilobits per second time slices.

Expansion Access Interface Unit (EAIU)
The EAIU extends the number of Access Interface Units that can be supported on an SM-2000 from 43 to 106.

Extended Data Expansion (XDX)
The XDX circuit packs, available in the time slot interchange unit model 4, Version 2, extend the capabilities of the data expander circuit packs.

Extended Switch Module 2000 (EXM-2000)
The EXM-2000 is an optically remoted SM-2000 that provides the capability to deliver SM-2000 functions at a remote location. The EXM-2000 has the functions provided by local switching modules during normal operations. When an EXM-2000 is isolated from the host switch, only optical stand-alone functions are available.

Extreme Value Engineering (EVE)
EVE is a method of engineering a switching system based on the extreme (that is, most space required, most lines needed) expected use parameters.

Facilities Interface Unit (FIU)
The FIU is used between the remote switching modules and the host switching modules and connects

the T1 format to the network control and timing format.

Fiber Common Data (FCD)
The FDC is an electrical to fiber optic interface that terminates peripheral control and timing links from the SM-2000 time slot interchange unit and distributes the data to each shelf in the multiplex access interface unit cabinet.

Field Replaceable Unit (FRU)
An FRU is a single component of a system (such as a circuit pack) that can be replaced on the spot by a field technician. The FRU is generally the smallest level of item that can be replaced at the customer's site. Board- and chip-level repairs usually involve shipping a defective FRU to a maintenance depot.

Firmware
Firmware is software contained on a non-volatile medium (for example read-only memory, programmable read-only memory, erasable programmable read-only memory, electronically erasable programmable read-only memory), as part of the onboard operating components of a circuit pack or FRU.

Foreign Exchange Service (FX)
The FX is a provider of customer access to a distant central office by FX trunks. Incoming foreign exchange calls are placed to the listed (FX) directory number and answered by the attendant. Outgoing calls may be made on an attendant basis and/or on a station user direct-dial basis.

Foundation Link Interface (FLI)
The FLI is a circuit pack (TN883) that is installed in switching module cabinets 5 and/or 6, and serves as a terminator.

Foundation Peripheral Controller (FPC)
An FPC is a peripheral control in the input/output processor used to provide an administrative module interface to the time-multiplexed switch and maintenance access to the message switch. The FPC issues time slot path requests to the time-multiplexed switch and acts as an interface between the peripheral subunits and the message switch. In the communication module model 1 configuration, the FPC is part of the message switch peripheral unit. Under direction of the administrative module processor, the FPC controls the configuration of hardware in the message interface clock units. In the communication module model 2 configuration, the FPC is part of the message switch control unit model 2. Under direction of the administrative processor, the FPC controls the configuration of hardware in the message switch control unit model 2.

Gated-Diode Crosspoint (GDX)
The GDX is an electronic device used to pass current in either direction and used in the line unit line concentrator.

Global Digital Service Function (GDSF)
The GDSFs are: conferencing (three-way and six-way), transmission test functions, and integrated services test functions.

Global Digital Service Unit (GDSU)
The GDSU is part of a switching module that provides up to eight digital service circuits for low usage functions such as three-port and six-port conferences, test tones, responses to test tones and processing test responses.

Global Messaging Server (GMS)
The GMS, formerly known as the communication module model 3, replaces the entire communication module block in the *5ESS*® switch architecture and provides the foundation for future evolution.

Global Power Distribution Frame (GPDF)

The GPDF provides redundant, protected direct current to power *5ESS*® switching system equipment.

Global Switching Module (GSM)
The GSM is a switching module equipped with signaling system 7 packet switch units and terminating signaling system 7 signaling links.

Graphical User Interface (GUI)
An interface that allows users to operate and maintain equipment through a graphical representation.

Growth
Growth is the systematic modification of central office equipment to provide increased call-handling capacity and improved service. Growth is required so a switch may evolve economically over a wide range of services and traffic needs.

Half-Call
The term half-call refers to the establishment of a path between a peripheral unit and the time slot interchanger. The terminating part of a call represents a half-call and the originating part of the call represents the other half-call. Each half-call generates a terminal process.

High Level Data Link Control (HDLC)
HDLC is a bit-oriented transmission protocol.

High Level Service Circuit (HLSC)
An HLSC is a service circuit in the line unit used to perform all line service circuit functions which cannot be provided through the time slot interchanger.

Host Adapter (HA)
The HA interfaces the duplex dual serial bus selector, intelligent control logic, and two different small computer system interface buses.

Host Office Collector (HOC)
The HOC is a central AMA data collection system which collects AMA data over data links from several telephone switching offices.

Host Switching Module (HSM)
The HSM is a switching module in the host office terminating umbilicals from one or more remote switching modules.

IOP Basic Unit (IOPBU)
The IOPBU is a processor used to control transfers between the main store and peripheral equipment.

IOP Disk File Controller Unit (IOPDFCU)
The IOPDFCU is a generic name for the type of device typified by the main store input/output disk file controller unit.

IOP Growth Unit (IOPGU)
The IOPGU is a generic name for the type of device typified by the main store input/output growth unit.

Information Product (IP)
An IP contains information that supports Lucent products. A variety of medium could be used to present the information; for example, paper, electronic, compact disk, and video.

Input/Output (I/O)
I/O is the process of transmitting information from an internal source to an external destination and vice versa.

Input/Output Microprocessor Interface (IOMI)
IOMI is a unit that provides the interface between the 16-bit peripheral interface controller and up to 16

of the 8-bit module message processors.

Input/Output Processor (IOP)
The IOP controls transfers between the main store of the administrative module and the master control center, operation and maintenance center, and remote terminals. The IOP provides interfaces to visual display units and hard-copy printers in the master control center and other work stations and magnetic tape drives.

Integrated Digital Carrier Unit (IDCU)
The IDCU provides a nonproprietary integrated interface with subscriber loop carrier systems. The IDCU provides the same functions as the digital carrier line unit but provides analog and integrated services digital network interface to customers on the remote terminal.

Integrated Mechanized Loop Testing System 2 (IMLT 2)
The IMLT 2 interface capability provides the functions necessary to remotely test lines connected to the *5ESS*® switch, its main distributing frame, the remote switching modules, and the *SLC*® carrier systems.

Integrated Ring Node Version 2 (IRN2)
The IRN2 adds a new backplane technology to the common network interface ring. Because fewer boards are required to support the common network interface ring, it enables new ring configurations, and most significantly, increases the number of link pair terminations from 5 to 19 pairs. The IRN2 circuit pack performs node processor and ring interface functions.

Integrated Services Digital Network (ISDN)
ISDN is an international plan originated by the Telecommunication Standardization Sector representing the latest step of the evolution of the analog telephone to an all-digital network. Digital voice, circuit-switched, and packet-switched data may be transmitted simultaneously over the same interface.

Integrated Services Line Unit (ISLU)
The ISLU houses the basic rate interface cards in the switching module and provides analog and digital services to subscribers by support of the following interfaces: ISLU-T, a four-wire basic rate interface that provides the basic Integrated services digital network 2B+D access over a range of up to 1,900 feet; ISLU-U, a two-wire basic rate interface that provides the basic integrated services digital network 2B+D access using echo-canceled hybrid technology appropriate for all carrier serving area nonloaded loops; ISLU-Z, for analog lines (that is, plain old telephone service, coin-first coin lines, party lines, etc.) which normally terminates on the analog-concentrated line unit. The ISLU-Z interface can have a concentration ratio of up to 8:1.

Integrated Services Test Function (ISTF)
The ISTF is a group of diagnostic functions, originally native to the digital service unit model 2; ISTF is also, a general term for diagnostic functions native to any field replaceable unit.

Inter-RSM Communication Link (ICL)
The ICLs interconnect switching modules in a multimodule remote switching module.

Inter-SM Quad-Link Packet Switch Communication Link (ISMQLNK)
Inter-SM Quad-Link Packet Switch Communication Link.

Interface Unit (IU)
The IU is a component that provides customer terminations.

International Telegraph and Telephone Consultative Committee (CCITT)
The CCITT is currently known as the Telecommunication Standardization Sector.

Interprocess Message Switch User Node (IUN)
An IUN is a component in the *5ESS*® switch which has no function other than to occupy a position

reserved for future growth. As such, it is a temporary filler component.

Interprocessing Message Switch (IMS)
The IMS is hardware and software in the switching module used to support the operator services position system, business and residential customer service, CSDSCII, and incoming call line identification for interoffice calls and 16 kb/s intraoffice packet switching.

Key
The term key is a designation assigned to one or more data base attributes that provides access to a particular tuple.

Key Service Indicators
Key service indicators give the administrator a quick view of the overall quality of service being provided to the subscribers.

Kilobyte (kB)
A kB is 1024 bytes (by analogy with the metric prefix "kilo-", 1,000).

Light Emitting Diode (LED)
An LED is a semiconductor diode which emits light when current passes through it.

Line Equipment Number (LEN)
A LEN is an eight-digit number used in translations to identify a customer's line.

Line Group (LG)
LG is a general term for a circuit pack installed in a drawer in a common shelf unit of an integrated services line unit. Up to 16 can be installed in each drawer.

Line Group Controller (LGC)
The LGC is the interface between switched information on the group interface data bus and the link interface data bus.

Line Group Power (LGP)
The LGP is a circuit pack located adjacent to the line group controller in the line group common area.

Line Information Data Base (LIDB)
The LIDB is a 32-time slot bus that connects the line group controllers and the common data boards in the integrated services line unit.

Line and Trunk Peripheral (LTP)
The LTP consists of the line unit, trunk unit, metallic service unit, digital carrier line unit, facilities interface unit, and the modular metallic service unit.

Line Unit (LU)
The LU is an interface unit between the analog (subscriber) lines and the switching module.

Link Nodes (LN)
The LN is a part of the common network interface that performs the message handling protocol, control functions, and self-diagnostics. The LN establishes the connection to the signaling network by way of A-links.

Local Digital Service Function (LDSF)
The LDSF circuit pack generates and decodes all tones for the *5ESS*® switch.

Local Digital Service Unit (LDSU)
The LDSU is a part of the switching module that provides high-usage service circuits such as tone decoding, tone generation, conferencing, and voice-frequency testing.

Local Digital Service Unit (Modified) (LDSUM)
The LDSUM is a single circuit pack (TN1637) which replaces tone decoding and generating equipment and common digital service units in the local digital service unit.

Local Digital Service Unit Function (LDSUF)
The LDSUF is the part of the digital service unit model 2 that generates and decodes tones.

Local Switching Module (LSM)
The LSM is one type of switching module supported by the *5ESS*® switch. The term LSM refers to any switching module that is located at the host office.

Local Test Desk (LTD)
The LTD provides equipment that performs local primary line testing. It may be used to test parts of the toll plant.

Loop Side Interface (LSI)
The LSI frames on each of the digital signal level 1 signals and converts it to a peripheral interface data bus-like format on the internal bus which connects to the peripheral interface data bus transmission interface. The LSI also collects digital signal level 1 performance-monitoring data and detects digital signal level 1 failures and alarms.

Machine Load and Service Summary (MLSS)
The MLSS is a report that provides cumulative service year to date and additional capacity information for each switching module.

Magnetic Tape (MT)
An MT is made of magnetic material upon which data may be stored for later retrieval by a computer.

Main Distributing Frame (MDF)
The MDF is a connection system that interfaces between loop cable pairs and switching equipment.

Main Store (MAS)
The MAS is random access memory (16 megabytes) in the administrative module that contains data needed for operating the switch, such as the software release for administrative module functions, translations, call processing registers, and billing registers. The MAS is duplicated for reliability.

Main Store Array (MASA)
The MASA is a circuit pack (TN56) which contains a series of up to eight 2-megabyte random access memory modules which extend the main store from 16 to up to 32 megabytes. See also Main Store Input/Output Disk File Controller Unit.

Main Store Controller (MASC)
The MASC controls access to the main store and main store array, determines memory priorities, and checks memory.

Main Store Input/Output Disk File Controller Unit (MASIOPDFCU)
The MASIOPDFCU is an optional unit needed to expand the 16 megabyte capacity of the main store main unit to a possible 32 megabyte by increments of two.

Main Store Input/Output Growth Unit (MASIOPGU)
Main Store Input/Output Growth Unit.

Main Store Update (MASU)
See Main Store.

Maintenance Teletypewriter (MTTY)
The MTTY is the human-machine interface to the administration module.

Master Control Center (MCC)
The MCC is the local human-machine interface to the *5ESS*® switch including system status displays, hard-copy printers, and manual controls over system operations.

Mechanized Loop Testing System (MLT)
The MLT is an external operations system for testing of the customer lines (loops) in the *5ESS*® switch.

Megabyte (MB)
The MB is a unit of data storage or memory capacity; it is 1,048,576 bytes or 1,024 kilobytes.

Memory Expansion Unit (MEU)
The MEU is hardware that provides additional memory capacity for switching modules and/or remote switching modules.

Message Handler (MH)
The MH is an independent processor unit which manages all data traffic among the various SM-2000 subprocessors.

Message Interface Bus (MIB)
The MIB is a channel for data transfer, such as that between the pump peripheral controller and the communication module control unit.

Message Interface Clock Unit (MICU)
The MICU is a unit in a message switch which consists of the network clock and the network control and timing link interface from the message switch.

Message Switch (MSG/MSGS)
The MSG/MSGS is the unit that performs internal interprocessor message switching, provides terminations for common channel signaling, and contains the message interface clock unit.

Message Switch Control Unit (MSCU)
The MSCU is a part of the communication module and is responsible for handling control information between the administrative module and module processors.

Message Switch Control Unit - Model 2 (MSCU2)
The MSCU2 circuit pack reformats data received from the administrative module or communication module processor unit and transmits it to the other units in the cabinet and vice versa; interprets destination codes of incoming control slots and switches the control time slots to the administrative module or another switching module and provides control of the other units in the communication module model 2 cabinet.

Message Switch Control Unit - Model 3 (MSCU3)
The MSCU3 is a unit which controls message transfers between the administrative module and as many as 14 peripheral control communities. It performs serial-to-parallel and parallel-to-serial conversion of data received from/transmitted to the administrative module; provides control to transfer data between the administrative module and foundation peripheral controller or pump peripheral controller; provides manual and administrative module control of the MSCU3 from an in-service/out-of-service perspective.

Message Switch Peripheral Processor (MSPP)
The MSPP is the controlling circuit pack of all message switch peripheral controller applications.

Message Switch Peripheral Unit (MSPU)
The MSPU is the hardware unit of the communication module that switches interprocessor messages on the control time slots.

Message Switch Peripheral Unit Model 2 (MSPU2)

The MSPU2 is the particular model of message switch peripheral unit which is mounted in equipment location 53 of all communication module model 1 cabinets.

Message Switch Peripheral Unit Model 3 (MSPU3)
The MSPU3 is the particular model of message switch peripheral unit which is mounted in equipment location 53 of all communication module model 2 cabinets.

Message Waiting Indicators (MWI)
The MWI feature is an ISDN feature informing a customer of a message waiting. Three types of indicators are provided:

(1) ***Audible Message Waiting Indicator***: Provides a tone when the customer goes off-hook.

(2) ***Electronic Billboard***: Provides name of person having messages.

(3) ***Visual Message Waiting Indicator***: Activates a message waiting lamp on the station set.

Metallic Access (MA)
An MA connection is made with metallic wires as opposed to connection with fiber-optics or other types of connections.

Metallic Service Unit (MSU)
The MSU provides an access network which connects analog facilities and direct current test equipment; provides scan and distribute functions, metallic access, automatic line insulation testing, and gated-diode crosspoint compensation.

Metallic Test Bus (MTB)
The MTB connects the modular metallic service unit to the test access circuit within each trunk unit. This bus is used for maintenance and routine test activities.

Metallic Test Interface Bus (MTIB)
See Metallic Test Bus.

Micro Code (MC)
MC is software written in a low-level computer language, typically an assembler language program. Also, an identifying code on a circuit pack label identifying the revision level of the onboard firmware.

Modular Controller Time Slot Interchanger (MCTSI)
MCTSI is an alternate designation for modular controller and time slot interchanger unit.

Modular Metallic Services Unit (MMSU)
The MMSU provides metallic access, miscellaneous scanning and distributing functions, automatic line insulation tests, and gated-diode crosspoint compensation.

Module Controller and Time Slot Interchanger Unit (MCTU)
The MCTU is a component that provides a variety of interface functions between the switching module and other components and modules in the *5ESS*® switch.

Module Controller and Time Slot Interchanger Unit - Model 2 (MCTU2)
The MCTU2 is a modified but equivalent version of the regular module controller and time slot interchanger unit.

Module Message Processor (MMP)
The MMP is circuitry in the message switch peripheral unit that handles control message protocol on the link to the switching modules.

Module Processor Interface (MPI)
Module Processor Interface.

Moving Head Disk (MHD)
The MHD is a high-capacity, random-access digital data storage device the administrative module uses to store infrequently used programs and data.

Multimodule Remote Switching Modules (MMRSM)
The MMRSM consists of one to four remote switching modules interconnected by dedicated T1 links. Each remote switching module is also connected to a switching module at the switch by dedicated T1 links.

Multiplex Access Interface Unit (XAIU)
The XAIU provides the same functionality as the access interface unit, but reduces cabling installation time by using fiber optic peripheral control and timing links instead of peripheral interface control buses and peripheral interface data buses.

Multiline Hunt Group (MLHG)
An MLHG is a group of customer facilities which are identified as a group in translations. When calls are placed to the MLHG, the switch hunts for an idle member of the group beginning with the dialed directory number.

Network Administration Center (NAC)
The NAC is a work group attached to the switching control center system and designated to automatically receive the following: 15-minute traffic reports; 5-minute, 1-hour, 24-hour and monthly plant reports; and 30-minute traffic reports on request.

Network Clock (NCLK)
The NCLK is a digital reference clock for a telecommunications network.

Network Clock and Control (NCC)
The NCC is a circuit pack (MMD101) in the Communication Module Unit 2 of the Global Messaging Server that provides functions such as synchronization and timing for the Global Messaging Server and the rest of the office, and call processing, maintenance, and error reporting control for the time-multiplexed switch fabric.

Network Control and Timing (NCT)
The NCT is a fiber-optic path which connects a switching module to the time-multiplexed switch, provides timeslot paths for network connections, carries a control time slot to the switching module, and distributes timing to the switching module.

Network Control and Timing 2 (NCT2)
An NCT2 link has 512 time slots and runs at a rate of 65.536 Mbps.

Network Link Interface (NLI)
The NLI terminates one bidirectional optic link (two physical fibers) to the communication module.

Next Generation Digital Loop Carrier (NGDLC)
Next Generation Digital Loop Carrier.

Nonredundant Office Dependent Data (NRODD)
NRODD is office dependent data that is not backed up (call processing data, for example).

North American Regional Technical Assistance Center (NARTAC)
The NARTAC is the technical support office assigned to your part of the country. The phone number for NARTAC information is 1-800-225-RTAC (7822).

Office Data Base (ODB)
The ODB is a store of information specific to the particular office or location served by a *5ESS*® switch. Also called office dependent information.

Office Data Base Editor (ODBE)
The ODBE is a *5ESS*® switch memory management tool that can be used by technicians to change data base information.

Office Dependent Data (ODD)
The ODD is equivalent to the office data base; a data base specific to a particular office.

Office Dependent Data (ODD) (Static)
Static ODD is data that establishes the types and amounts of various equipment that comprise the office (lines, trunks, equipment, etc.). The protected area of memory.

Office Monitoring System for the *5ESS*® Switch (OMS5)
The OMS5 is a tool or program that assists the maintenance personnel in the performance of the daily preventive maintenance of the switch.

Office Records
Office records are tabular listings of the actual inventories and assignments of the data base and serve as a means for administering the office. An explanation of the form entries is included in the translation guide TG-5.

Office Repeater Bay (ORB)
The ORB is a bay in the office, usually near the digital system cross-connect bays, that houses the digital repeaters used to regenerate pulse code modulation data for a T1 line.

Operating System for Distributed Switching (OSDS)
The OSDS provide an environment that supports distributed processing and allows the application processes to share system resources efficiently.

Operational Capacity
This capacity is the indefinitely sustainable operation point while processing calls with an ideal, fault-free exchange and an unlimited supply of internal resources and external facilities.

Operational Support System (OS)
An OS consists of computer systems which may be used to provide additional administrative support (for example, the engineering and administrative data acquisition system, central office equipment reports, and the switching control center system).

Operations, Administration, and Maintenance (OA&M)
The OA&M is a series of functions run by the digital network unit - synchronous optical network unit which provide, among other things, verification, monitoring, tracing, and alarms.

Operations, Administration, Maintenance, and Provisioning (OAM&P)
Operations, Administration, Maintenance, and Provisioning.

Operator Services Position System (OSPS)
The OSPS uses features provided by a host *5ESS*® switch and dedicated peripheral equipment to support operator and attendant services.

Optical Carrier Level 3 (OC3)
Optical Carrier Level 3 transmission system.

Optically Remoted Switching Module (ORM)
The ORM is a type of remoted switching module that is interfaced to the switch through the communication module instead of a host switching module. This is done by way of digital signal level 3 transmission or T1 facilities (fiber-optic, digital radio, cable, or T1) at a rate of 44.736 MB/s.

Outgoing Trunk (OGT)

An OGT is a one-way trunk where only originating traffic can reach a distant office to complete telephone calls. Originating traffic in the distant office cannot reach this trunk.

Peripheral Interface Data BusTransmission Interface (PTI)
The PTI provides a signal processing function that monitors incoming signaling to detect originations and transmits idle signaling.

Packet
A packet is a group of bits that is switched as an integral unit. Typically, a packet contains data, destination and origination information, and control information arranged in a particular format.

Packet Bus (PB)
The PB is the packet interface between the packet switch unit and the module controller and time slot interchanger unit.

Packet Interface (PI)
The PI sends control messages between the packet switch unit and the CORE via a packet bus.

Packet Interface Bus (PIB)
The PIB is internal to the packet switch unit; that is, the interface between the packet fanout and the control fanout circuitry.

Packet Switch Unit (PSU)
The PSU contains circuitry that provides a central high bandwidth interface to support packet signal messages and packet data switching. The PSU is a part of the switching module and occupies from one to five equipment shelves in a single cabinet.

Packet Switch Unit Type 1 (PSU1)
The PSU1 supports a 10 megahertz peripheral bus.

Packet Switch Unit Type 2 (PSU2)
The PSU2 supports a 100 megahertz peripheral bus and provides enhanced messaging capacity in the packet switch unit.

Path Hunting
Path hunting is a routine the switch uses to select the A- and B-link that connect a given line with an available channel circuit. In addition to finding this path, the path hunt software updates the A- and B-link status maps.

Peg Count
A peg count is a cumulative count of the number of times a specified event occurs during a given time interval. In some cases, the event may be an attempt to take some action, not necessarily a successful attempt.

Peripheral Control and Maintenance Bus (PCAMB)
The PCAMB is a bus on which the common data circuit packs send messages to the central control.

Peripheral Control and Timing (PCT)
The PCT is an interface between the digital network unit - synchronous optical network and the SM-2000 which replaces the peripheral interface data bus and peripheral interface control bus.

Peripheral Control and Timing (PCT) Data Exchanger Unit (PDXU)
The PDXU consists of two peripheral control and timing data exchanger circuits that contain one peripheral link interface paddle board, a peripheral control and timing fiber pair and one fiber common data circuit pack.

Peripheral Control and Timing (PCT) Facility Interface (PCTFI)
The PCTFI is a multi-use interface that terminates loosely coupled access services and transport

products onto the SM-2000 switching fabric.

Peripheral Control and Timing (PCT) Line and Trunk (virtual) Unit (PLTU)
The PLTU is a virtual unit (existing in software) that interfaces the PCT link(s) to the peripheral link interface at the time-slot interchanger unit.

Peripheral Controller (PC)
The PC is circuitry in the input/output processor that connects to peripherals outside the administrative module.

Peripheral Interface Control Bus (PICB)
The PICB is a duplex set of wires carrying control information between the module controller and an interface unit on the switching module.

Peripheral Interface Controller (PIC)
The PIC controls the movement of commands and data between the administrative module processor and the peripheral controllers.

Peripheral Interface Data Bus (PIDB)
The PIDB is a duplex set of wires providing 32 time slots between the data interface and interface units.

Peripheral Link Interface (PLI)
The PLI chosen to terminate the peripheral control and timing link(s) onto the time-slot interchanger is the BKD10 optical paddle board.

Peripheral Unit (PU)
The PU is equipment such as the line unit, trunk unit, digital line trunk unit, digital carrier line unit, or global digital service unit that works with, but is not a part of the administrative module, communication module, or switching module. Peripheral units reside in the switching module.

Plain Old Telephone Service (POTS)
POTS is basic voice service by way of the telephone.

Plant Measurements
Plant measurements provide data to evaluate equipment and craft performance.

Poisson Capacity Table
The Poisson capacity table is a statistical table, based on a theoretical mathematical formula, that is used to estimate the types and amounts of telecommunications equipment required to provide certain levels of service to a known or projected number of subscribers.

Port Switch Unit (PSU)
The PSU is the interface between the master control center, teletypewriter, and printer.

Power Distribution Frame (PDF)
Power Distribution Frame.

Power Distribution Unit (PDU)
The PDU is based in processor cabinet bays 0 and 1; it routes power from the power distribution frame to other components.

Preconstructed Feature
A preconstructed feature is defined by Lucent and is available to all switch users (service providers).

Primary Rate Interface (PRI)
PRI is an integrated services digital network feature supporting digital interface to digital private branch exchanges on a primary rate carrier (1.544 MB/s). It supports twenty-nine 64-kbps B-channels, plus

one 64-kbps D-channel.

Private Branch Exchange (PBX)
A PBX is a switching system installed on a customer's premises.

Private Facilities Access (PFA)
The PFA feature provides subscribers with dial access to various types of public and private switching arrangements.

Processor Control Cabinet (PCC)
The PCCs are cabinets in the administrative modules that house the central processing unit, main store, input/output processor, disk file controller unit, input/output processor basic unit, input/output processor growth unit, power distribution unit, port switch (cabinet 0 only), and cooling unit.

Power Control Fuse Distribution (PCFD)
The PCFD provides primary power distribution (-48V DC to all cabinets in the *5ESS*® switch) from an established source.

Process Identification (PID)
The PID is a number assigned to the running of a program for reporting and tabulating purposes.

Protocol
Protocol is an agreed-on procedure for transmitting information between two or more entities.

Protocol Handler Data Bus (PHDB)
The PHDB is a data bus internal to the peripheral switch unit that is the interface between the protocol handler and the data fanout circuitry.

Protocol Handler (PH)
The PH is circuitry that switches control messages between the basic rate interface and the module controller and time slot interchanger unit.

Protocol Handler for Voice (PHV)
The PHV encodes and decodes compressed packetized speech for sending and receiving to and from the cell sites over the packet pipe.

Pulse Code Modulation (PCM)
PCM is a technique for coding analog signals for transmission on a digital circuit.

Pump Peripheral Controller (PPC)
The PPC is circuitry in the message switch that is responsible for rapid reinitialization in case of total failure of the switching module.

Quad-Link Interface (QLI)
A QLI is a reconfigurable connection to a time-multiplexed switch fabric port (256 time slot access). Each quad-link packet switch has four quad-link packet switch links.

Quad Link Interface - Model 2 (QLI2)
The QLI2 connects a Network Control and Timing - Model 2 link for up to two SM-2000s.

Quad-Link Packet Switch (QLPS)
The QLPS is an optional message switch, QLPS is a high-speed subswitch that supports the increased call capacity of the *5ESS*® switch.

Quad-Link Packet Switch Communication Link (QLNK)
Quad-Link Packet Switch Communication Link.

Quad-Link Packet Switch Gateway Link (QGL)

A QGL is a 32-time slot/2-Mbps metallic link between a specific quad-link packet switch gateway and quad-link packet switch. Each quad-link packet switch gateway has four QGLs, each multiplexed into an associated quad-link packet switch link stream. Each quad-link packet switch may have zero, two, or four QGLs equipped, depending on the number of quad-link packet switch gateways equipped.

Quad-Link Packet Switch Gateway Processor (QGP)
The QGP is a device which provides an interface between the quad-link packet switch and the *5ESS*® switch communications foundation.

Quad-Link Packet Switch Pseudo Time Multiplexed Switch Links (QTMSLNKS)
Quad-Link Packet Switch Pseudo Time Multiplexed Switch Links.

Quad Peripheral Interface Data Bus Common Data and Control (QCOMDAC)
The QCOMDAC provides interface and control between the fiber common data circuit pack and the application circuit packs in the multiplexed access interface unit.

REORG
The term REORG refers to memory reorganization that may be needed when the processing speed is reduced.

Random Access Memory (RAM)
RAM is a type of memory that can be both read from and written to. It can contain resident information (static) or transient information (dynamic).

Read-Only Memory (ROM)
ROM is memory whose data content is preset by the manufacturer. Data content in ROM does not change even if power to memory is removed. See also Programmable Read-Only Memory, Erasable Programmable Read-Only Memory, and Electrically Erasable Programmable Read-Only Memory.

Receive-Only Printer (ROP)
The ROP is used only for receiving messages at the master control center.

Recent Change (RC)
RC is the ability to change the system data base to reflect changes in customer or system capabilities.

Recent Change and Verify (RC/V)
The RC/V system provides the ability to change the system data base to reflect changes in customer or system capabilities, and to determine the contents of the system data base.

Recorded Announcement Function (RAF)
The RAF provides independent playback of prerecorded, variable length, and variable content operator services position system announcements.

Recorded Announcement Unit (RAU)
The RAU is a totally electronic storage device (no moving parts) which uses magnetic bubble memory to store recorded messages in digital form. Using a maximum of four 13A announcement machines, the RAU provides up to 32 channels of recorded messages.

Redundant Office Dependent Data (RODD)
RODD is office dependent data that is backed up.

Relation
A relation, as used in this document, is a rectangular data table (matrix) that has rows called tuples and columns called attributes.

Remote Common Data and Control (RCOMDAC)
The RCOMDAC, used in the expansion access interface unit, provides a digital signal level 1 signal over a T1 facility that is multiplexed into a synchronous transport signal level 1 signal. Each

RCOMDAC can have up to 6 T1 facilities.

Remote Digital Terminal (RDT)
The RDT is a TR303 term for the remote unit that provides the line units in a digital loop carrier case.

Remote Integrated Services Line Unit (RISLU)
The RISLU terminates digital and analog lines. It consists of an integrated services line unit and a digital line trunk unit for an RISLU, and it is connected to a host switching module by T1 carrier. The RISLU may be located up to 175 miles from the host switch. The RISLU is a remote version of the central office equipment and provides analog and digital services (including some switch features) to remote subscribers. The RISLU provides up to 496 terminations for remote operations over 24- and 30-channel pulse code modulation facilities. The RISLU provides the same three types of interfaces (T, U, and Z) as the integrated line services unit.

Remote Memory Administration System (RMAS)
The RMAS is an operational support system used to load translation changes into the switch.

Remote Switching Module (RSM)
The RSM is a type of switching module that is located away from the switch. The RSM provides the switching capabilities of the *5ESS*® switch to areas that cannot economically support a *ESS*™ switch.

Remote Terminal (RT)
The term RT is a software release term denoting the remote vehicle in any pair gain or remote switch system.

Revenue Accounting Office (RAO)
The RAO is a telephone company central computation center where per-message charges are calculated from automatic message accounting billing data, combined with other fixed monthly charges and prepared for delivery to telephone customers.

Revertive Pulse (RP)
An RP is a signaling pulse made by an local digital service unit transceiver to another local digital service unit transceiver on the same line. The local digital service unit model 2 does not provide RP transceivers.

Ring Peripheral Controller (RPC)
The RPC is a part of the common network interface that transports signaling messages and internal control common network interface/interprocess message switch messages between the administrative processor and the ring by way of a dual serial channel. The RPC node does not provide network connection. The switch uses two RPCs.

Ring Peripheral Controller Node (RPCN)
The RPCN is a circuit pack that manages communications between the ring and the administrative module. Two RPCNs are always used in the *5ESS*® switch common network interface application.

Route Index
The Route Index is a code used in selecting the path a call takes through an office.

Service Announcement System Digital Service Circuit Controller (SASDSC)
The SASDSC is a controller board (TN1841) with a variety of interface functions for the switching module, peripheral interface control bus, peripheral interface data bus, and service announcement system memory.

Service Announcement System Memory Board (SASMEM)
A SASMEM is a board that uses personal computer memory card industry association flash memory cards to support speech recording at a rate of 422 seconds of speech per 4 megabytes of memory.

Screening

Screening is a translation process to determine what type of treatment to give a line. Screening information is used in the routing process.

Serial Time Slot Interchange Control Link (STCL)
Serial Time Slot Interchange Control Link.

Service Announcement System (SAS)
The SAS feature supports automatic collect call and requires speech recognition, digit reception, call progress monitoring, and the recording and playback of a caller's name on a per-call basis. Each SAS unit can provide up to 32 independently phased announcement channels.

Service Group (SG)
An SG is a maximum set of resources which can be affected by a single hardware fault.

Service Group 0 (SG0)
Service Group 0.

Service Group 1 (SG1)
Service Group 1.

Service Measurements
Service measurements provide data used to evaluate the quality of telephone service to the customer.

Signal Processor (SP)
An SP is circuitry in the switching module that performs supervisory scanning. It also detects incoming bylink pulses from step-by-step offices.

Signaling Connection Control Part (SCCP)
The SCCP is part of the ITU-T number 7 signaling protocol and of the signaling system 7 protocol. The SCCP provides additional routing and management functions for transfer of messages other than call setup between signaling points.

***SLC*® 96 Carrier**
The *SLC*® 96 Carrier is a digital loop carrier pair gain system used as a supplement or replacement for cable. It serves up to 96 subscribers over T1 transmission facilities.

Small Computer System Interface (SCSI)
The SCSI is an industry standard interface between a central processor (in *5ESS*® switching units this is the AM) and peripherals (that is, hard disk drives) which also conform to the SCSI standard.

Small Scale Integration (SSI)
SSI refers to micro electronic components which combine fewer transistors on an integrated circuit than large scale integration.

Software Change Administration and Notification System (SCANS)
SCANS is a dial-up system that uses a 2048 data set to distribute software changes in stored program control programs to the telephone company in the form of software updates. SCANS serves the responsible switching control center system.

Software Release
The software release is a fixed software program that makes up the basic operating system and is the same in all switch offices with the same program name and issue. It uses individual office translations to accommodate custom features for different installations.

Software Update
Software update is an electronic message containing a software release ``fix'' or update that is disseminated on a priority or urgent basis.

Some Tests Failed (STF)
STF is a message that acknowledges some diagnostic tests failed.

Space Division
Space division is a method of serving a number of simultaneous calls by assigning different physical transmission paths through a switching network to those calls. In the *5ESS*® switch, the time-multiplexed switch does space division switching.

Static Memory
Static memory is equipment used to store information which is changed infrequently, such as, characteristics of a particular telephone office (types and amounts of equipment, lines, trunks) and features associated with telephone numbers. Static memory, static data, and office dependent data are used interchangeably.

Static Random Access Memory (SRAM)
SRAM is a form of random access memory that retains its data without the constant refreshing that dynamic random access memory requires.

Storage Module Device (SMD)
SMDs are disk drives.

STSX-1
The STSX-1 is an electrical interface that has a synchronous transport signal -1 format conforming to the synchronous optical network standard.

STSX-1 Facility Interface (SFI)
SFI pairs in the digital network unit-synchronous optical network implement a duplicated electrical interface for six STSX-1 links. The SFI implements STSX-1 line drivers and receivers, implements bipolar 3-zero substitution encoding and decoding, and interfaces each of the six STSX-1 links to either one service transmission multiplexer or the spare transmission multiplexer.

STSX-1 Link Interface (SLI)
An SLI is a passive circuit containing a splitting transformer for coupling the received STSX-1 signal and two STSX-1 facility interface circuit packs and another transformer that couples the STSX-1 transmit signals from two STSX-1 facility interfaces to the facility. It also implements a line build out function on short links.

Subscriber Line Instrument Measurement [SLIM(2)] Board
The SLIM(2) (TN1422) is an optional board in the modular metallic services unit. The SLIM(2) is designed to do measurements on analog and digital subscriber lines as well as analog trunks. It will measure the metallic characteristics of the line/trunk such as voltages, insulation resistances, and capacitances. SLIM(2) can be operated in both Operator Mode (trunk and line work station 5700 page, similar to the directly connected test unit page) and Routine Mode (recent change driven, similar to the automatic line insulation test).

Subscriber Loop Interface Module (SLIM)
The SLIM replaces the standard office repeater bay used in direct Mode I or II interfaces and terminates T-carrier from Mode III shelves in D4 format.

Subunit Interface Bus (SUIB)
The SUIB connects the switching module processor and the time slot interchange unit.

Supplementary Trunk Line Work Station (STLWS)
The STLWS is additional (one or more) trunk test facilities (digital), usually in larger offices, that provide access to the trunk and line work station by way of the master control center. The STLWS need not be physically close to the master control center.

Switching Control Center (SCC)

The SCC is a central location from which the operations for one or more switches can be monitored and controlled.

Switching Control Center System (SCCS)
The SCCS is a system that centralizes control, administration, and maintenance of the switching systems for several central offices.

Switching Delay
A switching delay is the time from arrival of sufficient address information until the exchange starts sending a seizing signal on an outgoing circuit, a calling signal on a subscriber line, or another appropriate indication (for example, congestion tone).

Switching Module (SM)
The SM connects all external lines and trunks to the switch and handles most of the call processing tasks. The SM converts signals received from the lines and trunks into internal digital time-division format of the office.

Switching Module-2000 (SM-2000)
The SM-2000 provides the same basic functionality as the switching module, but the SM-2000 can provide many more terminations and supports additional features.

Switching Module Controller (SMC)
The SMC cabinet is equipped with units that are common to all switching modules, which includes: switching module processor and time slot interchange unit (module controller and time slot interchange unit or module controller and time slot interchange unit model 2), memory expansion unit (optional in the module controller and time slot interchange unit), local digital service unit or digital service unit - model 2 (not required with the module controller and time slot interchange unit model 2), and the digital service circuit.

Switching Module Processor (SMP)
The SMP is a part of the switching module that performs call-processing functions for lines and trunks terminating on the switching module and maintenance functions for the switching module equipment. There are two SMPs (an active and standby) in each switching module. Each SMP is augmented by a separate signal processor located in the time slot interface unit.

Switching Module Processor Unit (SMPU)
The SMPU is a part of the switching module and consists of a duplicated switching module processor (model 2) and the bootstrapper.

Switching Module Processor Unit - Model 5 (SMPU5)
The SMPU5 integrates digital service circuit - model 3 functions into the unit, employs a CORE60 processor board with additional integrated dynamic random access memory, and an application controller board.

Synchronous Optical Network (SONET)
SONET is the North American standard for digital hierarchy high bit rate transport systems used in fiber optic transmission (51 Mbps - 622 Mbps).

Synchronous Transport Signal Level 1 (STS1)
STS1 is a signal that is converted to or from the synchronous optical network signal format (equivalent to 51.480 megabytes per second).

System Process
A system process is a software process that exists as long as the switch is functioning. System processes are associated with non-call-processing tasks such as maintenance and billing functions.

T1
A T1 is a 24-channel pulse code modulation channel wire or cable transmission medium operating at a

rate of 1.544 megabytes per second.

Telephone Number (TN)
A TN is a seven-digit telephone number made up of a three-digit central office code and a four-digit station number. It is also called a dialing number.

Telephone Equipment Order (TEO)
A TEO is an order to Lucent specifying equipment required to construct the desired switch office.

Teletypewriter (TTY)
The TTY is an output device used to print information within the switch in a legible form. It is an outmoded term from a time when teletypewriters were the only visual output device.

Teletypewriter Controller (TTYC)
The TTYC is an output port that sends data to the teletypewriter device.

Terminal Equipment Number (TEN)
The TEN is a seven-digit number used in translation to identify the location of a digital carrier line unit channel or trunk circuit.

Terminal Process
A terminal process is a software process in the switching module processor which controls a terminal (line, trunk, or channel) during a call or call attempt. The terminal process is created and exists only as long as the terminal it controls is active.

Time Division
Time Division is a method of serving a number of simultaneous calls by assigning different time slots through a switching network to those calls. The time slot interchanger does time division switching.

Time Slot (TS)
A TS consists of eight consecutive bits of data, and is the smallest switchable data unit. In time division multiplexing or switching, the slot belonging to a voice, data, or video conversation.

Time Slot Groups (TSGRPs)
A TSGRP is made up of 32 time slots.

Time Slot Interchanger (TSI)
The TSI is an equipment arrangement in the switching module that takes information coming to it or from the time-multiplexed switch and switches it onto the time slot corresponding to the line or trunk involved in the call.

Time Slot Interchange Common (TSICOM)
The TSICOM provides the control interface to the switching module processor and is responsible for the synchronization timing for the switching module.

Time Slot Interchange Slice (TSIS)
The TSIS circuit pack switches time slots for the SM-2000.

Time Slot Interchange Unit (TSIU)
The TSIU is the part of the switching module that performs time slot switching. The TSIU consists of a time slot interchanger, data interface, dual link interface, control interface, and signal processor.

Time Slot Interchange Unit - Model 4 (TSIU4)
The TSIU4, a component of the SM-2000, can be grown to 30,000 network time slots compared to 512 network time slots of the existing switching module.

Time Slot Interchange Unit - Model 4, Version 2 (TSIU4-2)
The TSIU4-2 sends subscriber data between the time slot interchanger and peripheral units via the

peripheral interface data buses.

Time Slot Management Channel (TMC)
The TMC is a 64-Kbps channel used to report originations on non-integrated services digital network lines terminating on the remote terminal.

Time-Multiplexed Control Unit (TMCU)
The TMCU is a single-shelf assembly that terminates network control and timing links from the message interface clock unit and is equipped with the overall control circuit packs for the time-multiplexed switch. Positions are provided for seven control and interface packs in addition to space for two power converters.

Time-Multiplexed Switch (TMS)
The TMS, one of two switches that comprise the communication module model 1, performs the time-shared space division switching such as voice and data between any two switching modules or between an switching module and the administrative module. The message switch is the other switch in communication module model 1.

Time-Multiplexed Switch Expansion (TMSX)
The TMSX terminates link pairs (network control and timing number 2) in the Global Messaging Server.

Time-Multiplexed Switch Foundation (TMSF)
A circuit pack (MMC100) in the Global Messaging Server Communication Module Unit, Model 2 that provides functions such as clock synchronization and control, link pairs (network control and timing 2) terminations, quad link packet switch function, and test functions.

Time-Multiplexed Switch Network Control and Timing Link (TMSLNK)
See network control and timing.

Time-Multiplexed Switch Unit (TMSU)
The TMSU is circuitry within the time-multiplexed switch that terminates 30 network control and timing links and performs space switching of the time slots received.

Time-Multiplexed Switch Unit Model 2 (TMSU2)
The TMSU2 is a version of the time-multiplexed switch unit which breaks down further into field replaceable units. TMSU2 units cannot be mixed with time-multiplexed switch unit model 3 units in the same cabinet.

Time-Multiplexed Switch Unit Model 3 (TMSU3)
The TMSU3 is a version of the time-multiplexed switch unit which is functionally identical to the time-multiplexed switch unit model 2, but has fewer physical components. TMSU3 units cannot be mixed with time-multiplexed switch unit model 2 units in the same cabinet.

Time-Multiplexed Switch Unit Model 4 (TMSU4)
Used in the Global Messaging Server, the TMSU4 provides 24 even and 24 odd network control and timing number 2 links.

Tone Decoder (TD)
The TD resides in the local digital service unit of the switching module and performs digit reception and decoding functions for dial pulse and touch-tone originating calls from lines.

Traffic Measurements
Traffic measurements provide the current status of the *5ESS*® switch as well as indications to support the switching system with additional resources.

Transmission Control Protocol/Internet Protocol (TCP/IP)
TCP/IP are networking protocols that provide communication across interconnected networks and

between computers with different hardware architectures and various operating systems. TCP/IP is also used to denote the family of common internet protocols.

Transmission Multiplexer (TMUX)
The TMUX performs the format conversion of data between one STSX-1 link and 14 bi-peripheral interface data bus structures, which includes the mapping of data time slots between the two formats and signaling bit format conversion. It also performs functions associated with terminating the STS-1 synchronous optical network and facility overhead which include: STS-1 line and section overhead termination; STS-1 path overhead termination and virtual tributary extraction; digital signal level 1 framing and extraction; detection of digital signal level 1 facility alarms; digital signal level 1 cyclic redundancy code checking; digital signal level 1 facility data link extraction; initial collection of STS-1 and digital signal level 1 performance monitoring data and facility data alignment to the system clock.

Transmission Rate Conversion Unit - Model 2 (TRCU2)
The TRCU2 is used for rate conversion from the network control and timing rate to the digital signal level 3 transmission rate.

Transmission Rate Conversion Unit - Model 3 (TRCU3)
Transmission Rate Conversion Unit - Model 3.

Trunk
A trunk is a facility between two different entities, such as central offices and sections of the same switching system, that is used for transmission and/or signaling.

Trunk Circuit
The trunk circuit of a switching system is used to supervise a connection within the system and/or to associate the system with a transmission facility or another switching entity.

Trunk Unit (TU)
A TU is hardware that terminates 64 local or toll interoffice analog trunks without concentration. A minimum of one is required for each office.

Trunk and Line Work Station (TLWS)
The TLWS provides local access for lines and trunks, is an interface for circuit administration, and supports portable testing equipment for the switch.

Tuple
A tuple is a row in a data table (relation).

Two-Mile Optically Remoted Module (TRM)
A TRM is a switching module located up to 2 miles from the communication module and connected by a multimode optical fiber that serves as an extended network control and timing link.

Two-Party Service
Two-party service provides telephone service to a maximum of two customers on a common terminal appearance on the network.

Uniform Call Distribution (UCD)
UCD is a type of line hunting providing an even distribution of incoming calls among the available members of a hunt group.

Universal Conference Circuit (UCC)
The UCC is a service circuit (three- or six-port) used to connect three to six customers for service features.

Universal Tone Decoder (UTD)
The UTD decodes dial pulse, multifrequency, and touch-tone signals.

Universal Tone Generator (UTG)
the UTG creates digital tones for touch-tone, busy tone, dial tone, and multifrequency.

Very Compact Digital Exchange (VCDX)
The VCDX switch, based on the *5ESS*® switch, brings advanced digital services, including wideband data and video capabilities, to telecommunication service providers. The VCDX switch provides: virtually non-blocking access between non-concentrated switch terminations, integration of voice and digital data services into a single switch, direct digital interfacing with digital facility terminations, signaling and transmission treatment by an interface unit, testing access to modular metallic facilities as an integral part of the interface units, and conversion potential to a full-size *5ESS*® switch or remote.

Video Display Terminal (VDT)
A VDT is a nonmechanical output device, such as a cathode ray tube monitor or liquid crystal diode screen common to personal and laptop computers.

Virtual Terminal (VT)
A VT emulates the operation of a real terminal.

Voice Frequency Data Enhancement (VFDE)
VFDE is a *5ESS*® switch feature that allows a given digital signal level 0 to use the clear channel mode of operation.

Voice Path Assurance (VPA)
VPA is a test providing a voice path for common channel signaling trunks. This test ensures the integrity of the voice path since the voice and signaling paths are separated on common channel signaling trunks.

Web and Media Management (WMM)
WMM is an electronic documentation delivery systems which provide support for single-user applications or more broad-based multi-user network applications. The *5ESS*® switch support documentation is delivered in the form of electronic user guides, on-line tutorials, or job-aids.

Wide Area Telecommunications Service (WATS)
WATS is a discounted toll service provided by long distance and local telephone companies.

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