5ESS®-2000 Switch
3B21D Computer Hardware Reference Manual

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1. INTRODUCTION

1.1 PURPOSE

This *Hardware Reference Manual* describes the 3B21D computer, providing both physical and functional information. It is part of a documentation set that supports the 3B21D computer. See Section 10 for other Lucent Technologies documents that support the 3B21D computer.

1.2 UPDATE INFORMATION

Along with other network switching products, the *5ESS*® switch product line is being positioned to support Service Net-2000 (SN-2000). Therefore, the name of the switch has been changed to *5ESS*®-2000 switch. However, these name changes have not been carried forward into software-influenced items, such as input/output messages, Master Control Center screens, Recent Change/Verify screens, etc.

This manual is reissued to add information about the UN376E and UN597 circuit packs, and is a complete update for the 5E13 software release. And Chapter 4 was reorganized into three chapters. (See Section **1.3 DOCUMENT ORGANIZATION**.)

The Lucent Technologies Network Systems organization reserves the right to revise this document for any reason. The reasons for revision will include, but are not limited to: conformity with standards declared by ANSI, the Electronic Industrial Association (EIA), International Telecommunications Union-Telecommunications Standardization Sector (ITU-T), International Telegraph and Telephone Consultative Committee (CCITT), International Standards Organization (ISO), or similar agencies; advances in the state of the technical arts; or changes in the requirements of communications systems or equipment.

1.3 DOCUMENT ORGANIZATION

This manual is organized into the following sections and reference information (Table of Contents, Glossary, and Index). Specific topics are referenced in the "Table of Contents" and in the "Index" with page number locations. The "Glossary" defines the terms used in this manual.

This manual provides physical and functional descriptions of the 3B21D computer. The remainder of this document is organized into the following sections:

- Section 2 , System Overview
- Section 3 , 3B21D Computer Configurations
- Section 4 , 3B21D Computer Physical Description
- Section 5 , System Overview and Control Unit Functional Description □ CC
- Section 6 , Control Unit Functional Descriptions □ MAS, MASU, DMA, DSCH, UC, and EX
- Section 7 , Peripheral Device Functional Descriptions □ DFC, IOP, PC, and PSSDB
- Section 8 , Storage and Peripheral Devices
- Section 9 , Power Distribution and Control
- Section 10 , Documentation Roadmap
- Section 11 , System Specifications
- Section 12 , Connector and Cabling Information

- Glossary
- Index.

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2. SYSTEM OVERVIEW

2.1 GENERAL DESCRIPTION

The 3B21D computer is a high-speed, high-reliability, fault-tolerant, duplex computer. It is a bit-compatible version of the 3B20D computer, which is used in various roles in Lucent Technologies switching products. All major functional units are duplicated to ensure uninterrupted and reliable service.

The hardware contains self-checking and error-correction circuitry. The software detects faulty processes and equipment, reconfigures or reinitializes the system, and diagnoses and identifies faulty equipment.

2.2 APPLICATIONS

The 3B21D computer is used as the administrative module (AM) in the *5ESS*®-2000 switch.

2.3 SYSTEM ARCHITECTURE

The high-level architecture of the 3B21D computer is similar to that of the 3B20D computer except for the addition of Expansion (EX) slots in the 3B21D computer Control Unit (CU) complex, the maximum main store memory configuration is increased from 64 MB to 128 MB (see Note), and the support of Small Computer System Interface (SCSI) peripheral devices. The 3B21D computer hardware is packaged differently.

NOTE: The current maximum configuration of the main store memory is 128 MB; however, the system buses and registers support a 28-bit address to accommodate a future main store memory maximum of 256 MB.

The advantages of the 3B21D computer are reduced floor space and higher reliability because of a reduction in integrated circuits.

The 3B21D computer hardware consists of the following cabinets:

- Basic processor cabinet
- Growth cabinet (optional).

Figure 2-1 is a block diagram of the 3B21D computer.

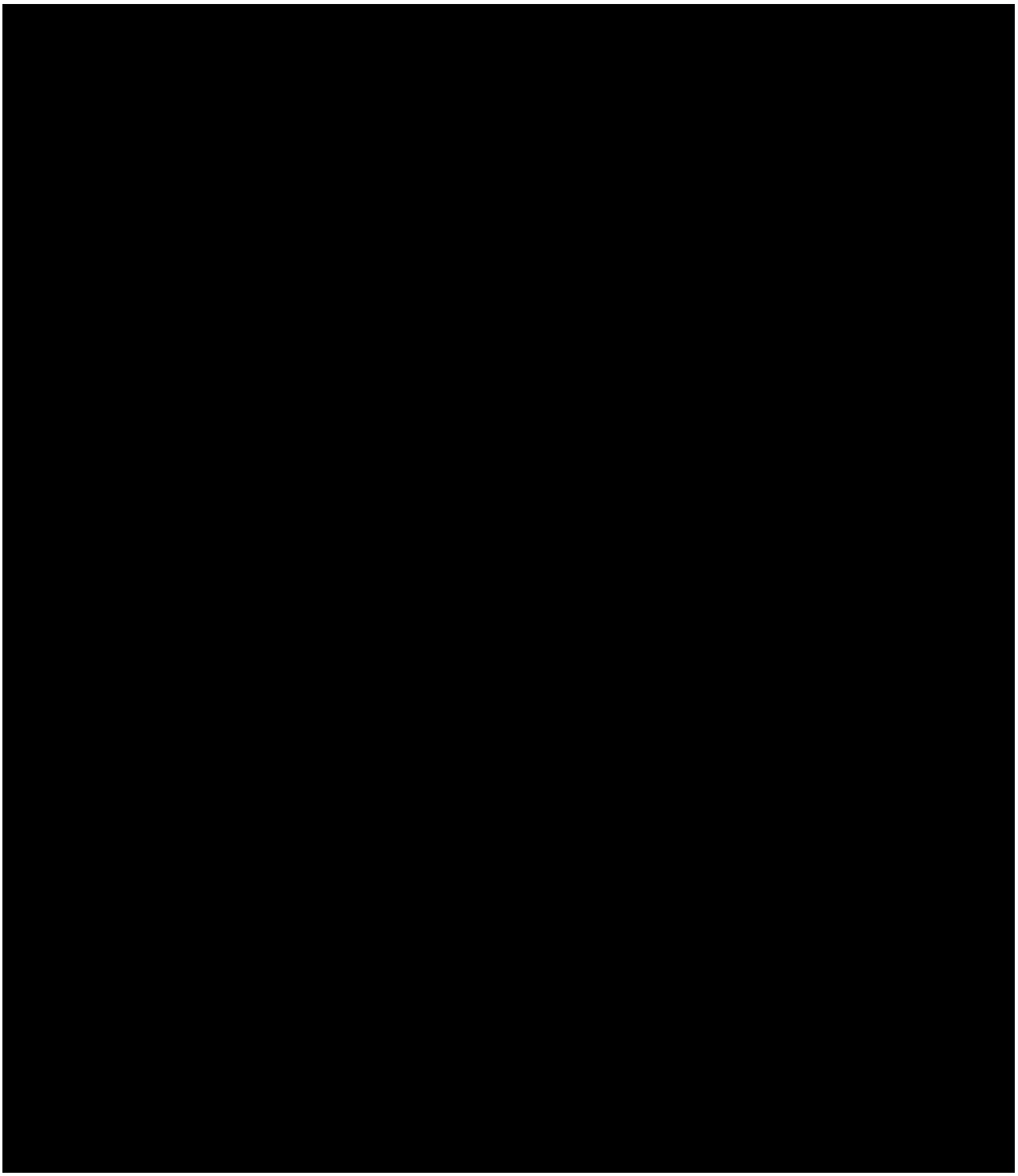


Figure 2-1 3B21D Computer System Block Diagram

2.3.1 Control Unit (CU)

Each Control Unit (CU) consists of the following functions:

- Central Control (CC)
- Cache Storage Unit (CSU)
- Main Store (MAS) and Main Store Update (MASU)

- Direct Memory Access (DMA 0 and DMA 1)
- Expansion Slots (EX 0 and EX 1)
- Utility Circuit (UC).

Each Control Unit is half of the duplexed Central Processing Unit (CPU) system. The CC, MAS, UC, EX, and input/output (I/O) functions are duplicated for reliability. Local control of the 3B21D computer for normal operation and manual recovery procedures is via the Emergency Action Interface (EAI) to a Maintenance TTY (MTTY) and Receive-Only Printer (ROP).

2.3.1.1 Central Control (CC)

The 3B21D Central Control (CC) is a microprogram-driven machine modeled after the 3B20D CC. The CC contains the following functional subsystems:

- Circuit pack identification capability
- MicroController (MC)
- MicroInstruction Store (MIS)
- Maintenance Channel (MCH)
- Emergency Action Interface (EAI)
- Data Manipulation Unit (DMU)
- Special Registers (SREGs)
- Store Address Interface (SAI)
- Store Data Interface (SDI)
- Store Address Translator (SAT)
- Cache Storage Unit (CSU)
- Micro Level Test Set (MLTS) Interface.

2.3.1.2 Expansion Slots (EX 0 and EX 1)

The Expansion (EX) slots provide an interface for new (future) hardware features to access the MAS and CC via the Central Control Input/Output (CCIO) bus and the Main Store Bus (MASB). Each CU has two EX slots, EX 0 and EX 1.

2.3.1.3 Utility Circuit (UC)

The Utility Circuit (UC) is an optional function that monitors operations between the CC and the main memory (cache or main store) for the purpose of program debugging and testing. One UC circuit pack (UN379) is optionally equipped in each CU.

2.3.1.4 Cache Storage Unit (CSU)

The Cache Storage Unit (CSU) provides a small, high-speed CC cache memory for the most recently accessed MAS words. The CC accesses the CSU concurrently with the MAS access on the MASB. The

CSU is part of the CC circuit pack (KLW31).

2.3.1.5 Main Store (MAS) and Main Store Update (MASU)

The Main Store (MAS) provides a minimum of 32 MB to a maximum of 256 MBs of Dynamic Random Access Memory (DRAM). One MAS circuit pack (KLW32, KLW40, KLW48, KLW64, or KLW128) is equipped in each CU. The same size MAS circuit pack is used in each CU. The KLW32 circuit pack is initially equipped with 32 MB of DRAM. The KLW40 circuit pack is initially equipped with 40 MB of DRAM. The KLW48 circuit pack is initially equipped with 48 MB of DRAM. The KLW64 circuit pack is initially equipped with 64 MB of DRAM. The KLW128 circuit pack is initially equipped with 128 MB of DRAM. Additional memory is added to a MAS circuit pack in either 8 MB or 32 MB increments. The addition of three 32-MB Single In-line Memory Modules (SIMMs) to a KLW32 circuit pack provides a current maximum of 128 MBs of DRAM. Twenty eight bits of address is designed into the system buses and registers for future expansion to 256 MB. Store data is 36 bits (32 data bits and 4 parity bits). However, in the MAS circuit pack, store data is 39 bits wide (32 data bits and 7 parity/check bits). The MASs in both CUs are kept coherent using the Update Bus. If control must be switched from the on-line processor to the other processor, the contents of both the off-line memory and the on-line memory must be identical. If the MASs are not coherent, the on-line processor must copy its data to the off-line MAS before the switch takes place.

2.3.1.6 Direct Memory Access (DMA)

The Direct Memory Access (DMA) provides peripheral devices access to the MAS via the MASB and provides the CC access to the peripheral devices through the CCIO bus. Each DMA supports connections for a maximum of 16 peripheral devices.

Peripheral devices are connected to the DMA through the Dual Serial Channel (DSCH). These devices have a dual-ported DSCH interface that allows them to communicate with either CU 0 or CU 1. Two DMA circuit packs (KBN15s) can be equipped in each CU. DMA 0 is standard and DMA 1 is optional.

The relationship of peripheral devices to DMA 0 and DMA 1 is as follows:

- DMA 0 and DMA 1 each provide four channels. DMA 0 supports channels 11, 12, 13, and 14. DMA 1 supports channels 16, 17, 18, and 19.
- Each channel supports four DSCH interfaces.

2.3.2 Peripheral Devices

Figure 2-1 shows three types of peripheral devices:

- Input/Output Processor (IOP)
- Disk File Controller (DFC)
- Communications Module/Communications Network Interface (CM/CNI).

The IOP provides connections to terminals, networks, and some tape devices. The DFC provides connection to peripherals with SCSI interfaces, which include disk and tape drives. The third device, CM/CNI, represents application peripheral hardware. The term "DFC" is not accurate since support is not limited to disk peripherals; however, the nomenclature is retained from the 3B20D computer.

Note that the 3B21D computer differs from the 3B20D computer in that 9-track tape is an SCSI peripheral device supported by the DFC in the 3B21D computer while it is supported by the IOP in the 3B20D computer. Also note that 3B21D computer DFC channel and device allocations differ from the 3B20D computer in that there are fewer devices per channel.

2.3.2.1 DFC Equipped with UN373 and TN2116

The 3B21D computer can have three DFCs (DFC 0 through DFC 2). DFC 0 is equipped in the Processor Cabinet, Processor Unit 0 at EQuipment Location (EQL) 28-170 and EQL 28-178. DFC 1 is equipped in the Processor Cabinet, Processor Unit 1 at EQL 53-170 and EQL 53-178. DFC 2 is equipped in the Processor Cabinet, Growth Unit at EQL 11-172 and EQL 11-180. Each DFC provides two SCSI buses (SBUS A and SBUS B). A maximum of seven SCSI peripheral devices can be equipped on an SCSI bus. Therefore, each DFC can support a maximum of 14 SCSI devices. DFC 0 provides two SCSI buses, SBUS 0(A) and SBUS 2(B). DFC 1 provides two SCSI buses, SBUS 1(A) and SBUS 3(B). DFC 2 provides two SCSI buses, SBUS 4(A) AND SBUS 6(B).

2.3.2.2 DFC Equipped with UN580

The 3B21D computer can have three DFCs (DFC 0 through DFC 2). DFC 0 is equipped in the Processor Cabinet, Processor Unit 0 at EQL 28-178. DFC 1 is equipped in the Processor Cabinet, Processor Unit 1 at EQL 53-178. DFC 2 is equipped in the Processor Cabinet, Growth Unit at EQL 11-180. Each DFC provides two SCSI buses (SBUS A and SBUS B). A maximum of seven SCSI peripheral devices can be equipped on an SCSI bus. Therefore, each DFC can support a maximum of 14 SCSI devices. DFC 0 provides two SCSI buses, SBUS 0(A) and SBUS 2(B). DFC 1 provides two SCSI buses, SBUS 1(A) and SBUS 3(B). DFC 2 provides two SCSI buses, SBUS 4(A) and SBUS 6(B).

2.3.2.3 Input/Output Processor (IOP)

The 3B21D computer can have four IOPs (IOP 0 through IOP 3) equipped in the Processor Cabinet. IOP 0 is equipped in Processor Unit 0 at EQL 19-065. IOP 1 is equipped in Processor Unit 1 at EQL 45-065. IOP 2 is equipped in the Growth Unit at EQL 11-011. IOP 3 is equipped in the Growth Unit at EQL 62-011.

Functionally, an IOP can support four peripheral controller communities with each community supporting four peripheral controllers. Therefore, 16 peripheral devices can be supported by an IOP. IOP 0 and IOP 1 are exceptions. IOP 0 and IOP 1 each support up to 15 Peripheral Controller (PC) slots. IOP 2 and IOP 3 each support up to 16 PC slots. The maximum number of available PC slots in a Processor Unit is 15; the maximum number of available PC slots in a Growth Unit is 16.

For IOP 0 and IOP 1, peripheral community 0, slot 0 (PC00) is always equipped with a TN983, UN583, or UN597 MTTY Controller (MTTYC) circuit pack. Also, IOP 0 and IOP 1, peripheral community 0, slot 2 (PC02) is reserved for a UN33D or UN933 Scanner and Signal Distributor circuit pack, which provides scan and signal distributor point interfaces for the 3B21D computer.

2.3.3 Port Switch and Scanner-Distributor Buffer (PSSDB)

The Port Switch and Scanner-Distributor Buffer (PSSDB) switches the MTTY and the local receive-only printer (ROP) between the MTTY Controller (MTTYC) circuit pack (TN983, UN583, or UN597) in IOP 0 and IOP 1. The PSSDB also buffers the scanner and signal-distributor controller from non-3B21D computer circuits such as office alarms, smoke detectors, and security monitoring devices. One port switch is equipped in Processor Unit 1. In the 3B21D computer, the PSSBD is located in CU 1. (Note that in the 3B20D computer, the PSSBD is located in CU 0.)

2.4 HARDWARE FEATURES

2.4.1 Reduced Floor Space

For Release 1, the 3B21D computer system is packaged in one, two, or three cabinets. The Processor Cabinet (J3T060A-1) is always required. One or two Peripheral Growth Cabinets (J3T059A-1) are provided as necessary when 9-track SCSI tape drives are required as part of the configuration. The Peripheral Growth Cabinets are always located to the right of the Processor Cabinet.

Each cabinet measures about 72 inches (183 cm) high by 30 inches (76 cm) wide by 24 inches (60 cm)

deep. A three-cabinet lineup occupies an area about 90 inches (229 cm) wide by 24 inches (60 cm) deep.

2.4.2 Application Specific Integrated Circuit (ASIC) Technology and Packaging

The 3B21D computer uses Complementary Metal Oxide Semiconductor (CMOS) Gate Array Technology in the form for Application Specific Integrated Circuits (ASICs). The ASICs are fabricated in a one-micron, two- or three-layer, metal process.

All 3B21D computer gate arrays are in surface-mounted packages. The largest package is a 240-pin Plastic Quad Flat Pack (PQFP). Plastic-Leaded Chip Carriers (PLCCs) are used for ASICs requiring 100 or fewer pins. Table 2-1 summarizes the 3B21D computer ASIC surface-mounted packages.

Table 2-1 3B21D Computer ASIC Summary

ASIC NAME	PACKAGE
CENTRAL CONTROL CIRCUIT PACK (KLW31/KLWCC)	
Cache Controller (CAC)	160 PQFP
Data Manipulation Unit (DMU)	240 PQFP
Maintenance Channel (MCH)	240 PQFP
MicroSequencer (MSEQ)	240 PQFP
Special Registers (SREGs) [a]	240 PQFP
Store Address Interface (SAI) [b]	240 PQFP
Store Address Translator (SAT)	240 PQFP
Store Data Interface (SDI) [b]	240 PQFP
MAIN MEMORY CIRCUIT PACK (KLW32/KLWMM)	
Memory Controller with Error Regulation and Test (MCERT2) [c]	160 PQFP
DIRECT MEMORY ACCESS CIRCUIT PACK (KBN15/KBNDMA)	
Direct Memory Access Controller (DMAC)	240 PQFP
INPUT/OUTPUT PROCESSOR 2 CIRCUIT PACK (KBN10/KBNIOP)	
Duplex Dual Serial Bus Selector/Bus Interface Controller (DDSBS/BIC)	120 PQFP
Input/Output Microprocessor Interface (IOMI)	160 PQFP
Peripheral Interface Controller/Sequencer (PIC/SEQ)	160 PQFP
DISK FILE CONTROLLER CIRCUIT PACK (UN373/DFCA)	
Duplex Dual Serial Bus Selector (DDSBS)	208 PQFP

Notes:

a. Two SREGs are used, SREG0 (Bits 15-00) and SREG1 (Bits 31-16).

b. Two Store Interfaces are used for the SAI and SDI function.

c. Modification of existing 0.9 CMOS code.

2.4.3 Circuit Pack Types

The functional blocks shown in Figure 2-1 are physically represented by the following circuit pack designs:

410AA DC-to-DC converter circuit pack provides +5 V DC from -48 V DC.

KBN10 Input/Output Processor (IOP) circuit pack contains the DSCH and IOMI interface functions.

KBN15 Direct Memory Access (DMA) circuit pack contains the DMAC and Channel functions.

KLW31 Central Control (CC) circuit pack contains the CC and Cache Storage Unit (CSU) functions.

KLW32, KLW40, KLW48, KLW64, or KLW128 The Main Memory (MM) circuit pack contains the MAS and Update functions. The KLW32 is initially equipped with 32 MB; KLW40 is initially equipped with 40 MB; KLW48 is initially equipped with 48 MB; KLW64 is initially equipped with 64 MB; KLW128 is initially equipped with 128 MB.

KLW__ The Expansion (EX) circuit pack is for future development.

TN74B Terminal Controller circuit pack.

TN75C Synchronous Data Link Controller circuit pack.

TN82B X.25 Synchronous Data Link Controller circuit pack.

TN983 Maintenance TTY Controller circuit pack.

TN1420 Synchronous Data Link Controller circuit pack.

TN1820 Input/Output Processor Power Switch (IOPPS) circuit pack is similar to the TN1821 circuit pack with additional onboard DC-to-DC (□12 V and -5 V) power converters.

TN1821 Control Unit Power Switch (CUPS) circuit pack contains power and control for the Central Control fault group.

TN1839 Synchronous Link Peripheral Controller□X.25 Network Level 2 Interface (NET2) circuit pack.

TN2116 and UN373 Disk File Controller A (UN373) and Disk File Controller B (TN2116) circuit packs contain the DSCH interface and SCSI host adapter functions.

UN33 Scanner and Signal Distributor circuit pack.

UN375 SCSI Disk circuit pack contains a 3.5-inch SCSI Moving Head Disk (MHD) drive, power converters for the drive, and power control. This circuit pack provides the MHD functions for the AM. On the UN375E series, an MHD with a single-ended SCSI interface is used. The UN375E series requires the addition of a differential-to-single-ended translation circuit.

UN376 SCSI Tape circuit pack contains a 3.5-inch SCSI Digital Audio Tape (DAT) drive, power converters for the drive, and power control.

UN377 Port Switch and Scanner-Distributor Buffer (PSSDB) circuit pack contains the PSSDB function.

UN379 Utility Circuit circuit pack contains the utility circuit function.

UN580 Disk File Controller circuit pack combines the functionality of TN2116 and UN373 into one circuit pack. The UN580B does not use an external power converter.

UN582 The UN582 circuit pack is a Synchronous Data Link, High-Speed Synchronous Data Link, and an Asynchronous Data Link Peripheral Controller that replaces the TN82B, TN74B, TN75C, and TN1839 circuit packs.

UN583 Maintenance TTY Controller circuit pack that replaces the TN983.

UN597 Maintenance TTY Controller circuit pack that replaces the UN583.

UN933 New Scanner and Signal Distributor circuit pack that replaces the UN33 with identical functionality.

2.4.4 Configurability and Growth

The 3B21D computer system offers cost-effective configurations for small switching offices and can be grown from a small office configuration to a large office configuration. The minimum configuration is packaged in one Processor Cabinet. The maximum Release 1 configuration is packaged in one Processor Cabinet and two Peripheral Growth Cabinets.

See Section 3 for a description of the 3B21D computer configuration and growth information.

The 3B21D computer is configured for manufacturability and orderability in J3T061A-1.

2.5 RELIABILITY AND MAINTENANCE FEATURES

The 3B21D computer is more reliable than the 3B20D computer because of a reduction in the number of integrated circuits, circuit packs, backplanes, and cables. This reduction in the number of components and interconnections is the result of extensive use of Application Specific Integrated Circuits (ASICs).

The 3B21D computer makes use of the following features that contribute to the reliability and maintainability of the system:

- Control Units are duplexed.
- The standby memory is kept current via memory update.
- Maintenance exercise routines are run on the standby Control Unit.
- Various system sanity mechanisms with subsequent automatic recovery are used.
- Duplexed circuitry with matchers is used in addition to parity checking.
- Error detection and correction is used on main memory.
- Standard equipment designation strips for power and circuit pack labeling.
- Forced air cooling is used to keep components within their rated temperature ranges.
- The 3B21D computer system is factory assembled and is following environmental stress *ESS*^{TM} switch screening to increase product reliability.
- Except for the PC community circuit pack slots, all circuit pack slots are keyed to prevent the installation of a wrong circuit pack. The PC community slots are keyed to accept the installation of several different circuit pack types.
- Cabling design follows specific rules to enhance the reliability and maintainability of the system as follows:
  - All cables are stamped with the appropriate cable EQuipment Location (EQL) information.
  - Total cable length for a differential SCSI bus is 20 meters (65.6 feet), because of internal circuit limits.

2.5.1 Fault Detection

Fault detection algorithms make extensive use of local matching circuits, parity techniques on all buses, and hamming detection with single-bit error correction on the main store. Technology-dependent fault detection/correction strategies on disks, and numerous sanity timers throughout the control unit and peripherals are used as the primary fault-detection techniques. In addition, routine diagnostics are used to detect failures in the fault-detection hardware itself. Finally, system integrity checks catch certain subtle problems that are not caught by unique detectors.

When any of the unique detectors determine an error condition, an error interrupt (or error report in the case of certain peripherals) is registered in the processor. The most severe of these will result in automatic hardware sequences that switch the activity of the processors (hard switch). Less severe errors result in

microinterrupts that enter microcode and software charged with recovery of the system.

2.5.1.1 Bus Parity

Self-checking is made possible by carrying a parity check bit per byte in the processor. Since each microinstruction may involve a data transfer from one register to another via a common data bus, an effective parity check is done by trapping the data off the bus and checking for correct parity during the next clock interval (that is, the source bus parity error). This avoids added delay in the normal operation. The data in the destination register is not checked. However, when used as the source, the data is then checked. For any arithmetic or logical operations, the data goes through the DMU. The DMU is divided into two parts (DMU 0 and DMU 1) for checking purposes. The results from one is used as data, whereas parity check bits derived from the result of the second is used with the data. As data leaves the DMU, the common bus parity check is performed [that is, the Data Manipulation Unit (DMU) parity error]. In the microprogram store, additional bits are provided to check the control section of the processor (that is, the microcontrol parity error).

2.5.1.2 Dynamic RAM Error Detection and Correction

The Main Memory (MM) detects and corrects one-bit errors. All data is checked when read. All data is continually checked during refresh cycles. In a systematic way, all memory locations are checked over a time period dependent on the amount of memory equipped. The MM detects most multiple bit errors (two-bit and greater errors). Both classes of errors are recorded in the Error Register (ER) and generate a microinterrupt. Registers in the MM are accessible via software to assist in fault recovery.

2.5.2 Fault Recovery

The microcode and recovery software provides a layered approach to the recovery architecture. Fault-recovery strategies are based on the fault-tolerant architecture of the 3B20D computer. Major hardware units are fully duplicated. This duplication provides a high probability that a combination of operational units can be retained in the face of faults. The mate processors are only loosely coupled; interprocessor connections are limited to the maintenance channel and memory update circuitry. This architecture forms the foundation of the hardware recovery strategy used in the 3B21D computer, namely to isolate an entire faulty processor as opposed to attempting fault resolution at the subunit level.

The *UNIX*® Real-Time Reliable (RTR) system is a modular operating system that provides a wide range of protection from various types of classical errors. Examples include write-protected memory areas, memory ranges that are used only for text execution, and protected virtual address spaces. Thus, much of the recovery from these types of errors is built into the operating system. Recovery actions that are required are greatly simplified by the underlying architecture. Hard faults and other conditions requiring recovery actions are treated according to their severity. Fault categories that are described individually are: hard faults, Sanity Timer time-out, software-requested recovery, and threshold-exceeded faults.

Different types of faults can result in different actions. The most severe action taken is a system initialization or boot. The boot sequence is discussed later in this section.

2.5.2.1 Hard Faults

The 3B21D computer has built-in self-checking circuitry designed to detect hard faults as soon as they occur. This circuitry simplifies recovery since early fault detection limits the possible damage done by the fault. Faults in this category indicate that the processor is no longer capable of proper operation and results in an immediate stop of the currently running processor and a switch to the other processor (stop-and-switch). Since the other processor does not match the active processor instruction by instruction, an initialization sequence is required to start execution properly.

2.5.2.2 Sanity Timer Timeout

Each processor has a Sanity Timer (ST) that will result in an initialization if it times out and is not inhibited (disable Sanity Timer request). The System Integrity Monitor process in the active processor maintains both its own and the standby ST so that if the active processor is out of control, an initialization of the standby processor will be triggered by a Sanity Timer time-out.

2.5.2.3 Software-Requested Recovery

The system provides an Operating System Trap (OST) for use by software to request an initialization. This capability is used by critical system processes when they encounter errors that preclude performance of a critical system function. Initializations occur when an error or fault has been detected that cannot be recovered without a change in hardware and/or software status. A stop-and-switch to the other processor may or may not be associated with any given initialization. All initializations include actions of varying severity, depending on what is required to deal with various faults and errors.

2.5.2.4 Other Fault Sources

Some types of faults and errors are not severe enough to justify an immediate stop-and-switch recovery action. Examples of errors of this kind are hardware faults, which are detected in the standby processor memory, and software errors, such as write-protection violations. Another type of error in this category is hardware faults that are handled by self-correcting circuitry. Although most faults are detected by self-checking, some units, such as main memories, have fault rates that justify self-correcting capabilities. Disks are also self-correcting via cyclic redundancy codes. All errors in this class are reported to the recovery system as error interrupts.

Recovery software classifies the interrupt by type, gathers and saves all available information about the interrupt, and reports the error to the system configuration management package. If a particular software process is suspected as the cause of the interrupt, such as in a software-triggered event, the process that was running at the time of the interrupt is faulted and entered at its fault entry after a stable system configuration is guaranteed. The fault entry of a process contains recovery and initialization sequences that are special to the process involved.

2.5.2.5 Threshold-Exceeded Faults

All error interrupts are reported to configuration management. Errors are logged against the failing unit and error rates are compared to allowed error thresholds. If the affected threshold is exceeded, further action is required and is based on several factors. If the faulty unit is essential to the system and a mate unit is available, the faulty unit will be removed from service and scheduled for diagnostic testing. If there is no available mate unit, the faulty unit will be initialized and returned to service since, in the case of essential units, it is better to have a faulty unit than no unit. Nonessential units are removed and scheduled for diagnostic testing whenever their error thresholds are exceeded.

2.5.2.6 Boot Sequence

The following simplified description of the *UNIX*® RTR system boot sequence addresses the actions taken by the hardware, micro-code, and system software during and after a boot.

2.5.2.6.1 Hardware Actions

The first event in a hardware-initiated or manual initialization sequence is a hardware-supported transfer to a fixed location [Maintenance Reset Function (MRF)] in the CU microstore. Software-requested initializations begin executing at MRF without hardware assistance.

2.5.2.6.2 Microcode Actions

Data about the initialization trigger is first saved in temporary registers and later copied to Main Store. A decision is made to bring this processor on-line or stop for the off-line initialization. If the current

initialization is level two or higher, the writable microstore, appropriate processes, and databases are loaded from the mass-storage device (disk or tape). These and other boot time decisions that are made are supported by the System Status Register (SSR).

2.5.2.6.3 System Software Actions

The *UNIX*® RTR system kernel initialization or bootstrap routine is then called to restart system processes or to fault active processes as appropriate. The initialization is now complete and the system has returned to normal operation.

2.5.2.6.4 Reboot

If an initialization does not recover the system to an operational state, another and more severe initialization will occur. Any initialization that occurs during a window of time following the previous initialization will escalate to the next higher level. The length of the initialization interval is a system-generation parameter that is established by the application.

In addition to the *UNIX*® RTR system-initialization levels, provision is made for an application to specify software-controlled "application levels."

2.5.2.6.5 Post-Recovery Actions

Data about various recovery actions taken by the system is supplied to provide much information about what went wrong. This information can be used by maintenance personnel to assist them in isolating difficult faults. Recovery data is provided in several forms. Each error interrupt is accompanied by a printout containing available information about the state of the processor when the interrupt occurred. A more difficult problem is presented by initializations. Since they are more severe than interrupts and represent a discontinuity in processing, gathering and preserving error data is more difficult. Initializations, as well as interrupts, can occur at a rate much too fast for data to be printed. The solution is to save all pertinent data in a protected area of memory for printing after the system has recovered.

Various kinds of error data are not generally printed as a part of the standard system output but instead are saved in error files on the system disks. Examples of this data are device driver errors and failing memory data.

One piece of data output by the system that is not saved in error files are the Processor Recovery Messages (PRMs). These are low-level one-line messages that are printed in real time. The PRMs thus represent progress marks through the recovery sequences and are extremely useful in those cases where stability cannot be achieved or postmortem data cannot be gathered.

2.5.3 Maintainability and Craft Interface

The maintainability of the 3B21D computer is a vital component that guarantees the overall high availability required of the system. There are conditions where automatic recovery is unable to restore the system to a fully-functioning state. This is where maintainability is critical to satisfying *UNIX*® RTR system's high availability requirements. The hardware requirements imposed by the maintainability needs are not as obvious as those prescribed by other portions of the system. This section describes the maintenance capabilities provided by *UNIX*® RTR system. The 3B21D computer hardware has been designed to ease in the implementation of these features.

2.5.3.1 Maintainability Overview

The basic premise of maintainability is to provide basic data-gathering and data-analysis mechanisms as well as the ability to act on the results of that analysis. These mechanisms must be able to collect and analyze diagnostic and debugging information from various hardware and software components in the system to isolate the error. These mechanisms must then allow the craft to control and modify the

configuration of the system based on the diagnostic and debugging information collected. Furthermore, these mechanisms must yield their information as quickly as possible while disturbing the rest of the system as little as possible.

Maintainability includes such areas as diagnostics, transient error analysis, routine maintenance procedures, field utilities, and plant measurements. Once an error has been isolated and analyzed, the problem must then be corrected as quickly and benignly as possible. This is termed updatability, and includes such aspects as growth and retrofit for hardware, emergency fixes, function update, and system update for software. Maintainability is partitioned into diagnostics (hardware) and the various field utilities (software). However, the craft interface to the various maintenance facilities in the system is central to the craft's ability to maintain and control the 3B21D computer hardware and software. This is an important capability of the craft interface system. The craft interface provides the craft and others with the means to request diagnostics, receive error analysis reports, initiate emergency recovery procedures, gather plant measurements data, and exercise routine maintenance programs. In addition, the craft interface system allows configuration control by providing access to growth and retrofit procedures, system and function update capabilities, emergency fix facilities, and the various field utilities.

2.5.3.2 System Updatability

One component of the maintainability required of *UNIX*® RTR-based systems is the ability of these systems to accept hardware and software changes in a way that does not interfere with their primary tasks. In other words, a *UNIX*® RTR-based system must be able to accept changes without disturbing call processing, networking, or other critical functions. *UNIX*® RTR system supports this through the following aspects of updatability: growth, retrofit, software update, and program update.

2.5.3.2.1 Growth

The first aspect of updatability is growth. Growth is the ability to add or remove hardware and related software components to the running system. Growth extends from physically connecting new equipment (such as memory boards, disks drives, tape drives, and other units) through informing the system of its existence, exercising it, logically connecting it into the system's configuration, and committing to its use in the system. Other subsystems, such as hardware and software fault recovery and diagnostics, then take over to ensure that the new system component continues to be sane and usable.

2.5.3.2.2 Retrofit

The second aspect of updatability is retrofit. Retrofit is the ability to replace hardware components in the system with similar components of a different vintage or with different capabilities or interface characteristics. Retrofit procedures may remove (de-grow) old units and then grow or add new ones. They also may add the new units first and then transition work from the old units to the new. Thus, retrofit of units may involve extensive periods of time where old and new units coexist in the system. Retrofit may also involve substantial software changes to interact with new units and to recognize the existence of both old and new units.

2.5.3.2.3 Software Update

The third component of updatability, software update, deals exclusively with software and data file changes in the *UNIX*® RTR system. Such changes are done logically, on a file-by-file or functional level. Just as with growth and retrofit, software update can install new or replace system programs or files, inform the system about them, logically connect them into the system, exercise them in that state, and then commit to or back out of them. Software update is intended primarily for installing fixes or small features that do not disturb the system's architecture.

2.5.3.2.4 Program Update

The fourth updatability component, program update, allows program and data changes of much greater

magnitude, up to complete software program replacement. A bootstrap is required to install the changes for any program update. By using disk redundancy or backup copies of sections of *UNIX*® RTR program disks, program update can prepare a new, partial, or total version of the program on disk and then switch to it (and back, if necessary). Where software update performs a logical change of files, program update does a physical change of a set of partitions (file systems and/or file partitions).

2.5.4 Improved Diagnostics

The 3B21D computer diagnostic system follows a systematic approach for isolating hardware failures and provides a suspect pack list to the user. For each circuit pack or unit, the diagnostic software does the following:

(1) Runs the self-test of the Boundary Scan Master (BSM) chip if the chip is used on the circuit pack.

(2) Runs the boundary-scan integrity test followed by the boundary-scan interconnect test.

(3) Instructs all the ASICs on the unit under test to run their internal device level Built-In Self Test (BIST) and analyze their results.

(4) Runs functional tests on non-BIST units.

System diagnostics are organized on a unit basis. Unit diagnostics are structured in subunit test phases. Test phases are executed to first test the most elementary operations, and then proceed to the more detailed subunit operations.

All diagnostic programs avoid interference with the normal system functions. Special driver functions handle error conditions generated by the diagnostic tests, thus avoiding the normal error handling routines.

The diagnostic system also provides maintenance personnel with interactive diagnostic commands. These can be used to do the following:

- Run a single or range of diagnostic phases.
- Repeat a single or range of diagnostic phases.
- Run a diagnostic up to a specified point in the data table and then stop.
- Repeatedly perform a specified group of tests within a phase.
- Provide optional parameters to main store diagnostics.
- Step through diagnostic data table commands.

See 235-600-700, *Input Message Manual*, and 235-105-220, *Corrective Maintenance Procedures*.

2.5.4.1 Boundary Scan Architecture

The 3B21D computer hardware uses Built-In Self Test (BIST) and Boundary Scan (BS) features at the circuit pack and ASIC device levels to reduce the testing difficulties and increase fault coverage. Additional circuits have been incorporated in the 3B21D computer hardware design to provide BS cells adjacent to each chip's input/output pins to control and observe the signals. BS cells are like test points that are interconnected as shift register chains. A separate BS bus is used to assess and control the BS cells.

Boundary scan cells can be operated in either a normal or test mode. In the test mode, the BS cells can accept test instructions and data, and scan out the test responses. They are used to perform interconnection tests or internal tests (BIST).

Software diagnosis is performed on the off-line processor complex through the maintenance channel. The maintenance channel connects the active and the standby processors. The diagnosis is initiated from the active processor. Diagnostic commands issued by the active processor are passed via the maintenance channel link. These commands are then received, interpreted, and reissued to the Boundary Scan Master (BSM) device through the Generic Processor Interface (GPI) by the Maintenance Channel (MCH).

2.5.4.2 Built-In Diagnostics

The inclusion of on-chip circuitry to provide test vectors or to analyze output responses is called Built-In Self Test (BIST). The BIST reduces the complexity and cost of an external tester by including some or all tester functions in the chip itself.

The use of BIST and Boundary Scan (BS) provides a higher percentage of fault coverage. The BIST and BS hardware is accessed via diagnostic software that executes the ASIC BIST test and the circuit pack BS test.

2.5.5 Auto Restart

The 3B21D computer system hardware is designed to automatically restart following a power interruption. To support this feature, the 3B21D computer unit power switches must be in the ON position. The unit power switch ON position allows auto-restart when power is applied to the unit. This feature provides for unattended system operation. The Auto Restart feature is available in RTR Release 21.5 and later.

2.5.6 Fault Isolation and Repair

The 3B21D computer design enables fault isolation to a circuit pack level. This is accomplished by the following:

- ASIC technology, which places complete functions on one circuit pack, making it easier to isolate a fault though functional testing.
- Built-In Self Test (BIST), which allows a more thorough test at the ASIC and circuit pack level.

2.5.7 Hot Card Replacement

CAUTION: All circuit packs must be removed and installed with the power OFF. The "hot card" replacement of circuit packs is not supported.

Before a 3B21D circuit pack is removed or installed in an apparatus housing, the power to the circuit pack must be removed. However, the SCSI *peripherals* can be installed without powering down the associated SCSI bus. The DFC, PSSDB, and SCSI peripheral circuit packs have their own board-mounted power converters and power switches. This is equivalent to a "hot card" replacement, because the other units on the SCSI bus are not affected.

NOTE: The SCSI bus must be removed when installing a disk.

See 235-105-110, *System Maintenance Requirements and Tools*, for more information about spare pack handling, circuit pack removal, and installation.

3. 3B21D COMPUTER CONFIGURATIONS

3.1 CONFIGURATION OVERVIEW

The 3B21D computer system, J3T061A-1, offers cost-effective configurations for small switching offices (1K to 6K lines) and can be grown from a small office configuration to a large office configuration with minimum system interruption. The minimum 3B21D computer system configuration is packaged in one cabinet called the Processor Cabinet, J3T060A-1. The maximum 3B21D computer system configuration is packaged in three cabinets, one Processor Cabinet and up to two Peripheral Growth Cabinets (PGC 0 and PGC 1), J3T059A-1.

A Maintenance Teletypewriter/Terminal (MTTY) and Receive-Only Printer (ROP) are also part of any 3B21D computer configuration.

Figure 3-1 shows the maximum system equipage supported by J3T061A-1. (J3T061A-1 is the 3B21D computer system Super J-Drawing.) The Peripheral Growth Cabinets are always located to the right of the Processor Cabinet, as viewed from the front of the cabinets. The cabinets each measure about 72 inches (183 cm) high by 30 inches (76 cm) wide by 24 inches (60 cm) deep.

Figure 3-1 3B21D Computer System Cabinets Front View

3.2 CONFIGURATION EXAMPLES, RELEASE 1

The customer can order any of the configurations supported by the Super J-Drawing, J3T061A-1. Some configuration examples are provided in the following paragraphs.

3.2.1 Processor Cabinet, J3T060A-1 □ Basic System

The initial (basic) system configuration consists of the Processor Cabinet equipped with the following major units:

- One Modular Filter and Fuse Panel Unit, J5D003FJ-1
- One Bidirectional Cooling Unit, J5D003FH-2
- Two Processor Units, J3T060AA-1.

See Figure 3-2 for equipage information. The basic system configuration provides the following equipment:

- Control Unit (CU) 0 and CU 1.
- Direct Memory Access (DMA) 0 is part of the basic system. DMA 1 is optional.
- Disk File Controller (DFC) 0 and DFC 1 supporting seven Small Computer System Interface (SCSI) peripheral units (SPUs). An SPU slot can be equipped with a UN375 Moving Head Disk (MHD) circuit pack or a UN376 Digital Audio Tape (DAT) circuit pack. DFC 0 supports four SPUs; DFC 1 supports three SPUs. There are five dedicated SPU slots in the basic units (Processor Units 0 and 1). Optionally, two additional SPUs (SPU04 and SPU05) can be grown instead of equipping Input/Output Processor (IOP) Peripheral Controller (PC) community 3 (PC31 and 32). The PC30 slot in each Processor Unit is always available for use as a PC. One DAT drive (SPU54) is controlled by DFC 0. See Table 3-1 for SPU controller and bus assignments.

  NOTE: DFC 0 and DFC 1 could be equipped with either a UN580 or with both a TN2116 and a UN373.

- IOP 0 with Peripheral Communities 0, 1, 2, and 3.
- IOP 1 with Peripheral Communities 0, 1, 2, and 3.

3.2.2 Processor Cabinet, J3T060A-1 □ Configuration Example 1

Configuration Example 1 for the Processor Cabinet contains the following major units:

- One Modular Filter and Fuse Panel Unit, J5D003FJ-1
- One Bidirectional Cooling Unit, J5D003FH-2
- Two Processor Units, J3T060AA-1
- One Growth Unit, J3T060AB-1.

See Figure 3-3 for equipage information. Note that the first Growth Unit can be equipped at either vertical position 57 (Figure 3-1) or vertical position 06 in the Processor Cabinet. Example 1 installs the Growth Unit at position 57 and provides the following equipment:

- CU 0 and CU 1.

- DMA 0 is part of the basic system. DMA 1 is optional.
- DFC 0 and DFC 1 supporting 12 SPUs. An SPU slot can be equipped with a UN375 MHD circuit pack or a UN376 DAT circuit pack. DFC 0 supports 6 SPUs; DFC 1 supports 6 SPUs. There are 5 dedicated SPU slots in the basic units (Processor Units 0 and 1). Optionally, 2 additional SPUs (SPU04 and SPU05) can be grown instead of equipping IOP PC community 3 (PC31 and 32). The PC30 slot in each Processor Unit is always for available use as a PC. One DAT drive (SPU54) is controlled by DFC 0.

  Five SPUs can be equipped in the Growth Unit. Three of the Growth Unit SPUs are connected to DFC 1, SBUS 1; two of the Growth Unit SPUs are connected to DFC 0, SBUS 0. See Table 3-1 for SPU controller and bus assignments.

  NOTE: DFC 0 and DFC 1 could be equipped with either a UN580 or with both a TN2116 and a UN373.
- IOP 0 with Peripheral Communities 0, 1, 2, and 3.
- IOP 1 with Peripheral Communities 0, 1, 2, and 3.
- Either IOP 2 or IOP 3 with Peripheral Communities 0 and 1, depending on where the Growth Unit is equipped in the Processor Cabinet. The growth unit can be optionally equipped to provide a Peripheral Community 2, a Peripheral Community 3, or SPUs in this configuration as shown in Figure 3-3 .

3.2.3 Processor Cabinet, J3T060A-1 Configuration Example 2

Configuration Example 2 for the Processor Cabinet contains the following major units:

- One Modular Filter and Fuse Panel Unit, J5D003FJ-1
- One Bidirectional Cooling Unit, J5D003FH-2
- Two Processor Units, J3T060AA-1
- Two Growth Units, J3T060AB-1.

See Figure 3-4 for equipage information. The growth units can be optionally equipped to provide Peripheral Community 2, Peripheral Community 3, or SPUs in this configuration as shown in Figure 3-4 . Configuration Example 2 provides the following equipment:

- CU 0 and CU 1.
- DMA 0 is part of the basic system. DMA 1 is optional.
- DFC 0 and DFC 1 supporting 17 SPUs. An SPU slot can be equipped with a UN375 MHD circuit pack or a UN376 DAT circuit pack. DFC 0 supports nine SPUs; DFC 1 supports eight SPUs. There are five dedicated SPU slots in the basic units (Processor Units 0 and 1). Optionally, two additional SPUs (SPU04 and SPU05) can be grown instead of equipping IOP PC community 3 (PC31 and 32). The PC30 slot in each Processor Unit is always available for use as a PC. One DAT drive (SPU54) is controlled by DFC 0.

  Five SPUs can be equipped in each Growth Unit. Five of the Growth Unit SPUs are connected to DFC 1; five of the Growth Unit SPUs are connected to DFC 0. See Table 3-1 for SPU controller and bus assignments.

  NOTE: DFC 0 and DFC 1 could be equipped with either a UN580 or with both a TN2116 and a

UN373.

- IOP 0 with Peripheral Communities 0, 1, 2, and 3.
- IOP 1 with Peripheral Communities 0, 1, 2, and 3.
- IOP 2 with Peripheral Communities 0 and 1.
- IOP 3 with Peripheral Communities 0 and 1.

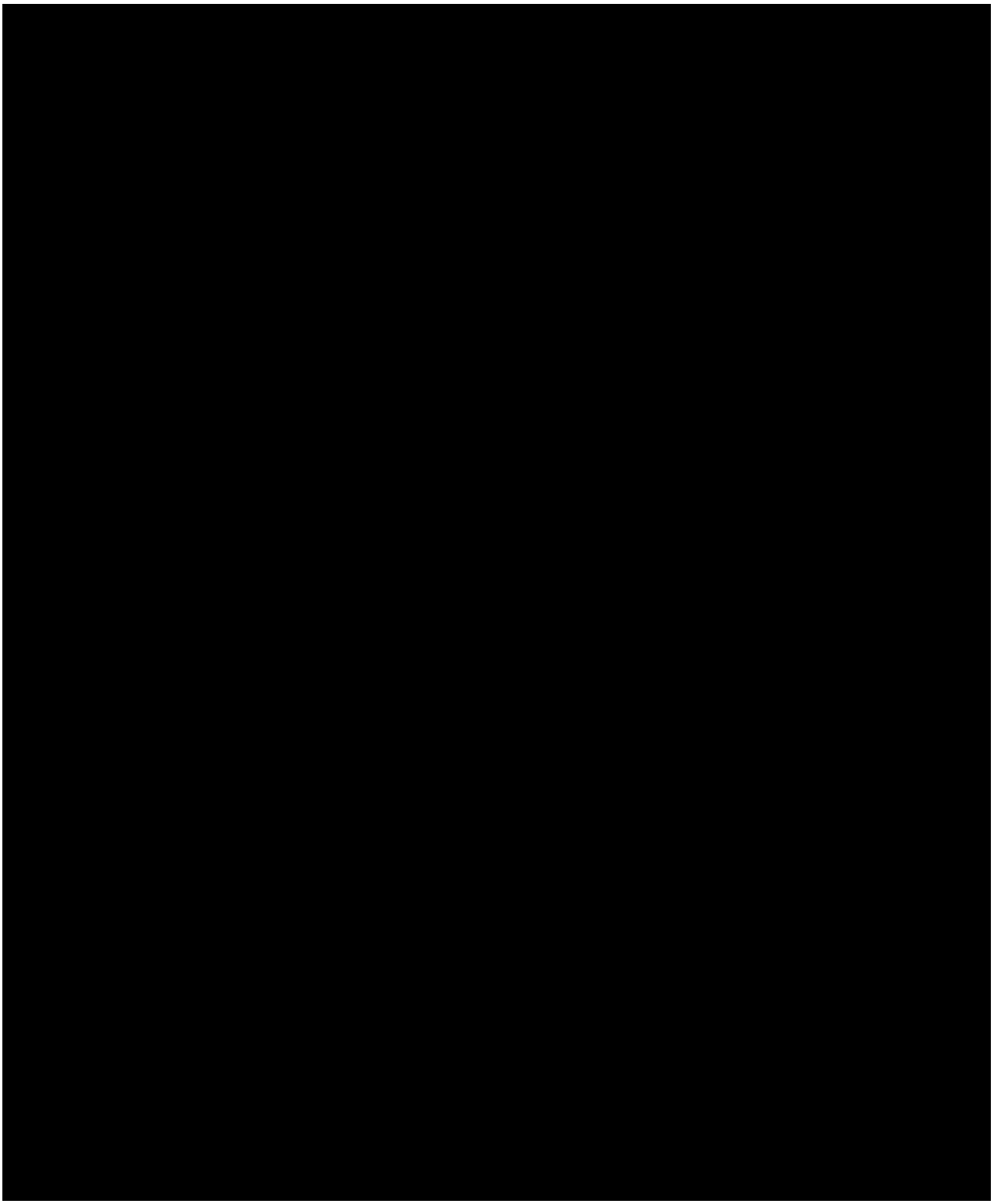


Figure 3-2 Processor Cabinet, J3T060A-1 Basic System Configuration, Front View

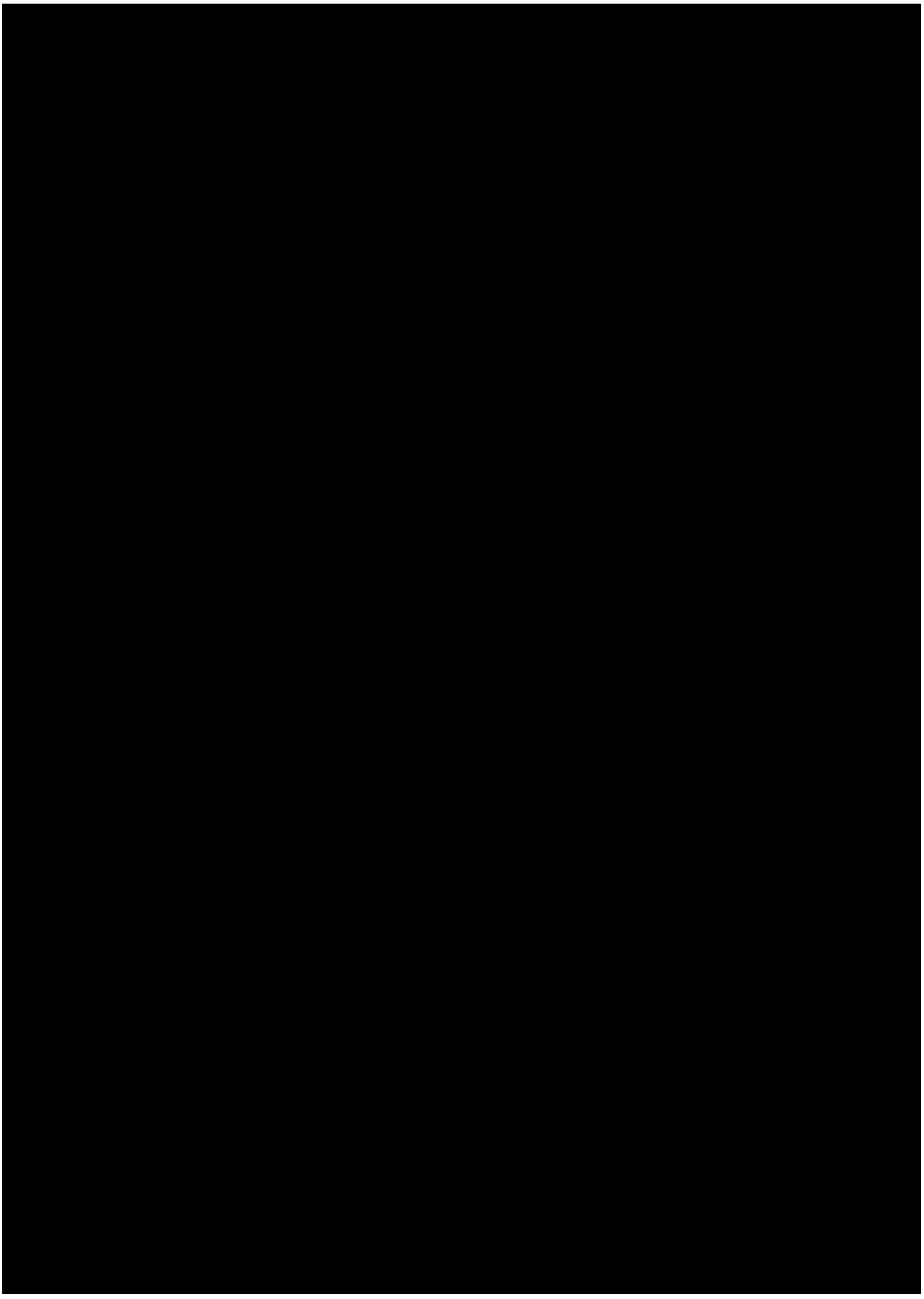


Figure 3-3 Processor Cabinet, J3T060A-1 Configuration Example 1, Front View

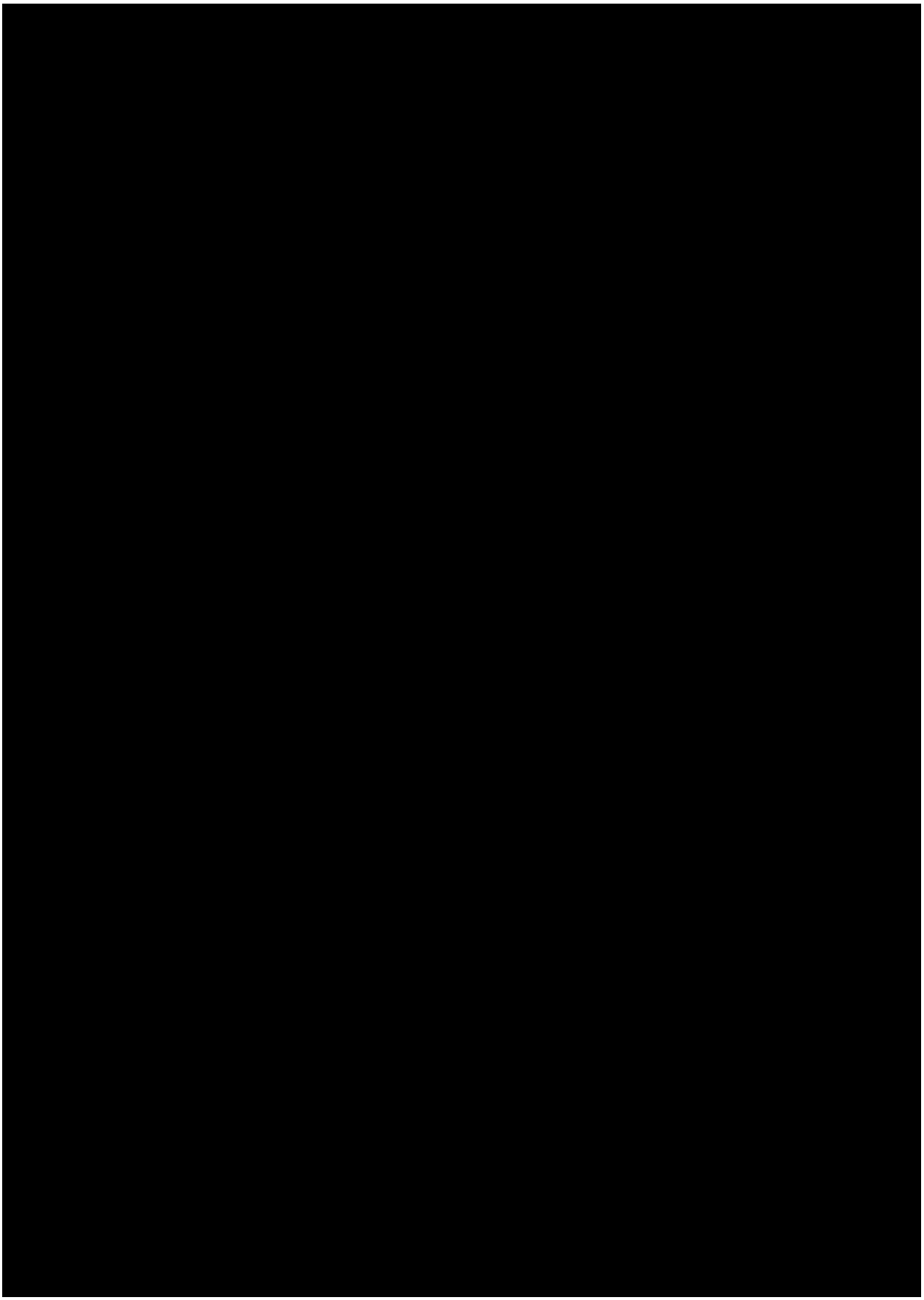


Figure 3-4 Processor Cabinet, J3T060A-1 Configuration Example 2, Front View

3.2.4 Peripheral Growth Cabinet, J3T059A-1 □ Configuration Example 1

Configuration Example 1 for the Peripheral Growth Cabinet provides the first Peripheral Growth Cabinet equipped with one SCSI 9-track tape drive, KS-23909. This is the first 9-track tape drive (SPU57) in the 3B21D computer system.

A single SCSI bus cable connects a 9-track tape drive to any available SCSI bus (SBUS 0, 1, 2, or 3).

The 9-track tape drives are AC powered and plug directly into an AC power outlet. The drives can be configured to use either 50- or 60-Hertz power.

See Figure 3-5 for equipage information.

3.2.5 Peripheral Growth Cabinet, J3T059A-1 □ Configuration Example 2

Configuration Example 2 for the Peripheral Growth Cabinet provides the second SCSI 9-track tape drive, KS-23909 (SPU56) in the first Peripheral Growth Cabinet.

See Figure 3-6 for equipage information.

3.2.6 Peripheral Growth Cabinet, J3T059A-1 □ Configuration Example 3

Configuration Example 3 for the Peripheral Growth Cabinet provides the second Peripheral Growth Cabinet equipped with one SCSI 9-track tape drive, KS-23909. This is the third 9-track tape drive (SPU59) in the 3B21D computer system.

See Figure 3-7 for equipage information.

3.2.7 Peripheral Growth Cabinet, J3T059A-1 □ Configuration Example 4

Configuration Example 4 for the Peripheral Growth Cabinet provides the fourth SCSI 9-track tape drive, KS-23909 (SPU58) in the second Peripheral Growth Cabinet.

See Figure 3-8 for equipage information.

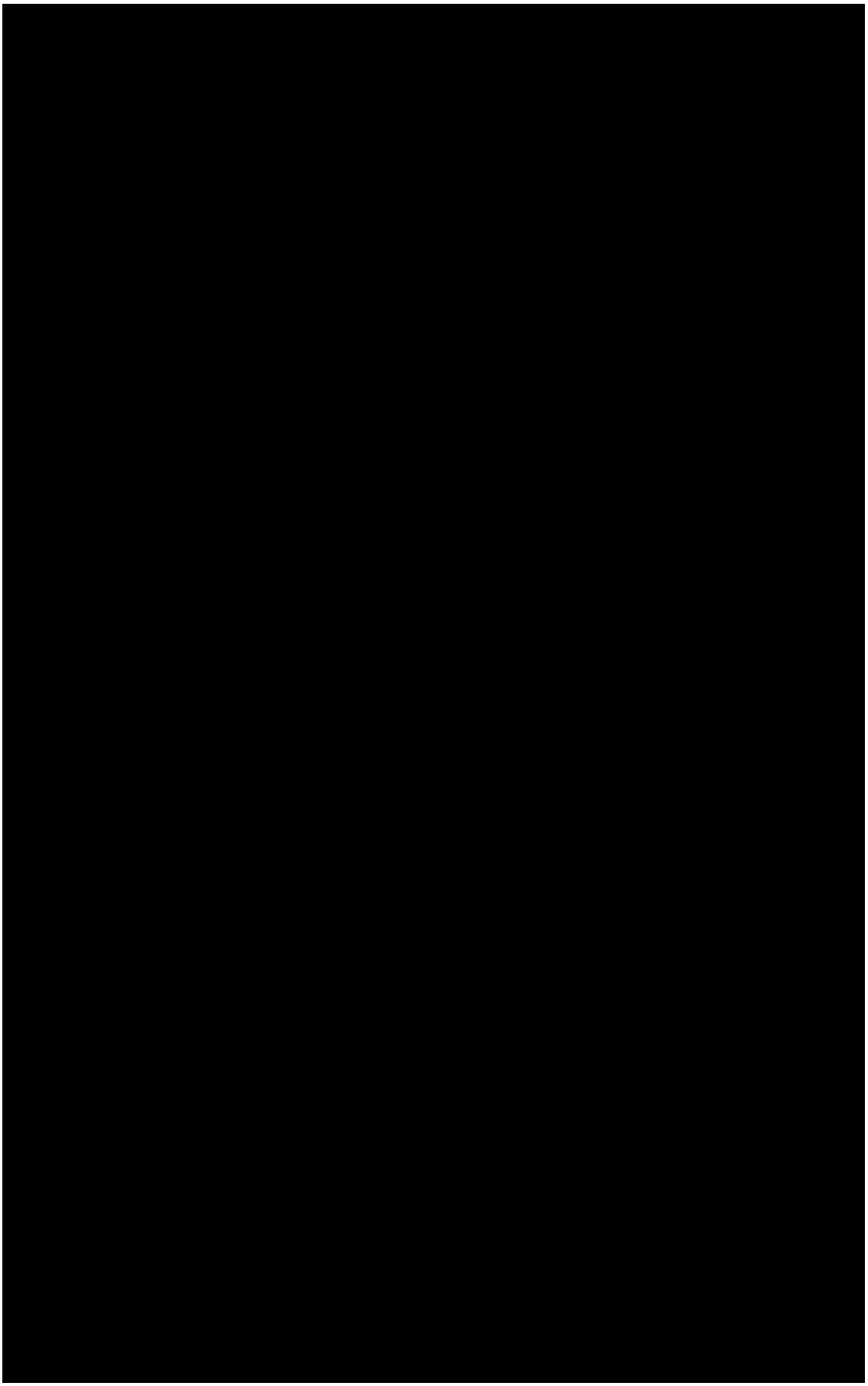


Figure 3-5 Peripheral Growth Cabinet, J3T059A-1 Configuration Example 1, Front View

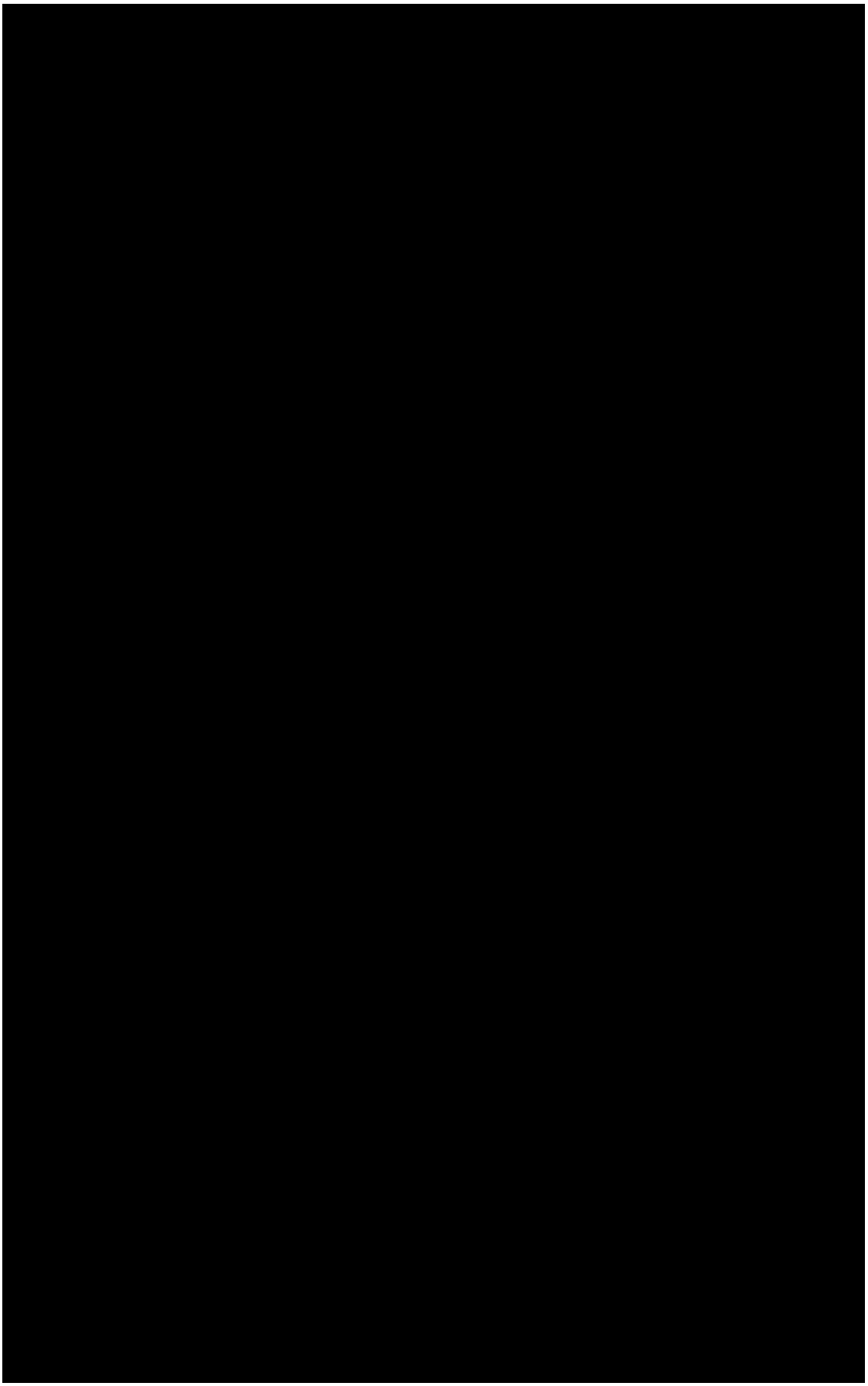


Figure 3-6 Peripheral Growth Cabinet, J3T059A-1 Configuration Example 2, Front View

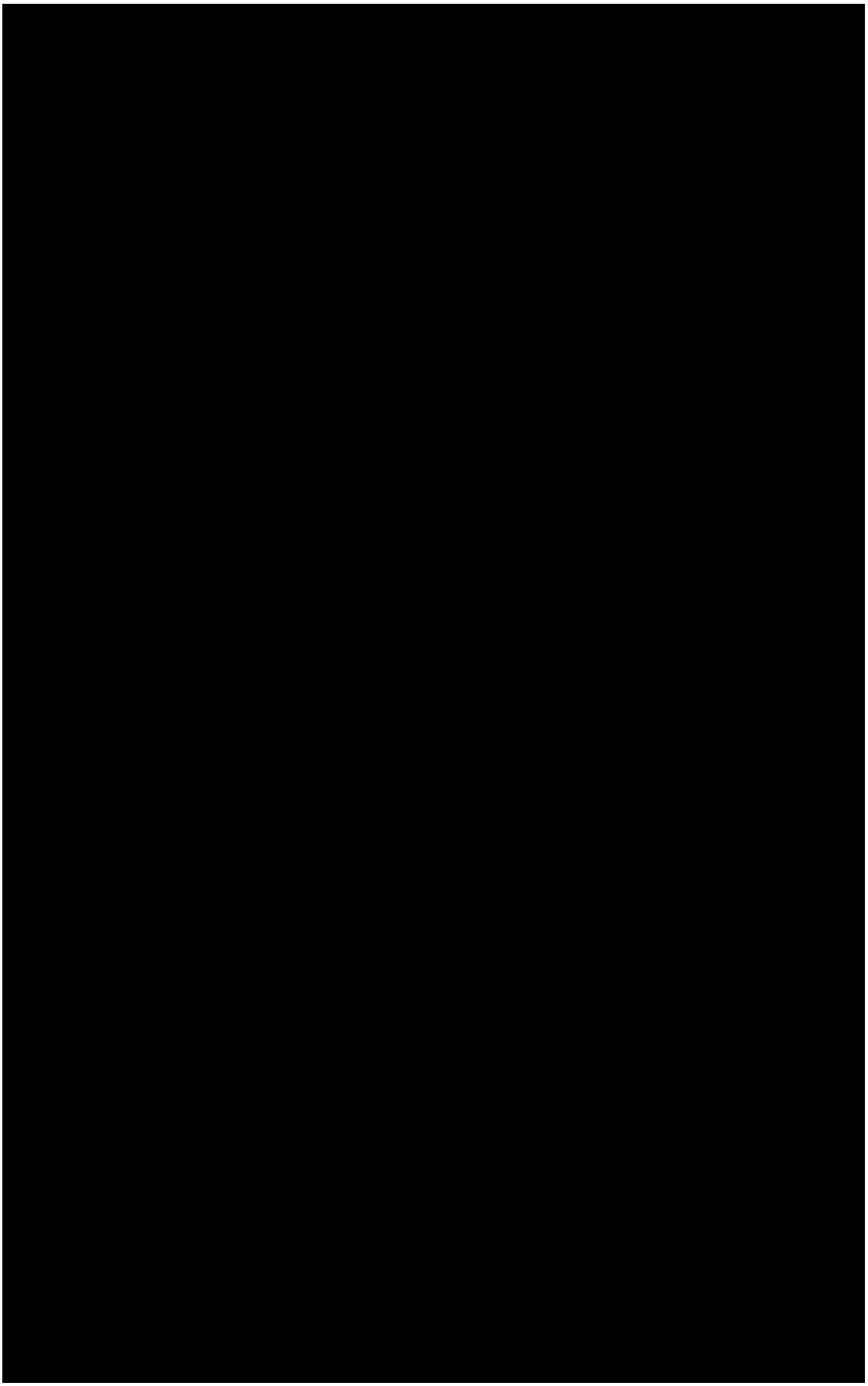


Figure 3-7 Peripheral Growth Cabinet, J3T059A-1 Configuration Example 3, Front View

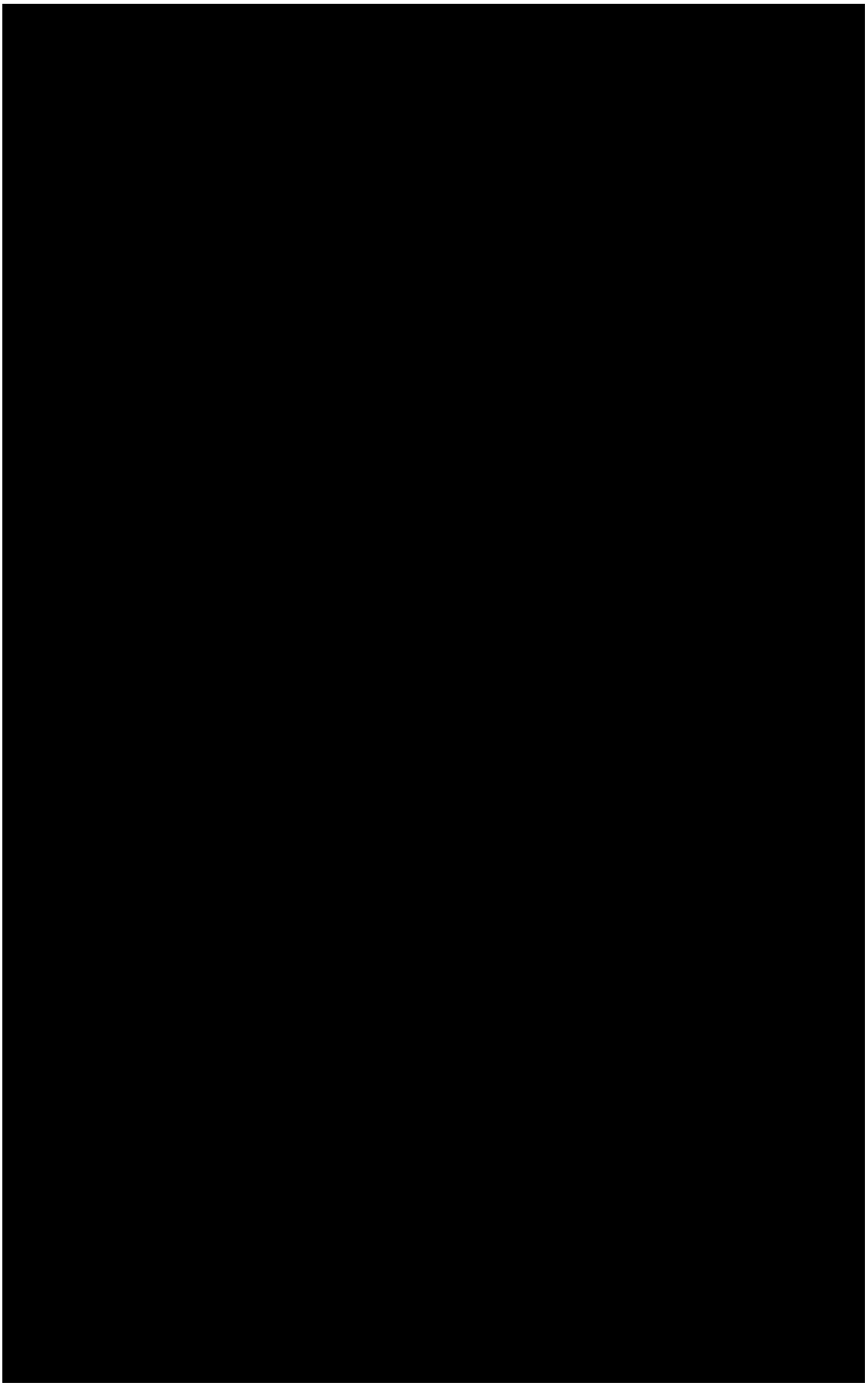


Figure 3-8 Peripheral Growth Cabinet, J3T059A-1 Configuration Example 4, Front View

3.3 SCSI PERIPHERAL UNIT CONTROLLER AND BUS ASSIGNMENTS

Table 3-1 identifies the DFC and SCSI bus assignments for the various SPUs as they apply to the previously described configuration examples for Release 1.

The naming convention for the two SCSI buses provided by a DFC designates the buses "BUS A" and "BUS B." The 3B21D computer system designations for the SCSI buses are different, as follows:

- The SCSI BUS A and BUS B provided by DFC 0 are designated "SBUS 0" and "SBUS 2," respectively.
- The SCSI BUS A and BUS B provided by DFC 1 are designated "SBUS 1" and "SBUS 3," respectively.

A DFC could include a UN373 (DFCA) and TN2116 (DFCB), powered by a 410AA (DC-to-DC converter). The equipment locations (EQLs) for DFC 0 and DFC 1 are as follows:

- DFC 0 is in the Processor Cabinet, Processor Unit 0, at 28-170 (TN2116), 28-178 (UN373), and 28-188 (CONVE).
- DFC 1 is in the Processor Cabinet, Processor Unit 1, at 53-170 (TN2116), 53-178 (UN373), and 53-188 (CONVE).

Or, a DFC could include a UN580 (DFCA/DFCB), powered by a 410AA (DC-to-DC converter). When using a UN580 circuit pack, EQLs for DFC 0 and DFC 1 are as follows:

- DFC 0 is in the Processor Cabinet, Processor Unit 0, at EQL 28-178 (UN580) and 28-188 (CONVE).
- DFC 1 is in the Processor Cabinet, Processor Unit 1, at EQL 53-178 (UN580) and 53-188 (CONVE).

Or, a DFC could include a UN580B (DFCA/DFCB), which is powered by an onboard DC-to-DC converter. When using a UN580B circuit pack, EQLs for DFC 0 and DFC 1 are as follows:

- DFC 0 is in the Processor Cabinet, Processor Unit 0, at EQL 28-178.
- DFC 1 is in the Processor Cabinet, Processor Unit 1, at EQL 53-178.

Table 3-1 SCSI Peripheral Unit Controller and Bus Assignments

SCSI PERIPHERAL UNIT [a]			PROCESSOR CABINET CONFIGURATION			ADDITIONAL GROWTH (WITH REDUCED IOP CAPABILITY)
DESCRIPTION	EQUIPMENT LOCATION		BASIC	EXAMPLE 1 - GROWTH UNIT AT EQL 57	EXAMPLE 2 - GROWTH UNITS AT EQLS 57 & 06	
	PROCESSOR CABINET	PERIPHERAL GROWTH CABINET	DFC/SCSI BUS	DFC/SCSI BUS	DFC/SCSI BUS	DFC/SCSI BUS
SPU00	28-162		DFC 0/SBUS 0	DFC 0/SBUS 0	DFC 0/SBUS 0	
SPU01	53-162		DFC 1/SBUS 1	DFC 1/SBUS 1	DFC 1/SBUS 1	
SPU02	19-170		DFC 0/SBUS 2	DFC 0/SBUS 2	DFC 0/SBUS 2	
SPU03	45-170		DFC 1/SBUS 3	DFC 1/SBUS 3	DFC 1/SBUS 3	
SPU04	28-146		DFC 0/SBUS 0	DFC 0/SBUS 0	DFC 0/SBUS 0	
SPU05	53-146		DFC 1/SBUS 1	DFC 1/SBUS 1	DFC 1/SBUS 1	
SPU06	19-154					DFC 0/SBUS 2
SPU07	45-154					DFC 1/SBUS 3
SPU08	28-118					DFC 0/SBUS 0
SPU09	53-118					DFC 1/SBUS 1

SPU10	19-138					DFC 0/SBUS 2
SPU11	45-138					DFC 1/SBUS 3
SPU12	28-102					DFC 0/SBUS 0
SPU13	53-102					DFC 1/SBUS 1
SPU14	19-118					DFC 0/SBUS 2
SPU15	45-118					DFC 1/SBUS 3
SPU16	19-102					DFC 0/SBUS 2
SPU17	45-102					DFC 1/SBUS 3
SPU18	11-180				DFC 0/SBUS 2	
SPU19	62-180			DFC 1/SBUS 1	DFC 1/SBUS 3	
SPU20	11-164				DFC 0/SBUS 0	
SPU21	62-164			DFC 0/SBUS 0	DFC 1/SBUS 1	
SPU22	11-148				DFC 0/SBUS 2	
SPU23	62-148			DFC 1/SBUS 1	DFC 1/SBUS 3	
SPU24	11-132				DFC 0/SBUS 0	
SPU25	62-132			DFC 0/SBUS 0	DFC 1/SBUS 1	
SPU26	11-116				DFC 0/SBUS 2	
SPU27	62-116			DFC 1/SBUS 1	DFC 1/SBUS 3	
SPU28	11-096					DFC 0/SBUS 0
SPU29	62-096					DFC 1/SBUS 1
SPU30	11-080					DFC 0/SBUS 2
SPU31	62-080					DFC 1/SBUS 3
SPU32	11-064					DFC 0/SBUS 0
SPU33	62-064					DFC 1/SBUS 1
SPU34	11-048					DFC 0/SBUS 2
SPU35	62-048					DFC 1/SBUS 3
SPU54 (MT)	19-186		DFC 0/SBUS 0	DFC 0/SBUS 0	DFC 0/SBUS 0	
SPU56 (9-TRACK1)		10-XXX	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	
SPU57 (9-TRACK0)		42-XXX	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	
SPU58 (9-TRACK3)		10-XXX	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	
SPU59 (9-TRACK2)		42-XXX	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	

Notes:

a. An SPU can be any SCSI device such as 9-track tape, DAT, MHD drive, or magnetic tape (MT) unit.

4. 3B21D COMPUTER PHYSICAL DESCRIPTION

4.1 CABINETS

The 3B21D computer system is packaged in one, two, or three cabinets. The Processor Cabinet, J3T060A-1, is always required. One or two Peripheral Growth Cabinets, J3T059A-1, are provided as necessary when 9-track Small Computer System Interface (SCSI) tape drives are required as part of the configuration. The Peripheral Growth Cabinets are always located to the right of the Processor Cabinet, as viewed from the front of the cabinets.

Each cabinet measures about 72 inches (183 cm) high by 30 inches (76 cm) wide by 24 inches (60 cm) deep.

Figure 4-1 shows the unit equipage of the Processor Cabinet and the two Peripheral Growth Cabinets. Figure 4-2 provides a general equipment configuration overview of the Processor Cabinet. The front doors of the cabinets are not shown in these figures.

Figure 4-1 3B21D Computer System Cabinets Front View

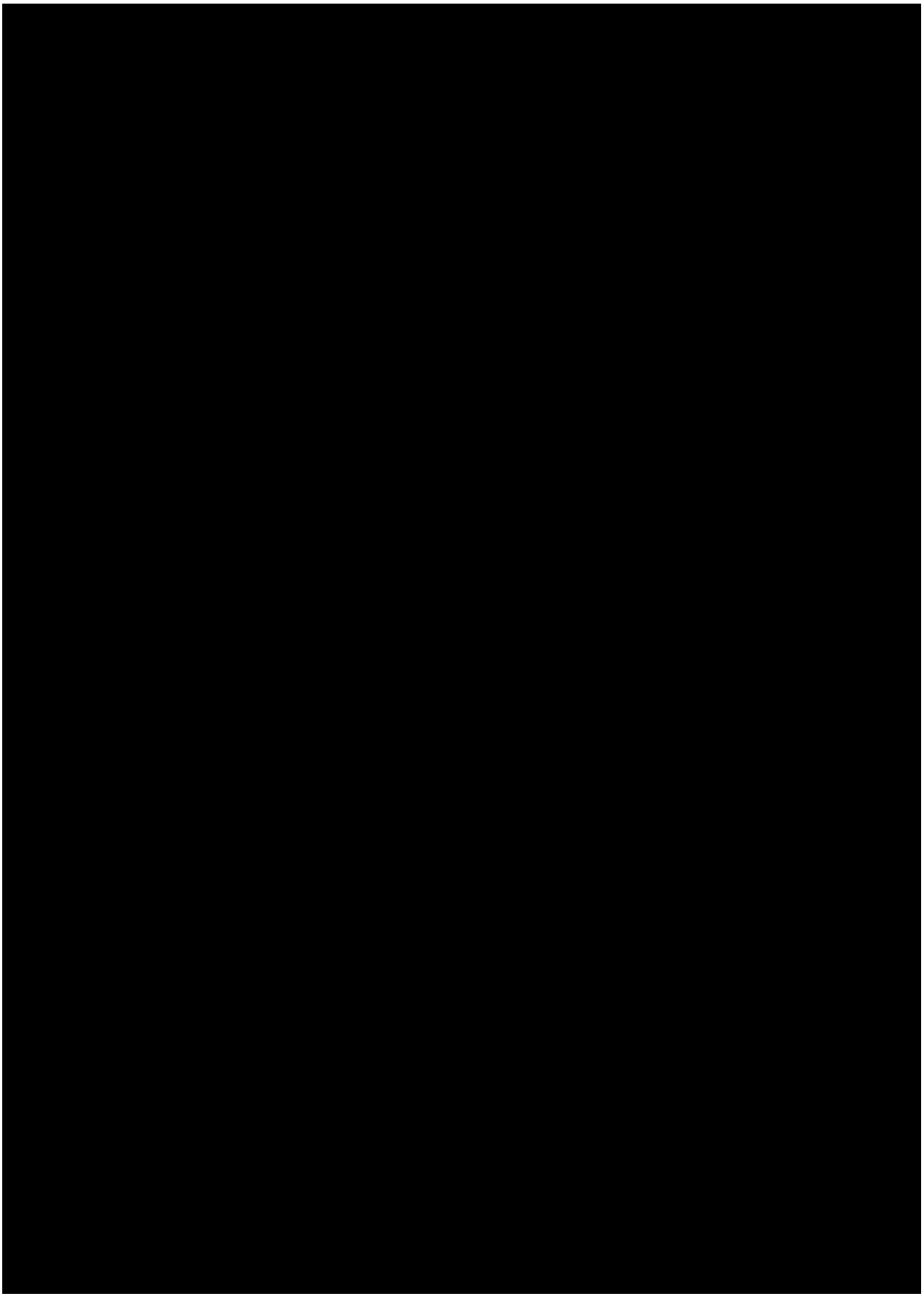


Figure 4-2 Processor Cabinet Equipment Overview Front View

4.2 PROCESSOR CABINET ARRANGEMENT

4.2.1 Processor Unit, J3T060AA-1

The Processor Unit, J3T060AA-1, supports the Central Control (CC), Direct Memory Access (DMA), Main Memory (MM), Disk File Controller (DFC), SCSI peripheral units (SPUs), DC-to-DC power conversion, power control, port switch with RS-232 interface, and IOP/PC functions. The SPUs include the UN375/UN375E circuit pack, UN376/UN376E circuit pack, and 9-track tape. The MM can be a KLW32, KLW40, KLW48, KLW64, or KLW128 circuit pack. The Processor Unit also provides two KLW-size slots (EX 0 and EX 1) for future expansion capability. Figure 4-3 shows apparatus housing layout details for the Processor Units 0 and 1. Table 4-1 identifies the equipage of the Processor Unit 0 and Processor Unit 1 in the Processor Cabinet.

Figure 4-3 Processor Unit, J3T060AA-1 Equipment Layout, Front View

Table 4-1 Processor Units 0 and 1 Circuit Packs

CIRCUIT PACK	PANEL DESIGNATION	PROCESSOR UNIT 0 EQL	PROCESSOR UNIT 1 EQL

410AA Power Converter	PWRA (RED) 410AA	28-052	53-052
410AA Power Converter	410AA PWRB (BLUE)	19-060	45-060
410AA Power Converter	410AA PWRC (BLACK)	19-088	45-088
410AA Power Converter	PWRD (GREEN) 410AA	28-088	53-088
410AA Power Converter	PWRE (PURPLE) 410AA	28-188	53-188
KBN10 Input/Output Processor	KBN10 IOP (BLACK)	19-065	45-065
KBN15 Direct Memory Access	DMA0 (RED) KBN15	28-075	53-075
KBN15 Direct Memory Access	DMA1 (BLUE) KBN15	28-065	53-065
KLW31 Central Control	CC (RED) KLW31	24-038	49-038
Main Memory (KLW32, KLW40, or KLW48)	MM (RED) KLW32	24-008	49-008
KLW__ Expansion Slot	EX0 (BLUE)	28-018	53-018
KLW__ Expansion Slot	EX1 (BLUE)	24-028	49-028
TN1820 I/O Processor Power Switch	TN1820 IOPPS (GREEN and BLACK)	19-080	45-080
TN1821 CU Power Switch	CUPS (RED) TN1821	28-060	53-060
TN2116 SCSI Host Adapter	DFC0 (PURPLE)	28-170	
TN2116 SCSI Host Adapter	DFC1 (PURPLE)		53-170
TN983/ UN583/ UN597 MTTY Controller	PC00 (BLACK)	19-094	45-094
	PC01 (BLACK)	19-102	45-102
	PC02 (BLACK)	19-110	45-110
	PC03 (BLACK)	19-118	45-118
UN33D/UN933 Scanner and Signal Distributor Controller	PC10 (BLACK)	19-130	45-130
	PC11 (BLACK)	19-138	45-138
	PC12 (BLACK)	19-146	45-146
	PC13 (BLACK)	19-154	45-154
	PC20 (GREEN)	28-094	53-094
	PC21 (GREEN)	28-102	53-102
	PC22 (GREEN)	28-110	53-110
	PC23 (GREEN)	28-118	53-118
	PC30 (GREEN)	28-130	53-130
	PC31 (GREEN)	28-138	53-138
	PC32 (GREEN)	28-146	53-146
UN373 or UN580 DDSBS/DSCH Interface	DFC0 (PURPLE) UN373 or UN580	28-178	
UN373 or UN580 DDSBS/DSCH Interface	DFC1 (PURPLE) UN373 or UN580		53-178
UN375 SCSI Disk	SPU 00 UN375	28-162	
UN375 SCSI Disk	SPU 01 UN375		53-162
UN375 SCSI Disk	SPU 02	19-170	
UN375 SCSI Disk	SPU 03		45-170
UN376 SCSI Tape (MT)	UN376 SPU 54	19-186	
UN377 PSSDB	PSSD (BLACK)		45-186
UN379 Utility Circuit	UC (RED)	19-050	45-050

4.2.2 Growth Unit, J3T060AB-1

The Growth Unit, J3T060AB-1, supports the equipage of additional SCSI peripheral units (SPUs) and IOP/PC circuit packs to provide a system growth capability. Two Growth Units can be equipped in the Processor Cabinet. Figure 4-4 shows apparatus housing layout details for the Growth Units. Table 4-2 identifies the equipage of the IOP 2-SPU and IOP 3-SPU Growth Units in the Processor Cabinet.

Figure 4-4 Growth Unit, J3T060AB-1, Equipment Layout Front View

Table 4-2 Growth Unit Circuit Packs

CIRCUIT PACK	PANEL DESIGNATION	PROCESSOR CABINET	
		IOP 2-SPU GROWTH UNIT EQL	IOP 3-SPU GROWTH UNIT EQL
410AA Power Converter	PWRF (RED) 410AA	11-006	62-006
410AA Power Converter	PWRG (BLACK) 410AA	11-034	62-034
KBN10 Input/Output Processor	IOP (RED) KBN10	11-011	
KBN10 Input/Output Processor	IOP (RED) KBN10		62-011
TN1820 Input/Output Processor Power Switch	IOPPS (RED and BLACK) TN1820	11-026	62-026
Equipage is application dependent and includes peripheral controllers.	PC00 (RED) PC01 (RED)		62-040 62-048
	PC00 (RED) PC01 (RED)	11-040 11-048	
	PC02 (RED) PC03 (RED)		62-056 62-064
	PC02 (RED) PC03 (RED)	11-056 11-064	
Equipage is application dependent and includes peripheral controllers.	PC10 (RED) PC11 (RED)		62-072 62-080
	PC10 (RED) PC11 (RED)	11-072 11-080	
	PC12 (RED) PC13 (RED)		62-088 62-096
	PC12 (RED) PC13 (RED)	11-088 11-096	
IOP Community 2 or SPUs 24 through 27. Equipage is application dependent and includes peripheral controllers	PC20 (BLACK) PC21 (BLACK)		62-108 62-116
	SPU 27		62-116
	PC20 (BLACK) PC21 (BLACK)	11-108 11-116	

and/or SCSI peripheral units.	SPU 26	11-116	
	PC22 (BLACK) PC23 (BLACK)		62-124 62-132
	SPU 25		62-132
	PC22 (BLACK) PC23 (BLACK)	11-124 11-132	
	SPU 24	11-132	
Equipage is application dependent and includes peripheral controllers and/or SCSI peripheral units.	PC30 (BLACK) PC31 (BLACK)		62-140 62-148
	SPU 23		62-148
	PC30 (BLACK) PC31 (RED)	11-140 11-148	
	SPU 22	11-148	
	PC32 (RED) PC33 (RED)		62-156 62-164
	SPU21		62-164
	PC32 (RED) PC33 (RED)	11-156 11-164	
	SPU 20	11-164	
Equipage is application dependent and includes SCSI peripheral units.	SPU 18	11-180	
	SPU 19		62-180

4.2.3 Modular Fuse and Filter Unit, J5D003FJ-1

Figure 4-5 shows the fuse assignments for the Processor Cabinet.

Figure 4-5 Processor Cabinet Fuse Assignments

4.3 PERIPHERAL GROWTH CABINET ARRANGEMENT

The Peripheral Growth Cabinet, J3T059A-1, is used to provide mounting space for two 9-track SCSI tape units. The first Peripheral Growth Cabinet (PGC 0) contains the first (SPU57) and second (SPU56) 9-track tape units at EQLs 42 and 10, respectively. The second Peripheral Growth Cabinet (PGC 1) contains the third (SPU59) and fourth (SPU58) 9-track tape units at EQLs 42 and 10, respectively.

The 9-track SCSI tape unit is a KS-23909. KS-23909 is either a 120 V AC, 60 Hz, 1600/6250 BPI, 125 IPS tape unit or 240 V AC, 50 Hz, 1600/6250 BPI, 125 IPS unit.

4.4 STANDARD PRINTED WIRING BOARDS (PWBs)

The Printed Wiring Board (PWB) general characteristics are summarized in Table 4-3 for the UN, TN, KLW, and KBN circuit pack types. All PWBs are manufactured per *Fastech*® electronic packaging system standards. See the *Fastech* electronic packaging system documentation for additional standards information.

Table 4-3 Typical PWB Parameters

CHARACTERISTIC	CIRCUIT PACK TYPE			

	UN	TN	KLW	KBN
SIZE (inches)	7.67 x 13.860	7.67 x 13.860	16.170 x 13.860	7.67 x 13.860
LAYERS (typical)	6-10	6-10	6-10	6-10
THICKNESS (mils)	62.0□7	62.0□7	62.0□7	0.062□7
PLATED THRU- HOLE SIZE (mils)	38.0□3	38.0□3	38.0□3	38.0□3
LAND SIZE (mils)	58.0□2	58.0□3	58.0□3	58.0□2
ROUTING	2-track cover/internal: 8-mil lines 9-mil spaces	2-track cover/internal: 8-mil lines 9-mil spaces	2-track cover/internal: 8-mil lines 9-mil spaces	2-track cover/internal: 8-mil lines 9-mil spaces
	3-track internal: 6-mil lines 6-mil spaces	3-track internal: 6-mil lines 6-mil spaces	3-track internal: 6-mil lines 6-mil spaces	3-track internal: 6-mil lines 6-mil spaces
CONNECTORS	963L2-300 (300 pins)	963C2-200 (200 pins)	two 963L2-300 (600 pins)	963R2-400 (400 pins)
REPAIR AND MODIFICATION	per X-74425 and X-18351	per X-74425 and X-18351	per X-74425 and X-18351	per X-74425 and X-18351
COMPONENT HEIGHT	per X-74425 L-903234	per X-74425 L-903234	per X-74425 L-903234	per X-74425 L-903234
MAXIMUM POWER DISSIPATION (watts)	30-35	30-35	70-75	30-35
SOLDER MASK	per X-17815	per X-17815	per X-17815	per X-17815
FACEPLATE (inches)	1.0-2.0	0.75-1.0	1.0-1.50	1.25

4.5 CIRCUIT PACK BACKPLANE KEYS

To prevent a circuit pack from being installed in an inappropriate position, backplane keys are used to permit only those circuit pack types with the appropriate connector plug arrangement to be installed in a given apparatus mounting position. Table 4-4 lists the backplane keys and associated circuit pack connector plugs used for the Processor Unit, J3T060AA-1. Table 4-5 lists the backplane keys and associated circuit pack connector plugs used for the Growth Unit, J3T060AB-1. Figure 4-6 shows a typical key holder.

The UN375 and UN376 circuit packs are keyed so that they can be installed in a UN373 slot, a UN377 slot, or in a PC community slot.

The UN373 and UN580 circuit packs are keyed so that they can be installed in a UN373 slot or a UN580 slot.

Also note that the UN377 slot and the Main Memory (MM) slot (KLW32, KLW40, KLW48, KLW64, or KLW128 circuit pack slot) have the same backplane key code. However, since the UN-type circuit pack and the KLW-type circuit pack are different sizes, they cannot be mistakenly interchanged.

Table 4-4 Processor Unit Backplane Keys

BACKPLANE KEY CODE	PROCESSOR UNIT EQL	CIRCUIT PACK	CONNECTOR PLUG
B-01289	13-065	KBN15 DMA 1	C-34567
B-01289	13-075	KBN15 DMA 0	C-34567
B-01367	04-060	410AA Power Converter B	C-24589
B-01367	04-088	410AA Power Converter C	C-24589
B-01367	13-052	410AA Power Converter A	C-24589
B-01367	13-088	410AA Power Converter D	C-24589
B-01367	13-188	410AA Power Converter E	C-24589
B-13678	13-170	TN2116 SCSI Host Adapter	C-02459
B-02368	04-038	KLW31 CC	C-14579
B-02457	04-018	EX 0 Slot	C-13689
B-02457	04-028	EX 1 Slot	C-13689
B-03456	13-060	TN1821 CUPS	C-12789
B-12579	04-050	UN379 UC	C-03468
B-14568	04-065	KBN10 DFC	C-02379
B-14789	04-080	TN1820 IOPPS	C-02356
B-36789	04-008	MM Slot (KLW32/KLW40/KLW48)	C-01245

B-36789	04-178	UN377 [a] PSSDB (Spare)	C-01245
B-36789	04-186	UN377 [a] PSSDB	C-01245
B-46789	13-178	UN373 DFC	C-01235
B-56789	04-094	TN983/UN583/UN597 MTTYC	C-01234
B-56789	04-102	PC01	C-01234
B-56789	04-110	UN33D SCSD Controller	C-01234
B-56789	04-118	PC03	C-01234
B-56789	04-130	PC10	C-01234
B-56789	04-138	PC11	C-01234
B-56789	04-146	PC12	C-01234
B-56789	04-162	UN375 MHD Drive	C-012
B-56789	04-186	UN376 [b] DAT Drive	C-012
B-56789	13-094	PC20	C-01234
B-56789	13-102	PC21	C-01234
B-56789	13-110	PC22	C-01234
B-56789	13-118	PC23	C-01234
B-56789	13-130	PC30	C-01234
B-56789	13-138	PC31	C-01234
B-56789	13-146	PC32	C-01234
B-56789	13-162	UN375 MHD Drive	C-012

Notes:

a. Located in CU 1.

b. Located in CU 0.

Table 4-5 Growth Unit Backplane Keys

BACKPLANE KEY CODE	GROWTH UNIT EQL	CIRCUIT PACK	CONNECTOR PLUG
B-01367	04-006	410AA Power Converter F	C-24589
B-01367	04-034	410AA Power Converter G	C-24589
B-01367	04-190	410AA Power Converter H	C-24589
B-13678	04-172	TN2116 SCSI Host Adapter	C-02459
B-14568	04-011	KBN10 IOP	C-02379
B-14789	04-026	TN1820 IOPPS	C-02356
B-46789	04-180	UN373 or UN580 DFC	C-01235
B-56789	04-040	PC00	C-01234
B-56789	04-048	PC01	C-01234
B-56789	04-056	PC02	C-01234
B-56789	04-064	PC03	C-01234
B-56789	04-072	PC10	C-01234
B-56789	04-080	PC11	C-01234
B-56789	04-088	PC12	C-01234
B-56789	04-096	PC13	C-01234
B-56789	04-108	PC20	C-01234
B-56789	04-116	PC21	C-01234
B-56789	04-124	PC22	C-01234
B-56789	04-132	PC23	C-01234
B-56789	04-140	PC30	C-01234
B-56789	04-148	PC31	C-01234
B-56789	04-156	PC32	C-01234
B-56789	04-164	PC33	C-01234

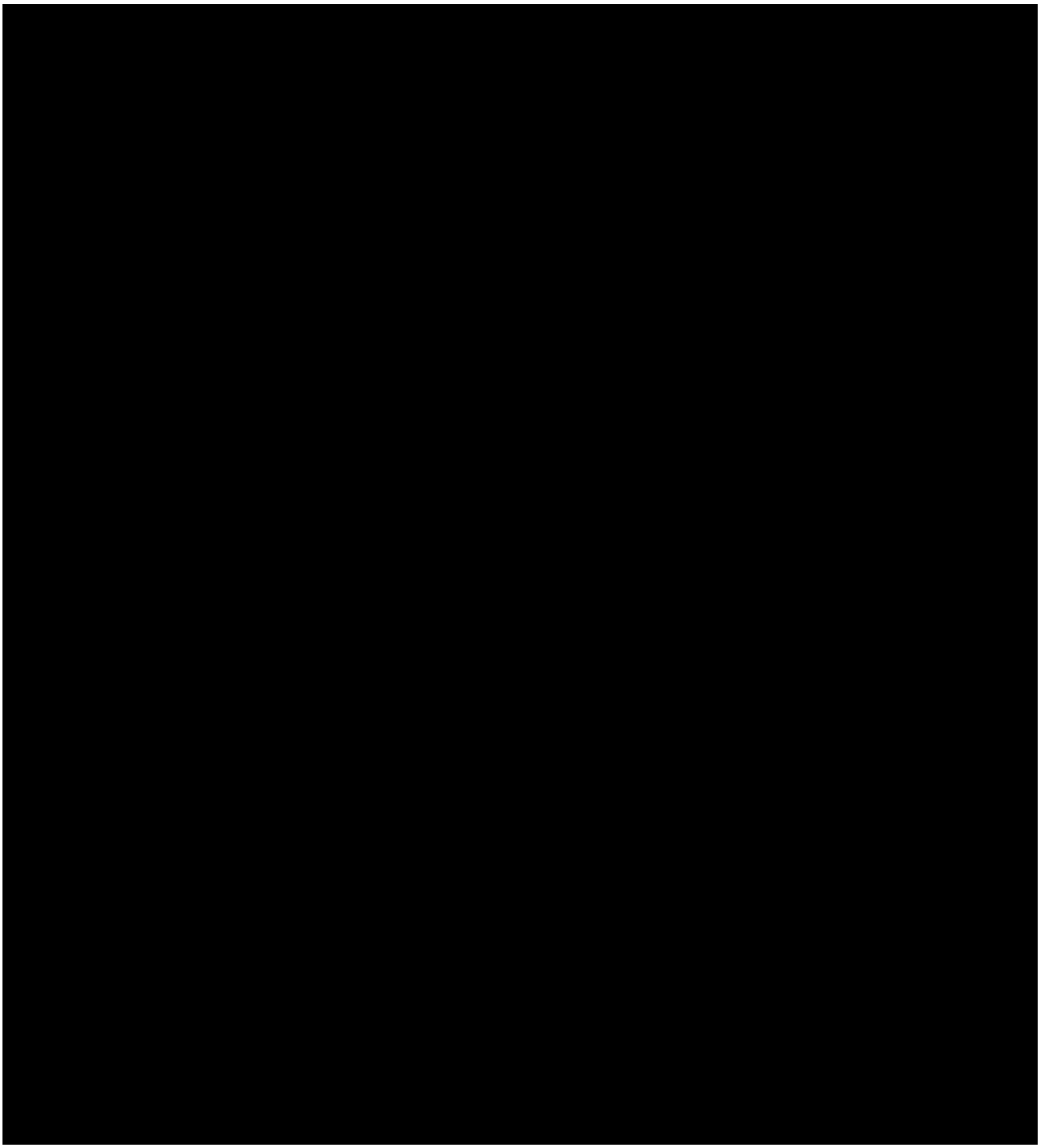


Figure 4-6 Backplane Key Holder

4.6 OPTIONAL CIRCUIT PACKS AND MODULES

4.6.1 UN379 Utility Circuit (UC) Circuit Pack

The optional Utility Circuit (UC) circuit pack (UN379), along with the Generic Access Package (GRASP) software or the Enhanced Generic Access Package (EGRASP) software, monitors operations between the Central Control (CC) and Main Memory (cache or main store) for the purpose of program debugging and testing. One UC circuit pack (UN379) is optionally equipped in each Control Unit (CU).

4.6.2 CM369A MLTS Interface Circuit Module

The CM369A Micro Level Test Set (MLTS) interface circuit module plugs into two connectors on the faceplate of the CC circuit pack (KLW31). The MLTS interface circuit module provides the connections between the MLTS host (TN16) and the CC. Four 8-foot ribbon cables are used to connect the MLTS and the CM369A MLTS interface circuit module.

NOTE: The MLTS is ***not*** available via the Super J-Drawing, J3T061A-1. The MLTS is intended for laboratory use only.

The MLTS interface circuit module is powered by the MLTS and has no intelligence of its own. All MLTS interface functions are controlled by the MLTS. The MLTS is used to do the following:

- Perform remote diagnostics on the 3B21D computer.
- Determine the condition of a failed 3B21D computer when other recovery actions have failed.

See 235-105-500, *5ESS®-2000 Switch Maintenance Reference Handbook*.

4.7 EXPANSION SLOTS (KLW-SIZE BOARDS)

The Expansion (EX) slots provide an interface for new (future) hardware features to access the Main Store (MAS) and CC via the Central Control Input/Output (CCIO) bus and the Main Store Bus (MASB). Each CU has two EX slots (EX 0 and EX 1).

Expansion slot functionality has yet to be defined.

4.8 BACKPLANE WIRING

The Processor Unit and Growth Unit backplanes are designed to minimize the amount of external wiring needed to complete circuit pack connections.

4.8.1 Processor Unit Backplane Wiring

The following external wires are used on the Processor Unit backplane.

4.8.1.1 Central Control Interrupt Status Register Inputs

The CC circuit pack (KLW31) has 11 interrupt status register inputs from the SREG0 ASIC that are brought out to the backplane. These are wired to interrupt signals from the two expansion slots and the two DMA Controller slots. These signals are routed to a pin field alongside the CC connector as shown in Table 4-6 . This permits the signals to be easily connected using either machine-made wire straps or an external connector card in any fashion as needed.

Table 4-6 CC Interrupt Inputs

CC PIN	CC SIGNAL NAME	EXTERNAL FIELD	INTERRUPT DESCRIPTION	USE
044T	SIS150	044	NC [a]	
045T	SIS140	045	NC	
046T	SIS130	046	NC	
047T	SIS120	047	NC	
048T	SIS110	048	NC	
049T [b]	SIS100	049	D1INT10	DMA0 Interrupt 1
050T	SIS090	050	D1INT00	DMA1 Interrupt 0
052T	SIS070	052	D0INT10	DMA0 Interrupt 1
053T	SIS060	053	D0INT00	DMA0 Interrupt 0
054T	SIS040	054	E1INT0	EX1 Interrupt 0
055T	SIS030	055	E0INT0	EX0 Interrupt 0

Notes:

a. NC is No Connection.

b. CC pin 049T is wired to EXTERNAL FIELD pins 052 and 053.

4.8.1.2 Central Control Identification

The Central Control (CC) circuit pack (KLW31) identity as CU 0 or CU 1 is determined by the backplane in which the circuit pack is installed. In CU 1, EQLs 038-000T and 038-001T are wired together. The KLW31 is set for CU 0 as a default. Grounding the CCID0 pin tells the KLW31 it is CU 1.

4.8.1.3 DMA Controller Straps

For normal operation, straps are used with the DMA controller. However, each KBN15 DMA circuit pack has an input that can disable quad word memory access. By default, quad word memory access is disabled with no plans to enable it at present. If quad word memory access needs to be disabled, a strap is added on the backplane to disable quad word access for each KBN15 circuit pack. Four straps are required, as follows:

- EQL 28-075-736 tied to EQL 28-075-636
- EQL 28-065-736 tied to EQL 28-065-636
- EQL 53-075-736 tied to EQL 28-075-636
- EQL 53-065-736 tied to EQL 28-065-636.

The DMA positions also have an input that provides DMA identity, but it is permanently wired in the backplane.

If for some reason quad work memory access needs to be enabled, remove the four straps previously mentioned.

4.8.1.4 Expansion Slot ID

The expansion slots do not need external wires. An expansion slot ID input is provided that is permanently wired in the backplane.

4.8.2 Growth Unit Backplane Wiring

There are no wires on this backplane. All connectivity is via the printed circuits within the backplane.

4.9 CABLING

4.9.1 Design Characteristics

The cabling design follows the following guidelines:

- All internal ribbon cabling is twisted pair to minimize electromagnetic noise.
- Total cable length for differential SCSI bus does not exceed 25 meters.
- SCSI stub length is from backplane connector to SCSI device driver pin. The differential SCSI bus stub length does not exceed 0.2 meter per stub.
- All cables are stamped with the appropriate cable EQL information.
- Cable wires and connectors are *UL*®-recognized components and have a flammability rating of 94V-1 or better.

- Cable insulation meets *UL* flammability standard VW1.
- Cables are routed away from sharp edges and from moving parts.

4.9.2 Logic and Power Cables

See Section 12 for a listing of logic and power cables required for the 3B21D computer system.

4.10 DESIGNATION STRIPS

Designation strips are used on the units to identify the circuit pack positions. In most cases, the information on the designation strips includes the equipment location (EQL) and circuit pack type designation. In other cases, SPU, MHD, and MT numbers are on the designation strips. Optional peel-off labels are provided to designate application-specific devices. Circuit pack positions are color-coded on the designation strips with respect to the DC-to-DC converter supplying power to the circuit pack.

Figure 4-5 shows the labeling for the Processor Cabinet fuses.

4.11 CABINET COOLING

4.11.1 Processor Cabinet Cooling

Processor Cabinet cooling is accomplished using a Bidirectional Cooling Unit, J5D003FH-2. The cooling unit is located at the middle of the Processor Cabinet at EQL 36. The upper half of the Processor Cabinet (Processor Unit 1 and IOP 3-SPU Growth Unit) is cooled by pulling the air through the front door, pushing it up through the front three fans, over the circuit packs, and then exhausting the air flow out at the top of the cabinet. The bottom half of the Processor Cabinet (Processor Unit 0 and IOP 2-SPU Growth Unit) is cooled by pulling the air through the rear door, pushing the air flow down the rear three fans, over the circuit packs, and exhausting the air flow out at the bottom of the cabinet. This cooling technique provides more efficient cooling due to lower air resistance and temperature rise at equipment exhaust. The cooling unit is capable of delivering air flow at 450 to 500 CFM with three single-high apparatus housings fully equipped with UN-type circuit packs.

Unoccupied slots in an apparatus housing are covered with standard *Fastech* press-on plastic filler plates to contain the cooling air flow. The filler plates present the same appearance as the circuit pack faceplates.

4.11.2 Peripheral Growth Cabinet Cooling

For the Peripheral Growth Cabinet, cooling is provided by each of the 9-track tape units.

4.11.3 Bidirectional Cooling Unit, J5D003FH-2

The Bidirectional Cooling Unit, J5D003FH-2, is equipped in the Processor Cabinet at EQL 36. The unit contains two groups of fans and an alarm circuit. Three fans are in each group. The fan motors operate on -48 V DC. One group blows air upward to cool Processor 1 and IOP 3-SPU Growth Unit; the other group blows downward to cool Processor 0 and IOP 2-SPU Growth Unit.

Each fan includes an integral Fan Performance Sensor (FPS) that operates from +5 V obtained from a Board-Mounted Power Module (BMPM) in the alarm circuit. If one or more fans fail, the circuit latches an alarm state on its scan point output. The SD point is used to retire the alarm. A switch on the cooling unit can also be used to manually retire the alarm.

5. SYSTEM OVERVIEW AND CONTROL UNIT FUNCTIONAL DESCRIPTION □ CC

5.1 SYSTEM OVERVIEW

Figure 5-1 is a functional block diagram of the 3B21D computer. Each of the functional areas defined in Figure 5-1 is described in this section. The 3B21D computer is a duplexed, 32-bit machine with a 28-bit addressing capability (28 address bits plus 4 parity bits). Data paths in the Control Units (CUs) are 36 bits wide (32 data bits plus 4 parity bits). Store data is 39 bits wide (32 data bits and 7 parity/check bits).

Communication between the CUs and peripheral devices is via Direct Memory Access (DMA) dual-ported Dual Serial Channels (DSCHs).

5.1.1 Control Unit (CU)

Each Control Unit (CU) consists of the following functions:

- □ Central Control (CC)
- □ Cache Storage Unit (CSU)
- □ Main Store (MAS) and Main Store Update (MASU)
- □ Direct Memory Access (DMA)
- □ Expansion Slots (EX 0 and EX 1)
- □ Utility Circuit (UC).

Each CU is half of the duplexed Central Processing Unit (CPU) system. The CC, MAS, UC, EX, and input/output (I/O) functions are duplicated for reliability.

Local control of the 3B21D computer for normal operation and manual recovery procedures is via the Emergency Action Interface (EAI) to a Maintenance TTY (MTTY) and Receive-Only Printer (ROP).

5.1.1.1 Central Control (CC)

The 3B21D CC is a microprogram driven processor of the 3B21D computer and is contained on one circuit pack (KLW31). Each CU is equipped with one KLW31 circuit pack.

5.1.1.2 Expansion (EX) Slots

The EX slots provide an interface for new (future) hardware features to access the Main Store (MAS) and CC via the Central Control Input/Output (CCIO) bus and the Main Store Bus (MASB). Each CU has two EX slots (EX 0 and EX 1).

5.1.1.3 Utility Circuit (UC)

The UC is an optional function that monitors operations between the CC and the main memory (cache or main store) for the purpose of program debugging and testing. One UC circuit pack (UN379) is optionally equipped in each CU.

5.1.1.4 Cache Storage Unit (CSU)

The CSU provides a small, high-speed CC cache memory for the most recently accessed Main Store (MAS) words. The CC accesses the CSU concurrently with the MAS access on the Main Store Bus (MASB). The CSU is part of the CC circuit pack (KLW31).

5.1.1.5 Main Store (MAS) and Main Store Update (MASU)

The MAS provides a minimum of 32 MB to a maximum of 256 MBs of Dynamic Random Access Memory (DRAM). One MAS circuit pack (KLW32, KLW40, KLW48, KLW64 or KLW128) is equipped in each CU. The same size MAS circuit pack is used in each CU. The KLW32 circuit pack is initially equipped with 32 MB of DRAM. The KLW40 circuit pack is initially equipped with 40 MB of DRAM. The KLW48 circuit pack is initially equipped with 48 MB of DRAM. The KLW64 circuit pack is initially equipped with 64 MB of DRAM. The KLW128 circuit pack is initially equipped with 128 MB of DRAM. Additional memory is added to a MAS circuit pack in either 8 MB or 32 MB increments. The addition of three 32 MB Single In-line Memory Modules (SIMMs) to a KLW32 circuit pack provides a current maximum of 128 MBs of DRAM. Twenty eight bits of address is designed into the system buses and registers for future expansion to 256 MB. Store data is 36 bits (32 data bits and 4 parity bits); however, within the MAS circuit pack store data is 39 bits wide (32 data bits and 7 parity/check bits). The MASs in both Control Units (CUs) are kept coherent using the Update Bus. If control must be switched from the on-line processor to the other processor, the contents of both the off-line memory and the on-line memory must be identical. If the MASs are not coherent, the on-line processor must copy its data to the off-line MAS before the switch takes place.

5.1.1.6 Direct Memory Access (DMA)

The Direct Memory Access (DMA) provides peripheral devices access to the MAS via the MASB, and provides the CC access to the peripheral devices through the CCIO bus. Each DMA supports connections for a maximum of 16 peripheral devices.

Peripheral devices are connected to the DMA through the Dual Serial Channel (DSCH). These devices have a dual ported DSCH interface that allows them to communicate with either CU 0 or CU 1. Two DMA circuit packs (KBN15s) can be equipped in each CU. DMA 0 is standard and DMA 1 is optional.

The relationship of peripheral devices to DMA 0 and DMA 1 is as follows.

- DMA 0 and DMA 1 each provide four channels. DMA 0 supports channels 11, 12, 13, and 14. DMA 1 supports channels 16, 17, 18, and 19.
- Each channel supports four DSCH interfaces.

5.1.2 Peripheral Devices

Figure 5-1 shows three types of peripheral devices: the Input/Output Processor (IOP), Disk File Controller (DFC), and Communications Module/Communications Network Interface (CM/CNI). The IOP provides connections to terminals, networks, and some tape devices. The DFC provides connection to peripherals with Small Computer System Interface (SCSI) interfaces, which include disk and tape drives. The third device, CM/CNI, represents application peripheral hardware. The term "DFC" is not accurate since support is not limited to disk peripherals; however, the nomenclature is retained from the 3B20D computer.

Note that the 3B21D computer differs from the 3B20D computer in that the 9-track tape is an SCSI peripheral device supported off of the DFC in the 3B21D computer while it is supported off of the IOP in the 3B20D computer. Also note that 3B21D computer DFC channel and device allocations differ from the 3B20D computer in that there are fewer devices per channel.

5.1.2.1 Disk File Controller (DFC)

The 3B21D computer can have three DFCs (DFC 0 through DFC 2) all equipped in the Processor Cabinet as follows:

- DFC 0 is in Processor Unit 0 and can be configured as the following:
  - A TN2116 at equipment location (EQL) 28-170 and a UN373 at EQL 28-178, or either a UN580 or

UN580B at EQL 28-178.

- DFC 1 is in Processor Unit 1 and can be configured as the following:
  - A TN2116 at EQL 11-170 and a UN373 at EQL 53-178, or either a UN580 or UN580B at EQL 53-178.

- DFC 2 is in the Growth Unit and can be configured as the following:
  - A TN2116 at EQL 11-172 and a UN373 at EQL 11-180, or either a UN580 or UN580B at EQL 11-180.

Each DFC provides two SCSI buses (SBUS A and SBUS B). A maximum of seven SCSI peripheral devices can be equipped on an SCSI bus. Therefore, each DFC can support a maximum of 14 SCSI devices. DFC 0 provides two SCSI buses, SBUS 0(A) and SBUS 2(B). DFC 1 provides two SCSI buses, SBUS 1(A) and SBUS 3(B). DFC 2 provides two SCSI buses, SBUS 4(A) and SBUS 6(B).

5.1.2.2 Input/Output Processor (IOP)

The 3B21D computer can have four IOPs (IOP 0 through IOP 3) equipped in the Processor Cabinet. IOP 0 is equipped in Processor Unit 0 at EQL 19-065. IOP 1 is equipped in Processor Unit 1 at EQL 45-065. IOP 2 is equipped in the Growth Unit at EQL 11-011. IOP 3 is equipped in the Growth Unit at EQL 62-011.

Functionally, an IOP can support four peripheral controller communities with each community supporting four peripheral controllers. Therefore, 16 peripheral devices can be supported by an IOP. IOP 0 and IOP 1 are exceptions. IOP 0 and IOP 1 each support up to 15 Peripheral Controller (PC) slots. IOP 2 and IOP 3 each support up to 16 PC slots. The maximum number of available PC slots in a Processor Unit is 15; the maximum number of available PC slots in a Growth Unit is 16.

For IOP 0 and IOP 1, Peripheral Community 0, slot 0 (PC00) is always equipped with a TN983, UN583, or UN597 MTTY Controller circuit pack. Also, IOP 0 and IOP 1, Peripheral Community 0, slot 2 (PC02) is reserved for a UN33D or UN933 Scanner and Signal Distributor circuit pack, which provides scan and signal distributor point interfaces for the 3B21D computer.

5.1.3 Port Switch and Scanner-Distributor Buffer (PSSDB)

The Port Switch and Scanner-Distributor Buffer (PSSDB) switches the maintenance terminal (MTTY) and the local receive-only printer (ROP) between the MTTY Controller (MTTYC) circuit pack (TN983/UN583/UN597) in IOP 0 and IOP 1. The PSSDB also buffers the scanner and signal-distributor controller from non-3B21D computer circuits such as office alarms, smoke detectors, and security monitoring devices.

One port switch is equipped in Processor Unit 1. In the 3B21D computer, the PSSBD is located in CU 1. (Note that in the 3B20D computer the PSSBD is located in CU 0.)

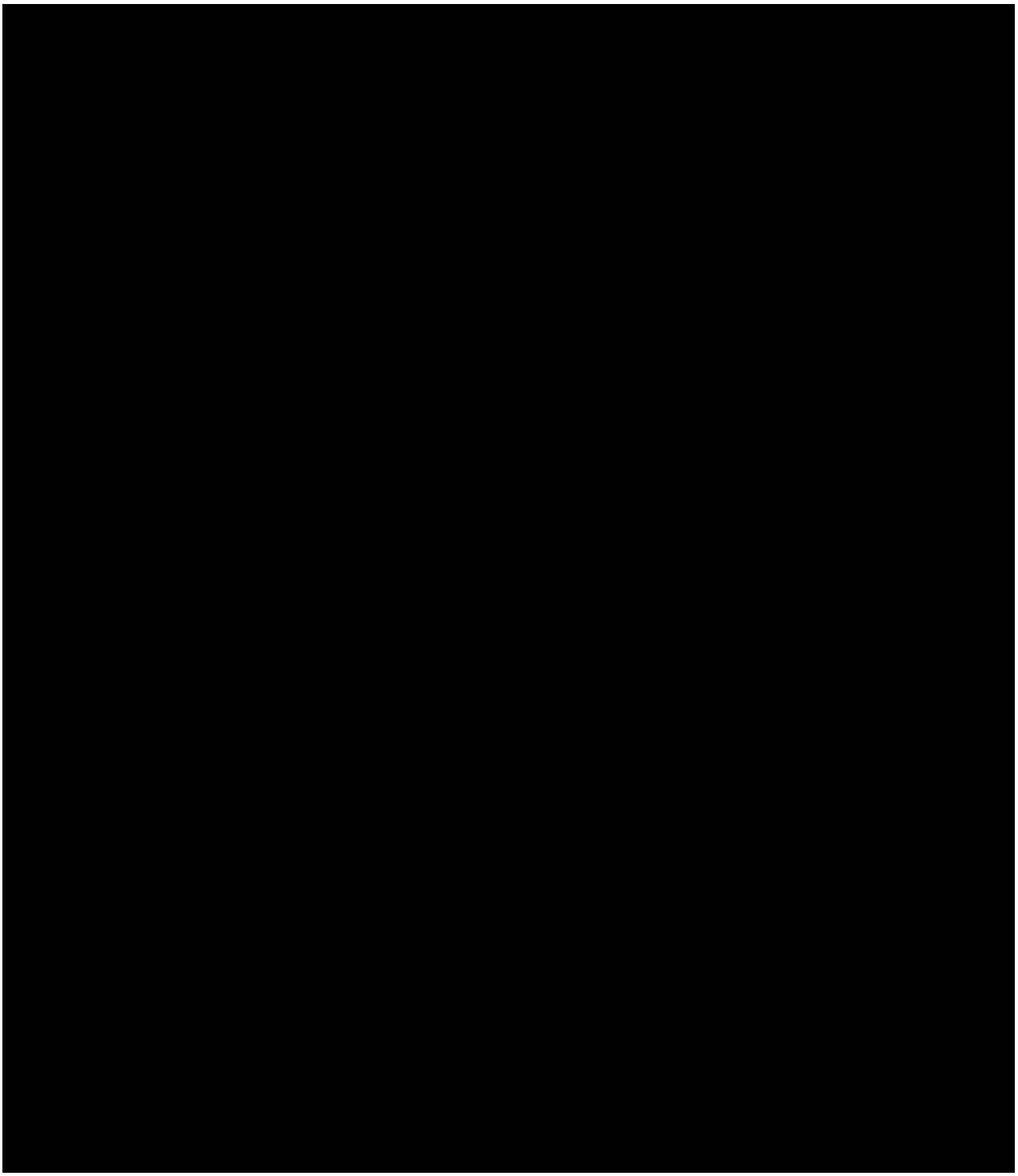


Figure 5-1 3B21D Computer Functional Block Diagram

5.2 CENTRAL CONTROL (CC)

Figure 5-2 is a functional block diagram of the Central Control (CC) circuit pack (KLW31). The CC is a microprogram-driven processor that contains the following functions:

- Circuit pack identification capability
- MicroController (MC)

- MicroInstruction Store (MIS)
- Maintenance Channel (MCH)
- Emergency Action Interface (EAI)
- Data Manipulation Unit (DMU)
- Special Registers (SREGs)
- Store Address Interface (SAI)
- Store Data Interface (SDI)
- Store Address Translator (SAT)
- Cache Storage Unit (CSU)
- Micro Level Test Set (MLTS) Interface.

Following a description of the CC interfaces, each of these functions is described in this section.

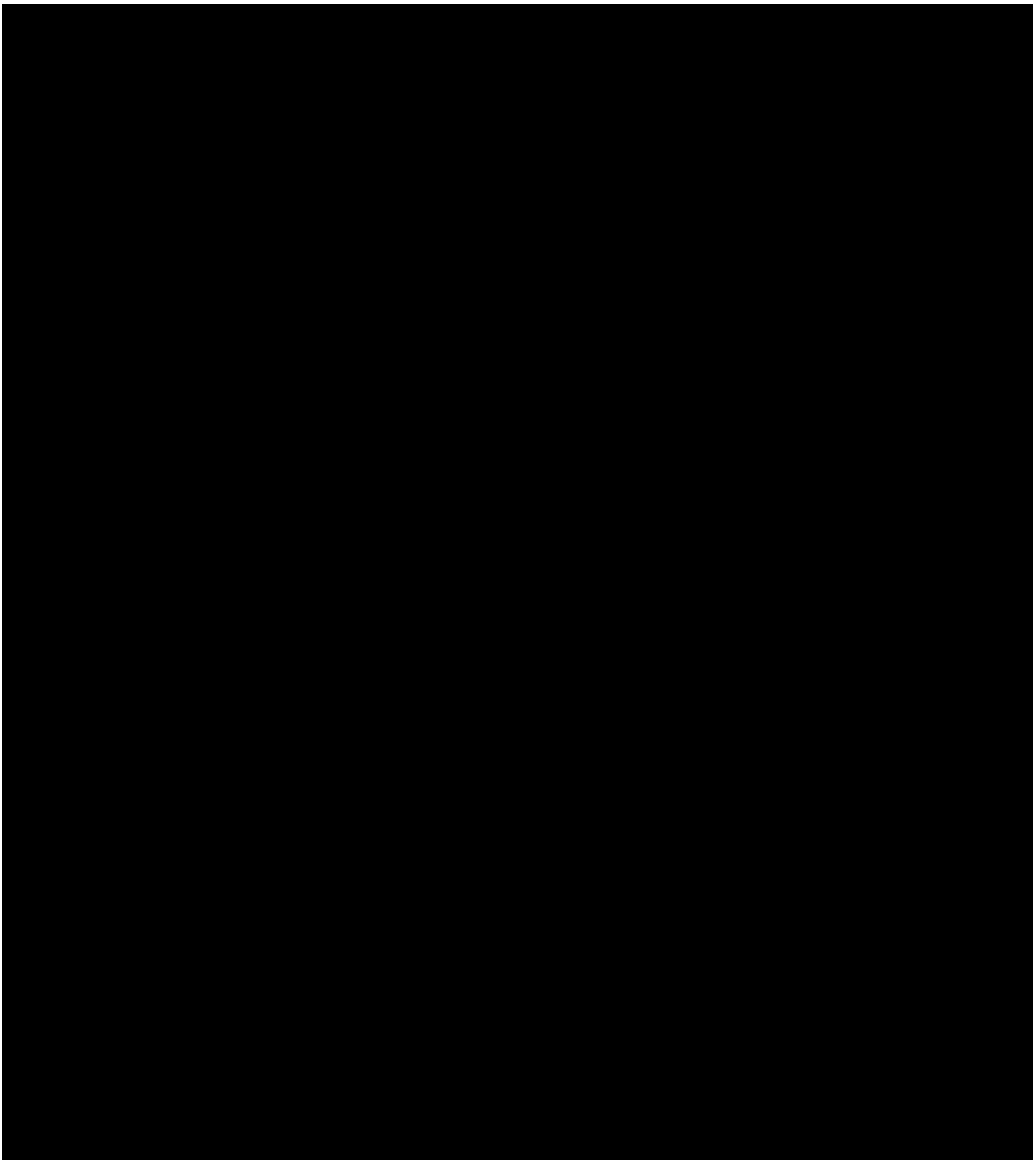


Figure 5-2 Central Control (CC) Functional Block Diagram

5.2.1 CC Interfaces

5.2.1.1 Central Control I/O (CCIO) Bus

The Central Control Input/Output (CCIO) bus interfaces the Central Control (CC), Direct Memory Access Controller (DMAC), and the expansion slots (EX 0 and EX 1).

The CCIO bus is summarized in Table 5-1 . Figure 5-3 is a functional block diagram of the CCIO bus.

Table 5-1 Central Control Input/Output (CCIO) Bus

CATEGORY	SIGNAL	TYPE	DESCRIPTION	CC	DMAC 0	DMAC 2	EX0	EX1
DATA	CCIOD (31-00)1	Tristate	32 data bits, noninverted.	I/O	I/O	I/O	I/O	I/O
	CCIOD (35-32)1	Bidirec-tional	4-byte even parity bits over 32 data bits.	I/O	I/O	I/O	I/O	I/O
ADDRESS	CCIOAD (5-0)1	Unidirec-tional	6 address bits, 3-out-of-6 code	OUT	IN	IN	IN	IN
CONTROL	CIORD0 (PPR 0)	Unidirec-tional	Read Data	OUT	IN	IN	IN	IN
	CIORST0 (PPR 1)		Read Status Register	OUT	IN	IN	IN	IN
	CIORINT0 (PPR 2)		Read Interrupt Register	OUT	IN	IN	IN	IN
	CIORSR0 (PPR 3)		Read Service Request Register	OUT	IN	IN	IN	IN
	CIOIAK0 (PPR 4)		Interrupt Acknowledge	OUT	IN	IN	IN	IN
	CIOEACK0 (PPR 5)		Error Acknowledge	OUT	IN	IN	IN	IN
	CIOIDL0 (PPR 7)		Idle Channel	OUT	IN	IN	IN	IN
	CIOCLE0 (PPR 8)		Clear Error	OUT	IN	IN	IN	IN
	CIOWD0 (PPR 9)		Write Data	OUT	IN	IN	IN	IN
	CIOWCA0 (PPR 10)		Write Control/Address	OUT	IN	IN	IN	IN
	CIOINH0 (SSR 9 or 30)		Input/Output Inhibit	OUT	IN	IN	IN	IN
RESPONSE	CIOACK (5-0)1	Open Collector	Acknowledge	IN	OUT	OUT	OUT	OUT
	CIOASW0	Unidirec-tional	All-Seems-Well	IN	OUT	OUT	OUT	OUT
	CIORDY0		Ready	IN	OUT	OUT	OUT	OUT
	CIOCER0		Channel Error	IN	OUT	OUT	OUT	OUT
INTER-RUPTS [a]	D0INT00	Open Collector	DMAC 0 Channel 0 Interrupt Interrupt summary for 3B21D peripherals	IN	OUT	NC [b]		
	D0INT10		DMAC 0 Channel 1 Interrupt Interrupt summary for application peripherals	IN	OUT	NC		
	D1INT00		DMAC 1 Channel 0 Interrupt Interrupt summary for 3B21D peripherals	IN	NC	OUT		
	D1INT10		DMAC 1 Channel 1 Interrupt Interrupt summary for application peripherals	IN	NC	OUT		
	E0INT00		Expansion Slot 0 Interrupt	IN	NC	NC	OUT	NC
	E1INT00		Expansion Slot 1 Interrupt	IN	NC	NC	NC	OUT

Notes:

a. The machine is provided with D0INT00 and D0INT10 interrupts connected to the SIS10 input.

b. NC = No Connection.

Figure 5-3 Central Control Input/Output (CCIO) Bus Functional Block Diagram

The CCIO bus consists of data, data parity, address, control, response, and interrupt signals as follows.

5.2.1.1.1 CCIO Data Bus

The CCIO data (CCIOD) bus is 32-bit bus. The bus connects the DMAC to the Channel Data Register (CDR) on the CC circuit pack.

5.2.1.1.2 CCIO Data Parity

Even parity is maintained across each byte of the CCIO data bus. Parity is checked on the DMAC side of the CCIO bus when the CC writes a command to the DMAC. The parity bits are designated CCIOD(35-32)1.

5.2.1.1.3 CCIO Address Bus

The 6-bit CCIO address (CCIOAD) bus is driven by the Channel Address Register (CAR) field of the CC Hardware Status Register (HSR) bits 15 through 10. A 3-out-of-6 code is used for the addresses. Table 5-2 provides DMAC CCIO address information. The addresses for channels 10 through 19 are used for the DMACs and the associated DSCHs. The other channel addresses (00 through 09) are reserved for the expansion slots (EX 0 and EX 1).

Table 5-2 DMAC CCIO Addressing

DMA CONTROLLER	CHANNEL	HSR BITS 15-10	ADDRESS (HEX)
EX 0	EX 0 (CHANNEL 00)	000111	0x07
EX 0	EX 0 (CHANNEL 01)	001011	0x0B
EX 0	EX 0 (CHANNEL 02)	001101	0x0D
EX 0	EX 0 (CHANNEL 03)	001110	0x0E
EX 0	EX 0 (CHANNEL 04)	010011	0x13
EX 1	EX 1 (CHANNEL 05)	010101	0x15
EX 1	EX 1 (CHANNEL 06)	010110	0x16
EX 1	EX 1 (CHANNEL 07)	011001	0x19
EX 1	EX 1 (CHANNEL 08)	011010	0x1A
EX 1	EX 1 (CHANNEL 09)	011100	0x1C
DMAC 0	DMAC 0 (CHANNEL 10)	100011	0x23
DMAC 0	DSCH 0 (CHANNEL 11)	100101	0x25
DMAC 0	DSCH 1 (CHANNEL 12)	100110	0x26
DMAC 0	DSCH 2 (CHANNEL 13)	101001	0x29
DMAC 0	DSCH 3 (CHANNEL 14)	101010	0x2A
DMAC 1	DMAC 1 (CHANNEL 15)	101100	0x2C
DMAC 1	DSCH 0 (CHANNEL 16)	110001	0x31
DMAC 1	DSCH 1 (CHANNEL 17)	110010	0x32
DMAC 1	DSCH 2 (CHANNEL 18)	110100	0x34
DMAC 1	DSCH 3 (CHANNEL 19)	111000	0x38

5.2.1.1.4 CCIO Control Leads

Control leads are driven by CC registers. Ten control pulses are driven by Pulse Point Register (PPR) bits 05-00 and 10-07. An I/O inhibit signal is driven by combining (logical OR) the System Status Register (SSR) bits 09 and 30.

5.2.1.1.5 CCIO Response Signals

The four CCIO response signals are as follows:

Acknowledge (CIOACK[0-5]1)

The DMAC acknowledges the receipt of any control pulse by returning a 3-out-of-6 code on the acknowledge leads. Each DMAC returns its address. The DMAC 0 returns a 100011 acknowledge pattern. The DMAC 1 returns a 101100 acknowledge pattern. If a valid acknowledge is ***not*** returned, the CC Error Register bits 17 and 18 are asserted.

Channel Error (CIOCER0)

The DMAC combines (logical OR) its error signal with the error signals from its four channels and passes the resulting error summary to the CC Error Register bit 16. This triggers an error interrupt in the CC.

All-Seems-Well (CIOASW0)

The All-Seems-Well signal indicates the absence of errors. Its status is stored in HSR bit 4. An All-Seems-Well failure asserts the CC Error Register bit 17.

Ready (CIORDY0)

The Ready is returned to the CC by the DMAC to synchronize the CC with the addressed channel. When the CC is reading data from a channel, Ready is asserted when the data is gated to the CCIO bus. For other control signals, Ready is returned immediately. Ready is stored in the CC as HSR bit 7. A Ready failure asserts the CC Error Register bit 17.

Table 5-3 summaries the CCIO response signals and identifies the Pulse Point Register (PPR) bit control pulse that triggers the response. Only one of these operations is active at any time. The violation of a 1-out-of-11 check causes a hardware error and asserts the CC Error Register bit 18 (ER18).

Table 5-3 CCIO Response Summary

CONTROL SIGNAL	PPR BIT	ADDRESS [a]

		DMAC	CHANNEL
Read Channel Data Buffer (CIORD0)	00	ASW, RDY [b], ACK	ASW [c], RDY [b], ACK
Read Channel Status Register (CIORST0)	01	ASW, RDY, ACK	ASW, RDY, ACK
Read Channel Interrupt State (CIORINT0)	02	ASW, RDY, ACK	P, ACK
Read Channel Service Request (CIORSR0)	03	ASW, RDY, ACK	P, ACK
I/O Interrupt Acknowledge (CIOIAK0)	04	ASW, RDY, ACK	□
Channel Error Acknowledge (CIOEACK0)	05	ASW, RDY, ACK	□
Idle Channel Sequencer (CIOIDL0)	07	ASW, RDY, ACK	P, ACK
Clear Channel Errors (CIOCLE0)	08	ASW, RDY, ACK	P, ACK
Write Channel Data Buffer (CIOWD0)	09	ASW, RDY, ACK	ASW, RDY, ACK
Write Channel Control/Address Register (CIOWCAO)	10	ASW, RDY, ACK, P	ASW, RDY, ACK, P

Notes:

a. ASW □ All-Seems-Well

RDY □ Ready

ACK □ Acknowledge

P □ Programmed I/O Request to DMAC microcode.

b. Read returns READY if CCIO BUSY is not set.

c. Read with CHANNEL ADDRESS returns ASW if CHANNEL ASW is set.

5.2.1.1.6 CCIO Interrupts

Six interrupts (two for each DMAC channel and one for each expansion slot) are part of the CCIO bus. Each channel interrupt signal is a summary of the interrupt requests coming from the channel peripheral devices.

5.2.1.2 Main Store Bus

The Main Store Bus (MASB) is used to transfer data to and from the Main Memory (MM) and the Central Control (CC), Direct Memory Access 0 (DMA 0), Direct Memory Access 1 (DMA 1), Expansion Slot 0 (EX 0), and Expansion Slot 1 (EX 1). The MASB consists of data, data parity, address, address parity, command, control, error, store requests, arbitrations, update control, and miscellaneous signals. Table 5-4 summarizes the MASB signals. Figure 5-4 is a functional block diagram of the MASB. The Update bus shown in Figure 5-4 is discussed in "Main Store (MAS) and Main Store Update (MASU)" in Section 6 .

Table 5-4 Main Store Bus

CATEGORY	SIGNAL	TYPE	DESCRIPTION	CC	DMA0/1	EX0/1	MM
DATA	SD(31-00)1	Tri [a]	32 noninverted	I/O	I/O	I/O	I/O
	SD(35-32)1	Bid [a]	4-byte even parity bits over 32 data bits	I/O	I/O	I/O	I/O
ADDRESS	SA(27-0)1	Tri [a]	28 bits, noninverted	OUT	OUT	OUT	IN
	SA(35-32)1	Uni [a]	4 bits, even parity	OUT	OUT	OUT	IN
COMMAND	SWRT0	Tri [a]	Write 0/Read 1 command	OUT	OUT	OUT	IN
	SBYTE0		Access size byte active 0	OUT	OUT	OUT	IN
	SHALF0		Access size half word active 0	OUT	OUT	OUT	IN
	SQUAD0		Access size quad word active 0	OUT	OUT	OUT	IN
	SRMW0		Read-Modify-Write command	OUT	OUT	OUT	IN
	SMAINT0		Maintenance access command	OUT	OUT	OUT	IN
	SCOMP1		Even parity bit over command bits	OUT	OUT	OUT	IN
CONTROL	DS0	Tri [a] Uni [a]	Quad word access only	OUT	OUT	OUT	IN
	PMSCM0	Uni [a]	Processor My-Store-Complete	IN	NC [b]	NC	OUT
	POSCM0		Processor	IN	NC	NC	OUT

			Other-Store-Complete				
	CAINVL0		Address Strobe-Cache Invalidate	IN	NC	IN	OUT
	D0SCM0		DMAC 0 Store Complete	NC	IN	NC	OUT
	D1SCM0		DMAC 1 Store Complete	NC	IN	NC	OUT
	E0SCM0		EX 0 Store Complete	NC	NC	IN	OUT
	E1SCM0		EX 1 Store Complete	NC	NC	IN	OUT
ERROR	MYSERA0	Uni [a]	My-Store-Error A	IN	IN	IN	OUT
	MYSERB0		My-Store-Error B	IN	IN	IN	OUT
	MYSERC0		My-Store-Error C	IN	IN	IN	OUT
	MYSERD0		My-Store-Error D	IN	NC	IN	OUT
	OSTERA0		Other-Store-Error A	IN	NC	NC	OUT
	OSTERB0		Other-Store-Error B	IN	NC	NC	OUT
	OSTERC0		Other-Store-Error C	IN	NC	NC	OUT
	OSTERD0		Other-Store-Error D	IN	NC	NC	OUT
STORE REQUESTS	PSGO01	Uni [a]	Processor request for Main Store Bus	OUT	NC	NC	IN
	D0SGO0		DMAC 0 request for Main Store Bus	NC	OUT	NC	IN
	D1SGO0		DMAC 1 request for Main Store Bus	NC	OUT	NC	IN
	E0SGO0		EX 0 request for Main Store Bus	NC	NC	OUT	IN
	E1SGO0		EX 1 request for Main Store Bus	NC	NC	OUT	IN
ARBITRA-TION	PABUS0	Uni [a]	Processor address enable	IN	NC	NC	OUT
	D0ABUS0		DMAC 0 address enable	NC	IN	NC	OUT
	D1ABUS0		DMAC 1 address enable	NC	IN	NC	OUT
	E0ABUS0		EX 0 address enable	NC	NC	IN	OUT
	E1ABUS0		EX 1 address enable	NC	NC	IN	OUT
	SDBUS0		Processor data enable	IN	NC	NC	OUT
	D0DBUS0		DMAC 0 data enable	NC	IN	NC	OUT
	D1DBUS0		DMAC 1 data enable	NC	IN	NC	OUT
	E0DBUS0		EX 0 data enable	NC	NC	IN	OUT
	E1DBUS0		EX 1 data enable	NC	NC	IN	OUT
UPDATE CONTROL	SISOU0	Uni [a]	Isolate other side request	OUT	NC	NC	IN
	SISOD0		Isolate DMAC0/1 request	OUT	NC	NC	IN
	SISOE0		Isolate EX0/1 request	OUT	NC	NC	IN
	PUPD0		Processor in update	OUT	NC	NC	IN
	PONL0		Processor on-line	OUT	NC	NC	IN
MISC.	OSTIME0	Uni [a]	Other store access time-out	IN	NC	NC	OUT
	SCR161		Cache Go Signal	OUT	NC	NC	IN
	SCR251		Arbiter reset	OUT	NC	NC	IN
	CACWT0		MM waits for invalidate	OUT	NC	OUT	IN
	CLER150		Clear Other store access time-out	OUT	NC	NC	IN
	CPWRCLR0		Power-up clear	IN	IN	IN	IN

Notes:

a. Tri = Tristate; Bid = Bidirectional; Uni = Unidirectional.

b. NC = No Connection.

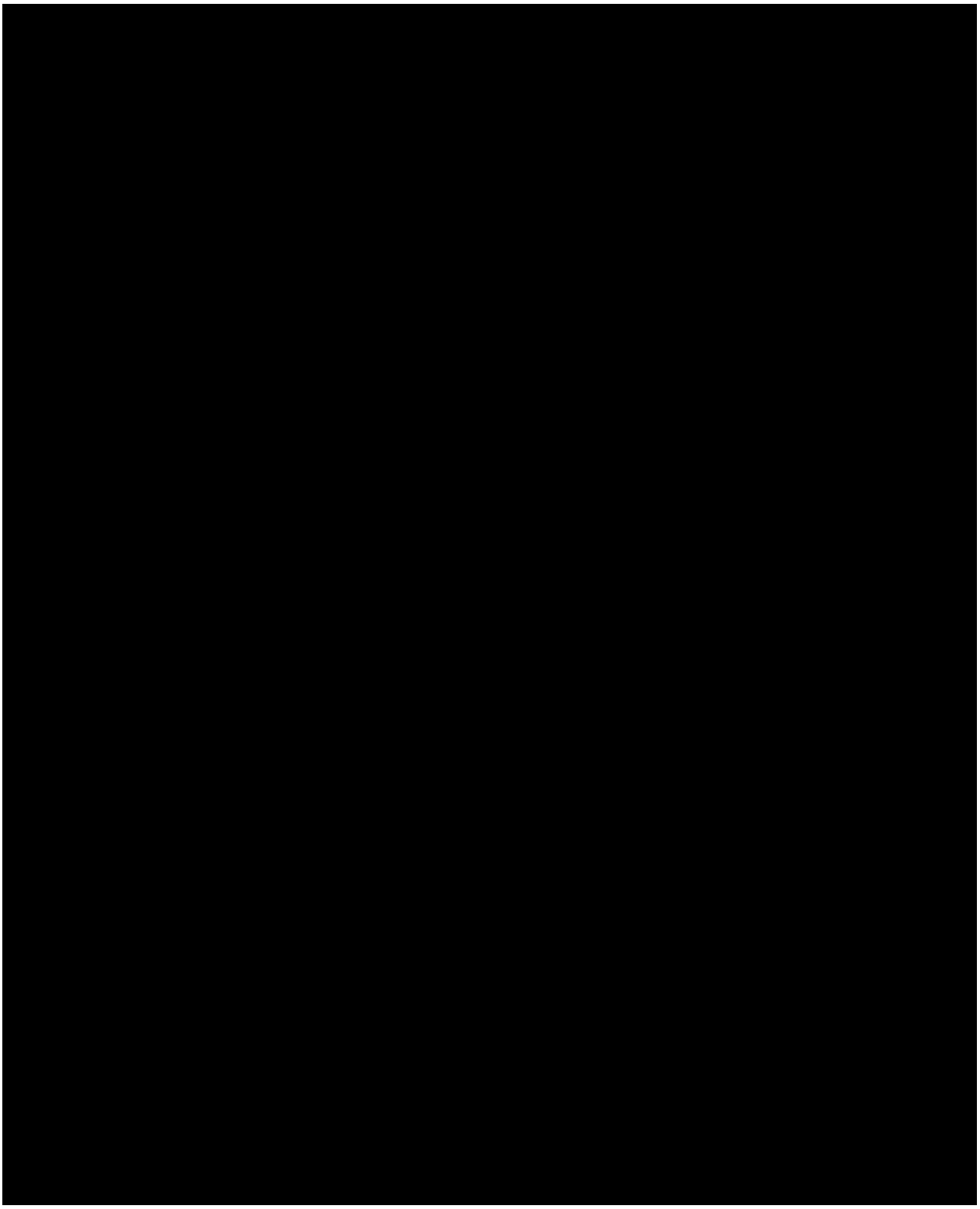


Figure 5-4 Main Store Bus Functional Block Diagram

5.2.1.3 MCH-to-MCH Link

The Maintenance Channel Link (MCHL) provides a direct connection between the Central Control (CC) units in Control Unit 0 (CU 0) and Control Unit 1 (CU 1). This link is needed for the duplexed operation of the CC. There is a Maintenance Channel (MCH) circuit on both ends of the link. A CC unit can request its

MCH to send instructions to the MCH in the other CU. These instructions, called slave commands, tell the receiving MCH to read and write its MIS buses, read and write its interface, read its MTC bus, or to clear and set certain status bits. The MCHL is also used to carry the stop and switch command from one CU to the other CU. These functions are further described in "Maintenance Channel (MCH)" in this section.

The MCHL interface is identical in the 3B20D and 3B21D computers in that the same format is used in the Dual Serial Channel (DSCH) interface. There are five signals in the MCHL interface. These five signals are driven electrically as five differential pairs as shown in Table 5-5 . The REQAP/N pair carries the stop and switch signal that requests the receiving CC to go on-line. The REQA signal is used separately from the other four signals in the MCHL that are used for other data transfer and command functions. The CLKA and XCKA signals are used as timing references for the data. The CLKA signal is an input for received data. The XCKA signal is sent out with the transmitted data. The data transmission contains an 8-bit start code and can optionally include 32 data bits and 4 parity bits. The data is split in two halves. The high-order bits are sent on the DAHA signal; the low-order bits are sent on the DALA signal. The data parity bits are used as parity bits in the MCHL. The MCHL protocol uses odd parity, requiring the 3B21D computer MCH circuits to do parity conversion on these bits.

Figure 5-5 shows the MCHL protocol. Table 5-5 summarizes the MCHL signals. Figure 5-6 is a functional block diagram of the MCHL.

Table 5-5 Maintenance Channel Link (MCHL) Interface

SIGNAL	TYPE	DIRECTION	DESCRIPTION
DAHAP	RS-422	I/O	Serial link high-order bits, positive phase
DAHAN	RS-422	I/O	Serial link high-order bits, negative phase
DALAP	RS-422	I/O	Serial link low-order bits, positive phase
DALAN	RS-422	I/O	Serial link low-order bits, negative phase
XCKAP	RS-422	IN	Serial link clock input, positive phase
XCKAN	RS-422	IN	Serial link clock input, negative phase
CLKAP	RS-422	OUT	Serial link clock output, positive phase
CLKAN	RS-422	OUT	Serial link clock output, negative phase
REQAP	RS-422	I/O	Link stop and switch interrupt, positive phase
REQAN	RS-422	I/O	Link stop and switch interrupt, negative phase

Figure 5-5 Maintenance Channel Link (MCHL) Protocol

Figure 5-6 Maintenance Channel Link (MCHL) Functional Block Diagram

5.2.1.4 CC to MLTS Link

The Micro Level Test Set (MLTS) link connects the MLTS host and the MLTS interface circuits. Figure 5-7 is a functional block diagram of the MLTS link.

Figure 5-7 Micro Level Test Set (MLTS) Link Functional Block Diagram

5.2.1.5 Boundary Scan Bus

A Boundary Scan (BS) bus is a serial bus used to link the components being tested. A component under test can be a circuit pack or a device on a circuit pack. Each boundary scan-compatible component has a Test Access Port (TAP).

All Application Specific Integrated Circuits (ASICs) on the Central Control (CC) circuit pack have a TAP. The serial test data input (TDI) and serial test data output (TDO) of each TAP interface with each other using a ring topology. The BS Master (BSM) can access ten different rings. The BSM is located on the KLW31 CC circuit pack and is controlled by the MCH. Ring selection is accomplished using an 8-bit register with a 1-to-10 demultiplexer and a 10-to-1 multiplexer. The demultiplexer and multiplexer select the active ring by driving a Test Mode Selection (TMS) signal and receiving an output data stream (TDO). Only one ring is active (selected) at a given time. Note that the MCH loads the idle value (0X00) between legal values to prevent simultaneous multiple ring accesses. The 8-bit register is loaded via the MCH. Table 5-6 lists the 8-bit codes used to select the BS rings.

Table 5-6 Boundary Scan Ring Selection Register Codes

BS RING	SELECT CODE
Idle (None Selected)	0X00
MM Slot (KLW32, KLW40, or KLW48)	0X08
TN1821 CUPS Circuit Pack	0X09
UN379 UC Circuit Pack	0X0A

KBN15 DMA0 Circuit Pack	0X0B
KBN15 DMA1 Circuit Pack	0X0C
EX0 Slot	0X0D
EX1 Slot	0X0E
TN1820 IOPPS in "My CU"	0X0F
TN1820 IOPPS in "Other CU"	0X10
KLW31 CC Circuit Pack	0X20

Figure 5-8 is a functional block diagram of a typical boundary scan ring. Figure 5-9 is a functional block diagram showing the boundary scan architecture for the 3B21D computer.

A boundary scan bus has five signals as follows:

TCK The boundary scan clock (TCK) is a free-running clock signal. All latches and registers retain their states while TCK is low.

TMS The test mode selection (TMS) signal selects the test mode and is clocked on the rising edge of TCK. In the test mode, the boundary scan cells accept test instructions and data, and scan out the test responses.

TRST The test reset (TRST) signal is an active low asynchronous reset for the TAP controller. The TRST signal does ***not*** initialize any system logic. For the 3B21D computer, the TRST signal is not on the boundary scan bus. The TRST input on each ASIC is connected to either an internal power reset or to a system power reset signal.

TDI The serial test data input (TDI) signal feeds test data to the device under test and is clocked into internal data or instruction registers on the rising edge of TCK.

TDO The serial test data output (TDO) signal feeds test data out of the device under test and changes state on the falling edge of TCK.

The 3B21D computer BS bus goes to all circuit packs except the power converters. Figure 5-9 shows that the BS bus consists of a primary bus, a secondary bus, and a growth bus. All boundary scan operations are controlled by the CC; however, additional circuitry is provided by the Input/Output Processor Power Switch (IOPPS) circuit pack (TN1820) for access to the secondary and growth buses.

Figure 5-8 Typical Boundary Scan (BS) Bus Functional Block Diagram

5.2.1.5.1 Circuit Pack Self-Identification

Circuit pack self-identification is done using the boundary scan bus for all circuit pack positions except for the IOP and the power converters. The power converters do not support self-identification. The KBN10 IOP circuit pack supports self-identification by accessing an internal memory via the dual serial channel.

The initial release of the 3B21D computer will not have a functioning circuit pack self-identification feature. The circuit pack self-identification circuits are designed into all new circuit packs; however, the components will not be installed on the circuit packs. The components consist of an EPROM, containing the self-identification data, and a boundary scan interface (test access port) to access the EPROM from the boundary scan bus.

The self-identification data is stored in a separate EPROM on all 3B21D computer circuit packs supporting circuit pack self-identification. The EPROM is programmed when the circuit pack is manufactured. In general, circuit pack self-identification is invoked by commands to the Maintenance Channel (MCH). The active CU instructs the MCH on the inactive CU to scan for self-identification data. The KBN10 IOP self-identification EPROM is read via the dual serial channel.

Figure 5-8 shows how the boundary scan bus is used for circuit pack self-identification. A shorting strap is used to maintain the continuity of the boundary scan bus when the self-identification feature is not used.

5.2.1.5.2 Primary Boundary Scan Bus

In Figure 5-9 , the primary chain begins at the CC circuit pack. The CC has 10 separate boundary scan links to the CC, Main Memory (MM), Direct Memory Access 0 (DMA 0), Direct Memory Access 1 (DMA 1), Utility Circuit (UC), Control Unit Power Switch (CUPS), Expansion Slot 0 (EX 0), Expansion Slot 1 (EX 1), Input/Output Processor Power Switch 0 (IOPPS 0), and the Input/Output Processor Power Switch 1 (IOPPS 1) circuit packs. The CC's TDI and TMS outputs are common to all circuit packs in the primary boundary scan chain, while the corresponding TCK output and TDO input are individually accessed one at a time by a multiplexer circuit in the CC.

The TAPs in the CC circuit pack are provided in sequence for the Self-Identification (SELF-ID), Store Data Interface (SDI), Special Registers 1 (SREG1), Store Address Interface (SAI), MicroSequencer (MSEQ), Data Manipulation Unit (DMU), Store Address Translator (SAT), Cache Controller (CAC), Special Registers 0 (SREG0) ASICs.

5.2.1.5.3 Secondary Boundary Scan Bus

The secondary bus is distributed from the IOPPS circuit pack. The four boundary scan leads (TCK, TMS, TDI, and TDO) are connected in parallel to 21 units in the Processor Unit backplane. Individual select leads are routed to each unit to activate a boundary scan port. The IOPPS and CC circuit packs are cross coupled on CU 0 and CU 1 to provide fault redundancy. Differential cables are used to span between backplanes. The IOPPS receives a processor on-line output from both CC circuit packs in this cross coupled arrangement. Its boundary scan circuitry will be under the control of the on-line Processor Unit.

5.2.1.5.4 Growth Boundary Scan Bus

The IOPPS circuit pack has an expansion port that allows a differential cable to be attached to the Processor Unit backplane and a Growth Unit backplane. This cable carries the four boundary scan signals plus an on-line signal. If an IOPPS is installed in a Growth Unit backplane, it will interface directly to the IOPPS in the Processor Unit backplane, under control of the on-line Processor Unit.

5.2.1.5.5 Circuit Pack Access

All circuit pack positions in a Processor Unit backplane and Growth Unit backplane have boundary scan access, except for the power converter positions. Access is shown in Figure 5-10 .

Although the boundary scan bus is provided to all PC community positions, in the Growth Unit and Processor Unit backplanes, certain circuit packs (TN74, TN75, TN82, TN983/UN583/UN597, and UN33D) ***do not*** have boundary scan capability. In addition, the boundary scan port is located on the fifth and sixth columns of the UN-type connectors. Therefore, a four-column TN-type circuit pack installed in a PC slot cannot use the boundary scan port unless a jumper cable is provided.

The boundary scan bus is routed to the DFCB position. The current DFCB circuit pack (TN2116) does not support boundary scan. The port is routed to pin fields not used by the TN2116, allowing any future circuit packs that may be installed here to support boundary scan, if desired.

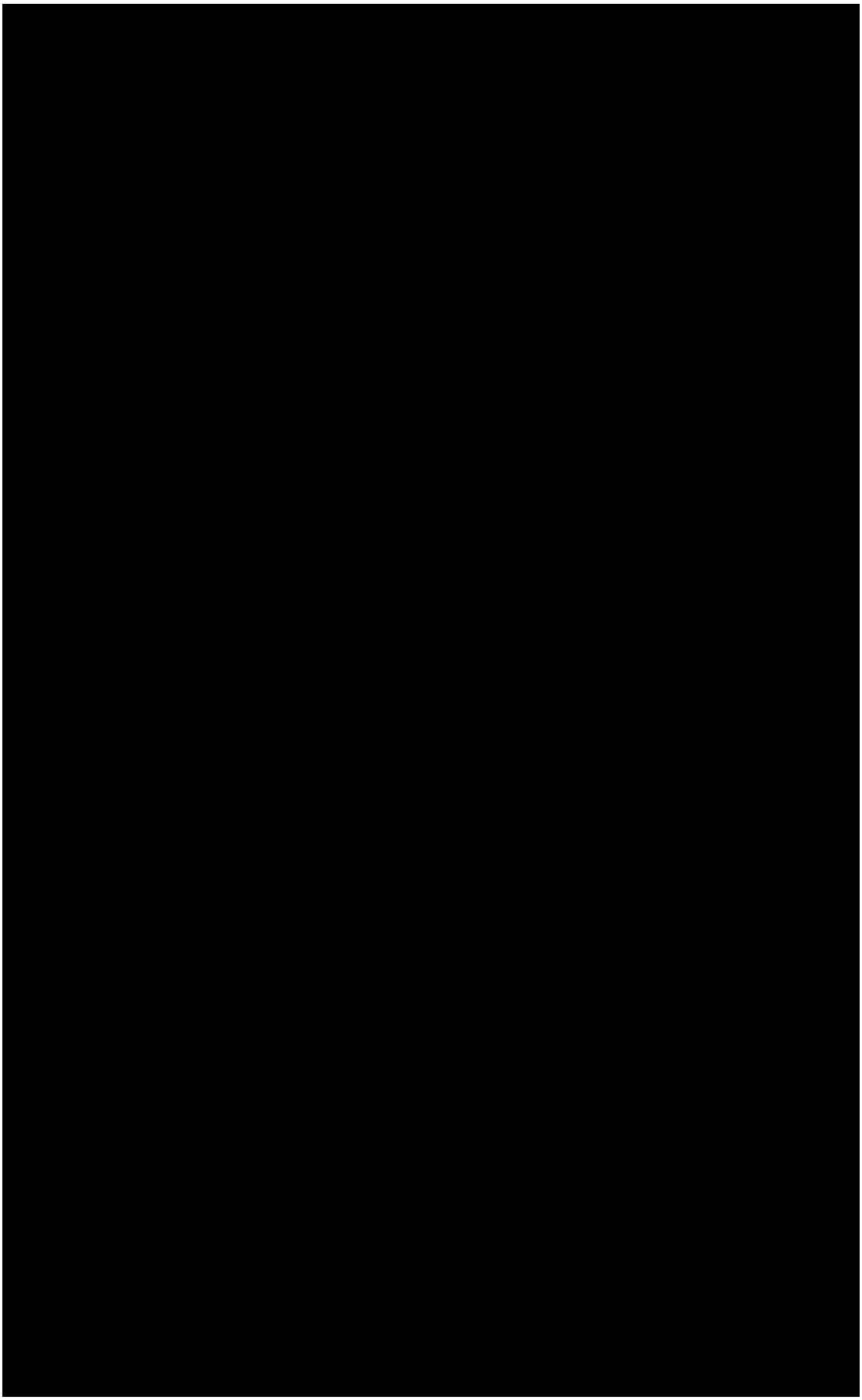


Figure 5-9 Boundary Scan (BS) Functional Block Diagram

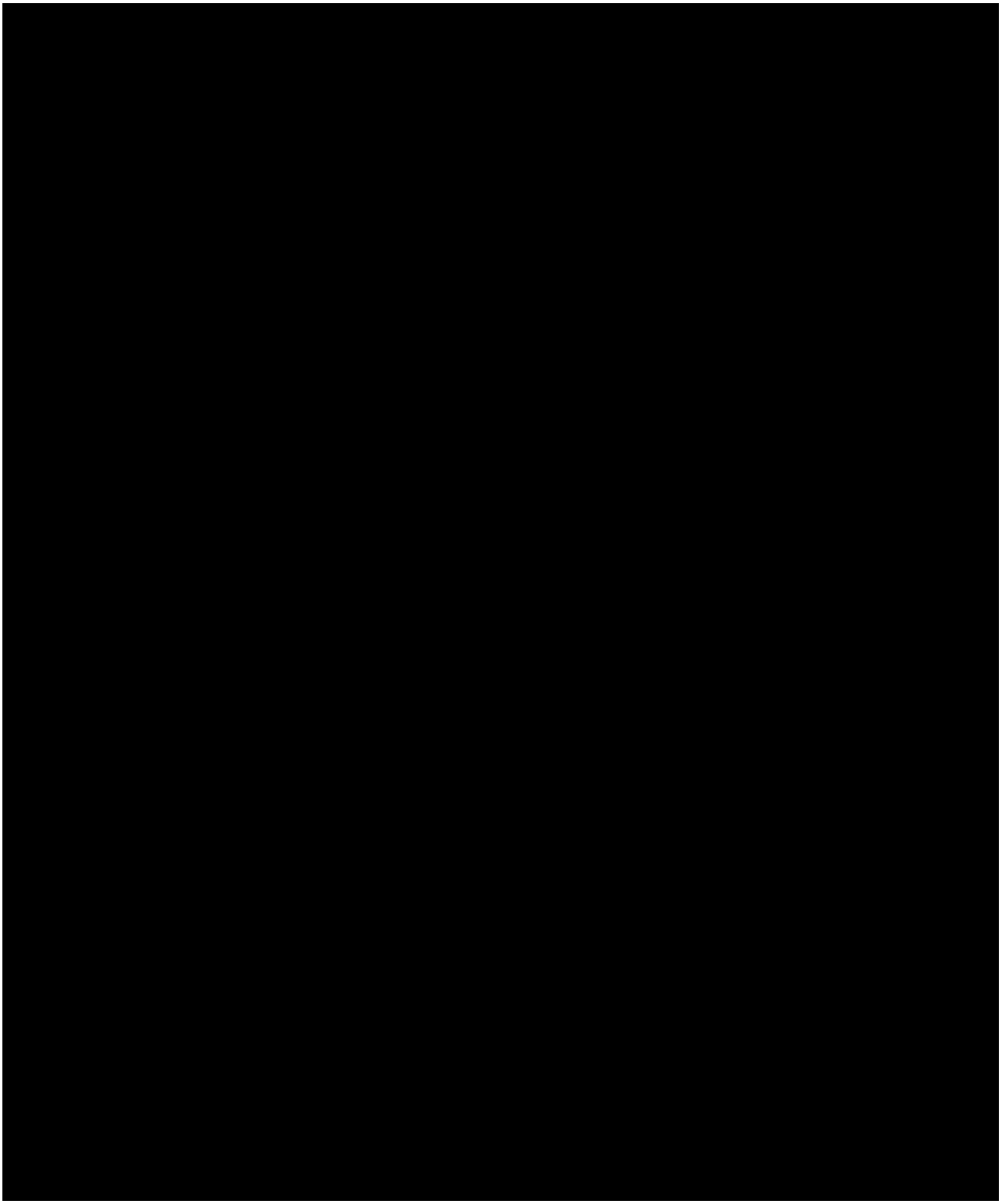


Figure 5-10 Boundary Scan Circuit Pack Access

5.2.2 CC Internal Buses

5.2.2.1 Bidirectional Gating Bus

The Bidirectional Gating Bus (BGB) is a 36-bit bus (32 data bits and 4 parity bits). The BGB is used to pass

data between the Central Control (CC) and various maintenance and diagnostic units. It is used to load and unload the Writable MicroStore (WMS). Table 5-7 summarizes the BGB. Figure 5-11 is a functional block diagram of the BGB.

The MLTS Interface and the CC are bus masters and have active control over the BGB. The MCH and UC are passive receivers on the bus.

Table 5-7 Bidirectional Gating Bus (BGB)

CATEGORY	SIGNAL	TYPE	DESCRIPTION	MLTS	CC	MCH	UC
DATA	BGB(31-00)1	Tristate	32 data bits, noninverted	I/O	I/O	I/O	I/O
	BGB(35-32)1	Bidirec-	4-byte even parity bits over 32	I/O	I/O	I/O	NC [a]
		tional	data bits				
CONTROL	MCHGBR0		Bus release request to Control Unit	I/O	IN	NC	NC
	MLTENO0		Enable WMS access by MLTS via BGB	I/O	IN	NC	NC
	MLTPP (2-0)		Clocking pulses for WMS address, low data, and high data	I/O	IN	NC	NC
	MLTRW0		WMS access direction by MLTS	I/O	IN	NC	NC
	HSR (23-16)		BGB sources, destinations, direction, and enable	NC	I/O	IN	IN
	PPR (21-16)		Pulse point register bits 21-16 for BGB accesses	NC	I/O	IN	IN

Notes:

a. NC = No Connection.

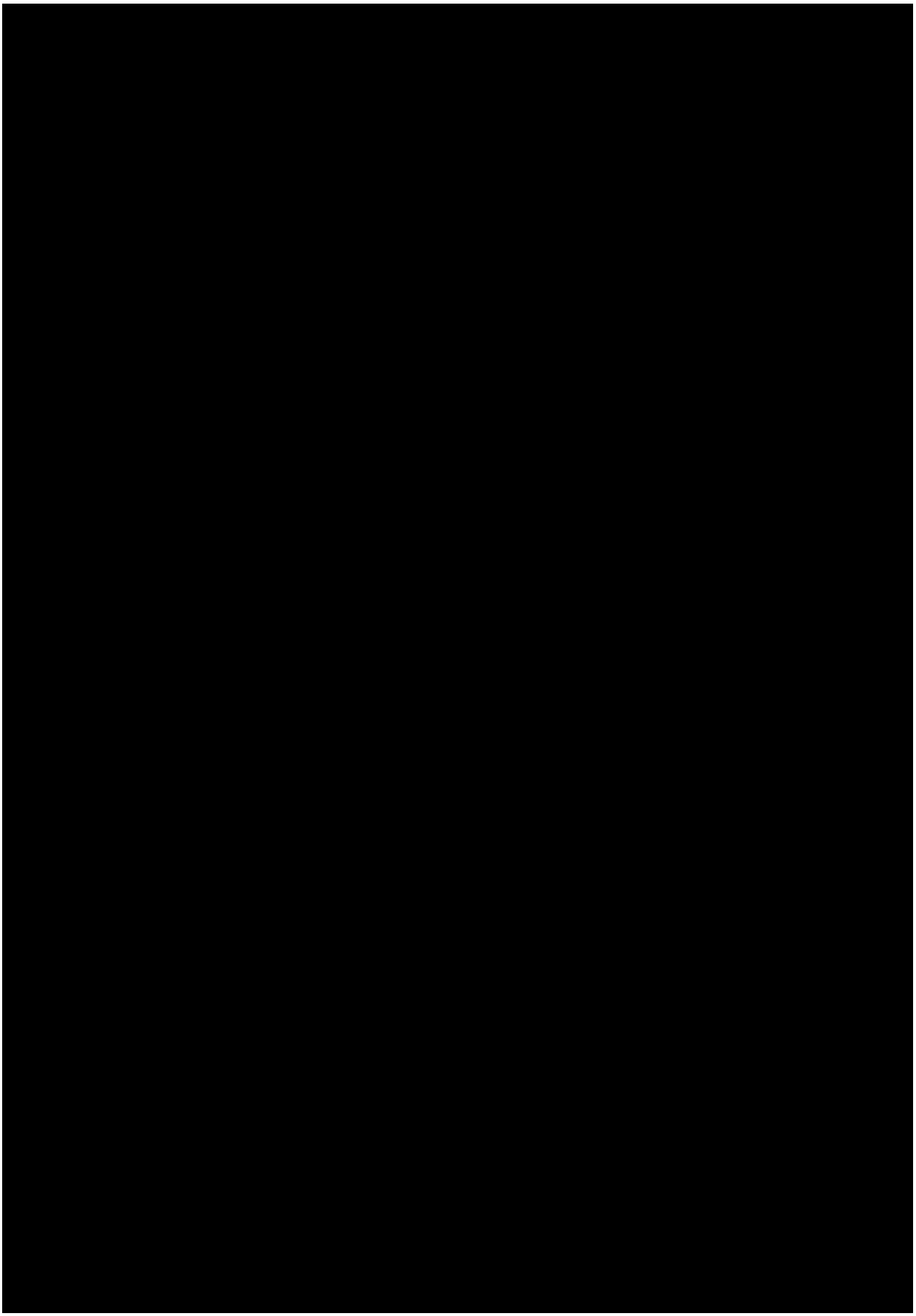


Figure 5-11 Bidirectional Gating Bus (BGB) Functional Block Diagram

5.2.2.2 MicroStore Bus Interface

The MicroInstruction Store (MIS) memory is accessed over the MicroStore (MS) bus by the MicroSequencer (MSEQ), Maintenance Channel (MCH), or by the Micro Level Test Set (MLTS) Interface. The MicroStore Address (MSA) bus is driven by only one of these devices at any instance. The MSEQ buffers the MSA data onto the RAM MicroStore Address (RMSA) bus when the RMSA enable signal from the MIS is asserted. The MIS disables the RMSA bus during BGB Static Random Access Memory (SRAM) accesses.

5.2.2.2.1 MicroStore Address Bus

The MicroStore Address (MSA) bus connects the MicroController (MC), MicroInstruction Store (MIS), Maintenance Channel (MCH), and the Micro Level Test Set (MLTS) Interface.

The MSA bus is 18-bits (16 address bits and 2 parity bits).

MSA bus bit 17 (MAS[17]1) is the even parity bit over MSA bits 15-08; MSA bus bit 16 (MAS[16]1) is the even parity bit over MSA bits 07-00. MS address parity is checked by the MSEQ on each memory access. The MSEQ compares the address parity bits against the MIR parity bit (MIR[63]1). A parity error asserts the MCPARE0 signal at the end of the current microinstruction cycle. The MCPARE0 (error register bit 1) signal remains asserted until the end of the next microinstruction cycle. The MIS does not check MSA parity.

5.2.2.2.2 MicroStore Data Bus

The MicroStore Data (MSD) bus connects the MicroController (MC), MicroInstruction Store (MIS), Maintenance Channel (MCH), and the Micro Level Test Set (MLTS) Interface.

The MSD bus is 64 bits (56 data bits and 8 parity bits). MSD bus bit 56 is the even parity bit over MSD bits 07-00. MSD bus bit 57 is the even parity bit over MSD bits 15-08. MSD bus bit 58 is the even parity bit over MSD bits 23-16. MSD bus bit 59 is the even parity bit over MSD bits 31-24. MSD bus bit 60 is the even parity bit over MSD bits 39-32. MSD bus bit 62 is the even parity bit over MSD bits 47-40. MSD bus bit 62 is the even parity bit over MSD bits 55-48. MSD bus bit 63 is the even parity bit over the command.

5.2.2.3 Source and Destination Buses

The Source (SRC) and Destination (DST) buses are 36-bit buses (32 data bits and 4 parity bits). The SRC and DST buses work together to pass data from a Central Control (CC) register through the Arithmetic Logic Unit (ALU) or ALU bypass logic to another CC register.

The SRC and DST buses are summarized in Table 5-8 . Figure 5-12 is a functional block diagram of the SRC and DST buses.

At the start of a MicroInstruction execution sequence, an SRC bus enable code is sent to gate a register onto the SRC bus. Depending on the MicroInstruction, the data either passes through the ALU or ALU bypass logic in the Data Manipulation Unit (DMU). The result is driven onto the DST bus by the DMU. At the end of the MicroInstruction, a DST clock is generated to gate the DST bus data into a CC register.

The MicroController (MC) sends two sets of six signals that the receiving ASICs use to generate Destination (DST) Clocks. Each set of six signals is used to clock half of a CC register and parity over the other half of the CC register. Each set consists of six signals, a 5-bit code, and a master clock signal. The 5-bit code is generated and sent by the MC at the start of the MicroInstruction execution. The 5-bit code represents the CC register to be clocked. The MC sends the master clock signal at the end of the MicroInstruction execution. The ASICs receive these signals, decode the 5-bit code, and combine the results with the master clock to control the CC registers in each ASIC. For some ASICs, this decoding is

done in the MSEQ and individual DST clocks are sent to the ASIC to save pins on the receiving ASIC.

Table 5-8 Source (SRC) and Destination (DST) Buses

CATEGORY	SIGNAL	TYPE	DESCRIPTION	MC	DMU	SREG	SDI	SAI	SAT
DATA	SRC(31-00)1	Tristate	32 data bits		I/O	OUT	OUT	OUT	OUT
	SRC(35-32)1	Tristate	4-byte even parity bits over 32 data bits		I/O	OUT	OUT	OUT	OUT
	DST(31-00)1	Tristate	32 data bits		OUT	IN	IN	IN	IN
	DST(35-32)1	Tristate	4-byte even parity bits over 32 data bits		OUT	IN	IN	IN	IN
DESTIN-ATION CLOCKS (DSTC)	DSTEN (4-0)A0	Unidirectional	Encoded value for register to be clocked by the master DST clock for set A	OUT	IN	IN	IN	IN	IN
	DSTMCA0	Unidirectional	Master DST clock for set A	OUT		IN	IN	IN	
	DSTEN (4-0)B0	Unidirectional	Encoded value for register to be clocked by the master DST clock for set B	OUT	IN	IN	IN	IN	IN
	DSTMCB0	Unidirectional	Master DST clock for set B	OUT	IN		IN	IN	
SOURCE BUS ENABLES	SRCEAA10	Unidirectional	Source enable 1 AA	OUT		IN			
	SRCEAA30	Unidirectional	Source enable 3 AA	OUT			IN		
	SRCEAB10	Unidirectional	Source enable 1 AB	OUT		IN			
	SRCEAB30	Unidirectional	Source enable 3 AB	OUT			IN		
	SRCEA000	Unidirectional	Source enable 00 A	OUT	IN				
	SRCEB000	Unidirectional	Source enable 00 B	OUT	IN				
	SRCEA010	Unidirectional	Source enable 01 A	OUT	IN				
	SRCEB010	Unidirectional	Source enable 01 B	OUT	IN				IN
	SRCEA200	Unidirectional	Source enable 20 A	OUT				IN	
	SRCEB200	Unidirectional	Source enable 20 B	OUT				IN	
	SRCEA210	Unidirectional	Source enable 21 A	OUT				IN	IN
	SRCEB210	Unidirectional	Source enable 21 B	OUT				IN	IN
	SRCEBA10	Unidirectional	Source enable 1 BA	OUT		IN			
	SRCEBA30	Unidirectional	Source enable 3 BA	OUT			IN		
	SRCEBB10	Unidirectional	Source enable 1 BB	OUT		IN			
	SRCEBB30	Unidirectional	Source enable 3 BB	OUT			IN		

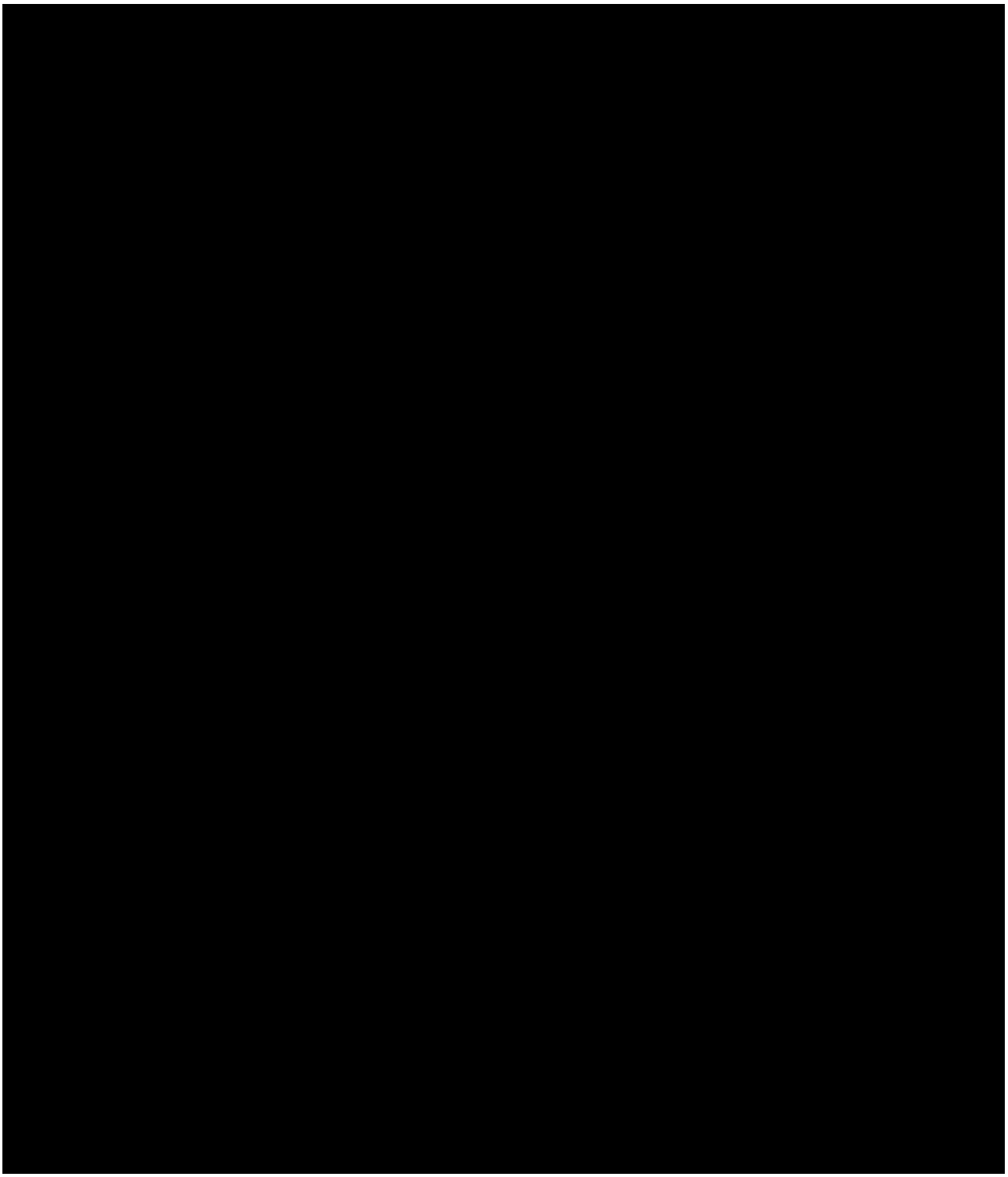


Figure 5-12 Source (SRC) and Destination (DST) Bus Functional Block Diagram

5.2.2.4 Maintenance (MTC) Bus

The Maintenance (MTC) bus is a 36-bit bus (32 data bits and 4 parity bits). The MTC bus is used primarily during maintenance and diagnostics operations for status information from the Central Control (CC) to the Maintenance Channel (MCH) and Micro Level Test Set (MLTS) Interface. The MTC bus is summarized in Table 5-9 . Figure 5-13 is a functional block diagram of the Maintenance (MTC) bus.

Table 5-9 Maintenance (MTC) Bus

CATEGORY	SIGNAL	TYPE	DESCRIPTION	MLTS	SREG	DMU	MCH
DATA	MTC(31-00)1	Tristate, bidirec-tional	32 data bits, noninverted	I/O	OUT	NC [a]	IN
	MTC(35-32)1	Tristate, bidirec-tional	4-byte even parity bits over 32 data bits	I/O	NC	OUT	IN
CONTROL	MTCEN(1-0)1	Open Collector	MTC bus source enable	I/O	IN	IN	OUT
	MTCSL(1-0)1	Open Collector	MTC bus source select	I/O	IN	IN	OUT

Notes:

a. NC = No Connection.

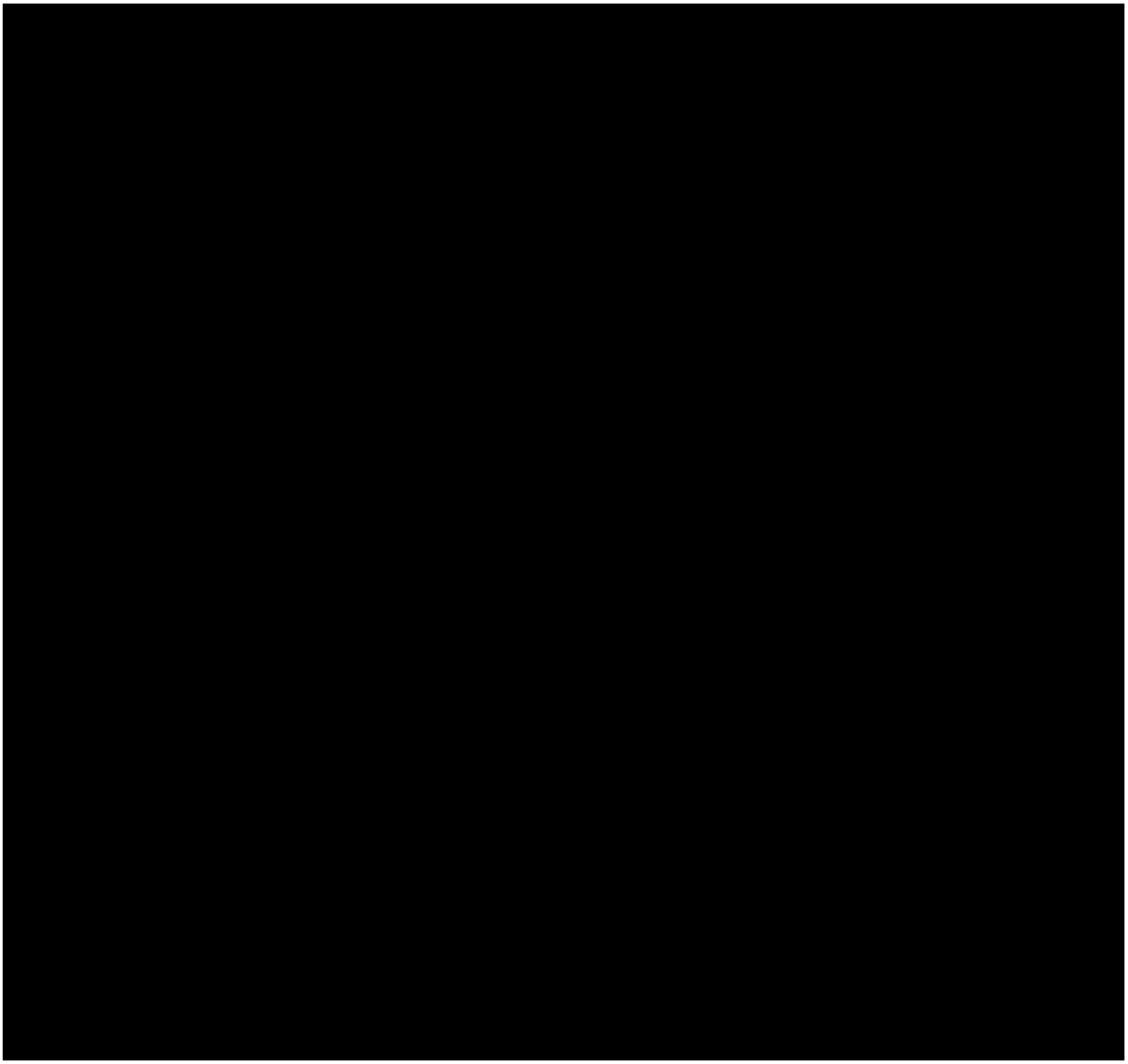


Figure 5-13 Maintenance (MTC) Bus Functional Block Diagram

5.2.2.5 Cache Memory Bus

The Cache Memory bus is used by the Store Address Interface (SAI) and Store Data Interface (SDI) to access the Cache Storage Unit (CSU). The CSU is discussed in "Cache Storage Unit (CSU)" in this

section. The Cache Memory bus consists of the Cache Data (CD) bus, the Cache Address (CA) bus, command leads, and control leads. Table 5-10 summarizes the cache memory bus.

Table 5-10 Cache Memory Bus

CATEGORY	SIGNAL	TYPE	DESCRIPTION	SAI	SDI	CSU
DATA	CD(31-00)1	Tristate	32 data bits, noninverted	NC [a]	I/O	I/O
	CDP(35-32)1	Bidirec- tional	4-byte even parity bits over 32 data bits	NC	I/O	I/O
ADDRESS	CA(27-00)1	Unidirec- tional	28 address bits	OUT	NC	IN
	CA(35-32)1		4-byte even parity bits over 32 data bits	OUT	NC	I/O
COMMAND	SWRT0	Unidirec- tional	Write 0/Read 1 command	OUT	NC	IN
	SCRI211		Access size byte	OUT	NC	IN
	SCRI221		Access size half word	OUT	NC	IN
	SQUAD0		Access size quad word	OUT	NC	IN
	SRMW0		Read-Modify-Write command	OUT	NC	IN
	SCRI311		Maintenance access command	OUT	NC	IN
CONTROL	SCRI161	Unidirec- tional	Access enable (SCR bit 16)	OUT	NC	IN
	SSR131		Cache bypass mode (from SREG)	NC	NC	IN
	CACHER0		Cache detected an error (to SREG)	NC	NC	OUT
	CAHIT0		Cache hit	IN	NC	OUT
	CARDY0		Cache is ready with data	IN	NC	OUT
	SCRI231		Subroutine stack access	OUT	NC	IN
	PMSCM0		Processor My-Store-Complete (from MASC)	NC	NC	IN
	THIT1		ATB Translation Hit and no ATB error from SAT	NC	NC	IN

Notes:

a. NC = No Connection.

5.2.2.5.1 Cache Data Bus

The Cache Data (CD) bus is a 36-bit, bidirectional bus (32 data bits and 4 parity bits) that conveys data among the Store Data Interface (SDI), Cache Storage Unit (CSU), and the Utility Circuit (UC).

5.2.2.5.2 Cache Address Bus

The Cache Address (CA) bus is a 32-bit, unidirectional bus (28 address bits and 4 parity bits) that conveys physical cache address information to the Cache Storage Unit (CSU) from the Store Address Interface (SAI).

5.2.3 MicroController (MC)

The MicroController (MC) consists of the MicroSequencer (MSEQ) ASIC, MicroInstruction Register (MIR), two programmable logic devices, and a 33-MHz oscillator.

The 33-MHz crystal-based oscillator is the primary CC timing source. The oscillator has a symmetry of 45 percent to 55 percent and an accuracy of 100 parts per million. Buffered versions of this primary CC timing source are distributed throughout the CC complex as various processor clock signals.

The MC fetches and decodes MicroInstructions from the CC MicroInstruction Store (MIS) and controls the resulting execution sequences among the other CC subsystems.

The MC operates from a 33-MHz oscillator and provides the following functions:

- Determines and generates the next MicroInstruction address with parity.
- Interprets and presents the current MicroInstruction in the MicroInstruction Register (MIR).

- Checks parity on each MicroInstruction fetched and the MicroInstruction address using the parity information stored with the data.
- Verifies the contents of the MIR by comparing its parity result with the MicroInstruction parity bits.
- Maintains an 8-word deep, wrap-around MicroInstruction return address stack.
- Provides wait logic in the event of a MicroInstruction and MAS operational conflict.
- Recognizes and processes MicroInterrupts.

5.2.4 MicroInstruction Store (MIS)

The MicroInstruction Store (MIS) provides a 4-K by 64-bit EPROM and a 32-K by 64-bit SRAM for CC microinstruction storage. Each MIS memory location contains microinstruction data with parity. The SRAM is read or written using the Bidirectional Gating Bus (BGB). Both the EPROM and the SRAM are read through the MicroStore (MS) bus interface.

The MIS provides the following functions:

- The EPROM and Control Interface Logic receive and decode 16 Main Store Address (MSA) bus bits (64 K words). The MSA bus is driven by the Maintenance Channel (MCH), the MicroSequencer (MSEQ), or by the Micro Level Test Set (MLTS).
- The SRAM and Control Interface Logic allows bidirectional data transfers, reads, and writes over the Bidirectional Gating Bus (BGB).
- The MIS generates data parity during BGB read transactions. The data written to the MIS SRAM includes microinstruction parity bits that are checked during instruction execution.
- The MIS operates in either the Normal mode or in the MicroCode Debug mode. In the Normal mode, the MSA EPROM address range is from 0x000 to 0xFFF; the RAM MicroStore Address (RMSA) and BGB SRAM address range is from 0x1000 to 0x8FFF. In the MicroCode Debug mode, the MSA and BGB bus SRAM address range is from 0x0000 to 0x7FFF and the EPROM cannot be accessed.

  This dual address feature is used to test software without programming EPROMs; instructions are executed only from SRAM. See Note.

NOTE: In the Normal mode, EPROM addressing, MSA bus logical addresses 0x000 to 0xFFF correspond to physical location 0x000 to 0xFFF. In the MicroCode Debug mode, the EPROM cannot be accessed.

In the Normal mode, SRAM addressing, the RMSA and BGB logical addresses 0x8000 to 0x8FFF correspond to physical addresses 0x0000 to 0x0FFF and logical addresses 0x1000 to 0x7FFF correspond to physical addresses 0x1000 to 0x7FFF. In the MicroCode Debug mode, SRAM addressing, the RMSA and BGB logical addresses 0x0000 to 0x7FFF correspond to physical addresses 0x0000 to 0x7FFF.

5.2.5 Store Data Interface (SDI)

The Store Data Interface (SDI) function is provided by a Store Interface (SI) ASIC operating in the SDI mode.

In the SDI mode, the SI ASIC provides a Store Data Register Pipeline (SDRP), partial Bidirectional Gating Register (BGR), partial Store Control Register (SCR), Store Sequencer (SSEQ), and SI Decoder.

The functions provided by the SDI are as follows:

- The SDR holds the source data during a write to Main Memory (MM) and is the destination of data for a MM read operation. The SDR can be loaded from the DST bus or from the MAS bus. Similarly, the SDR can be read from the SRC bus or placed onto the MAS bus.
- The Store Instruction Register (SIR) contains the next macroinstruction fetched from the MM. The SIR can also be accessed from the DST or SRC buses.
- The Instruction Buffer (IB) contains the current macroinstruction under execution by microcode. The IB can be loaded from the Halfword Multiplexer (HM) or DST bus. The content of the IB can also be gated to the SRC bus under MSEQ control.
- A partial Bidirectional Gating Register (BGR) is provided, bits 35-32, and 27-12. The BGR interfaces to the SRC and DST buses and provides the MicroController (MC) an interface to and from the BGB.
- Store Data Register (SDR) bits 31 and 15, SDR(31,15)1, are provided to the DMU. The DMU selectively multiplexes these signals to the MSEQ flag bits, VALU(A,B)(0,1)0.
- The SRC bus multiplexer is used to gate the SIR, SDR, IB, or HM to the SRC bus as selected.
- Store Clocks and Selects combine duplicated clocks with control functions for the SDI registers. These clocks and selects are generated by the Store Decoder.
- A Store Decoder provides outputs that are used to generate clocks and selects for the SDI register.
- The SSEQ coordinates activities between the SAT, CSU, and MM. During a memory access, intermediate results are checked and MM interactions with the CC are controlled by the SSEQ.
- The SDI provides the CC bidirectional data interface with the MASB, SD(35-32,27-00)1. The data transceivers are enabled by the MM arbiter. Transceiver direction is controlled by the SAI.
- Cache Data (CD) bus latches are provided for the UC.

5.2.6 Store Address Interface (SAI)

The Store Address Interface (SAI) function is provided by a Store Interface (SI) ASIC operating in the SAI mode.

In the SAI mode, the SI ASIC provides a Store Control Register (SCR), a Store Sequencer (SSEQ), a set of SI decoders, and the Store Address Update Registers (SAURs).

The functions provided by the SAI are as follows:

- The SAI provides a DST bus interface for loading the Program Address (PA) counter, Store Address Register (SAR), or SCR. The SAR is loaded with new information each time the MM is accessed. The SAI increments the SAR by one word during an autofetch cycle or the MC writes the address (virtual or physical) over the DST bus to the SAR. The SCR contains the control information for MM accesses.
- The SAI provides an SRC bus interface for gating the contents of the PA, SAR, or SCR to the SRC bus.
- The SAUR configuration allows either auto-increment or branch manipulations on both the PA and SAR. A parity predict circuit determines new parity for the incremented value.
- During CC MAS bus accesses, the SAI generates the MAS bus master control signals.
- The SAI provides an SSEQ to coordinate activities between the Store Address Translator (SAT), Store

Data Interface (SDI), Cache Storage Unit (CSU), and Main Memory (MM) during CC memory accesses. The SSEQ coordinates MM accesses.

5.2.7 Store Address Translator (SAT)

The Store Address Translator (SAT) function is provided by the SAT ASIC, a set of MASB buffers, and a set of Cache Address (CA) latches for the Utility Circuit (UC).

The SAT provides a logical address interface between the virtual byte segments of the Store Address Register (SAR), SAR(35-33,27-08)1, and the corresponding segments of the CA bus, CA(35-33,27-08)1. The least significant SAR byte, SAR(07-00)1, and its parity bit, SAR(33)1, are passed directly to the Cache Storage Unit (CSU) and/or to the MASB; no translation is necessary. SAR(10-08)1 are used with translated address bits (15-11)1 when generating the parity bit, CA(33)1, for CA bus byte 3, CA(15-08)1.

The SAT contains the Address Translation Buffers (ATBs). The ATBs are a two-way set associative memory that can be selectively read or written by microcode over the SRC or DST buses, respectively. ATB words or blocks are invalidated using Store Control Register (SCR) interface signals, SCR(29-27,10-00)1, from the SAI.

The SAR provides either a virtual or a physical address to the SAT for processing.

If the address is a virtual address, the SAT determines if a physical translation exists in either ATB set. If a physical translation exists, the SAT checks the read/write/execute permissions and generates a macrointerrupt if a violation occurs. If no violation is detected, the SAT generates a translated physical address with correct parity. This information is provided to the CSU and to the UC. If a physical translation does not exist, the SAT generates a microinterrupt to the MicroSequencer (MSEQ) so that microcode can access and load the proper page table entry to the appropriate ATB location.

If the address is a physical address, the ATBs are bypassed and the physical address flows through the SAT. If the ATBs are not bypassed and a physical address is provided, a macrointerrupt or a microinterrupt is likely to occur.

The following functions are performed by the SAT.

- The SAT accesses, controls, and maintains a two-way set associative ATB. Functions include hit detection logic, protection check logic, associative addressing logic, ATB write logic (including invalidation), ATB read logic, and error detection logic.
- The SAT receives a virtual address and determines if a physical translation exists in either ATB set.
- The SAT provides an SRC and DST bus interface for reading and writing selective ATB entries or locations.
- A CC address interface to the MASB, SA(35-32,27-00)1, is also provided. The address drivers are enabled by the bus arbiter on the Main Memory (MM).
- The SAT provides CA bus data latches for the UC.
- The SAT ASIC also provides the SREG, SSR(03-00)1, and parity logic for the Instruction Multiplexer (IM), Processor Status Word (PSW), Pulse Point Register (PPR), Channel Data Register (CDR), and the Central Control Input/Output Data (CCIOD).

5.2.8 Cache Storage Unit (CSU)

The Cache Storage Unit (CSU) function is provided by the Cache Controller (CAC) ASIC, six 32-K by 9-bit SRAM devices, three sets of tristate buffers for bus isolation, and one set of data transceivers for TAG

RAM maintenance.

The CSU increases CC performance by reducing the average main memory access time. It provides two distinct high-speed memory functions as follows:

- A direct-mapped data and instruction cache memory
- A high-speed interrupt stack memory.

The functions provided by the CSU are as follows:

- The CSU provides a 16-K word (64-K byte) direct-mapped data and instruction cache memory. The memory control logic recognizes, stores, and provides the contents of the most recently accessed MM locations.
- A write-through scheme is used to maintain cache and main memory coherency during write operations.
- A CSU memory read cycle completes within two clock cycles (60 nanoseconds), not including two cycles for address translation.
- The Cache Address (CA) bus parity, supplied by the SAT, is checked while the address is supplied to RAM. If parity is correct and the upper address segment matches the corresponding tag entry, a cache "hit" occurs and the corresponding data is written to or read from the cache data memory. During a write operation, the data is also written to MM. If the upper address segment and tag entry do not match, a cache "miss" occurs and the SAI accesses MM. During a read "miss," the MM data word is written into the cache data memory and the corresponding tag memory location is updated with the new address information. During a write "miss," no changes to cache memory are made.
- The cache is not affected during Direct Memory Access (DMA), Expansion (EX) circuit pack, and Other Store (OS) read operations. DMA, EX circuit pack, and OS write cycles require cache activity. DMA, EX, and OS write accesses to MM transfer one word or four words (a quad word) of data in sequence. During single word DMA, EX, and OS write operations, a cache tag memory location is indexed and its contents are compared with the MAS address. If a match occurs, a hit is generated and the cache tag is invalidated. During DMA and EX quad word write cycles, all four tag entries are checked for "hits." Any "hit" results in the invalidation of the corresponding tag entry.
- A cache bypass mode is provided that inhibits the hit detect logic during read cycles, thus forcing all accesses to MM. In the bypass mode, the cache is updated during all read operations and is invalidated on MM writes when a hit occurs. Write operations are not affected by the bypass mode and are performed the same as in normal operation. The cache is, therefore, kept current with MM when bypassed. All cache errors are disabled in the bypass mode.

  Bypass mode selection can change states only during initialization. This is because of the interrupt stack data stored in the cache data RAMs. The CSU may have the only copy of this data when the bypass is asserted.
- The CSU provides data during byte and halfword memory read accesses when a "hit" occurs. Byte and halfword memory write accesses result in a CSU update if a "hit" occurs.

5.2.9 Data Manipulation Unit (DMU)

The Data Manipulation Unit (DMU) function is provided by the DMU ASIC. The DMU ASIC contains data manipulation logic, Find-Low-Zero (FLZ) logic, Bypass ALU logic, temporary registers, firmware registers, and a partial Bidirectional Gating Register. The ASIC also provides parity checking and redundant logic for error detection and reporting.

The following functions are provided by the DMU:

- The data manipulation logic provides data rotation, bit masking, and an Arithmetic Logic Unit (ALU) that performs arithmetic and logical operations on 32-bit words. The Data Manipulation Logic receives data from the SRC bus and gates the resulting data to the DST bus.
- The FLZ logic identifies the bit position of the first zero found from the least significant end of the data word or source register.
- The Bypass ALU logic transfers data from the SRC bus to the DST bus without any manipulation.
- Sixteen Temporary 32-bit (one word) registers are provided for "scratch pad" storage.
- Sixteen Firmware 36-bit (one word, 32 data bits and 4 parity bits) registers are provided for instruction storage.
- A partial Bidirectional Gating Register (BGR), bits 31-28 and 11-00, is provided. The BGR interfaces with the SRC and DST buses and accommodates the MC interface to and from the BGB.
- Because parity cannot be passed through the ALU, the ALU function is duplicated for error detection. The output results from each unit are compared with each other to detect data discrepancies. (The DMU General and Q registers do not have parity protection.)
- The MTC bus parity generation logic is provided. Bus parity is calculated and transferred to the MCH as bits MTC(35-32)1.

5.2.10 Special Registers (SREG)

Most of the Special Register (SREG) function is provided by two SREG ASICs; one SREG ASIC operates as SREG0, the other ASIC operates as SREG1. Discrete logic provides the Special Register Programmable Array Logic (SRPAL). Special registers are 32-bit data storage elements used to hold hardware and software information. The least significant bits of the 32-bit registers (bits 15-00) are provided by SREG0. The most significant bits of the 32-bit registers (bits 31-16) are provided by SREG1.

The SREG subsystem provides the following functions:

- Hardware Status Register (HSR)
- Processor Status Word (PSW) register
- Pulse Point Register (PPR)
- System Status Register (SSR)
- Error Register (ER)
- Interrupt Mask (IM) register
- Interrupt Set (IS) register, also known as Interrupt Source
- Channel Data Register (CDR)
- Real-Time Clock (RTC)
- Timer Register (TR).

Figure 5-14 is a functional block diagram of the Special Registers.

The HSR, SSR, ER, and IS register are 32-bit registers. The PSW register, PPR, IM register, and CDR are 36-bit registers (32 data bits with 4 parity bits). Register interfaces are provided to the SRC, DST, CCIO, and MTC buses. The MTC bus is used to verify the proper operation of the processor.

The TR provides a Sanity Timer, Interrupt Timer (IT), and prescalars for the RTC and IT.

The CCIO backplane interface is provided. This interface includes data, address, and control signals.

5.2.10.1 Hardware Status Register (HSR)

The Hardware Status Register (HSR) contains control and status information. Bits 07-04 are read only, and bit 05 is wired to zero. All other bits can be written and read.

The HSR is loaded from the DST bus (except for the read-only bits), and read via the source bus and the destination bus.

The HSR bits are summarized in Table 5-11 .

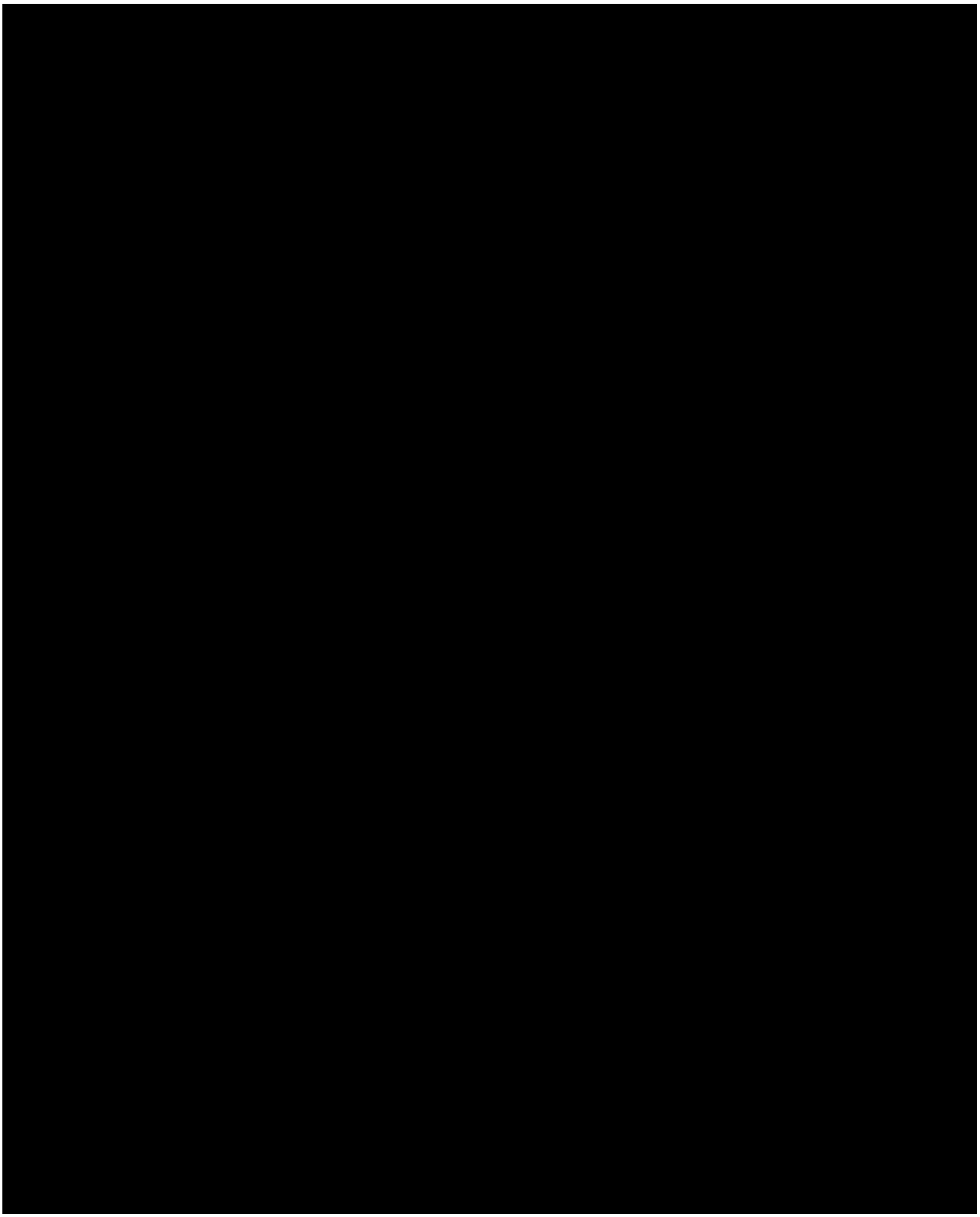


Figure 5-14 Special Registers Functional Block Diagram

Table 5-11 Hardware Status Register (HSR) Bit Layout

BIT	MEANING
03-00	The temporary flags Zero (bit 03), Overflow (bit 02), Sign (bit 01), and Carry (bit 00) are loaded as the result of a computation on the DMU.
07-04	Stores the status of I/O operations. Bits are channel all-seems-well (bit 04), not used (bit 05 wired to zero), no error

	in check sum (bit 06), and channel ready (bit 07). Normal state is all zeros. Read only.
09-08	Indicators (status bits) for the use of the backup MCH channel. Loadable via PPR points 14 (bit 08) and 15 (bit 09) in the mate processor, to disable the I/O in the processor in the event that the Maintenance Channel (MCH) fails. Cleared on power up.
15-10	The Channel Address Register independently loadable bits, which define the 3-out-of-6 address code for the CCIO data bus. Not writable by an HSR write, only by a CAR write.
23-16	Control the Bidirectional Gating Bus (BGB). Writable only by an HSRBGR write, not writable by an HSR write. Bits 22-20 select the source or destination device depending on the direction bit (bit 16) when the BGB is enabled by bit 23. Cleared on power up.
25-24	Write/read bits. Cleared on power up.
31-26	Decoded to form "maintenance states," which allow various hardware checks such as forcing parity errors. Cleared on power up.

Bits 30-26	MAINTENANCE STATE FUNCTION
0XXXX	No maintenance state active
1000X	RTC timing chain: Increment (PPR25), Reset (PPR24)
1001X	3-out-of-6 CCIO response check
1010X	Force bad parity (store control signal)
1011X	Force bad parity on Destination bus 35-32
1100X	Block parity, Arithmetic-logic unit clock
1101X	Force address translation buffer check circuit mismatch
1110X	Update circuit clock disable
1111X	Not used
XX001	Not used
XX011	Not used
XX101	Clear bit rotate error latch
XX111	Clear source parity error latch

5.2.10.2 Processor Status Word (PSW) Register

The Processor Status Word (PSW) register controls program function and records program status. The PSW outputs are read and tested by microcode.

The PSW is loaded via the DST bus (except for read-only bits) and is read via the SRC bus and the MTC bus.

The PSW register bits are summarized in Table 5-12 .

Table 5-12 Processor Status Word (PSW) Register Bit Layout

BIT	MEANING
03-00	The general flags Zero (Z□bit 03), Overflow (V□bit 02), Sign (N□bit 01), and Carry (C□bit 00), are loaded as the result of a computation on the DMU. A "1" is active.
06, 04	Interrupt stack (bit 06) and kernel stack (bit 04) active bits. Only one bit is active (set to a 1) at a time.
05	Spare.
07	Memory management on/off status. Memory management is on when bit 07 is 1.
08	Source is Primary base register when bit 08 is 0. Source is Secondary base register when bit 08 is 1.
09	Destination is Primary base register when bit 09 is 0. Destination is Secondary base register when bit 09 is 1.
12-10	Primary Segmentation Base Register.
15-13	Secondary Segmentation Base Register.
17-16	Reserved.
19-18	Reserved.
23-20	Set write PSW (bit 23), set I/O (bit 22), set maintenance (bit 21), and set execution (bit 20) privilege (permission) bits.
27-24	Interrupt execution level for fetching Interrupt Mask (IM) value.
31-28	Software controlled bits.

5.2.10.3 Pulse Point Register (PPR)

The Pulse Point Register (PPR) is used to generate control pulses. The PPR normally contains all zeros. An immediate data microinstruction asserts a bit via the destination register, and another immediate microinstruction then clears (negates) the bit. PPR points are used as miscellaneous control points under microinstruction control.

The PPR is read via the SRC bus. The PPR is cleared on power up.

The PPR bits and resulting actions when they are asserted are summarized in Table 5-13 .

Table 5-13 Pulse Point Register (PPR) Bit Layout

BIT	MEANING
10-00	CCIO channel command signals: Bit 00: Read channel data buffer Bit 01: Read channel status register Bit 02: Read channel interrupt state Bit 03: Read channel service request Bit 04: I/O interrupt acknowledge Bit 05: Channel error acknowledge Bit 06: Reserved for future use Bit 07: Idle channel sequencer Bit 08: Clear channel errors Bit 09: Write channel data buffer Bit 10: Write channel control/address register.
11	EAI channel interface.
13-12	Not used.
15-14	MCH channel backup 0 (bit 14) and 1 (bit 15). Allows a processor to disable I/O the mate processor without the use of the MCH. This operation also sets HSR bits 08 and 09 in the mate processor.
21-16	BGB control.
23-22	EAI Interface.
25-24	Timer maintenance.
26	Not used, can be used to trigger a logic analyzer.
28-27	I/O Read and response clocks.
29	Set (non-assert) Error Register (ER).
31-30	Clear SSR bit 30, enabling I/O. The pulse points must be pulsed in numerical order (bit 30 and then bit 31) to do this.

5.2.10.4 System Status Register (SSR)

The System Status Register (SSR) contains processor status information. The SSR is loaded via the DST bus (except for read-only bits) and is read via the SRC bus and the MTC bus. The SSR is asserted low; that is, an asserted bit reads back as a zero. The bits in the SSR are summarized in Table 5-14 .

Table 5-14 System Status Register (SSR) Bit Layout

BIT	MEANING
00	CU ID bit, wire strapped (read only) where 0 is CU 0 and 1 is CU 1.
01	Tape boot device indicator (read only) where 0 is LDFT from IOP and 1=LDFT from DFC.
02	Input Parameter Buffer in EAI available (ready) indicator (read only).
03	Request-out-of-service, reads the status of the ROS switch (read only).
05-04	Initialization sequence counter. The number of times that the initialization sequence has been entered unsuccessfully.
07-06	Force primary (bit 06) or secondary (bit 07) boot device.
08	Panel Interrupt (read only).
10-09	Force processor on-line (bit 10) or off-line (bit 09) (read only).
14-11	Disable/enable sanity timer (bit 11), panel interrupt (bit 12), cache (bit 13), and EAI Maintenance Reset Function (bit 14).
17-15	Signal Power Clear (bit 15), "This CC On-Line" (bit 16), and halt mode (bit 17).
18	Block IS interrupts when = 0 (Non-asserted on power up).
19	In update mode when = 0.
21-20	Isolate DMA (bit 20) and other CC (bit 21).
22	Isolate Expansion Slot.
23	Block hardware checks.
27-24	EAI bus.
29-28	Stop Processor (bit 28) and program/sanity timer (bit 29).
30	I/O disable.
31	Power switch state.

5.2.10.5 Error Register (ER)

The Error Register (ER) consists of 32 bits that are asserted by hardware faults. The ER is asserted low;

that is, asserted bits signifying errors are read as zeros. The ER is read via the SRC bus and the MTC bus. Most bits in the ER are individually clearable via the DST bus; however, some can only be cleared by resetting the circuitry that caused the error. The bits and the resulting actions when they are set are summarized in Table 5-15 .

Table 5-15 Error Register (ER) Bit Layout

BIT	ERROR	RESPONSE
00	Source bus error/Bit rotate parity error	Stop-and-switch
01	MSA or MSD parity error	Stop-and-switch
02	Clock Match error	Stop-and-switch
03	IB parity error	Stop-and-switch
04	ATB error	Stop-and-switch/microinterrupt
05	Cache error	Stop-and-switch
06	MASC error (read only)	Stop-and-switch
07	My MASC Timeout	Stop-and-switch/microinterrupt
08	My MASC data parity error	Microinterrupt
09	DMU error	Stop-and-switch
10	SAC parity error	Stop-and-switch
11	Invalid MCH Order	Other CC Interrupt
12	Other MASC error (read only)	Other CC Interrupt
13	Other Refresh parity error (read only)	Other CC Interrupt
14	Other MAS parity error	Other CC Interrupt
15	Other MASC Timeout	Other CC Interrupt/microinterrupt
16	Channel error (read only)	Hardware Error Interrupt
17	I/O Response error	Hardware Error Interrupt
18	I/O Address error	Hardware Error Interrupt
19	Parity Divert error	Hardware Error Interrupt
20	My Refresh parity error (read only)	Hardware Error Interrupt
21	ATB Protection violation	Microinterrupt/Software Error Interrupt
22	Cache byte/halfword write error	Microinterrupt/Memory Management Interrupt
23	Access Unequipped MAS	Microinterrupt/Software Error Interrupt
24	Access Unequipped Other MAS	Software Error Interrupt
25	Privileged Instruction violation	Microinterrupt/Software Error Interrupt
26	Store Addressing	Software Error Interrupt
27	Unused	
31-28	Source Bits 35-32, (source bus parity bits) are loaded when the BGR is specified as the destination.	NA

5.2.10.6 Interrupt Mask (IM) Register

The Interrupt Mask (IM) register bits are set or cleared by the microprogram via the DST bus. The IM is also read via the SRC bus. Each bit in the IM register corresponds to a bit in the Interrupt Set (IS) register. A bit set in the IM register prevents the recognition of the corresponding interrupt set in the IS register.

5.2.10.7 Interrupt Set (IS) Register

The 32 bits of the Interrupt Set (IS) register are set by external signals or interrupts. The IS register is also known as the Interrupt Source register. If a bit in the IS is set and the corresponding bit in the IM is cleared, an interrupt signal is generated. The IS is read via the SRC bus.

5.2.10.8 Channel Data Register (CDR)

The Channel Data Register (CDR) is used to interchange data between the SRC or DST bus and the CCIO bus. It is loaded from either the DST bus or the CCIO bus and is read from either the SRC bus or the CCIO bus. It is loaded from the DST bus as part of a move microinstruction and loaded from the CCIO bus in response to an I/O microinstruction. Thus, there are no interference problems; the CDR cannot be loaded from two different sources at the same time.

The CCIO bus is used to transmit data, address, and control signals between the Central Control (CC) and the main I/O channels. These I/O channels are the Direct Memory Access Controller (DMAC) and the Dual Serial Channels (DSCH).

5.2.10.9 Real-Time Clock (RTC)

The Real-Time Clock (RTC) is a 32-bit synchronous counter that is normally incremented at a 1-ms rate. The RTC is read via the SRC bus and is loaded via the DST bus. For diagnostics, the RTC can be single stepped using the HSR and PPR. The RTC is used as a systems clock when time, day, or date is required.

5.2.10.10 Timer Register (TR)

The timers are used as prescalars for the RTC, as interrupt timer prescalar, interrupt timer, and sanity timer. The timers are readable via the SRC bus and loadable via the DST bus. The timer bits and their functions are summarized in Table 5-16 .

Table 5-16 Timer Register (TR) Bit Layout

BIT	MEANING
07-00	Sanity timer, counts up a 50-ms signal (20 KHz) to 3.2- and 6.4-second signals. Cleared on power up and by software.
10-08	5-ms interrupt timer, divides a 1-ms signal by 5.
11	10-ms interrupt timer, divides the 5-ms interrupt output by 2.
14-12	25-ms interrupt timer, divides the 5-ms interrupt output by 5.
15	Sanity Timer prescalar. Cleared when bits 07-00 are loaded.
23-16	Real-Time Clock prescalar. These bits count down a 50-KHz signal (20 microseconds) to 1 KHz.
31-24	Interrupt Clock prescalar. These bits count down a 50-KHz signal (20 microseconds) to 1 KHz.

5.2.11 Maintenance Channel (MCH)

The Maintenance Channel (MCH) function is provided by an MCH ASIC, MCH microcode EPROMs, a set of bidirectional latches, a group of RS-422 transceivers, and a 20-MHz clock oscillator.

The Maintenance Channel provides diagnostic and maintenance access to the 3B21D computer. Both processors are linked via a serial interface called the Maintenance Channel Link (MCHL). The MCH circuitry sits at both ends of the MCHL. A processor sends commands and data to its MCH using the Bidirectional Gating Bus (BGB). In turn, this MCH can relay this information across the MCHL to the MCH in the other processor for processing. Therefore, an MCH can respond to master commands from its processor or to slave commands from the other processor. In a 3B21D computer running in duplex mode, the MCH in the active or on-line processor is called the master MCH; the MCH in the inactive or off-line side is called the slave MCH.

The following are the major MCH functions:

- The active processor stops and then uses the MCH to signal the other processor to switch on line (stop and switch). This can be performed by the processor logic directly activating the STPSW0 input to the master MCH. Alternately, it can be done under microprogram control where a command is sent to the MCH. In both cases, the MCH responds by sending an interrupt to the other MCH using the REQA signal in the MCHL. When the other MCH receives this interrupt, it activates its MRF0 output, which causes the other processor to go on-line. If the other processor is already on-line, and not disabled, the receiving MCH does not activate MRF0. Instead, an error is recorded.

- The MCH interfaces with the Boundary Scan Master (BSM) device on the KLW31 circuit pack. Both master and slave commands are available to access the BSM interface, allowing a processor to communicate with the BSM devices on both the active and inactive CUs. Diagnostics only accesses the inactive CU's BSM device. The BSM interface to the MCH uses an 8-bit parallel data bus.

- The active MCH interprets and executes commands received from the active processor via the BGB. Commands fall into the following categories:

  - Send data to the other processor's MCH.

  - Send commands to the other processor's MCH.

- Request data from the other processor's MCH.
- Request status from the other processor's MCH.
- Read and write onboard BSM control register.
- Read and write onboard BSM interface.
- Diagnostic commands to test internal MCH logic.

- The slave MCH can also execute the previously described commands. However, it is normally expected to execute slave commands received across the MCHL, as its processor is expected to be inactive. The slave commands include the following:
  - Read and report MTC bus data. The slave MCH can report on the SRC bus, DST bus, Hardware Status Register (HSR), Error Register (ER), Processor Status Word (PSW), and the System Status Register (SSR).
  - Read and write the BSM control register.
  - Read and write the BSM interface.
  - Read the BGB bus.
  - Clear the Error Register.
  - Reset Sanity Timer.
  - Set panel interrupt (PINT0).
  - Setup the backup MCH flipflop in CC.
  - Set or clear the STOP condition in the processor.
  - Read and write the MSA and MSD buses. In conjunction with the ability to step the microsequencer, this capability allows microcode to be loaded into the Writable MicroStore (WMS) and to execute it one microcommand at a time.

Figure 5-15 is a functional block diagram of the MCH. Table 5-17 summarizes the MCH signals. The internal logic of the MCH is under microprogram control. Although two 8-K by 8-bit EPROMs contain the MCH microcode, the MCH only uses 2 K of address space. The differential signals in the MCHL are converted by the RS-422 circuitry to logic signals for the MCH. The 64-bit MSD bus is multiplexed and requires the external registers. The BSM interface allows the MCH to control BIST and boundary scan activities. Note that the MCH boundary scan port is not used.

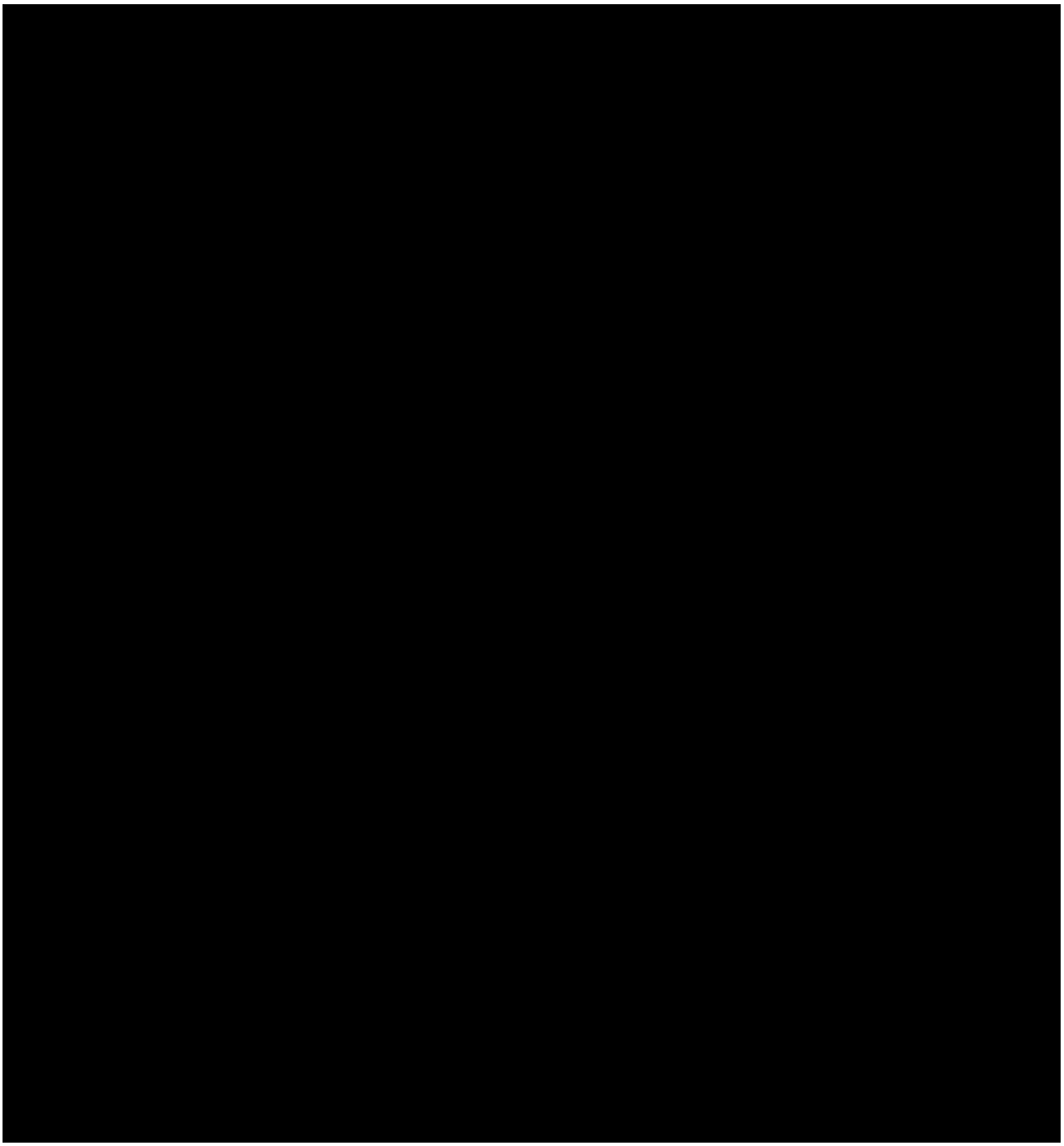


Figure 5-15 Maintenance Channel (MCH) Functional Block Diagram

Table 5-17 Maintenance Channel (MCH) Signals

CATEGORY	SIGNAL	TYPE	DIRECTION	DESCRIPTION
MICROSTORE BUS (MSA, MSB)	MSD(63-00)1	Tristate	I/O	MicroStore Data bus, multiplexed 32 data bits.
	MCHMDR0	Open Collector	OUT	MCH MSD Release, directs outside systems to cease driving the MSD.
	MSDWR1		OUT	MSD external latch write.
	MSDHCLK0		OUT	Clocks MCH MSD output data to high-order external latch.
	MSDLCLK0		OUT	Clocks MCH MSD output data to low order external latch.
	MSDHDR0		OUT	MSD external high order latch drive enable.
	MSDLDR0		OUT	MSD external low order latch drive enable.

	MSA(17-00)	Tristate	I/O	MicroStore Address bus, 18-bit address bus.
	MCHMAR0	Open Collector	OUT	MCH MSA Release, directs outside systems to cease driving the MSA.
	MSDV0	Open Collector	OUT	MicroStore Data Valid, indicates that the MCH is driving the MSD.
MAINTENANCE CHANNEL (MCH) BUS	MTC(35-00)1		IN	Maintenance Bus, 32 data bits and 4 parity bits. Monitors the SSR, ER, HSR, PSW register, SRC bus, and DST bus.
	MCHMSR0	Open Collector	OUT	MCH MTC Release, directs outside systems to cease driving the MTC bus.
	MTCEN00	Open Collector	OUT	Maintenance Channel Bus Enable 0 Selects the processor register to be via the MTC bus.
	MTCEN10	Open Collector	OUT	Maintenance Channel Bus Enable 1 Selects the processor register to be via the MTC bus.
	MTCSL01	Open Collector	OUT	Maintenance Channel Bus Select 0 Selects the processor register to be via the MTC bus.
	MTCSL11	Open Collector	OUT	Maintenance Channel Bus Select 1. Selects the processor register to be via the MTC bus.
BIDIRECTIONAL GATING BUS (BGB)	BGB(35-00)1	Tristate	I/O	Bidirectional Gating Bus, 36-bit data bus carries control communications between the MCH and the processor.
	BGBEN20		IN	BGB Enable In.
	BGBPP00		IN	BGB Pulse Point 0 from SREG directs MCH to execute command in the Master Command Register.
	BGBPP01		IN	BGB Pulse Point 1 from SREG initializes MCH Microsequencer.
	BGBPP02		IN	BGB Pulse Point 2 from SREG clocks data into Master Command Register.
	BGBPP03		IN	BGB Pulse Point 3 from SREG clocks data into MCHB.
	BGBPP04		IN	BGB Pulse Point 4 from SREG clears Panel Interrupt.
	BGBRS00		IN	BGB Register Select from SREG, 0 for MCHB, 1 for Master Status.
	BGBRW0		IN	BGB Read/Write control from SREG, 0 for read, 1 for write.
MAINTENANCE CHANNEL LINK (MCHL)	DAHAP	RS-422	I/O	Serial link high-order bits, positive phase.
	DAHAN	RS-422	I/O	Serial link high-order bits, negative phase.
	ALAP	RS-422	I/O	Serial link low-order bits, positive phase.
	DALAN	RS-422	I/O	Serial link low-order bits, negative phase.
	XCKAP	RS-422	IN	Serial link clock input, positive phase.
	XCKAN	RS-422	IN	Serial link clock input, negative phase.
	CLKAP	RS-422	OUT	Serial link clock output, positive phase.
	CLKAN	RS-422	OUT	Serial link clock output, negative phase.
	TXEN0		OUT	Enable external DAHA and DALA RS-422 drivers.
	RXEN0		OUT	Enable external DAHA and DALA RS-422 receivers.
	REQAP	RS-422	I/O	Link stop and switch interrupt, positive phase.
	REQAN	RS-422	I/O	Link stop and switch interrupt, negative phase.
BOUNDARY SCAN TEST ACCESS PORT	TDO		OUT	Test Data Output.
	TDI		IN	Test Data Input.
	TMS		I/O	Test Mode Selection.
	TCK		I/O	Test Clock.
	TRST		IN	Test Reset. TRST is not connected to the boundary scan bus. TRST is connected to either an internal power reset or to a system power reset signal.
MISCELLANEOUS	MCHMCD(19-00)1		IN	MCH microcode ROM data input.

	MCHMCA(9-0)1		OUT	MCH microcode ROM address output.
	STPSET0	Open Collector	OUT	Set Central Control (CC) stop. Pulsed as a result of a slave command.
	STPCLR0	Open Collector	OUT	Clear Central Control (CC) stop. Pulsed as a result of a slave command.
	CLRER0	Open Collector	OUT	Clear system error register. Pulsed as a result of a slave command.
	PTRST0	Open Collector	OUT	Program (sanity) Timer Reset.
	TRIST0		IN	Tristate MCH outputs.
MISC. (Contd)	TESTOUT		OUT	Used in MCH ASIC component parametric test.
	STOP0		IN	Stop Central Control (CC) sequencing (from MLTS).
	STPSW0		IN	Stop and switch from local SREG.
	PINT0	Open Collector	OUT	Panel Interrupt, set on receipt of particular slave command, interrupts CC.
	MDISA0	Open Collector	OUT	To Special Register (SREG). Pulsed as a result of slave command.
	MDISB0	Open Collector	OUT	To Special Register (SREG). Pulsed as a result of slave command.
	SCLK201		IN	Maintenance Channel clock input (20 MHz).
	PONL0		IN	Processor On-Line (from SREG).
	DISAB0		IN	Disable (from SREG).
	MLTMCR0		IN	Micro Level Test Set to Maintenance Channel bus release signal.
	MLTMCI0		IN	Micro Level Test Set to Maintenance Channel inhibit signal.
	MCHINT0		IN	Maintenance Channel Initialize (from SREG).
	MCHER0	Open Collector	OUT	Maintenance Channel Error. Pulsed on inappropriate slave commands or on inappropriate MCHL interrupt signals.
	MRF0	Open Collector	OUT	Maintenance Reset Function, commands inactive processor to become active. Pulsed in response to MCHL interrupt signal.
	STEP0	Open Collector	OUT	Single Step (pulsed under microprogram control).
BOUNDARY SCAN MASTER (BSM) PORT	BSMDATA		I/O	BSM Port serial data to/from the BSM.
	BSMDS		OUT	BSM Port Strobe paces serial data to/from the BSM.
	BSMADRS(1-0)		OUT	BSM Port Address, controlled by the BSM Port control and status register.
	BSMRD		OUT	BSM Port Read.
	BSMINT		IN	BSM Port Interrupt.
	BSMSELCLK		OUT	Boundary scan chain selector clock.
	BSMTCLK		OUT	BSM Timing Clock references supplied to the BSM by the MCH.

5.2.11.1 MCH BGB Interface

The BGB interface is used by the processor to communicate with the MCH. Associated with this data bus are control signals that are driven by bits in the Hardware Status Register (HSR) and Pulse Point Register (PPR). Table 5-18 summarizes these controls. All signals are asserted low.

Therefore, MCH transactions are executed by setting up the Hardware Status Register for the proper read/write condition, and then asserting the appropriate pulse points to transfer the data on the BGB bus.

Table 5-18 Maintenance Channel (MCH) Control Signals

MCH NAME	SYSTEM NAME	FUNCTION
BGBPP00	PPR 0	Executes MCH Command.

BGBPP10	PPR 1	Resets MCH microsequencer.
BGBPP20	PPR 2	Writes MCH Master Command.
BGBPP30	PPR 3	Writes Data to MCH.
BGBPP40	PPR 4	Clears Panel Interrupt.
BGBRW0	HSR16	1 to read BGB, 0 to write BGB.
BGBRS00	HSR17	1 to read status, 0 to read data.
BGBEN0	BGBEN20	Enables previous commands. Active when HSR[23-20] = 1010.

5.2.11.2 MCH Commands

MCH commands are placed on the BGB bus and the write master command pulse point is asserted. Then the execute command pulse point must follow. The master command is a 16-bit word written to the 36-bit BGB bus. BGB bits 35-16 are ignored. Most commands will take at least 40 MCH clock cycles to execute. If a command results in a slave transaction, execution time can take 140 to 200 cycles. The MCH has a bit in an internal status register that is zero while the MCH is executing a command. This register can be read at any time to determine the MCH status; that is, to see if the MCH is idle.

5.2.11.3 MCH Data

MCH data is read and written on the 36-bit BGB bus. This data can consist of internal status register information, register data sent from the other processor, microstore addresses and data, and BSM data.

5.2.11.4 MCH Microsequencer

The MCH microsequencer uses a 32-bit command word. It has the capability to branch anywhere in its 2-K address space. Although the MTC bus is read only, the MCH microsequencer can move data between the major MCH external bus interfaces, MSD, MSA, MTC, BGB, and BSM. An internal accumulator with increment, decrement, byte, and bit rotation capability is provided.

5.2.11.5 BSM Interface

The MCH uses the BSM interface to access the BSM device and the KLW31 boundary scan select logic. The internal MCH BSM control register is programmed to allow the MCH to access either the BSM or the BSM select logic.

5.2.11.6 Stop and Switch

Asserting the STPSW0 input to the MCH ASIC causes it to send an interrupt on the MCHL link. The same result can be achieved by entering the "sendsw" master command. When the STPSW0 approach is used, the resulting REQAOUT interrupt from the MCH is used with the STPSW0 signal to automatically set the STOP flipflop. When a master command is used, the processor must stop itself.

5.2.11.7 Maintenance Reset Function

On receipt of a stop and switch interrupt, the MCH ASIC activates the Maintenance Reset Function (MRF0) output. This initiates a reset on the previously inactive processor. If the MCH senses that the processor is already on-line, and not disabled, then it will NOT assert MRF0. Instead, a maintenance channel error is indicated by asserting the MCHER0 output.

5.2.12 Emergency Action Interface (EAI)

The Emergency Action Interface (EAI) function provides the following capabilities:

- Manual recovery intervention
- Central Control (CC) status monitoring
- Normal processor control.

The Emergency Action Interface (EAI) function provides a means of manually forcing certain system recovery configurations if the automatic system error recovery is unsuccessful. The EAI is accessed via the Maintenance Terminal Controller (MTTYC) through the maintenance terminal. Emergency action requests can also be entered remotely via the Switching Control Center (SCC). The EAI also captures the Processor Recovery Messages (PRMs) and forwards them to the MTTYC.

The operations of the EAI are categorized as follows:

- ***MTTYC Initiated Operations:*** The EAI receives and decodes a serial message from the MTTYC and carries out the requested action. The action might involve changing the state of the emergency action nodes, initializing the EAI, initializing the CC, or returning a status message.
- ***CC Initiated Operations:*** The EAI responds to stimuli from the CC by accepting data, performing maintenance operations, or signaling the MTTYC that a significant system event has occurred.
- ***EAI Initiated Operations:*** The EAI can signal the MTTYC that an EAI internal audit has failed.

Table 5-19 summarizes the EAI force functions. Table 5-20 summarizes the EAI initialization functions. Table 5-21 summarizes the EAI Pulse Point Latch Clear Register. Table 5-22 summarizes the 3B21 computer EAI normal pulse point functions. Table 5-23 summarizes the 3B21D computer EAI maintenance pulse point functions Table 5-24 summarizes the 3B21D computer EAI maintenance commands. Note that the 3B21D computer uses both the 3B20D computer and 3B21D computer maintenance pulse point functions.

The Emergency Action Interface function on the Central Control (CC) circuit pack is provided by a microprocessor-based circuit with an 8-MHz clock. Figure 5-16 is a functional block diagram of the EAI.

Table 5-19 EAI Force Functions

FUNCTION	DESCRIPTION
Force CC On-Line (FONL)	Forces the Central Control (CC) associated with the EAI to remain the on-line CC, regardless of attempts by software to switch the CCs. The mate CC will concurrently be forced off-line (FOFL).
Force Boot Device Primary (FBDP)	Forces subsequent system boot information to be taken from the primary boot device, regardless of software or firmware attempts to use the secondary device.
Force Boot Device Secondary (FBDS)	Forces subsequent system boot information to be taken from the secondary boot device, regardless of software or firmware attempts to use the secondary device.
Disable Sanity Timer (DTIM)	Forces the associated CC sanity timer to be disabled, thus inhibiting subsequent switches if software execution is abnormal.

Table 5-20 EAI Initialization Functions

FUNCTION	DESCRIPTION
Clear EAI (CLREAI)	Causes the outputs from the EAI to the CC to be reset, and clears the EAI RAM associated with the initialization parameter (IP) buffer.
EAI Maintenance Reset Function (EAIMRF)	Forces the associated CC to initialize (MRF).
Input Initialization Parameter (INIP)	Transfers 64 bits of 3B21D computer system initialization parameter (IP) from the MTTYC to the EAI, where it is buffered in RAM.
Output Initialization Parameter (OUTIP)	Transfers the contents of the EAI IP buffer to the MTTYC for verification.
Output EAI Status (OUTSTAT)	Transfers a status message to the MTTYC.
Output PRM (OUTPRM)	Transfers the 64-bit Processor Recovery Message (PRM) output buffer to the MTTYC.

Figure 5-16 Emergency Action Interface (EAI) Functional Block Diagram

5.2.12.1 EAI Microprocessor

The EAI microprocessor is a 16-bit processor. The 16-bit, time-multiplexed address/data bus (AD) carries address and data to all functional areas of the EAI. The processor contains programmable chip-select generation logic that is used to implement the EAI address map. Each functional area (EPROM, RAM, Port A, Port B, Error Register, and others) is assigned an initial address that is used to access a particular EAI device.

5.2.12.2 EAI Controller

The EAI Controller contains the following functions:

Pulse Point/Interrupt Register

A low-going pulse on a pulse point lead (PP110, PP220, or PP230) causes an interrupt to the microprocessor. The Pulse Point/Interrupt Register latches these signals so that the identity of the

pulse causing the interrupt can be determined by reading Port A. The Pulse Point Latch Clear Register is defined in Table 5-21 . Table 5-22 summarizes the 3B21D computer EAI normal pulse point functions. Table 5-23 summarizes the 3B21D computer EAI maintenance pulse point functions. Table 5-24 summarizes the 3B21D computer EAI maintenance commands.

Diagnostic Data Register (DDR)

The DDR is a 4-bit register. The state of the Diagnostic/Recover Data bus bits 03-00 is gated to the DDR by pulse point PP110, PP220, or PP230. Table 5-25 defines the DDR.

CC Status

CC status signals are read via EAI input Port A via the Address/Data (AD) bus bits 08-00. EAI Port A is defined in Table 5-26 .

Initialization Parameter (IP)/Processor Recovery Message (PRM) Buffer The CC sends a 64-bit Processor Recover Message (PRM) to the EAI or reads the Initialization Parameter (IP) from the EAI during various phases of initialization. The PRM is transferred over the low 4-bits of the CC System Status Register to the Diagnostic/Recovery Data (DRD) bus under the control of pulse points PP110, PP220, and PP230. The MTTYC writes the IP at initialization. The CC reads the IP from the EAI SRAM. These messages are transferred as sixteen 4-bit nibbles.

Emergency Action Nodes

The EAI controller drives the Emergency Action Nodes to control the Central Control (CC). The nodes are written via EAI output Port B via the Address/Data (AD) bus bits 11-00. The nodes can be read by the EAI microprocessor for diagnostic and audit operations. EAI Port B is defined in Table 5-27 .

EAI Display Control

The EAI controller drives the EAI indicators located on the CC circuit pack faceplate.

EAI Error Register

The EAI Error Register is defined in Table 5-28 .

Table 5-21 EAI Pulse Point Latch Clear Register

AD BUS BIT	DEFINITION
7-0	The latch is cleared by a read operation. Bit values are "don't cares."

Table 5-22 EAI Normal Pulse Point Functions

3B21D COMPUTER NORMAL EAI PULSE-POINT INTERRUPTS			
PPR23	PPR22	PPR11	FUNCTION
0	0	0	No Interrupt.
0	1	0	Reads the DRD and stores the four bits in the buffer at the location pointed to by the Array Pointer.
1	0	0	Causes the DRD to be used as the new Array Pointer and places the nibble of the IP buffer on the PB as indicated by the Array Pointer.
1	1	0	Indicates the start of a 3B21D computer initialization sequence.
0	0	1	Resets the EAI microprocessor and hardware, then begins power-on firmware initialization sequence.
0	1	1	Halts the EAI microprocessor and isolates the PB, FONL, FOFL, DTIM, EAEN, EAIMRF, FBDP, and FBDS signals from the CC until a CC power-up or a EAI pulse point reset (PPR23=0, PPR22=0, PPR11=1) occurs.
1	0	1	Clears Error Register nibbles 0 and 1.
1	1	1	Causes the DRD to be used as the new Error Array Pointer and places the nibble of the Error Register on the PB as indicated by the Error Array Pointer.

Table 5-23 EAI Maintenance Pulse Point Functions

3B21D COMPUTER EAI MAINTENANCE PULSE-POINT INTERRUPTS					
PPR23	PPR22	PPR11	OPCODE	MNEMONIC	FUNCTION

			(SSR03-00)		
0	0	1	-	RESET	Resets EAI microprocessor and hardware, then begins power-on firmware initialization sequence.
0	1	1	-	EAHLT	Halts the EAI microprocessor and isolates the PB, FOML, FOFL, DTIM, EAEN, EAIMRF, FBDP, and FBDS signals from the CC until a power-up or a EAI pulse point reset (PPR23=0, PPR22=0, and PPR11=1) occurs.
1	0	1	-	WEREG	Reads the DRD and stores the four bits in the Error Register at the location pointed to by the Error Array Pointer.
1	1	1	0-1	REREG	Causes the DRD to be used as the new Error Array Pointer and places the nibble of the Error Register on the PB as indicated by the Error Array Pointer.
1	1	1	2-3	NOP	No Operation.
1	1	1	4	PARERR	Forces an SRAM Parity Error to set bit 0 in the EAI Error Register.
1	1	1	5	SANITY	Causes the firmware to invoke the sanity timer diagnostic self-test.
1	1	1	6	QFLUSH	Flushes any PRMs that are held in the EAI PRM queues and resets the queue pointers.
1	1	1	7-15	NOP	No Operation.

Table 5-24 EAI Maintenance Commands

3B21D COMPUTER EAI MAINTENANCE COMMANDS				
a		OPCODE b	MNEMONIC	FUNCTION
PPR23	PPR22	(SSR03-00)		
0	1	0	NOP	No Operation
0	1	1	FBDP	Force Boot Device Primary
0	1	2	FBDS	Force Boot Device Secondary
0	1	3	FONL	Force On-Line
0	1	4	FOFL	Force Off-Line
0	1	5	DTIM	Disable Timer
0	1	6	EAIMRF	EAI Initiated Restart
0	1	7	ENBL	Light EAI Enable Lamp
0	1	8	SETASW	Set ASW Bit
0	1	9	MINIT	Clear Effects of Maintenance Operations
0	1	10	MVOB00	Move PRM 0 Input Buffer to IP Buffer
0	1	11	MVOB01	Move PRM 0 Output Buffer to IP Buffer
0	1	12	MVOB10	Move PRM 1 Input Buffer to IP Buffer
0	1	13	MVOB11	Move PRM 1 Output Buffer to IP Buffer
0	1	14	MVINST	Move Input Status to IP Buffer
0	1	15	MVOUTST	Move Output Status to IP Buffer
1	0	0-15	EAIREAD	Read IP Buffer Nibbles 0-15
1	1	0	NOP	No Operation
1	1	1	CLRASW	Clear ASW Bit and Reset DUART
1	1	2	NOP	No Operation
1	1	3	TSTRAM	RAM Test
1	1	4	CHKSUM	Verify Checksum Over EAI ROM
1	1	5-15	NOP	No Operation

Notes:

a. PPR23 and PPR22 values are as written by the CU microcode to the CC PPR.

b. The OPCODE is the nibble of data written to the DRD bus.

Table 5-25 EAI Diagnostic Data Register

AD BUS BIT	DEFINITION
3	DRD Bus Bit 3 (SSR3)
2	DRD Bus Bit 2 (SSR2)
1	DRD Bus Bit 1 (SSR1)
0	DRD Bus Bit 0 (SSR0)

Table 5-26 EAI Input Port A

AD BUS BIT	DEFINITION
8	(AEF1) equals 1 when PP110 is strobed.
7	0
6	0
5	(APF1) equals 1 when PP230 is strobed.
4	(ADF1) equals 1 when PP220 is strobed.
3	EAI Maintenance State Indication (EAIMSI1).
2	Processor Stopped/Halted Indication (STPINDI0 * SSHLTI0).
1	Processor On-Line (PONL1).
0	CC Identification Input (CCIDI0).

Table 5-27 EAI Output Port B

AD BUS BIT	DEFINITION
12	Force Bad Parity (FBPAR0)
11	EAI Ready (SSR02)
10	Emergency Action Enabled (EAEN1)
09	Force Boot Device Primary (FBDP1) (SSR06)
08	Force Boot Device Secondary (FBDS1) (SSR07)
07	Force On-Line (FONL1) (SSR10)
06	Force Off-Line (FOFL1) (SSR09)
05	Disable (sanity) Timer (DTIM1) (SSR11)
04	Emergency Action Interface Maintenance Reset Function (EAIMRF1) (SSR14)
03	Parameter Bus Bit 3 (PB31) (SSR27)
02	Parameter Bus Bit 2 (PB21) (SSR26)
01	Parameter Bus Bit 1 (PB11) (SSR25)
00	Parameter Bus Bit 0 (PB01) (SSR24)

Table 5-28 EAI Error Register

BIT	DEFINITION
7	Emergency Action Output Error
6	DUART Self-test Loopback Failure
5	DUART Self-test Initialization Failure
4	EPROM Self-test Checksum Failure
3	SRAM Self-test/Diagnostic Failure
2	Unexpected Software Interrupt
1	Sanity Timeout
0	SRAM Parity Error

5.2.12.3 EAI EPROM

The EAI EPROM contains the EAI firmware. The program memory consists of two 32-K by 8-bit EPROM devices. Data is output to the Address/Data (AD) bus.

5.2.12.4 EAI RAM

The EAI RAM consists of two 32-K by 9-bit SRAM (25 ns) devices. The RAM is used by the EAI firmware for temporary storage, data buffers, flag registers, and stack data.

The Processor Recover Message (PRM) is also stored in the RAM. The PRM is sent to the EAI by the CC during various phases of system initialization via the 4-bit DRD bus. The DRD bus is the output of the CC System Status Register (SSR), bits 03-00, under the control of three pulse points (PP11I0, PP22I0, PP23I0). The EAI forwards this information to the maintenance TTY controller for display on the maintenance terminal.

5.2.12.5 Serial Input/Output and RS-422 Interface

Emergency action requests are entered via a maintenance terminal. This interface is an RS-422 operating at 9600 baud with even parity and 7 bits per character. Status changes and processor recover information sensed by the EAI are sent to the maintenance terminal via the RS-422 interface. Table 5-29 summarizes the EAI/MTTYC RS-442 signals.

Table 5-29 EAI RS-422 Interface

SIGNAL	TYPE	DIRECTION	DESCRIPTION
EAISP0P	Differential	IN	MTTYC0 EAI Reset, Positive
EAISP0N	Differential	IN	MTTYC0 EAI Reset, Negative
EAISP1P	Differential	IN	MTTYC1 EAI Reset, Positive
EAISP1N	Differential	IN	MTTYC1 EAI Reset, Negative
EARCV0P	Differential	IN	MTTYC0 Receive Data, Positive
EARCV0N	Differential	IN	MTTYC0 Receive Data, Negative
EARCV1P	Differential	IN	MTTYC1 Receive Data, Positive
EARCV1N	Differential	IN	MTTYC1 Receive Data, Negative
EAXMT0P	Differential	OUT	MTTYC0 Transmit Data, Positive
EAXMT0N	Differential	OUT	MTTYC0 Transmit Data, Negative
EAXMT1P	Differential	OUT	MTTYC1 Transmit Data, Positive
EAXMT1N	Differential	OUT	MTTYC1 Transmit Data, Negative
EARTS0P	Differential	OUT	MTTYC0 Service Request, Positive
EARTS0N	Differential	OUT	MTTYC0 Service Request, Negative
EARTS1P	Differential	OUT	MTTYC1 Service Request, Positive
EARTS1N	Differential	OUT	MTTYC1 Service Request, Negative

5.2.12.6 EAI Status Indicators

The EAI status information is displayed via five light-emitting diode (LED) indicators as defined in Table 5-30 . The indicators are located on the Central Control (CC) circuit pack (KLW31) faceplate.

Table 5-30 EAI Status Indicators

INDICATOR	DESCRIPTION
RUN	Displays the RUN status bit, which is defined as the logical AND of *NOT STOPPED* and *NOT HALTED* (SSR17 and STOP outputs). Lights (green) when the processor is running. This indicates that the associated 3B21D computer is executing main store instructions.
ACTIVE	Displays the state of the Processor On-Line (PONL) signal (SSR16) from the associated 3B21D computer. Lights (green) when the processor is on-line.
FORCED ON-LINE	Displays the state of the Forced On-Line (FONL) signal (SSR10) to the 3B21D computer. Lights (amber) when the Central Control (CC) is forced on-line.
FORCED OFF-LINE	Displays the state of the Forced Off-Line (FOFL) signal (SSR09) to the 3B21D computer. Lights (amber) when the Central Control (CC) is forced off-line.
EMERGENCY ACTION ENABLED	Displays the state of the Emergency Action Enabled (EAEN) status bit of the EAI. Lights (amber) when a force function to the 3B21D computer is active or when the Initialization Parameter (IP) is nonzero.

5.2.13 Micro Level Test Set (MLTS) Interface

The Micro Level Test Set (MLTS) Interface circuit is on a circuit module (CM369A) that plugs into the Central Control (CC) circuit pack (KLW31).

Figure 5-17 is a functional block diagram of the MLTS Interface. The MLTS Interface circuit provides the connections between the MLTS host (TN16) and the CC. The functions supported by the MLTS Interface circuit are as follows:

- Break point matcher stops the CC when a pattern on the MSA bus is recognized.
- Trace memory stores bit patterns of the MSA bus.
- MCH circuit inhibit, which isolates the MCH circuit, preventing it from interfering with the MLTS control of the CC.
- Bus access provides the capability of reading and writing to the major CC buses (BGB, MSD, MSA, and MTC buses).
- MicroStore access provides the capability of reading the entire microstore and writing to the entire Writable MicroStore (WMS).

- Power clear provides the capability of power clearing the CC for master initialization.
- Single step provides the capability of executing one microinstruction at a time.
- Clear and set provides the capability of clearing (negating) or setting (asserting) a number of important CC bits or registers such as Panel Interrupt, STOP bit, Sanity Timer, Disable bit, and the Error register.

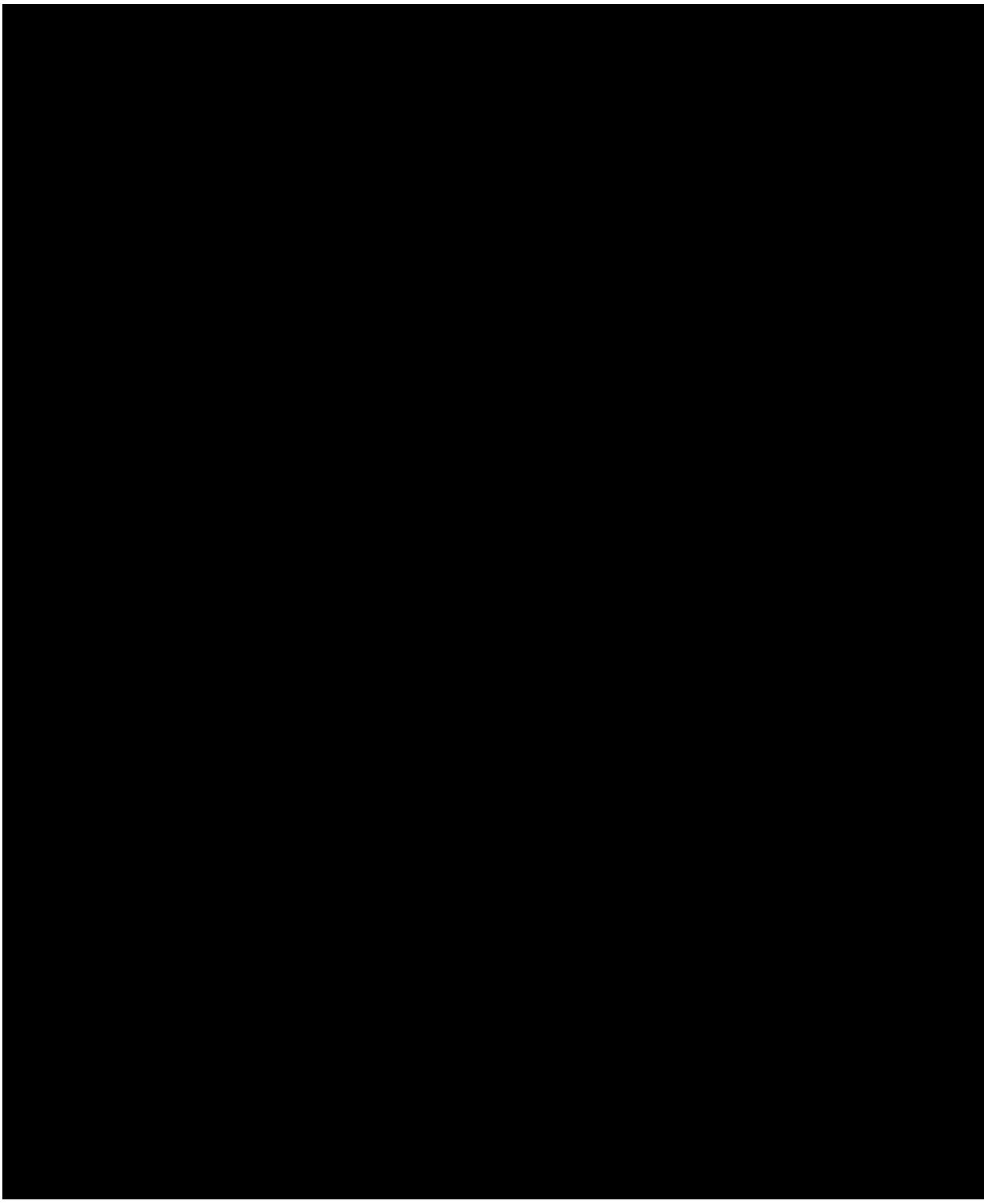


Figure 5-17 Micro Level Test Set Interface Functional Block Diagram

6. CONTROL UNIT FUNCTIONAL DESCRIPTIONS □ MAS, MASU, DMA, DSCH, UC, and EX

6.1 MAIN STORE (MAS) AND MAIN STORE UPDATE (MASU)

6.1.1 Main Memory Overview

The purpose of the Main Memory (MM) circuit pack is to provide the 3B21D computer main storage memory, which includes the following functions:

- □ Dynamic Random Access Memory (DRAM)
- □ DRAM Control
- □ Refresh/Error Scrubbing
- □ Update/Arbitration
- □ Error Detection and Correction
- □ Main Store Error Reporting
- □ Backup Maintenance Channel Link.

Figure 6-1 is a functional block diagram of the Main Memory circuit pack (KLW32, KLW40, KLW48, KLW64, or KLW128). Main Memory is accessed via the Main Store Bus (MASB) or through the Update Bus. The MASB allows CC, DMA 1, DMA 0, the other CC, and the two expansion slots (EX 0 and EX 1) access to MM. The Update Bus links the active memory (My Store) to the off-line or standby memory (Other Store) and provides a Backup Maintenance Channel. The MASB allows asynchronous communication with the CC, DMAs, and expansion slots.

The backup Maintenance Channel is via the Update Bus cabling, but has no functionality to the memory. The Backup Maintenance Channel is a group of four CC signals that are passed through the MM circuit pack and through the Update Bus cabling. These four CC signals are not connected with any logic in the MM circuit pack but enable the two processors to communicate if the regular Maintenance Channel has failed.

Table 6-1 summarizes the Update Bus signals.

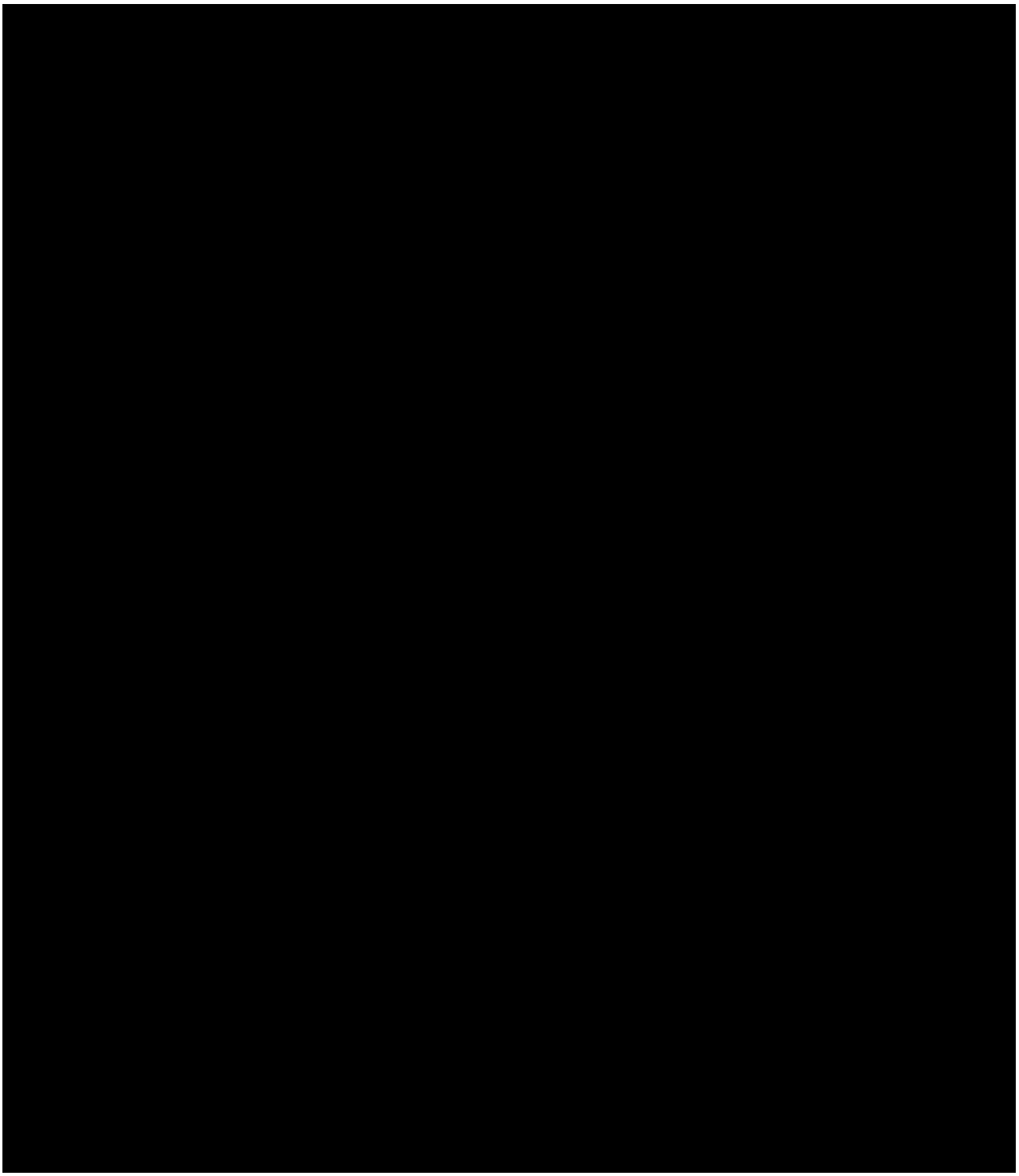


Figure 6-1 Main Memory (MM) Functional Block Diagram

Table 6-1 Update Bus

CATEGORY	SIGNAL	TYPE	DIRECTION	DESCRIPTION
ADDRESS	SUA(27-00)N SUA(27-00)P	Differential	IO IO	Update address bus differential (negative) Update address bus differential (positive)
	SUAP(3-0)N SUAP(3-0)P	Differential	IO IO	Update address bus parity (negative) Update address bus parity (positive)
DATA	SUD(31-00)N SUD(31-00)P	Differential	IO IO	Update data bus (negative) Update data bus (positive)
	SUDP(3-0)N SUDP(3-0)P	Differential	IO IO	Update data bus parity (negative) Update data bus parity (positive)

CONTROL	SUABUSN SUABUSP	Differential	IO IO	Update address bus enable (negative) Update address bus enable (positive)
	SUBYTEN SUBYTEP	Differential	IO IO	Update data byte access (negative) Update data byte access (positive)
	SUCMPN SUCMPP	Differential	IO IO	Update complete ends memory cycle (negative) Update complete ends memory cycle (positive)
	SUCOMPN SUCOMPP	Differential	IO IO	Update command even parity signal (negative) Update command even parity signal (positive)
	SUDBUSN SUDBUSP	Differential	IO IO	Update data bus enable (negative) Update data bus enable (positive)
	SUDSN SUDSP	Differential	IO IO	Update data strobe indicates data valid (negative) Update data strobe indicates data valid (positive)
	SUGON SUGOP	Differential	IO IO	Update go requests other memory (negative) Update go requests other memory (positive)
	SUHALFN SUHALFP	Differential	IO IO	Update data half word access (negative) Update data half word access (positive)
	SUMAINTN SUMAINTP	Differential	IO IO	Update maintenance access (negative) Update maintenance access (positive)
	SUOPONLN SUOPONLP	Differential	IO IO	Other Processor ONLINE (negative) Other Processor ONLINE (positive)
	SUOPUPDN SUOPUPDP	Differential	IO IO	Other CU is in UPDATE mode (negative) Other CU is in UPDATE mode (positive)
CONTROL (Contd)	SUPONLN SUPONLP	Differential	IO IO	Processor ONLINE to other CU (negative) Processor ONLINE to other CU (positive)
	SUPUPDN SUPUPDP	Differential	IO IO	Send UPDATE mode to other CU (negative) Send UPDATE mode to other CU (positive)
	SUQUADN SUQUADP	Differential	IO IO	Update data quad word access (negative) Update data quad word access (positive)
	SURMWN SURMWP	Differential	IO IO	Update read-modify-write cycle (negative) Update read-modify-write cycle (positive)
	SUUPDN SUUPDP	Differential	IO IO	Other processor in update (negative) Other processor in update (positive)
	SUWRTN SUWRTP	Differential	IO IO	Update write 0, read 1 cycle (negative) Update write 0, read 1 cycle (positive)
ERROR	SUERRAN SUERRAP	Differential	OUT OUT	My Store Error A (negative) My Store Error A (positive)
	SUERRBN SUERRBP	Differential	OUT OUT	My Store Error B (negative) My Store Error B (positive)
	SUERRCN SUERRCP	Differential	OUT OUT	My Store Error C (negative) My Store Error C (positive)
	SUERRDN SUERRDP	Differential	OUT OUT	My Store Error D (negative) My Store Error D (positive)
	SUOERRAN SUOERRAP	Differential	IN IN	Other Store Error A (negative) Other Store Error A (positive)
	SUOERRBN SUOERRBP	Differential	IN IN	Other Store Error B (negative) Other Store Error B (positive)
	SUOERRCN SUOERRCP	Differential	IN IN	Other Store Error C (negative) Other Store Error C (positive)
	SUOERRDN SUOERRDP	Differential	IN IN	Other Store Error D (negative) Other Store Error D (positive)
BACKUP MAINTENANCE CHANNEL LINK	PODISAN PODISAP	Differential	OUT OUT	Pulse Point Register bit 14 to other side (negative) Pulse Point Register bit 14 to other side (positive)
	PODISBN PODISBP	Differential	OUT OUT	Pulse Point Register bit 15 to other side (negative) Pulse Point Register bit 15 to other side (positive)
BACKUP (Contd)	PUDISAN	Differential	IN	Pulse Point Register bit 14 from other side (negative)

	PUDISAP		IN	Pulse Point Register bit 14 from other side (positive)
	PUDISBN	Differential	IN	Pulse Point Register bit 15 from other side (negative)
	PUDISBP		IN	Pulse Point Register bit 15 from other side (positive)

6.1.2 DRAM and DRAM Controller

The memory array is made up of Dynamic Random Access Memory (DRAM). The 3B21D computer simplex system contains a minimum of 32 MB of memory and a maximum of 128 MB in increments of 32 MB. The system is designed to accommodate 28-bit address buses and registers for future expansion to 256 MB. The current design uses only 27 of the 28 address bits. Even parity is maintained across data, command, and address.

The DRAM interfaces to the system via the MASB. The arbitration circuitry determines priority of the requester and allows read and write access. The data signals from the MASB are buffered and conditioned by error and correction circuitry. The store data is 39 bits wide (32 data bits, 7 parity/check bits). The physical addressing is 27 bits wide with 4 bits of even parity. The address and parity signals are buffered and then control circuitry multiplexes the address bits into row and column addresses for DRAM accesses. Parity is verified across the bus.

The update circuitry interfaces the active CU's DRAM to the other CU's DRAM maintaining a memory image on the other Store to provide a clean processor switch over.

The memory array consists of 4-megabit (Mb) by 4-bit DRAM devices with 80-ns access times. The 32-MB configuration uses twenty discrete 16-Mb DRAMs. To expand memory size by 32 MBs, Single In-line Memory Modules (SIMM) with twenty 4-Mb by 4-bit devices are inserted. The module is 8 Mb deep by 40 bits wide and meets the standard Joint Electron Device Engineering Council (JEDEC) outline. Three 72-pin SIMM connectors are used to upgrade the system in 32-MB increments to 128 MB. These connectors seat the SIMMs at a 22.5-degree angle. The input and output data is multiplexed to the same data pins, controlled by an enable. The device addressing requires an 11-row, 11-column address multiplexing with a 2-K refresh in 32 milliseconds. The 16-Mb devices are packaged differently from other DRAM devices. The lead-on chip with center board (LOCCB) maintains uniform input pin capacitance. Two metal bus lines run parallel above the length of the device to connect dual Vcc and Vss pins. This structure reduces resistance, inductance, and electrical noise.

The following list of DRAM control signals provide the correct timing protocol to the DRAM devices:

- Data
- Address
- Row Address Strobe (RAS)
- Column Address Strobe (CAS)
- Write Enable (WE)
- Output Enable (OE).

Different protocols exist for the corresponding operations. A normal read or write access requires single row and column address strobes (RAS and CAS) with the multiplexed address. The OE signal controls the direction of the data to/from the DRAM and WE signals read or write operations. The read-modify-write mode selects a single row and column address while changing the control signals. Fast page mode allows reading or writing of several words by supplying a single row address and strobing consecutive column addresses. Fast page mode provides the protocol for quad word accesses. The DMAs and Expansion (EX) slots use this feature. The memory controller supports the following cycle types:

- **READ** – quad word or full word
- **WRITE** – quad word, full word, half word, or byte
- **READ-MODIFY-WRITE** – full word, half word, or byte.

The full word is identified as having 32 bits and 4 parity bits. The half word and byte addressing is controlled by address bits 1 and 0 (SA01 and SA00), the control signals for half word (SHALF,SUHALFP/N), and byte (SBYTE,SUBYTEP/N). See Table 6-2 .

Table 6-2 Data Bit, Byte, and Word Definitions

DATA LENGTH DEFINITION					
DEFINITION	**SHALF**	**SBYTE**	**SA01**	**SA00**	**DATA BITS**
FULL WORD	1	1	0	0	31-00
HALF WORD(0)	0	1	0	0	31-16
HALF WORD(1)	0	1	1	0	15-00
BYTE(0)	1	0	0	0	31-24
BYTE(1)	1	0	0	1	23-16
BYTE(2)	1	0	1	0	15-08
BYTE(3)	1	0	1	1	07-00

Data from a bus master is passed with even parity on each valid byte. When a byte(s) is invalid, odd parity is passed with that byte(s). Parity bit SDP0 corresponds to parity over byte 0 with the remaining parity bits SDP3-1 representing the bytes 3-1.

Other commands are necessary for defining writes and reads (SWRT), quad word transfers (SQUAD), read-modify-writes (SRMW), and store maintenance access (SMAINT). An even parity bit is provided across the command signals.

The DRAM Control is invisible to the MASB and Update Bus. Command signals are passed across these buses to provide information to the DRAM controller.

A Memory Controller with Error Regulation and Test (MCERT) ASIC device is used to perform several memory functions. The MCERT device runs at 33 MHz to provide input signals to the DRAMs. The MCERT device requires the CC to program up to 17 registers for the control mode. The CC can gain access to these registers through an expanded address map in the maintenance mode. The device has two modes of operation: control (MC) and data (DP). The MCERT device is used for the DRAM control, refresh, Error Detection and Correction (EDC), parity checking, memory test, and power up functions on the MM pack. The MCERT device reduces board area that would be required by discrete components. Additional parity checking is needed because the MCERT device addresses based on word boundaries (for example, quad word, half word, or full word) and assumes even parity. This affects byte 3 where bits 0 and 1 are not used.

Registers in the MC mode determine the following:

- Refresh interval/generation
- Page mode length
- Odd/even address parity selection and checking
- Bank definition, size, addressing, fault indication, and status
- Memory scrubbing during reads and refresh
- Error status
- DRAM signal definition (pulse widths, setup, and hold times).

The MCERT device has a programmable data and address First-In First-Out (FIFO), providing a maximum depth of four entries. A full and a full -1 flag are also programmable for use in quad word transfers to hold the bus master from putting more data/address information on the MASB or Update Bus. This also enables the device to look ahead to the row and column addresses. Accesses to consecutive addresses allow the device to shorten what would be two full access cycles to a long single access (that is, remove the precharge and leave RAS low while bringing CAS low consecutively with new column address information).

6.1.3 Refresh/Error Scrubbing

The refresh function is required due to the nature of DRAM devices. An RAS-only refresh cycle is used with error checking and correcting performed (error scrubbing). The 4-Mb by 4-bit DRAM configured with 11 rows and 11 columns requires a 2-K refresh in 32 milliseconds. The MCERT provides a refresh rate of 15.3 microseconds for the 2048 rows, performing a full DRAM refresh in 31.33 milliseconds. An address counter and a watchdog timer are used to ensure each row is refreshed in the required time frame. If the first refresh request is not performed and the request reset, a second refresh is requested. If the controller is still busy, the controller aborts its operation and does two refresh cycles sequentially. An abort error flag is set and latched in the MCERT device running in the control mode. A general error signal is output from the MCERT device to signal the error.

The refresh function interfaces the DRAM controller, the DRAM devices, the EDC function, and error reporting to the CCs. The refresh function is invisible to the rest of the system unless an error occurs and requires reporting to the CCs.

Memory array refresh is performed by the DRAM control circuitry (MCERT) using an internal timer, an address counter and error address latch, automatic correction of single bit errors, and error reporting of single and multiple bit errors during the scrub function. The refresh/error scrubbing functions are internal to the MCERT device. The functions are accomplished through the connection of two MCERT devices; one in the MC mode, performing the refresh and one in the DP mode for error checking. The hardware will RAS-only refresh on all 16-MB increments, but error scrub each 16-MB bank individually and continue to the next 16-MB bank.

6.1.4 Update/Arbitration

The update function is used in fault tolerant design to maintain a mirror image of memory on the other side for switch over, if it is in standby. Update is performed when the DRAM is written. When the write is not controlled by the CC, then a signal (CAINVL0) is sent to the CC to invalidate the cache.

The arbitration function is software changeable. Arbitration is done on the devices that have access to the MASB and Update Bus. These are the CC, DMA 0, DMA 1, the other CU, and the two expansion slots (EX 0 and EX 1). The function allows software to set priorities to each possible bus requester. If two or more requesters are asking for the bus with the same priority, a round-robin scheme is used. The highest priority is other CU access, followed by "my" CC access.

Both the update and arbitration functions use the MASB and the Update Bus for memory accesses. Each device has a set of signals that make up the memory access protocol. These signals are Store Go, Abus, Dbus, Data Strobe, and Store CoMplete. The functional hardware accepts requests, arbitrates to provide the six possible requesters access, then provides address and data enables and cycle complete signals. The arbitration circuit informs the memory control logic that a memory access has started.

When the DMAs, Expansion slots, or the other CU are bus masters, the arbitration circuitry provides a cache invalidate signal (CAINVL0) for a write or read-modify-write cycles. The cache in the other CU is not invalidated on updates to memory from the active side.

6.1.5 Error Detection, Correction, and Reporting

Memory array EDC uses the flow-through method. During a word write, the data flows through the EDC device and seven check bits derived through an algorithm on the data are output. The 39 bits are then

stored in DRAM. When a word read is requested, the data (39 bits) is sent to the EDC device to check for errors. Syndrome bits are created to define the bit or multiple bits in error. If a single bit error is detected, data is corrected and an error flagged and reported. If a multiple bit error is encountered, data is not corrected, and a multiple bit error is flagged and reported. The address at the time of the error is latched and can be read via the maintenance addressing of the MCERT device.

When byte or half-word write cycles occur, a read from that address in DRAM must extract the non-modified data and overlay it with the new data, then create new check bits. Now the 39 bits of data are placed in memory.

The EDC function interfaces to the control function circuitry for reads, writes, and refreshes. It also reports errors that go to My CC via the MSB and to the Other CC via the Update Bus. The data paths are to and from the MSB and to and from the DRAM.

The MCERT device is also used for the EDC function on the memory pack. It is connected to the other MCERT device used for the DRAM control functions. The device uses a seven-bit hamming algorithm to identify single-bit errors given the syndrome bits. Multiple-bit errors are identified but not corrected. The correction of data is done internally using temporary registers and providing good data in the read data queue.

The MM reports five types of errors to the CC. Their severity can cause a stop and switch. The address is latched when an error occurs. The five error types are as follows:

MYSERA Address parity error detected. CC Error Register bit 6.

MYSERB Address out of range. CC Error Register bit 23.

MYSERC Multiple-bit data error. CC Error Register bit 8, Stop and Switch.

MYSERD Single-bit data error. CC Error Register bit 20, Single bit correctable or Stop and Switch for multiple bit error.

OSTIMEOUT Other Store access time-out (5.6 microseconds). CC Error Register bit 15.

OSTIMEOUT is a time-out started by the "go" signal and ended with the "complete" signal. The CC contains a timer that watches the CU's memory for cycle completion. It is called the MYTIMEOUT and is located in CC Error Register bit 7.

The MYSER(A,B,C,D) signals belong to the MASB. These signals go to DMA 0, DMA 1, Special Registers (SREGs) 0 and 1, the cache storage unit (CSU), and the Store Address Interface (SAI). The active memory circuit pack feeds the My Store Errors to the other store through the Update Bus [SUERR(A,B,C,D)]. The other store passes these signals to its SREG [OSTER(A,B,C,D)]. My Store also receives the Other Store Errors [SUOERR(A,B,C,D)] and sends them to the SREGs [OSTER(A,B,C,D)].

6.1.6 Self-Identification (SLFID) Circuit

The Self-ID (SLFID) circuit provides the means for a Central Control (CC) to interrogate the MM circuit pack for identification information (version, issue, and so forth). The circuit operates independently from the other circuit pack functions.

The circuitry consists of transceivers to interface the SLFID bus with the circuit pack, an ID field that is the bus address of the circuit pack, an address register to store the incoming bus address, a comparator to compare the ID field to the bus address, a binary counter to generate the programmable read-only memory (PROM) address, and a PROM that contains the circuit pack ID information and control lead interface and logic.

6.1.7 Boundary Scan Interface

The Boundary Scan (BS) interface to the MM circuit pack is via the primary BS bus. The BS bus is a serial bus used to test (diagnose) components. All boundary scan functions are controlled by the CC.

6.1.8 Backup Maintenance Channel

The Backup (or emergency) Maintenance Channel is a second processor-to-processor communications link. The Backup Maintenance Channel used when the regular maintenance channel is either not functional or when it is necessary for the active processor to maintenance reset the other processor. The Backup Maintenance Channel consists of four signals. The outputs from Pulse Point Register (PPR) bits 14 and 15 in each processor are connected to logic in the other processor. The signal connections are made by routing the pulse points from the KLW31 circuit pack to the MM circuit pack (KLW32, KLW40, KLW48, KLW64, or KLW128). At the MM circuit pack, the logic signals are converted to differential signals and included as part of the update cable between the processors. Therefore, eight wires are used to carry the four signals in the Update Bus. The transmitting side of the Backup Maintenance Channel is the PPR. The receiving end includes the Hardware Status Register (HSR), System Status Register (SSR), and the reset logic.

As shown in Figure 6-2 , pulse points 14 and 15 (PPR14 and PPR15) from the other processor come in as signals PDISA0 and PDISB0 to the HSR where they are registered as HSR bits 8 and 9. They also go to reset logic. Pulsing PDISA0 and PDISB0 in certain sequences will disable the receiving processor and then cause it to reset. To disable the processor, PDISA0 and PDISB0 are pulsed in sequence. This action will also set SSR bit 30, and IO is inhibited to that processor. If the next pulse is a PDISA0, then that processor will do a maintenance reset. The pulses are activated by writing sequentially to PPR14 and PPR15 in the active processor. This is done by the software when it deems vital to reset the other processor and the regular maintenance channel is determined to be not working.

Figure 6-2 Backup Maintenance Channel Functional Block Diagram

6.2 DIRECT MEMORY ACCESS (DMA) AND DUAL SERIAL CHANNEL (DSCH)

Figure 6-3 is a functional block diagram of the DMA circuit pack (KBN15). The 3B21D computer supports two DMAC/DSCH units (KBN15 circuit packs). For a description of the Central Control Input/Output (CCIO) bus, Main Store Bus (MASB), and Boundary Scan (BS) bus, see "Central Control (CC)" in Section 5 .

The Direct Memory Access and Dual Serial Channel circuit pack (KBN15) transfers data between peripheral devices and main memory. It allows programmed I/O between peripheral devices and the CC. The DMAC/DSCH consists of one direct memory access controller and four I/O channels. Each I/O channel supports four peripheral devices. Therefore, a DMAC supports 16 peripheral devices.

The specific functions of the DMAC/DSCH (DMA circuit pack) are as follows:

- Interfaces with the main memory via the MASB.
- Interfaces with the Duplex Dual Serial Bus Selector (DDSBS) in the Disk File Controller (DFC), Input/Output Processor (IOP), and application peripherals through the DSCH interface.
- Converts the dual serial streams of data received from the DDSBS into a 36-bit (32 data bits and 4 parity bits) parallel format.
- Decodes and arbitrates the interrupts, DMA setup requests, and DMA transfer requests received across the DSCH interface from the peripheral devices.
- Translates the virtual addresses used by the peripheral devices to physical addresses used by the main memory.
- Transfers data to and from the peripheral devices as full 36-bit (32 data bits and 4 parity bits) words or as sixteen 36-bit word blocks.
- Interfaces with the CC through the CCIO bus. The CC performs programmed I/O (PIO) operations to the DMAC, the channels, and the peripheral devices through this interface.

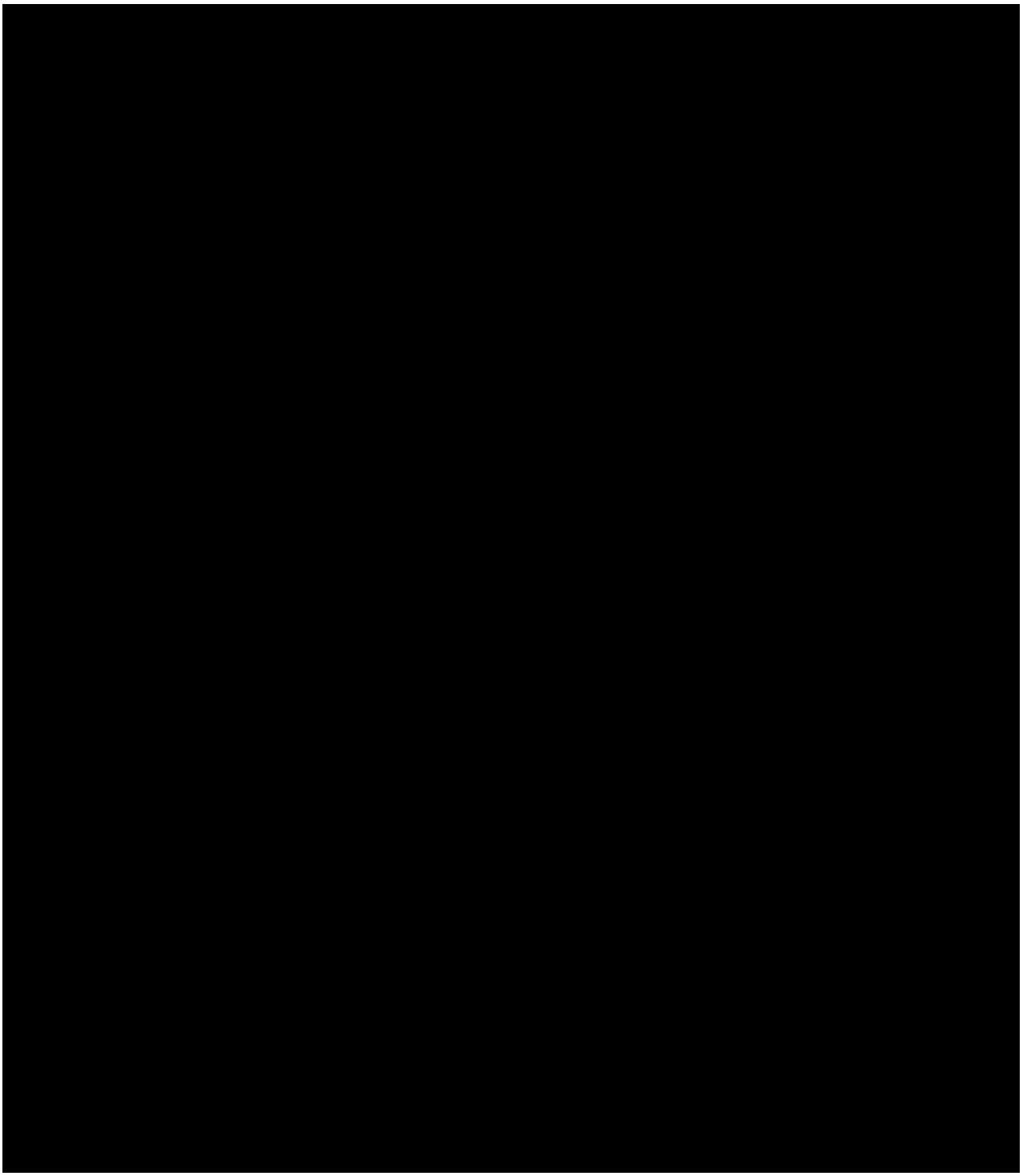


Figure 6-3 Direct Memory Access (DMA) Functional Block Diagram

6.2.1 Direct Memory Transfers

The DMAC Main Memory Interface implements the 3B21D computer MASB protocol and controls full and quad word transfers between the DSCHs and the Main Memory. The DMAC transfers data to and from Main Memory as full 36-bit words. The DMAC can also transfer data to and from the Main Memory in groups of four words. The DMAC determines when to do a quad word transfer by checking the quad word alignment of the address.

6.2.2 Direct Memory Access Controller (DMAC)

The DMAC/DSCH ASIC with its microcoded PROM provides the control and sequencing for the CCIO interface, MASB interface, and the Dual Serial Channel interfaces. The DMAC/DSCH ASIC is divided into five functional partitions as follows:

- CCIO Interface
- Main Memory Interface
- Control
- Device Priority Logic
- Channel Interface.

The DMAC Control logic consists of a microprogram controller and the associated logic that controls the sequencing and timing of itself and the other functional partitions within the ASIC. The Control logic also contains the request logic that arbitrates the DSCH channel and CC requests for DMAC.

The Device Priority Logic arbitrates the DMA service requests from the peripheral devices.

The Channel Interface consists of four DSCHs that control the transfer of data, commands, status, and requests between the peripheral devices and the DMAC. Each DSCH supports up to four peripheral devices.

6.2.3 PROM

The PROM (microcoded PROM) is 40 bits wide and 8 K deep. The 40 bits are divided into 12 fields as follows:

- Bits 08-00 provide DSCH control information.
- Bits 13-09 provide pulse point information.
- Bit 14 (no function is assigned).
- Bits 18-15 identify the destination registers.
- Bits 22-19 identify the source registers and also contain the four-way branch enables.
- Bit 23 indicates RAM access.
- Bits 27-24 indicate branch conditions.
- Bit 28 is the clear ROM sequencer check bit.
- Bit 29 is the increment control bit.
- Bit 30 enables internal bus parity checking.
- Bits 34-31 contain the 2910 device instructions.
- Bits 39-35 contain the 5 parity bits across the 5 bytes that make up the 40-bit word.

6.2.4 20-MHz Clock

The 20-MHz clock provides the primary clock stream for the DMAC/DSCH ASIC and the microcoded

PROM. It consists of a 40-MHz oscillator and a divide-by-2 circuit.

6.2.5 CCIO Interface

The CCIO interface on the circuit pack is a set of buffers and tristate bus transceivers that are used to interface signals between the CCIO bus and the DMAC/DSCH.

6.2.6 Main Store Bus Interface

The MASB interface circuitry on the circuit pack interfaces the 36-bit, tristate bus from the ASIC to a 32-bit Main Store Address Bus and a 36-bit Main Store Data Bus. The ASIC multiplexes the Main Store address (28 address bits and 4 parity bits) and data (32 data bits and 4 parity bits) to and from the 32-bit tristate bus. A register is provided on the circuit pack to store the address with its parity bits. Tristate drivers (32) interface the address register to the Main Store tristate bus. The data register is internal to the ASIC. After the address has been set up in the address register, the data register is gated to the 36-bit tristate bus. The data can then be transferred. A set of 36 tristate transceivers interface the data register to the 36-bit tristate MASB.

6.2.7 DSCH Interface

There are four independent DSCHs. Each channel can interface four peripheral devices, but only one device on each channel at a time. The complementary circuit in the peripheral device that communicates with the DSCH is called the Duplex Dual Serial Bus Selector. The DSCH and DDSBS operate in a half-duplex mode, alternating between sending and receiving. In each transmission, 36 bits are sent simultaneously by sending two 18-bit streams called high data and low data. Requests for service are initiated by peripheral devices over their dedicated request lead. The physical cable link is implemented with RS-422 drivers and receivers.

The DSCH interface is the interface between the DMA I/O channels and the peripheral devices, such as DFCs and IOPs. The DSCH interface consists of five differential signals that pass between the DMAC/DSCH and the Duplex Dual Serial Bus Selector (DDSBS) as follows:

HIGH DATA Signal used for the serial transmission of the high half-word of each 32-bit data word.

LOW DATA Signal used for the serial transmission of the low half-word of each 32-bit data word.

TRANSMIT CLOCK A clock signal transmitted by the I/O channel to the peripheral device.

RECEIVE CLOCK A clock signal received by the I/O channel from the peripheral device.

REQUEST Signal used by the peripheral device to transmit requests to the I/O channel. There are three types of requests: DMA transfer, DMA setup, and Interrupt. The DMA setup request is used when the peripheral device wants a virtual memory address translated to a physical address. The DMA transfer request is used when the peripheral device wants to access main memory. The Interrupt request sends an interrupt to the CC from the DMAC/DSCH (KBN15) unit over the CCIO interface.

6.2.8 Self-Identification (SLFID) Circuit

The SLFID circuit provides the means for a Central Control (CC) to interrogate the DMA circuit pack for identification information (version, issue, and so forth). The circuit operates independently from the DMAC/DSCH ASIC.

The circuitry consists of transceivers to interface the SLFID bus with the circuit pack, an ID field that is the bus address of the circuit pack, an address register to store the incoming bus address, a comparator to compare the ID field to the bus address, a binary counter to generate the PROM address, and a PROM that contains the circuit pack ID information and the control lead interface and logic.

6.2.9 Boundary Scan Interface

The Boundary Scan (BS) interface to the DMA circuit pack is via the primary BS bus. The BS bus is a serial bus used to test (diagnose) components. All boundary scan functions are controlled by the CC.

6.2.10 Miscellaneous Control Group

6.2.10.1 Quad Word Inhibit Strap

A pin is provided on the backplane for disabling quad word transfers. When the pin is grounded, requests for quad word transfers result in single-word transfers.

6.2.10.2 DMA Identification Strap

A ground is provided on an input pin in the DMA 1 backplane position to provide the card identity to the ASIC and also provides a ground to the power controller when a DMA circuit pack is inserted in the DMA 1 backplane slot. The ground to the power controller allows it to decide whether to generate an alarm because the B power supply is not installed. That is, an alarm is generated if DMA 1 is installed and the B power supply is not installed. No alarm is generated if DMA 1 is not installed and the B power supply is not installed.

6.2.10.3 Power Programming Resistor

If the leads from the power programming resistor are open or shorted to some other circuit, the power supply associated with the DMA circuit pack will not supply power.

6.3 UTILITY CIRCUIT (UC)

The optional Utility Circuit (UC) circuit pack (UN379), along with the Generic Access Package (GRASP) software, monitors operations between the CC and Main Memory (cache or main store) for the purpose of program debugging and testing. Figure 6-4 is a high-level functional block diagram of the UC.

The UC matcher circuits monitor both main memory reads and main memory writes and can compare both virtual or physical addresses. The UC can be configured to interrupt the processor on one unique condition or on several program states.

The Transfer-trace circuitry records both program transfers and process changes [Utility IDentification (UID) changes]. Program transfers include direct program transfers, calls to and returns from subroutines, and transfers to/from interrupt routines. Process changes are recorded each time program execution changes from one process to another. Data History alone or Data History with Simultaneous Program Transfer Trace can be recorded by the Trace Memory.

The following functions are provided by the UC:

- Compare and match on Virtual or Physical Addresses, Data, Address Range (Block Match), Memory Access (Read/Write, Instruction Fetch, etc.), and Process Transfer (UID Change).
- Provide four triggers that can accept input from any matcher or combination of matchers and generate an interrupt.
- Record Trace Memory, which is controlled by the Trigger Function outputs. The Trace Memory can record until ordered to halt, record during a window defined by trigger outputs, or record until full.

- Configure Trace Memory to monitor and record Data History. In this mode the data, data address, and program address are recorded.
- Configure Trace Memory to monitor and record the FROM and TO addresses and UID values of Program Transfers, UID Changes, Function Calls, and Function Returns. In addition, any of these program trace modes can be used simultaneously with Data History Trace.

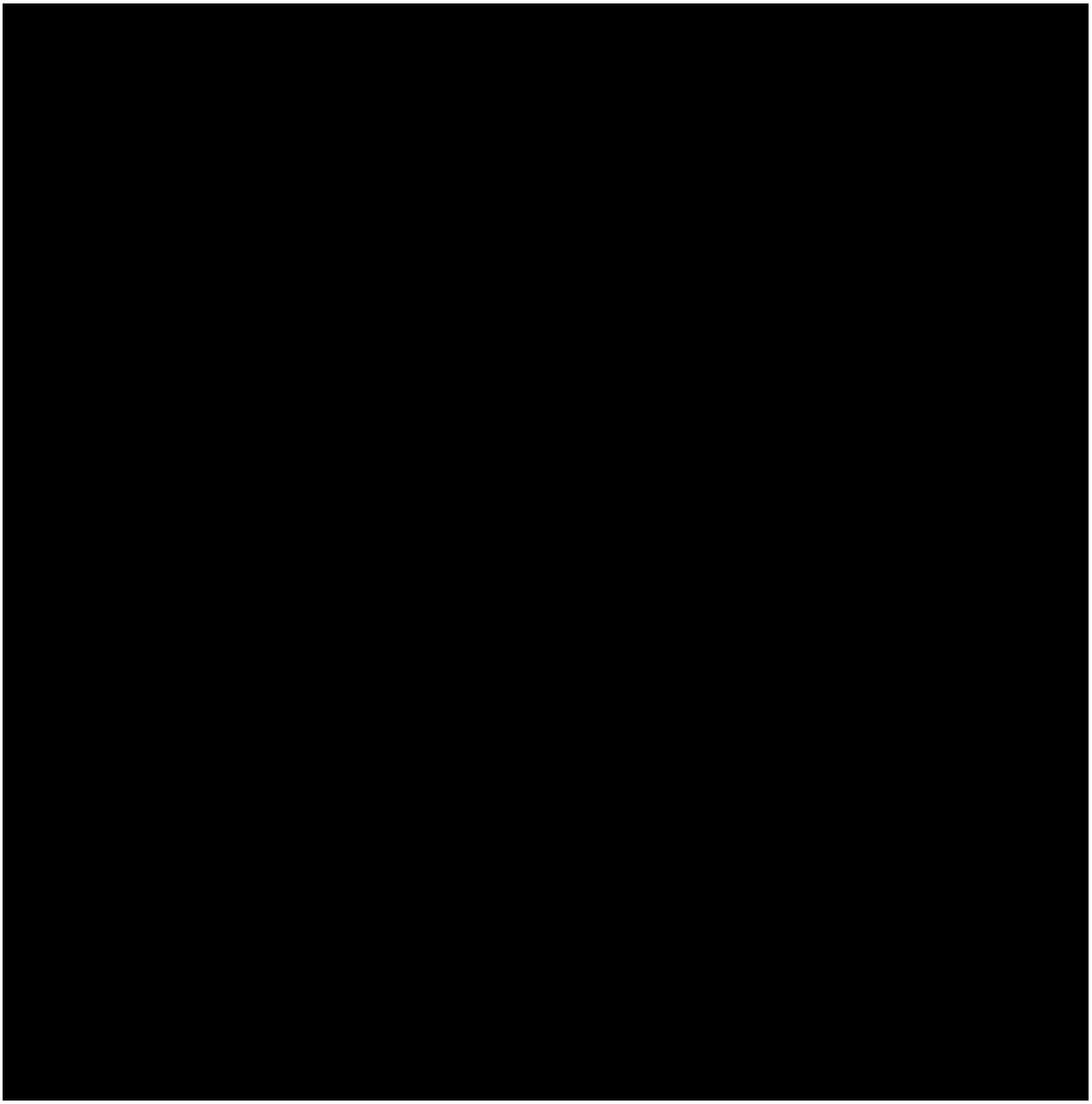


Figure 6-4 Utility Circuit (UC) Functional Block Diagram

6.3.1 UC Internal Data Bus (DATB)

The Internal Data Bus in the UC is designated as DATB. The DATB connects the various data sources and destinations in the UC. This 32-bit bus provides the means to program the UC and to read results from the UC via the Bidirectional Gating Bus (BGB).

6.3.2 BGB Input/Output Interface

The BGB is used to program the UC circuit pack for specific conditions and operations. The BGB is also used to read trace memory and status data from the UC circuit pack via the DATB.

6.3.3 Matcher Address and Data Input Logic

The input logic for the Address Matcher, Address Block Matcher, and Data Matcher accepts the data that the UC will use for matching and possible triggering. This data includes the Virtual Address (SAR[27-11]), Physical Address (CA[27-00]), Cache Data (CD[31-00]), and FTCH, WRT, HALF, and BYTE. The Address Data (SAR[27-11], CA[27-00]) and Cache Data (CD[31-00]) is buffered on the CC circuit pack with transparent latches to provide hold time. Enabling of this latch is done by a signal provided by the Store Interface.

The Access Counter/Latch stores FTCH, WRT, HALF, and BYTE signals at the beginning of each store access. This latch is clocked by ACCCK1. The Data Counter/Latch stores the Cache Data Bus. This latch is clocked by DATCK1. Input to the Address Counter/Latch is provided by the output of the Address Multiplexer, which multiplexes either the physical address (CA[27-11]) or Virtual Address (SAR[27-11]) into the upper 17 bits of the latch. The lower 11 bits are driven by the Physical Address offset (CA[10-00]).

All three latches can be configured as counters for programming the matchers and for testing the UC circuit pack. The CC can clear the latches to logical zeros and then increment the counter/latches until the desired value is reached.

6.3.4 Matcher Logic

The matcher logic includes five matcher circuits. Each matcher circuit provides outputs that drive each of the four trigger circuits.

The Data Matcher uses a 256- by 16-bit RAM configured as four matchers to match any data pattern output from the Data Counter/Latch.

The Address Matcher uses a 256- by 16-bit RAM configured as four matchers to match any address pattern output from the Address Counter/Latch.

The Access Matcher uses a 16- by 4-bit RAM to match on any access type (FTCH0, WRT0, HALF0, or BYTE0).

The UID Matcher uses a 256- by 12-bit RAM to match on UID values output by the UID Map.

The Address Block Matcher circuits each contain four 256- by 16-bit RAMs. The RAM outputs are connected to logic that detects whether the data in the Address Counter/Latch is within the address range indicated by the matcher programming.

6.3.5 Utility IDentification (UID) Map

The Utility IDentification (UID) Map is an 8-word by 24-bit RAM addressed by the Address Translation Buffer (ATB) select bits TAA(10-08). These three bits indicate the current process UID. Microcode writes new UID values to the UID Map using BGBPP(2)0. When a nonsequential access occurs (BRANCH0 is active), the new value of TAA(10-08) is compared to the old value. An indication of any UID change is output to the Trigger Logic, which decides if a trigger function should be enabled.

6.3.6 Trigger Logic

The Trigger Logic stores the trigger conditions programmed via the BGB in the "freeze" mode. In the "run" mode, the Trigger Logic accepts outputs from all matcher circuits and compares the matcher circuit outputs to the programmed conditions. When matches are made, the Trigger Logic activates the appropriate trigger

output to the Control Logic that controls the Trace Memory recording.

6.3.7 Trace Memory

The Trace Memory records store accesses (Cache or Main Store) under the control of the Trigger and Access Control circuitry. It consists of a 16-K by 97-bit RAM. Address, data, UID values, and other data is stored in various combinations depending on the GRASP-generated programming.

6.3.8 Utility Circuit Interrupt

The UC generates a CC-interrupt signal called UTLINT0. This signal, when active, tells the CC that the UC Trace Memory is full. This allows the CC to inform the user via GRASP that the UC can no longer monitor operations between the CC and Main Memory.

6.3.9 Self-Identification (SLFID) Circuit

The Self-Identification (SLFID) circuit provides the means for a Central Control (CC) to interrogate the UC circuit pack for identification information (version, issue, etc.). The SLFID circuit operates independently from the other UC functions.

The initial release of the 3B21D computer and the UC circuit pack will not have a functioning circuit pack self-identification feature. The circuit pack self-identification circuits are designed into all new circuit packs; however, the components will not be installed on the circuit packs.

6.3.10 Boundary Scan Interface

The Boundary Scan (BS) bus interface is used only to read the UC circuit pack self-identification data stored in the SLFID circuit. No gate array devices supporting boundary scan diagnostics are used by the UC circuit pack.

6.4 EXPANSION SLOTS (EX 0 AND EX 1)

The Expansion Slots (EX 0 and EX 1) provide an interface for new hardware features to access the MAS and for the CC to access the new hardware through the CCIO bus or the MASB.

7. PERIPHERAL DEVICE FUNCTIONAL DESCRIPTIONS □ DFC, IOP, PC, and PSSDB

7.1 DISK FILE CONTROLLER (DFC)

The Disk File Controller (DFC) connects peripherals that use the Small Computer System (SCSI) Interface, which includes disk and tape drives, with the Direct Memory Access Dual Serial Channels. The DFC consists of Disk File Controller A (DFCA), DFCB, and a 410AA power converter. Each DFC provides two independent SCSI buses (see Note). The DFC connects to the Control Unit via the Dual Serial Channel (DSCH) interface.

NOTE: The naming convention for the two SCSI buses provided by a DFC designates the buses "BUS A" and "BUS B." The 3B21D computer system designations for the SCSI buses are as follows.

- The SCSI BUS A and BUS B provided by DFC 0 are "SBUS 0" and "SBUS 2."
- The SCSI BUS A and BUS B provided by DFC 1 are "SBUS 1" and "SBUS 3."
- The SCSI BUS A and BUS B provided by DFC 2 are "SBUS 4" and "SBUS 6."

Figure 7-1 is a functional block diagram of the DFC, which shows six blocks of information (in dashed boxes) as follows:

- Two blocks are called DFCA and represent the hardware in a UN373 circuit pack. The UN373 circuit pack provides the SCSI bus interface.
- The DFCB block represents the logic in the TN2116 SCSI Host Adapter circuit pack that supports SCSI-1. Therefore, the TN2116 controls the SCSI bus.
- The fourth block is the power supply. For the UN580, power is supplied by the 410AA power converter circuit pack. For the UN580B, power is onboard the UN580B circuit pack.
- The fifth block shows the UN580 circuit pack, which consists of combined blocks DFCA and DFCB. Therefore, the UN580 circuit pack replaces the functionality of both UN373 and TN2116 circuit packs in one circuit pack. Remember that power is supplied by the 410AA circuit pack.
- The sixth block (UN580B) consists of the DFCA and DFCB blocks and a power supply located on the UN580B circuit pack. Therefore, the UN580B circuit pack replaces the functionality of the UN373, TN2116, and 410AA circuit packs in one circuit pack.

SCSI-1 is a byte-wide data transfer protocol that uses a 50-pin interface. SCSI-2 is a 32-bit, four-byte-wide data transfer protocol that is called "wide SCSI." The SCSI Host Adapter circuit packs (UN373 and TN2116, or UN580, or UN580B) support only SCSI-1. None of these circuit packs support the 32-bit SCSI-2.

In later versions of the 3B21D computer, the DFCA and DFCB blocks were combined into a single circuit pack called the UN580. This allowed the DFC to be realized with one logic circuit pack (UN580) and one power supply (410AA). When a DFC is equipped with a UN580, the UN580 installs in the slot previously used for a UN373. Then, the TN2116 is not needed, although it could be installed without doing any harm.

Shortly after the release of the UN580 circuit pack, a UN580B version was released that combined the DFCA, DFCB, and power supply blocks. This allowed the DFC to be realized with one logic circuit pack (UN580B). Thus, in the UN580B series circuit pack, the TN2116 and 410AA circuit packs were eliminated, and the UN373 or UN580 was replaced by the UN580B.

When a DFC is equipped with a UN580B, the UN580B installs in the slot previously used for a UN373 or

UN580. There is an unused circuit pack position on both sides of a UN580B.

The SCSI DFC controls the hard disk drives and tape drives. It consists of a Duplex Dual Serial Bus Selector (DDSBS), a Bus Interface Controller (BIC) that provides an interface to the Control Unit (CU), an SCSI Host Adapter (HA), and power control circuitry. The SCSI HA has two parts: a microprocessor-based control section and an SCSI interface. A description of each of these functional blocks follows. A high-level block diagram of the DFC is shown in Figure 7-1 .

7.1.1 Duplex Dual Serial Bus Selector (DDSBS)

The DDSBS provides an interface between the Dual Serial Channel (DSCH) and SCSI HA. Each DFC has a DDSBS that connects to two DSCHs; one on each duplex processor. This allows both CUs of the duplex processor (CU 0 and CU 1) to have access to the peripherals. The specific functions of a DDSBS are as follows:

- To select which DSCH can currently communicate with the peripheral device.
- To convert between the dual serial bit-stream protocol used by the DSCH to the 36-bit (32 data and 4 parity) format used by the peripheral device's BIC.
- To provide maintenance functions such as request generation and data loop-around for diagnostic testing.

7.1.2 Bus Interface Controller (BIC)

The specific functions of the BIC are as follows:

- To buffer data passing between the devices and the DDSBS.
- To provide logic that allows the device to send DMA setup requests, DMA transfer requests, and interrupt requests to the DMAC.
- To monitor and report error conditions.

7.1.3 Host Adapter (HA) Control

The control portion of the HA is a 32-bit, microprocessor-based design that allows the HA to run autonomously. The specific functions of the control portion are as follows:

- Read and write all memory on the HA, including memory-mapped registers.
- Arbitrate between the HA CPU and HA Direct Memory Access Controller (DMAC) for control of the HA microbus.
- Handle interrupt conditions.
- Receive reset requests and generate resets throughout the HA.
- Provide memory for operational firmware, onboard diagnostics, and data buffering.
- Control an RS-232 debugging interface. Note that this interface is supported.

7.1.4 Small Computer System Interface (SCSI)

The SCSI portion of the HA controls data transfers between two independent SCSI buses and the rest of the HA. The specific functions of the SCSI are as follows:

- Provide high-speed data transfers between the SCSI buses, HA memory, and the BIC.
- Support both the SCSI-1 and SCSI-2 bus protocols (see Note).
- Provide an SCSI-compatible electrical interface.

NOTE: The UN373 DFCA circuit pack and the TN2116 SCSI Host Adapter circuit pack support SCSI-1 only. Neither circuit pack supports 32-bit SCSI-2.

7.1.5 Power Control

The DFC is an independent fault group and has its own power supply and power switch. The UN373 and UN580 circuit pack provides the power control function.

7.1.6 Self-Identification (SLFID)

The UN373 circuit pack incorporates a self-identification (SLFID) and boundary scan function into the boundary scan function. Self-identification is done using the boundary scan bus. The contents of a ROM identifying the circuit pack is returned via the boundary scan bus when the ROM is addressed. The UN373 circuit pack self-identification circuits are part of the circuit pack design; however, the circuit components are not installed.

The UN580 circuit pack does not have any self-identification functionality. The self-identification function was put back on the UN580B; however (like the UN373), the circuit components are not installed.

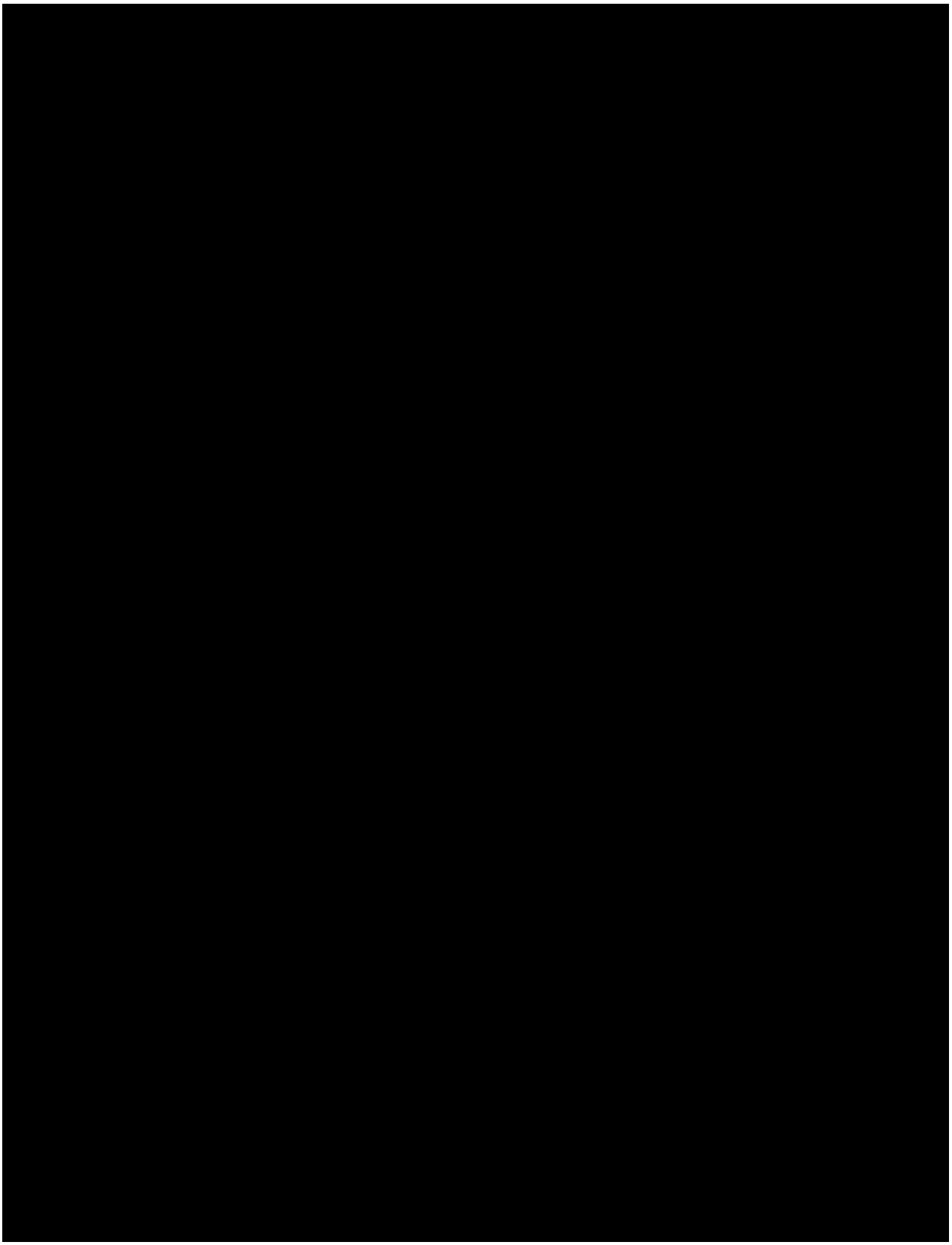


Figure 7-1 Disk File Controller (DFC) Functional Block Diagram

7.2 INPUT/OUTPUT PROCESSOR (IOP)

7.2.1 IOP System Overview

The 3B21D computer can have four IOPs (IOP 0 through IOP 3). IOP 0 is equipped in Processor Unit 0 at EQL 19-065. IOP 1 is equipped in Processor Unit 1 at EQL 45-065. IOP 2 is equipped in the Growth Unit at EQL 11-011. IOP 3 is equipped in the Growth Unit at EQL 62-011.

Functionally, an IOP can support four peripheral controller communities with each community supporting four peripheral controllers. Therefore, 16 peripheral devices can be supported by an IOP. IOP 0 and IOP 1 are exceptions. IOP 0 and IOP 1 each support up to 15 Peripheral Controller (PC) slots. IOP 2 and IOP 3 each support up to 16 PC slots. The equipage of SCSI Peripheral Units (SPUs) like the UN375 SCSI Disk circuit packs in the Processor Unit reduces the number of available PC slots. Therefore, the maximum number of available PC slots in a Processor Unit is 15 with the UN375s. The equipage of each growth SPU reduces the number of available PC slots by 2.

For IOP 0 and IOP 1, Peripheral Community 0, slot 0 (PC00) is always equipped with a TN983, UN583, or UN597 MTTY Controller circuit pack. Also, IOP 0 and IOP 1, Peripheral Community 0, slot 2 (PC02) is reserved for a UN33D or UN933 Scanner and Signal Distributor circuit pack.

7.2.2 IOP Unit Functions

An IOP is a front-end processor for low- and medium-speed I/O peripheral units. Such units include asynchronous terminals, asynchronous data links, synchronous data links, and point scanner/signal distributors. The maintenance receive-only printer (ROP), maintenance teletypewriter/terminal (MTTY), and maintenance data link are examples of these units. The IOP provides an intermediate level of I/O processing between the CU and the various I/O PCs to handle low-level I/O processing. The IOP performs the following intermediate-level functions:

- Distributes I/O commands from the CU to the peripheral controllers
- Collects and batches responses from the peripheral controllers to the CU
- Concentrates interrupts from the peripheral controllers, thus off-loading a significant processing burden from the CU
- Performs low-level mediation for the peripheral controllers with the Direct Memory Access Controller (DMAC) for the transfer of commands, responses, and data to/from the Main Store
- Monitors and reports the operational status of the peripheral controllers to the CU
- Isolates defective/babbling peripheral controllers to prevent them from affecting the performance of other peripheral controllers
- Sets the operational status (in service or out of service) of the peripheral controllers on command from the CU.

Figure 7-2 is a functional block diagram of the IOP circuit pack (KBN10). The IOP consists of the following functional blocks:

- Duplex Dual Serial Bus Selector (DDSBS)
- Bus Interface Controller (BIC)
- Peripheral Interface Controller (PIC)
- Input/Output Microprocessor Interface (IOMI).

Each of these functional areas is described in the following sections.

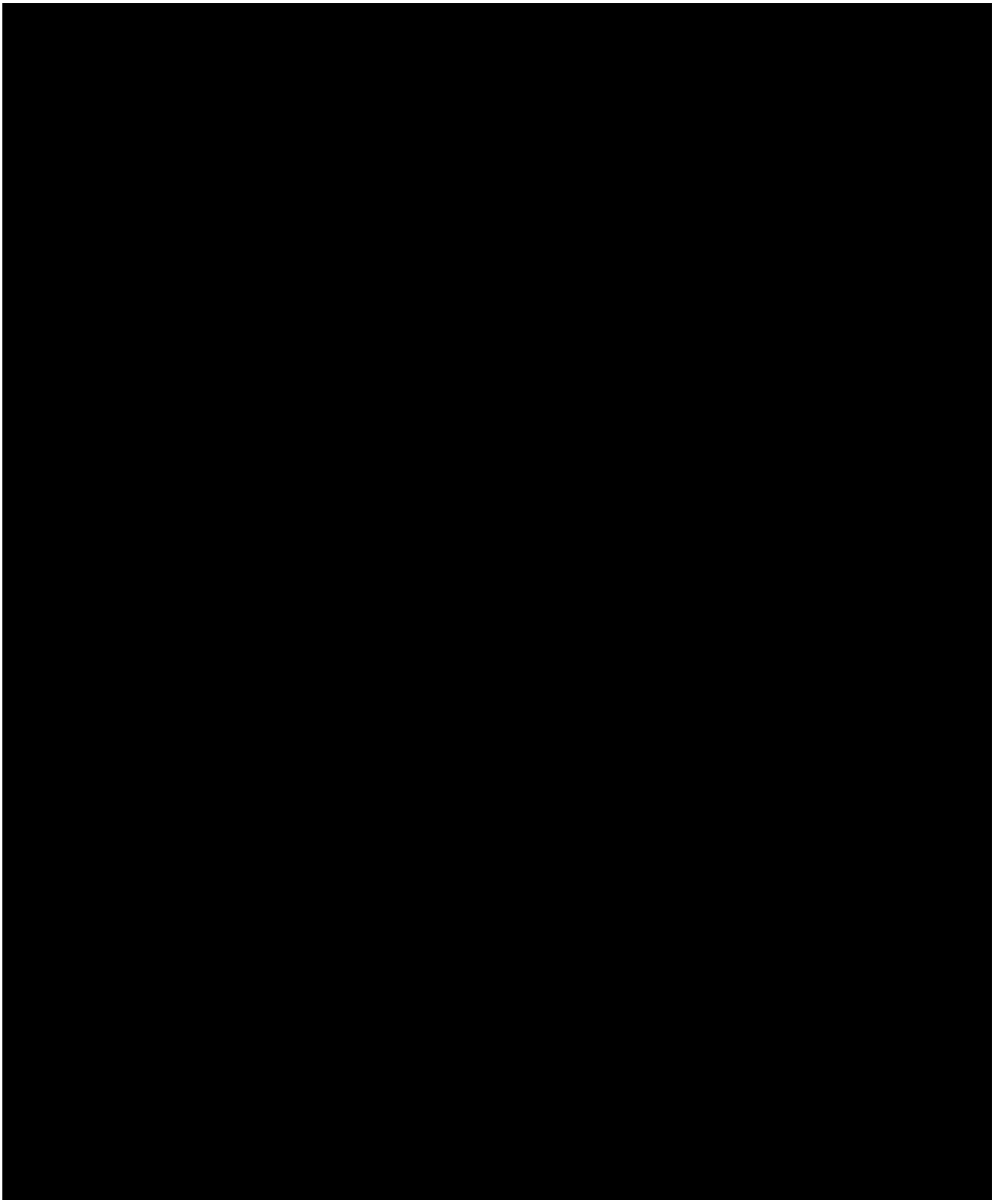


Figure 7-2 Input/Output Processor Functional Block Diagram

7.2.3 Duplex Dual Serial Bus Selector (DDSBS)

The Duplex Dual Serial Bus Selector (DDSBS) connects to two Dual Serial Channels (DSCH) (one from each side of the duplex processor). This allows both CUs of the processor to access the IOP. The functions of a DDSBS are as follows:

- To select which DSCH can currently communicate with the peripheral device.
- To convert between the dual serial bit-stream protocol used by the DSCH to the 36-bit (32 data and 4 parity) format used by the peripheral device's BIC.
- To provide maintenance functions such as request generation and data loop-around for diagnostic testing.

7.2.4 Bus Interface Controller (BIC)

The Bus Interface Controller (BIC) provides an interface between the DDSBS and the Peripheral Interface Controller (PIC). The specific functions of the BIC are as follows:

- To translate between the 36-bit (32 data and 4 parity bits) data format used by the DDSBS and the 18-bit (16 data and 2 parity bits) format used by the PIC.
- To buffer data passing between the IOP peripherals and the DDSBS.
- To provide logic that allows the device to send DMA setup requests, DMA transfer requests, and interrupt requests to the DMAC.
- To monitor and report error conditions.

7.2.5 Peripheral Interface Controller (PIC)

The Peripheral Interface Controller (PIC) is the central processing unit of the IOP, which allows the IOP to run independently from the CU. The specific functions of the PIC are as follows:

- To provide the MicroControl Store (MCS) that holds the IOP software
- To control data transfers between the IOP peripherals and the BIC
- To read and write all IOP memory and registers
- To handle interrupts.

7.2.6 Input/Output Microprocessor Interface (IOMI)

The Input/Output Microprocessor Interface (IOMI) connects the PIC with up to four communities of peripheral controllers (PCs). Each PC community can contain up to four PCs. The functions of the IOMI are as follows:

- Act as an interface between the 16-bit PIC and the 8-bit PCs.
- Provide a mechanism for the PIC to select which PC to service.

Each Peripheral Controller (PC) communicates with the IOMI via three request leads (error, interrupt, and service), a control signal acknowledge lead, and a PC select lead. Each community of four PCs share an 8-bit plus 1 parity bit data bus, a 16-bit memory address bus, and an 8-bit bus containing control signals.

To communicate with a PC, the IOP performs a DMA operation, which loads information into a dual-port memory (DPM) located on the PC. The IOP uses the PC select register to choose which PC to communicate with. Only the PC that is selected responds to the information loaded in the other registers. The DPM address that the IOP wants to access is loaded into the Microprocessor Memory Address (MPMADD) counter. A demultiplexer controlled by the PC select register routes this 16-bit address to the

appropriate PC.

For DPM write operations, the first 16 bits of data to be transferred to the PC are loaded into the Microprocessor Data (MPDATA) Register. Again, the PC select register routes the data to the proper PC. While the IOP interface to PC select register is a 16-bit interface, the PC side is only 8 bits wide. Therefore, the IOP can load the PC select register in one access; however, two accesses must be made to send this information to the PCs.

For read operations, the information from the PC is loaded into the MPDATA Register in two 8-bit operations. Then the IOP can read 16-bits at a time.

The IOP controls the DMA operation by asserting bits in the PC Control Register. Some of these control register bits are used to control events on the IOP itself, such as incrementing or decrementing the MPMADD counter, or determining whether the high byte or low byte of the data in the MPDATA register is being read or written. Eight of the signals form a control bus that is sent to the selected PC. In return (Response), the IOP receive four signals from each PC.

Table 7-1 summarizes the IOMI bus signals. The *X* in the signal names is the PC community designator and is 0, 1, 2, or 3.

Table 7-1 Input/Output Microprocessor Interface (IOMI) Bus

CATEGORY	SIGNAL	TYPE	DESCRIPTION	IOP	PC
DATA	DMAD*X*(7-0)1	Tristate Bidirec-	8 data bits, noninverted	I/O	I/O
	DMAD*X*81	tional	Data parity bit for 8 data bits	I/O	I/O
ADDRESS	DMA*X*(15-00)1	Unidirec- tional	16-bit memory address	OUT	IN
SELECT	PCSEL*X*(3-0)0	Unidirec- tional	PC select (one per PC)	OUT	IN
CONTROL	CINT*X*0	Unidirec- tional	Command Interrupt	OUT	IN
	CLRPC*X*0		Clear PC	OUT	IN
	DMAOC*X*0		DMA Operation Complete	OUT	IN
	DMARQ*X*0		DMA Request	OUT	IN
	DMAWR*X*0		DMS Write	OUT	IN
	RISL8*X*0		Reset PC Isolate	OUT	IN
	SISL8*X*0		Set PC Isolate	OUT	IN
RESPONSE	CSA*X*(3-0)0		4-Bit Control Signal Acknowledge (one per PC)	IN	OUT
	ER*X*(3-0)0		Error Detected (one per PC)	IN	OUT
	INT*X*(3-0)0		Interrupt Request (one per PC)	IN	OUT
	SR*X*(3-0)0		Service Request (one per PC)	IN	OUT

7.2.7 Boundary Scan Interface

The Boundary Scan (BS) interface to the IOP circuit pack is via the secondary BS bus when equipped in the Processor Unit and is via the growth boundary scan cable when equipped in the Growth Unit. The BS bus is a serial bus used to test (diagnose) components. All boundary scan functions are controlled by the CC.

7.3 PERIPHERAL CONTROLLERS (PC)

The 3B21D computer supports the following peripheral controllers:

- TN74B TTY Peripheral Controller
- TN75C Synchronous Link Peripheral Controller

- TN82B X.25 Synchronous Data Link Peripheral Controller
- TN983, UN583, or UN597 Maintenance TTY Peripheral Controller [The UN583 is a Multipurpose Peripheral Controller (MPC) that can be used to replace the TN983 and TN83B peripheral controllers.]
- TN1420 X.25 Synchronous Data Link Peripheral Controller
- TN1839 Synchronous Data Link Peripheral Controller X.25 Network Level 2 Interface (NET2)
- UN33D or UN933 Scanner and Signal Distributor Controller.
- UN582 MPC Can be used to replace the TN74B, TN75C, TN82B, and TN1839 circuit packs at a reduced cost per port.

7.3.1 TN74B Terminal Controller

The TN74B circuit pack is an asynchronous terminal controller that provides two EIA RS-232C channels operating at 300, 1200, 2400, 4800, and 9600 bps. It is used to provide data communication between the computer and a wide variety of asynchronous serial communications equipment.

The data throughput capabilities of the TN74 are shown in Tables 7-2 , 7-3 , and 7-4 .

Table 7-2 TN74B Interactive Terminal (Cooked Mode) Channel Output

ACTIVE CHANNELS	CHANNEL 1 BAUD RATE	CHANNEL 2 BAUD RATE	CHARACTERS PER SECOND	
			PER CHANNEL	PER CONTROLLER
1	9600		960	960
2	9600	9600	930	1860

Table 7-3 TN74B Interactive Terminal (Cooked Mode) Channel Input/Output

ACTIVE CHANNELS	CHANNEL 1 BAUD RATE	CHANNEL 2 BAUD RATE	CHARACTERS PER SECOND [a]	
			PER CHANNEL (Input+Output)	PER CONTROLLER
2	9600	9600	5+837	1684
2	1200	1200	5+120	250

Notes:

a. Typical typist input rate is 5 characters per second.

Table 7-4 TN74B Computer-to-Computer (Raw Mode) Channel Input/Output

ACTIVE CHANNELS	CHANNEL 1 BAUD RATE	CHANNEL 2 BAUD RATE	CHARACTERS PER SECOND	
			PER CHANNEL (Input+Output)	PER CONTROLLER (Maximum)
1	9600		960+0	960
2		9600	0+960	960
2	4800	4800	480+480	960

7.3.2 TN75C Synchronous Data Link Controller

The TN75C circuit pack provides two independent X.25 level 2 interfaces (channel 0 and channel 1), with automatic dial-out on channel 0. It is used to provide interfaces to packet switching networks, personal computers, or machine-to-machine links via dialup, private, or leased lines. The TN75C is compatible with EIA RS-232C and EIA RS-449 modems. The TN75C operates at 9600 bps, full duplex. Typical configurations are one channel operating at 9600 bps or two channels operating at 4800 bps.

It handles Byte-Control Protocol (BCP) such as Digital Data Communication Message Protocol (DDCMP), and bit-oriented protocols such as Synchronous Data Link Control (SDLC), High-Level Data Link Control

(HDLC), and Advanced Data Communications Control Procedures (ADCCP).

7.3.3 TN82B X.25 Synchronous Data Link Controller

The TN82B circuit pack provides a single, high-speed serial data link that implements the X.25 level 2 protocol. It is used to provide a high-performance interface to packet switching networks or machine to machine links via dialup, private, or leased lines. The TN82B is compatible with EIA RS-232C, EIA RS-449, and CCITT V.35 modems.

It handles bit-oriented protocols such as SDLC, HDLC, and ADCCP. The channel provides the necessary control signals that meet the EIA RS-232C interface standard for data rates up to 19.2 Kbps and CCITT V.35 interface for 20 Kbps and up to a maximum of 64 Kbps. The TN82B circuit pack can operate as one 64-Kbps, full duplex, data link channel.

7.3.4 TN983, UN583, or UN597 Maintenance TTY (MTTY) Controller

PC00 is reserved for a TN983, UN583, or UN597 Maintenance TTY Controller (MTTYC) in IOP 0 and IOP 1. See Figure 7-3 . The TN983/UN583/UN597 circuit pack provides RS-232C and RS-422 interfaces to monitor and control the 3B21D computer as follows:

- One RS-232C asynchronous input/output channel used for a local operator terminal and one synchronous port for remote operator terminals. The local operator terminal is the MTTY.
- One RS-232C input/output channel used for the local Receive-Only Printer (ROP).
- Two RS-422 input/output channels that are switchable to one universal asynchronous receiver-transmitter for communication with the Emergency Action Interface (EAI).

The local ROP and MTTY are automatically or manually switched to the appropriate TN983, UN583, or UN597 circuit pack input/output channel via the UN377 Port Switch and Scanner-Distributor Buffer circuit pack. The local ROP and MTTY cables are the same but with different equipment locations (EQLs).

The TN983, UN583, and UN597 circuit packs have different Emergency Action Interface cables going to or from the Central Control circuit pack (KLW31). Also, the TN983/UN583/UN597 circuit packs have the same EQLs, which are 19-094 for IOP 0 and 45-094 for IOP 1.

CAUTION: All backplanes shipped with UN583s or UN597s have two pins, located at EQLs 19-094-022 and 45-094-022, that must be isolated for the UN583/UN597 to operate. If you are retrofitting a UN583 or UN597 in place of a TN983 on an older backplane, make sure these two pins are isolated. The UN583/UN597 will not operate if these two pins are not isolated.

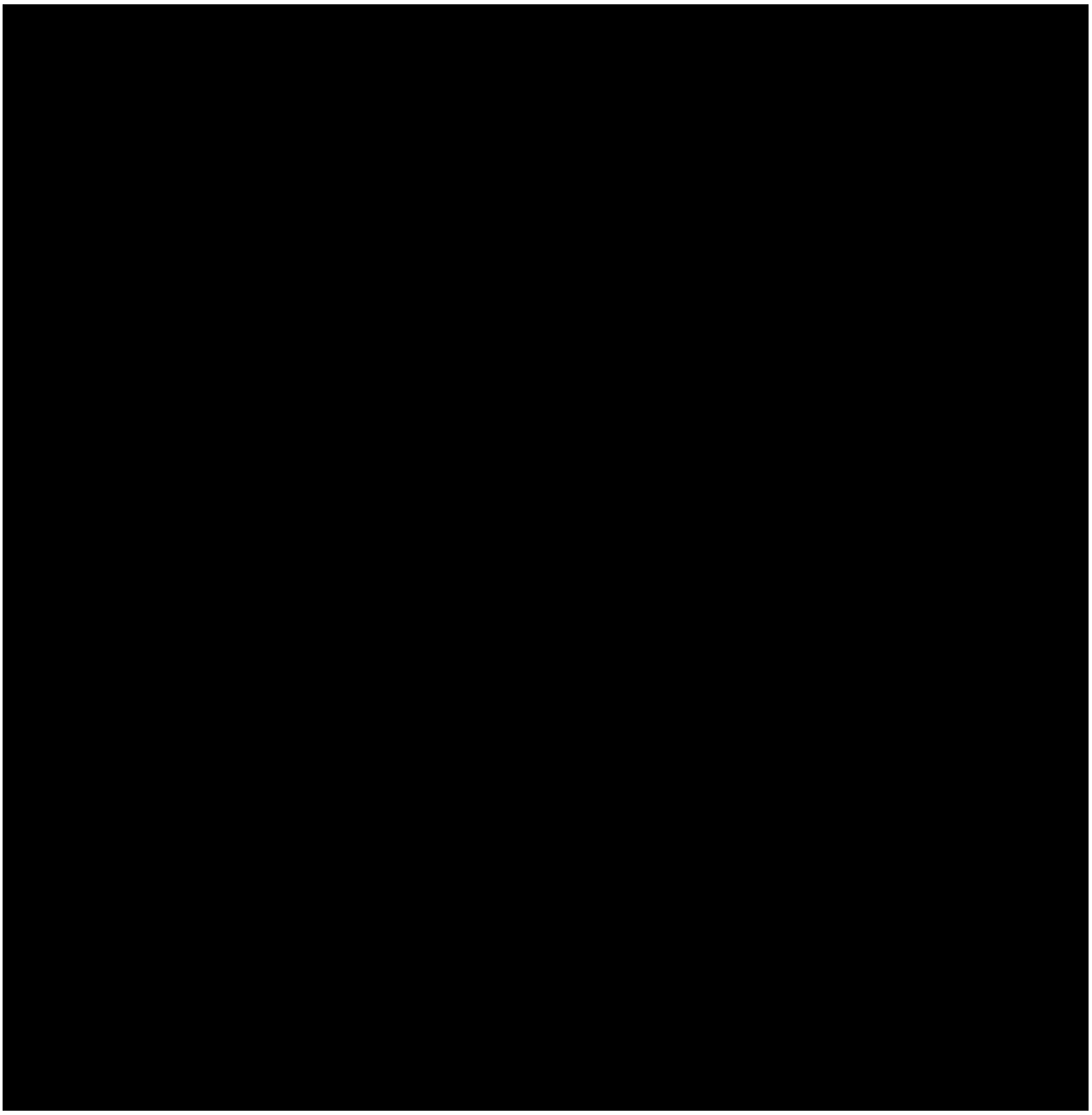


Figure 7-3 TN983/UN583/UN597 Maintenance TTY Controller Circuit Pack Functional Block Diagram

7.3.5 TN1420 X.25 Synchronous Data Link Controller

The TN1420 circuit pack provides a single, high-speed serial data link that implements the X.25 level 2 protocol. It is used to provide a high-performance interface to packet switching networks or machine-to-machine links via dialup, private, or leased lines. The TN1420 is compatible with EIA G.703 and CCITT V.36 modems.

It handles bit-oriented protocols such as SDLC, HDLC, and ADCCP. The channel provides the necessary control signals that meet the EIA RS-232C interface standard for data rates up to 19.2 Kbps and CCITT V.36 interface for 20 Kbps and up to a maximum of 64 Kbps. The TN1420 circuit pack can operate as one 64 Kbps, full duplex, data link channel.

7.3.6 TN1839 Synchronous Link Peripheral Controller□NET2

The TN1839 circuit pack is similar to the TN75 circuit pack, but the TN1839 circuit pack meets the NET2 requirements. The TN1839 circuit pack provides two independent X.25 level 2 interfaces (channel 0 and channel 1), with automatic dial-out on channel 0. It is used to provide interfaces to packet switching networks, personal computers, or machine-to-machine links via dialup, private, or leased lines. The TN1839 is compatible with EIA RS-232C and EIA RS-449 modems. The TN1839 operates at 9600 bps, full duplex. Typical configurations are one channel operating at 9600 bps or two channels operating at 4800 bps.

It handles Byte-Control Protocol (BCP) such as Digital Data Communication Message Protocol (DDCMP), and bit-oriented protocols such as SDLC, HDLC, and ADCCP.

7.3.7 UN582, UN583, and UN597 Multipurpose Peripheral Controller (MPC)

The MPC provides a common hardware platform to the 3B20D and 3B21D computer that reduces the cost per port and is a technology upgrade for peripheral controller. The UN582 and UN583 have similar hardware, but have different firmware resident in the nonvolatile memory, and are used as follows:

- UN583 or UN597 replaces the TN983 and TN83B peripheral controllers.
- UN582 replaces the TN74B, TN75C, TN1839, TN82, and TN82B peripheral controllers.
- UN582B replaces the UN582 and adds NET2 compliance to the V.28 and V.36 physical interfaces.

7.3.8 UN33 or UN933 Scanner and Signal Distributor Controller

7.3.8.1 Scan and Signal Distributor Point Characteristics

PC02 in IOP 0 and IOP 1 is reserved for a UN33D or UN933 Scanner and Signal Distributor (SCSD) circuit pack. IOP 0, PC02 is SCSD Controller 0 (SCSDC 0); IOP 1, PC02 is SCSD Controller 1 (SCSDC 1).

The UN33 or UN933 consists of circuitry for monitoring 48 scan (SC) points and controlling 32 signal distributor (SD) points (see Figure 7-4). A scan point is defined as an open pair of leads connected to a monitored current source on the UN33 or UN933.

The characteristics of the SC points are as follows:

- Each SC point is examined every 48 milliseconds, and the scan map (in the UN33 or UN933 circuit pack) is updated with any change.
- A point must remain in the new state for two scans (96 ms) for the change to be reported to the CU.

The characteristics of the SD points are as follows:

- SD points are activated by commands from the CU. Only one point at a time may be activated or deactivated.
- SD points can be directed by the CU to any of four states:
  - Operate
  - Clear
  - Flash continuously
  - Flash for 8 seconds, then terminate to the off state.

7.3.8.2 Scan and Signal Distributor Point Responses

The SC and SD points are connected to each unit of the 3B21D computer except the 9-track tape drive. The power switch circuits of the units all use SC and SD points and have similar responses. The following are the expected responses from the units:

- Any manual power up or power down results in a message.
- Any automatic power down results in an alarm and a message.
- Any nonpower down fault results in an alarm and a message.
- Switching the Request-Out-of-Service/Restore (ROS/RST) switch to ROS requests removal of the unit from service.
- The Request-In-Progress (RQIP) indicator is on when a request (either a remove or restore) is in progress. If a remove request is denied, the RQIP indicator is flashed several times and then extinguished. Remove and restore commands made from the unit do not operate the RQIP indicator.
- The Out-Of-Service (OOS) indicator is on when the unit is out of service.
- Switching the ROS/RST switch to RST requests a diagnostic and restoral of the unit to service.
- Diagnostics will not be run on power up if the ROS/RST switch is left in the ROS position.
- Switching the Alarm Cutoff-Test (ACO-T) switch to ACO-T and back again retires an alarm associated with the particular powered down unit.

NOTE: The other functions (MOR, indicator test, and the ROS indicator) do not interface with the SCSDC. The power switch on the KS-23909 9-track tape drive does not interface with the SC and SD points.

The UN377 circuit pack has six pairs of SC that reflect the state of the port switch. These SC points are as follows:

- SCA40 Closed when the UN377 circuit pack has power.
- SCB40 Closed if ROP output is from MTTYPC0.
- SCC40 Closed if ROP select switch is set to automatic (AUTO).
- SCA56 Closed when the UN377 has power.
- SCB56 Closed if MTTY output is from MTTYPC0. (Duplicates SCA40.)
- SCC56 Closed if MTTY select switch is set to AUTO.

One UN33D or UN933 circuit pack in each IOP has two pairs of SC points that report the status of the fuses for both processors. A blown fuse is indicated by a closed scan point.

Figure 7-4 UN33 or UN933 Scanner and Signal Distributor Circuit Pack Functional Block Diagram

7.3.8.3 Scan and Signal Distributor Point Assignments

Each SCSD circuit pack (UN33 or UN933) provides 48 SC points and 32 SD points. The basic 3B21D computer complex requires two base UN33 or UN933 circuit packs. One base UN33 or UN933 circuit pack is equipped in IOP 0, PC02; and the other base UN33 or UN933 circuit pack is equipped in IOP 1, PC02. The number of SC and SD points required for a basic 3B21D computer complex consisting of two CUs, four IOPs, two DFCs, six disks, one Digital Audio Tape (DAT), one MTTY, one ROP, a Bidirectional Cooling Unit, and a Fuse and Filter Unit is 42 SC points and 32 SD points. In addition, eight SD points (four SD points per base UN33 or UN933 circuit pack) are assigned for the software generated alarms (critical, major, minor, and retire functions). The following rules are used for assigning the scan and signal distributor points:

- Minimum of one SCSD circuit pack (UN33 or UN933) per IOP 0 and IOP 1.
- Duplicate SC and SD points (if required) must be assigned to the same points on the duplicate controllers.

- Scan groups, that is SC and SD points from one power switch, must be assigned to the same SCSDC (UN33 or UN933).
- SCSDC 0 is equipped in IOP 0, PC slot 02, and monitors the 3B21D computer equipment with even numbers, for example, CU 0, DFC 0, SPU 0, SPU 2, etc. SCSDC 1 is equipped in IOP 1, PC slot 02, and monitors the 3B21D computer equipment with odd numbers. The exceptions to this rule are IOP 0 and IOP 1, which are monitored from SCSDC 1 and SCSDC 0, respectively.
- Applications assign their equipment to the remaining SC and SD points and/or add additional SCSD packs (UN33 or UN933) if needed.

Table 7-5 lists the SC and SD points on SCSDC 0 and SCSDC 1 of the 3B21D computer for a small office. Table 7-6 lists the SC and SD points on SCSDC 0 and SCSDC 1 of the 3B21D computer for a large office. These tables show what points are assigned to a particular unit and their scan and/or signal distributor functions. The SC and SD point assignments *for an application* are noted in both tables. These table entries are ***not*** part of the 42 SC and 40 SD points required for the basic 3B21D computer complex, inclusive of the software-generated alarms.

Table 7-5 Small Office Scan and Signal Distributor Point Assignments

SC/SD	SCSDC 0 (IOP 0, PC02) EQL 19-110			SCSDC 1 (IOP 1, PC02) EQL 45-110		
POINT	UNIT	SC FUNCTION	SD FUNCTION	UNIT	SC FUNCTION	SD FUNCTION
00 **a**	CMU 0	Y(POWER)	OOS	CMU 0	Y(POWER)	OOS
01 **a**	CMU 0	X(ROS/RST)	RQIP	CMU 0	X(ROS/RST)	RQIP
02 **a**	CMU 0	W( )	DIAGNOSTICS	CMU 0	W( )	DIAGNOSTICS
03 **a**	CMU 0	V( )		CMU 0	V( )	
03 **a**	NCLK 0		OOS	NCLK 0		OOS
04 **a**	CMU 1	Y(POWER)	OOS	CMU 1	Y(POWER)	OOS
05 **a**	CMU 1	X(ROS/RST)	RQIP	CMU 1	X(ROS/RST)	RQIP
06 **a**	CMU 1	W( )	DIAGNOSTICS	CMU 1	W( )	DIAGNOSTICS
07 **a**	CMU 1	V( )		CMU 1	V( )	
07 **a**	NCLK 1		OOS	NCLK 1		OOS
08	3B FAN	FAN	RESET	3B FAN	FAN	RESET
09	**b**	**b**	**b**	**b**	**b**	**b**
10 **a**	MISC FAN	FAN	RESET	MISC FAN	FAN	RESET
11	**b**	**b**	**b**	**b**	**b**	**b**
12	ALARM	**b**	CRITICAL	ALARM	**b**	CRITICAL
13	ALARM	**b**	MAJOR	ALARM	**b**	MAJOR
14	ALARM	**b**	MINOR	ALARM	**b**	MINOR
15	ALARM	**b**	RETIRE	ALARM	**b**	RETIRE
16				SPU 54	X(ROS/RST)	OOS
17				SPU 54	Y(POWER)	RQIP
18	SPU 04	X(ROS/RST)	OOS	SPU 05	X(ROS/RST)	OOS
19	SPU 04	Y(POWER)	RQIP	SPU 05	Y(POWER)	RQIP
20	IOP 2	Y(POWER)	OOS	IOP 3	Y(POWER)	OOS
21	IOP 2	X(ROS/RST)	RQIP	IOP 3	X(ROS/RST)	RQIP
22	IOP 1	Y(POWER)	OOS	IOP 0	Y(POWER)	OOS
23	IOP 1	X(ROS/RST)	RQIP	IOP 0	X(ROS/RST)	RQIP
24	SPU 02	X(ROS/RST)	OOS	SPU 03	X(ROS/RST)	OOS
25	SPU 02	Y(POWER)	RQIP	SPU 03	Y(POWER)	RQIP
26	SPU 00	X(ROS/RST)	OOS	SPU 01	X(ROS/RST)	OOS
27	SPU 00	Y(POWER)	RQIP	SPU 01	Y(POWER)	RQIP
28	DFC 0	X(ROS/RST)	OOS	DFC 1	X(ROS/RST)	OOS
29	DFC 0	Y(POWER)	RQIP	DFC 1	Y(POWER)	RQIP
30	CU 0	Y(POWER)	OOS	CU 1	Y(POWER)	OOS
31	CU 0	X(ROS/RST)	RQIP	CU 1	X(ROS/RST)	RQIP
32 **a**	NCLK 0	Y(POWER)	**c**	NCLK 0	Y(POWER)	**c**
33 **a**	NCLK 0	X(ROS/RST)	**c**	NCLK 0	X(ROS/RST)	**c**
34 **a**	NCLK 1	Y(POWER)	**c**	NCLK 1	Y(POWER)	**c**
35 **a**	NCLK 1	X(ROS/RST)	**c**	NCLK 1	X(ROS/RST)	**c**

36 **a**	ESM POWER	CRITICAL ALARM	**c**	ESM POWER	CRITICAL ALARM	**c**
37 **a**	ESM POWER	MAJOR ALARM	**c**	ESM POWER	MAJOR ALARM	**c**
38 **a**	MISC FA	FA 1	**c**	MISC FA	FA 1	**c**
39 **a**	MISC FA	FA 0	**c**	MISC FA	FA 0	**c**
40	ROP	C(PTSW)	**c**			**c**
41	ROP	B(PTSW)	**c**			**c**
42	IOP 1	Z(FUSE)	**c**	IOP 0	Z(FUSE)	**c**
43	ROP	A(PTSW)	**c**	**b**	**b**	**c**
44	MTTY	C(PTSW)	**c**			**c**
45	MTTY	B(PTSW)	**c**			**c**
46	CU 0	Z(FUSE)	**c**	CU 1	Z(FUSE)	**c**
47	MTTY	A(PTSW)	**c**	**b**	**b**	**c**

Notes:

a. SC and SD point assignments for an application.

b. Inaccessible.

c. SD points 32 through 47 do not exist. (SD points are 00 through 31.)

Table 7-6 Large Office Scan and Signal Distributor Point Assignments

SC/SD POINT	SCSDC 0 (IOP 0, PC02) EQL 19-110			SCSDC 1 (IOP 1, PC02) EQL 45-110		
	UNIT	SC FUNCTION	SD FUNCTION	UNIT	SC FUNCTION	SD FUNCTION
00 **a**	3B GROWTH FAN	FAN	RESET	3B GROWTH FAN	FAN	RESET
01			**b**			**b**
02						
03						
04						
05						
06						
07						
08	3B FAN	FAN	RESET	3B FAN	FAN	RESET
09	**b**	**b**	**b**	**b**	**b**	**b**
10 **a**	MISC FAN	FAN	RESET	MISC FAN	FAN	RESET
11			**b**			**b**
12	ALARM	**b**	CRITICAL	ALARM	**b**	CRITICAL
13	ALARM	**b**	MAJOR	ALARM	**b**	MAJOR
14	ALARM	**b**	MINOR	ALARM	**b**	MINOR
15	ALARM	**b**	RETIRE	ALARM	**b**	RETIRE
16				SPU 54	X (ROS/RST)	OOS
17				SPU 54	Y (POWER)	RQIP
18	SPU 04	X (ROS/RST)	OOS	SPU 05	X (ROS/RST)	OOS
19	SPU 04	Y (POWER)	RQIP	SPU 05	Y (POWER)	RQIP
20	IOP 2	Y (POWER)	OOS	IOP 3	Y (POWER)	OOS
21	IOP 2	X (ROS/RST)	RQIP	IOP 3	X (ROS/RST)	RQIP
22	IOP 1	Y (POWER)	OOS	IOP 0	Y (POWER)	OOS
23	IOP 1	X (ROS/RST)	RQIP	IOP 0	X (ROS/RST)	RQIP
24	SPU 02	X (ROS/RST)	OOS	SPU 03	X (ROS/RST)	OOS
25	SPU 02	Y (POWER)	RQIP	SPU 03	Y (POWER)	RQIP
26	SPU 00	X (ROS/RST)	OOS	SPU 01	X (ROS/RST)	OOS
27	SPU 00	Y (POWER)	RQIP	SPU 01	Y (POWER)	RQIP
28	DFC 0	X (ROS/RST)	OOS	DFC 1	X (ROS/RST)	OOS
29	DFC 0	Y (POWER)	RQIP	DFC 1	Y (POWER)	RQIP
30	CU 0	Y (POWER)	OOS	CU 1	Y (POWER)	OOS
31	CU 0	X (ROS/RST)	RQIP	CU 1	X (ROS/RST)	RQIP
32	**b**	**b**	**c**	**b**	**b**	**c**
33 **a**	3B GROWTH FA	FA	**c**	3B GROWTH FA	FA	**c**
34			**c**			**c**

35			**c**			**c**
36			**c**			**c**
37			**c**			**c**
38 **a**	MISC FA	FA 1	**c**	MISC FA	FA 1	**c**
39 **a**	MISC FA	FA 0	**c**	MISC FA	FA 0	**c**
40	ROP	C (PTSW)	**c**			**c**
41	ROP	B (PTSW)	**c**			**c**
42	IOP 1	Z (FUSE)	**c**	IOP 0	Z (FUSE)	**c**
43	ROP	A (PTSW)	**c**	**b**	**b**	**c**
44	MTTY	C (PTSW)	**c**			**c**
45	MTTY	B (PTSW)	**c**			**c**
46	CU 0	Z (FUSE)	**c**	CU 1	Z (FUSE)	**c**
47	MTTY	A (PTSW)	**c**	**b**	**b**	**c**

Notes:

a. SC and SD point assignments for an application.

b. Inaccessible.

c. SD points 32 through 47 do not exist. (SD points are 00 through 31.)

7.3.8.4 Verifying SCSD Operation

To verify the operation of either the scan points or the distributor points, manual action is required. To verify SCSD operations, follow the procedures in the following paragraphs.

7.3.8.4.1 Verifying Scan Point Status

Operation of the scanner portion of the SCSD is controlled by the following messages:

- **OP:SCSD** – Reports the inhibit status and the state of the scan points on the SCSD.
- **INH:SCSD** – Inhibits the reporting of transitions of a scan point on the SCSD.
- **ALW:SCSD** – Allows the reporting of transitions of a scan point on the SCSD.

Obtain physical scan point assignments from schematic drawings or office records. The physical and logical assignments of scan points are recorded in the Equipment Configuration Data (ECD) and can be accessed via the recent change and verify (RC/V) mechanism. To determine logical and physical scan point assignments using the RC/V mechanism, use the following procedure.

(1) At the recent change terminal, enter the following:

- PDS **RCV:MENU:RCVECD,DB "root",NREVIEW!**
- MML **RCV:MENU:DATA,RCVECD,DB="root",NREVIEW;**

System displays the "UNIX RTR RCV (ODIN)-DATA ENTRY" page.

(2) Enter: Form name **klist**

(3) Enter: In block number 1, a temporary file name, for example, **/tmp/scsd**

(4) Enter: **n** in all blocks except *scsdbody*.

(5) At *scsdbody*, enter: **y**

(6) In the field at the lower right corner, enter: **e**

(7) At the maintenance terminal, enter:

- PDS **DUMP:FILE:ALL,FN"/tmp/scsd"!**
- MML **DUMP:FILE:DATA,ALL,FN="tmp/scsd";**

The contents of the file */tmp/scsd* are printed. A list of the SCSD option names and logical names make up the contents.

(8) Enter: *form name*, for example, **scsdbody**

(9) Enter: *option name*, for example, **scsdopt0**

(10) Enter: *scsdname* (logical group name).

The remainder of the form is populated. Column 9 contains scan point assignments and column 11 contains SD point assignments.

7.3.8.4.2 Verifying SD Point Operation

To verify the operation of an SD point, the selected point must be identified by either physical or logical assignment. The method of identification is the same as was used to identify scan point assignments.

Once identified, the SD points can be placed in any of four states using the **ORD:SCSD** input message. The four states are as follows:

- OPERATE set
- RELEASE clear
- STEP flash for 8 seconds
- REPEAT flash continuously.

To verify operation of the selected SD point, use the **ORD:SCSD** message to flash the point while observing the state of associated lamps and indicators.

Typical SD Point Verification Example

Verify the operation of the SDD points on MHD 0 as follows:

(1) Identify SD point assignment. From the office records, MHD 0 SD points are assigned as follows:

- MDG 0 Lead OS is a member number 0, SD point 18.
- MHD 0 Lead RQIP is member number 0, SD point 19.

(2) Using information from the previous step, enter the following command:

- PDS **ORD:SCSD;UNIT 0: PT 18, OPR STEP!**
- MML **ORD:SCSD; UNIT=0: DATA,PT=18,OPR=STEP;**

(3) At MDG 0, observe the Other Store (OS) lamp. If the SD point is operating, the lamp will flash for 8 seconds.

(4) Repeat using the data associated with lead RQIP.

7.3.8.4.3 Troubleshooting the SCSD

You should have access to the SCSD assignments and should be familiar with using the **OP:SCSD** and **ORD:SCSD** commands.

SCSD diagnostics test the circuitry on the pack but do not loop through the outside connections. For problems with single scan points, the point should be manually operated. The transition of the point can then be verified with the **OP:SCSD** command. A problem with a single signal distributor point can be investigated using the **ORD:SCSD** command. The operation of all lamps can be tested with the ACO-T switch on the power switch (TN2, TN3, TN5, and TN6).

7.4 PORT SWITCH AND SCANNER-DISTRIBUTOR BUFFER (PSSDB)

The Port Switch and Scanner-Distributor Buffer (PSSDB) circuit pack (UN377) performs the following functions:

- Switches the maintenance terminal (MTTY) and the local printer (ROP) between the TN983, UN583, or UN597 Maintenance TTY Controller (MTTYC) in IOP 0 and the TN983, UN583, or UN597 MTTYC in IOP 1.
- Buffers the scanner and signal distributor controller (SCSDC) from non-3B21D computer circuits, such as office alarms, smoke detectors, door access mechanisms, etc.

NOTE: The terms "Maintenance Terminal," "Maintenance Teletypewriter," and "Maintenance TTY (MTTY)" refer to the same type of terminal.

Figure 7-5 shows the PSSDB circuit pack (UN377) interfaces.

7.4.1 MTTY and ROP Port Switching

The UN377 faceplate has a three-position rocker switch and two indicators for each peripheral device. The MTTY is controlled by the "A" switch; the ROP is controlled by the "B" switch. Figure 7-6 shows the layout of the UN377 circuit pack faceplate. Table 7-7 defines the UN377 switch positions. Table 7-8 defines the UN377 indicators.

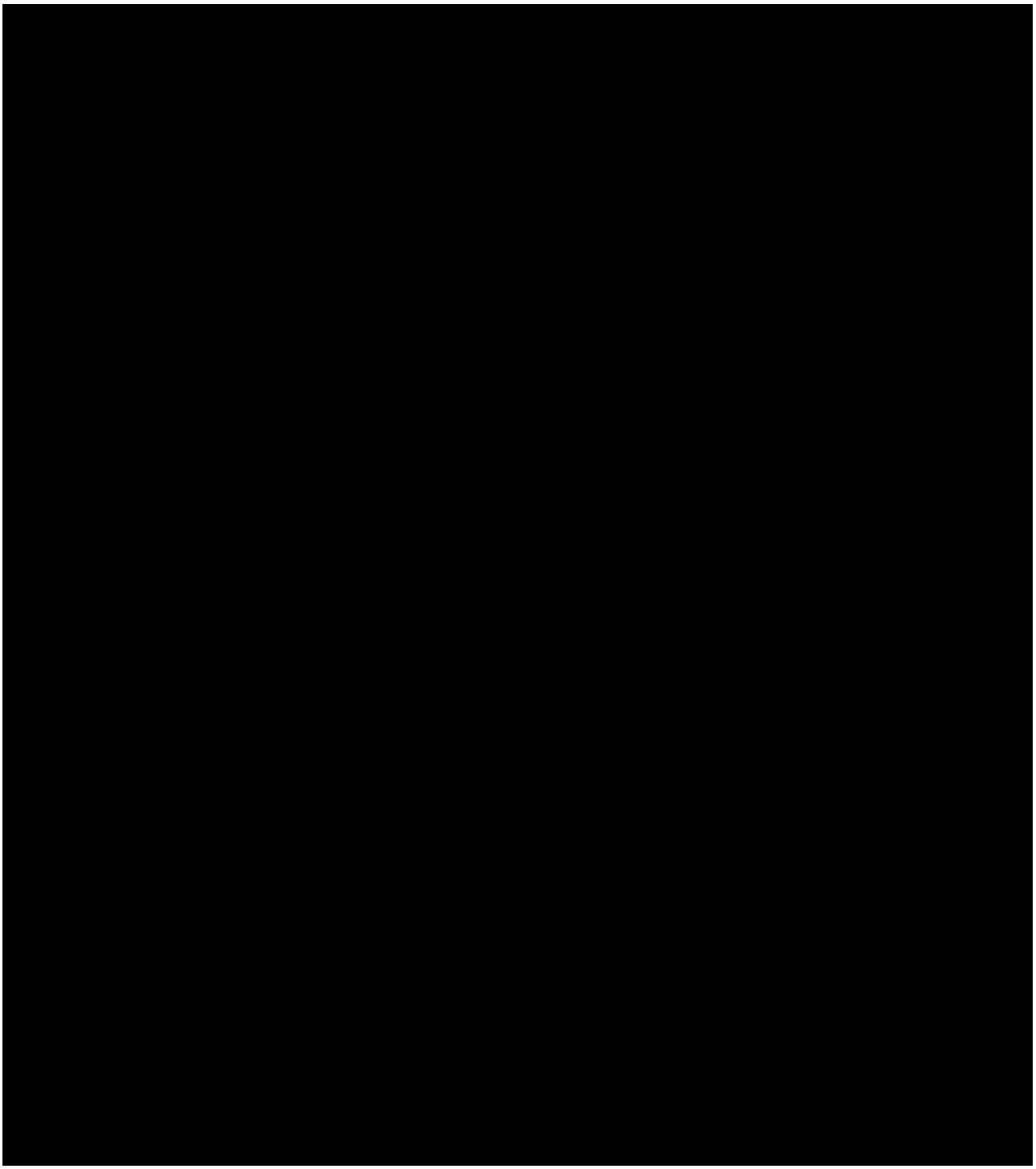


Figure 7-5 Port Switch and Scanner-Distributor Buffer (PSSDB) Functional Interface Diagram

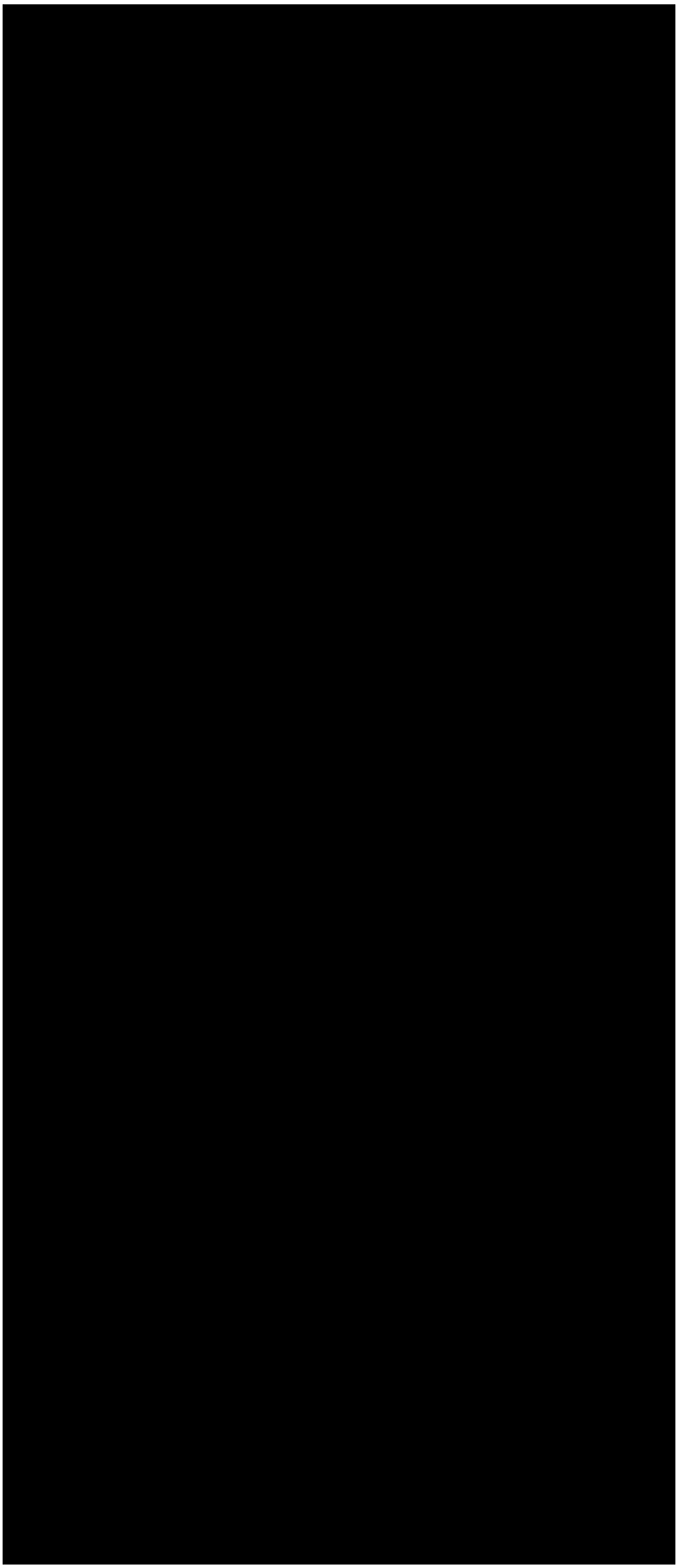


Figure 7-6 UN377 Circuit Pack Faceplate

Table 7-7 UN377 Circuit Pack Switch Functions

NAME	TYPE	FUNCTION
A	3-Position Rocker	"0" forces connection of Device A (MTTY) to PC00 in IOP 0. "1" forces connection of Device A (MTTY) to PC00 in IOP 1. "AUTO" defers selection to software generated DTR signals.
B	3-Position Rocker	"0" forces connection of Device B (ROP) to PC00 in IOP 0. "1" forces connection of Device B (ROP) to PC00 in IOP 1. "AUTO" defers selection to software generated DTR signals.

Table 7-8 UN377 Circuit Pack Indicators

POSITION	NAME	FUNCTION [a]
A	0 1	Lights when Device A (MTTY) is connected to PC00 in IOP 0. Lights when Device A (MTTY) is connected to PC00 in IOP 1.
B	0 1	Lights when Device B (ROP) is connected to PC00 in IOP 0. Lights when Device B (ROP) is connected to PC00 in IOP 1.
Notes: a. All four light-emitting diodes (LEDs) are green.		

7.4.2 Buffering

The UN377 circuit pack provides isolation between the 3B21D computer (UN33 circuit pack) and external circuits. Buffers (opto-isolators) are provided for 12 SC and 12 SD points.

An external circuit must provide a current through the UN377 scanner buffer of 5 mA to 20 mA for a logical 1; 0 mA for a logical 0. The SD buffers handle a current of 20 mA for an SD state of 1 and are protected by avalanche diodes rated at 68 V □5%.

7.4.3 UN377 Power

The UN377 circuit pack is supplied power from two sources. The Test Access Port (TAP) and SELF-ID circuits are supplied +5 V power from CONVC. The port switch circuits are supplied +5 V power from a Board-Mounted Power Module (BMPM). The BMPM is supplied -48 V from the Modular Fuse and Filter Unit. The UN377 includes a voltage monitor that checks the circuit pack +5 V power. When the +5 V power is out of range, the voltage monitor generates a power alarm.

8. STORAGE AND PERIPHERAL DEVICES

8.1 DEVICE OVERVIEW

This section describes the various Small Computer System Interface (SCSI) peripheral units and the other 3B21D computer peripheral devices.

The SCSI Peripheral Units (SPUs) provide Moving Head Disk (MHD) drive and Magnetic Tape (MT) drive capabilities for the 3B21D computer. Magnetic tape drives include Digital Audio Tape (DAT) and 9-track tape drives.

The other 3B21D computer peripheral devices include the Maintenance Terminal (MTTY) and Receive-Only Printer (ROP) that provide the principle operator interface for the computer.

The following storage and peripheral devices are described in this section:

- UN375/UN375E 3.5-Inch 1000-MB SCSI Hard Disk Drive (KS-23908) Circuit Packs
- UN376/UN376E 3.5-Inch SCSI DAT Cartridge Tape Drive (NCR006-3503341) Circuit Packs
  - NCR006-3503341 (UN376)
  - NCR006-3300608/Comcode 407545243 (UN376C)
  - KS-24367,L1/Comcode 40771260 (UN376E)
- Optional 9-Track SCSI Tape Drive (KS-23909)
- Maintenance Terminal (KS-23996 Color Video Terminal)
- Receive-Only Printer (ROP).

8.2 UN375/UN375E 3.5-INCH 1000-MB SCSI HARD DISK DRIVE (KS-23908) CIRCUIT PACK

8.2.1 UN375/UN375E Physical Description

The UN375 circuit pack provides a board-mounted, 3.5-inch, differential SCSI hard disk drive with a formatted capacity of 1000 MB (where 1 MB is 10^6 bytes).

The UN375E circuit pack (KS-23908,L41/Comcode 407207762) provides a board-mounted, 3.5-inch, single-ended SCSI hard disk drive with a formatted capacity of 4 gigabytes.

NOTE: These hard disk drives are used as 1000-MB capacities.

Figure 8-1 shows the UN375/UN375E circuit pack faceplate controls and indicators. Figure 8-2 shows the power and SCSI connectors on the KS-23908 disk drive. The SCSI device address selection pin field is cabled to the SCSI ID selector pushbutton switch on the circuit pack faceplate.

The SCSI ID for the UN375/UN375E circuit pack is set to any available device address in the range of 0 to 6, inclusive, using the ID selector pushbutton switch; see Note. A device address (SCSI ID) is available if it does not conflict with any other device on the same SCSI bus; see ***Caution***. SCSI ID 7 is assigned to the SCSI Host Adapter and is not an available selection on the ID pushbutton switch.

NOTE: Set the SCSI ID for the UN375/UN375E circuit pack when the circuit pack is powered OFF. The SCSI ID will take effect when the circuit pack is powered ON.

CAUTION: Take extreme care to ensure that there are no SCSI ID conflicts. If two or more devices have

the same ID, the results are unpredictable.

Figure 8-3 shows the general layout of the UN375/UN375E circuit pack, the location of the SCSI power header, and differential and single-ended SCSI connectors (headers) on the UN375/UN375E circuit boards. Table 8-1 identifies the standard differential SCSI connector pins. Table 8-2 identifies the standard single-ended SCSI connector pins associated with the UN375 circuit pack.

The UN375/UN375E circuit pack uses three cables as follows:

- An SCSI power cable connects the SCSI power header (J3) on the circuit board and the disk drive DC power connector.
- For the UN375, an SCSI differential cable connects the differential SCSI header (J4) on the circuit board and the differential disk drive SCSI connector.

  For the UN375E, an SCSI single-ended cable connects the single-ended SCSI header (J4) on the circuit board and the single-ended disk drive SCSI connector.
- An SCSI identification cable connects the SCSI ID switch on the faceplate and the SCSI ID header on the disk drive.

  Note that different SCSI ID connectors are provided for the KS-23908,L20 disk drive and KS-23908,L10 disk drive SCSI ID headers as shown in Figure 8-3 . Only one of these SCSI ID connectors is used, depending on which disk drive is used in the circuit pack.

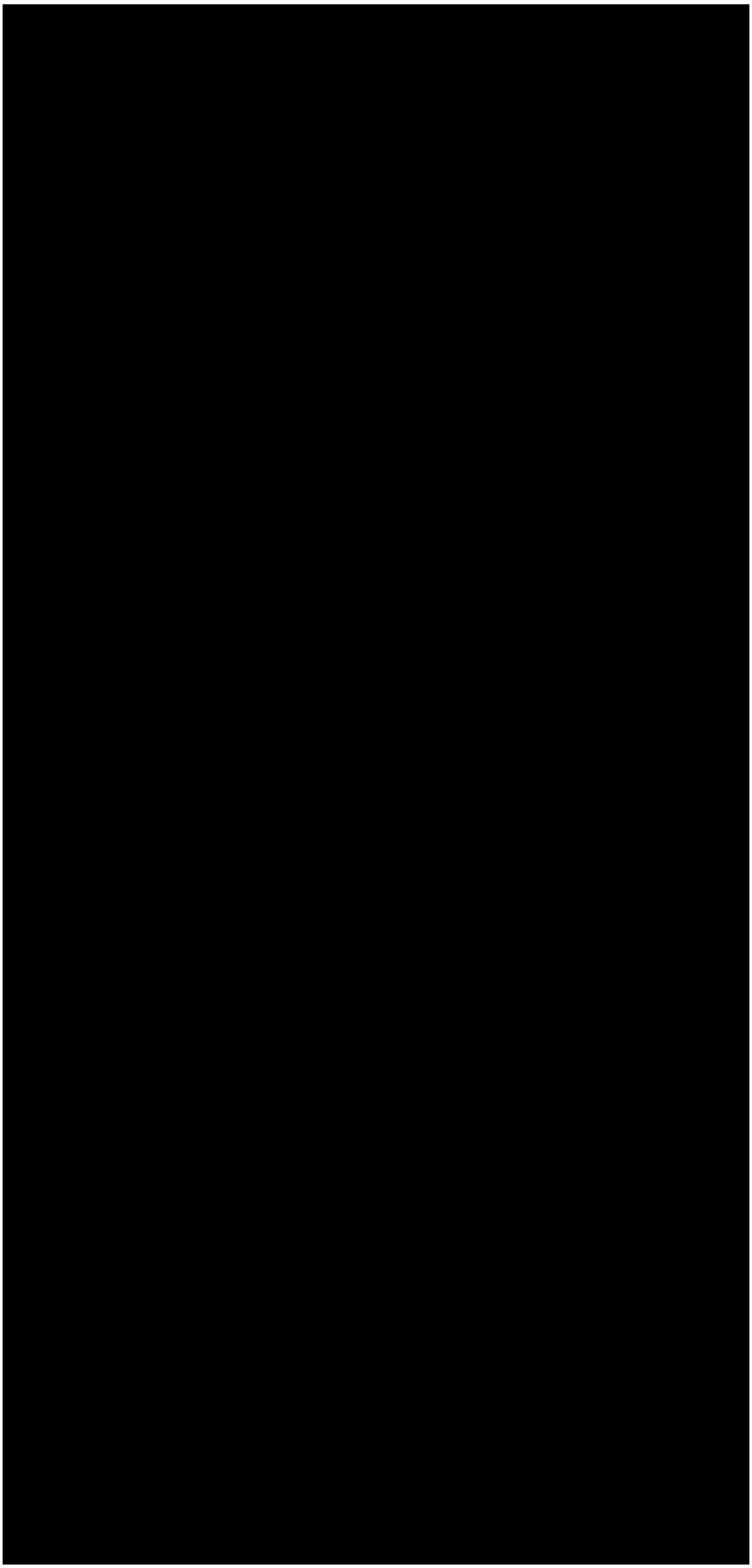


Figure 8-1 UN375/UN375E Circuit Pack Faceplate

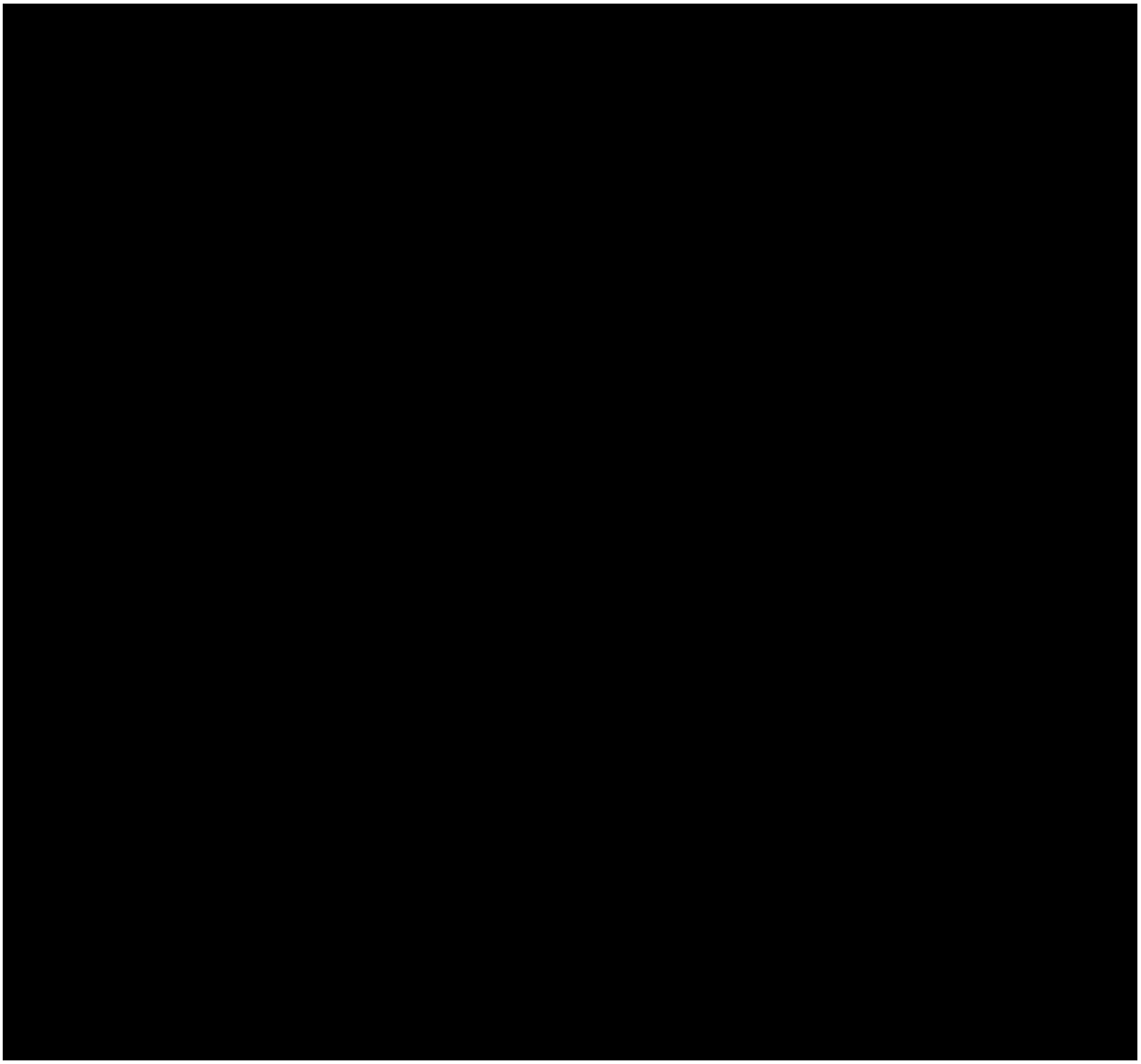


Figure 8-2 UN375/UN375E (KS-23908) 3.5-Inch Hard Disk Drive Rear View

Figure 8-3 UN375/UN375E Circuit Pack Layout

Table 8-1 Standard Differential SCSI Connector Pins

PIN	SIGNAL	FUNCTION
01	Shield Ground	Shield ground is optional for some cables.
02	Ground	
03, 04	+DB(0), -DB(0)	Positive and negative Data Bus bit 0.
05, 06	+DB(1), -DB(1)	Positive and negative Data Bus bit 1.
07, 08	+DB(2), -DB(2)	Positive and negative Data Bus bit 2.
09, 10	+DB(3), -DB(3)	Positive and negative Data Bus bit 3.
11, 12	+DB(4), -DB(4)	Positive and negative Data Bus bit 4.
13, 14	+DB(5), -DB(5)	Positive and negative Data Bus bit 5.
15, 16	+DB(6), -DB(6)	Positive and negative Data Bus bit 6.
17, 18	+DB(7), -DB(7)	Positive and negative Data Bus bit 7.
19, 20	+DB(P), -DB(P)	Positive and negative Data Bus parity bit. Parity is odd. The use of parity is a system option. The system is configured to either have all SCSI devices generate and detect parity or no devices generate and detect parity. Parity is not valid during the Arbitration phase.
21	+DIFFSENS	Positive Differential Sense.
22-24	Ground	
25, 26	TERMPWR	Optional terminator power is supplied through a backflow diode.
27, 28	Ground	
29, 30	+ATN, -ATN	Positive and negative Attention signal is driven by an initiator to indicate the Attention condition.
31, 32	Ground	
33, 34	+BSY, -BSY	Positive and negative Busy signal indicates the bus is being used.

35, 36	+ACK, -ACK	Positive and negative Acknowledge signal is driven by an initiator to indicate an acknowledgment for a REQ/ACK data transfer handshake.
37, 38	+RST, -RST	Positive and negative Reset signal indicates the Reset condition.
39, 40	+MSG, -MSG	Positive and negative Message signal is driven by a target during the Message phase.
41, 42	+SEL, -SEL	Positive and negative Select signal is used by an initiator to select a target or by a target to reselect an initiator.
43, 44	+C/D, -C/D	Positive and negative Control/Data signal is driven by a target to indicate whether control or data information is on the data bus. True (active) indicates control.
45, 46	+REQ, -REQ	Positive and negative Request signal is driven by a target to indicate a request for a REQ/ACK data transfer handshake.
47, 48	+I/O, -I/O	Positive and negative Input/Output signal is driven by a target that controls the direction of data movement on the data bus with respect to an initiator. True (active) indicates input to the initiator. The signal is also used to distinguish between Selection and Reselection phases.
49, 50	Ground	

Table 8-2 Standard Single-Ended SCSI Connector Pins Associated with UN375

PIN	SIGNAL	FUNCTION
odd	Ground	All odd pins except pin 25 are ground.
02	-DB(0)	Negative Data Bus bit 0.
04	-DB(1)	Negative Data Bus bit 1.
06	-DB(2)	Negative Data Bus bit 2.
08	-DB(3)	Negative Data Bus bit 3.
10	-DB(4)	Negative Data Bus bit 4.
12	-DB(5)	Negative Data Bus bit 5.
14	-DB(6)	Negative Data Bus bit 6.
16	-DB(7)	Negative Data Bus bit 7.
18	-DB(P)	Negative Data Bus parity bit. Parity is odd. The use of parity is a system option. The system is configured to either have all SCSI devices generate and detect parity, or no devices generate and detect parity. Parity is not valid during the Arbitration phase.
20, 22, 24	Ground	
25		Open (no connection).
26	TERMPWR	Optional terminator power is supplied through a backflow diode.
28, 30	Ground	
32	-ATN	Negative Attention signal is driven by an initiator to indicate the Attention condition.
34	Ground	
36	-BSY	Negative Busy signal indicates the bus is being used.
38	-ACK	Negative Acknowledge signal is driven by an initiator to indicate an acknowledgment for a REQ/ACK data transfer handshake.
40	-RST	Negative Reset signal indicates the Reset condition.
42	-MSG	Negative Message signal is driven by a target during the Message phase.
44	-SEL	Negative Select signal is used by an initiator to select a target or by a target to reselect an initiator.
46	-C/D	Negative Control/Data signal is driven by a target to indicate whether control or data information is on the data bus. True (active) indicates control.
48	-REQ	Negative Request signal is driven by a target to indicate a request for a REQ/ACK data transfer handshake.
50	-I/O	Negative Input/Output signal is driven by a target that controls the direction of data movement on the data bus with respect to an initiator. True (active) indicates input to the initiator. The signal is also used to distinguish between Selection and Reselection phases.

8.2.2 UN375/UN375E Functional Description

Figure 8-4 is a functional block diagram of the UN375/UN375E circuit pack. The UN375/UN375E circuit pack includes the following major functions:

- Latch switch
- Power switch circuit providing power control, power alarm, scan point, and signal distributor point functions

- +12 V power supply
- +5 V power supplies
- Voltage monitors
- KS-23908,L20,L21,L30 differential SCSI, 3.5-inch 1000-MB hard disk drive
- KS-23908,L41 single-ended SCSI, 3.5-inch 4-Gigabyte hard disk drive
- Self-identification circuit (currently not supported).

8.2.2.1 Latch Switch

When the UN375/UN375E circuit pack is inserted into the apparatus housing, the -48 V power is not applied to the circuit pack until the Latch Switch is closed. Power is then applied only to the board-mounted power module (BMPM) supplying the 5-V DC power control for the circuit pack. The Latch Switch also mechanically locks the circuit pack in place when it is closed (pushed in). The ST/ON/OFF switch controls the application of power to the logic and drive circuits after control power is applied to the circuit pack.

8.2.2.2 Power Switch Circuit

The Power Switch Circuit provides power controls and indicators, power alarms, and an interface for Scan (SC) and Signal Distributor (SD) points. Figure 8-1 shows the UN375/UN375E circuit pack faceplate.

Table 8-3 defines the UN375/UN375E circuit pack switch functions. Table 8-4 defines the UN375/UN375E circuit pack indicator functions. Table 8-5 defines the UN375/UN375E circuit pack scan point outputs.

The MAJOR ALARM (MJ) is generated when any converter alarm is active, an input voltage is out of range, or when the -48 V is lost and the alarm cutoff-test (ACO-T) switch is off. The MJ is cleared when power is reapplied.

The POWER ALARM is generated when either ALM50 or ALM120 alarms are present and -48 V is present (ON). The POWER ALARM is independent of the position of the ACO-T switch.

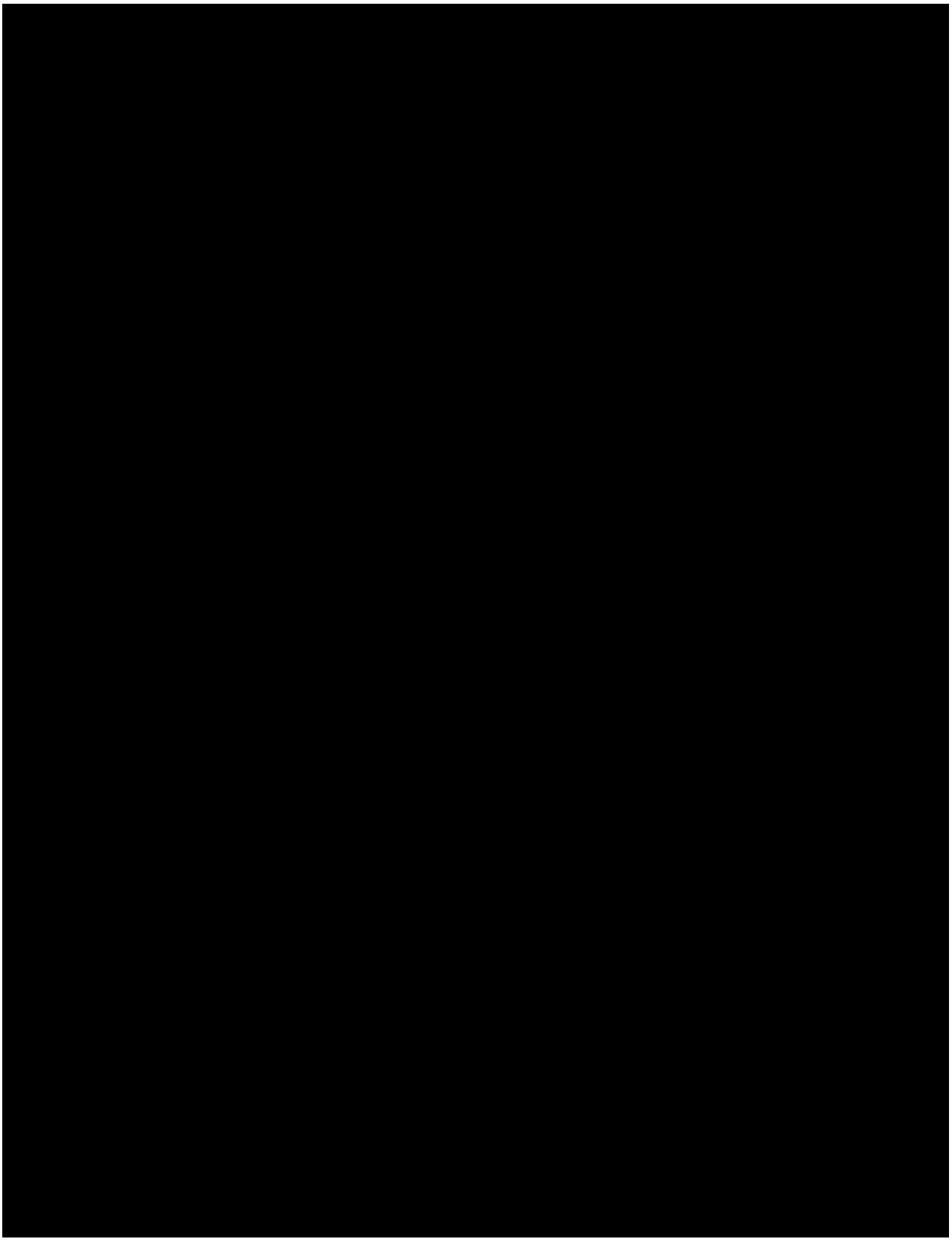


Figure 8-4 UN375/UN375E 3.5-Inch SCSI Hard Disk Drive Functional Block Diagram

Table 8-3 UN375/UN375E Faceplate Switch Functions

NAME	TYPE	FUNCTION

ST/ON/OFF	ROCKER (3-POSITION)	Controls circuit pack power. OFF functions only if the OOS SD input is active. ON allows auto-restart when N48V is applied. ST (momentary position) turns on power (start) when the ACO-T switch is off.
ROS/RST	ROCKER (2-POSITION)	Sends a request via the scan points to remove the circuit pack from service (ROS position) or restore it to service (RST position). The disposition of the request is determined by the system.
ACO-T	ROCKER (2-POSITION)	Retires power alarms, locks out the ON function and tests the OFF, ALM, and OOS faceplate indicators when in the ACO-T position.

Table 8-4 UN375/UN375E Faceplate Indicator Functions

NAME	COLOR	FUNCTION
OFF	Red	Lights when +5 V power is removed from the circuit pack or when the ACO-T switch is operated. Flashes for 30 seconds after power is applied or removed as a warning that the circuit pack is NOT ready to be removed.
ALM	Red	Lights when a power alarm exists in the circuit pack or when the ACO-T switch is operated.
OOS	Amber	Lights when the OOS SD input is active showing that the circuit pack is out-of-service or when the ACO-T switch is operated.

Table 8-5 UN375/UN375E Scan Point Outputs

POWER CONTROL	N48V POWER	POWER ALARM [a]	ROS/RST SWITCH [b, c]	SCAN STATES SCX/Y [d]
ON	ON	0	RST	00
ON	ON	0	ROS	10
ON	ON	1	X [e]	01
X	OFF	X	X	11
OFF	X	X	X	11

Notes:

a. 1 = Active.

b. ROS = Request to remove UN375 circuit pack from service.

c. RST = Request to restore UN375 circuit pack to service.

d. If the pack or scan cable is removed, SCX/Y = 00.

e. X = Don't care.

8.2.2.3 Board-Mounted Power Modules (BMPMs)

8.2.2.3.1 JW030B +12 V Board-Mounted Power Module

The JW030B +12 V board-mounted power module is a 30-watt DC-to-DC converter that operates from -48 V and provides a +12 V output for operation of the disk drive.

8.2.2.3.2 ME005A +5 V Board-Mounted Power Module

The ME005A +5 V board-mounted power module is a 5-watt DC-to-DC converter that operates from -48 V DC and provides a +5 V DC output. The ME005A module provides power to the power control and alarm circuits. This separate power module is used for the power control and alarm circuits to increase system reliability. If the power from the +12 V converter or the other +5 V converter fails, the power control and alarm circuits will still operate to control shutdown, alarms, and the display indicators.

8.2.2.3.3 JW030A +5 V Board-Mounted Power Module

The JW030A +5 V board-mounted power module is a 30-watt DC-to-DC converter that operates from -48 V DC and provides a +5 V DC output. The JW030A module supplies +5 V to the faceplate-mounted disk

drive.

8.2.2.3.4 TW070AB Dual Voltage +5 V and +12 V Board-Mounted Power Module

The TW070AB board-mounted power module provides +5 V and +12 V DC on some disk drive circuit packs. It is a 70-watt converter that operates from -48 V DC. It is specifically designed for use with disk drives and it replaces a JW030B when used.

8.2.2.4 Voltage Monitors

The +5 V, +12 V, -48 V power is monitored as follows:

- The ME005A +5 V power output is monitored by a voltage supervisor that generates an INIT0 signal for the automatic restart of the circuit pack if the ST/ON/OFF switch is ON and the ACO-T switch is OFF. The JW030A +5 V power output is monitored by a voltage supervisor that generates the RST0 signal for controlling the power on relay. The +5 V power must be greater than +4.5 V for the operation of the circuit pack.
- The JW030B or TW070AB +12 V power output is monitored by a voltage comparator that generates a power alarm and lights the ALM indicator when the voltage falls below 11.4 V.
- The -48 V power is monitored by a voltage comparator that generates a remote shutdown of the BMPMs when the voltage falls below -38 V.

8.2.2.5 KS-23908 3.5-Inch SCSI Disk Drive

The 3.5-inch hard disk drive is used to boot the system and to provide random access data storage. Each disk drive provides 1000 MB of formatted data storage, where 1 MB is 10^6 bytes.

8.3 UN376/UN376C/UN376E 3.5-INCH SCSI DAT CARTRIDGE TAPE DRIVE CIRCUIT PACK

8.3.1 UN376/UN376C/UN376E Physical Description

The UN376 series of circuit packs are referred to in a generic sense as UN376 and are identified specifically as follows:

- UN376 (NCR006-3503341)
- UN376C (NCR006-3300608/Comcode 407545243)
- UN376E (KS-24367,L1/Comcode 407771260).

The UN376 provides a faceplate-mounted, 3.5-inch, single-ended SCSI, Digital Data Storage (DDS) formatted Digital Audio Tape (DAT) drive. The DAT drive uses 4 millimeter (3.81 mm) wide tape in 90-, 60-, and 30-meter cartridges (cassettes). Tape media cartridges with the DDS logo are required in the DAT drive unit. DAT tapes with the DDS logo meet the requirements of the European Computer Manufacturers Association (ECMA-130) and ANSI X3.206 standards.

The usable storage capacity provided by the DAT drive varies with the length of tape and the recording mode. Table 8-6 identifies some of the storage capabilities of the DAT cartridges.

Table 8-6 DAT Cartridge Tape Capacity

CARTRIDGE SIZE	MODE	CAPACITY [a]
30 meters	Noncompressed	650 MB
60 meters	Noncompressed	1300 MB

90 meters	Noncompressed	2000 MB

Notes:

a. A megabyte is 2^{20} (1,048,576) bytes.

Figure 8-5 shows the front view of the UN376 circuit pack faceplate using the NCR006-3503341, NCR006-3300608/Comcode 407545243, and KS-24367,L1/Comcode 407771260 SCSI DAT drive. Table 8-7 defines the functions of the NCR006-3503341 DAT drive cassette and drive indicators.

Table 8-8 defines the functions of the NCR006-3300608/Comcode 407545243 and KS-24367,L1/Comcode 407771260 SCSI DAT drive cassette and drive indicators. The cassette and drive indicators are light-emitting diodes (LEDs) located on the front of the SCSI DAT drive.

Figure 8-6 shows the rear view of the power and SCSI connectors on the NCR006-3503341, NCR006-3300608/Comcode 407545243, and KS-24367,L1/Comcode 407771260 DAT drive. Table 8-1 identifies the standard differential SCSI connector pins. Table 8-9 identifies the standard single-ended SCSI connector pins associated with the UN376 circuit pack.

The SCSI device identification for the UN376 circuit pack is set to any available device address in the range of 0 to 6, inclusive, using the three SCSI device identification switches on the circuit pack. A device address (SCSI ID) is available if it does not conflict with any other device on the same SCSI bus. SCSI ID 7 is assigned to the SCSI Host Adapter and is not allowed as a UN376 SCSI device identification. The SCSI device identification pins at the rear of the drive are connected to three switches (SW8-SW6) on the UN376 circuit board by a 6-wire cable assembly. Figure 8-7 shows the general layout of the UN376 circuit pack and the location of the SCSI device identification switches and connectors (headers) on the UN376 circuit board. Table 8-10 identifies the switch settings for the various SCSI device identification addresses.

Figure 8-8 shows the option select switches on the NCR006-3503341, NCR006-3300608/Comcode 407545243, and KS-24367,L1/Comcode 407771260 SCSI DAT drive. The option switches in Figure 8-8 are set as indicated and are NOT to be changed. The states of the option switches are read when power is applied to the drive and determine various drive functions. For the NCR006-3503341 DAT, the option select switches 1 through 8 are set to 00111100, respectively. (1 is the "ON" state.) For the NCR006-3300608/Comcode 407545243 and KS-24367,L1/Comcode 407771260 DAT, the options select switches 1 through 8 are set 01111111, respectively.

The UN376 circuit pack uses seven cables as follows:

- An SCSI power cable connects the SCSI power header (J3) on the circuit board and the DAT drive DC connector.
- An SCSI single-ended cable connects the single-ended SCSI header (J4) on the circuit board and the single-ended DAT drive SCSI connector.
- An Out-Of-Service (OOS) indicator cable connects the OOS indicator header (J5) on the circuit board and the OOS indicator on the faceplate.
- An ALM indicator cable connects the ALM indicator header (J6) on the circuit board and the ALM indicator on the faceplate.
- A Request-Out-of-Service/Restore (ROS/RST) switch cable connects the ROS/RST switch header (J7) on the circuit board and the ROS indicator on the faceplate.
- An ACO-T switch cable connects the ACO-T switch header (J8) on the circuit board and the ACO-T switch on the faceplate.
- An SCSI identification cable connects the SCSI ID switches SW8-SW6 on the circuit board (via J9, a 6-pin header) and the SCSI ID header on the DAT drive (via a paddleboard).

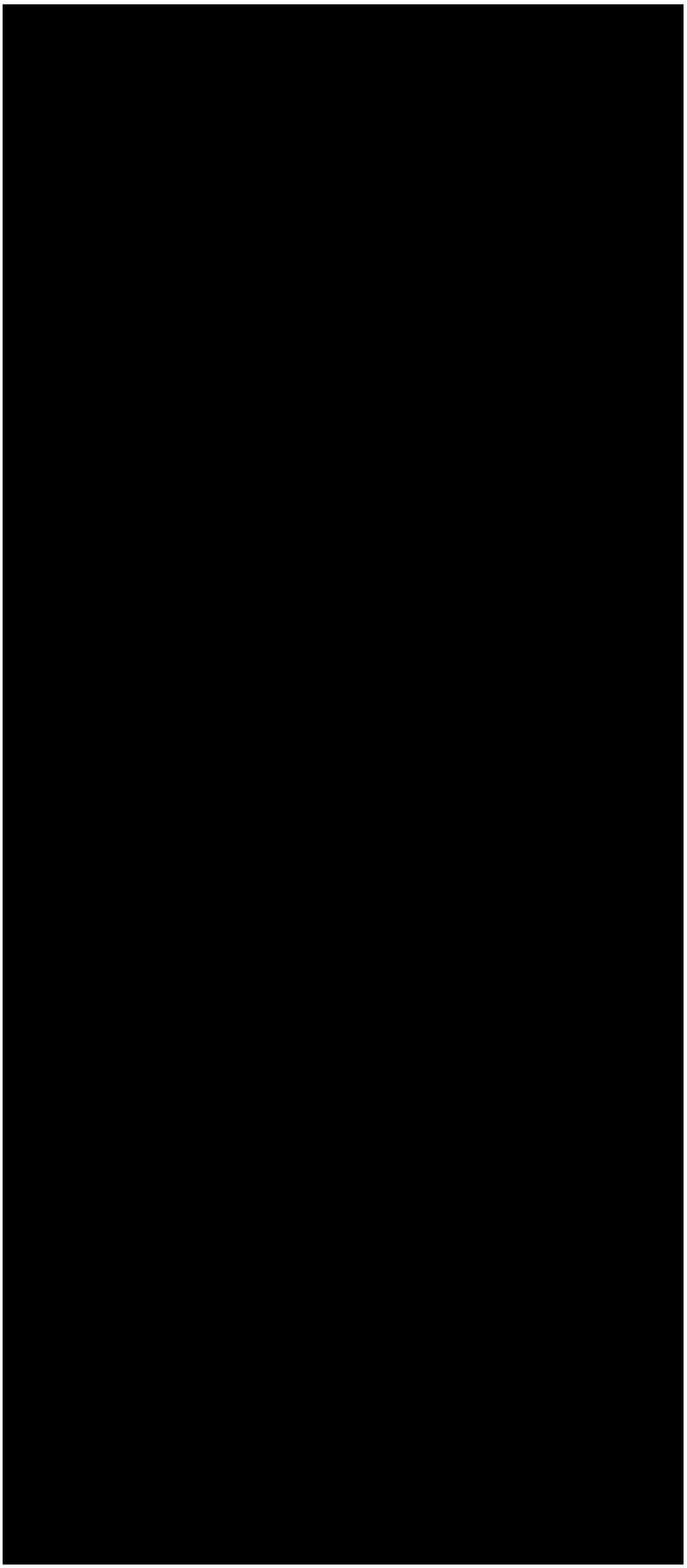


Figure 8-5 UN376/UN376C/UN376E SCSI DAT Drive Front View

Table 8-7 UN376 (NCR006-3503341) 3.5-Inch SCSI DAT Drive Indicators

CASSETTE INDICATOR	DRIVE INDICATOR	STATE	DESCRIPTION [a]
Off	Off	Not Applicable	(1) Power is off. (2) Power is on and the cassette is not present.
Flashing Green	Flashing Green	Read/Write	Cassette is in the process of unloading or loading.
Green	Green	Read/Write	Cassette is loaded and is on-line.
Green	Flashing Green	Read/Write	Cassette is loaded and is being accessed.
Green	Off	Read/Write	Cassette is loaded and is off-line. Taking the UN376 circuit pack Out-Of-Service (OOS) does NOT take the DAT drive on the circuit pack off-line.
Flashing Amber	Flashing Green	Write-Protect	Cassette is write-protected and is in the process of unloading or loading.
Amber	Green	Write-Protect	Cassette is write-protected, loaded, and on-line.
Amber	Flashing Green	Write-Protect	Cassette is write-protected, loaded, and being accessed.
Amber	Off	Write-Protect	Cassette is write-protected, loaded, and off-line.
Green	Alternately Flashing Green and Amber	Error	Media wear caution signal. An excessive number of read-after-writes or an excessive number of errors corrected by third-level error correction have been detected.
Amber	Amber	Error	High-humidity warning. All commands are aborted and the tape is unthreaded to prevent damage to the tape and head. This state is also used to indicate no terminating resistor on the SCSI bus.
Flashing Amber	Flashing Amber	Error	Normal self-test diagnostic sequence.
Flashing Amber	Amber	Error	Self-test diagnostic failure.

Notes:

a. See Table 8-14 for definitions of the terms Not Present, Present, Present But Not Loaded, Loaded, Loading, Unloading, and Ejecting.

Table 8-8 UN376C (NCR006-3300608/Comcode 407545243) and UN376E (KS-24367,L1/Comcode 407771260) 3.5-Inch SCSI DAT Drive Indicators

CASSETTE INDICATOR [a]	DRIVE INDICATOR	STATE	DESCRIPTION
Off	Off	Not Applicable	(1) Power is off. (2) Power is on and the cassette is not present.
Pulse Green	Off	Read/Write	Cassette is in the process of unloading or loading, or Self-Test is in progress.
Green	Off	Read/Write	Cassette is loaded and is on-line.
Flash Green	Off	Read/Write	Cassette is loaded and is being accessed.
Pulse Green	Off	Write-Protect	Cassette is write-protected and is in the process of unloading or loading.
Green	Off	Write-Protect	Cassette is write-protected, loaded, and on-line.
Flash Green	Off	Write-Protect	Cassette is write-protected, loaded, and being accessed (Read only).
Green	Alternately Flashing Green and Amber	Error	Caution signal. If triggered by the wellness check, insert a cleaning cartridge and repeat the test with a fresh tape. If the Caution Signal persists, fail the drive. If the Caution Signal cleared when the fresh tape was used, the original tape is faulty. Discard the faulty original tape.
Any	Pulse Amber	Error	Cleaning is needed or cassette is nearing end of useful life.
Any	Amber	Error	Hard fault.
Flash Green	Off	Cleaning	Cleaning cartridge is in process of loading, unloading, or cleaning.

Notes:

a. Flash = ¼ second ON, ¼ second OFF;

Pulse = ½ second ON, ½ second OFF.

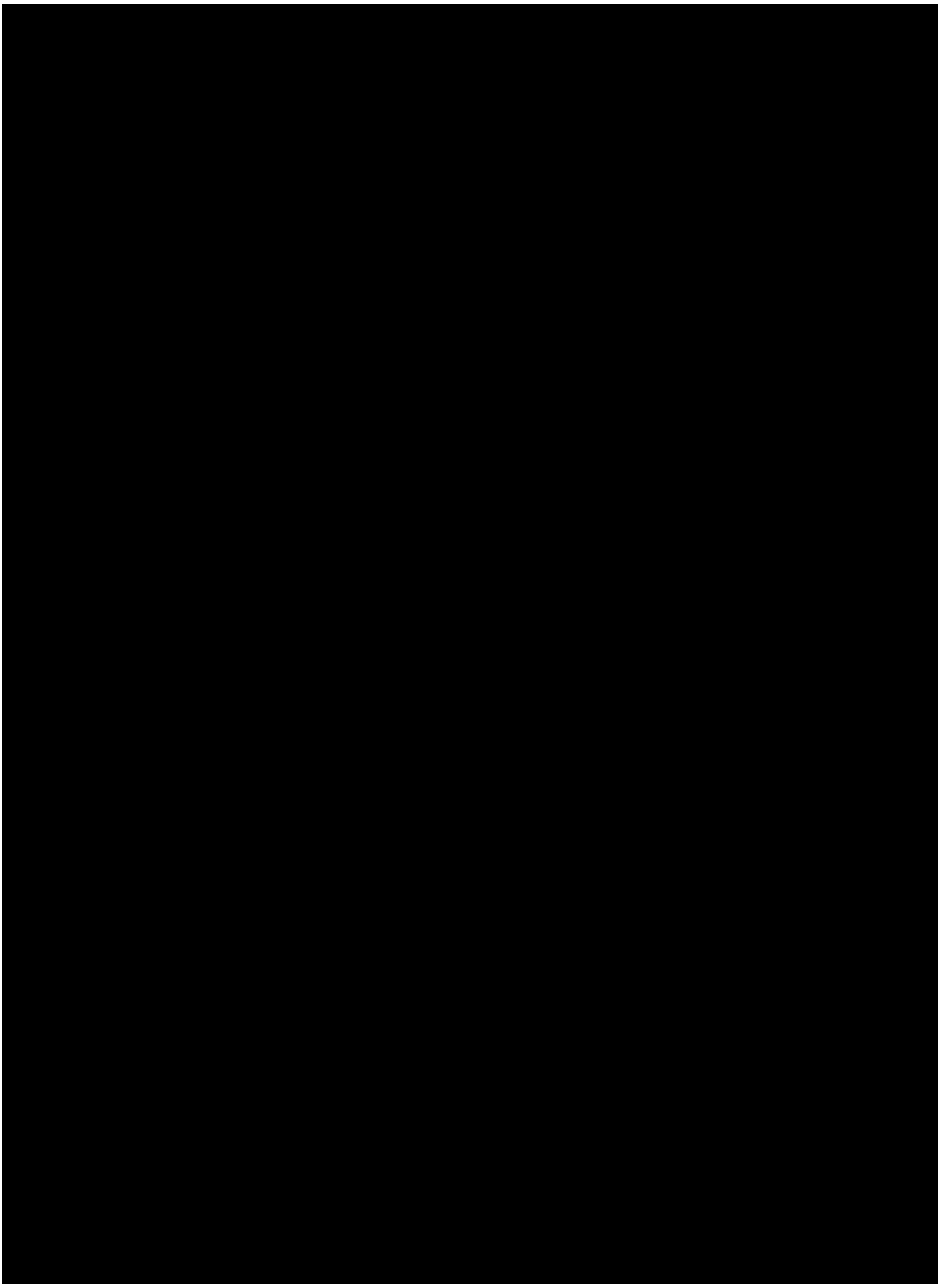


Figure 8-6 UN376/UN376C/UN376E SCSI DAT Drive Rear View

Table 8-9 Standard Single-Ended SCSI Connector Pins Associated with UN376

PIN	SIGNAL	FUNCTION
odd	Ground	All odd pins except pin 25 are ground.
02	DB(0)0	Data Bus bit 0.
04	DB(1)0	Data Bus bit 1.
06	DB(2)0	Data Bus bit 2.
08	DB(3)0	Data Bus bit 3.
10	DB(4)0	Data Bus bit 4.
12	DB(5)0	Data Bus bit 5.
14	DB(6)0	Data Bus bit 6.
16	DB(7)0	Data Bus bit 7. Bit 7 is the most significant bit and has the highest priority during arbitration.
18	DB(P)0	Data Bus parity bit. Parity is odd. The use of parity is a system option. The system is configured to either have all SCSI devices generate and detect parity or no devices generate and detect parity. Parity is not valid during the Arbitration phase.
20-24	Ground	
25		Open (no connection).
26	TERMPWR	Optional terminator power is supplied through a backflow diode.
28-30	Ground	
32	ATN0	Attention signal is driven by an initiator to indicate the Attention condition.
34	Ground	
36	BSY0	Busy signal is an "OR-tied" signal that indicates the bus is being used.
38	ACK0	Acknowledge signal is driven by an initiator to indicate an acknowledgment for a REQ/ACK data transfer handshake.
40	RST0	Reset is an "OR-tied" signal that indicates the Reset condition.
42	MSG0	Message signal is driven by a target during the Message phase.
44	SEL0	Select signal is used by an initiator to select a target or by a target to reselect an initiator.
46	C/D0	Control/Data signal is driven by a target to indicate whether control or data information is on the data bus. True (active) indicates control.
48	REQ0	Request signal is driven by a target to indicate a request for a REQ/ACK data transfer handshake.
50	I/O0	Input/Output signal is driven by a target that controls the direction of data movement on the data bus with respect to an initiator. True (active) indicates input to the initiator. The signal is also used to distinguish between Selection and Reselection phases.

Figure 8-7 UN376 Circuit Pack Layout

Table 8-10 DAT SCSI Device Identification Switch Settings

SCSI ID	SW8	SW7	SW6
0	Open (0)	Open (0)	Open (0)
1	Open (0)	Open (0)	Closed (1)
2	Open (0)	Closed (1)	Open (0)
3	Open (0)	Closed (1)	Closed (1)
4	Closed (1)	Open (0)	Open (0)
5	Closed (1)	Open (0)	Closed (1)
6	Closed (1)	Closed (1)	Open (0)
7 **a**	Closed (1)	Closed (1)	Closed (1)

Notes:

a. SCSI device ID number 7 is not allowed.

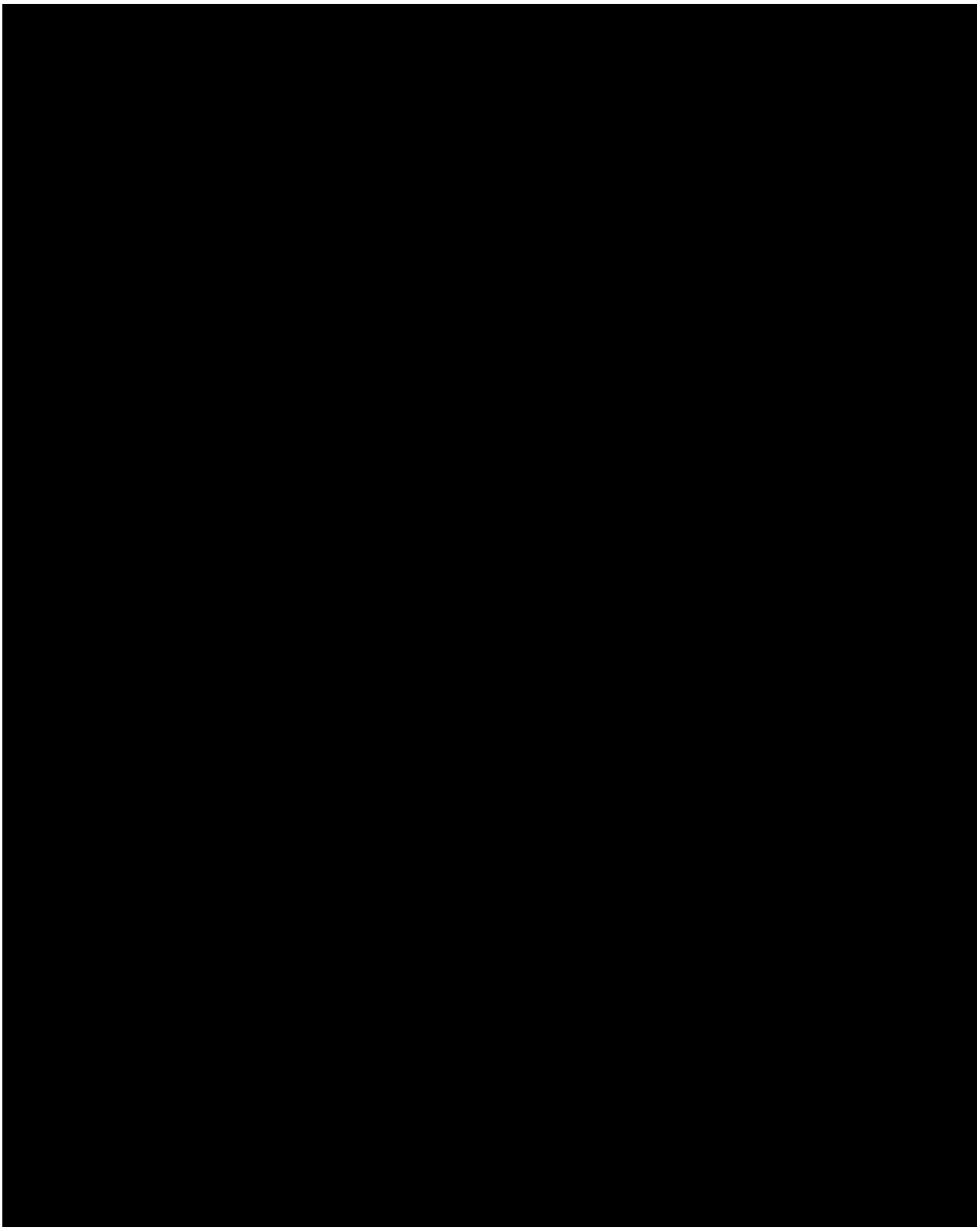


Figure 8-8 UN376 SCSI DAT Drive Option Select Switches Bottom View

8.3.1.1 DAT Drive Cartridge Tapes

The DAT uses DDS-grade 4-millimeter-wide tape in 90-, 60-, and 30-meter cartridges (cassettes). The 120-meter DDS-2 cartridges are not supported by the NCR006-3503341, the NCR006-3300608/Comcode

407545243, or the KS-24367,L1/Comcode 407771260 DATs, and cannot be used.

The 90-meter cartridge is recommended.

The recommended maximum use for a tape is 2000 passes over any particular area of the tape. This includes retries. The recommended maximum number of times a tape should be loaded into a drive is 100. Data should be transferred to a new tape and the old tape discarded if either of these "useful life" thresholds are reached.

Worn tapes and tapes at or near end of "useful life" may cause excessive read-after-write error recovery and high error-correction counts to occur. The following are indicators that a tape is worn or has exceeded one of the "useful life" thresholds:

UN376 (NCR006-3503341) SCSI DAT Drive

- The "Media Wear Caution" signal is displayed. Also, this indicates that cleaning may be needed. "Media Wear Caution" is signaled by the Cassette Indicator LED (green) and Drive Indicator LED (alternately flashing green and amber). (See Table 8-7 for DAT drive indicators.)

UN376C (NCR006-3300608/Comcode 407545243) and UN376E (KS-24367,L1/Comcode 407771260) SCSI DAT Drives

- The "Cleaning Needed" signal LED does not extinguish after cleaning. "Cleaning Needed" is signaled by the Cassette Indicator LED (any) and Drive Indicator LED (pulse amber). (See Table 8-8 for DAT drive indicators.)

- The "Cleaning Needed" signal LED extinguishes after cleaning, but reappears following the next tape access. "Cleaning Needed" is signaled by the Cassette Indicator LED (any) and Drive Indicator LED (pulse amber). (See Table 8-8 for DAT drive indicators.)

- The "Caution" signal is displayed. "Caution" is signaled by the Cassette Indicator LED (green) and Drive Indicator LED (alternately flashing green and amber). (See Table 8-8 for DAT drive indicators.)

8.3.2 UN376 Functional Description

Figure 8-9 is a functional block diagram of the UN376 circuit pack. The UN376 circuit pack includes the following major functions:

- Latch switch
- Power switch circuit providing power control, power alarm, scan point, and signal distributor point functions
- +12 V power supply
- +5 V power supply
- NCR006-3503341, NCR006-3300608/Comcode 407545243 (UN376C), or KS-24367,L1/Comcode 407771260 (UN376E) single-ended SCSI, 3.5-inch DAT drive
- Single-ended to differential SCSI converter
- Self-identification circuit.

8.3.2.1 Latch Switch

When the UN376 circuit pack is inserted into the apparatus housing, the -48 V power is not applied to the circuit pack until the Latch Switch is closed. When the Latch Switch is pushed in and the ACO-T switch is off, the UN376 circuit pack power-up sequence is started. Power is first applied to the BMPM supplying the +5 V DC power control for the circuit pack and then a power-up sequence is started for logic and drive circuits. The Latch Switch functions as the on/off switch for the circuit pack and mechanically locks the circuit pack in place when it is closed (pushed in).

8.3.2.2 Power Switch Circuit

The Power Switch Circuit provides power controls and indicators, power alarms, and an interface for SC and SD points. Figure 8-5 shows the UN376 circuit pack faceplate controls and indicators.

Table 8-11 defines the UN376 circuit pack switch functions. Table 8-12 defines the UN376 circuit pack indicator functions. Table 8-13 defines the UN376 circuit pack scan point outputs.

The MAJOR ALARM (MJ) is generated when any converter alarm is active, an input voltage is out of range, or when the -48 V is lost and the ACO-T switch is off. The MJ is cleared when power is reapplied.

The POWER ALARM is generated when either ALM50 or ALM120 alarms are present and -48 V is present (ON). The POWER ALARM alarm is independent of the position of the ACO-T switch.

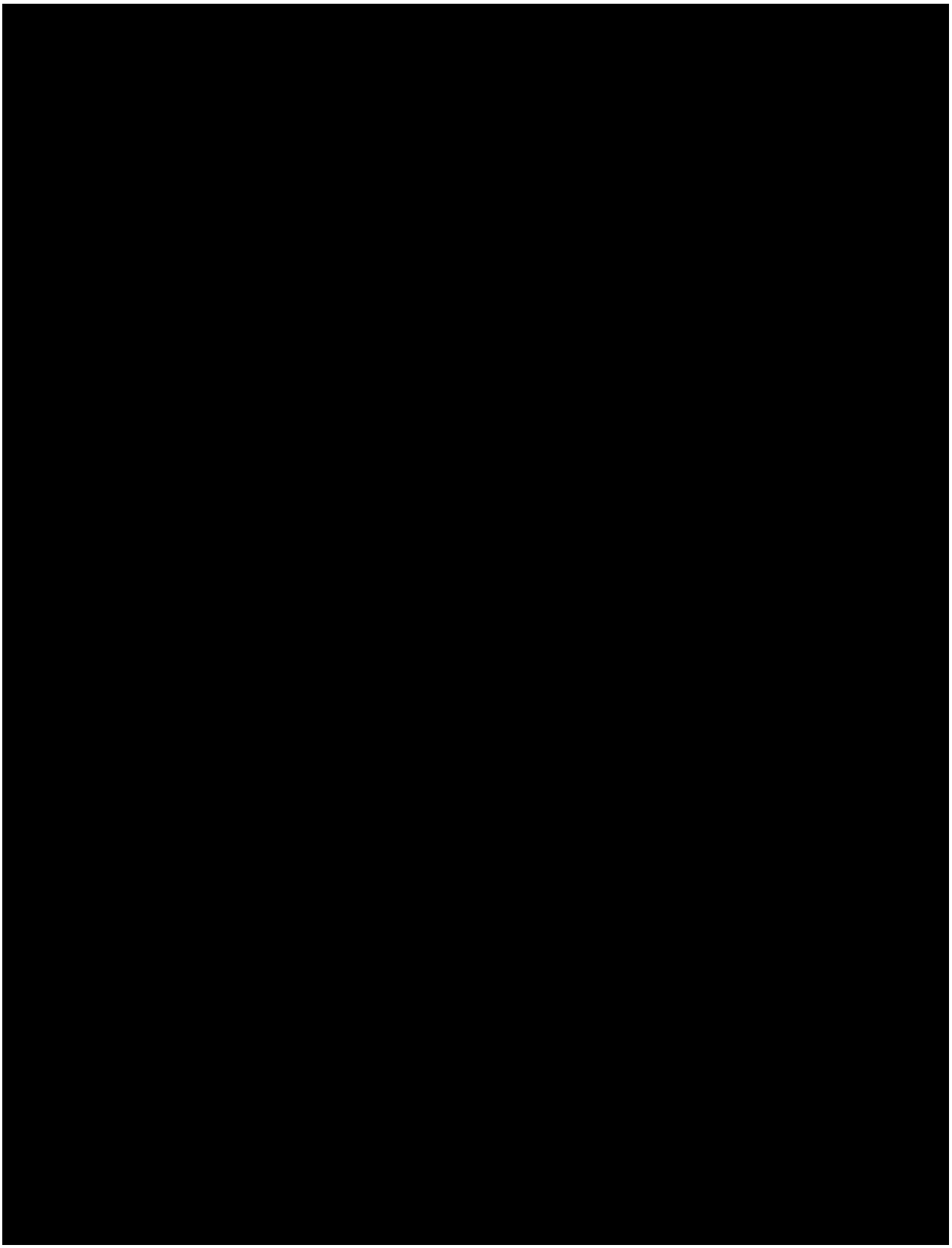


Figure 8-9 UN376/UN376C/UN376E 3.5-Inch SCSI DAT Drive Functional Block Diagram

Table 8-11 UN376 Faceplate Switch Functions

NAME	TYPE	FUNCTION

ROS/RST	ROCKER (2-POSITION)	Sends a request via the scan points to remove the circuit pack from service (ROS position) or to restore it to service (RST position). The disposition of the request is determined by the system.
ACO-T	ROCKER (2-POSITION)	Retires power alarms, locks out the ON function, and tests the ALM and OOS faceplate indicators when in the ACO-T position.

Table 8-12 UN376 Faceplate Indicator Functions

NAME	COLOR	FUNCTION
ALM	Red	Lights when a power alarm exists in the circuit pack or when the ACO-T switch is operated.
OOS	Amber	Lights when the OOS SD input is active showing that the circuit pack is out-of-service or when the ACO-T switch is operated.

Table 8-13 UN376 Scan Point Outputs

POWER CONTROL	N48V POWER	POWER ALARM [a]	ROS/RST SWITCH [b, c]	SCAN STATES SCX/Y [d]
ON	ON	0	RST	00
ON	ON	0	ROS	10
ON	ON	1	X [e]	01
X	OFF	X	X	11
OFF	X	X	X	11

Notes:

a. 1 = Active.

b. ROS = Request to remove UN375 circuit pack from service.

c. RST = Request to restore UN375 circuit pack to service.

d. If the pack or scan cable is removed, SCX/Y = 00.

e. X = Don't care.

8.3.2.3 Board-Mounted Power Modules (BMPMs)

8.3.2.3.1 JW030B +12 V Board-Mounted Power Module

The JW030B +12 V board-mounted power module is a 30-watt DC-to-DC converter that operates from -48 V and provides a +12 V output for operation of the tape drive.

8.3.2.3.2 ME005A +5 V Board-Mounted Power Module

The ME005A +5 V board-mounted power module is a 5-watt DC-to-DC converter that operates from -48 V DC and provides a +5 V DC output. The ME005A module provides power to the power control and alarm circuits. This separate power module is used for the power control and alarm circuits to increase system reliability. If the power from the +12 V converter or the other +5 V converter fails, the power control and alarm circuits will still operate to control shutdown, alarms, and the display indicators.

8.3.2.3.3 JW030A +5 V Board-Mounted Power Module

The JW030A +5 V board-mounted power module is a 30-watt DC-to-DC converter that operates from -48 V DC and provides a +5 V DC output. The JW030A module supplies +5 V to the faceplate-mounted tape drive and to the Differential-to-Single-Ended SCSI Converter circuit.

8.3.2.4 Voltage Monitors

The +5 V, +12 V, -48 V power is monitored as follows:

- The ME005A +5 V power output is monitored by a voltage supervisor that generates an INIT0 signal for the automatic restart of the circuit pack if the Latch Switch is closed and the ACO-T switch is OFF. The JW030A +5 V power output is monitored by a voltage supervisor that generates the RST0 signal for controlling the power on relay. The +5 V power must be greater than +4.5 V for the operation of the circuit pack.
- The JW030B +12 V power output is monitored by a voltage comparator that generates a power alarm and lights the ALM indicator when the voltage falls below 11.4 V.
- The -48 V power is monitored by a voltage comparator that generates a remote shutdown of the board-mounted power modules when the voltage falls below -38 V.

8.3.2.5 NCR006-3503341, NCR006-3300608/Comcode 407545243, or KS-24367,L1/Comcode 407771260 3.5-Inch, Single-Ended SCSI DAT Drive

The 3.5-inch DAT drive provides a low-cost cartridge tape capability for the 3B21D computer.

8.3.2.6 Single-Ended-to-Differential SCSI Converter

The Single-Ended-to-Differential SCSI Converter circuit provides the following functions:

- Interfaces the 3B21D computer differential SCSI bus and the single-ended SCSI device bus.
- Monitors SCSI bus activity to correctly interface the two buses.
- Terminates the single-ended SCSI bus.
- Maintains transparency to all SCSI commands.

8.3.2.7 SCSI ID Switch

Figure 8-7 and Table 8-10 show the placement and settings for the SCSI ID switches.

CAUTION: Take extreme care to ensure that there are no SCSI ID conflicts. If two or more devices have the same ID, the results are unpredictable.

8.3.3 NCR006-3503341 Operation Notes

8.3.3.1 Cartridge Tape Loading and Unloading Definitions

The DAT drive may be in any one of seven states with respect to the cartridge tape. Table 8-14 defines the cartridge tape drive states. These states do NOT directly relate to the state of the drive and cassette indicators defined in Table 8-7 .

Table 8-14 NCR006-3503341 DAT States

STATE	DEFINITION
Not Present	No cassette is in the drive.
Present But Not Loaded	A cassette is in the drive, but the tape has not been threaded around the head drum.
Present	A cassette is fully in the drive mechanically, but the tape may or may not be logically loaded.
Loaded	A cassette is in the drive and it has been logically loaded. The drive is ready to accept commands.
Loading	The drive is in the process of loading the tape. This is a transition state between the "Present But Not Loaded" and "Loaded" states.
Unloading	The drive is in the process of unloading the tape. This is a transition state between the "Loaded" and "Present But Not Loaded" states.
Ejecting	The drive is in the process of ejecting the cassette. This is a transition state between the "Present But Not

| Loaded" and "Not Present" states.

8.3.3.2 How to Write-Protect a Cartridge Tape

CAUTION: When a cassette tape is write-protected, the tape log cannot be updated. This means that the history of tape use will be inaccurate.

A cartridge (cassette) tape is write-protected by sliding the tab on the rear of the cassette so that the hole is open. When write-protected, data can only be read from the tape. A cassette tape is write-enabled when the hole is closed.

8.3.3.3 How to Load a Cartridge Tape

CAUTION: Although the manufacturer has provided pins to prevent the cassette from being over-inserted, excessive insertion force will damage the drive mechanism components. The cassette should be inserted gently into the drive. Very little force is required to cause the drive to grab the cassette; after that, the drive will pull the cassette into the drive.

Gently insert the cartridge tape (cassette) into the drive until the drive takes hold of the cartridge. The cartridge tape loading sequence is as follows:

(1) The drive threads the tape and rewinds the tape to the Beginning of Media (BOM). The tape is then moved to the Beginning of Partition (BOP) for Partition 0. The Reference area is then checked to determine the tape format (DDS, audio, and so forth.).

(2) If the tape is blank, the drive leaves the tape at the BOP for Partition 0 and waits for the next command.

(3) If the error rate is high, Caution is signaled on the front panel indicators by lighting the Cassette indicator green and alternately flashing the drive indicator green and amber.

(4) The system area on the tape is then accessed, and the tape log is read into the drive.

(5) The drive rewinds to the BOP and goes on-line.

NOTE: If the NCR006-3503341 DAT drive is power-cycled while a cassette is loaded, the drive performs a load sequence and goes on-line.

8.3.3.4 How to Remove a Cartridge Tape

CAUTION: To protect the media from damage, remove the cassette from the drive before powering down the UN376 circuit pack.

The cassette tape can be removed from the NCR006-3503341 (UN376), NCR006-3300608/Comcode 407545243 (UN376C), or KS-24367,L1/Comcode 407771260 (UN376E) DAT drive by pressing the Unload button on the drive. The Unload button ejects the cassette from the drive.

The unload sequence is as follows:

(1) The tape is rewound to the BOP for Partition 0.

(2) If the tape is write-enabled, a copy of the tape log held in the drive RAM is written back to the tape.

(3) The tape is rewound to the BOM, unthreaded from the drive mechanism, and ejected.

8.3.3.5 How to Clean the Drive

Clean the UN376/UN376C/UN376E tape heads after every 25 hours of operation.

- Clean the *UN376* tape heads when the cassette indicator is green and the drive indicator alternately flashes green and amber.
- Clean the *UN376C/UN376E* tape heads when either of the following conditions occur:
  - The cassette indicator is in any state and the drive indicator pulses amber, or
  - The cassette indicator is green and the drive indicator alternately flashes green and amber.

Use a (*Hewlett-Packard part number C5709A. or equivalent*) 4-mm cleaning cassette to clean the drive. Insert the cleaning cassette into the drive and the drive will automatically load the cassette, clean the heads, and eject the cassette. When the operation is complete, record the date on the cassette label to maintain a history of use. After 25 uses, replace the cleaning cassette.

8.4 OPTIONAL 9-TRACK SCSI TAPE DRIVE (KS-23909)

8.4.1 KS-23909 Physical Description

The KS-23909 9-Track SCSI Tape Drive is a vertically-mounted, half-inch, reel-to-reel magnetic tape drive. The use of 9-track tape media that complies with ANSI standard 3.40-1983 (or later issue) or ECMA-62 specification is recommended.

The KS-23909,L10 drive is a 1600/6250 Characters Per Inch (CPI), dual-density, automatically-loaded drive with a 512-kilobyte buffer operating at 42 Inches Per Second (IPS) in either electronic start/stop or streaming modes, or operating at 125 IPS in the streaming mode.

The KS-23909,L21 drive is a 1600/6250 CPI, dual-density, manually loaded drive with a 1 megabyte buffer operating at 125 IPS in either electronic start/stop or streaming modes.

The drives can operate in either a buffered or unbuffered mode. In the buffered mode, either a 512-kilobyte or 1-megabyte electronic cache buffer allows the system designs to maintain streaming performance.

Data is recorded in either the 1600 CPI Phase Encoded (PE) method or the 6250 CPI Group Coded Recording (GCR) method. (A megabyte is 2^{20} bytes of data.)

The differential buffered SCSI permits the location of the tape unit to be up to 82 feet (25 meters) from the SCSI host adapter. The 9-track tape units are located in Peripheral Growth Cabinets, to the right of the Processor Cabinet.

Table 8-15 identifies the available KS-23909 9-track drives. Table 8-1 identifies the standard differential SCSI connector pins.

Table 8-15 KS-23909 9-Track Tape Drives

KS-23909	DESCRIPTION
List 10	Universal 120- or 240-V AC, 9-track tape drive with differential SCSI, automatic loading, and 512-kilobyte buffer.
List 21	Universal 120- or 240-V AC, 9-track tape drive with differential SCSI, manual loading, and 1-megabyte buffer.

The KS-23909 9-track tape drive accepts 6.25-, 7-, 8.5-, and 10.5-inch tape reels of 0.5-inch wide magnetic tape. Table 8-16 summarizes the data storage capabilities available with the various sizes of reels and recording methods.

Table 8-16 KS-23909 9-Track Tape Capacity

REEL SIZE (inches)	REEL CAPACITY (feet)	APPROXIMATE STORAGE CAPACITY	
		1600 CPI (64-Kbyte Blocking)	6250 CPI (256-Kbyte Blocking)
10.50	2400	45 MB [a]	178 MB [a]
8.50	1200	22 MB [a]	89 MB [a]
7.00	600	11 MB [a]	44 MB [a]
6.25	300	5 MB [a]	22 MB [a]

Notes:

a. A megabyte (MB) is 2^{20} bytes.

8.4.2 KS-23909 Functional Description

See the vendor manuals provided with the 9-track tape drive unit for functional information. KS-23909,L10 is documented in the vendor manual KS-23909,L40. KS-23909,L21 is documented in the vendor manual KS-23909,L30.

8.4.3 KS-23909,L10 Operation Notes

8.4.3.1 How to Load Tape

To load tape on the KS-23909,L10 unit, perform the following steps:

(1) Wait for the OK indication at the end of the power-on sequence.

(2) Ensure that a write-enable ring is installed on the tape reel to permit writing, or is removed to prevent over-writing the existing data.

(3) Ensure that the tape end is free. For new reels, remove the adhesive strip and/or rubber block constraining the free end of the tape to the tape pack.

(4) Open the loading door.

(5) Place the tape reel onto the self-centering supply hub with the write enable ring side towards the casting. Push the tape reel onto the self-centering hub in the loading chamber. The pushing action both locates the reel and locks it onto the hub.

(6) Close the loading door. When the loading door is closed, the auto-threading procedure is started. The unit checks that the reel is not inverted. The tape is then threaded to the take-up spool, tensioned, and advanced to the Beginning of Tape (BOT). The display should indicate LOCATING, quickly followed by LOADING.

(7) When the BOT is indicated, the load sequence is complete. Check the Loading/Unloading Indications for other indications that might be displayed during the loading sequence.

8.4.3.2 How to Remove the Tape Reel (With Power On)

To remove a tape reel from the unit with power on, perform the following steps:

(1) Set the KS-23909,L10 unit off-line either by pressing the RESET button, or, if in the diagnostic mode, by pressing the DIAG button once.

(2) If "Offline" is displayed, press and hold down the RESET button, and then press RWD/UNL. The tape will rewind with REW/UNLD indicated through to the BOT.

(3) Wait for the OK indication, and then press the center of the supply hub to release the tape reel.

8.4.3.3 How to Remove the Tape Reel (During a Power Failure)

If power to the KS-23909,L10 unit is OFF, and it is essential that the tape be removed, the tape reel may be rewound manually by performing the following steps:

(1) Set power OFF (for safety reasons).

(2) Open the loading door, and then rotate the supply reel counter-clockwise until all of the tape has been rewound.

(3) Press the hub release button, and then lift off the unclamped tape reel.

(4) Close the loading door.

8.4.4 KS-23909,L21 Operation Notes

8.4.4.1 How to Load Tape

To load tape on the KS-23909,L21 unit, perform the following steps:

(1) Open the tape door.

(2) Slide a tape reel, free end to the right, over the center of the supply hub until the rollers retain the reel.

(3) Manually thread the tape following the tape path to the take-up reel.

(4) Secure the end of the tape on the take-up reel, and rotate the reel two times.

(5) Close the tape door.

8.4.4.2 How to Remove the Tape Reel

To remove a tape reel from the KS-23909,L21 unit with power on, perform the following steps:

(1) Take the drive off-line by pressing ONLINE.

(2) Press the REW/UNLD key.

(3) Open the tape door. Note that if the door is opened before the unload cycle is complete, the supply hub fingers may not completely retract. Manual retraction of the supply hub fingers will then be required. Push and hold the tape lock/unlock lever, and turn the supply hub counter clockwise to manually retract the supply hub fingers.

(4) Remove the tape from the supply hub.

(5) Close the tape door.

8.5 MAINTENANCE TERMINAL (KS-23996 COLOR VIDEO TERMINAL)

The 3B21D computer maintenance terminal, Maintenance Teletypewriter (MTTY), is a KS-23996 Color Video Terminal. The KS-23996 Color Video Terminal is a low-cost color video terminal with the following characteristics:

- Display is 24 lines by 80 columns.

- Display is 12 inches minimum (diagonally).
- Supports eight foreground and eight background colors (Table 8-17).
- Supports two RS-232C ports: one for connection to the 3B21D computer [Data Terminal Equipment (DTE) configuration] and one for connection to a serial printer [Data Communications Equipment (DCE) configuration].
- Supports one parallel printer port.
- Keyboard is a QWERTY layout with standard alphanumeric keys, a numeric keypad, programmable function keys, private function keys, and a set of arrow keys (Figure 8-10).

Table 8-18 identifies the KS-23996 list numbers.

Table 8-17 Background and Foreground Colors

COLOR	FOREGROUND PARAMETER VALUE	BACKGROUND PARAMETER VALUE
Black	30	40
Red	31	41
Green	32	42
Yellow	33	43
Blue	34	44
Magenta	35	45
Cyan	36	46
White	37	47

Figure 8-10 260C ANSI Keyboard

Table 8-18 KS-23996 Color Video Terminal List Numbers

LIST	DESCRIPTION	NET UNIT WEIGHT (lb.)
KS-23996,L1	Color Video Terminal, Domestic (U.S.)	42.2
KS-23996,L5	Color Video Terminal, International	42.2
KS-23996,L10	Color Video Terminal Base Unit, Domestic (U.S.)	11.5
KS-23996,L15	Color Video Terminal Base Unit, International	11.5
KS-23996,L20	Color Video Terminal Keyboard	3.7
KS-23996,L30	Color Video Terminal Monitor, Domestic (U.S.)	27.0
KS-23996,L35	Color Video Terminal Monitor, International	27.0
KS-23996,L40	Color Video Terminal Instruction Manual	0.05

Figure 8-11 is a rear view of the Color Video Terminal Base Unit, KS-23996,L10 or L15, and shows the location of the *power*, **Parallel**, **Aux**, **EAI** (Emergency Action Interface), **Video**, and **Kybd** connections. These connections are as follows:

- Power for the domestic (U.S.) MTTY is 120-V AC, 60 Hz; the international version is 240-V AC, 50-Hz power. There are no user adjustable voltage settings. KS-23996,L1 is the domestic (U.S.) version of the MTTY, and KS-23996,L5 is the international version. Note that the installing organization (the application) is responsible for supplying the power cords for the international version because of variations in plug/receptacle configurations in international installations. The domestic (U.S.) version, KS-23996,L1, comes with two detachable, 6-foot, 3-wire power cords (one cord for the Monitor and one cord for the Base Unit).

- The **EAI** connector is the primary 3B21D computer port. This is a 25-pin D connector providing an RS-232C serial port configured for Data Terminal Equipment (DTE). Figure 8-12 shows the pinout for the **EAI** connector. The EAI port on the Base Unit is connected to the 3B21D computer UN377 Port Switch and Scanner-Distributor Buffer (PSSDB) circuit pack with an ED-3T076-20,G7B (50 feet), ED-3T076-20,G7D (100 feet), or an ED-3T076-20,G7F (250 feet) MTTY cable. The connection to the UN377 circuit pack is at the Processor Unit 1 backplane at EQL 045-186-332.

- The **Aux** connector is a secondary host port for connection to a serial printer or to a second host computer (host computer or modem). This is a 25-pin D connector providing a port configured for Data Communications Equipment (DCE). No adapter is needed to connect a serial printer to the **Aux** port (generally a DTE device); however, a null modem adapter may be needed if the port is connected to a host computer or modem (generally a DCE device). Figure 8-12 shows the pinout for the **Aux** connector.

- The **Parallel** connector is a Centronics parallel port for connection to a printer or other parallel device. Figure 8-13 shows the pinout for the **Parallel** 25-pin D connector.

- The **Kybd** connector is used to connect the 260C ANSI keyboard.

- The Color Video Monitor connects to the **Video** connector on the Color Video Base Unit.

Figure 8-11 KS-23996,L10 or L15 Base Unit Rear View

Figure 8-12 MTTY EAI and Aux Connector Pinout

Figure 8-13 MTTY Parallel Connector Pinout

8.6 RECEIVE-ONLY PRINTER (ROP)

There are two types of printers available that can be used as the Receive-Only Printer (ROP). One is a Lucent Technologies Model 577 dot-matrix printer intended for large office applications where the workload is greater than 8000 pages/month of typical ROP output.

The other is the Lucent Technologies Model 602 dot-matrix printer intended for small office applications where the workload is equal to or less than 8000 pages/month of typical ROP output.

The ROP is connected to the 3B21D computer UN377 Port Switch and Scanner-Distributor Buffer (PSSDB) circuit pack with one of the following ROP cables:

- ED-3T076-20,G7J (50 feet)
- ED-3T076-20,G7L (100 feet)
- ED-3T076-20,G7N (250 feet).

The connection to the UN377 circuit pack is at the Processor Unit 1 backplane at EQL 045-186-132.

9. POWER DISTRIBUTION AND CONTROL

9.1 POWER DISTRIBUTION OVERVIEW

Figure 9-1 shows the typical -48 V DC distribution arrangement for the 3B21D computer Processor Cabinet. The primary power source for the 3B21D computer is -48 V DC from a local battery plant. Power is distributed to the computer via power feeders from a Power Distribution Cabinet (PDC). In international applications, the power feeders connect to dedicated power line Electromagnetic Interference (EMI) filters above the computer cabinet. The EMI filter outputs are routed to the Fuse and Filter Unit (FFU) where they are split into branches to the equipment units and cooling fans. In domestic applications, the power feeders from the PDC connect directly to the FFU. In the equipment units, DC-to-DC converters generate the voltages used by the circuit packs. The cooling fans and a few circuit packs directly use -48 V DC. The DC-to-DC converters are -48 V DC to +5 V DC supplies that plug into the backplane or are board-mounted power modules (BMPMs) that provide power directly to the circuit pack on which they are mounted.

The 3B21D computer complies with the European Telecommunication Standardization Institute (ETSI) extended voltage limits.

9.2 PROCESSOR CABINET POWER DISTRIBUTION

CAUTION 1: Equipment damage can result if the PDC fuses are installed without first unseating the associated 3B21D computer circuit packs that draw -48 V current. To prevent equipment damage, unseat the circuit packs associated with the PDC feeder before installing the PDC fuse for that feeder.

CAUTION 2: Fuse failure will result if the 3B21D computer FFU fuse for a 410AA DC-to-DC converter is installed without first unseating the 410AA converter. To prevent fuse failure, unseat a 410AA converter before installing its fuse in the FFU. Reinstall the 410AA converter after its fuse is installed.

Figure 9-2 is a rear view of the FFU in the Processor Cabinet showing how blocks of fuses split the feeders into branches to the internal units. Table 9-1 identifies the -48 V DC loads for associated power feeder, fuse, and branch.

Power feeders originating from PDC Buses 0 and 1 terminate in the FFU in the 3B21D computer Processor Cabinet. Note that some 3B20D computer applications refer to these buses as Bus A and Bus B, respectively. The left half of the FFU distributes power from PDC Bus 0 (6 feeders) to Processor Unit 0; the right half distributes power from PDC Bus 1 (6 feeders) to Processor Unit 1.

In the FFU, blocks of fuses split the feeders into branches to the internal units. Each branch is protected with a single fast-blow fuse. The fuse blocks contain a "fuse-alarm" light-emitting diode (LED) associated with each fuse position and two alarm outputs that signal a fuse blowing event. The failure of any fuse is indicated via a LED indicator on the indicator strips above the cabinet doors at the front and rear of the Processor Cabinet. Fuse blowing transients are minimized by capacitors (one per feeder). Each 4700 □F capacitor has a 10-K ohm bleeder resistor. Each processor can require up to 33 branches (2 to 9 branches per feeder).

Since the 3B21D computer FFU has electrolytic filter capacitors on the input power feeders, a charging tool must be used when installing 3B21D computer fuses at the Power Distribution Cabinet (PDC). See ***Caution 1***.

Also note that when installing a fuse in the 3B21D computer FFU that protects a 410AA DC-to-DC converter, the 410AA must be unseated to prevent fuse failure. After a 410AA fuse is installed, the associated 410AA can be installed because the converter latch switch circuit limits the inrush current and prevents fuse failure. See ***Caution 1*** and ***Caution 2***.

Figure 9-1 Typical -48 V DC Distribution

Table 9-1 Processor Cabinet -48 V DC Loads

POWER FEEDER [a]	FUSE LOCATION (PROC 0, PROC 1)		LOAD [b], [c]	BRANCH	PEAK CURRENT @ 40.5 V (Amps) [d]	FUSE RATING (Amps)	WIRE SIZE (AWG)
	FIG. 9-2	EQL					
A(0,1)	D(1,19)	014D,186D	PWR A	N48V02	6.7	10	14
	C(1,19)	014C,186C	CUPS	N48V01	0.2	3.0	16
	B(1,19)	014B,186B	PC00-01	N48V07	0.1	3.0	16
	A(1,19)	014A,186A	PC02-03	N48V08	0.1	3.0	16
					7.1		
B(0,1)	D(2,18)	023D,177D	PWR B	N48V03	6.4	10	14
	C(2,18)	023C,177C	PC10-11	N48V09	0.1	3.0	16
	B(2,18)	023B,177B	FAN A, FAN G	N48VF(A,G)	0.8	3.0	16
	A(2,18)	023A,177A	PC22-23	N48V12	0.1	3.0	16
					7.4		

C(0,1)	D(3,17)	032D,168D	PWR C	N48V05	3.1	10	14
	C(3,17)	032C,168C	IOPPS	N48V04	2.0	5.0	16
	B(3,17)	032B,168B	FAN B, FAN F	N48VF(B,F)	0.8	3.0	16
	A(3,17)	032A,168A	PC12-13	N48V10	0.1	3.0	16
					6.0		
D(0,1)	D(4,16)	041D,159D	PWR D	N48V06	3.1	10	14
	C(4,16)	041C,159C	PC20-21	N48V11	0.1	3.0	16
	B(4,16)	041B,159B	FAN C, FAN E	N48VF(C,E)	0.8	3.0	16
	A(4,16)	041A,159A	PC30-32 [SPU04, SPU05]	N48V13	0.15 [1.3]	3.0	16
					4.15 [5.3]		
E(0,1)	D(5,15)	050D,150D	PWR E [e]	N48V15	1.5	10	14
	C(5,15)	050C,150C	DFC 0, DFC 1	N48V14	0.2	3.0	16
	B(5,15)	050B,150B	SPU00, SPU01	N48V16	1.3	3.0	16
	A(5,15)	050A,150A	SPU02, SPU03	N48V17	1.3	3.0	16
E(0,1)	D(6,14)	059D,141D	SPU54, PSSDB	N48V18	1.0	3.0	16
	C(6,14)	059C,141C	PWR H [e]	N48V19	1.5	10	16
	B(6,14)	059B,141B	SPU18, SPU19 [DFC 2,]	N48V20	0.2 [1.3]	3.0	16
	A(6,14)	059A,141A	PC32-33 [SPU20, SPU21]	N48V21	0.1 [1.3]	3.0	16
					7.1 [9.4]		
F(0,1)	D(7,13)	073D,127D	PWR F	N48V22	3.1	10	14
	C(7,13)	073C,127C	IOPPS	N48V23	2.0	5.0	16
	B(7,13)	073B,127B	PC00-01	N48V24	0.1	3.0	16
	A(7,13)	073A,127A	PC02-03	N48V25	0.1	3.0	16
F(0,1)	D(8,12)	082D,118D	spare	N48V26			
	C(8,12)	082C,118C	spare	N48V27			
	B(8,12)	082B,118B	PC10-11	N48V28	0.1	3.0	16
	A(8,12)	082A,118A	PC12-13	N48V29	0.2	3.0	16
F(0,1)	D(9,11)	091D,109D	PWR G* [spare] [f]	N48V30	3.1 [0.0]	10	16
	C(9,11)	091C,109C	PC20-21 [SPU26, SPU27]	N48V31	0.1 [1.3]	3.0	16
	B(9,11)	091B,109B	PC22-23 [SPU24, SPU25]	N48V32	0.1 [1.3]	3.0	16
	A(9,11)	091A,109A	PC30-32 [SPU22, SPU23]	N48V33	0.1 [1.3]	3.0	16
					9.0 [9.5]		

Notes:

a. The power feeder designation "(0,1)" connects to Processor 0 and 1 from PDC Bus 0 and Bus 1, respectively.

b. Loads in the Growth Unit are identified with an asterisk (*).

c. An SPU can be a UN375 MHD or UN376 MT circuit pack.

d. Alternate loads are in square brackets (**[ ]**).

e. PWR E, PWR H, N48V15, and N48V19 are not equipped if DFC 0 and DFC 1 use a UN580B.

f. PWR G (410AA) is omitted if N48V21, N48V31, N48V32, and N48V33 feed SPUs.

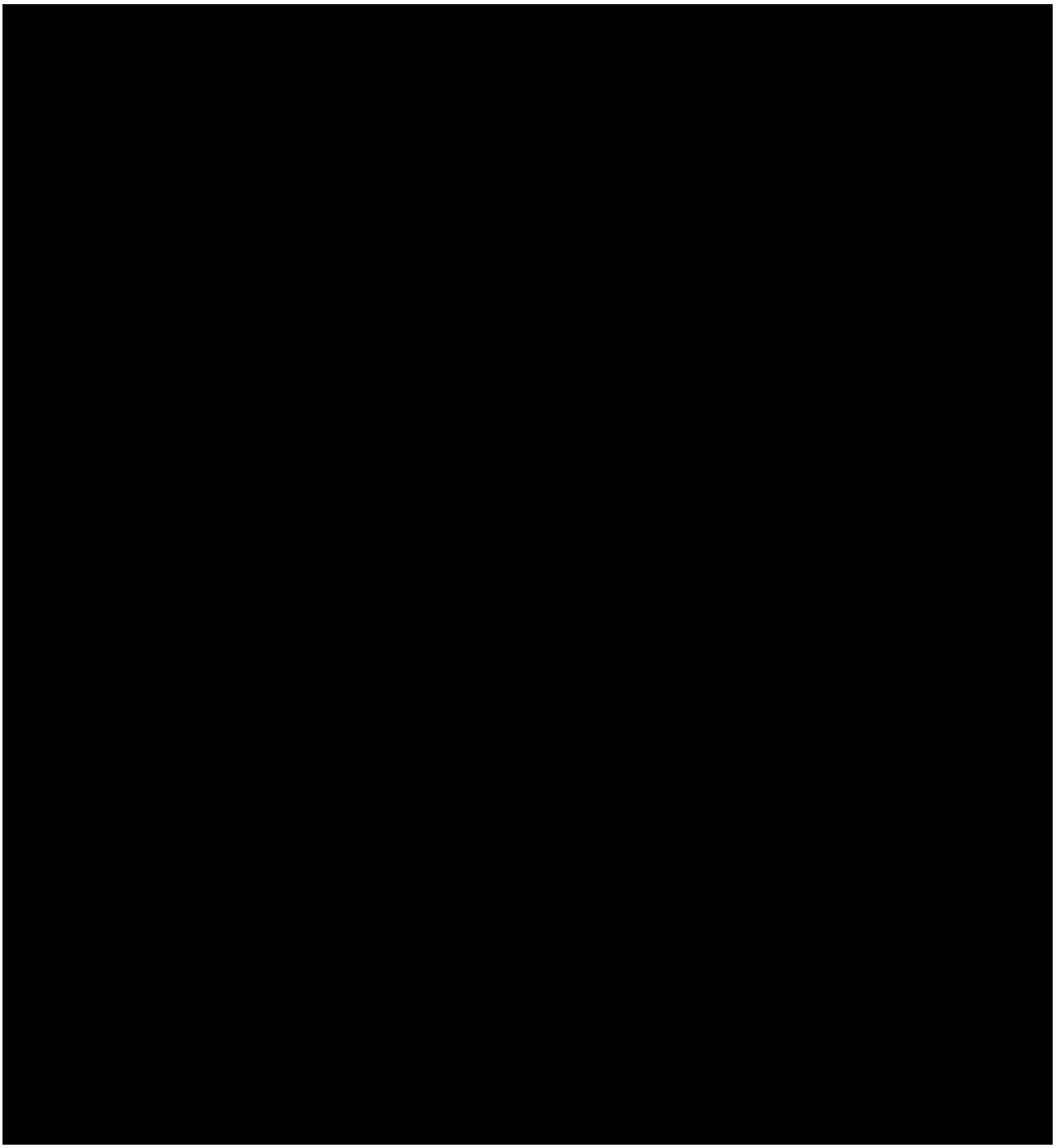


Figure 9-2 Processor Cabinet Fuse and Filter Unit -48 V DC Distribution (Rear View)

9.3 PERIPHERAL GROWTH CABINET POWER DISTRIBUTION

The Peripheral Growth Cabinet provides mounting space for Small Computer System Interface (SCSI) 9-track tape drives. The tape drives require either 120-V AC, 60-Hz or 240-V AC, 50-Hz power. The 9-track tape drives plug directly into AC outlets located within 6 feet of the cabinet.

9.4 PROCESSOR CABINET FUSE ALARMS

Figure 9-3 shows how fuse alarms are reported via scan points. When an FFU fuse blows, the LED next to the fuse lights, and a fuse alarm signal is activated. The failure of any fuse is also indicated via an LED on the indicator strips above the cabinet doors at the front and rear of the Processor Cabinet.

The Processor Cabinet FFU outputs two fuse alarm leads: FA10 monitors the fuses for Processor 1; FA00 monitors the fuses for Processor 0. Each alarm lead is cabled to both the Input/Output Processor (IOP) and Control Unit (CU) power switches, TN1820 and TN1821, where they are converted to scan points (CSCZ and ISCZ). Since all IOP scan and signal-distributor points are cross-connected between processors, a blown fuse is reported by two scan points (one in each processor). This permits reporting the failure of a fuse that protects a power switch (TN1820/TN1821) or a Scanner and Signal Distributor Controller (SCSDC) circuit pack (UN33). The failure is also reported via an output message on the Receive-Only Printer (ROP).

9.5 FAULT GROUPS

9.5.1 Processor Unit

The Processor Unit has three fault groups: CU, Disk File Controller (DFC), and IOP. The power for these fault groups is independently generated and controlled. The minimum entry computer is equipped with DC-to-DC converters CONVA and CONVC. The DC-to-DC converters CONVB and CONVD are added as the CU and IOP communities grow. Some systems that use earlier DFC controllers will have a CONVE.

9.5.2 Growth Unit

The Growth Unit has two fault groups: DFC and IOP. The growth apparatus unit is used to expand the number of Peripheral Controllers (PCs) and/or the number of SCSI peripheral units (SPUs). SPU expansion is done by adding a DFC, SPUs, and a DC-to-DC converter (CONVH). PC expansion is done by using SCSI bus extension cables from DFC 0 and DFC 1 or by adding another DFC. Additional IOPs can be grown in either Growth Unit by adding IOP circuit packs. The power converter provided with the IOP circuit pack powers the first and second PC communities (0 and 1) in each Growth Unit. Additional power converters are required to power PC communities 2 and 3 in each Growth Unit.

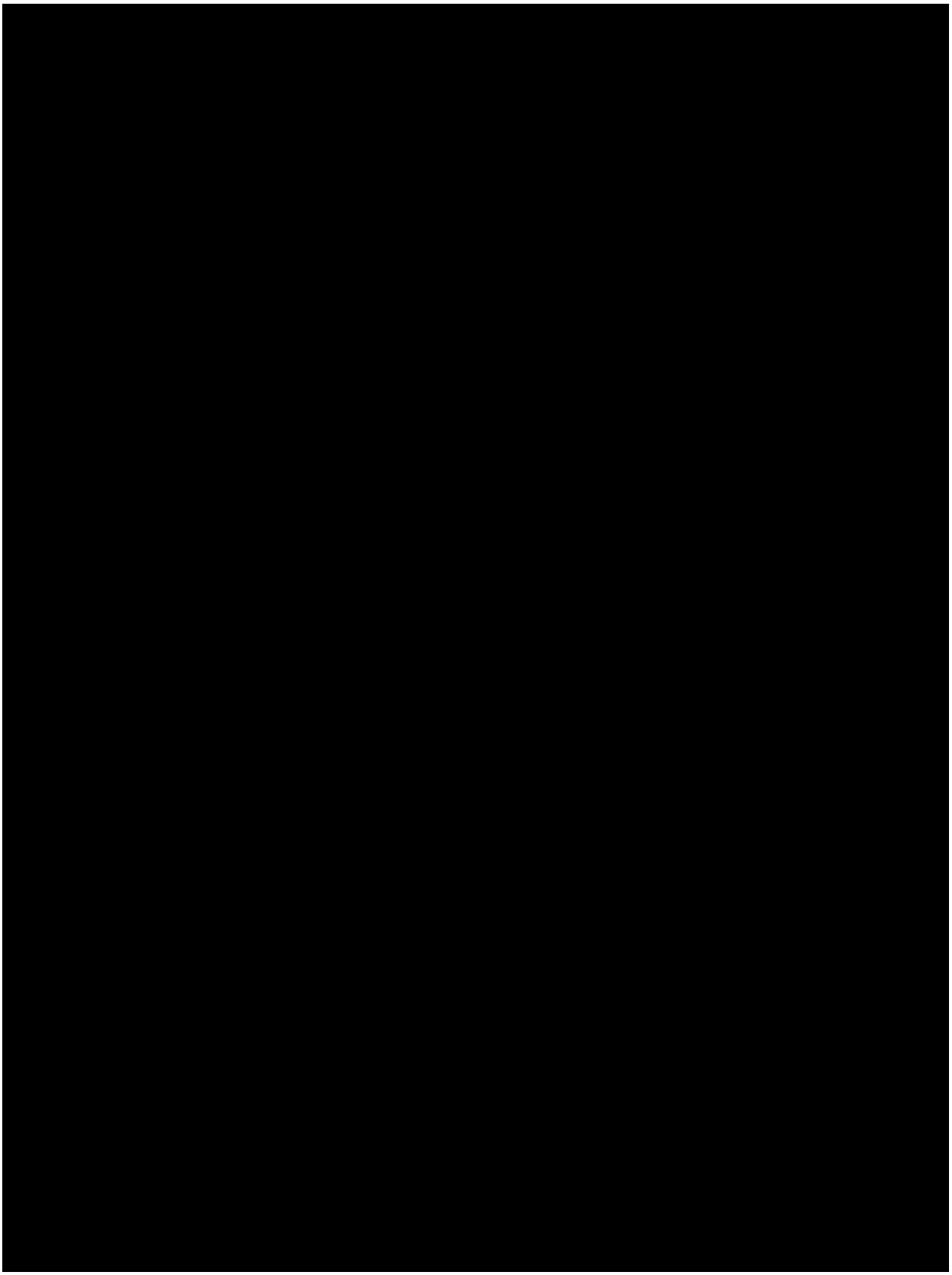


Figure 9-3 Fuse Alarm Functional Block Diagram

9.6 PROCESSOR UNIT POWER DISTRIBUTION

The 3B21D computer Processor Unit can contain up to five power converters (CONVA through CONVE). Figure 9-4 shows these five converters, and the circuit packs they serve. Two of the converters, CONVA and CONVC, are always equipped. CONVB and CONVD are optionally equipped. Control for the power converters is in the TN1821 Control Unit Power Switch (CUPS), TN1820 [IOP Power Switch (IOPPS)], and the UN373 (DFCA) circuit packs. The power converters and their controllers require -48 V DC as a supply voltage. DFCA (UN373) is unlike the other two power control circuit packs in that power control is only a small part of its functionality. DFCA also uses the 5 V from an onboard converter to supply its internal logic. Earlier DFCA configurations will receive a CONVE.

Figure 9-4 shows there are 18 separate -48 V branches to the Processor Unit backplane. Each converter and power switch has a fused power input. Likewise, each SCSI peripheral has a fused input. In PC Communities 0, 1, and 2, two -48 V branches are provided per community, with one branch per slot pair. The primary purpose of these -48 V feeds are to power optional SCSI units in the PC community. The only current PC card supported by the 3B21D requiring -48 V is the UN33 and UN933. In PC community 3, one -48 V branch supplies all three slots. Finally, 5 V from CONVC is routed to the SPU54/Port Switch and Scanner-Distributor Buffer (PSSDB) position for use by the PSSDB. The PSSDB uses -48 V from the backplane and 5 V from CONVC. The SPU54 uses only -48 V from the backplane.

The PC Communities also require □12 V and -5 V, which are provided by the IOPPS. The □12 V supplies on the IOPPS are rated at 50 watts each. As indicated in Figure 9-4 , the -48 V return is isolated from frame and logic ground. All other supply voltages have their returns tied to logic and frame ground.

The circuit pack designation strips on the unit are color-coded to show which DC-to-DC converters supply power to the various circuit pack positions. Figure 9-4 identifies this color-coding for each of the converters.

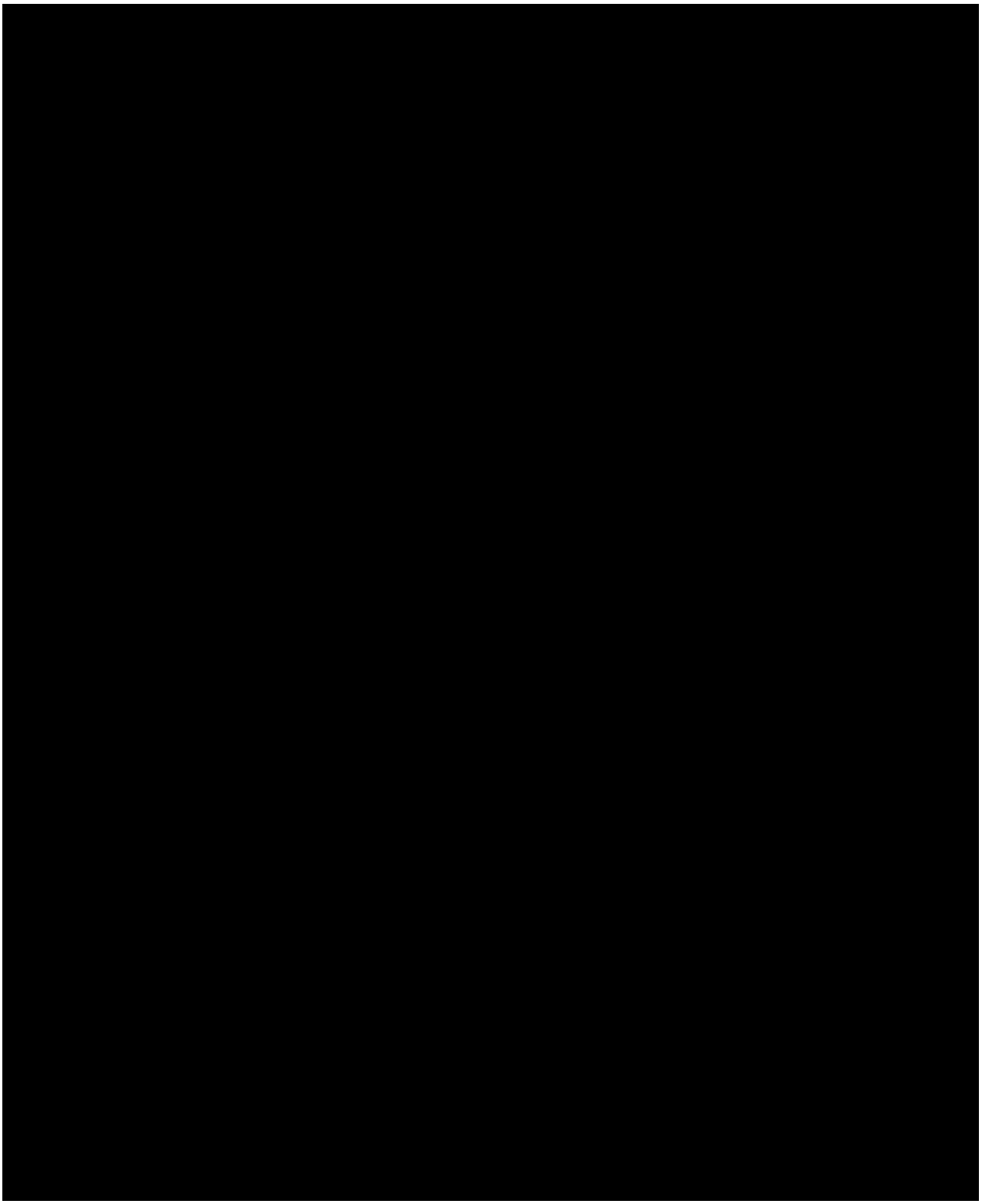


Figure 9-4 Processor Unit Power Groups

9.7 PROCESSOR UNIT POWER INTERLOCKS

CAUTION: It is strongly emphasized that hot insertion or removal of circuit packs into any of these positions is NOT an allowable procedure. Equipment damage can result. Remove power from the circuit pack(s) using the appropriate power switch(es) before installing or removing circuit packs.

The power interlocks in the Processor Unit are designed to shut down the power converters if any *critical* circuit packs are removed while the power switch and converters are in operation. The power interlocks also prevent powering up if the *critical* circuit packs are not installed. For the Control Unit (CU) power group, the critical circuit packs are the MM (KLW32, KLW40, KLW48, KLW64, or KLW128), DMA 0 (KBN15), and CC (KLW31). For the IOP power group, the critical circuit pack is the IOP (KBN10). Finally, for the DFC power group, the critical pack is the DFCB (TN2116) when the UN373 is equipped. Otherwise, the UN580 and UN580B do not use interlocks.

Figure 9-5 shows the interlocks are passed through each power group's primary converter and then to the critical circuit packs. The CINTA0, IINTA0, and DINTA0 inputs to each power group must sense a logic "0" for normal operation. A break in the primary interlock connection causes the power converter to activate its major alarm output. If the attached power converter had been operating, it is turned off. If the break occurs during converter start up, the converter is not started. Therefore, hot removal of any critical circuit pack or converter will shut down that power group. Likewise, hot insertion is not possible, since power is not applied unless all critical circuit packs are installed.

On the CU and IOP power groups, secondary interlock inputs are provided that are intended to detect the need for a growth power controller. Installation of a circuit pack at the DMA 1, EX 0, or EX 1 positions requires power converter CONVB to be installed. Installation of a circuit pack in any of the positions in PC communities 2 or 3 requires CONVD to be installed. The secondary interlocks are shown in Figure 9-5 as CINTB0 and CINTC0 for the CUPS, and as IINTB0 and IINTC0 for the IOPPS. If either one of the secondary interlock circuits is closed, and the other open, the corresponding power switch will activate its major alarm output and turn off both the primary and secondary power converters. If CONVD is installed but there are no circuit packs in the associated PC slots, the power is not turned off because there is nothing to shut down. If there is a PC circuit pack installed in a PC slot associated with CONVD, but CONVD is not installed, an alarm is activated.

Note that PC communities 0 and 1 are not interlocked. Circuit packs in these positions may be removed or installed with power on without detection by the IOPPS power switch. Furthermore, if at least one circuit pack is installed in PC communities 2 or 3, then hot insertion/removal of packs at other positions will not activate the IOPPS interlock. The CUPS is interlocked with the DMA 1, EX 0, and EX 1 positions as an OR'd function. If one position is equipped, the other two positions may be installed/removed without detection by the CUPS interlocks. See ***Caution***.

The PC community interlocks do not apply when an SCSI peripheral circuit pack is installed. The SCSI circuit packs contain their own power converters and power switches. A SCSI circuit pack may be installed into a PC community slot without affecting either the 5-V power or the logic connections to the remainder of the community.

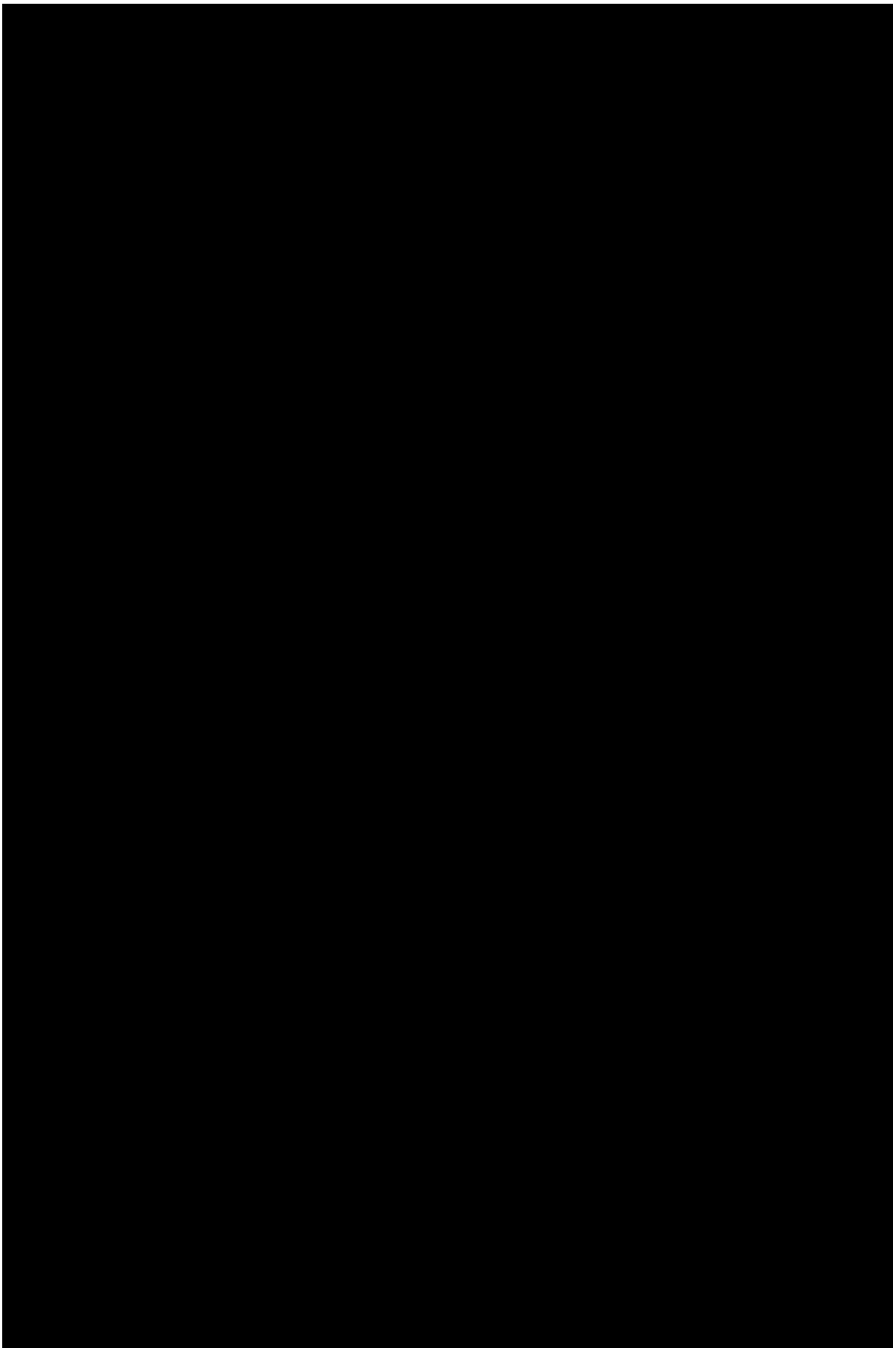


Figure 9-5 Processor Unit Power Interlocks

9.8 GROWTH UNIT POWER DISTRIBUTION

The 3B21D computer Growth Unit can contain up to three power converters (CONVF, CONFG, and CONVH). Figure 9-6 illustrates these three converters and the circuit packs they serve. Control for the power converters is in the TN1820 (IOPPS) and the UN373 or UN580 (DFCA) circuit packs. The power converters and their controllers require -48 V DC as a supply voltage. DFCA (UN373) is unlike the other two power control circuit packs in that power control is only a small part of its functionality. DFCA also uses the 5 V from the converter it controls to supply its other internal logic. The UN580B, if equipped as DFCA, has onboard power converters and does not require CONVH.

Figure 9-6 shows there are 13 separate -48 V branches to the growth backplane. Each converter and power switch has a fused power input. Likewise, each SCSI peripheral has a fused input. In PC Communities 0, 1, 2, and 3, two -48 V branches are provided per community, with one feed per slot pair. The primary purpose of these -48 V feeds are to power optional SCSI units in the PC community. The only current PC circuit pack supported by the 3B21D computer requiring -48 V is the UN33 and UN933 circuit pack.

CONVF supplies +5 V to the PC Communities 0 and 1. CONVG supplies +5 V to the PC Communities 2 and 3. The PC Communities also require □12 V and -5 V, which are provided by the IOPPS. The □12 V supplies on the IOPPS are rated at 50 to 150 watts each, depending on which version of the IOPPS is equipped.

As indicated in Figure 9-6 , the -48 V return is isolated from frame and logic ground. All other supply voltages have their returns tied to logic and frame ground.

The circuit pack designation strip on the unit is color-coded to show which DC-to-DC converters supply power to the various circuit pack positions. Figure 9-6 identifies this color-coding for each of the DC-to-DC converters.

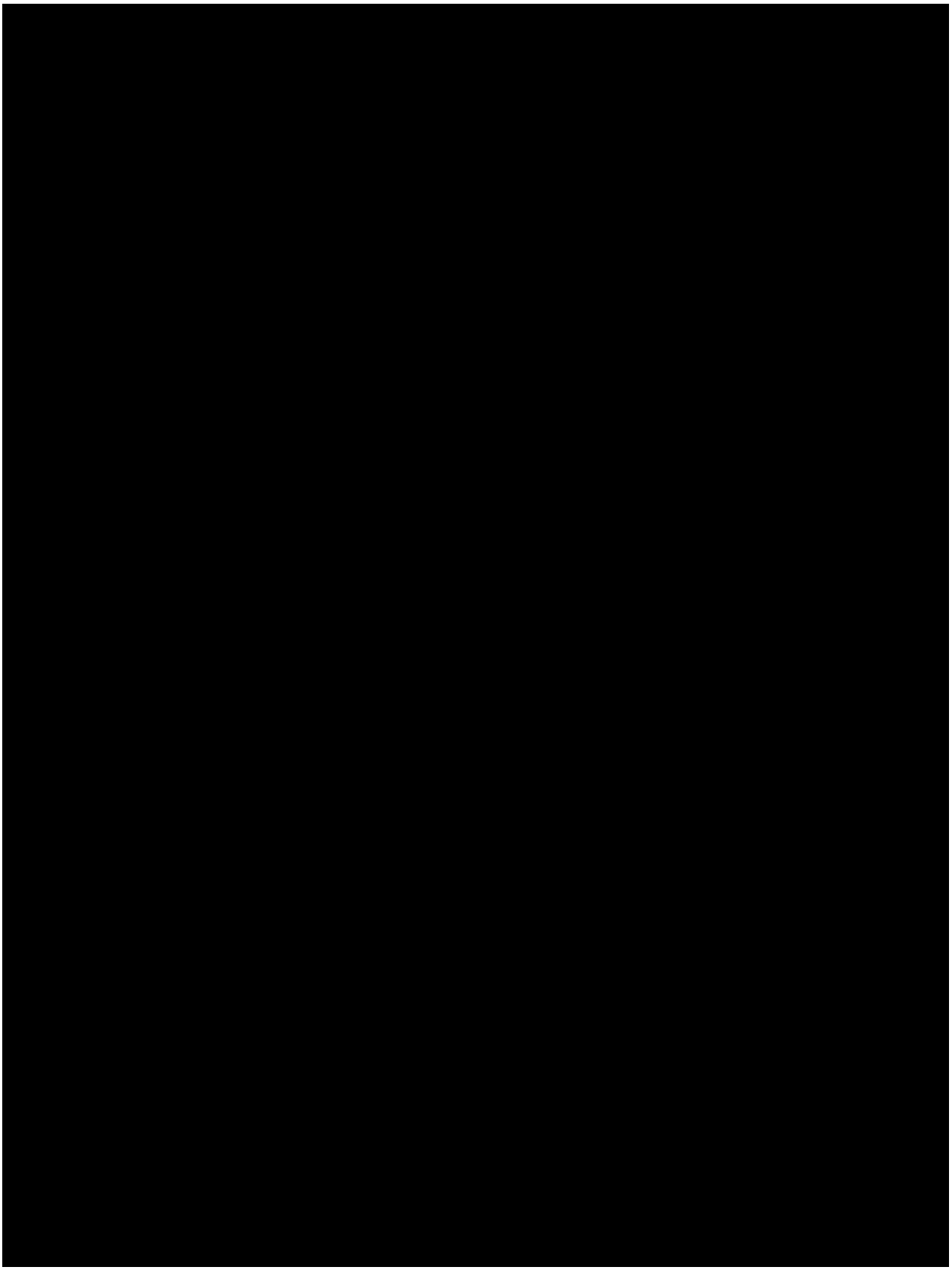


Figure 9-6 Growth Unit Power Groups

9.9 GROWTH UNIT POWER INTERLOCKS

CAUTION: It is strongly emphasized that hot insertion or removal of circuit packs into any of these positions is NOT an allowable procedure. Equipment damage can result. Remove power from the circuit pack(s) using the appropriate power switch(es) before installing or removing circuit packs.

The power interlocks in the Growth Unit are designed to shut down the power converters if any *critical* circuit packs are removed while the power switch and converters are in operation. The power interlocks also prevent powering up if the *critical* circuit packs are not installed. For the IOP power group, the critical circuit pack is the IOP (KBN10). For the DFC power group, the critical pack is the DFCB (TN2116) when DFCA is the UN373. Otherwise, the UN580 and UN580B do not use interlocks.

Figure 9-7 shows how the interlocks are passed through each power group's primary converter and then to the critical circuit packs. The CINTA0, IINTA0, and DINTA0 inputs to each power group must sense a logic "0" for normal operation. A break in the primary interlock connection causes the power converter to activate its major alarm output. If the attached power converter had been operating, it is turned off. If the break occurs during converter start up, the converter is not started. Therefore, hot removal of any critical circuit pack or converter will shut down that power group. Likewise, hot insertion is not possible, since power is not applied unless all critical circuit packs are installed.

Secondary interlock inputs are provided on the IOP power groups, which are intended to detect the need for a growth power controller. Installation of a circuit pack in any of the positions in PC communities 2 or 3 requires CONVG to be installed. The secondary interlocks are shown in Figure 9-7 as IINTB0 and IINTC0 for the IOPPS. If either one of the secondary interlock circuits is closed, and the other open, the corresponding power switch will activate its major alarm output and turn off both the primary and secondary power converters. If CONVG is installed but there are no circuit packs in the associated PC slots, the power is not turned off because there is nothing to shut down. If there is a PC circuit pack installed in a PC slot associated with CONVG, but CONVG is not installed, an alarm is activated.

Note that PC communities 0 and 1 are not interlocked. Circuit packs in these positions may be removed or installed with power on without detection by the IOPPS power switch. Furthermore, if at least one circuit pack is installed in PC communities 2 or 3, then hot insertion/removal of packs at other positions will not activate the IOPPS interlock. See ***Caution***.

The PC community interlocks do not apply when an SCSI peripheral circuit pack is installed. The SCSI circuit packs contain their own power converters and power switches. A SCSI circuit pack may be installed into a PC community slot without affecting either the 5-V power or the logic connections to the remainder of the community.

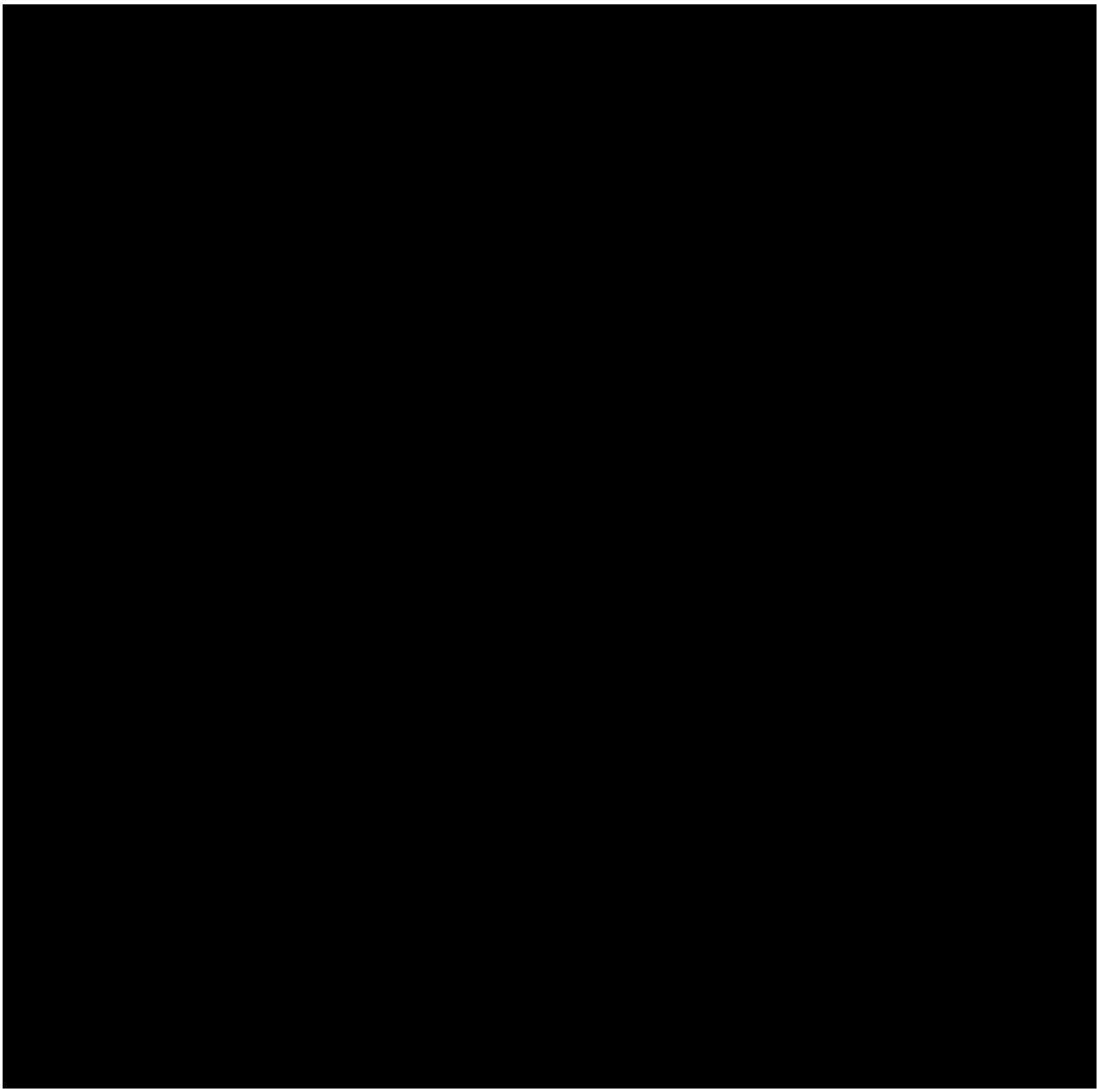


Figure 9-7 Growth Unit Power Interlocks

9.10 410AA *Fastech*® POWER CONVERTER

CAUTION: When installing a fuse in the 3B21D computer Fuse and Filter Unit (FFU) for a 410AA converter, the converter must be unseated. Fuse failure will result if the fuse for a 410AA DC-to-DC converter is installed without first unseating the 410AA converter. To prevent fuse failure, unseat a 410AA converter before installing its fuse in the FFU. Reinstall the 410AA converter after its fuse is installed.

The 410AA Power Converter is a 310-watt DC-to-DC converter that operates from -48 V DC and outputs +5 V DC at 62 amperes. Some of the 410AA converter features are as follows:

- A latch switch mechanically locks the converter in place when closed (pushed in). When the latch switch is open (pulled out), the latch switch circuit limits the inrush current when the converter is installed. See ***Caution***. Converter start is controlled by the associated power switch circuit pack (TN1820, TN1821, or UN373).

- High output voltage shutdown.
- Programmable Over-Current Shutdown (POCS).
- The front panel has the following features:
  - Test points for the output voltage.
  - An amber Out-of-Service (OOS) indicator.
  - A red indicator used for any alarm or shutdown condition. For example, a low output voltage alarm turns on this indicator.

9.11 BOARD-MOUNTED POWER MODULES (BMPMs)

Board-mounted power modules (BMPMs) provide power directly to the circuit pack on which they are mounted. The following circuit packs use BMPMs:

- TN1820 Input/Output Processor Power Switch (IOPPS) circuit pack
- TN1821 Control Unit Power Switch (CUPS) circuit pack
- UN376 SCSI Digital Audio Tape (DAT) drive circuit pack
- UN377 Port Switch and Scanner-Distributor Buffer (PSSDB) circuit pack
- UN580B Disk File Controller (DFC) circuit pack.

9.11.1 FE050B +12 V Board-Mounted Power Module

The FE050B +12 V board-mounted power module is a 50-watt DC-to-DC converter that operates from -48 V and provides a +12 V output. The FE050B is used on the TN1820 circuit pack.

9.11.2 FE150B +12 V Board-Mounted Power Module

The FE150B is a 150-watt version of the FE050B. The TN1820C uses two FE150B modules to provide its +12 V and -12 V outputs. The TN1820D uses one FE150B for the 12-V output and one FE050B for the -12 V output.

9.11.3 JW030A +5 V Board-Mounted Power Module

The JW030A +5 V board-mounted power module is a 30-watt DC-to-DC converter that operates from -48 V DC and provides a +5 V DC output. The JW030A module is used on the UN375, UN376, and UN580B circuit packs.

9.11.4 JW030B +12 V Board-Mounted Power Module

The JW030B +12 V board-mounted power module is a 30-watt DC-to-DC converter that operates from -48 V DC and provides a +12 V DC output. The JW030B is used on the UN375 and UN376 circuit pack.

9.11.5 ME005A +5 V Board-Mounted Power Module

The ME005A +5 V board-mounted power module is a 5-watt DC-to-DC converter that operates from -48 V DC and provides a +5 V DC output. The ME005A module provides power to the power and alarm circuits. This separate power module is used for the power control and alarm circuits to increase system reliability. If

the power from the +12 V converter or the other +5 V converter fails, the power control and alarms circuits will still operate to control shutdown and the display indicators. The ME005A is used on the TN1820, TN1821, UN375, UN376, and UN377 circuit packs.

9.11.6 TW070AB Dual Voltage +5 and +12 V Board-Mounted Power Module

The TW070AB board-mounted power module is a 70-watt converter that operates from -48 V DC and provides a +5 V and +12 V DC output. It is used on the UN375E to power the disk drive.

9.12 POWER CONTROL SWITCH FUNCTIONS

The power for the three processor fault groups is controlled by power switch functions contained in three circuit packs types: the TN1821 CU Power Switch (CUPS), the TN1820 IOPPS, and the UN373, UN580, or UN580B DFCA circuit pack.

Figure 9-8 shows the UN373 DFCA circuit pack. A description of the 3B21D computer power switches and LEDs is given in Tables 9-2 and 9-3 .

NOTE: The 3B21D computer power switch faceplate differs from the 3B20D computer. The ON and OFF momentary contact pushbuttons are replaced by a 3-position START/ON/OFF rocker switch to provide the auto-restart feature.

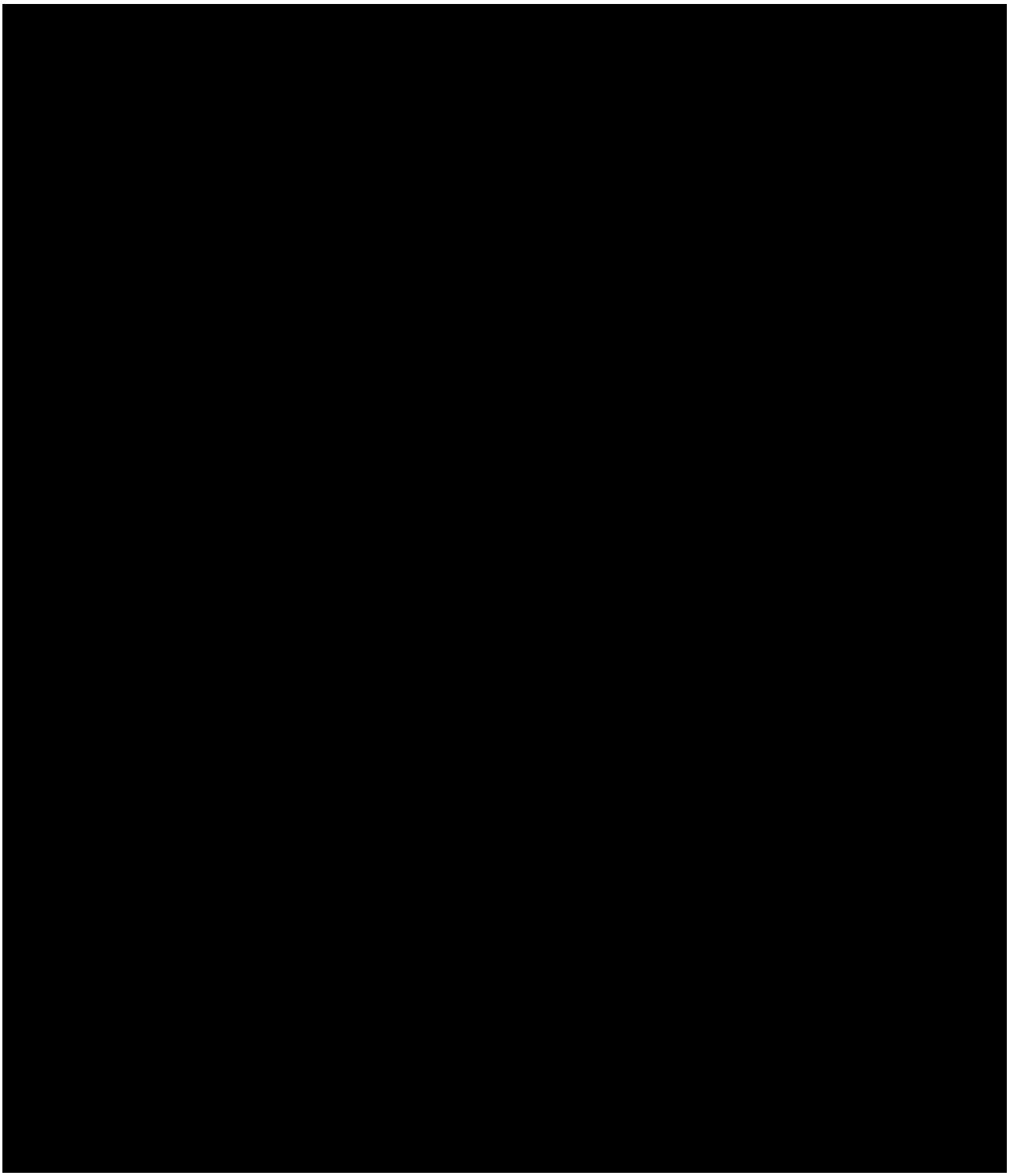


Figure 9-8 Power Switch Faceplate

Table 9-2 Power Switch Faceplate Switch Functions

NAME	TYPE	FUNCTION
START/ON/OFF	3-POSITION ROCKER	Controls 5-V power. OFF functions only if the OOS SD input is active or if the MOR pushbutton is pressed. ON allows auto-restart when N48V is applied. START (the momentary position) turns on power. The ACO-T switch must be off.
ROS/RST	2-POSITION ROCKER	Sends a request via the scan points to remove the unit from service (ROS position) or to restore it to service (RST position). The disposition

		of the request is determined by the system.
ACO-T	2-POSITION ROCKER	Retires major alarms generated by the power switch, locks out the ON function, and tests the faceplate LEDs.
MOR	MOMENTARY CONTACT ROCKER	Overrides the OFF lockout for emergency power off.

Table 9-3 Power Switch Faceplate LED Functions

NAME	COLOR	FUNCTION
OFF	Red	Lights when power has been removed from the fault group or when the ACO-T switch is pressed.
ALM	Red	Lights when a power alarm exists in the fault group or when the ACO-T switch is pressed.
OOS	Amber	Lights when the OOS SD input is active showing that the fault group is out-of-service or when the ACO-T switch is pressed.
RQIP	Green	Lights when the RQIP SD input is active showing that an ROS or RST request has been recognized or when the ACO-T switch is pressed. When the system denies the request, RQIP flashes for a few seconds then extinguishes.
ROS	Green	Lights when the ROS/RST switch is in its ROS position or when the ACO-T switch is pressed.

9.13 SCAN, ALARM, AND SIGNAL DISTRIBUTOR POINTS

All power switch functions have the Scanner and Signal Distributor (SCSD) interface described in Tables 9-4 and 9-5 .

Table 9-4 Power Switch SD Inputs

NAME	FUNCTION
OOS	Active when the fault group is out of service. It controls OOS LED and OFF lockout.
RQIP	Active when ROS or RST has been acknowledged, extinguishes when the request has been granted, and flashes then extinguishes when the request has been denied.

Table 9-5 Power Switch Scan Outputs

+5V PWR [a]	N48V PWR	PWR ALARM	ROS/RST SWITCH [b], [c]	SCAN STATES SCX/Y [d]
ON	ON	0	RST	00
ON	ON	0	ROS	10
ON	ON	1	X [e]	01
X	OFF	X	X	11
OFF	X	X	X	11

Notes:

a. +5 V in the CU and DFC. +5 V and □12 V in the IOP.

b. ROS = Request to remove fault group from service.

c. RST = Request to restore fault group to service.

d. If the pack or scan cable is removed, SCX/Y = 00.

e. X = Don't care.

9.14 CU POWER DISTRIBUTION AND CONTROL

9.14.1 CU Power Distribution

Standard +5 V is distributed to the CU circuit packs via the multilayer backplane (see P5VA and P5VB in Figure 9-9).

The CU (Processor Unit) backplane is divided into two power segments. Each segment is supplied by a dedicated *Fastech*™ -48 V to +5 V DC-to-DC converter. CONVA supplies power to the CC, DMA 0, UC and MEMORY circuit packs; CONVB supplies the DMA 1 pack and two Expansion Slots. Both CONVA and CONVB are controlled by the CU Power Switch circuit pack. The CU Power Switch (CUPS) provides power control, alarms, power reset signals, and the craft interface. In the minimum configuration, only segment A is equipped. CONVB is added when DMA 1 and/or the expansion slots are needed. Backplane power pins are protected from short circuit damage by Programmable Over-Current Shutdown (POCS) via leads CPA(N,P) and CPB(N,P).

9.14.2 TN1821 CU Power Switch (CUPS)

The 3B21D computer CU Power Switch (CUPS) provides the following functions:

- Controls and monitors power for the CU fault group
- Generates power reset signals
- Interfaces the computer through scan and distribute points
- Generates power alarms
- Provides the craft interface (switches and LEDs) to the CU power system
- Provides self-identification.

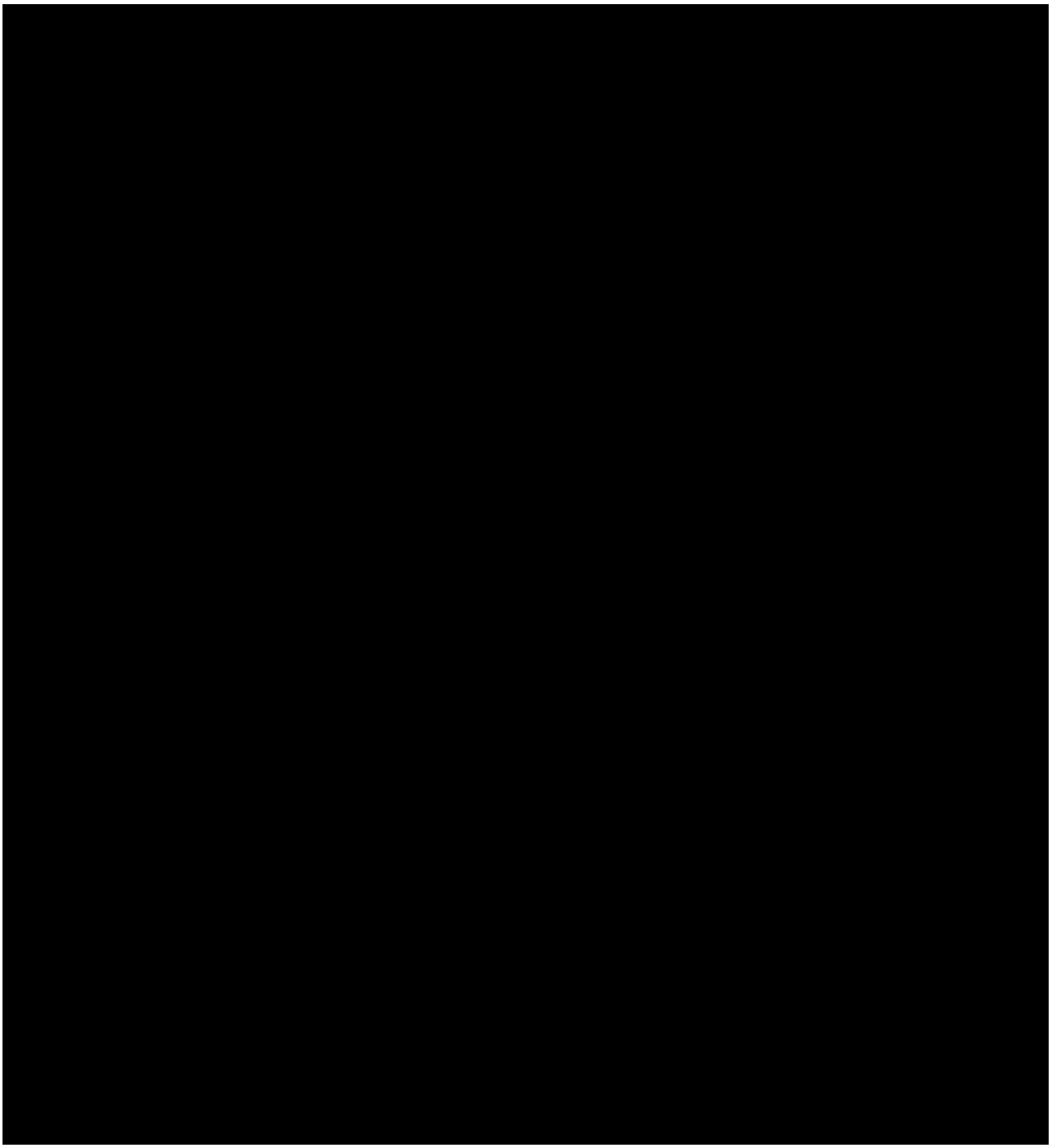


Figure 9-9 CU Power Distribution and Control

9.15 IOP POWER DISTRIBUTION AND CONTROL

9.15.1 Power Distribution

The IOP fault group includes an IOP Controller and four Peripheral Controller (PC) communities with up to four PC circuit packs per community. A fully equipped 3B21D computer can support four IOPs. IOP 0 and IOP 1 are equipped in the Processor Unit for CU 0 and CU 1. IOP 2 is equipped in the Growth Unit at EQL 11-011. IOP 3 is equipped in the Growth Unit at EQL 62-011. Figure 9-10 shows the IOP Power Distribution and Control for a Processor Unit. Figure 9-11 shows the IOP Power Distribution and Control for a Growth Unit.

PC circuit packs require standard +5 V DC along with miscellaneous voltages including □12 V for EIA bus interface circuits (N12E and P12E), and +12 V DC (P12M), and -5 V DC (N5M). A common +12 V supply is used for the P12E and P12M. Therefore, only the P12E is shown in Figures 9-10 and 9-11 .

The IOP is divided into two power segments. The first segment consists of the IOP Controller (KBN10) PC Communities 0 and 1, and the PSSDB (UN377) circuit pack. The second segment consists of PC Communities 2 and 3. For IOP 0 or IOP 1, the CONVC supplies +5 V DC for the first segment; CONVD supplies +5 V DC for the second segment. For IOP 2 or IOP 3, the CONVF supplies +5 V DC for the first segment; CONVG supplies +5 V DC for the second segment. The miscellaneous voltages for both segments are generated by BMPMs on the TN1820 IOP Power Switch (IOPPS) circuit pack. All IOP power is controlled by the IOPPS. Backplane power pins are protected from short circuit damage by Programmable Over-Current Shutdown (POCS) via leads CPC(N,P) and CPD(N,P).

The IOP 1 unit also contains a Port Switch and Scanner-Distributor Buffer (PSSDB) circuit pack that switches MTTY and ROP EIA buses to controllers in Processors 0 or 1, and interfaces office alarms and other non-3B21D computer circuits to the Scanner/Signal-Distributor Controllers in Processors 0 and 1. The PSSDB is located in Processor 1 only; Processor 0 uses the dual function slot for SPU54. The PSSDB uses -48 V from the backplane and P5VC from CONVC. The SPU54 uses only -48 V from the backplane.

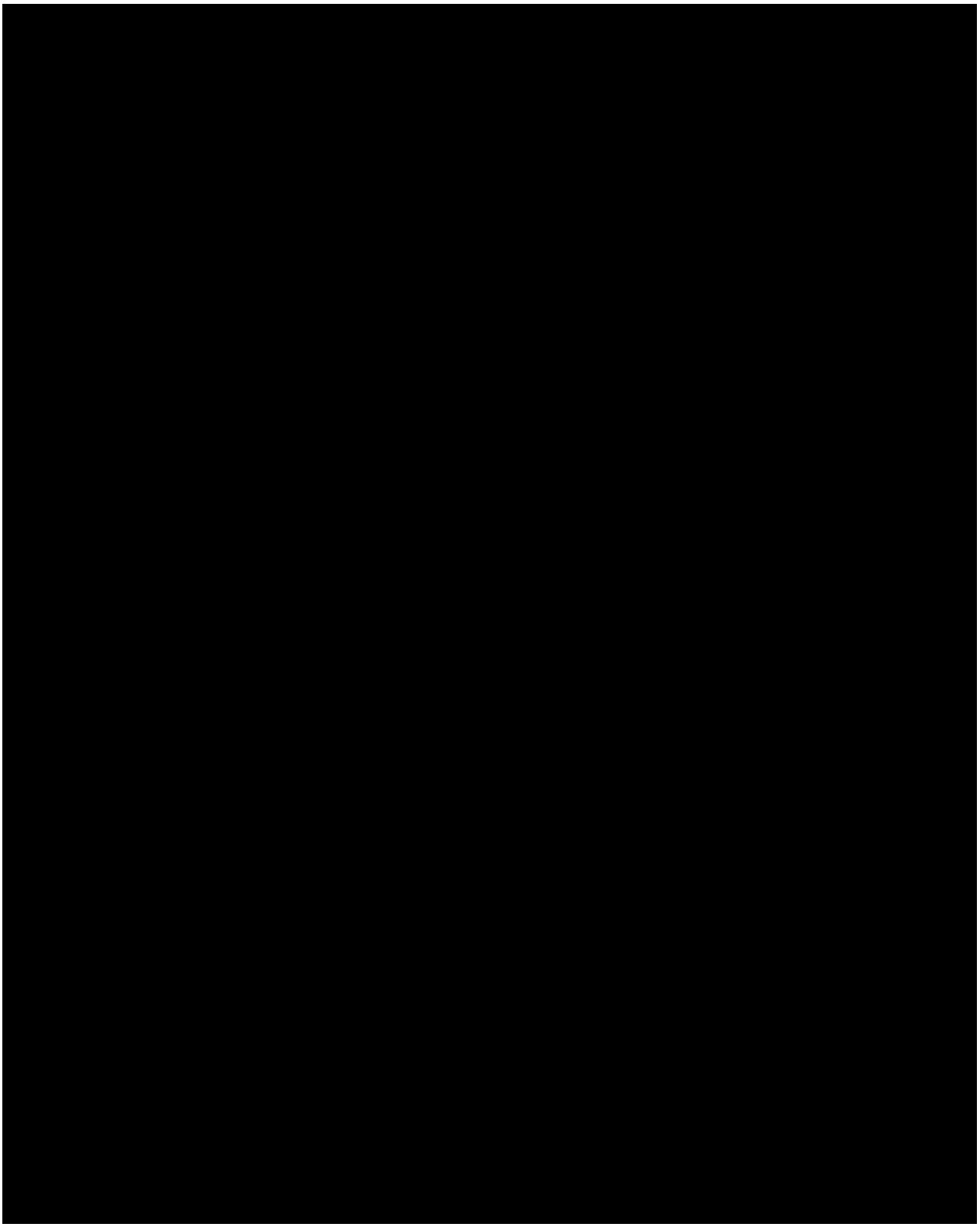


Figure 9-10 Processor Unit IOP Power Distribution and Control

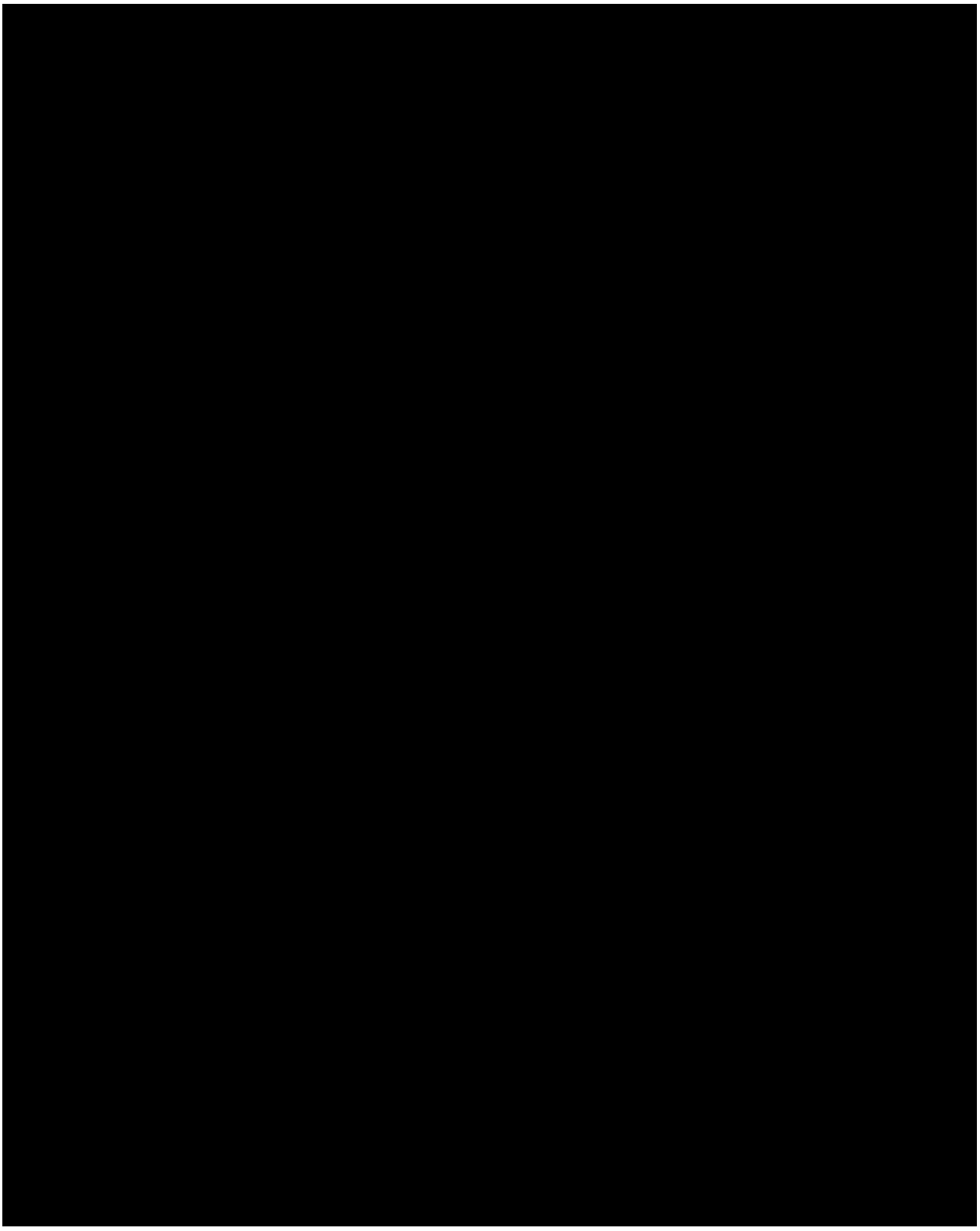


Figure 9-11 Growth Unit IOP Power Distribution and Control

9.15.2 TN1820 IOP Power Switch (IOPPS)

The 3B21D computer IOP Power Switch (IOPPS) provides the following functions:

- Controls and monitors power for the IOP fault group

- Generates and monitors miscellaneous voltages used by the PC Communities
- Generates power reset signals
- Interfaces the computer through scan and distribute points
- Generates power alarms
- Provides the craft interface (switches and LEDs) to the IOP power system
- Links the primary, secondary, and growth Boundary Scan buses
- Self-identification.

The following versions of the TN1820 may be in use:

- TN1820: Does not support auto-power-restart feature.
- TN1820B: Supports the auto-power-restart feature.
- TN1820C: Provides 150-watt +12 and -12 V outputs. The TN1820C is required if the UN582 or UN582B circuit packs are equipped in the IOP community.
- TN1820D: Provides 150-watt +12 and 50-watt -12 V outputs. The TN1820D is required when the UN582 or UN582B circuit packs are equipped in the IOP community. Also, the TN1820D provides full electrical isolation between -48 V supply lines and the frame ground.

9.16 DFC POWER DISTRIBUTION AND CONTROL

The DFC fault group consists of the DFC controller circuit packs and a power converter (not required for DFC controllers that have onboard power converters). Figure 9-12 illustrates the power connections for a DFC configured with a UN373, TN2116, and 410AA. For a DFC that uses a UN580, the TN2116 is not equipped, and the existing connections to it are not used. For a DFC that uses a UN580B, the 410AA converter is not equipped, and those connections are not used. Systems using the UN580B will not have the N48V15 and 48R15 feeders equipped, so it is not possible to use the UN580 or UN373 circuit packs on these systems.

The 3B21D computer is provided with two DFCs. DFC 0 is equipped in Processor Unit 0, and DFC 1 is equipped in Processor Unit 1. A third DFC, DFC 2, can be equipped in the Processor Cabinet, Growth Unit at EQL 11-172. While current systems are shipped with the single DFC controller pack with onboard power (UN580B), earlier systems may use a DFC controller configured with the UN580 and 410AA circuit packs, or the DFC controller may be configured with a combination of UN373, TN2116, and 410AA circuit packs.

The power alarm, power control, power reset, and craft interface functions are still identical in all the different DFC configurations. The same scan and SD points and alarm grid connections are used.

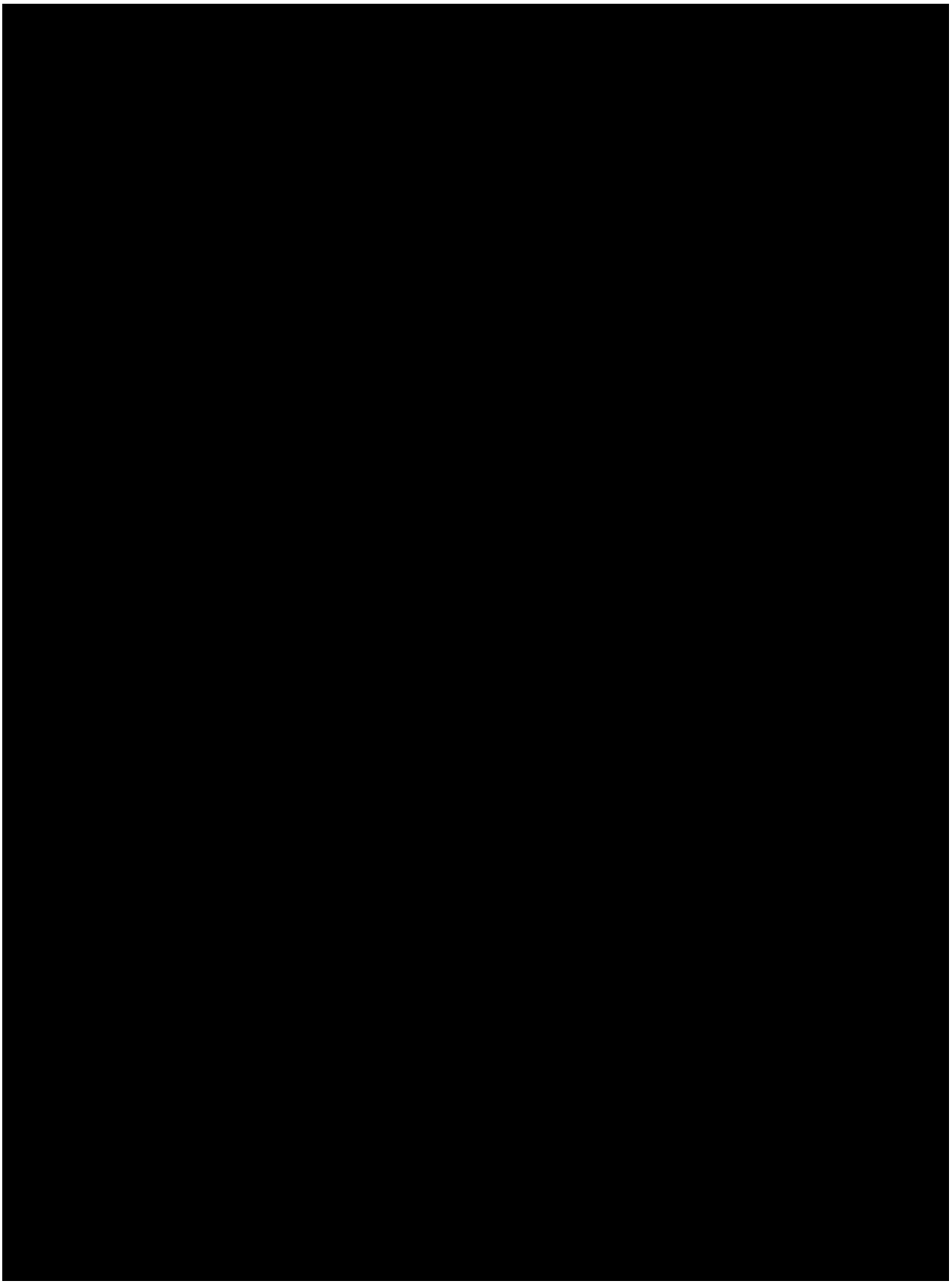


Figure 9-12 DFC Power Distribution and Control

9.17 UN375 SCSI DISK DRIVE AND UN376 SCSI DAT DRIVE POWER CONTROL

The 3B21D computer UN375 Moving Head Disk (MHD) drive and UN376 DAT drive circuit packs contain drives with SCSI bus interfaces, BMPMs, voltage monitors, and power switch circuits as shown in Figure 9-13 .

These packs are self powered. They contain board-mounted power modules that convert -48 V to +5 V and +12 V for the power control circuits, SCSI bus interfaces (if equipped), and the SCSI tape or disk drive units.

Power switch circuits provide the power control, alarm, and interface functions.

See Section 8 for more information about the UN375 and UN376 circuit packs.

9.18 BIDIRECTIONAL COOLING UNIT

The Bidirectional Cooling Unit is equipped in the Processor Cabinet. The unit contains two groups of fans. One group blows air upward to cool Processor 1 and IOP 3-SPU Growth Unit; the other group blows downward to cool Processor 0 and IOP 2-SPU Growth Unit. Figure 9-14 is a functional block diagram of the Bidirectional Cooling Unit power and alarm circuits.

The fan motors operate on -48 V. Fan groups 0 and 1 are supplied from FFU side 0 and 1, respectively. The alarm circuit is powered by N48VFANC and N48VFANG that are OR'd within the alarm circuit board.

Each fan includes an integral Fan Performance Sensor (FPS) that operates from +5 V obtained from a BMPM in the alarm circuit. If one or more fans fail, the circuit latches an alarm state on its scan point output and lights the associated fan indicator (LED) on the cooling unit. A fan indicator is on when a fan is not running. The SD point is used to retire the alarm. A switch on the cooling unit can also be used to manually retire the alarm.

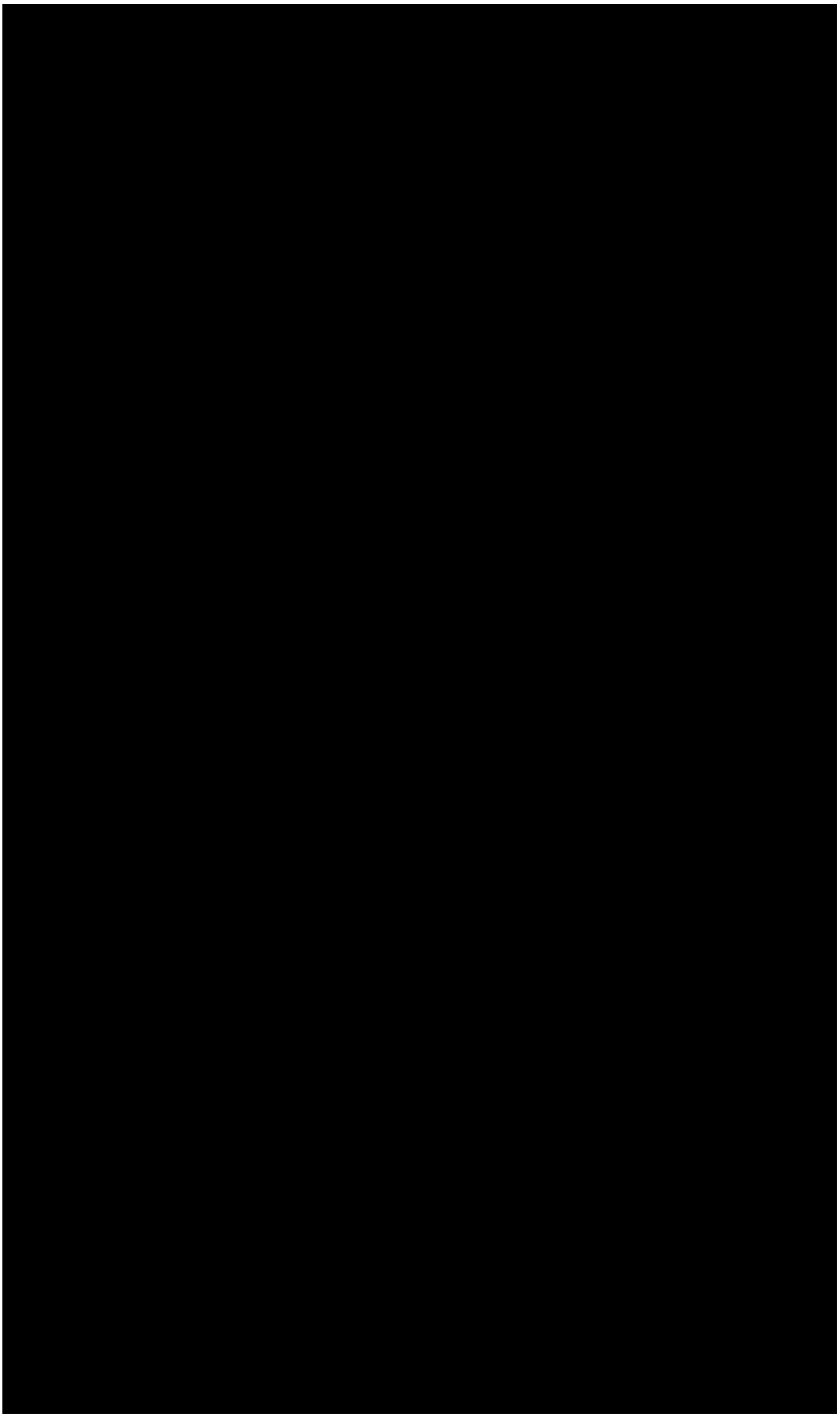


Figure 9-13 UN375 and UN376 Power Distribution and Control

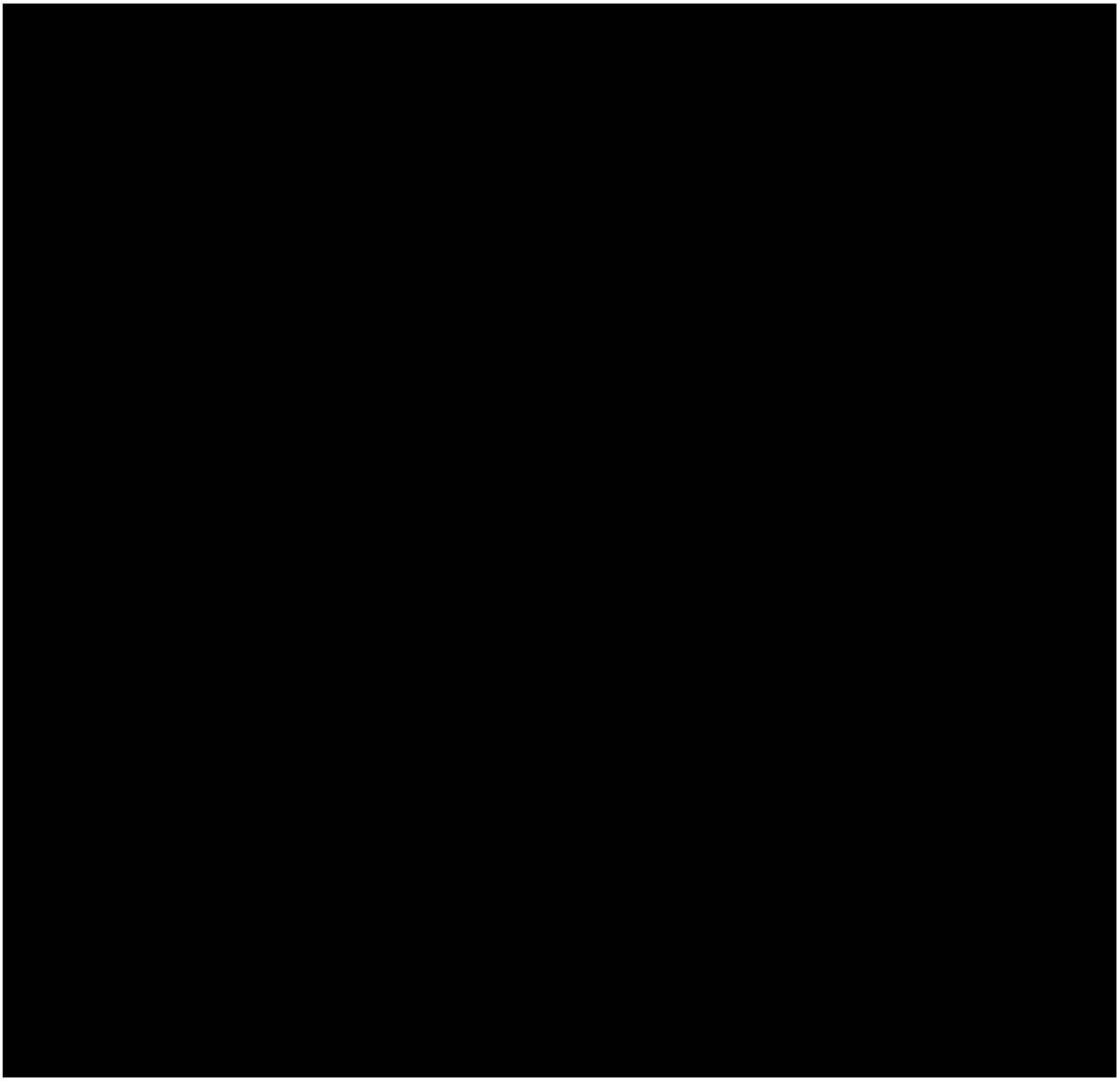


Figure 9-14 Bidirectional Cooling Unit Power and Alarms

9.19 48-V ISOLATION

The following 3B21D computer circuit packs have circuitry that is powered by isolated 48-V DC power. The listed series shown in Table 9-6 will provide complete isolation between both of the 48-V supply leads and 3B21D computer frame ground.

Table 9-6 3B21D Computer Circuit Packs Powered by Isolated 48-V DC

NAME	CIRCUIT PACK
CU Power Switch	TN1821C
IOP Power Switch	TN1820D
DFC Controller	UN580, UN580B
SCSI DAT Circuit Pack	UN376E
SCSI MHD Circuit Pack	UN375E
SCSDC Circuit Pack	UN33-all series, UN933
PSSDB Circuit Pack	UN377

Some earlier series of the previous circuit packs contained voltage-monitoring circuitry that did not fully isolate the 48-V supply from the 3B21D computer frame ground. These are listed in Table 9-7 . These circuit packs will draw about 225 microamperes per circuit pack between -48 V DC and frame ground.

Table 9-7 3B21D Computer Circuit Packs Powered by Not-Fully-Isolated 48-V DC

NAME	CIRCUIT PACK
CU Power Switch	TN1821, TN1821B.
IOP Power Switch	TN1820, TN1820B, TN1820C
DFC Controller	UN373, UN373B
SCSI DAT Circuit Pack	UN376, UN376B, UN376C
SCSI MHD Circuit Pack	UN375, UN375B, UN375C, UN375D

In all cases, there is no connection between the +48 V supply line and frame or logic ground in the 3B21D computer.

10. DOCUMENTATION ROADMAP

10.1 ENGINEERING DRAWINGS

The 3B21D computer mechanical drawings (J-drawings) and schematic drawings (SDs) are identified in Table 10-1 .

Table 10-1 3B21D Computer Drawings

DESCRIPTION	J-DRAWING	SCHEMATIC
3B21D Computer System	J3T061A-1	SD-3T015-01
Processor Cabinet	J3T060A-1	SD-3T014-01
Processor Unit	J3T060AA-1	SD-3T011-01
Bidirectional Fan Unit	J5D003FH-2	SD-5D168-01
Peripheral Growth Cabinet	J3T059A-1	SD-3T013-01
Growth Unit	J3T060AB-1	SD-3T012-01
Modular Fuse and Filter Unit Unit	J5D003FJ-1	SD-5D190-01

10.2 PACKAGING/MANUFACTURING TECHNOLOGIES

Table 10-2 lists the Lucent Technologies internal documents that provide detailed information on the packaging/manufacturing technologies.

Table 10-2 Packaging/Manufacturing Specifications

DOCUMENT NUMBER	DESCRIPTION
MPS-80RG0020	Design criteria for multilayer PWBs
MPS-81RG0003	Design criteria for double-sided PWBs
MPS-82RG0605	Design criteria for compliant printed backplanes
WL-2151	Marking inks requirements/applications
WL-2243	Cover coat□Clear cover coat
WL-2250	Electroplated finishes
WL-2333	Solder finish□Green solder resist coating
X-17199	Plug end of the PWB connectors/fingers requirements
X-17815	MLB PWB requirements
X-18021	UV-curable solder masks
X-18118	MLB end point requirements
X-18300	PWB cleaning
X-18351	PWB repair and modification
X-18386	Connector contacts cleaning
X-19569	*Fastech*® Circuit Pack PWB requirements
X-19602	Backplane assemblies requirements
X-74392	Component data
X-74425	*Fastech*® electronic packaging system guidelines

10.3 SPECIFICATION DRAWINGS

Table 10-3 identifies some of the specification drawings for 3B21D computer equipment.

Table 10-3 Specification Drawings

DOCUMENT NUMBER	DESCRIPTION
KS-23860	Single-Ended SCSI Digital Audio Tape Drive
KS-23908	Differential SCSI Disk Drive
KS-23909	9-Track SCSI Tape Unit
KS-23996	Color Video Terminal (MTTY)
NCR006-3503341 NCR006-3300608/Comcode 407545243 KS-24367,L1/Comcode 407771260	Single-Ended SCSI Digital Audio Tape Drive (UN376) Single-Ended SCSI Digital Audio Tape Drive (UN376C) Single-Ended SCSI Digital Audio Tape Drive (UN376E)
NCR-0026543, Rev. B	602 Dot-Matrix Printer

10.4 REFERENCES

Table 10-4 lists the Lucent Technologies documents supporting the 3B21D computer.

Table 10-4 Lucent Technologies Documentation

DOCUMENT NUMBER	DOCUMENT TITLE
235-105-110	Maintenance Requirements and Tools
235-105-210	Routine Operations and Maintenance
235-105-220	Corrective Maintenance Procedures
235-105-250	System Recovery Manual
235-105-500	*5ESS*®-2000 Switch Maintenance Reference Handbook
235-600-3XX	Equipment Configuration Data/System Generation
235-600-400	Audits Manual
235-600-601	Processor Recovery Messages
235-600-700	Input Messages Manual
235-600-750	Output Messages Manual

11. SYSTEM SPECIFICATIONS

11.1 SPECIFICATIONS OVERVIEW

This section identifies the standards that apply to the 3B21D computer system and briefly summarizes some of the basic environmental specifications. See Table 11-1 . For detailed 3B21D computer system specification information, contact your Lucent Technologies Service Representative.

11.2 STANDARDS

The Lucent Technologies 3B21D computer complies with regulatory and safety standards (requirements) specified by the following standards:

- Network Equipment-Building System (NEBS), Issue 4 (generic equipment requirements)
- *UL*® Standard for Telephone Equipment, UL1459 Safety
- FCC Class A Electromagnetic Compatibility (EMC).

11.3 SYSTEM ENVIRONMENTAL SPECIFICATIONS

Table 11-1 shows the environmental specifications.

Table 11-1 System Environmental Specifications

CHARACTERISTIC	DESCRIPTION
Maximum Ambient Temperature	0 to 50°C (32 to 122°F.)
Operating Humidity	5 to 95%, noncondensing
Operational Altitude	60 meters (197 feet) below sea level to 3,960 meters (12,992 feet) above sea level

12. CONNECTOR AND CABLING INFORMATION

12.1 CABLE ASSEMBLIES OVERVIEW

This section identifies the various cable assemblies used for the 3B21D computer. The following Equipment Drawings are included:

- Connectorized Switchboard Cable Assemblies, ED-3T076-20
- Flex Tape Cable, ED-3T076-40
- Formed Cable, ED-3T076-50
- Paddleboards, 9824A
- Small Computer System Interface (SCSI) Bus Terminators, ED-3T076-40,G3
- SCSI Bus Jumpers, 9824AN connector.

12.2 ED-3T076-20 CONNECTORIZED SWITCHBOARD CABLES

Table 12-1 identifies the connectorized switchboard cables. Figure 12-1 is a rear view of the Processor Cabinet, J3T060A-1, showing the location of the connectorized switchboard cables.

Table 12-1 ED-3T076-20 Connectorized Switchboard Cables

CABLE ID [a]	CABLE DESCRIPTION	QTY	FROM EQL	TO EQL
ED-3T076-20, G1	Dual Serial Channel Cable	1	CU 0, DFC 0, 028-178-106	CU 0, DMA 0, 028-075-338
ED-3T076-20, G1A	Dual Serial Channel Cable	1	CU 1, DFC 1, 053-178-106	CU 0, DMA 0, 028-075-306
ED-3T076-20, G1B	Dual Serial Channel Cable	1	CU 0, IOP 0, 019-065-506	CU 0, DMA 0, 028-075-351
ED-3T076-20, G1C	Dual Serial Channel Cable	1	CU 1, IOP 1, 045-065-506	CU 0, DMA 0, 028-075-319
ED-3T076-20, G1D	Dual Serial Channel Cable	1	CU 0, DFC 0, 028-178-119	CU 1, DMA 0, 053-075-338
ED-3T076-20, G1E	Dual Serial Channel Cable	1	CU 1, DFC 1, 053-178-119	CU 1, DMA 0, 053-075-306
ED-3T076-20, G1F	Dual Serial Channel Cable	1	CU 0, IOP 0, 019-065-706	CU 1, DMA 0, 053-075-351
ED-3T076-20, G1G	Dual Serial Channel Cable	1	CU 1, IOP 1, 045-065-706	CU 1, DMA 0, 053-075-319
ED-3T076-20, G1H	Dual Serial Channel Cable	1	IOP 2-SPU, IOP 2, 011-011-506	CU 0, DMA 0, 028-075-345
ED-3T076-20, G1J	Dual Serial Channel Cable	1	IOP 2-SPU, IOP 2, 011-011-706	CU 1, DMA 0, 053-075-345
ED-3T076-20, G1K	Dual Serial Channel Cable	1	IOP 3-SPU, IOP 3, 062-011-506	CU 0, DMA 0, 028-075-313
ED-3T076-20, G1L	Dual Serial Channel	1	IOP 3-SPU, IOP 3,	CU 1, DMA 0,

	Cable		062-011-706	053-075-313
ED-3T076-20, G1M	Dual Serial Channel Cable	1	IOP 2-SPU, DFC 2, 011-180-106	CU 0, DMA 0, 028-075-332
ED-3T076-20, G1N	Dual Serial Channel Cable	1	IOP 2-SPU, DFC 2, 011-180-119	CU 1, DMA 0, 053-075-332
ED-3T076-20, G2	Maintenance Terminal (MTTY) Control Cable	1	CU 0, PC00 (TN983 MTTYC), 019-094-345	CU 1, UN377 PSSDB, 045-186-345
ED-3T076-20, G2A	Receive-Only Printer (ROP) Control Cable	1	CU 0, PC00 (TN983 MTTYC), 019-094-132	CU 1, UN377 PSSDB, 045-186-145
ED-3T076-20, G2B	Maintenance Terminal (MTTY) Control Cable	1	CU 1, PC00 (TN983 MTTYC), 045-094-345	CU 1, UN377 PSSDB, 045-186-351
ED-3T076-20, G2C	Receive-Only Printer (ROP) Control Cable	1	CU 1, PC00 (TN983 MTTYC), 045-094-132	CU 1, UN377 PSSDB, 045-186-151
ED-3T076-20, G2D	Maintenance Terminal (MTTY) Control Cable	1	CU 1, PC00 (UN583/UN597 MTTYC), 019-094-132	CU 1, UN377 PSSDB, 045-186-345
ED-3T076-20, G2E	Receive-Only Printer (ROP) Control Cable	1	CU 0, PC00 (UN583/UN597 MTTYC), 019-094-332	CU 1, UN377 PSSDB, 045-186-145
ED-3T076-20, G2F	Maintenance Terminal (MTTY) Control Cable	1	CU 1, PC00 (UN583/UN597 MTTYC), 045-094-132	CU 1, UN377 PSSDB, 045-186-351
ED-3T076-20, G2G	Receive-Only Printer (ROP) Control Cable	1	CU 1, PC00 (UN583/UN597 MTTYC), 045-094-332	CU 1, UN377 PSSDB, 045-186-151
ED-3T076-20, G3	Emergency Action Interface (EAI) Cable	1	CU 0, PC00 (TN983/UN597 MTTYC), 019-094-153	CU 0, KLW31 CC, 019-038-500
ED-3T076-40, G3A	Emergency Action Interface (EAI) Cable	1	CU 0, PC00 (TN983 MTTYC), 019-094-149	CU 1, KLW31 CC, 045-038-500
ED-3T076-20, G3B	Emergency Action Interface (EAI) Cable	1	CU 1, PC00 (TN983 MTTYC), 045-094-149	CU 1, KLW31 CC, 045-038-300
ED-3T076-20, G3C	Emergency Action Interface (EAI) Cable	1	CU 1, PC00 (TN983 MTTYC), 045-094-153	CU 0, KLW31 CC, 019-038-300
ED-3T076-20, G4	Boundary Scan Bus Cable	1	CU 0, KLW31 CC, 019-038-506	CU 1, TN1820 IOPPS, 045-080-132
ED-3T076-20, G4A	Boundary Scan Bus Cable	1	CU 1, KLW31 CC, 045-038-506	CU 0, TN1820 IOPPS, 019-080-132
ED-3T076-20, G5	Maintenance Channel (MCH) Cable	1	CU 0, KLW31 CC, 019-038-100	CU 1, KLW31 CC, 045-038-100
ED-3T076-20, G6	Boundary Scan Bus Cable	1	CU 0, TN1820 IOPPS, 019-080-151	IOP 2-SPU, TN1820 IOPPS, 011-026-132
ED-3T076-20, G6A	Boundary Scan Bus Cable	1	CU 1, TN1820 IOPPS, 045-080-151	IOP 3-SPU, TN1820 IOPPS, 062-026-132
ED-3T076-20, G7B	Maintenance Terminal (MTTY) Cable (50 Feet)	1	CU 1, UN377 PSSDB, 045-186-332	MTTY
ED-3T076-20, G7C	Receive-Only Printer (ROP) Cable (50 Feet)	1	CU 1, UN377 PSSDB, 045-186-132	ROP
ED-3T076-20, G7D	Maintenance Terminal (MTTY) Cable (100 Feet)	1	CU 1, UN377 PSSDB, 045-186-332	MTTY
ED-3T076-20, G7E	Receive-Only Printer (ROP) Cable (100 Feet)	1	CU 1, UN377 PSSDB, 045-186-132	ROP
ED-3T076-20, G7F	Maintenance Terminal	1	CU 1, UN377 PSSDB,	MTTY

	(MTTY) Cable (250 Feet)		045-186-332	
ED-3T076-20, G7G	Receive-Only Printer (ROP) Cable (250 Feet)	1	CU 1, UN377 PSSDB, 045-186-132	ROP
ED-3T076-20, G7H	Maintenance Terminal (MTTY) Cable (50 Feet)	1	CU 1, UN377 PSSDB, 045-186-332	MTTY
ED-3T076-20, G7J	Receive-Only Printer (ROP) Cable (50 Feet)	1	CU 1, UN377 PSSDB, 045-186-132	ROP
ED-3T076-20, G7K	Maintenance Terminal (MTTY) Cable (100 Feet)	1	CU 1, UN377 PSSDB, 045-186-332	MTTY
ED-3T076-20, G7L	Receive-Only Printer (ROP) Cable (100 Feet)	1	CU 1, UN377 PSSDB, 045-186-132	ROP
ED-3T076-20, G7M	Maintenance Terminal (MTTY) Cable (250 Feet)	1	CU 1, UN377 PSSDB, 045-186-332	MTTY
ED-3T076-20, G7N	Receive-Only Printer (ROP) Cable (250 Feet)	1	CU 1, UN377 PSSDB, 045-186-132	ROP
ED-3T076-20, G8	DSCH Computer Interconnect (DCI) Cable (50 Feet)	1	DMA in CU 1 or 0	*Sun* [b] DCI Board
ED-3T076-20, G8A	DCI Cable (75 Feet)	1	DMA in CU 1 or 0	*Sun* DCI Board
ED-3T076-20, G8B	DCI Cable (100 Feet)	1	DMA in CU 1 or 0	*Sun* DCI Board
ED-3T076-20, G14	Scanner and Signal Distributor (SCSD) Cable	1	CU 0, PC02 (UN33/ UN933 SCSDC 0), 019-110-333	Bidirectional Fan Unit 0, 036-011-200
ED-3T076-20, G14A	Scanner and Signal Distributor (SCSD) Cable	1	CU 1, PC02 (UN33/ UN933 SCSDC 1), 045-110-333	Bidirectional Fan Unit 1, 036-011-300
ED-3T076-20, G15A	Scanner and Signal Distributor (SCSD) Cable	1	CU 0, PC02 (UN33/ UN933 SCSDC 0), 019-110-550	CU 1, TN1820 IOPPS, 045-080-306
ED-3T076-20, G15D	Scanner and Signal Distributor (SCSD) Cable	1	CU 1, PC02 (UN33/ UN933 SCSDC 1), 045-110-550	CU 0, TN1820 IOPPS, 019-080-306
ED-3T076-20, G17	Scanner and Signal Distributor (SCSD) Cable	1	CU 0, PC02 (UN33/ UN933 SCSDC 0), 019-110-537	CU 0, SPU04, 028-146-539
ED-3T076-20, G17A	Scanner and Signal Distributor (SCSD) Cable	1	CU 1, PC02 (UN33/ UN933 SCSDC 1), 045-110-537	CU 1, SPU05, 053-146-539
ED-3T076-20, G17B	Scanner and Signal Distributor (SCSD) Cable	1	CU 0, PC30 (UN33/ UN933 SCSDC 2), 028-130-337	IOP 2-SPU, SPU18, 011-180-539
ED-3T076-20, G17C	Scanner and Signal Distributor (SCSD) Cable	1	CU 0, PC30 (UN33/ UN933 SCSDC 2), 028-130-133	IOP3-SPU, SPU19, 062-180-539
ED-3T076-20, G17D	Scanner and Signal Distributor (SCSD) Cable	1	CU 0, PC30 (UN33/ UN933 SCSDC 2), 028-130-346	IOP 2-SPU, SPU20, 011-164-539
ED-3T076-20, G17E	Scanner and Signal Distributor (SCSD) Cable	1	CU 0, PC30 (UN33/ UN933 SCSDC 2), 028-130-137	IOP 3-SPU, SPU21, 062-164-539
ED-3T076-20, G17F	Scanner and Signal Distributor (SCSD) Cable	1	CU 0, PC30 (UN33/ UN933 SCSDC 2), 028-130-350	IOP 2-SPU, SPU22, 011-148-539
ED-3T076-20, G17G	Scanner and Signal Distributor (SCSD) Cable	1	CU 0, PC30 (UN33/ UN933 SCSDC 2), 028-130-146	IOP 3-SPU, SPU23, 062-148-539
ED-3T076-20, G17H	Scanner and Signal Distributor (SCSD) Cable	1	CU 0, PC30 (UN33/ UN933 SCSDC 2), 028-130-533	IOP 2-SPU, SPU24, 011-132-539
ED-3T076-20, G17J	Scanner and Signal Distributor (SCSD) Cable	1	CU 0, PC30 (UN33/ UN933 SCSDC 2), 028-130-150	IOP 3-SPU, SPU25, 062-132-539

ED-3T076-20, G17K	Scanner and Signal Distributor (SCSD) Cable	1	CU 0, PC30 (UN33/ UN933 SCSDC 2), 028-130-537	IOP 2-SPU, SPU26, 011-116-539
ED-3T076-20, G17L	Scanner and Signal Distributor (SCSD) Cable	1	CU 0, PC30 (UN33/ UN933 SCSDC 2), 028-130-333	IOP 3-SPU, SPU27, 062-116-539
ED-3T076-20, G18	Scanner and Signal Distributor (SCSD) Cable	1	CU 0, PC02 (UN33/ UN933 SCSDC 0), 019-110-546	IOP 2-SPU, TN1820 IOPPS, 011-026-306
ED-3T076-20, G18A	Scanner and Signal Distributor (SCSD) Cable	1	CU 1, PC02 (UN33/ UN933 SCSDC 1), 045-110-546	IOP 3-SPU, TN1820 IOPPS, 062-026-306
ED-3T076-20, G18B	Scanner and Signal Distributor (SCSD) Cable	1	CU 0, PC30 (UN33/ UN933 SCSDC 2), 028-130-546	IOP 2-SPU, TN1820 IOPPS, 011-180-539
ED-3T076-20, G30	Alarm Cable	1	Port Switch (UN377)	SCSD (UN33D/ UN933) in CU 0 or 1
ED-3T076-20, G33	Emergency Action Interface (EAI) Cable	1	CU 0, PC00 (UN583/UN597 MTTYC), 019-094-317	CU 0, KLW31 CC, 019-038-500
ED-3T076-20, G33A	Emergency Action Interface (EAI) Cable	1	CU 1, PC00 (UN583/UN597 MTTYC), 045-094-117	CU 1, KLW31 CC, 045-038-300
ED-3T076-40, G34	Emergency Action Interface (EAI) Cable	1	CU 0, PC00 (UN583/UN597 MTTYC), 019-094-120	CU 0, KLW31 CC, 045-038-500
ED-3T076-20, G34A	Emergency Action Interface (EAI) Cable	1	CU 1, PC00 (UN583/UN597 MTTYC), 045-094-320	CU 1, KLW31 CC, 019-038-300
ED-3T076-20, G50	Peripheral Control Cable (50 feet max)	1	201C or 212AR Data Set	UN582 - Provides RS232C SDL
ED-3T076-20, G51	Peripheral Control Cable (50 feet max)	1	201C Data Set	UN583/UN597 - Provides RS232C SCC SDL
ED-3T076-20, G52	Peripheral Control Cable (50 feet max)	1	202T Data Set	UN582 - Provides RS232C ADL
ED-3T076-20, G52A	Peripheral Control Cable (250 feet max)	1	202T Data Set	UN582 - Provides RS232C ADL
ED-3T076-20, G53	Peripheral Control Cable (50 feet max)	1	*Gandalf* **c** 3309 Data Set	UN582 - Provides RS232C ADL
ED-3T076-20, G53A	Peripheral Control Cable (250 feet max)	1	*Gandalf* 3309 Data Set	UN582 - Provides RS232C ADL
ED-3T076-20, G54	Peripheral Control Cable (100 feet max)	1	212AR Data Set	UN582 - Provides RS232C ADL
ED-3T076-20, G55	Peripheral Control Cable (50 feet max)	1	AT&T STU-ll Secure (Model 1900) Data Set	UN582 - Provides RS232C ADL
ED-3T076-20, G56	Peripheral Control Cable (50 feet max)	1	ROP	UN582 - Provides A Null Modem RS232C ADL
ED-3T076-20, G56A	Peripheral Control Cable (250 feet max)	1	ROP	UN582 - Provides A Null Modem RS232C ADL
ED-3T076-20, G57	Peripheral Control Cable (50 feet max)	1	VT100	UN582 - Provides A Null Modem RS232C ADL
ED-3T076-20, G57A	Peripheral Control Cable (250 feet max)	1	VT100	UN582 - Provides A Null Modem RS232C ADL
ED-3T076-20, G58	Peripheral Control Cable (50 feet max)	1	Color VT	UN582 - Provides RS232C ADL
ED-3T076-20, G58A	Peripheral Control Cable (250 feet max)	1	Color VT	UN582 - Provides RS232C ADL

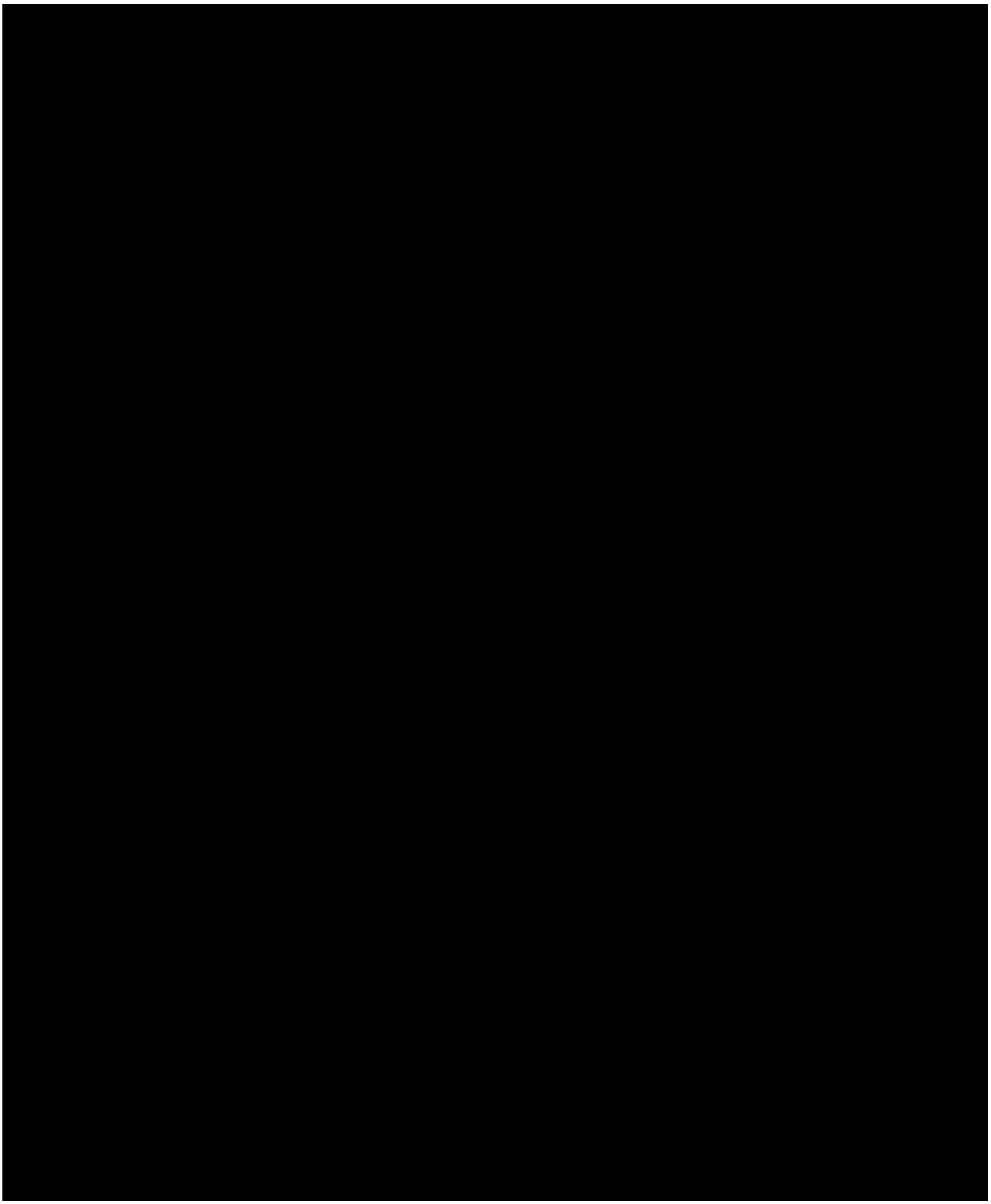
ED-3T076-20, G59	Peripheral Control Cable (50 feet max)	1	Hardware Flow Control Data Set	UN582 - Provides RS232C ADL
ED-3T076-20, G60	Peripheral Control Cable (50 feet max)	1	Hardware Flow Control Data Set	UN582 - Provides RS232C ADL
ED-3T076-20, G61	Peripheral Control Cable (50 feet max)	1	2024A, 2048A, or 2096A Data Set	UN582 - Provides RS449 DL
ED-3T076-20, G62	Peripheral Control Cable (50 feet max)	1	2556B Data Set	UN582 - Provides A V.35/V.36 DL
ED-3T076-20, G63	Peripheral Control Cable (50 feet max)	1	V.35 Data Set	UN582 - Provides A V.35 DL
ED-3T076-20, G64	Peripheral Control Cable (50 feet max)	1	V.36 Data Set	UN582 - Provides A V.36 DL

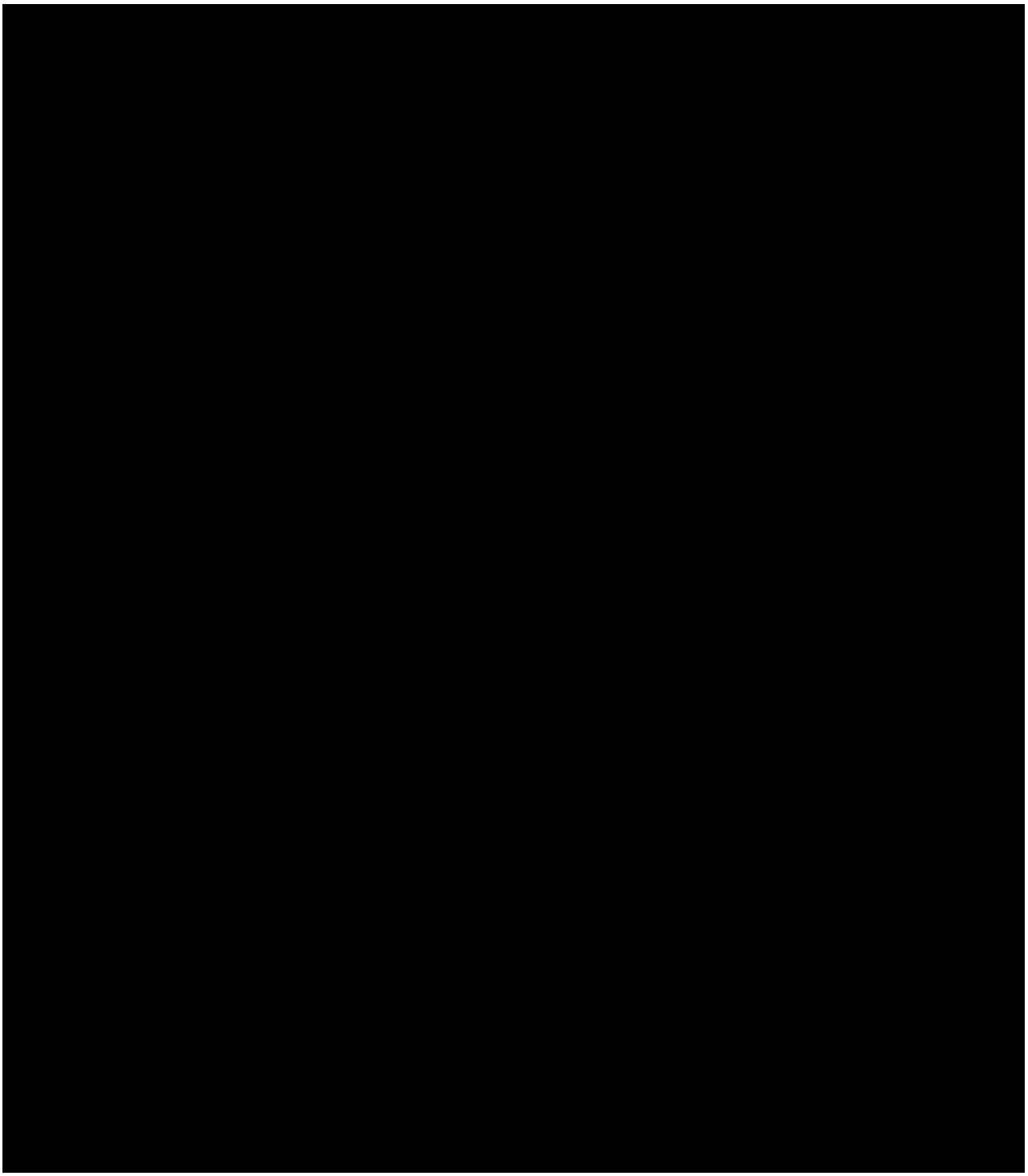
Notes:

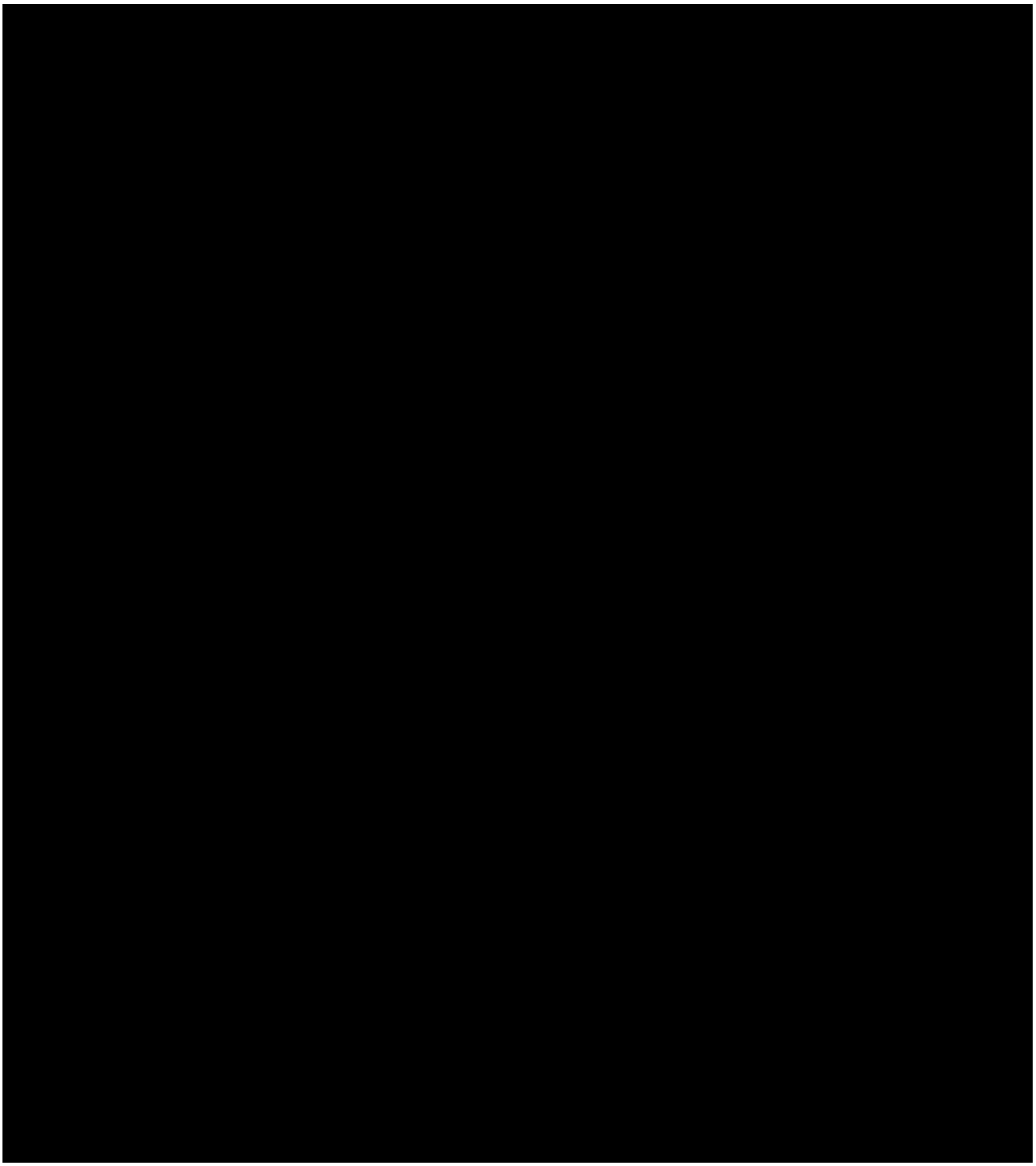
a. Cables for Peripheral Community Synchronous Data Link Control (SDLC) devices are not included.

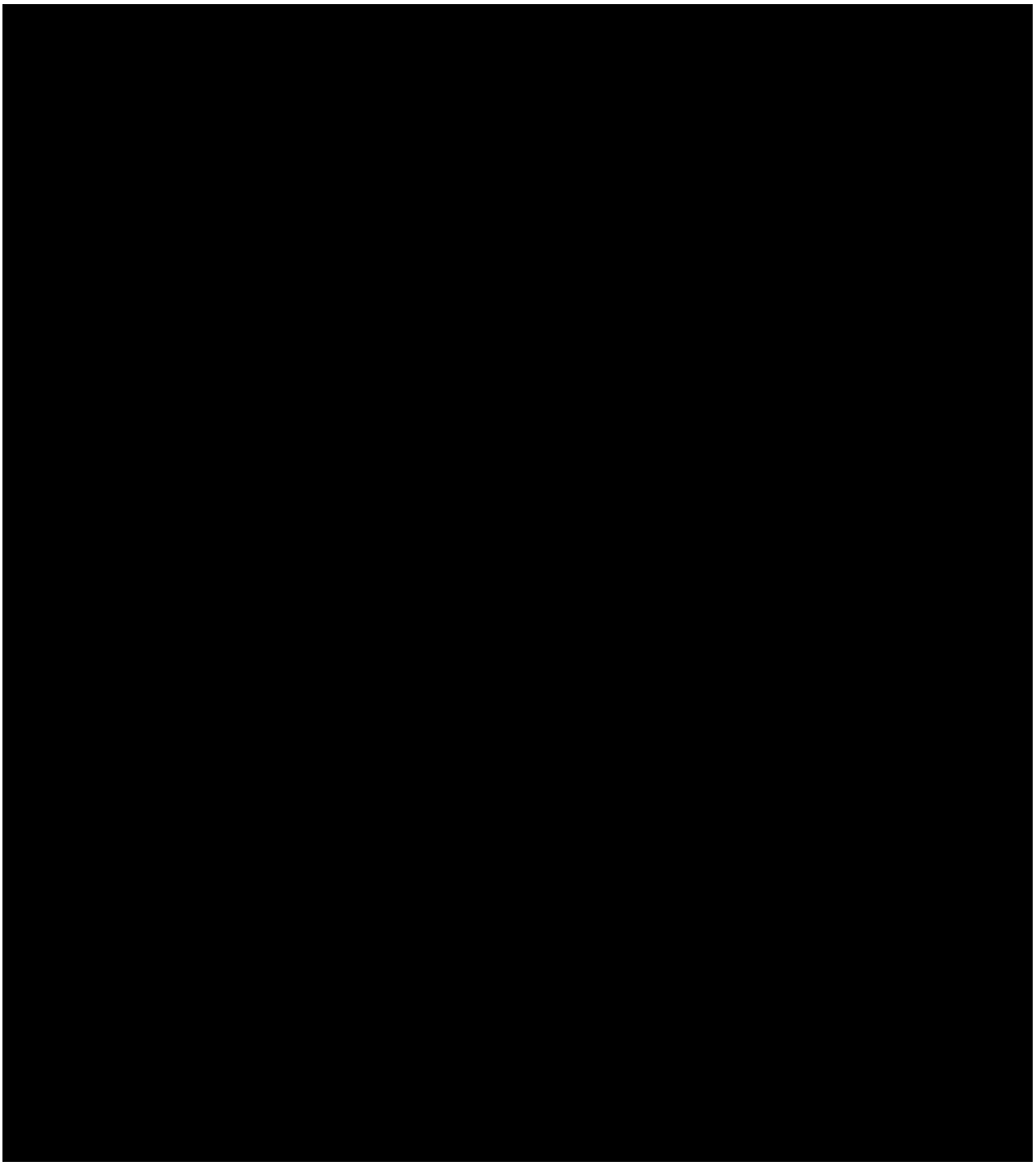
b. Sun, Sun Microsystems, and the Sun Logo are trademarks or registered trademarks of Sun Microsystems Inc. in the United States and other countries.

c. Gandalf is a registered trademark of Mitel Corporation.









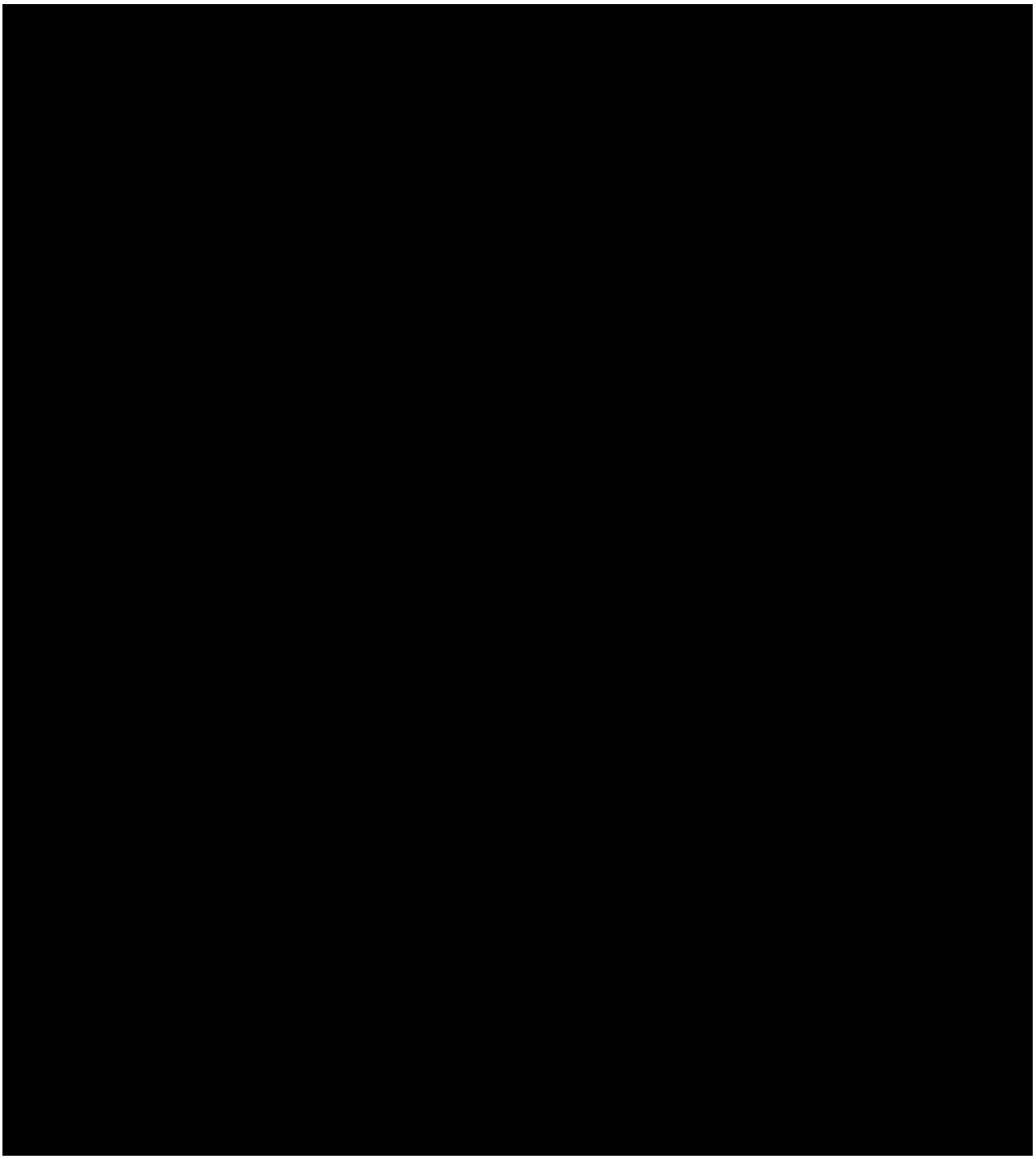


Figure 12-1 ED-3T076-20 Connectorized Switchboard Cables Location Information

12.3 ED-3T076-40 FLEX TAPE CABLES

Table 12-2 identifies the connectorized flex tape cables. Figure 12-2 is a rear view of the Processor Cabinet, J3T060A-1, showing the location of the flex tape cables. KLW32 could also refer to KLW40, KLW48, KLW64, or KLW128.

Table 12-2 ED-3T076-40 Flex Tape Cables

CABLE ID	CABLE DESCRIPTION	QTY	FROM EQL	TO EQL
ED-3T076-40, G1	Main Store Update Bus Cable	1	CU 0, KLW32 MM,	CU 1, KLW32 MM,

			019-008-100 CU 0, KLW32 MM, 019-008-132 CU 0, KLW32 MM, 019-008-300 CU 0, KLW32 MM, 028-008-100 CU 0, KLW32 MM, 028-008-132	045-008-100 CU 1, KLW32 MM, 045-008-132 CU 1, KLW32 MM, 045-008-300 CU 1, KLW32 MM, 053-008-100 CU 1, KLW32 MM, 053-007-032
ED-3T076-40, G3	Connectorized Bus Terminating Resistor Cable Connectorized Bus Terminating Resistor Cable Connectorized Bus Terminating Resistor Cable Connectorized Bus Terminating Resistor Cable Connectorized Bus Terminating Resistor Cable Connectorized Bus Terminating Resistor Cable Connectorized Bus Terminating Resistor Cable Connectorized Bus Terminating Resistor Cable Connectorized Bus Terminating Resistor Cable Connectorized Bus Terminating Resistor Cable		62-180-500 62-180-300 53-178-300 53-101-000 45-186-500 45-101-000 28-178-300 28-101-000 19-186-500 19-101-000 11-180-300 11-180-500	62-180-500 62-180-300 53-178-300 53-101-000 45-186-500 45-101-000 28-178-300 28-101-000 19-186-500 19-101-000 11-180-300 11-180-500
ED-3T076-40, G4	Processor 0, Bus 0 and IOP 2-SPU, Bus A SCSI Bus Extension Cable (SPU20 and SPU24)	1	28-101-000	11-063-000
ED-3T076-40, G4A	Processor 0, Bus 2 and IOP 2-SPU, Bus B SCSI Bus Extension Cable (SPU18, SPU22, and SPU26)	1	19-101-000	11-047-000
ED-3T076-40, G4B	Processor 1, Bus 1 and IOP 3-SPU, Bus A SCSI Bus Extension Cable (SPU21 and SPU25)	1	53-101-000	62-063-000
ED-3T076-40, G4C	Processor 1, Bus 3 and IOP 3-SPU, Bus B SCSI Bus Extension Cable (SPU19, SPU23, and SPU27)	1	45-101-000	62-047-000
ED-3T076-40, G4D	Processor 0, Bus 0 and IOP 3-SPU, Bus A SCSI Bus Extension Cable (SPU21 and SPU25)	1	28-101-000	62-063-000
ED-3T076-40, G4E	Processor 1, Bus 1 and IOP 3-SPU, Bus B SCSI Bus Extension Cable (SPU19, SPU23, and SPU27)	1	53-101-000	62-047-000
ED-3T076-40, G100	Processor 0 or 1 and 9-Track Tape Drive 0 or 1 SCSI Bus Cable	1	19-186-500 45-186-500	9-Track Tape Drive 0 or 1
ED-3T076-40, G101	Processor 0 or 1 and 9-Track Tape Drive 2 or 3 SCSI Bus Cable	1	28-186-300 53-178-300	9-Track Tape Drive 2 or 3

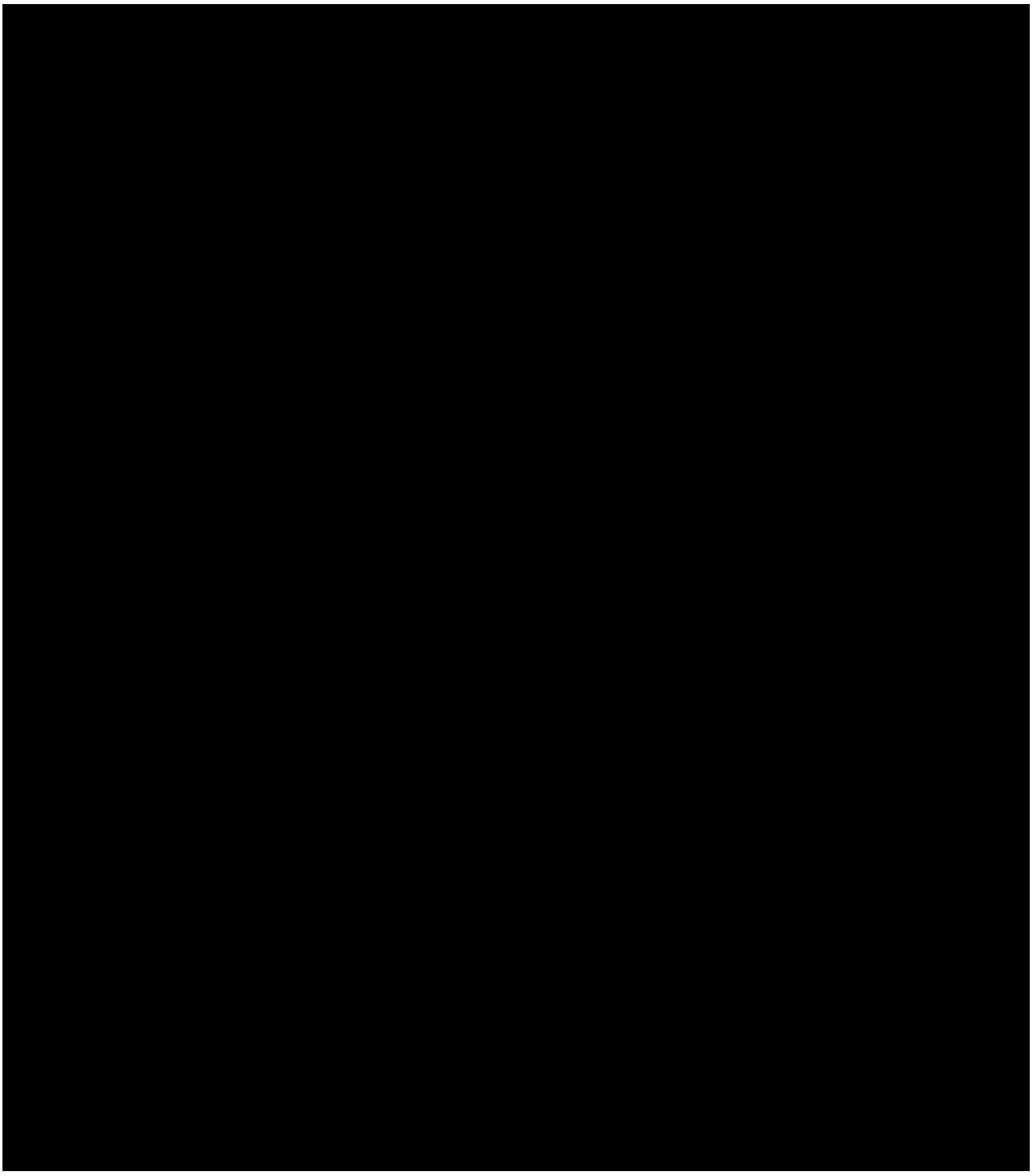


Figure 12-2 ED-3T076-40 Flex Tape Cables Location Information

12.4 ED-3T076-50 FORMED CABLES

Table 12-3 identifies the formed cable assemblies. Figures 12-3 and 12-4 are rear views of the Processor Cabinet, J3T060A-1, showing the location of the formed cable assemblies.

Table 12-3 ED-3T076-50 Formed Cables

CABLE ID	CABLE DESCRIPTION	QTY	FROM EQL	TO EQL
ED-3T076-50, G1	Processor Unit 0 Power (and Fuse Alarm) Cable	1	028-060-316	069-100-103
ED-3T076-50, G2	Processor Unit 1 Power (and Fuse Alarm) Cable	1	053-060-316	069-100-106
ED-3T076-50, G3	IOP 2-SPU Growth Unit Power Cable	1		
ED-3T076-50, G4	IOP 3-SPU Growth Unit Power Cable	1		

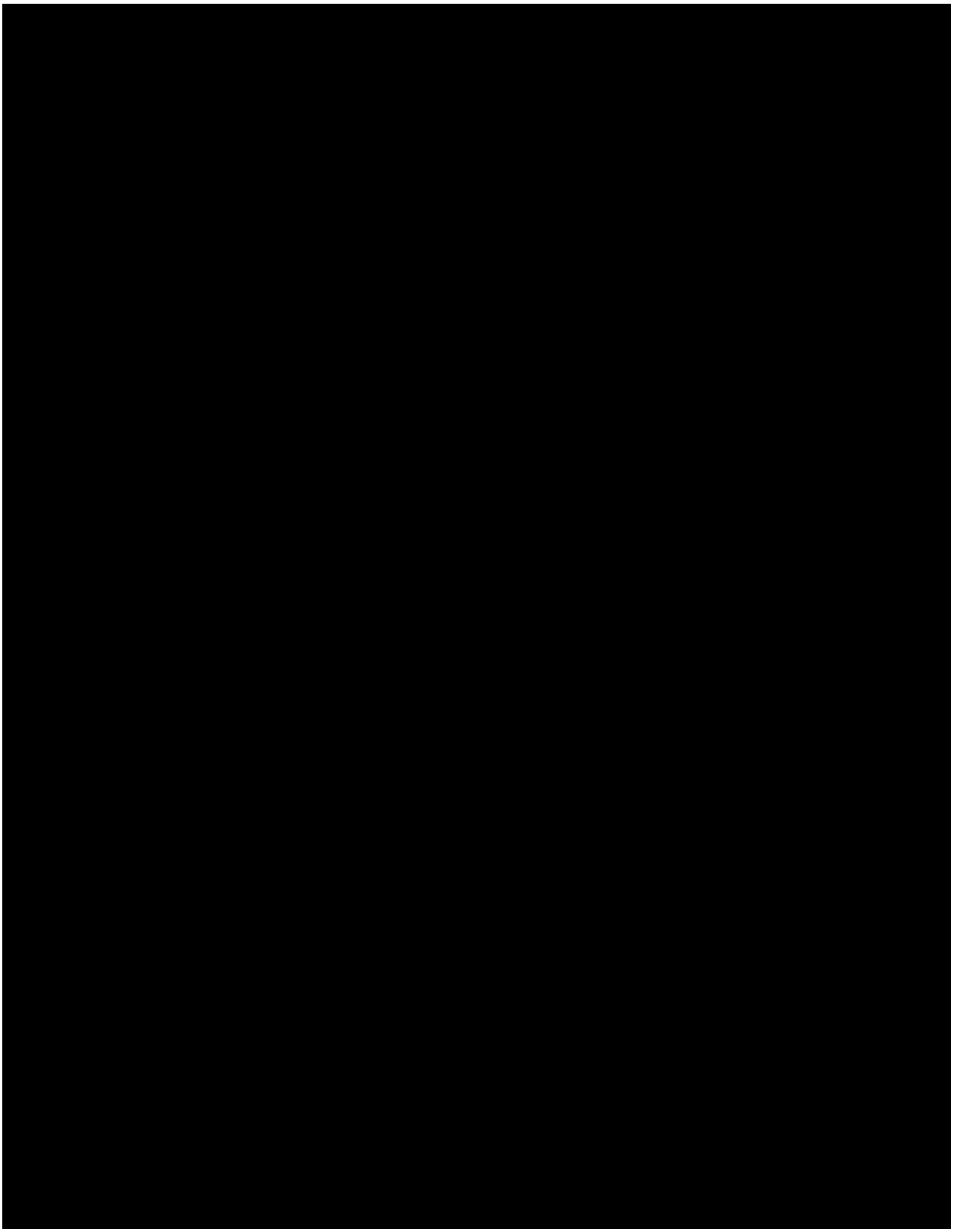


Figure 12-3 ED-3T076-50,G1,2 Formed Cable Assemblies Location Information

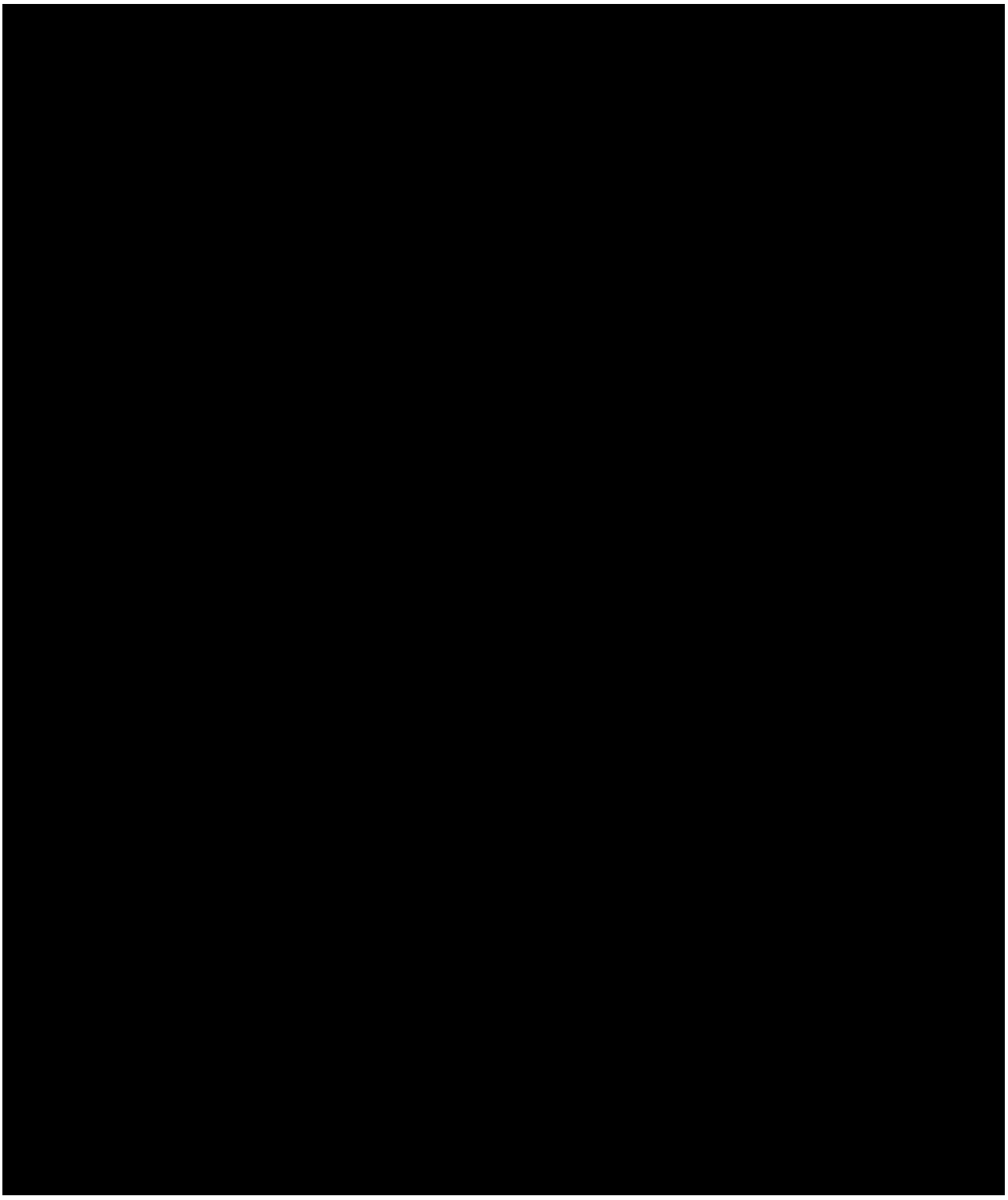


Figure 12-4 ED-3T076-50,G3,4 Formed Cable Assemblies Location Information

12.5 9824A PADDLEBOARD ASSEMBLIES

Table 12-4 identifies the paddleboard assemblies used on the Processor Unit backplane. All paddleboards contain a network of series RC terminations to ground. The resistance value is 56 ohms and the capacitance is 47 pF. This matches the line impedance of 65 ohms and assumes a series impedance of 10 ohms in the driving elements. Paddleboard assembly BTR1 also contains pull-up resistors to Vcc for the Central Control Input/Output (CCIO) data bus, CCIO addresses, and CCIO commands. The pull-up

resistance is 1000 ohms. The pull-up resistors are on the same power boundary (P5VA) as the CC and DMA 0 circuit packs.

Table 12-4 9824A Paddleboard Assemblies

NAME	EQL	NUMBER	DESCRIPTION
BTR1	13-075-732	9824AP	CCIO Bus terminations and pull-ups, DMA 0 end
BTR2	13-075-700	9824AR	MAS Data and Address terminations, DMA 0 end
BTR3	08-018-532	9824AS	CCIO Bus terminations, EX 0 end

12.6 ED-3T076-40,G3 SCSI BUS TERMINATORS

Table 12-5 identifies the Small Computer System Interface (SCSI) bus terminators. Termination resistors for the SCSI buses are mounted external to the backplane and circuit packs but not on paddleboards. A SCSI bus terminator consists of a commercial resistor assembly that plugs into a connector cabled to the backplane. There are four of these assemblies, two for each end of the two SCSI buses. Table 12-5 identifies all possible locations for the SCSI bus terminators.

Table 12-5 ED-3T076-40,G3 SCSI Bus Terminators

UNIT	EQL
IOP 3-SPU Growth Unit	62-180-500 62-180-300
Processor Unit 1	53-178-300 53-101-000 45-186-500 45-101-000
Processor Unit 0	28-178-300 28-101-000 19-186-500 19-101-000
IOP 3-SPU Growth Unit	11-180-300 11-180-500

12.7 9824AN SCSI BUS JUMPERS

Table 12-6 lists the SCSI bus jumper locations. Figure 12-2 is a rear view of the Processor Cabinet, J3T060A-1, showing the location of the 9824AN SCSI Bus Jumpers.

Table 12-6 9824AN SCSI Bus Jumper Locations

UNIT	EQL	NOTES
IOP 3-SPU Growth Unit	62-171-000 62-155-000 62-139-000 62-123-000	SPU21 SPU23 SPU25 SPU27
Processor Unit 1	53-153-000	SPU05
Processor Unit 0	28-153-000	SPU04
IOP 2-SPU Growth Unit	11-171-000 11-155-000 11-139-000 11-123-000	SPU20 SPU22 SPU24 SPU26

GLOSSARY

The following abbreviations, acronyms, and terms are used in this document.

-- GLOSSARY --

AC
Alternating Current

ACK
Acknowledge

ACO-T
Alarm Cutoff-Test

AD
Address/Data (bus)

ADCCP
Advanced Data Communications Control Procedures

ALM
Alarm

ALU
Arithmetic Logic Unit

AM
Administrative Module

AND
A logical operation that outputs a signal only if all inputs receive a signal.

ASIC
Application Specific Integrated Circuit

ASW
All Seems Well

ATB
Address Translation Buffer

BCP
Byte-Control Protocol

BGB
Bidirectional Gating Bus

BGR
Bidirectional Gating Register

BIC
Bus Interface Controller

BIST
Built-In Self Test

BMPM
Board-Mounted Power Module

BOM
Beginning of Media (associated with cartridge tape)

BOP
Beginning of Partition (associated with cartridge tape)

BOT
Beginning of Tape (associated with 9-track tape)

BPI
Bits Per Inch

BS
Boundary Scan (bus)

BSM
Boundary Scan Master

CA
Cache Address (bus)

CAC
Cache Controller

CAR
Channel Address Register

CAS
Column Address Strobe

CC
Central Control

CCIDI
CC Identification Input

CCIO
Central Control Input/Output

CCIOAD
Central Control Input/Output Address (bus)

CCIOD
Central Control Input/Output Data (bus)

CCITT
International Telegraph and Telephone Consultative Committee

CD
Cache Data (bus) or Carrier Detect

CDR
Channel Data Register

CLREAI
Clear Emergency Action Interface

CM
Communications Module

CNI
Communications Network Interface

CMOS
Complementary Metal Oxide Semiconductor

CMU
Communications Module Unit

CONV

Power Converter

CPI
Characters Per Inch

CPU
Central Processing Unit

CSU
Cache Storage Unit

CTS
Clear To Send

CU
Control Unit

CUPS
Control Unit Power Switch

DAT
Digital Audio Tape. A 3.5-inch tape drive that uses a removable 4-millimeter digital audio tape cartridge.

DATB
Internal Data Bus

DC
Direct Current

DCI
DSCH Computer Interconnect

DCE
Data Communications Equipment

DDCMP
Digital Data Communication Message Protocol

DDR
Diagnostic Data Register

DDS
Digital Data Storage (tape format)

DDSBS
Duplex Dual Serial Bus Selector

DFC
Disk File Controller

DFCA
Disk File Controller A (UN373 circuit pack)

DFCB
Disk File Controller B (TN2116 circuit pack)

DMA
Direct Memory Access

DMAC
Direct Memory Access Controller

DMU
Data Manipulation Unit

DPM
Dual-Port Memory

DRAM
Dynamic Random Access Memory

DRD
Diagnostic/Recovery Data bus

DSCH
Dual Serial Channel

DSR
Data Set Ready

DST
Destination (bus)

DSTC
Destination Clock

DTE
Data Terminal Equipment

DTIM
Disable Sanity Timer

DTR
Data Terminal Ready

DUART
Dual Universal Asynchronous Receiver/Transmitter

EAEN
Emergency Action Enabled

EAI
Emergency Action Interface

EAIMRF
EAI Maintenance Reset Function

EAIMSI
EAI Maintenance State Indication

ECD
Equipment Configuration Data

ECMA
European Computer Manufacturers Association

EDC
Error Detection and Correction

EGRASP
Enhanced Generic Access Package software; a debugger that is fully resident on the 3B21D computer.

EIA
Electronic Industrial Association

EMC
Electromagnetic Compatibility

EMI
Electromagnetic Interference

EPROM
Electrically Programmable Read-Only Memory

EQL
EQuipment Location

ER
Error Register

ESM
External Sanity Monitor

ETSI
European Telecommunication Standardization Institute

EX
Expansion (slot)

FA
Fuse Alarm

FBDP
Force Boot Device Primary

FBPAR
Force Bad Parity

FBDS
Force Boot Device Secondary

FCC
Federal Communications Commission

FFU
Fuse and Filter Unit

FG
Frame Ground

FIFO
First-In First-Out

FLZ
Find-Low-Zero

FOFL
Forced Off-Line or Force Off-Line

FONL
Forced On-Line or Force On-Line

FPS
Fan Performance Sensor

GCR
Group Coded Recording

GPI
Generic Processor Interface

GRASP
Generic Access Package software; a debugger that is fully resident on the 3B21D computer.

HA
Host Adaptor

HDLC
High Level Data Link Control

HM
Halfword Multiplexer

HSR
Hardware Status Register

I/O
Input/Output

IB
Instruction Buffer

IM
Instruction Multiplexer or Interrupt Mask (register)

INIP
Input Initialization Parameter

I/O
Input/Output

IOMI
Input/Output Microprocessor Interface

IOP
Input/Output Processor

IOPPS
Input/Output Processor Power Switch

IP
Initialization Parameter

IPS
Inches Per Second

IS
Interrupt Set (register) also known as Interrupt Source

ISO
International Standards Organization

IT
Interrupt Timer

ITU-T
International Telecommunications Union-Telecommunications Standardization Sector

JEDEC
Joint Electron Device Engineering Council

LED
Light-Emitting Diode

LOCCB
Lead-On Chip with Center Board

MAS
Main Store

MASB
Main Store Bus

MASU
Main Store Update

Mb
Mega*bit*

MB
Mega*byte*. When referring to disk devices, a megabyte is 1 million bytes. When referring to main store memory, a megabyte is 2^{20} bytes (1,048,576 bytes).

MC
MicroController

MCERT
Memory Controller with Error Regulation and Test

MCH
Maintenance Channel

MCHL
Maintenance Channel Link

MCS
MicroControl Store

MHD
Moving Head Disk

mil
One-thousandth of an inch

MIR

MicroInstruction Register

MIS
MicroInstruction Store

MJ
Major Alarm

MLB
Multi-Layer Board

MLTS
Micro Level Test Set

MM
Main Memory

MOR
Momentary rocker switch that overrides the OFF lockout for emergency power off.

MPC
Multipurpose Peripheral Controller

MPDATA
Microprocessor Data (register)

MPMADD
Microprocessor Memory Address

MRF
Maintenance Reset Function

MS
MicroStore (bus)

MSA
MicroStore Address or Main Store Address (bus)

MSD
MicroStore Data (bus)

MSEQ
MicroSequencer

MT
Magnetic Tape

MTC
Maintenance (bus)

MTTY
Maintenance Teletypewriter or Maintenance Terminal

MTTYC
MTTY Controller

MUX
Multiplexer

NARTAC
North American Regional Technical Assistance Center

NCLK
Network Clock

NEBS
Network Equipment-Building System

NET2
X.25 Network Level 2 Interface

OE
Output Enable

OOS
Out Of Service

OR
A logical operation that outputs a signal if any input receives a signal.

OS
Other Store

OST
Operating System Trap

OUTIP
Output Initialization Parameter

OUTSTAT
Output EAI Status

OUTPRM
Output PRM

P/O
Part Of (a drawing or schematic)

PA
Program Address

PB
Parameter Bus

PC
Peripheral Controller

PC00
Peripheral Community 0, Slot 0

PDC
Power Distribution Cabinet

PE
Phase Encoded

PGC
Peripheral Growth Cabinet

PIC
Peripheral Interface Controller

PIO
Programmed Input/Output

PLCC
Plastic-Leaded Chip Carrier

POCS
Programmable Over-Current Shutdown

PONL
Processor On-Line

PPR
Pulse Point Register

PQFP
Plastic Quad Flat Pack

PRM
Processor Recovery Message

PROM
Programmable Read-Only Memory

PSSDB
Port Switch and Scanner-Distributor Buffer

PSW
Processor Status Word (register)

PTSW
Port Switch

PWB
Printed Wiring Board

RAM
Random Access Memory

RAS
Row Address Strobe

RC
Resistance/Capacitance

RC/V
Recent Change and Verify

RDY
Ready

REQ
Request

RMSA
RAM MicroStore Address (bus)

ROM
Read-Only Memory

ROP
Receive-Only Printer

ROS/RST
Request-Out-of-Service/Restore two-position rocker switch. Sends a request via scan points to remove the associated unit from service or to restore the associated unit to service.

RQIP
ReQuest-In-Progress indicator (green). Lights via signal distributor point to indicate that either an ROS or RST request has been recognized by the system. When the system denies a request, the RQIP flashes for a few seconds. The RQIP indicator also lights when the ACO-T switch is pressed.

RTAC
See NARTAC.

RTC
Real-Time Clock

RTR
Real-Time Reliable

RTS
Request To Send

RXD
Receive Data

SAI
Store Address Interface

SAR
Store Address Register

SAT
Store Address Translator

SAURs
Store Address Update Registers

SC
Scan

SCC
Switching Control Center

SCR
Store Control Register

SCSD
Scanner and Signal Distributor

SCSDC
Scanner and Signal Distributor Controller 0 (SCSDC 0) is a UN33 or UN933 circuit pack equipped in IOP 0, PC02. SCSDC 1 is a UN33 or UN933 circuit pack equipped in IOP 1, PC02.

SCSI
Small Computer System Interface

SCSI ID
The bit representation of the SCSI address referring to one of the signal lines DB(7-0).

SCSI initiator
An SCSI device that requests an operation to be performed by another SCSI device.

SCSI target
An SCSI device that performs an operation requested by an initiator.

SD
Signal Distributor or Schematic Drawing

SDI
Store Data Interface

SDLC
Synchronous Data Link Control

SDR
Store Data Register

SDRP
Store Data Register Pipeline

SEQ
Sequencer

SG
Signal Ground or System Generation

SI
Store Interface

SIMM
Single In-line Memory Module

SIR
Store Instruction Register

SLFID
The Self-Identification, Self-ID, or SELF-ID circuit provides the means for a Central Control (CC) to interrogate the Main Memory circuit pack for identification information (version, issue, etc.). The circuit operates independently from the other circuit packs functions.

SMAINT
Store Maintenance Access

SN-2000
Service Net-2000

SPU
SCSI Peripheral Unit

SQUAD
Quad Word Transfer

SRAM
Static Random Access Memory

SRC
Source (bus)

SREGs
Special Registers

SRMW
Read-Modify-Write

SRPAL
Special Register Programmable Array Logic

SSEQ
Store Sequencer

SSR
System Status Register

ST
Sanity Timer

STP
Signal Transfer Point

TAP
Test Access Port

TCK
Boundary Scan Clock

TDI
Test Data Input

TDO
Test Data Output

TMS
Test Mode Selection

TR
Timer Register

TRST
Test Reset

TXD
Transmit Data

UC
Utility Circuit (UN379 circuit pack)

UID
Utility IDentification

UV
Ultraviolet (light)

WE
Write Enable

WMS
Writable MicroStore

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