

INTERLEAVING ANALOG-TO-DIGITAL CONVERTERS

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It is tempting when pushing the limits of analog-to-digital conversion to consider interleaving two or more converters to increase the sample rate (Figure 1). However, such designs must take into consideration several possible sources of error.

The first consideration is the bandwidth of the converters. For example, if the bandwidth of the converters is just over half their sampling rate, then it would not do much good to interleave them. Fortunately, the bandwidth of most converters which currently "push the envelope" is often many times higher than their sample rate since these converters are often used in undersampling situations.

The next consideration is possible offset and gain errors between the converters. Figure 2 shows two interleaved converters digitizing a sine wave. Converter A has an offset problem and converter B a gain problem. The digitized codes represent not only the original sine wave but also an error signal. In the discrete digital domain, the error signal is seen to contain two sine frequencies—a frequency of half

the sample rate (due to the offset error) and the other with a frequency of half the sample rate minus the frequency of the original input signal (due to the gain error).

The last consideration covered is the difference in INL (integral non-linearity) between the converters. INL represents the number of LSBs the output of a converter is from the expected output for a given input voltage. For example, if a converter would ideally put out a code of N for an input voltage M but actually puts out a code N+2, then the INL at that point is two.

It is not unusual for a converter to have an INL of one or two LSBs over a good part of its input voltage range. For interleaving converters, the output codes could differ by as much as two times the maximum INL (say two to four codes) for the same input voltage. This could cause errors in the output codes which resemble the gain and offset problems discussed earlier, and may drastically reduce the number of effective bits of the digitizing system.

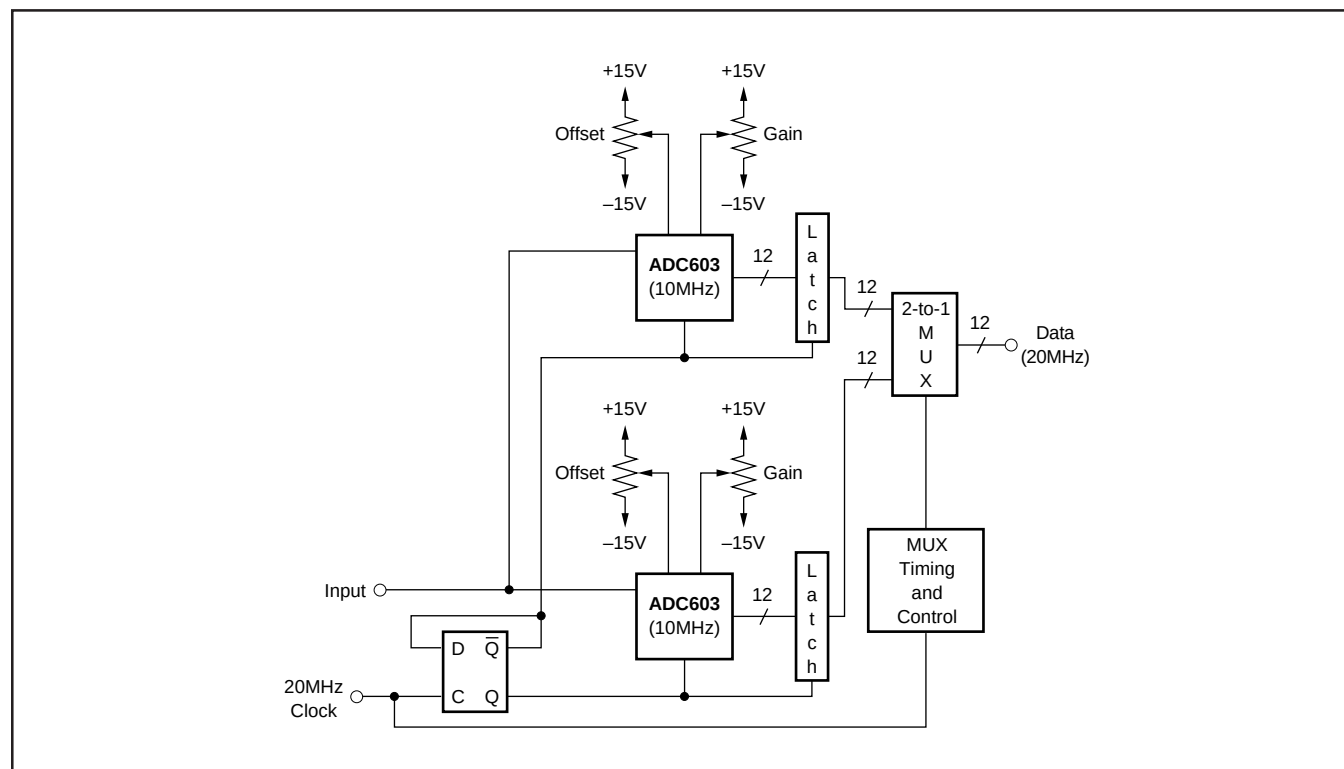


FIGURE 1. Two Interleaved Analog-to-Digital Converters.

With careful design, many of these problems can be reduced. Select ADCs with a wide enough bandwidth. Find ones that have offset and gain adjust circuitry built in or add this externally. ADCs which need external references may work well because the same reference can be provided to all the converters (but be careful of board layout). Unfortunately in this case, the trend has been to include internal references.

Reducing the errors even further is also possible, but quickly becomes increasingly complicated and costly. Correcting INL problems will almost certainly involve some form of

post digital signal processing. Correcting in the time domain will involve lengthy calibration of the converters and storing correction tables. Correcting in the frequency domain will involve computationally intensive mathematical algorithms.

On the practical side, an interleaving digitizing system will suffer some performance penalty. The amount of degradation depends on how well the converters are matched and/or how much digital signal processing the designer is willing to do. Contact Burr-Brown Applications Engineering for more information on this subject.

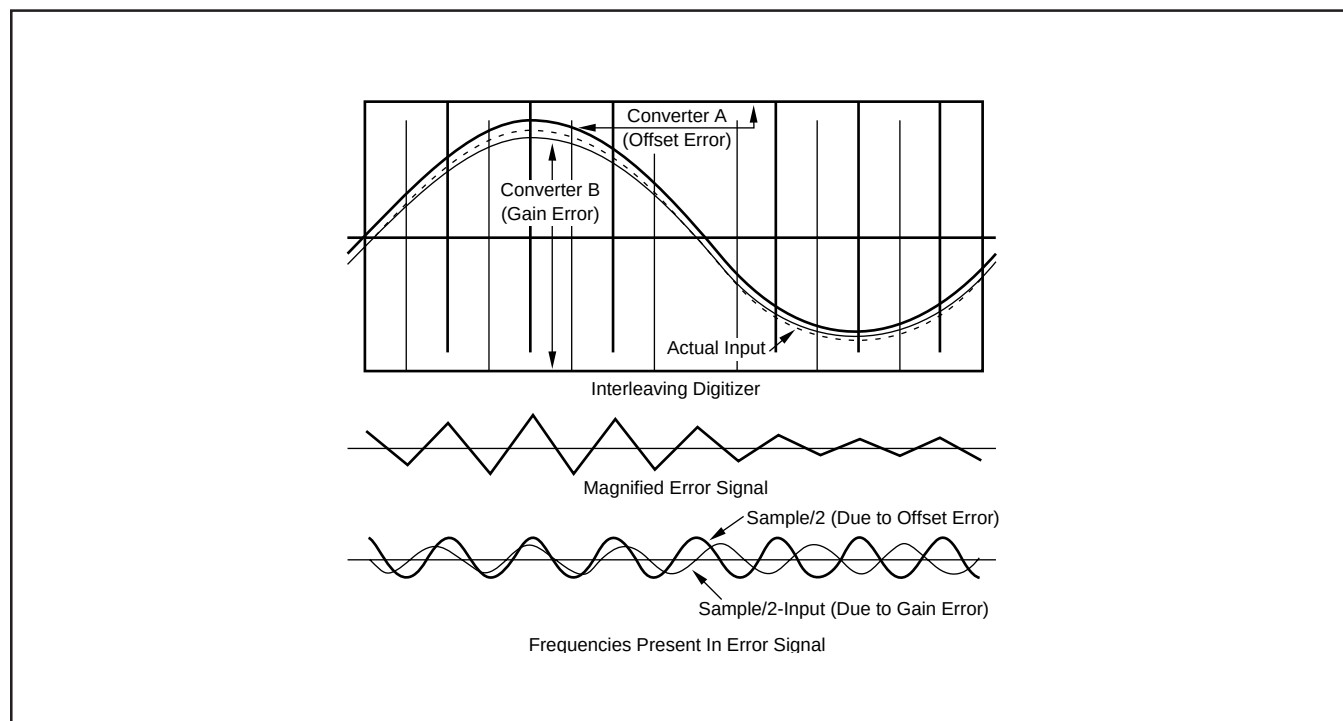


FIGURE 2. Digitized Signal of Two Interleaved Converters.