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A "GETTING STARTED" GUIDE FOR THE ΔΣ CONVERTERS: ADS1210, ADS1211, ADS1212, ADS1213, ADS1214, AND ADS1215

By Bonnie C. Baker

With increased functionality sometimes comes increased complexity. This can happen particularly when bridging the analog to the digital world. The ΔΣ Analog-to-Digital converter challenges the notion of using analog signal conditioning systems on the front end of the independent converters with an alternative. A delta-sigma converter now has the capability of replacing these discrete analog/digital systems with a complete solution in one chip.

If you are using a ΔΣ A/D converter in your circuit for the first time, the supportive documents can be somewhat overwhelming. The device itself is capable of numerous configurations accompanied with a set of trade-offs that can present a difficult first time review. The most comprehensive document you should refer to is the ΔΣ product's respective product data sheet. All of the major functions of the ΔΣ A/D converter are discussed in detail in these manuals. This application note has been written at the request of many first time users who have a problem with connecting the converter in a basic circuit and establishing communication. Not all of the problems that could come up are in this note, however the most frequent problems are discussed with viable solutions.

SELECTING THE RIGHT CONVERTER FOR THE APPLICATION

Prior to putting a chip in your circuit, the right converter should be selected for the application. The six products, ADS1210, ADS1211, ADS1212, ADS1213, ADS1214 and ADS1215 functionality are organized in an easy to remember fashion. For instance, the converters come in pairs where one of the two has a single differential input and the other has a four channel, multiplexed differential input front end. In the case of the single differential input ADS1210, the multiplexed quad differential input version is the ADS1211. In an effort to simplify this discussion, the ADS1210 and ADS1211 will be called the ADS1210/11. The numbering system follows where the ADS1212 and ADS1213 (ADS1212/13) have a similar relationship as well as the ADS1214 and ADS1215 (ADS1214/15). All of these input configuration relationships are shown in Table I.

The ADS1210/11 pair is the higher speed, more accurate version as compared to the ADS1212/13. All four of these devices have voltage references that can be used to bias external circuits. The third pair, ADS1214/15 are similar to

	# BITS NMC(1)	# DIFFERENTIAL INPUT CHANNELS	INPUT VOLTAGE RANGE	ON CHIP REFERENCE	MINIMUM PROGRAMMABLE DATA RATE	MAXIMUM PROGRAMMABLE DATA RATE	COMMENTS
ADS1210	24	1	0V - 5V or 10Vp-p	2.5V and 3.3V	2.4Hz	15,625Hz	Capable of Higher speeds, up to 20 bits at 1000Hz
ADS1211	24	4	0V - 5V or 10Vp-p	2.5V and 3.3V	2.4Hz	15,625Hz	Capable of Higher speeds, up to 20 bits at 1000Hz
ADS1212	20	1	0V - 5V or 10Vp-p	2.5V and 3.3V	0.96Hz	6,250Hz	Low Power Version of ADS1210
ADS1213	20	4	0V - 5V or 10Vp-p	2.5V and 3.3V	0.96Hz	6,250Hz	Low Power Version of ADS1211
ADS1214	20	1	0V - 320mV or 640mVp-p	Two 200µA Sources	0.96Hz	6,250Hz	Input Range Appropriate for Direct Connection to Sensors
ADS1215	20	4	0V - 320mV or 640mVp-p	Two 200µA Sources	0.96Hz	6,250Hz	Input Range Appropriate for Direct Connection to Sensors

NOTE: (1) NMC = No Missing Codes.

TABLE I. The ADS1210, ADS1211, ADS1212, ADS1213, ADS1214, and ADS1215 are all ΔΣ analog-to-digital converters. The input stages of these devices vary in voltage range and number of differential channels. On the other hand, the digital portion of these circuits have the same fundamental operation and architecture.

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the ADS1212/13 in every way except for the input voltage ranges and the biasing circuit. The input range of the ADS1214/15 is 0 to 320mV and the bias circuit has two current sources instead of two voltage sources. Refer to Table I for more detail.

POSSIBLE DIGITAL INTERFACES

There are two classes of interface that you will encounter when designing these devices into your circuit; the analog front end and the digital communication links. Although both types offer their own set of application considerations, this application note will spend more time on the digital communication issues. For more information about the analog interface, refer to the Burr-Brown Application Bulletins AB-106, AB-107, and AB-115.

The digital interface for all six of the converters mentioned in this application note are fundamentally the same. They differ only in terms of the frequency range of the external clock (X_{IN}) and the mathematical constants in the clocking network. Consequently, all six converters can be designed into the same hardware configurations.

These converters can interface with a DSP or processor chip with a two-wire up to a seven-wire connection. Each additional connection from the A/D converter to the processor adds more flexibility in the communication link. For instance, the two-wire interface can be used between the main processor and the converter. It may appear that the simplest of all digital connections is the two-wire, but in fact it is difficult to implement. This particular interface has limited visibility between the two devices. In this configuration, the A/D converter should be configured in the master mode (MODE = HIGH) and the main processor would trigger from the SCLK. The slave mode is even more cumbersome in that the main processor would have to read and write "blindly". This approach is not recommended, but is

DIGITAL INTERFACE	$\overline{DRDY}$ (Function)	SDIO (Function)	SCLK (Function)	SDOUT (Function)	$\overline{CS}$ (Function)	MODE (Function)	DSYNC (Function)	COMMENTS
2-wire	Open	DSP (I/O)	DSP (O)	Open	GND	$+V_{DD}$	$+V_{DD}$	Master mode, SDIO is used for input and output serial data communication. Processor must use SCLK as the data framing clock as well as the "notification" signal as to when communication can occur.
2-wire	Open	DSP (I/O)	DSP (I)	Open	GND	GND	$+V_{DD}$	Slave mode, SDIO is used for input and output serial data communication. Processor must communicate at least twice per data rate time to insure communication between the A/D and DSP occurs.
3-wire	DSP (O)	DSP (I/O)	DSP (I)	Open	GND	GND	$+V_{DD}$	Slave Mode, SDIO is used for the input and output serial data communication.
3-wire	Open	DSP (I)	DSP (O)	DSP (O)	GND	$+V_{DD}$	$+V_{DD}$	Master mode, Communication is triggered from SCLK. SDIO is used for the input and SDOUT for output serial data communication.
4-wire	DSP (O)	DSP (I)	DSP (I)	DSP (O)	GND	GND	$+V_{DD}$	Slave mode, serial data input and serial data output are run on separate pins between the ADC and DSP. $\overline{DRDY}$ is used to notify the DSP. SCLK must be supplied by DSP or external clock.
4-wire	DSP (O)	DSP (I)	DSP (O)	DSP (O)	GND	GND	$+V_{DD}$	Slave mode, serial data input and serial data output are run on separate pins between the ADC and DSP. $\overline{DRDY}$ is used to notify the DSP. SCLK must be supplied by DSP or external clock.
7-wire	DSP (O)	DSP (I/O)	DSP (I/O)	DSP (O)	DSP (I)	DSP (I)	DSP (I)	Software configured Master or Slave mode, most versatile configuration offering the most options for digital communication.
Function	O	I/O	I/O	O	I	I	I	O = Output, I = Input
Comments	Falling edge indicates that the converter is ready for communication.	Serial Data I/O port. Start of communication is triggered by SCLK.	Data framing clock. SCLK is an output in the master mode and input in the slave mode.	Serial Data output used in conjunction with SDIO as an Input for complete communication.	Chip Select, Used when there are multiple serial peripherals on SDIO and/or when the "Continuous Read Mode" is desired.	Configures the A/D converter in the master mode or slave mode.	Allows for synchronizing the conversion of multiple converters.	

TABLE II. Suggested connections versus available digital functions of the ΔΣ A/D converters. DSP indicates that the A/D pin is connected to an I/O port of the processor, GND indicates that the pin is connected to digital ground, $+V_{DD}$ indicates that the pin is connected to digital plus supply, Open indicates no connection.

possible. In contrast, the seven-wire interface offers the software programmer access to all of the A/D converter functions that are available. In terms of programming, the 4-wire connection is the most straight forward and will be explored later in this application note. The number of digital connections in the interface versus the possible features is summarized in Table II. Refer to the product data sheets for details about the actual circuit diagrams and timing requirements for these digital interface options.

Most commonly, the synchronization between the A/D converter and the processor is done through $\overline{\text{DRDY}}$ and SCLK. The $\overline{\text{DRDY}}$ flag notifies the processor that the A/D converter is ready to communicate. SCLK provides the framing clock for the serial data, whether the A/D converter is receiving an input or sending an output data stream. In the master mode, SCLK is an output and in the slave mode the processor must provide SCLK. The converter's serial communication is done through SDIO or SDIO and SDOUT. SDIO can operate as an input and output pin where instructions are sent to the converter as well as conversion results sent to the processor. If the A/D converter's SDOUT is used, SDIO serves exclusively as an input pin and SDOUT serves as an output.

POWER-ON SEQUENCE AND TROUBLESHOOTING SUGGESTIONS

Once the appropriate device is chosen along with the desired communication link, the next step is to build the circuit, power up the converter, and then establish communication. In this example, a four-wire connection between the DSP chip and the A/D $\Delta\Sigma$ converter is considered. The converter is configured in the slave mode. This recommended circuit is shown in Figure 1.

Once this circuit is built, the power should be applied and a preliminary check made. In this preliminary check, the A/D converter is examined to make sure all is well before communication is attempted between the DSP chip and the converter. The most common start-up problems are summarized in Table III.

VERIFICATION OF COMMUNICATION

The first key indicators that something is wrong with $\Delta\Sigma$ converter are discussed in the power-on section above. Before proceeding further, the $\overline{\text{DRDY}}$ output must be running at the frequency specified in Table III. Once the converter demonstrates that the power-on sequence was successful, the DSP should run a simple communication test with the converter. Per the flow diagram in Figure 3 and the timing diagram in Figure 2, the DSP should wait for $\overline{\text{DRDY}}$ to go low. After five X_{IN} cycles, the DSP should send a 8-bit code (synchronized with SCLK), instructing the converter to receive one 8-bit instruction which will change the data rate of the converter. The DSP should then send the second 8-bit instruction (following the "Write Data" flow) that should change the output frequency of $\overline{\text{DRDY}}$. After these 16-bits of instruction and the last SCLK, $\overline{\text{DRDY}}$ should return to high. This simple exchange will verify that communication has been established. If this first attempt at communication fails, refer to Table IV for troubleshooting guide. AB-112 gives an example of a 80 x 51 type processor interface code.

SYMPTON	CAUSE	CORRECTIVE ACTION
Supply Current exceeds specified currents	Digital power supply has exceeded the analog supply voltage by 0.3V at some time during the power up process.	• Insure that the digital supply is never more than 0.3V above the analog supply. • Voltage should not be applied to the inputs of the A/D converter, such as SDIO, A_{IN}, or REF_{IN}, before the analog supply comes up. If these pins have voltage present before the analog supply power comes up, current limiting resistors should be used.
$\overline{\text{DRDY}}$ has no output frequency response— for the ADS1210/11 $\overline{\text{DRDY}} = 850 (X_{IN}/10^7)$ Hz for the ADS1212/13 $\overline{\text{DRDY}} = 850 (X_{IN}/2.5 \times 10^6)$ Hz for the ADS1214/15 $\overline{\text{DRDY}} = 850 (X_{IN}/2.5 \times 10^6)$ Hz	Internal state machine of converter is not operating correctly.	• Cycle supplies. Make sure during this process that the power stays down between the cycles at least 300ms. • Insure that the rise time of the power supply is less than 100ms. • Disable X_{IN} clock to the converter during power up. The power to the converter must stabilize at least 25ms before X_{IN} is applied to the converter. • Allow X_{IN} to cycle at least 59000 times before $\overline{\text{DRDY}}$ is expected. • Verify that $\overline{\text{DSYNC}}$ is HIGH and $\overline{\text{CS}}$ is low. • If in slave mode, reset the converter state machine through SCLK. Timing diagram for the reset function is given in each respective product data sheet (Figure 27. Resetting the A/D Converter).
The reference outputs are not outputting nominal values REF_{OUT} = 2.5V (for the ADS1210, ADS1211, ADS1212 and ADS1213) or I_{SOURCE} = 200µA (for the ADS1214 and ADS1215)	Digital power supply has exceeded the analog supply voltage by 0.3V at some time during the power up process.	• Insure that the digital supply is never more than 0.3V above the analog supply. • Voltage should not be applied to the inputs of the A/D converter, such as SDIO, A_{IN}, or REF_{IN}, before the analog supply comes up. If these pins have voltage present before the analog supply power comes up, current limiting resistors should be used.

TABLE III. Power-on troubleshooting guide for the $\Delta\Sigma$ A/D converters from Burr-Brown.

SYMPTON	CAUSE	CORRECTIVE ACTION
Supply Current exceeds specified currents	Digital power supply has exceeded the analog supply voltage by 0.3V at some time during the power up process.	See Table III.
$\overline{DRDY}$ has no output frequency response— for the ADS1210/11 $\overline{DRDY}$ = 850 ($X_{IN}/10^7$) Hz for the ADS1212/13 $\overline{DRDY}$ = 850 ($X_{IN}/2.5 \times 10^6$) Hz for the ADS1214/15 $\overline{DRDY}$ = 850 ($X_{IN}/2.5 \times 10^6$) Hz	Internal state machine of converter is not operating correctly.	See Table III.
$\overline{DRDY}$ goes high before communication to the converter is complete.	The processor and A/D converter are not synchronized.	• Terminate SCLK to the digital GND through a 10kΩ resistor. • Verify that the timing between $\overline{DRDY}$, SCLK, SDIO and SDOUT are correct per respective product data sheet. • Allow X_{IN} to cycle at least 59000 times after power-on before $\overline{DRDY}$ is expected.
With completion of communication $\overline{DRDY}$ does not change frequency or changes to the wrong frequency.	The processor and A/D converter are not synchronized.	• Terminate SCLK to the digital GND through a 10kΩ resistor. • Verify that the timing between $\overline{DRDY}$, SCLK, SDIO and SDOUT are correct per respective product data sheet. • Allow X_{IN} to cycle at least 59000 times after power-on before $\overline{DRDY}$ is expected. • Did you send MSB first?

TABLE IV. Communication troubleshooting guide for the ΔΣ A/D converters from Burr-Brown.

FURTHER CONFIDENCE BUILDING TESTS

As a last test the converter should convert an analog input voltage and output a 24-bit serial stream to the processor. Another appropriate test would be to program the converter and write back the code that was originally sent. These algorithms are listed below. Refer to Table VII, IX and X in the product data sheets more for details about the meaning of the HEX codes presented here. All of these tests assume that the ΔΣ converter starts in its default mode (specified in the respective data sheet, Table X.). If the device is not in it's default setting, cycling the supplies or reset the converter through SDIO (per Figure 27 of the respective data sheet) will easily solve the problem.

Convert an Analog Input Voltage

- **Change the data output pin on the A/D converter from SDIO to SDOUT—**Per Figure 3, change the first HEX code to 84h and the second HEX code to 42h. The first HEX code will tell the converter to expect instruction. The second HEX code will change the output interface from SDIO to SDOUT.
- **Read back conversion data—**Apply a voltage to channel one of the differential input of the A/D converter. Per Figure 2, change the first HEX code to C0h. Then take the "Read Data" route in the flow chart and read back 3 sets of 8-bit data totaling 24 bits. Verify output code with input voltage on channel one of the A/D converter.

Read Back the Command Register Code from the Converter

- **Change the data output pin on the A/D converter from SDIO to SDOUT—**Per Figure 3, change the first HEX code to 84h and the second HEX code to 42h. The first HEX code will tell the converter to expect instruction. The second HEX code will change the output interface from SDIO to SDOUT.
- Sending and reading code from the ΔΣ converter is a two step process. In both cases, $\overline{DRDY}$ is used to indicate the beginning of the step. In the first step, the converter is told that a code or command is coming and then it is sent the converter. In the second step the converter is told that a code or command will be read and then the code is read back. For this reason, the instructions are grouped in sets of four.

See Table VII for details on this command sequence. Send all or a few of sequences of commands in Table V, VI and VII to your satisfaction.

STEP	SEND TO THE CONVERTER	READ	PURPOSE	EXTERNAL RESULTS
A.1	07h (at least $6X_{IN}$ after DRDY falling edge)		To inform the converter that you will be writing to CMR, byte 0, to change the decimation ratio.	None
A.2	C3h		To change the decimation ratio	for the ADS1210/11 DRDY = 100 ($X_{IN}/10^7$) Hz for the ADS1212/13 DRDY = 100 ($X_{IN}/2.5 \times 10^6$) Hz for the ADS1214/15 DRDY = 100 ($X_{IN}/2.5 \times 10^6$) Hz
A.3	87h (at least $6X_{IN}$ after DRDY falling edge)		To inform the converter that you will be reading from CMR, byte 0, which changed the decimation ratio.	None
A.4		C3h	To verify that C3h was actually programmed into the converter in steps A.1. and A.2 above.	µP receives the code C3h into one of its registers. This data will appear on the SDIO pin of the converter.

TABLE V. A.1 and A.2 Show the Instruction Set Needed to Change the Decimation Ratio, Which Changes the Data Rate of the Converter. A.3 and A.4 are used to read back the command register, byte 0.

STEP	SEND TO THE CONVERTER	READ	PURPOSE	EXTERNAL RESULTS
B.1	06h (at least $6X_{IN}$ after DRDY falling edge)		To inform the converter that you will be writing to CMR, byte 1, to change the Turbo Mode.	None
B.2	80h		To change the Turbo Mode to 16, keeping the PGA equal to 1 and the Channel input for the ADS1211, ADS1213 and ADS1215 set to CH 1.	for the ADS1210/11 DRDY = 13600 ($X_{IN}/10^7$) Hz for the ADS1212/13 DRDY = 13600 ($X_{IN}/2.5 \times 10^6$) Hz for the ADS1214/15 DRDY = 13600 ($X_{IN}/2.5 \times 10^6$) Hz
B.3	80h (at least $6X_{IN}$ after DRDY falling edge)		To inform the converter that you will be reading the CMR, byte 1, which changed the Turbo Mode to 16	None
B.4		80h	To verify that 80h was actually programmed into the converter in steps B.1. and B.2. above.	µP receives the code 80h into one of its registers. This data will appear on the SDIO pin of the converter.

TABLE VI. This Sequence of Instructions Changes the Turbo Mode to 16 (B.1 and B.2) and Then Reads Back the Code That was Sent to the Converter (B.3 and B.4).

STEP	SEND TO THE CONVERTER	READ	PURPOSE	EXTERNAL RESULTS
C.1	05h (at least $6X_{IN}$ after DRDY falling edge)		To inform the converter that you will be writing to all three bytes of the CMR.	None
C.2	50h 04h 17h		The first byte transmitted: Change mode from bipolar to unipolar input The second byte transmitted: Change PGA from G = 1 to G = 2 The third byte transmitted: No changes to default setting of the converter are made.	None
C.3	85h (at least $6X_{IN}$ after DRDY falling edge)		To inform the converter that you will be reading from CMR, byte 2, 1 and 0	None
C.4		50h 04h 17h	To verify that 50h, 04h and 17h were actually programmed into the converter in steps C.1. and C.2. above	µP receives three codes 50h, 04h, and 17h into its registers. This data will appear on the SDIO pin of the converter.

TABLE VII. This Sequence Changes Several Things in the Converter in Steps C.1 and C.2. Steps C.3 and C.4 Read back the commands that were sent to the A/D converter.

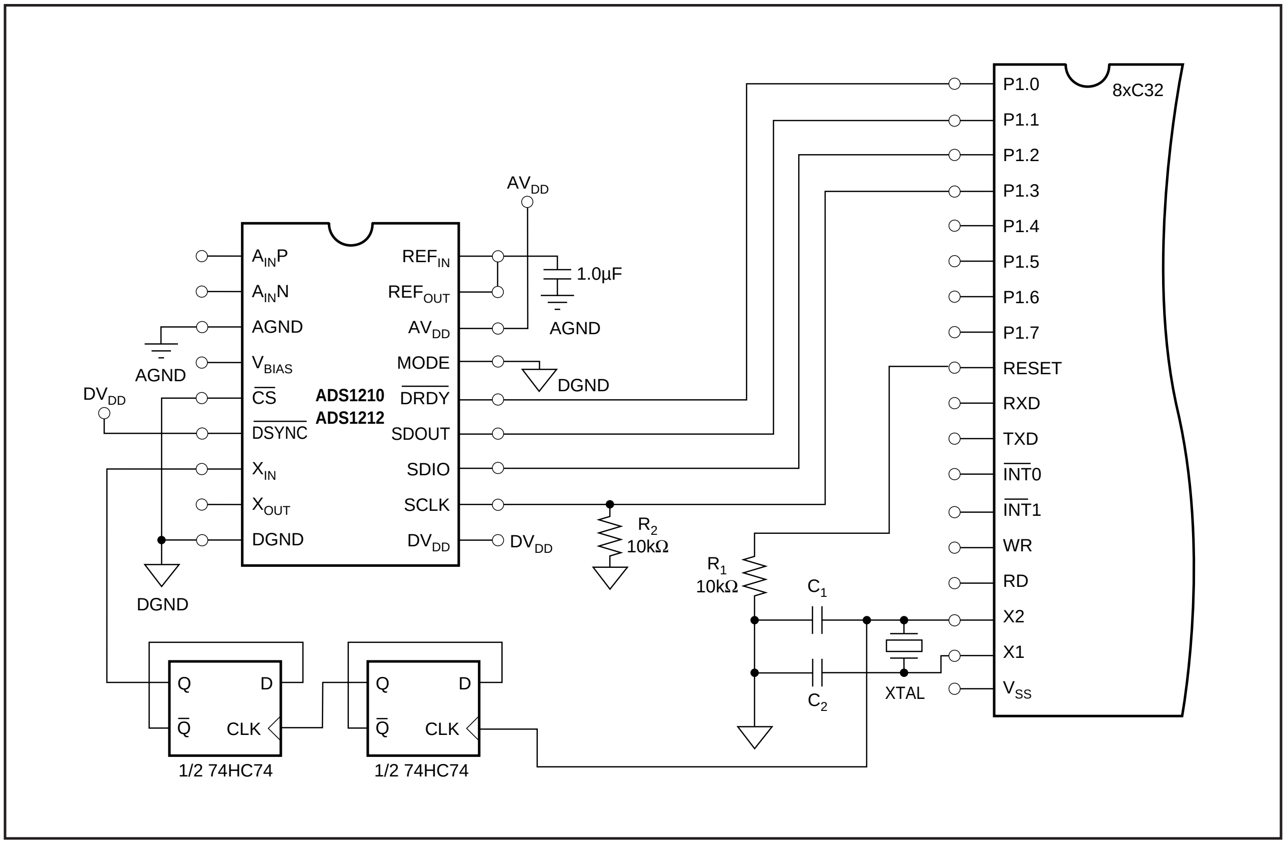

FIGURE 1. Four-Wire Interface with a 8xC32 Microprocessor.

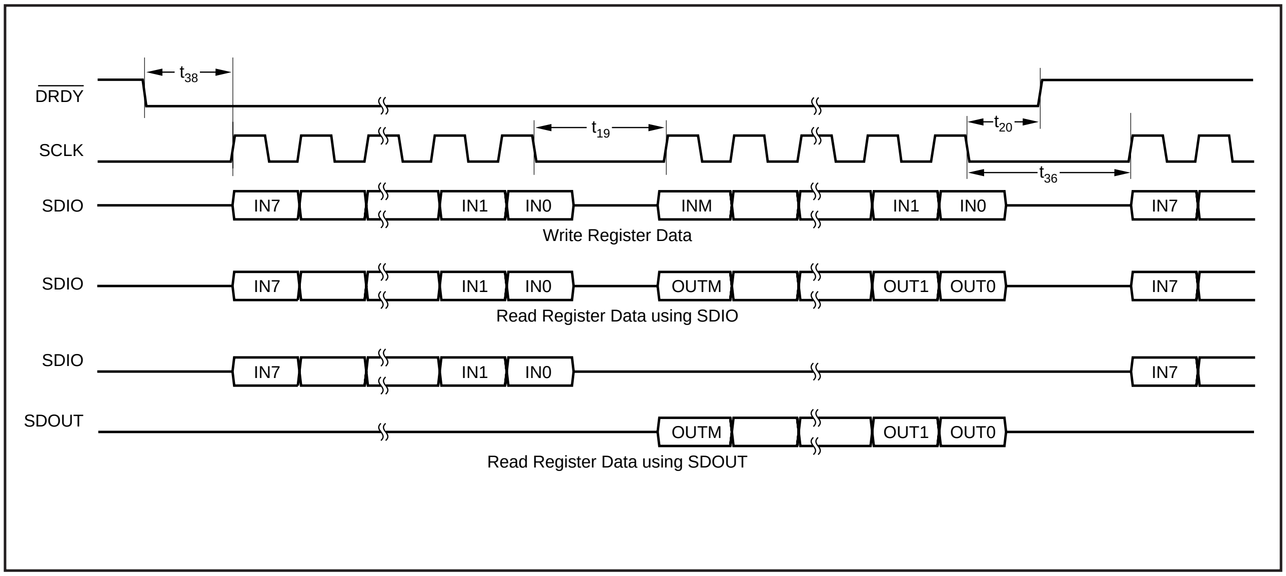

FIGURE 2. Serial Interface Timing ($\overline{CS}$ LOW), Slave Mode. Refer to product data sheet for specific times.

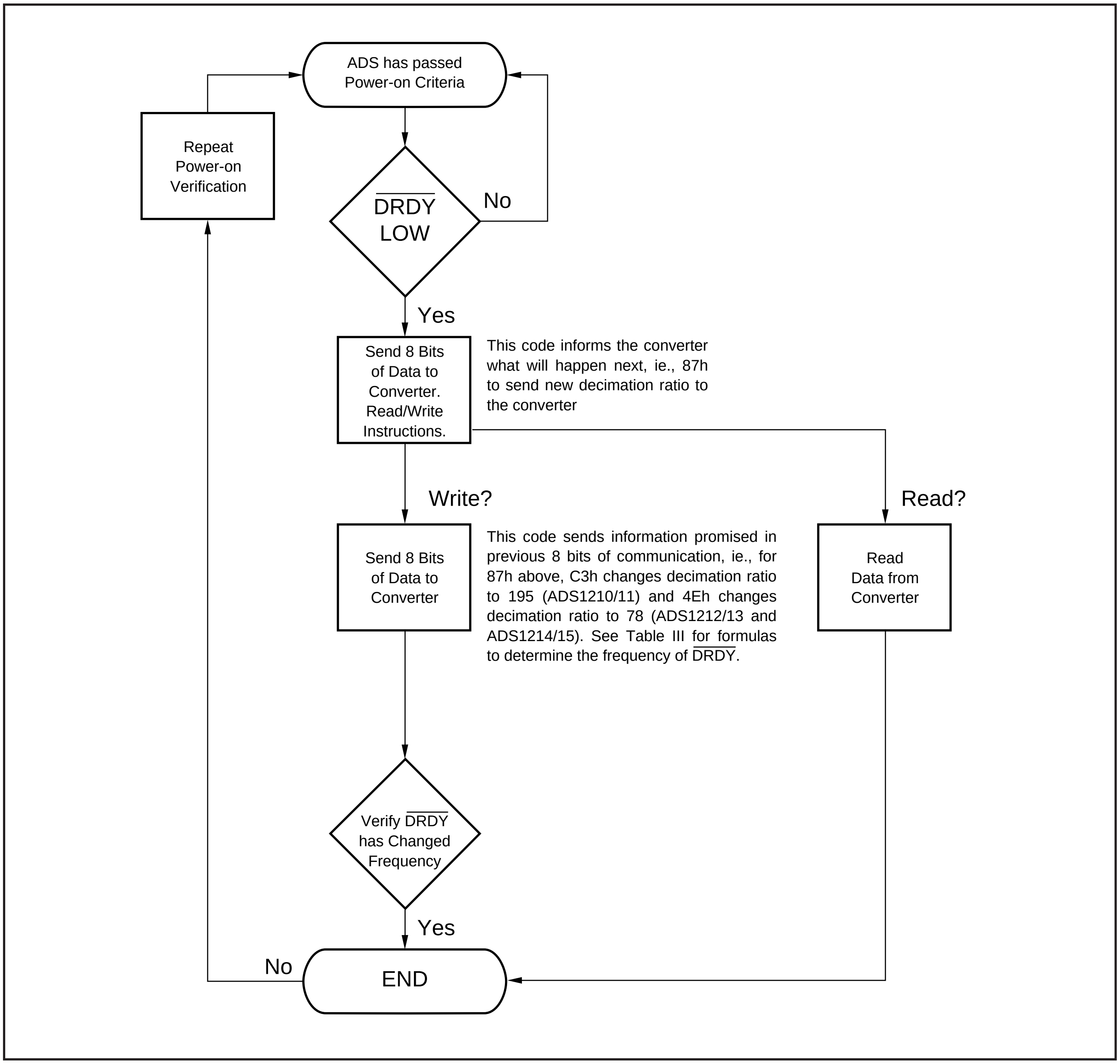

FIGURE 3. This Flow Chart will Program the A/D Converter to Change the Frequency on the $\overline{\text{DRDY}}$ Output Pin.