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APPLICATION BULLETIN
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ADS121x ANALOG-DIGITAL CONVERTER APPLICATIONS PRIMER

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The ADS121x[1] family of analog-to-digital converters represents a unique form of device for industrial use. To accomplish the performance level of no missing codes to 24 bits and effective resolution to 23 bits (ADS1210/11) requires some special handling. Each of the members of the ADS121x family of A/D converters is a digital subsystem with an analog front-end. This paper is intended to help understand the operation and therefore make the inclusion of these unique devices easier for the system designer.

The structure of these devices is shown in the simplified circuit diagram in Figure 1. The signal processing channel is composed of a Programmable Gain Amplifier (PGA), a second-order delta-sigma modulator, and a third-order digital filter. The signal processing channel is supported by a 2.5V reference, a 3.3V bias generator, a clock generator, and a microcontroller with serial interface. Additionally, in the ADS1211 and ADS1213, a four input differential multiplexer is included.

In operation, the converter accepts a voltage at the analog input, amplifies it through the PGA, and presents that voltage to the delta-sigma modulator. The PGA is a switched capacitor circuit with gain being accomplished by the repeated sampling of the applied signal voltage being accumulated on a capacitor circuit. A unique feature of these converters, to improve effective resolution, is the Turbo Mode, which is processing extra samples of the PGA output through the delta-sigma modulator and then averaging these readings in the digital filter. This extra conversion rate is set by the Turbo Mode Rate (TMR). The values, averaged by the digital filter, are loaded into the Data Out Register (DOR). Self calibration procedures exist to compensate for offset and gain errors.

The control of all of these functions is accomplished by a combination of pin programming and internal control register values. The DOR is updated at regular intervals. Each DOR update is used to signal the opportunity to communicate with the device through a serial interface. These communication events can be used to change the values in the control registers or read the data from the DOR.

The converter is considered here from five aspects. The topics to be discussed are Analog Elements, Digital Elements, Power Supply Considerations, Internal Elements and Operational Considerations.

[1] As this Application Bulletin is going to press, the ADS1214 and ADS1215 are being introduced. These new devices differ from the devices described here in two areas. A follow-on Application Bulletin is planned to cover the unique features of these new devices.

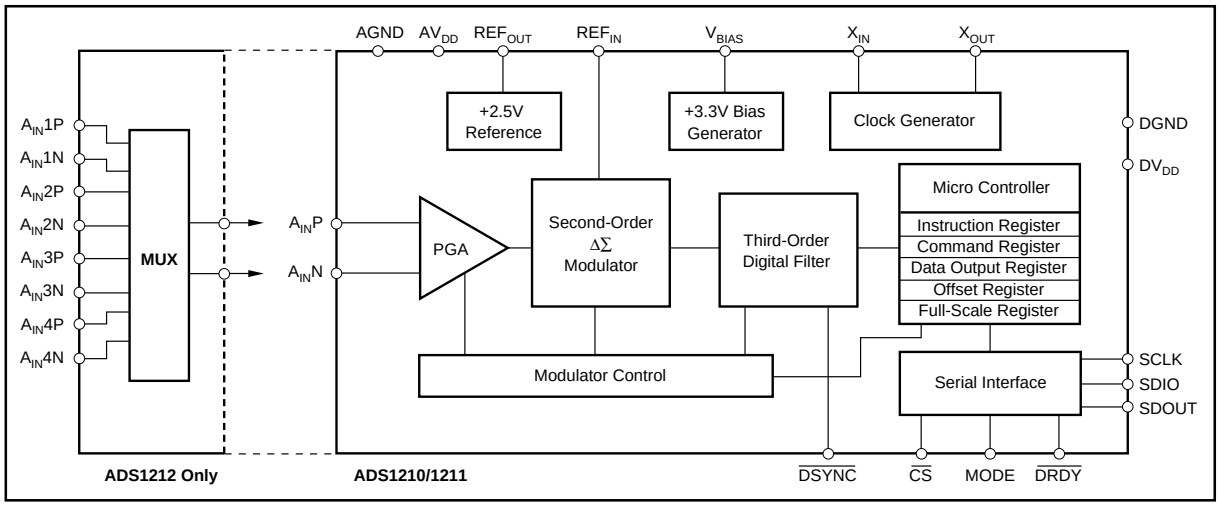


FIGURE 1. Simplified Circuit Diagram.

Printed in U.S.A. February, 1998

ANALOG ELEMENTS

The analog portion of these delta-sigma converters includes the signal input, the bias voltage, and the voltage reference. The input stage is differential with an absolute range from GND to AV_{DD} at the device input pins. V_{BIAS} is a voltage generated by the device to allow the input signal range to be extended to ±10V by adding an external resistor network. V_{REF} is the voltage that determines the device full-scale range and, therefore, the voltage of the least significant bit (LSB).

ANALOG SIGNAL INPUT

The full scale voltage calculation is best explained by a series of examples. For a converter operating in the bipolar mode, with a PGA setting of 1, and V_{REF} = 2.5V, if V_{inP} = 5V and V_{inN} = 0V the output will be positive full scale. With V_{inP} = 0V and V_{inN} = 5V the output will be negative full scale. The Full Scale Range (FSR) will be 10V. Notice that the absolute value of the input voltage never went below AGND or above +5V.

For PGA set at a gain of 2 and V_{REF} = 2.5V again, the problem becomes more interesting. With V_{inP} < 5V and V_{inP} – V_{inN} = 2.5V the output will be positive full scale, and with V_{inP} > 0V and V_{inN} – V_{inP} = 2.5V the output will be negative full scale. The Full-Scale Range (FSR) will be 5V. In no case may any of the applied voltage levels go above the supply voltage or below ground.

If single-ended input is used with V_{inN} connected to ground the full-scale range is cut in half. Errors in offset voltage and full-scale gain can be compensated through several calibration procedures discussed under operations.

As a signal sampling device care must be taken to avoid signal aliasing. The sampling frequency is given by:

$$f_{SAMP} = \frac{f_{XIN} \bullet TMR \bullet G}{K_1} \qquad \text{Note}^2$$

Where: K_1= 512 for the ADS1210/11
and 128 for the ADS1212/13.

[2] Many of the formulas in this paper contain constants that are model dependent. The symbol K_{SUB} is used where a unique subscript is assigned for that formula.

The digital filter will remove other frequency components at integer multiples of the sampling frequency.

The input impedance is of concern for anti-aliasing filter design. A circuit model is shown in Figure 2.

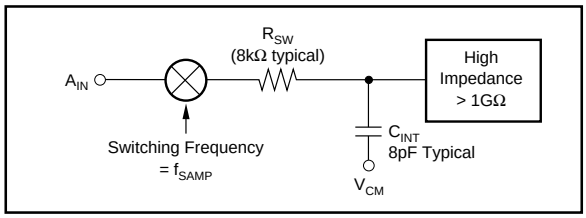


FIGURE 2. Input Impedance Model.

As noted above, the input of the ADS121X is a switched capacitor, programmable gain amplifier. As such the input impedance is a function of the gain (G), the system clock frequency (f_{IN}), and Turbo Mode Rate (TMR). These variables are defined in the Product Data Sheet (PDS) as well as here, and the method for setting them will be explained under the Digital Elements section of this paper. This function is:

$$Z_{IN} = \frac{f_{XIN(max)} \bullet K_2 \bullet 10^6}{f_{XIN} \bullet G \bullet TMR}$$

	K_2	$f_{XIN\ (max)}$
ADS1210/11	4.3	$10 \bullet 10^6$
ADS1212/13	20	$2.5 \bullet 10^6$

BIAS VOLTAGE

The V_{BIAS} voltage is generated by an internal gain stage of approximately 1.33 applied to V_{REF}, whether V_{REF} is internal or external. This added functionality does cost in accuracy and temperature drift. The gain stage and the external resistors have a temperature drift coefficient which must be considered. To conserve power V_{BIAS} can be turned off by software command. If turned off the V_{BIAS} pin goes to a high impedance state.

The input signal range can be changed from the 10V default value by adding a resistor network as shown in Figure 3.

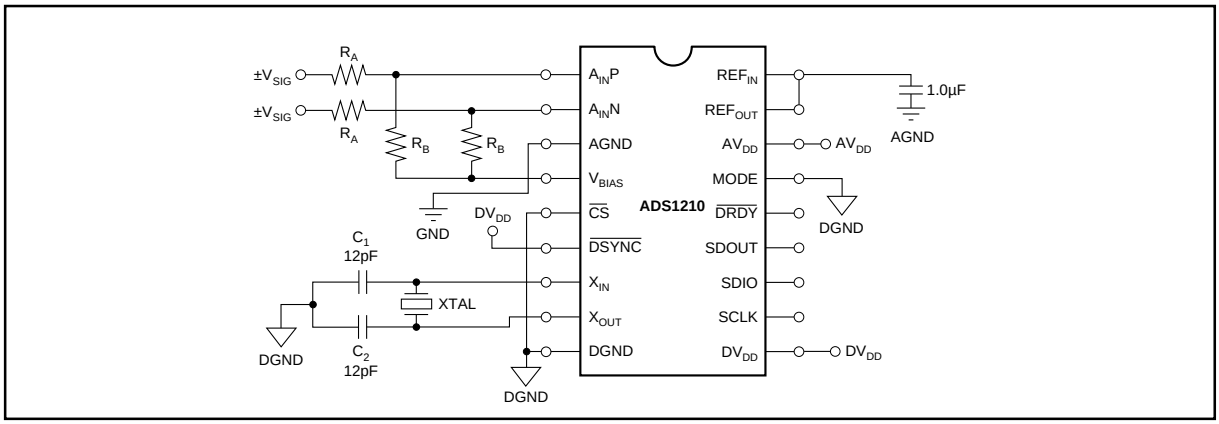


FIGURE 3. Input Signal-Range Modification Circuit.

The resistor values are calculated by applying the following relationship. Since the current through R_A must equal the current through R_B:

$$\frac{V_{SIG}\big|_{max} - A_{IN}P\big|_{max}}{R_A} = \frac{A_{IN}P\big|_{max} - V_{BIAS}}{R_B}$$

Substitute the voltages and solve this expression for the ratio of R_A to R_B. The allowed current load on the V_{BIAS} source will determine the sum of the resistors.

REFERENCE VOLTAGE

The reference voltage has two aspects. The internal generator may be buffered and used in other parts of the system or an external reference may be generated to replace the built in circuit for greater accuracy. Under software control the internal reference can be disabled. This will save some power.

V_{REF} IN

Because the internal reference voltage is generated by a CMOS circuit it has higher noise than a bipolar reference. In laboratory experiments data taken with the internal reference was 1.5 to 2 times noisier than the data taken with a REF1004. The REF1004 is a bandgap reference device with a nominal output voltage of 2.5V. Therefore, to obtain the maximum effective resolution for the converter an external reference is necessary. V_{REF} may be between 2.0V and 3.0V with 2.5V as nominal. The input impedance of the V_{REF} pin is given by:

$$Z_{IN} = \frac{f_{XIN(max)} \bullet K_3 \bullet 10^6}{f_{XIN} \bullet TMR}$$

Where: K_3 = 1 for ADS1210/11
and 5 for ADS1212/13

Changes in the value of V_{REF} will reflect in the full scale range of the device. A higher value V_{REF} will result in an increased LSB value which, for constant noise, will yield a better signal to noise ratio and effective resolution.

V_{REF} OUT

This pin will source or sink up to 1mA of current to supply other circuits. Dynamic loads on this pin can compromise the overall accuracy. Under software control this output can be turned off. Turning V_{REF} off reduces power supply current draw and the pin goes to a high impedance state.

DIGITAL CONSIDERATIONS

Since this chip is primarily digital the options here are greater in number than in the analog area.

CLOCK - X_{IN}/ X_{OUT}
MODE - Master versus Slave
$\overline{DRDY}$ - Data Ready
$\overline{CS}$ - Chip Select
$\overline{DSYNC}$ - Data Sync Control
SDIO, SDOUT, and SCLK - Serial Interface Signals

All of these signals may be under the control of the host computer.

CLOCK

X_{IN} and X_{OUT} are connections for the system clock circuits. This is the basic operating clock signal. An external oscillator may be connected to X_{IN}, or a crystal or ceramic resonator may be connected between X_{IN} and X_{OUT}. The best noise performance is obtained when a sine wave is used. High frequency components of a square wave clock are radiated and contaminate the analog signals. A type MP100 crystal from CTS produces a sine wave which yields good noise performance. Ceramic resonators with load capacitance from 32pF to 470pF have been used with the ADS1210/11, however, the ADS1212/13 does not have enough drive capability to function with ceramic resonators.

To determine the sensitivity of the converter to various clock signals an experiment was performed using a function generator as the source. Four signals were tested with the results in Table I.

SIGNAL DESCRIPTION	EFFECTIVE RESOLUTION μV (rms)	DEGRADATION IN RESOLUTION FROM BEST
Sine Wave	16.181	Best
80% Duty Cycle Pulse	30.963	0.94 Bits
20% Duty Cycle Pulse	37.928	1.23 Bits
Square Wave	61.831	1.94 Bits

TABLE I. Resolution Based on System Clock Waveform.

MODE

With MODE control tied high the device is in the MASTER mode, alternately, MODE low sets the SLAVE mode.

Characteristics of the MASTER MODE:

SCLK is generated on chip at 0.5 • X_{IN} clock for the ADS1210/11 and 0.25 • X_{IN} clock for the ADS1212/13.

All serial clock cycles will be produced by the device.

Only one instruction is allowed per data cycle.

The SLAVE MODE:

SCLK is an input with a maximum frequency of $f_{XIN}/5$ and $f_{XIN}/10$ for the ADS1210/11.

Serial clock cycles may be started any time.

Multiple instruction cycles are allowed per data cycle.

$\overline{DRDY}$ (Data Ready)

The level on this output pin reports the state of the Data Output Register (DOR). When new data has been loaded into the DOR this pin goes LOW. At this time the device is ready for a new instruction/command sequence. Upon completion of that command the level goes HIGH. This sequence is independent of MODE. In the SLAVE mode additional instruction/command sequences may be completed. If no instruction is transmitted $\overline{DRDY}$ stays low until the next conversion result is ready to be loaded into the DOR. At that time $\overline{DRDY}$ will go HIGH for X_{IN} • n clock periods, where n = 12 for the ADS1210/11 and 24 for the ADS1212/13. If reading of the DOR is in progress then the old data, which is being read, is retained and the new data is discarded.

$\overline{CS}$ (Not-Chip Select)

This pin might better have been named CR/$\overline{CLKEN}$ for Continuous Read/Not-Clock Enable. When this pin is low SCLK is enabled. When it is high the data clock will be inhibited if other conditions are met, but also, a state called Continuous Read Mode is enabled.

When this pin is taken high SCLK is disabled if the serial interface is NOT in the process of a transfer. This pin will delay start of a transfer but will not interrupt a transfer.

The alternate function assigned to this pin is the Continuous Read Mode. When the pin is taken high the first time the Continuous Read Mode is enabled[3] and can not be disabled, except by power cycle reset. The Continuous Read Mode will be entered if the $\overline{CS}$ pin is held low, after $\overline{DRDY}$ goes high, following an INSR/Byte Transfer operation. On the next $\overline{DRDY}$ cycle the Continuous Read Mode will be entered. In normal operating mode the device would wait for an INSR write cycle, however, in the Continuous Read Mode the device will operate with the contents of the instruction register from the last cycle, whatever that might have been. Normally this will be to output the data register contents. Action will continue in either Slave or Master mode until the Continuous Read Mode is exited by taking the $\overline{CS}$ high for N, or more, X_{IN} clock cycles and then low again (N = 10.5 for the ADS1210/11 and 22 for the ADS1212/13)

$\overline{DSYNC}$ (Not-Data Sync)

This is another multi-use pin. In systems with multiple converters it may be necessary to start all data collection sequences at the same point in time. By holding this pin low for 10.5 • t_{XIN} on the ADS1210/11 (22 • t_{XIN} on the ADS1212/13) or more the modulator count is reset. With all converters operating on a common X_{IN} and having been set to the same Turbo Mode and Decimation Ratio all modulator counts start at zero. Thus all $\overline{DRDY}$ lines will go low at the same time. This is accurate to within one period of the X_{IN} clock. $\overline{DRDY}$ is inhibited until $\overline{DSYNC}$ goes high.

This ability to clear the modulator count can be used to advantage even with a single converter system. If the embedded controller is informed that the signal has changed drastically, perhaps by moving the multiplexor or changing the PGA gain the system would normally wait for the required four data periods to be sure the digital filter was properly loaded or pulse the $\overline{DSYNC}$ pin. Three data periods after $\overline{DSYNC}$ is released the data will be valid. This can save one data period in waiting for valid data output.

SERIAL INTERFACE

The action of these converters is controlled by commands transferred over a serial link. The realization of the communications link is dependent on the nature of the host controller and the degree of flexibility required for the specific application. A major factor in this design decision is the MODE (Master or Slave) of operation. The signals which compose the Serial Interface are: SCLK, SDIO, and SDOUT. The serial interface is covered in detail in a separate Application Bulletin and therefore will not be treated in detail here.

The serial interface has a self resetting ability. If a communication operation is interrupted before completion for a length of time equal to 8 • t_{DATA} then the I/O function is reset. The converter has taken the position that the host has lost track of the communication channel. This procedure allows the device to system to recover without reset. No register contents are changed. This operation can only occur when in the slave mode.

SCLK - (Serial Clock)

This pin is either output or input, depending upon the MODE of the device. If the converter is operated in the MASTER mode then this pin is an output operating at one-half of the X_{IN} frequency for the ADS1210/11 and one-quarter of the X_{IN} frequency for the ADS1212/13. If the converter is operated in the SLAVE mode then this pin is an input with a maximum frequency of X_{IN}/N, where N = 5 for the ADS1210/11 and 10 for the ADS1212/13. Independent of mode or pin use the new data bit is brought to the input or output pin after this clocks rising edge so it is available before the clock falls and the data is held for a minimum time after the falling edge.

A secondary function for this pin, in the SLAVE mode, is to accomplish a device reset. If the SCLK period is modulated in accordance with the description in Figure 4 then the converter will be reset as if the power had been cycled. This function requires that the $\overline{CS}$ is low and the $\overline{DRDY}$ is high. The contents of the control registers are reset to the default state and no communication can be attempted with the device for 59,000 periods of the system X_{IN} clock. If the device is normally operated in the MASTER mode then it will be necessary to change to SLAVE before the reset operation is started.

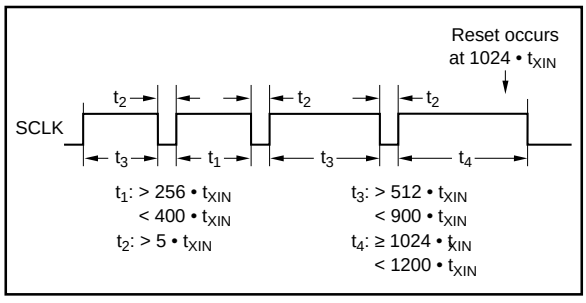


FIGURE 4. SCLK Timing to Reset the Converter.

After this reset the control registers are to their default values as described in the INTERNAL ELEMENTS section that follows.

SDIO - (Serial Data Input/Output)

Following power up or SCLK reset this pin is the input/output data link. It is possible to change the configuration of

[3] The terms "ENABLED" and "ENTERED" are used here with exact meaning. A mode is "ENABLED" (ie: the device is made ready for the mode) by one action. That mode is "ENTERED" (ie: started) by a second action. The mode may be "ENABLED" but never "ENTERED".

the serial interface to assign the data out function to another pin (SDOUT) and leave this as the input pin. This pin reassignment is accomplished through a command byte which is discussed later.

SDOUT - (Serial Data Output)

This pin may be configured as the data output if desired. By setting a bit in the command register the reassignment is made. If this function is not used then the pin should be left open.

POWER SUPPLY CONSIDERATIONS

On the surface the power considerations for this family of converters is straight forward, two 5V supply pins with their respective return paths are all that need be serviced. In reality, the power supply considerations to achieve maximum accuracy require some planning. While the analog supply is the most critical, high frequency noise on the digital supply may contaminate the analog side of the converter. Good power supply decoupling is necessary for optimum operation of the converter. A 0.1µF ceramic capacitor in parallel with a 1µF to 10µF capacitor is considered minimum. In those systems where a single 5V supply is all that is available, it is recommended that the analog side be supplied directly and the digital side be isolated by a series 10Ω resistor and the supply further filtered with the capacitor pair described above as shown in Figure 5. The ceramic capacitors should be placed as close as possible to the supply pins of the converter.

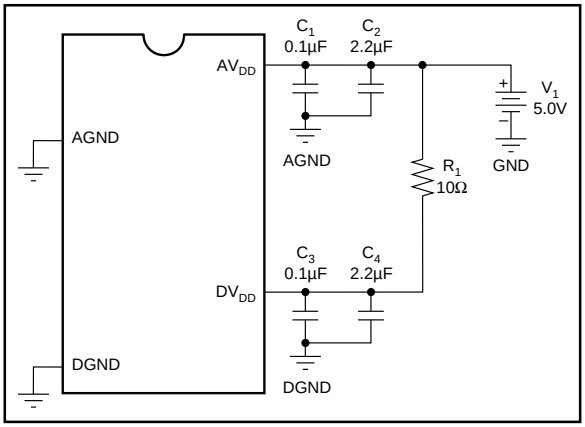


FIGURE 5. Suggested Connections for Combined AV_{DD} and AV_{DD}.

It is critical that the Absolute Maximum specification which states DV_{DD} must be no more that 0.3V more positive than AV_{DD} be kept. Exceeding this limit for even a short time can cause the converter to enter a lock-up state.

LAYOUT AND GROUND CONSIDERATIONS

The pin assignment on these devices is such as to suggest a clean division between analog and digital. In a single converter system all analog circuit elements would share one ground plane and all digital a separate ground plane. These two planes should not overlap and should be joined with one signal trace under the converter. In multi converter systems the junction of the two grounds should be close to the geometric center of the system. There may be several possible points and the best choice may need to be determined by experimentation.

POWER TURN-ON AND RESET OPERATIONS

Since the converter is generally a digital circuit the power turn-on sequence and timing is critical. The analog supply must come up before the digital and both must rise within 100ms. All digital signal lines should be held stable for 25ms after power is stable or there is a good chance that the chip will enter an abnormal state which can only be exited by reset. In those cases where power cycle reset is used it is necessary to maintain the power off condition for a minimum of 300ms. A shorter off cycle does not allow internal cells to fully discharge. A software reset can be accomplished as has been discussed previously (See the SCLK description under Serial Interface).

POWER SAVING MODE (SLEEP)

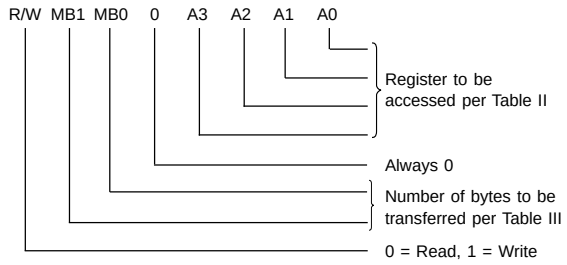
It is possible through serial command to place these converters in a standby or sleep mode. This mode is entered by sending a unique command over the serial link. Upon entering the sleep mode device power dissipation is reduced to 18% of maximum in the ADS1210/11 and to 5.3% in the ADS1212/13. To insure quick recovery from the sleep mode the internal oscillator is not turned off.

In the sleep mode V_{REF} and V_{BIAS} are not turned off. To realize the power reduction given in the specification table they must be turned off separately. Turning these voltage generators off places the output pins in a high impedance state.

Exiting the sleep mode requires establishing serial communication. The action required depends on the mode of operation. If $\overline{CS}$ is used then taking it low will restart serial communication. This is MODE independent. If $\overline{CS}$ is tied LOW then the required action is MODE dependent. In MASTER mode the SDIO line must see a falling edge. If the SDIO is low then it must be taken high for a minimum of 2 • t_{XIN} periods. In SLAVE mode simply sending a normal instruction will end the sleep mode.

INTERNAL ELEMENTS

These converters are controlled by signals sent over the serial communication link described above. With few exceptions these communications are time framed by the $\overline{DRDY}$ signal. At the end of a data period a value is loaded into the Data Output Register (DOR) and the $\overline{DRDY}$ line is pulled LOW. The converter will hold the data until instructed otherwise or the data is overwritten by the next result. The first byte sent to the converter is loaded into the Instruction Register (INSR). This byte defines the next communication packet.



The INSR is a write only register. It does not have a register address and therefore cannot be read.

REGISTER BYTE	A3	A2	A1	A0
Data Output Register Byte 2 (MSB)	0	0	0	0
Data Output Register Byte 1	0	0	0	1
Data Output Register Byte 0 (LSB)	0	0	1	0
Command Register Byte 3 (MSB)	0	1	0	0
Command Register Byte 2	0	1	0	1
Command Register Byte 1	0	1	1	0
Command Register Byte 0 (MSB)	0	1	1	1
Offset Cal Register Byte 2 (MSB)	1	0	0	0
Offset Cal Register Byte 1	1	0	0	1
Offset Cal Register Byte 0 (LSB)	1	0	1	0
Full-Scale Cal Register Byte 2 (MSB)	1	1	0	1
Full-Scale Cal Register Byte 1	1	1	0	1
Full-Scale Cal Register Byte 0 (LSB)	1	1	1	0

TABLE II. Register Byte Addresses.

1 Byte	0	0
2 Bytes	0	1
3 Bytes	1	0
4 Bytes	1	1

TABLE III. Codes for Number of Bytes Transferred.

This data is written to the converter Most Significant Bit (MSB) first. In a multi byte, successive write operation, the highest numbered byte is taken first. Later discussions will cover changing the byte order on read operations, but the write order is fixed. The DOR, Offset Calibration Register and Full-Scale Calibration Register are all value registers. The value of the binary number read from or written to these registers is the information. The command register takes four bytes to define thirteen variables ranging in length from one bit to thirteen bits. This bit definition is given in Table III. The default (reset value) is given for each variable. This register may be read as well as written.

BIAS (Bias Voltage)—A one enables the V_{BIAS} generator output pin. The voltage will be 1.33 times the V_{REF}. A zero sets the pin to a high impedance state and reduces the device quiescent current.

REFO (Reference Output)—A one enables the V_{REF} pin at the internally set value of 2.5V. A zero disables the circuit and reduces the device quiescent current.

DF (Data Format)—A one sets the data output number system to Offset Binary (See Table V for example). A zero sets the data output number system to Two's Complement. This applies only to the values in the DOR.

Most Significant Bit **Byte 3**

BIAS	REFO	DF	U/$\overline{B}$	BD	MSB	SDL	DSYNC(1) $\overline{DRDY}$	
0 Off	1 On	0 Two's	0 Biplr	0 MSByte	0 MSB	0 SDIO	0	Defaults

NOTE: (1) DSYNC is Write only, $\overline{DRDY}$ is Read only.

Byte 2

MD2 MD1 MD0	G2 G1 G0	CH1 CH0	
000 Normal Mode	000 Gain 1	00 Channel 1	Defaults

Byte 1

SF2 SF1 SF0	DR12 DR11 DR10 DR9 DR8	
000 Turbo Mode Rate of 1	00000	Defaults

Byte 0 Least Significant Bit

DR7 DR6 DR5 DR4 DR3 DR2 DR1 DR0	
(00000) 0001 0111 (23) Data Rate of 850Hz	Defaults

TABLE IV. Command Register Organization with Default Values.

DF	FORMAT	ANALOG INPUT	DIGITAL OUTPUT	
0	Two's Complement	+Full-Scale	$7FFFFF_H$	Default
		Zero	000000_H	
		–Full Scale	800000_H	
1	Offset Binary	+Full-Scale	$FFFFFF_H$	
		Zero	800000_H	
		–Full-scale	000000_H	

TABLE V. Data Format Examples.

U/$\overline{B}$ (Unipolar Bit)—A one sets the output to the unipolar mode and negative numbers are not allowed in the DOR. Data values less that zero are reported as zero. A zero in this position allows normal bipolar operation.

BD (Byte Order)—This bit affects the sequence of the bytes as they are read from the device. A one causes the contents of INSR(A3..A0) to point to the least significant byte for the first read and then advance to the most significant byte. A zero causes the contents of INSR (A3..A0) to point to the most-significant byte and then advance to the least significant byte on successive reads. Byte order is not changed on write operations.

MSB (Bit Order)—This bit affects the bit order as data is read from the registers. A one causes the Least Significant Bit (LSB) to be sent first. A zero causes the MSB to be sent first. As with BD, this bit has no effect on the bit order of the write operations.

SDL (Serial Data Line)—This bit specifies the serial data output pin. A one selects the SDOUT line as output. A zero selects the SDIO to be both input and output, as such it is bi-directional. Note that the bi-directional state is the default condition. Therefore, at start-up, in the Master mode, bus contention is possible until the command register can be modified.

$\overline{DRDY}$ (Data Ready) and DSYNC (Data Synchronization)—This is the only dual function bit in the Command Register and it duplicates the hardware functions of the same names. All of the comments concerning the hardware realization of these functions applies here. The DSYNC bit functions as if the pin was taken low for a minimum time ant then returned high.

MD2-MD0 (Operating Modes)—The code in this bit position sets the mode of operation according to the chart below. Since several variables are involved this subject is treated in detail at the end of this section.

G2-G0 (PGA Gain Set)—This bit pattern sets the input capacitor sampling rate as a function of the main system clock f_{XIN}. The equivalent gain settings are given in the table below. Notice that this setting operates in concert with the Turbo Mode Rate discussed below.

G2	G1	G0	GAIN SETTING	POSSIBLE TURBO MODE RATES	
0	0	0	1	1, 2, 4, 8, 16	Default
0	0	1	2	1, 2, 4, 8	
0	1	0	4	1, 2, 4	
0	1	1	8	1, 2	
1	0	0	16	1	

TABLE VI.

CH1-CH0 (Channel Selection)—These are the multiplexer control bits. On those devices with a four channel multiplexed input (odd model numbers) the channel selection is per the table. For those devices that do not have a multiplexer these bits must be zero.

CH1	CH0	ACTIVE INPUT	
0	0	Channel 1	Default
0	1	Channel 2	
1	0	Channel 3	
1	1	Channel 4	

TABLE VII. Input Multiplexer Codes.

SF2-SF0 (Turbo Mode Rate)—The bit pattern here sets the delta-sigma modulator rate. By over sampling and averaging the result a higher number of significant bits can be realized. The table below gives the TMR for each bit pattern. Notice that the product of gain times TMR has a maximum value of sixteen.

SF2	SF1	SF0	TURBO MODE RATE	POSSIBLE GAIN	
0	0	0	1	1, 2, 4, 8, 16	Default
0	0	1	2	1, 2, 4, 8	
0	1	0	4	1, 2, 4	
0	1	1	8	1, 2	
1	0	0	16	1	

TABLE VIII. TMR Codes.

DR12-DR0 (Decimation Ratio)—This thirteen bit word sets the number of samples that are averaged for each data word. For maximum effective resolution the TMR should be set as high as possible. The Decimation_Ratio is given by the following expression.

$$\text{Decimation\_Ratio} = \frac{f_{XIN} \bullet \text{TMR}}{K_4 \bullet f_{DATA}} - 1$$

Where: K_4 = 512 for the ADS1210/11
and 128 for the ADS1212/13

Valid decimation ratios are between 20 and 8000. Values outside of this range will yield incorrect results from the digital filter.

OPERATIONAL DESCRIPTION

The modes of operation are defined by the contents of the command register, Byte 2, MD2-MD0, and are variations in the self calibration feature or sleep mode. Table IX contains a list of the modes.

MD2	MD1	MD0	MODE	OPERATING MODE
0	0	0	Perm	Normal Mode
0	0	1	Temp	Self-Calibration
0	1	0	Temp	System Offset Calibration
0	1	1	Temp	System Full-Scale Calibration
1	0	0	Temp	Pseudo System Calibration
1	0	1	Perm	Background Calibration
1	1	0	Perm	Sleep
1	1	1		Reserved

TABLE IX. Operating Mode Codes.

Permanent modes stay in force until changed. Temporary modes only stay in force for one action cycle, and then will revert to normal mode.

Normal Mode is conventional data conversion. Contents of OCR and FSR are applied to the data as it is loaded into the DOR. The contents of these correction registers may be placed there by a calibration cycle or loaded over the serial link from the host controller.

The conditions applied to the device for the various calibration sequences are summarized in Table X.

MODE	SKIPPED DATA FRAMES[1]	ZERO	FULL-SCALE	RETURN TO NORMAL MODE
Self Calibration	6/7	Shorted	Reference	Yes
System Offset Calibration	3/4	Input	N/A	Yes
System Full-Scale Calibration	3/5	N/A	Input	Yes
Pseudo System Calibration	6/7	Input	Reference	Yes
Background Calibration	3/4[2]	Shorted	Reference	No

NOTES: (1) Number of data frames missed. No $\overline{\text{DRDY}}$ pulse. Master/Slave mode. (2) Frames missed in first cycle, only if in slave mode.

TABLE X. Operating Mode Effects Chart.

For “System Full Scale Calibration” the device will treat the applied voltage as the maximum signal. All other calibration modes that use the reference voltage for full scale calibration calculate the true full scale factor based on the knowledge that the actual applied voltage, V_{REF}, is one-half of the full scale value.

CONCLUSIONS

Through this Application Bulletin an attempt has been made to introduce the reader to the overall features of the ADS1210/11 and associated family of converters. These devices span the boundary between analog and digital and as such pose a problem in understanding to users with a strong background in either area. The product data sheets and the subject specific applications bulletins attempt to give the necessary insight to fully utilize these devices.