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EXTERNAL SYNCHRONIZATION OF THE DCP01/02 SERIES OF DC/DC CONVERTERS

By D. McIlroy

The DCP01/02s are a family of miniature DC-DC converters providing both step-up and step-down voltage conversions within the 1W and 2W power range. These converters are approved to UL1950 and are available in through-hole and surface-mount packages.

The DCP01/02s have the facility to be synchronized to an external frequency. This has the benefit of eliminating beat frequencies caused by two or more devices operating at frequencies that are close to one another. Additionally, with all the DCP01/02s operating at the same frequency, any EMC emissions generated will have a similar spectral density, making it easier to design circuits with high EMC immunity.

There are several methods that can be used to externally synchronize the DCP01/02 family. The following describes how to interface external circuits to the DCP01/02, and how to derive a clock pulse for synchronization.

CIRCUIT DESCRIPTION

Each DCP01/02 has an on-board oscillator that runs at a nominal 800kHz. The internal oscillator operates by charging an internal timing capacitor from a constant current of 75µA. This voltage appears on the $SYNC_{IN}$ pin in the form of a ramp. When the ramp exceeds the upper threshold, the internal discharge circuit discharges the capacitor to the lower threshold and the process repeats, as shown in Figure 1.

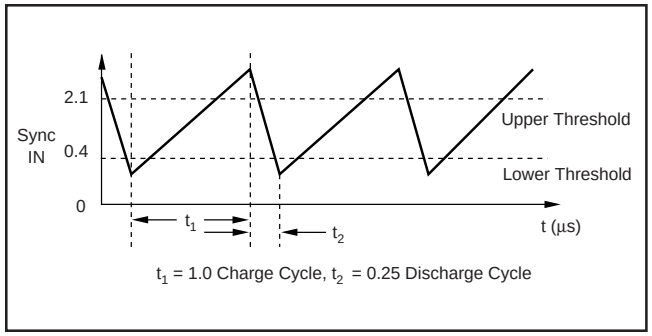

FIGURE 1. Internal Oscillator Timing.

The oscillator frequency is divided by two before being used to drive the power stages. Both the internal oscillator and the divide by two circuits are controlled from comparator outputs with a lower input threshold value of 0.4 volts and an upper input threshold of 2.1V, as shown in Figure 2.

The internal oscillator may be overridden by the application of an external signal that exceeds the comparator thresholds. Typically the signal should be 0.3V to 2.5V with a maximum peak voltage of 3.0V, and with a frequency between 720kHz to 880kHz.

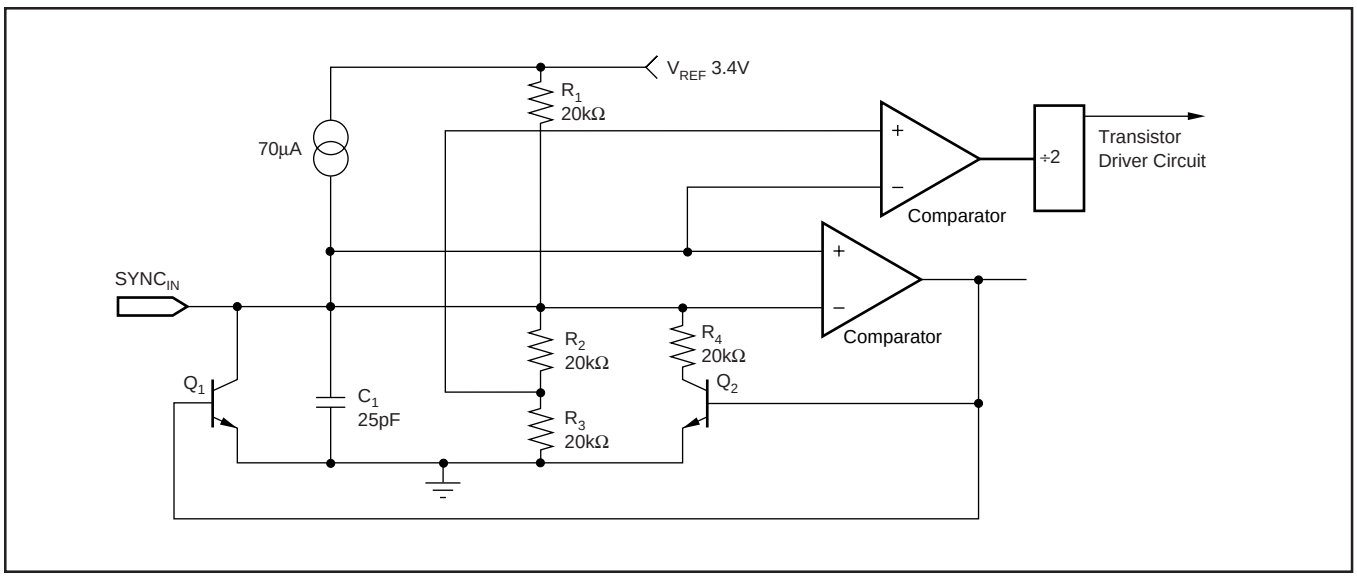

FIGURE 2. Internal Oscillator Circuit.

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EXTERNAL INTERFACE CIRCUITS

Two methods can be deployed in interfacing external circuitry to the DCP01/02. Either a signal may be applied to ensure that the internal circuits operate in phase with the external signal, thus synchronizing all the devices to a common frequency, or the internal oscillator may be disregarded by driving from an external source.

SYNCHRONIZATION USING AN EMITTER FOLLOWER CIRCUIT

Synchronization can be achieved by the injection of a positive pulse into the $SYNC_{IN}$ pin during a charge cycle, thus rapidly charging the internal capacitor. This forces the $SYNC_{IN}$ pin above the upper threshold and initiates a discharge cycle. By injecting this pulse simultaneously onto the $SYNC_{IN}$ pins of all other DCP01/02s, they will also synchronize to this external frequency.

Figure 3 shows an emitter follower configured for operation from a +5V power supply to give a 3.0Vpk signal output capable of driving eight DCP01/02 devices.

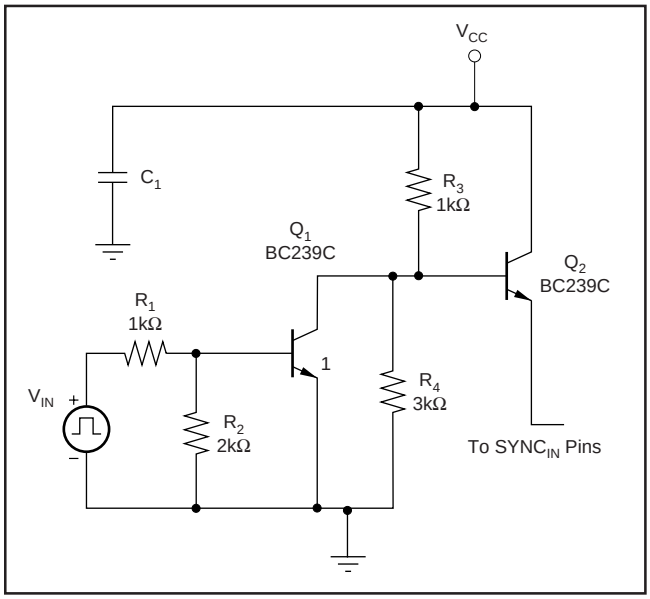

FIGURE 3. DCP01 Series, Emitter Follower Interface.

The peak output voltage is set by the resistor ratio, R_3:R_4, less the forward voltage drop, V_{BE}, of the transistor, Q_2.

$$\text{Output Voltage} = V_{CC} \bullet R_4/(R_3 + R_4) - 0.6$$

where V_{CC} = 5 in the above example.

The driving signal, V_{IN}, is fed to transistor Q_1, which is used to switch off transistor Q_2, allowing the DCP01/02 to run freely in the charge cycle. Before completion of the charge cycle, V_{IN} goes low, switching off Q_1. Consequently Q_2 is turned on rapidly, charging the internal timing capacitor. The internal discharge cycle is delayed until Q_2 is turned off. When the discharge cycle is complete, a charge cycle is initiated automatically.

The choice of Q_1 will depend upon the available driving source, however, most readily available logic levels can be accommodated by careful choice of values for R_1 and R_2. Q_1 can be replaced with an FET with an appropriate gate threshold voltage. Caution must be exercised to ensure that Q_1 is not driven into heavy saturation, necessitating a long recovery time, as this would prevent the circuit from running. Likewise, an FET with a low capacitance should be chosen if being driving from a high impedance source. Capacitor C_1 is provided for power supply filtering.

The duty cycle of the driving signal is not critical. A value within the range of (20% – 60%) will ensure correct operation, as shown in Figure 4.

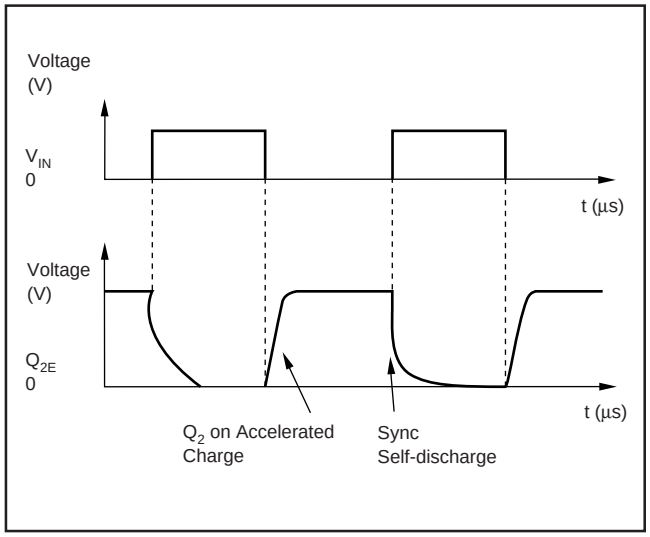

FIGURE 4. Emitter Follower Output Waveform V_S and V_{IN}.

Important Note: The frequency of the internal oscillator is dependant upon the internal capacitor. This signal has a value of approximately 34pF at the $SYNC_{IN}$ pin. Therefore, using an oscilloscope probe to monitor this signal places additional capacitance in parallel with the internal capacitance, and reduces the frequency of oscillation. If it is required to view the waveform at this point, a low capacitance probe must be used (i.e., x100), and caution must be exercised to ensure that the frequency is not taken outside operational limits. Otherwise, damage to the device may occur.

The frequency of the internal oscillator can be measured accurately on the DCP01s by monitoring the $SYNC_{OUT}$ pin and multiplying the frequency obtained by 2. This method ensures that the oscillator circuit is not loaded.

INTERFACING THE DCP01/02 SERIES USING HCMOS LOGIC

The ready availability and flexible operating supply voltage of the standard 74HCMOS logic family provide a suitable interface to the DCP01/02 series. If a 3.0V supply is available, the HCMOS logic family can be powered directly. Otherwise, the supply will have to be regulated.

The digital output of the HCMOS is used to force the $SYNC_{IN}$ pin high by charging the internal timing capacitor at a faster rate than internal constant current, thereby reaching the upper threshold more rapidly. The internal discharge cycle is initiated, but prevented from discharging the internal capacitor until the HCMOS logic output is low, whereby the internal discharge circuit and the HCMOS logic discharge the internal capacitor together. Although a charge cycle is initiated internally, the voltage is held low until the HCMOS logic goes high again. Therefore, the DCP01/02's oscillator is overridden by the external logic signal, as shown in Figure 5.

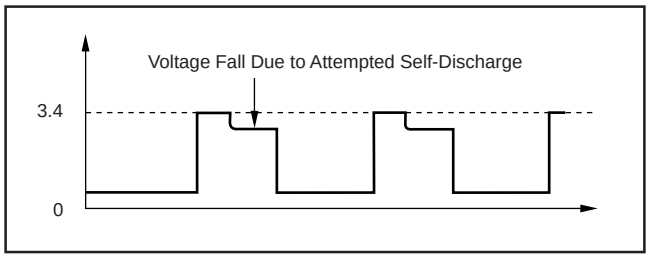

FIGURE 5. 74HC245 O/P Drive Waveform.

The maximum load presented to the HCMOS device is the charging ramp current of 75µA, as seen by the HCMOS device when its output is low, and the discharge current of 1.5mA (maximum) when the HCMOS device is still trying to hold its output high.

The choice of the 74HC245, (an octal bus transceiver) ensures that there is sufficient current output to drive a total of 3 DCP01/02 $SYNC_{IN}$ pins connected in parallel from each 74HC245 output, giving a total capability of synchronizing 24 DCP01/02 devices, as shown in Figure 6.

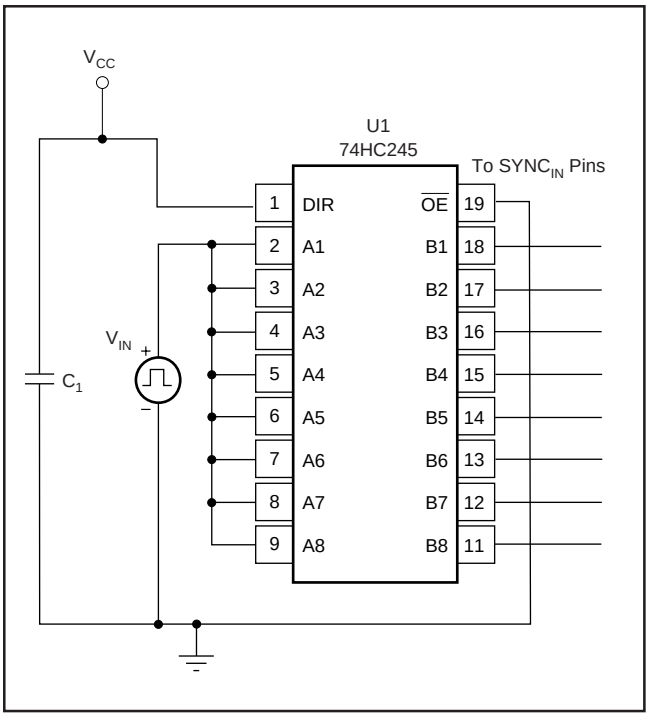

FIGURE 6. DCP01 Series HCMOS Interface.

If V_{IN} is incapable of driving all eight inputs simultaneously, one input can be driven from V_{IN} and its output used to drive the remaining inputs. Capacitor C_1 is for power supply filtering, and V_{CC} is 3.0V.

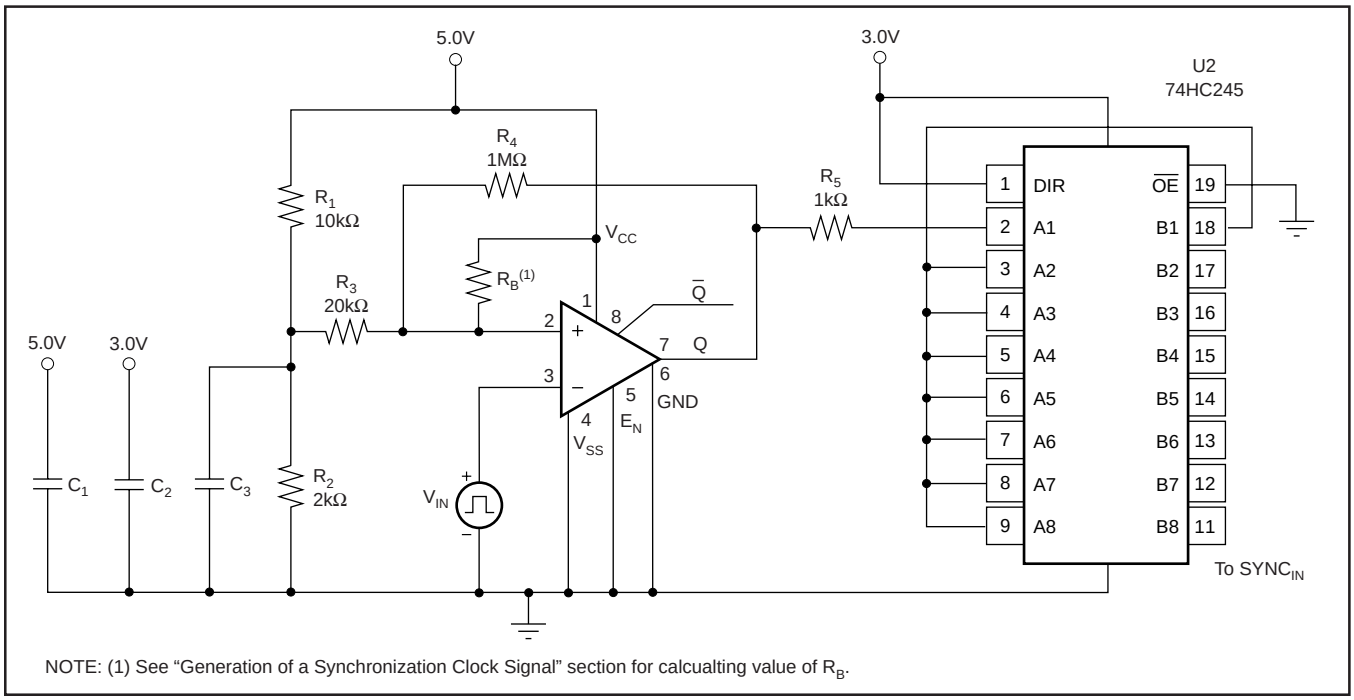

FIGURE 7. Comparator Generated Timing Pulses.

GENERATION OF A SYNCHRONIZATION CLOCK SIGNAL

In the absence of a suitable clock signal to synchronize the DCP01/02 devices, a clock signal can be derived from one of the DCP01/02 devices. This presents a master-slave situation, whereby all the slave devices are locked onto the frequency of the master device.

The $SYNC_{IN}$ pin of the master device is used to drive a comparator whose reference is set to approximately 1V (midpoint of the waveform). A pulse train is then obtained from the comparator that can be used to drive the HCMOS driver. The comparator must exhibit a low-input capacitance, as this is connected directly in parallel with the internal timing capacitor of approximately 34pF. The frequency of oscillation is lowered, approximately, by the ratio of external to internal capacitance, (i.e., 3p3 will produce approximately 10% reduction in oscillator frequency). An input capacitance of 1-2pF is ideal. The response time of the comparator must be small enough not to effect the operation of the circuit; ideally less than 100nS. The use of a single-supply comparator will give a unipolar output, making it easier to interface with the HCMOS devices.

Figure 7 shows an application using a comparator to derive a synchronizing clock pulse capable of driving a single input to the 74HC245, one of the outputs being used to drive all the other inputs.

With a supply voltage of 5.0V the comparator reference is set to a nominal 1V, with C_3 acting as a bypass filter. Resistors R_3 and R_4 provide 0.1V of hysteresis (this is necessary, as the charging ramp is changing relatively slowly). If the DCP01/02 is being operated over the specified range of input supply voltages, this will have a direct effect on the comparator reference voltage. This may be overcome by using a semiconductor voltage reference in place of R_2.

The split supplies are used to provide 5V for the comparator, and 3V for the 74HC245. This allows the HCMOS output to be connected directly to the DCP01/02 devices. R_5 is provided to limit the current from the comparator to the HCMOS part, when its output is greater than 3V.

The circuit was evaluated using a Linear Technology (LT1016) comparator whose input capacitance was given as 3.5pF. This value, plus an allowance of 3.5pF (measured with an LCR bridge) for the tracking, gives a total additional capacitance of 7pF.

In order to accommodate the additional capacitance, a bleed resistor, R_B, has been added. The current through this resistor should be sufficient to compensate for the additional capacitance, thereby making it transparent to the internal oscillator circuit.

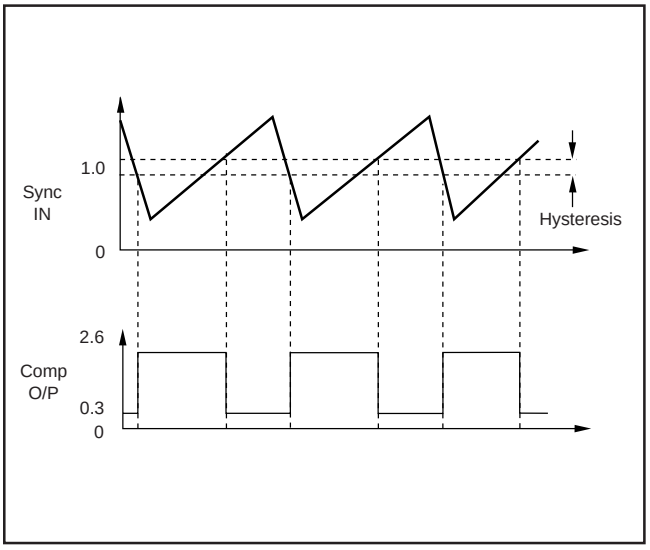

FIGURE 8. Comparator Generated Timing Pulses.

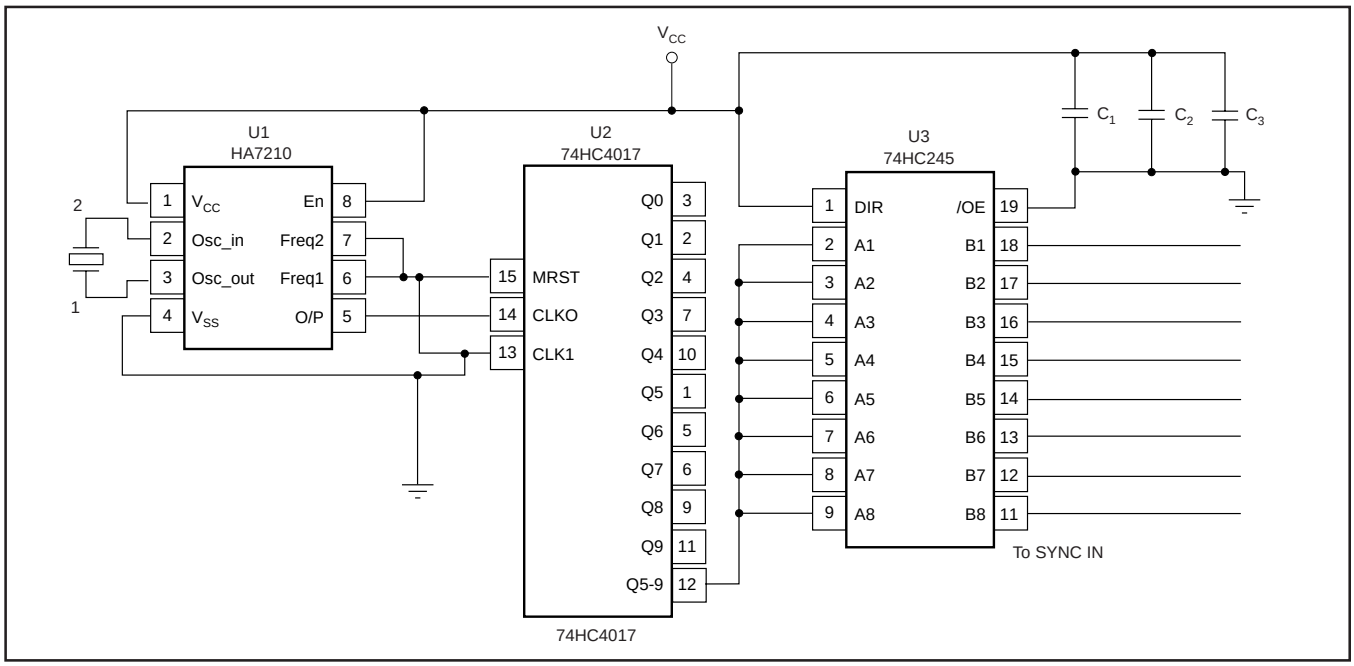

FIGURE 9. Crystal Generated Clock Signal.

The voltage on the $SYNC_{IN}$ pin is changing at a rate of:

$$\text{Voltage Rate} = \frac{\text{Constant Charge Current}}{\text{Internal Capacitance}}$$

$$= \frac{75 \cdot 10^{-6}}{34 \cdot 10^{-12}}$$

$$= 2.2\ \mu V/S$$

Nominal charge time = 1.1µS gives a peak voltage of approximately 2.4V.

To maintain this rate with the additional capacitance, the charging current has to be increased. This is now made up of the constant current plus the bleed resistor current, $I_{B:}$

$$\text{Voltage Rate} = \frac{\text{Charge Current + Bleed Current}}{\text{Total Capacitance}}$$

Or rearranging to give:

$$\text{Bleed Current} = (\text{Voltage Rate} \cdot \text{Total Capacitance}) - \text{Charge Current}$$

$$= (2.2 \cdot 10^{6} \cdot 41 \cdot 10^{-12}) - 75 \cdot 10^{-6} = 15.2\mu A$$

$$\text{Bleed Resistor} = \frac{\text{Nominal Voltage } R_B}{\text{Bleed Current}} = \frac{5 - 1.2}{15.2\mu A} = 250k\Omega$$

The voltage across the resistor is taken as the nominal, or supply voltage minus half the peak ramp voltage.

With R_B equal to 270kΩ, the circuit was tested using the DCP01series with the $SYNC_{OUT}$ pin monitored before and after the comparator circuit was added. The change in the frequency of the output signal was less than +3%.

The above gives a good guide to the value of the bleed resistor, however, as pcb layouts vary considerably, a value of resistor may be found empirically, using the above as a starting point.

The maximum value of additional capacitance using the bleed method is 10pF, as this gives rise to a non-linear ramp due to the varying voltage across the bleed resistor (this decreases as the capacitor charges).

The output waveform of the comparator switched from a low of 0.3V to a high of 4V. The output from the 74HC245 switched from 0 to 3.0V with a load of 3 $SYNC_{IN}$ pins, as shown in Figure 8.

Capacitors C_1 and C_2 are power supply decoupling capacitors.

GENERATING A CLOCK SIGNAL FROM A CRYSTAL.

See Figure 9 for an alternative circuit for generating a clock signal. U1 is an Intersil HA7210 crystal driver circuit capable of being driven by a wide range of crystal frequencies. U2 is a standard HCMOS decade counter from which the carry out pin has been used, as this gives an equal mark-to-space ratio. The crystal frequency is 8.0MHz. Therefore, the drive to the 74HC245 is 800KHz. This output is capable of driving all 8 inputs of the 74HC245 simultaneously.

CIRCUIT CHOICE.

Each circuit has its own merits and the correct solution will ultimately depend upon the specific application, however, a brief comparison can be made between the circuits.

Emitter Follower (Figure 3)

Advantages—low cost; can accept a wide variation of supply voltages; able to drive many channels.

Disadvantages—requires a logic signal at 800kHz for synchronization.

HCMOS Interface (Figure 6)

Advantages—low-cost, single-chip solution with capability of driving up to 24 DCP01/02s.

Disadvantages—requires a low-voltage supply, and a logic signal at 800kHz for synchronization.

Comparator Derived Clock Signal (Figure 7)

Advantages—self-generated clock from single DCP01/02 for synchronization to other DCP01/02s.

Disadvantages—requires fast comparator.

Crystal Generated Clock Signal (Figure 9)

Advantages—crystal-controlled clock frequency, low-component count, and capability of driving up to 24 DCP01/02s.

Disadvantages—requires low-voltage supply.

CIRCUIT LAYOUT CONSIDERATIONS.

Careful consideration should be given to the track layout of the DCP01/02 series, and in particular the 5V input version, due to the presence of high switching currents. Ideally, ground and power planes should be used on the input side. If this is not possible, then the input supply and ground must be connected in a star formation. Otherwise, large start up currents may cause the input voltage to fall below the minimum input voltage specification, and the DCP01/02 may not operate. A 2.2µF low-ESR ceramic capacitor connected across the input voltage and mounted close to the device will ensure start up on full load over the specified input voltage range. The output voltage ripple will depend on the load, the value of filter capacitor, and its value of ESR. A minimum value of 0.47µF is recommended.

When using the $SYNC_{IN}$ pin to generate a synchronizing clock pulse, it is important to note that the internal timing capacitor is 34pF and is highly susceptible to stray capacitance at the $SYNC_{IN}$ pin, which will reduce the oscillator frequency. Therefore, the tracking from the $SYNC_{IN}$ pin to the comparator must be kept as short as possible. Avoiding any tracks on adjacent layers within this area will ensure a minimum capacitance (including ground and power planes).

It should be observed that connecting an oscilloscope probe to the $SYNC_{IN}$ pin places a relatively large capacitance in parallel with the internal timing capacitor, consequently decreasing the frequency of oscillation. If the oscillator frequency is substantially reduced, damage may result to the device. Therefore, a low-capacitance oscilloscope probe must always be used (x100).