

Application Tips for the ADS1210/11

last revision : 12/23/97

1. **Data Sheet Clarification (PDS-1284C)** - Resetting the ADS1210/11 (Slave Mode only), Figure 27 (pg. 30) - This is a serial reset function for the A/D converter. The data sheet shows the time sequence of a signal through SCLK which resets the A/D converter into its default condition. A successful reset will give a 850Hz frequency output on the /DRDY pin (assuming a 10MHz clock at Xin). The data sheet specifies the time sequence of T1, T2, T1, T2, T3, T2, T4 in Figure 27. The first parameter, T1 should be T3. The correct sequence is T3, T2, T1, T2, T3, T2, T4.

2. **Data Sheet Clarification (PDS-1284C)** - Decimation Ratio Calculations (pg. 11) - In the “DIGITAL FILTER” section of the data sheet there is a formula that is used to determine the correct Decimation Ratio for a desired data rate. This formula is incorrect. It should be:

$$f_{\text{DATA}} = (f_{\text{XIN}} * \text{Turbo Mode}) / (512 * [\text{Decimation Ratio} + 1])$$

which is equivalent to:

$$\text{Decimation Ratio} = ([f_{\text{XIN}} * \text{Turbo Mode}] / [512 * f_{\text{DATA}}]) - 1$$

3. **Data Sheet Clarification (PDS-1284C)** - Calculating Effective Resolution in Bits vs. Effective Resolution in Vrms with PGA gains greater than one (pg. 10) - The formulas for the conversion from bits to Vrms on page 10 of the data sheet assume a PGA gain of one. These formulas can be used for all PGA settings by changing the constant value of “10V” (in the numerator of both equations) into a value of “10V / PGA”. To clarify these formulas, Effective Resolution in Bits is a number that refers to the digital output of the A/D converter. Effective Resolution in Vrms is a voltage and is referred to the input of the A/D converter. The second to last paragraph of page 10 is incorrect and should be ignored.
4. **Data Sheet Clarification (PDS-1284C)** - Continuous Read Mode (pg. 29) : Add this text to the last paragraph of this section - “Note that once /CS has been taken HIGH, the Continuous Read Mode will be enabled (but not entered) and can never be disabled. The mode is actually entered and exited as described previously.”
5. **Data Sheet Clarification (PDS-1284C)** - Application Circuits, Figure 43 and Figure 44 (pg. 38 and 39) - Pin 6 in the diagram is correctly labeled “AGND”, however, the connection to that pin “DV_{DD}” is incorrect. This pin should be connected to “AGND”.
6. **Data Sheet Clarification (PDS-1284C)** - I/O Recovery (pg. 32) - If serial communication stops during an instruction or data transfer, the I/O port will reset itself. This occurs after $4 * t_{\text{DATA}}$. The data sheet states in this section that the device recovers after $8 * t_{\text{DATA}}$. This is an error.
7. **Data Sheet Clarification (PDS-1284C)** - Flowchart for Writing and Reading Register Data, Slave Mode, Figure 26 (pg. 28) - In the right most flow chart, 5th box down (or second real looking box), actually reads “External device generates 8 serial clock cycles and receives instruction register data via SDIO” should read “... and TRANSMITS instruction register data via SDIO”.
8. **Data Sheet Clarification (PDS-1284C)** - CMR test conditions (pg. 2) - The common-mode rejection test is performed with a 100mV differential input.
9. **Commonly Asked Questions - What’s the best clock signal that I can provide for the ADS1210 and ADS1211?** - The ADS1210 and ADS1211 were characterized using CTS

MP100 for the XIN and XOUT pins. This part is a 10MHz crystal. A crystal, instead of a clock oscillator, was chosen because it produced a sine wave as opposed to a square wave. It was found through characterization, that a square wave system clock for the ADS1210 and ADS1211 degraded CMR and PSR. Additionally, a square wave type signal increased the noise level enough to disallow 23-bit type performance.

10. Commonly Asked Questions - The A/D converter will occasionally go into a latch mode at power up. In this state, the A/D converter will draw excessive currents.

What is the problem and how do I solve it? - If the digital voltage exceeds the analog voltage by 0.3V an SCR on the chip will be enabled. Once this parasitic device is turned on, the only way to stop it from drawing exorbitant currents is to power the entire A/D converter down. This condition can be avoided by insuring that the analog power is greater than or equal to the digital power supply.

11. Commonly Asked Questions - What is the definition of “TTL Load” for this product? - There are several types of TTL logic with various fan-out specifications, however, the specification for these products are defined with the industry standard TTL load of 1.6mA. Therefore, 2 TTL loads would be equal to 3.2mA.