## SCD8522

Dual 16-Channel Analog Multiplexer Module Radiation Tolerant

# MUX8522

## Features

- 32-channels provided by four 16-channel multiplexers
- Radiation performance
  - Total dose: 300 krads(Si), Dose rate = 50 - 300 rads(Si)/s
  - SEU: Immune up to 120 MeV-cm$^2$/mg
  - SEL: Immune by process design
- Full military temperature range
- Low power consumption < 30mW
- Separate address ($A_0 \sim A_3$ & $B_0 \sim B_3$) and enable ($\overline{EN}$0-15 & $\overline{EN}$16-31) for CH0-15 and CH16-31
- Fast access time 1500ns typical
- Break-Before-Make switching
- High analog input impedance (power on or off)
- Designed for aerospace and high reliability space applications
- Packaging – Hermetic ceramic
  - 56 leads, 0.80"Sq x 0.20"Ht quad flat pack
  - Typical Weight 6 grams
- **CAES Radiation Hardness Assurance Plan is DLA Certified to MIL-PRF-38534, Appendix G.**

## General Description

CAES MUX8522 is a radiation tolerant, dual 16 channel multiplexer MCM (Multi Chip Module). The MUX8522 has been specifically designed to meet exposure to radiation environments. It is available in a 56 lead High Temperature Co-Fired Ceramic (HTCC) Quad Flatpack (CQFP). It is guaranteed operational from -55°C to +125°C. Available screened in accordance with MIL-PRF-38534, the MUX8522 is ideal for demanding military and space applications.



## Organization and Application

The MUX8522 consists of two independent 16 channel multiplexers arranged as shown in the block diagram.

## A Section

Sixteen (16) channels addressable by bus $A_0 \sim A_3$, enabled by $\overline{EN}$0-15 and outputted on Output1(0-15).
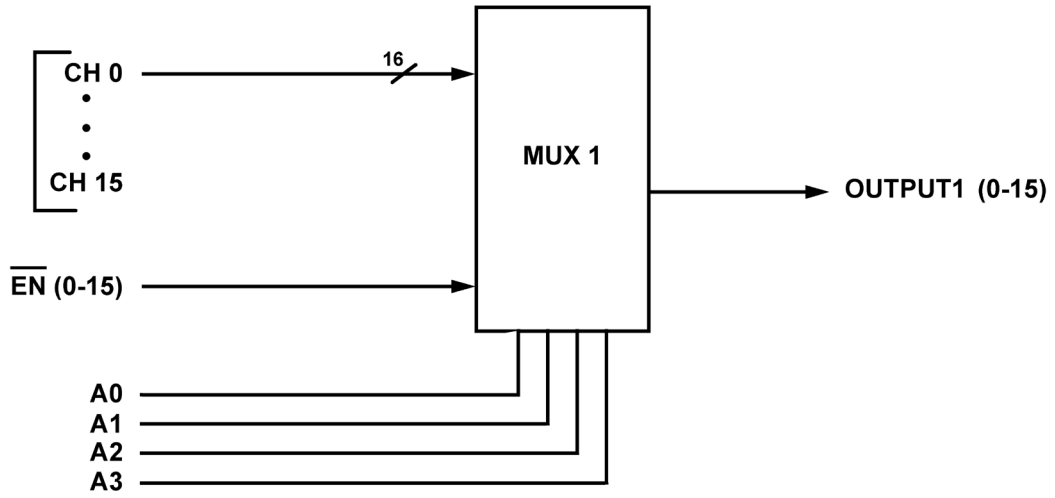
## B Section

Sixteen (16) channels addressable by bus $B_0 \sim B_3$, enabled by $\overline{EN}$16-31 and outputted on Output2(16-31).

**SECTION A**

CH 0
⋮
CH 15

16 / → MUX 1 → OUTPUT1 (0-15)

$\overline{EN}$ (0-15)

A0
A1
A2
A3

**SECTION B**

CH 16
⋮
CH 31

16 / → MUX 2 → OUTPUT2 (16-31)

$\overline{EN}$ (16-31)

B0
B1
B2
B3

+VEE

-VEE

VREF

GND

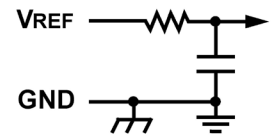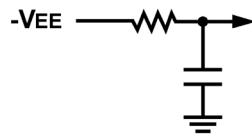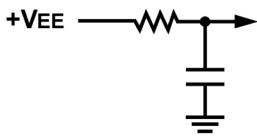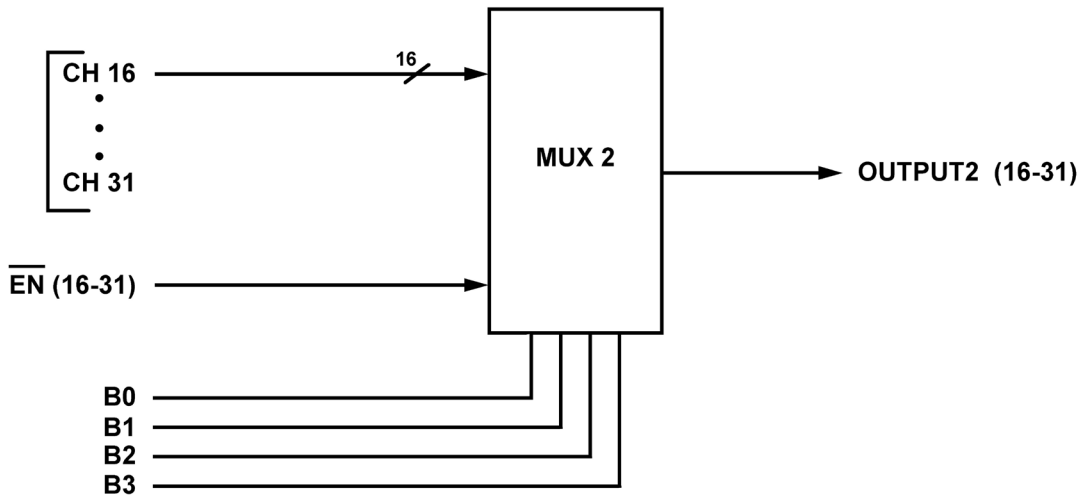MUX8522: Dual 16–Channel Analog Mux Block Diagram

## SCD8522
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### Absolute Maximum Ratings 1/

| Parameter | Range | Units |
|---|---|---|
| Case Operating Temperature Range | -55 to +125 | °C |
| Storage Temperature Range | -65 to +150 | °C |
| Supply Voltage<br>+$V_{EE}$ (Pin 18)<br>-$V_{EE}$ (Pin 46)<br>$V_{REF}$ (Pin 39) | +16.5<br>-16.5<br>+16.5 | V<br>V<br>V |
| Digital Input Overvoltage<br>$V_{EN}$0-15 (Pin 13), $V_{EN}$16-31 (Pin 44), $V_A$ (Pins 14, 15, 16, 17), $V_B$ (Pins 40, 41, 42, 43) | < $V_{REF}$ +4<br>> GND - 4 | V<br>V |
| Analog Input Over Voltage $V_{IN}$ | ±35 | V |

**Note:**

1) All measurements are made with respect to ground.

**Notice**: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may affect device reliability.

### Recommended Operating Conditions 1/

| Symbol | Parameter | Typical | Units |
|---|---|---|---|
| +$V_{EE}$ | +15V Power Supply Voltage | +15.0 | V |
| -$V_{EE}$ | -15V Power Supply Voltage | -15.0 | V |
| $V_{REF}$ | Reference Voltage | +5.00 | V |
| $V_{AL}$ | Logic Low Level | +0.8 | V |
| $V_{AH}$ | Logic High Level | +4.0 | V |

**Note:**

1) Power Supply turn-on sequence shall be as follows: +$V_{EE}$, -$V_{EE}$, followed by $V_{REF}$.

# MUX8522

## DC Electrical Performance Characteristics 1/

($T_C$ = -55°C TO +125°C, +$V_{EE}$ = +15V, -$V_{EE}$ = -15V, $V_{REF}$ = +5.0V, unless otherwise specified)

| Parameter | Symbol | Conditions | MIN | MAX | Units |
|---|---|---|---|---|---|
| Supply Current | +$I_{EE}$ | $V_{EN}$(0-15)=$V_{EN}$(16-31)=$V_A$(0-3)=$V_B$(0-3)=0 | 0.1 | 1 | mA |
| | -$I_{EE}$ | $V_{EN}$(0-15)=$V_{EN}$(16-31)=$V_A$(0-3)=$V_B$(0-3)=0 | -1 | -0.1 | mA |
| | +$I_{SBY}$ | $V_{EN}$(0-15)=$V_{EN}$(16-31)= 4V, $V_A$(0-3)=$V_B$(0-3)=0 6/ | 0.1 | 1 | mA |
| | -$I_{SBY}$ | $V_{EN}$(0-15)=$V_{EN}$(16-31)= 4V, $V_A$(0-3)=$V_B$(0-3)=0 6/ | -1 | -0.1 | mA |
| Address Input Current 7/ | $I_{AL}$(0-3)$_A$ | $V_A$ = 0V | -1 | 1 | µA |
| | $I_{AH}$(0-3)$_A$ | $V_A$ = 5V | -1 | 1 | µA |
| | $I_{AL}$(0-3)$_B$ | $V_B$ = 0V | -1 | 1 | µA |
| | $I_{AH}$(0-3)$_B$ | $V_B$ = 5V | -1 | 1 | µA |
| Enable Input Current 7/ | $I_{ENL}$(0-15) | $V_{EN}$(0-15) = 0V | -1 | 1 | µA |
| | $I_{ENH}$(0-15) | $V_{EN}$(0-15) = 5V | -1 | 1 | µA |
| | $I_{ENL}$(16-31) | $V_{EN}$(16-31) = 0V | -1 | 1 | µA |
| | $I_{ENH}$(16-31) | $V_{EN}$(16-31) = 5V | -1 | 1 | µA |
| Positive Input Leakage Current (CH0-CH31) | +$I_{SOFFOUTPUT(ALL)}$ | $V_{IN}$ = +10V, $V_{EN}$ = 4V, output and all unused MUX inputs under test = -10V 2/, 3/, 7/ | -100 | +100 | nA |
| Negative Input Leakage Current (CH0-CH31) | -$I_{SOFFOUTPUT(ALL)}$ | $V_{IN}$ = -10V, $V_{EN}$ = 4V, output and all unused MUX inputs under test = +10V 2/, 3/, 7/ | -100 | +100 | nA |
| Positive Output Leakage Current OUTPUTS (pins 12,45) | +$I_{DOFFOUTPUT(ALL)}$ | $V_{OUT}$ = +10V, $V_{EN}$ = 4V, output and all unused MUX inputs under test = -10V 3/, 4/, 7/ | -100 | +100 | nA |
| Negative Output Leakage Current OUTPUTS (pins 12,45) | -$I_{DOFFOUTPUT(ALL)}$ | $V_{OUT}$ = -10V, $V_{EN}$ = 4V, output and all unused MUX inputs under test = +10V 3/, 4/, 7/ | -100 | +100 | nA |
| Switch ON Resistance OUTPUTS (pins 12,45) | $R_{DS}$(ON)(0-31)$_A$ | $V_{IN}$ = +15V, $V_{EN}$ = 0.8V, $I_{OUT}$ = -1mA 2/, 3/, 5/ | 500 | 3000 | Ω |
| | $R_{DS}$(ON)(0-31)$_B$ | $V_{IN}$ = +5V, $V_{EN}$ = 0.8V, $I_{OUT}$ = -1mA 2/, 3/, 5/ | 500 | 3000 | Ω |
| | $R_{DS}$(ON)(0-31)$_C$ | $V_{IN}$ = -5V, $V_{EN}$ = 0.8V, $I_{OUT}$ = +1mA 2/, 3/, 5/ | 500 | 3000 | Ω |

**Notes:**

1) Measure inputs sequentially. Ground all unused inputs of the device under test. $V_A$ is the applied input voltage to the address lines A(0-3). $V_B$ is the applied input voltage to the address lines B(0-3).
2) $V_{IN}$ is the applied input voltage to the input channels (CH0-CH31)
3) $V_{EN}$ 0-15 is the applied input voltage to the enable lines $\overline{EN}$ (0-15), $V_{EN}$ 16-31 is the applied input voltage to the enable line $\overline{EN}$ (16-31)
4) $V_{OUT}$ is the applied input voltage to the output lines OUTPUT1(0-15), OUTPUT2(16-31)
5) Negative current is the current flowing out of each of the MUX pins. Positive current is the current flowing into each MUX pin.
6) Not tested, guaranteed to the specified limits.
7) These parameters for $T_C$ = -55°C are guaranteed by design, characterization, or correlation to other test parameters.

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## Switching Characteristics

($T_C$ = -55°C to +125°C, +$V_{EE}$ = +15V, -$V_{EE}$ = -15V, $V_{REF}$ = +5.0V -- Unless otherwise specified)

| Parameter | Symbol | Conditions | MIN | MAX | Units |
|---|---|---|---|---|---|
| Switching Test MUX | $t_A$HL | $R_L$ = 10KΩ, $C_L$ = 50pF | 10 | 1500 | ns |
| | $t_A$LH | $R_L$ = 10KΩ $C_L$ = 50pF<br>$T_C$ = +25°C, +125°C<br>Tc = -55°C | 10<br>10 | 2000<br>5000 | ns<br>ns |
| | $t_{ON}$EN | $R_L$ = 1KΩ, $C_L$ = 50pF | 10 | 1500 | ns |
| | $t_{OFF}$EN | | 10 | 1000 | ns |

## Truth Table (CH0 − CH15)

| A3 | A2 | A1 | A0 | $\overline{EN}$(0-15) | "ON" CHANNEL 1/ (OUTPUT 1) |
|---|---|---|---|---|---|
| X | X | X | X | H | NONE |
| L | L | L | L | L | CH0 |
| L | L | L | H | L | CH1 |
| L | L | H | L | L | CH2 |
| L | L | H | H | L | CH3 |
| L | H | L | L | L | CH4 |
| L | H | L | H | L | CH5 |
| L | H | H | L | L | CH6 |
| L | H | H | H | L | CH7 |
| H | L | L | L | L | CH8 |
| H | L | L | H | L | CH9 |
| H | L | H | L | L | CH10 |
| H | L | H | H | L | CH11 |
| H | H | L | L | L | CH12 |
| H | H | L | H | L | CH13 |
| H | H | H | L | L | CH14 |
| H | H | H | H | L | CH15 |

1/ Between (CH0-CH15) and OUTPUT1 (0-15)

## Truth Table (CH16 − CH31)

| B3 | B2 | B1 | B0 | $\overline{EN}$(16-31) | "ON" CHANNEL 1/ (OUTPUT 2) |
|---|---|---|---|---|---|
| X | X | X | X | H | NONE |
| L | L | L | L | L | CH16 |
| L | L | L | H | L | CH17 |
| L | L | H | L | L | CH18 |
| L | L | H | H | L | CH19 |
| L | H | L | L | L | CH20 |
| L | H | L | H | L | CH21 |
| L | H | H | L | L | CH22 |
| L | H | H | H | L | CH23 |
| H | L | L | L | L | CH24 |
| H | L | L | H | L | CH25 |
| H | L | H | L | L | CH26 |
| H | L | H | H | L | CH27 |
| H | H | L | L | L | CH28 |
| H | H | L | H | L | CH29 |
| H | H | H | L | L | CH30 |
| H | H | H | H | L | CH31 |

1/Between (CH16-CH31) and OUTPUT 2 (16-31)

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**Address Lines**
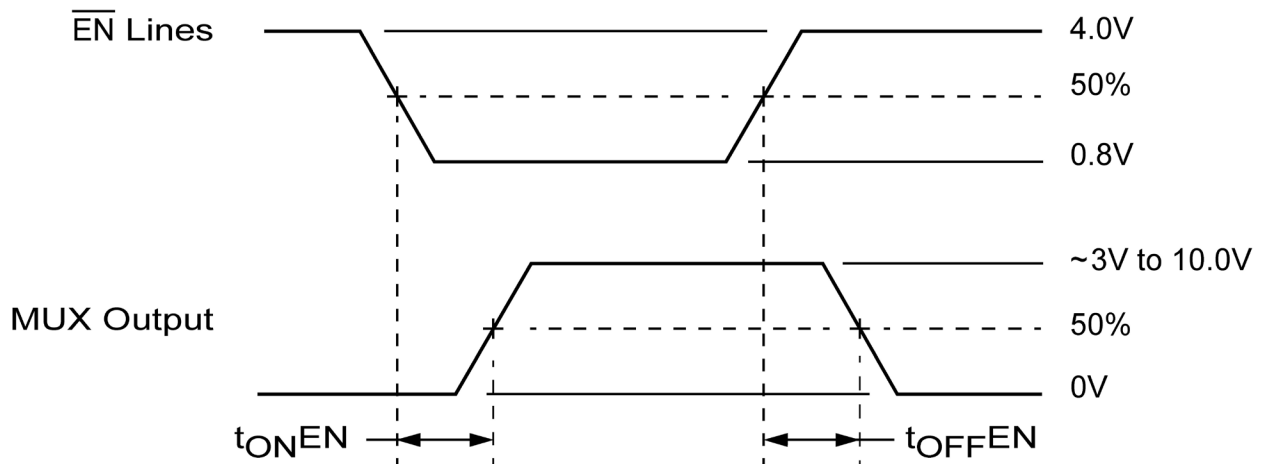(A0 - A3 / B0 - B3)

— 4.0V
— 50%
— 0.8V

**MUX Output**

— 11.6V MIN
— 50%
— 0V

$t_{A}HL$

Definition of $t_{A}HL$

**Address Lines**
(A0 - A3 / B0 - B3)

— 4.0V
— 50%
— 0.8V

**MUX Output**

— 11.6V MIN
— 50%
— 0V

$t_{A}LH$

Definition of $t_{A}LH$

**$\overline{EN}$ Lines**

— 4.0V
— 50%
— 0.8V

**MUX Output**

— ~3V to 10.0V
— 50%
— 0V
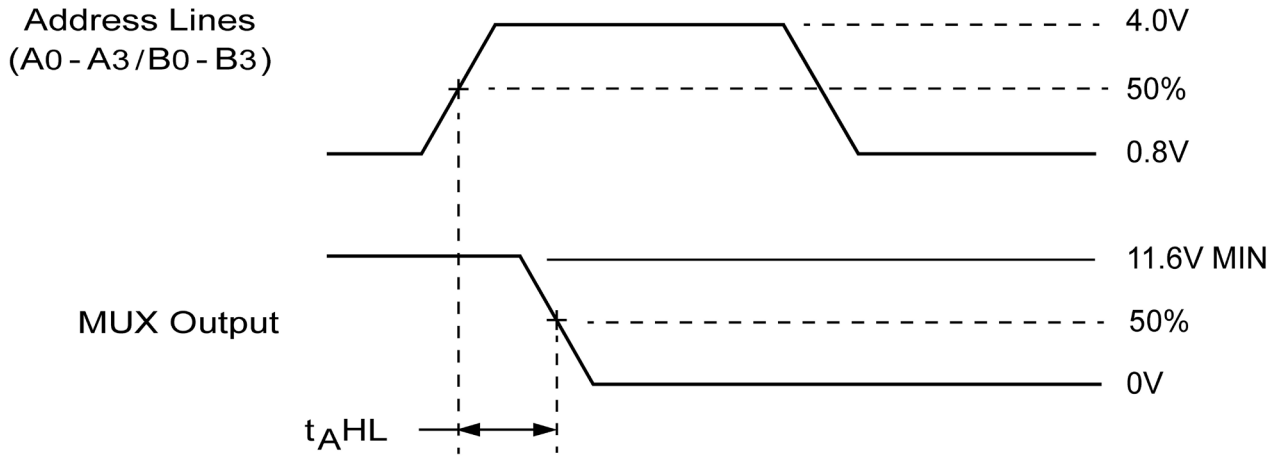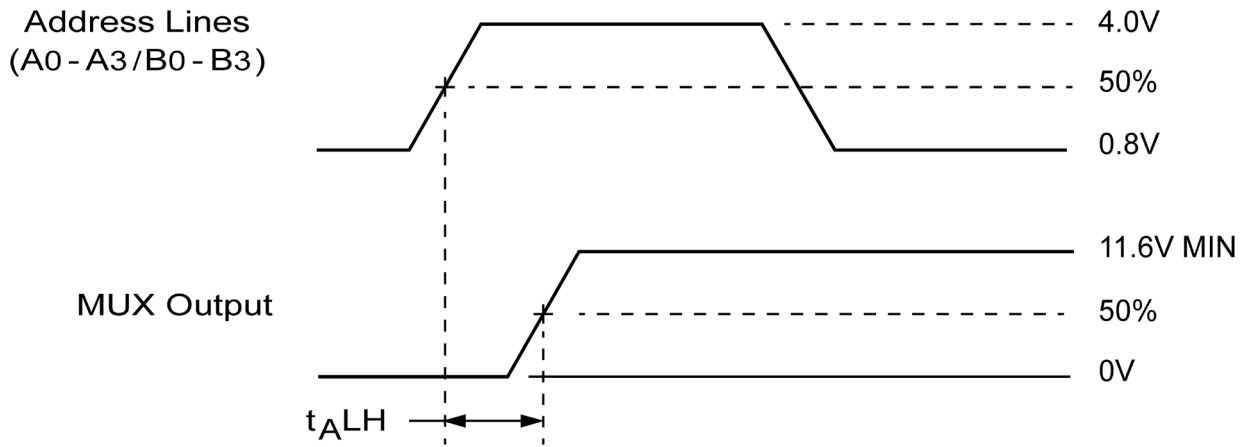
$t_{ON}EN$       $t_{OFF}EN$

Definition of $t_{ON}EN$ and $t_{OFF}EN$
MUX8522 Switching Diagrams

**Note:** f = 10KHz, Duty cycle = 50%.

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## Pin Numbers & Functions

| MUX8522 – 56 Leads Ceramic QUAD Flat Pack | | | |
|---|---|---|---|
| Pin # | Function | Pin # | Function |
| 1 | CH0 | 29 | CH31 |
| 2 | CH1 | 30 | CH30 |
| 3 | CH2 | 31 | CH29 |
| 4 | CH3 | 32 | CH28 |
| 5 | CH4 | 33 | CH27 |
| 6 | CH5 | 34 | CH26 |
| 7 | GND | 35 | GND |
| 8 | GND | 36 | GND |
| 9 | CH6 | 37 | CH25 |
| 10 | CH7 | 38 | CH24 |
| 11 | CASE GND | 39 | $V_{REF}$ |
| 12 | OUTPUT1 (0-15) | 40 | B3 |
| 13 | $\overline{EN}$ (0-15) | 41 | B2 |
| 14 | A0 | 42 | B1 |
| 15 | A1 | 43 | B0 |
| 16 | A2 | 44 | $\overline{EN}$ (16-31) |
| 17 | A3 | 45 | OUTPUT2 (16-31) |
| 18 | $+V_{EE}$ | 46 | $-V_{EE}$ |
| 19 | CH15 | 47 | CH16 |
| 20 | CH14 | 48 | CH17 |
| 21 | GND | 49 | GND |
| 22 | GND | 50 | GND |
| 23 | CH13 | 51 | CH18 |
| 24 | CH12 | 52 | CH19 |
| 25 | CH11 | 53 | CH20 |
| 26 | CH10 | 54 | CH21 |
| 27 | CH9 | 55 | CH22 |
| 28 | CH8 | 56 | CH23 |

**Notes:**

1) It is recommended that all "NC or "no connect pin" be grounded. This eliminates or minimizes any ESD or static buildup.

2) Package lid is internally connected to circuit ground (Pins 7, 8, 11, 21, 22, 35, 36, 49, 50)

## SCD8522
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## Ordering Information

| Model | DLA SMD # | Screening | Package |
|---|---|---|---|
| MUX8522- 7 | - | Commercial Flow, +25°C testing only | |
| MUX8522-S | - | Military Temperature, -55°C to +125°C Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications | QUAD Flat Pack |
| MUX8522- 201-1S | 5962-0923101KXC | In accordance with DLA SMD | |
| MUX8522- 901-1S | 5962F0923101KXC | In accordance with DLA Certified RHA Program Plan to RHA Level "F", 300krad(Si) | |

## Package Outline
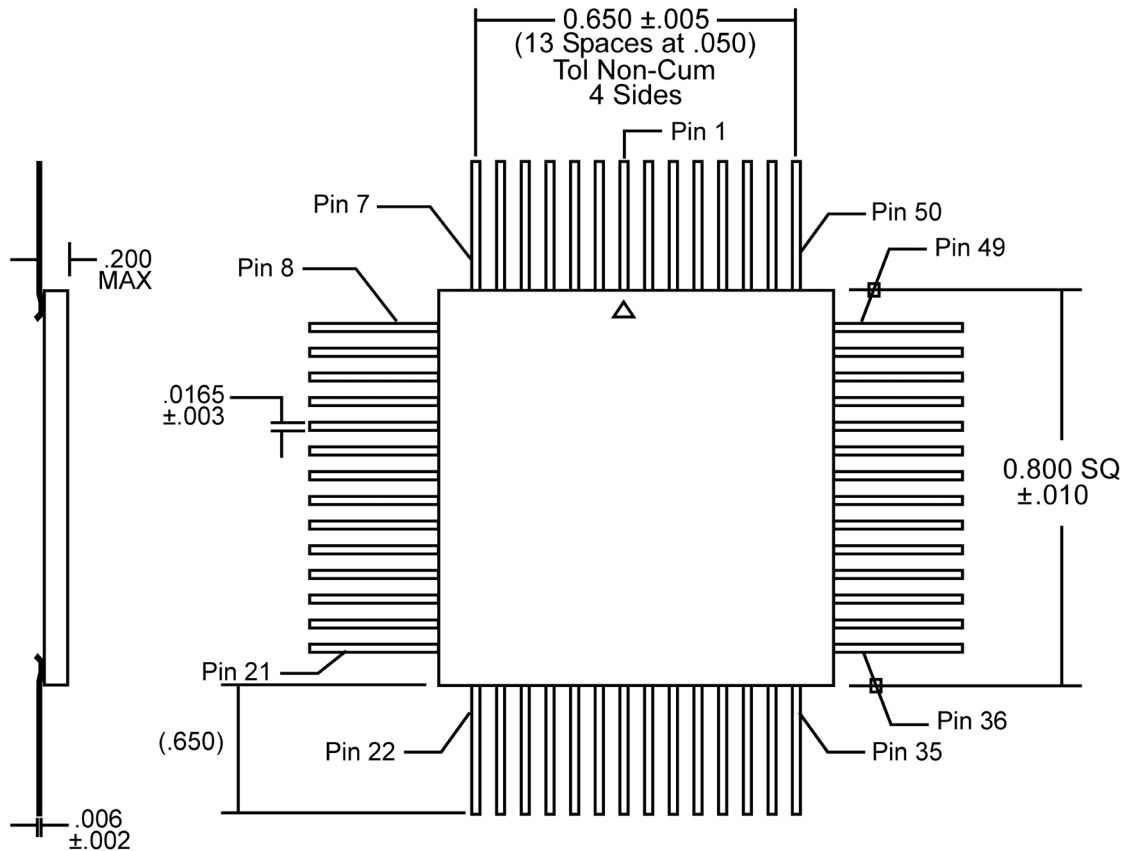


**Note:**

1) Outside ceramic tie bars not shown for clarity. Contact factory for details.

## REVISION HISTORY

| Date | Rev. # | Change Description | Initials |
|---|---|---|---|
| 6/24/11 | B | REVISED PER ECN 8522-3 | KM |
| 9/30/13 | C | REVISED PER ECN 8522-5 | KM |
| 3/4/21 | D | REVISED PER ECN 23534 | |
| | | | |

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## Datasheet Definitions

| | DEFINITION |
|---|---|
| Advanced Datasheet | CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**. |
| Preliminary Datasheet | CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available. |
| Datasheet | Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes. |

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