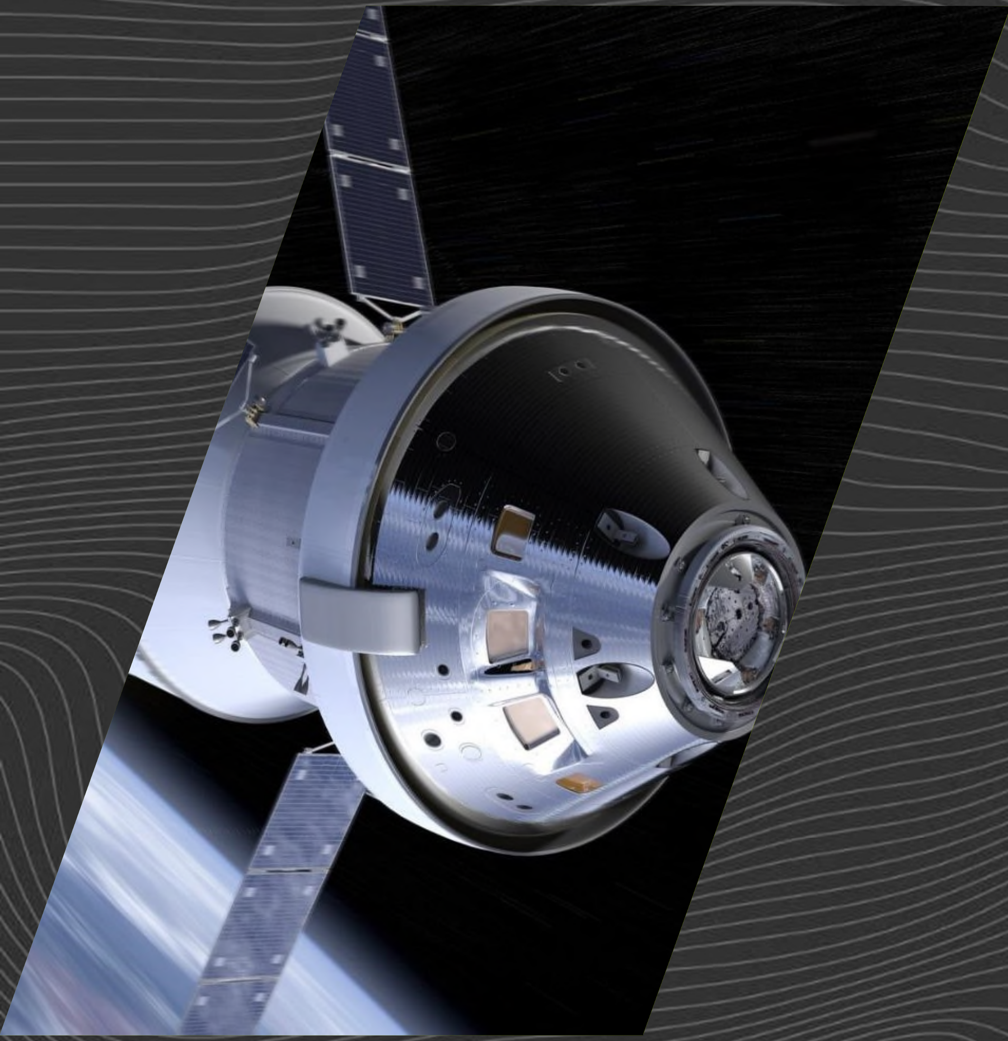
GR740 Ecosystem Design Examples



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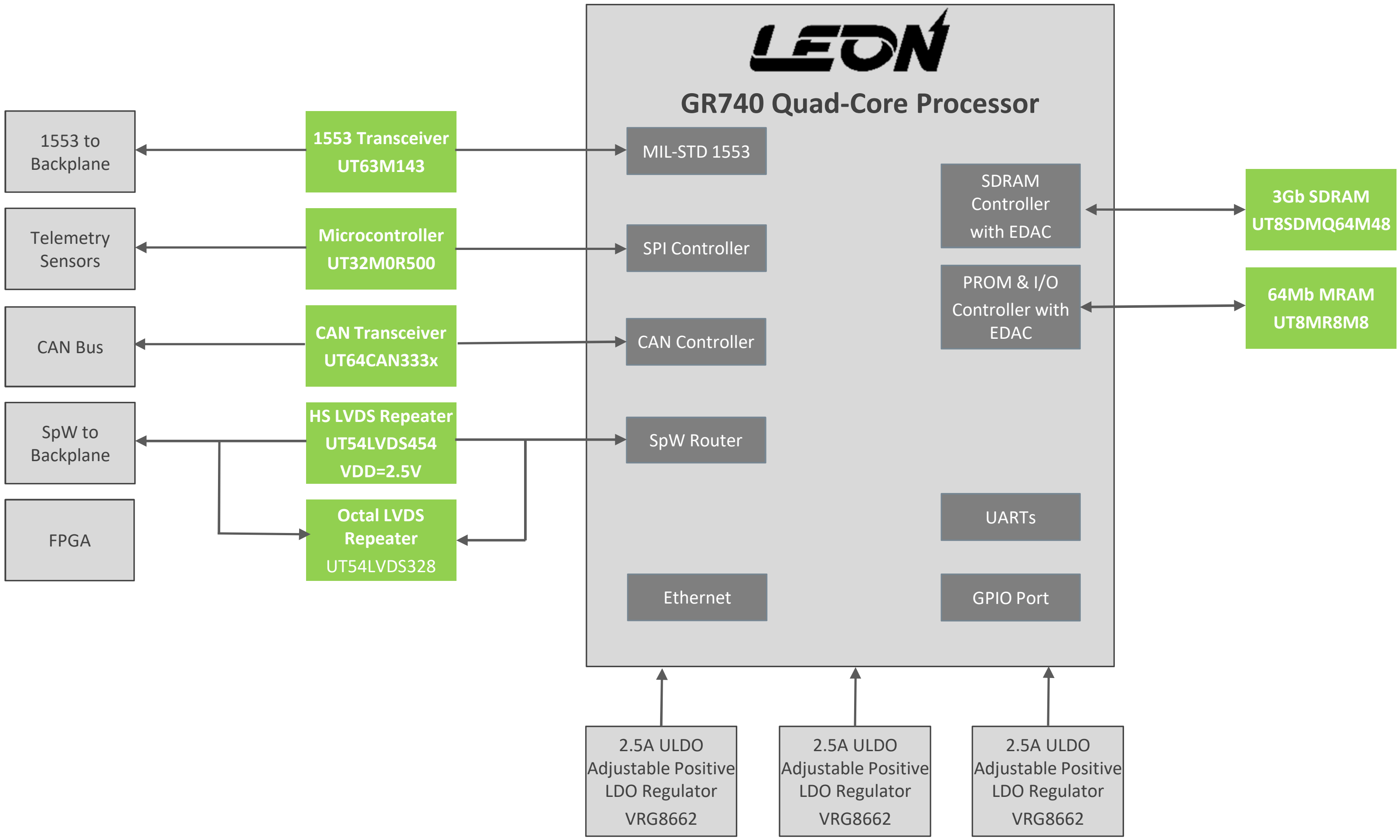
CAES Ecosystem Top Level Diagram



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CAES GR740 Ecosystem – GR740

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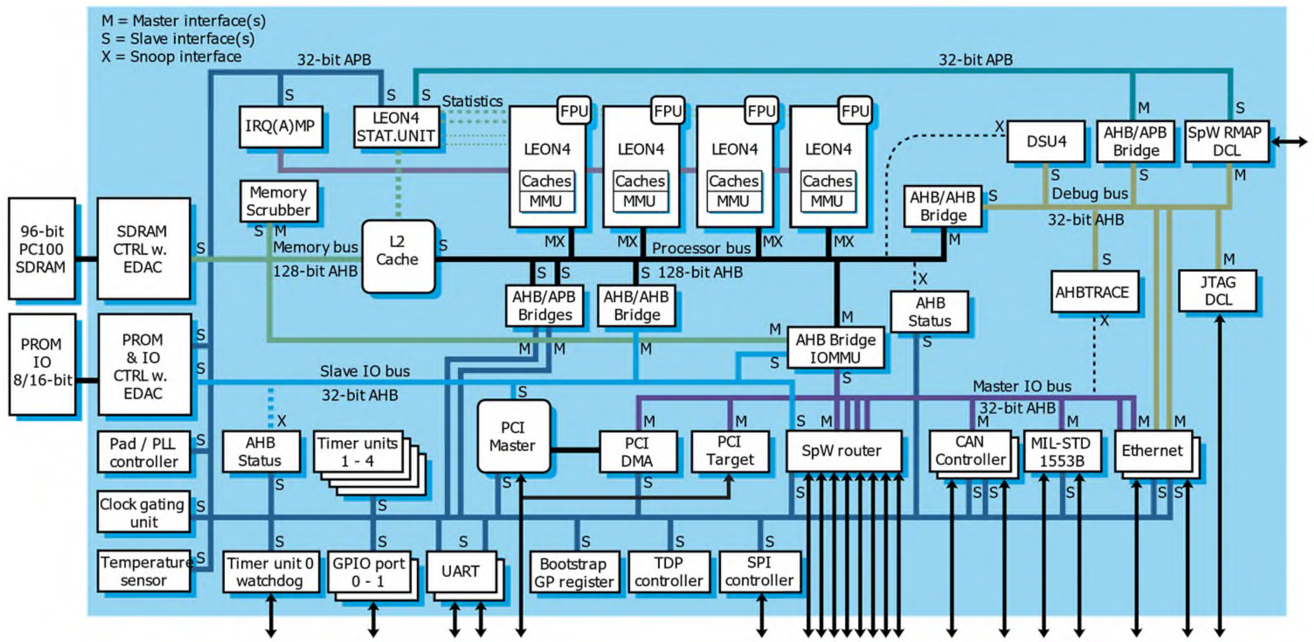
GR740 Quad-Core LEON4FT Processor

CAES PIONEERING ADVANCED ELECTRONICS

Features

- Fault-tolerant quad-processor SPARC V8 integer unit with 7-stage pipeline, 8 register windows, 4x4 KiB instruction and 4x4 KiB data caches.
- Double-precision IEEE-754 FPU (1 FPU/Core)
- 250 MHz
- >1700 DMIPS
- Power consumption < 2W
- 2 MiB Level-2 cache
- 64-bit PC100 SDRAM memory interface with Reed-Solomon EDAC
- 8/16-bit PROM/IO interface with EDAC
- CPU and I/O memory management units
- Multi-processor interrupt controller with support for asymmetric and symmetric multiprocessing
- SpaceWire TDP controller and support for time synchronisation



Interfaces

- SpaceWire router with 8 SpaceWire links (200 MHz)
- 2x 10/100/1000 Mbit Ethernet interfaces
- 2x MIL-STD-1553B interface
- 2x CAN 2.0 controller interface
- 2x UART, SPI, timers and watchdog, 16+22 pin GPIO
- PCI Initiator / target interface
- JTAG

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CAES GR740 Ecosystem – 1553 Transceiver

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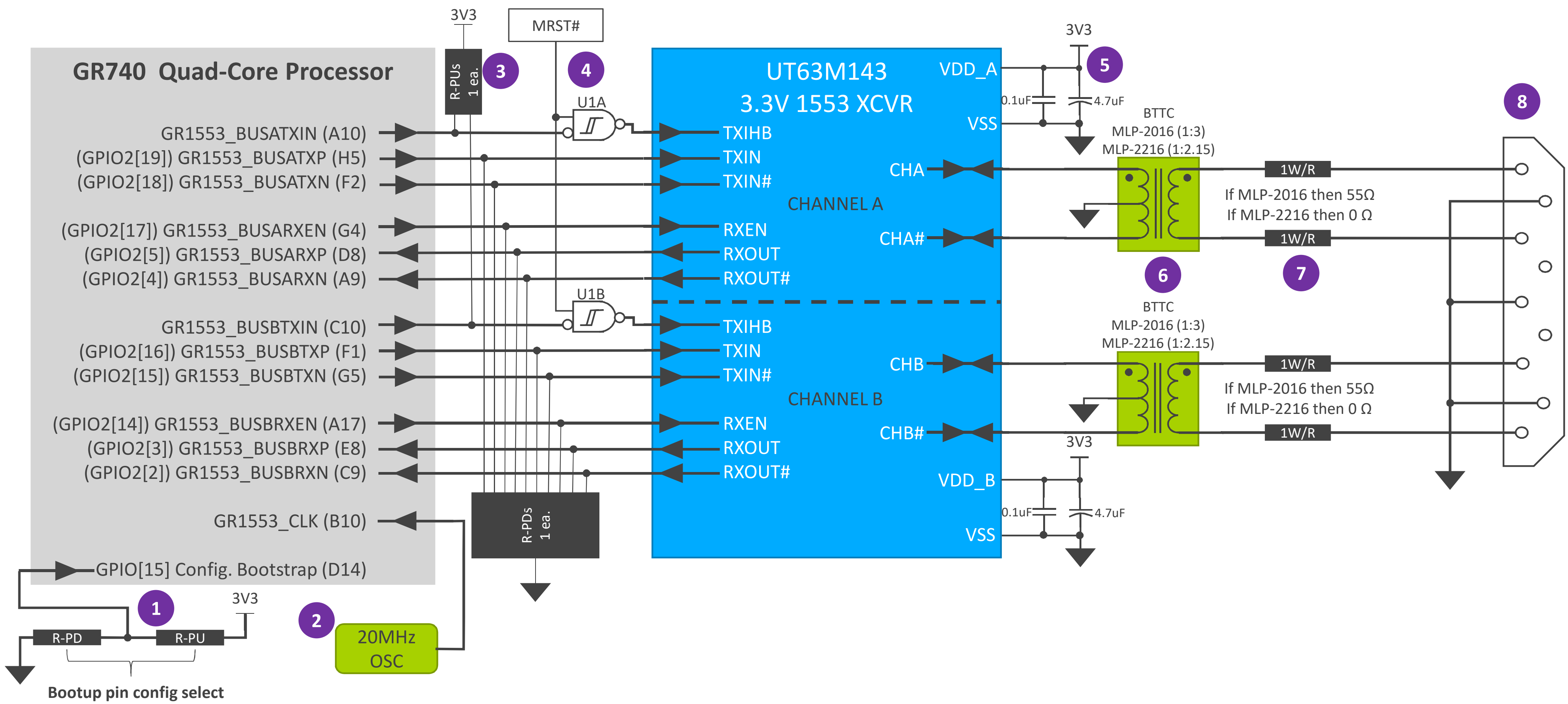
GR740 MIL-STD-1553 Interface



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GR740 MIL-STD-1553 Interface

Notes

1. The GR740 uses an alternate I/O muxing selection between PROMIO and selected peripheral functions such as MIL-STD-1553, UART0&1, CAN0&1, and SpW. The reset configuration of these pins can be defined by the state of GPIO[15] when exiting reset. For hardware defined activation of the peripherals, GPIO[15] shall be pulled high during reset. Else, holding GPIO[15] low during reset will start the GR740 with full PROMIO features enabled. In the latter configuration, software can enable the desired alternate functions that share the GPIO2[xx] PROMIO pins, such as MIL-STD-1553
   - To accommodate a wide range of start-up sequences without disrupting the MIL-STD-1553 databus, the GR740 provides dedicated pins for the GR1553_CLK and the transmitter inhibit outputs (GR1553_BUSA/BTXIN)
2. The GR1553 core requires a 20MHz clock. The GR740 provides a dedicated 20MHz GR1553_CLK input on pin B10
3. All the I/O between the GR740 and the UT63M143 should have pull-up or pull-down bias resistors to place the 1553 signals in their inactive states during power-up and until the GR740 is able to take control of the I/O
4. To ensure your interface does not inadvertently transmit a signal onto the 1553 databus during the power-up phase, we recommend gating the Master Reset signal with the transmitter inhibit from the GR740. In the design example provided, the logic function is shown as U1A and U1B. This device is recommended to be the UT54ACS3G99S, which is the CAES Many Gate configurable logic device. It is a 20-lead flatpack proving 3 independent, pin configurable, logic functions. The function depicted in the design example can be implemented with the UT54ACS3G99S.
5. While transmitting, the UT63M143 transmitter can draw up to 1Amp/100ns, so stiff decoupling at the transceiver is recommended with a minimum of 100nF and 4.7uF decoupling per VDD pin on the device. The UT63M143 has two physically isolated transceivers with independent VDD domains to support BUS A and BUS B isolation
6. CAES recommends the BTTC 3.3V transformer, or alternatively the Pulse Signal GL1553-70. Considering the BTTC product for direct coupled configurations, the MLP-2016 with 1:3 turns ratio is recommended, while the MLP-2216 serves transformer-coupled applications with the 1:2.15 turns ratio. Both part numbers use the exact same footprint, which would support configuration changes through PCB assembly selections. The Pulse GL1553-70 product uses a different footprint than BTTC, but provide a single transformer with windings for both coupling methods.
7. When using a direct-coupled bus interface, series 55-ohm / 1W resistors are required between the transformer secondary terminals and the bus connector. To support assembly configuration changes when implementing a transformer coupled interface, the 55-ohm resistors would be replaced with 0-ohm resistors
8. Generally, the program will dictate the off-board interface and connector requirements. Often times CAES sees DB9 or TRIAC BNC COAX connectors used for the MIL-STD-1553 bus connection. In this design example, the DB9 based configuration is proposed

GR740 MIL-STD-1553 Interface
Proposed BoM

Description	QTY	Part Number	Mfg.
GR740 Processor	1	GR740-CP-CG625 (Prototype) GR740-MSV-CG625 (QML-V equiv. Flight)	CAES
Many Gate Logic	1	UT54ACS3G99S-XPC (Prototype) 5962R1523801VXA (QML-V, 100Krad)	CAES
MIL-STD-1553 3V Transceiver	1	UT63M143-DPC (Prototype) 5962R0724201VZC (QML-V, 100Krad)	CAES
MIL-STD-1553 3V Transformer Short Stub (1:3 Turns Ratio)	2	MLP-2016 – Non QPL (SCD Required) SMQ1553-70 – Non QPL (SCD Required)	BTTC (DDC) Pulse Rugged
MIL-STD-1553 3V Transformer Long Stub (1:2.15 Turns Ratio)	2	MLP-2216 – Non QPL (SCD Required) SMQ1553-70 – Non QPL (SCD Required)	BTTC (DDC) Pulse Rugged
55-ohm/ 1 Watt MIL-STD-1553 Direct-Coupled Fault Resistor	4	RWR81NN55R0FS (MIL-PRF-39007)	Vishay Dale
33K-ohm, 1%, 0603, Bias Resistors	13	M55342M12B33E0V (MIL-PRF-55342)	Vishay Dale
0.1uF, 10%, 1210, BX Ceramic Decoupling Cap	2	M123A11BXB104KS (MIL-PRF-123/11)	
4.7uF, 10%, F-Case, Tantalum Decoupling Cap	2	CWR06FC475KDC (MIL-PRF-55364/4)	Vishay Dale
Micro DB9 Connector or MIL-STD-D38999 Type	1	Program ICD Driven	As Required

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GR740 Ecosystem – Arm Microcontroller

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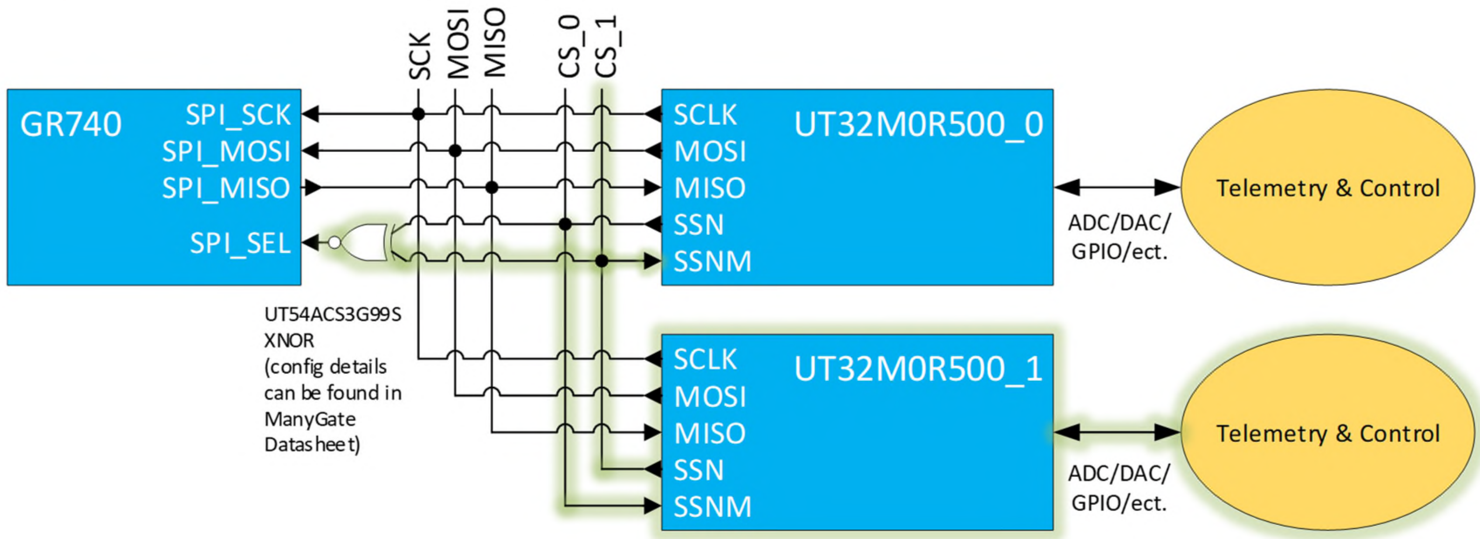
GR740 – UT32M0R500 SPI and UART Interfaces



SPI Interface

(See next slide ref green highlighted components)

UART Interface

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GR740 – UT32M0R500 SPI and UART Interface
Notes

SPI Interface

- Intended application is to "stream" telemetry and other data from the UT32M0R500s to the GR740, with the GR740 sending minimal information back to the UT32M0R500s
- The UT32M0R500s are operating as "SPI Masters", and the GR740 is operating as a "SPI Slave"
  - The XNOR gate and SSNM inputs ensure only one SPI Master is transmitting information on the bus at a given time
    - The XNOR gate is created by the UT54ACS3GSS9, a CAES ManyGate logic device. Configuration information can be found in that part's datasheet
      - Additionally, users would have an additional two logic gates available for other components near the GR740 (AND, OR, NAND, NOR, etc.)
- If a user only wants to implement a single UT32M0R500, the components and connections highlighted green can be removed (the CS_0 line would directly connect to SPI_SEL)

UART Interface

- Intended application is for transmitting control and telemetry data equally from the UT32M0R500 to the GR740 and vice versa
- The UART interface is straightforward, the TX pins go to RX pins, and vice versa. Depending on cable length users may need to look into termination options
- The UART1 pins of the UT32M0R500 were selected to ensure users still have access to the UART0 pins for bootloading and firmware update purposes

CAN Interface (not shown)

- Intended application is both devices are part of a CAN 2.0B Bus, listening and transmitting control and telemetry data
- Use the UT54CAN333x to interface with the CAN bus, as shown in later slides

GR740 Ecosystem – CAN Transceiver

These are not reference designs. They are conceptual approaches for guidance purposes only.

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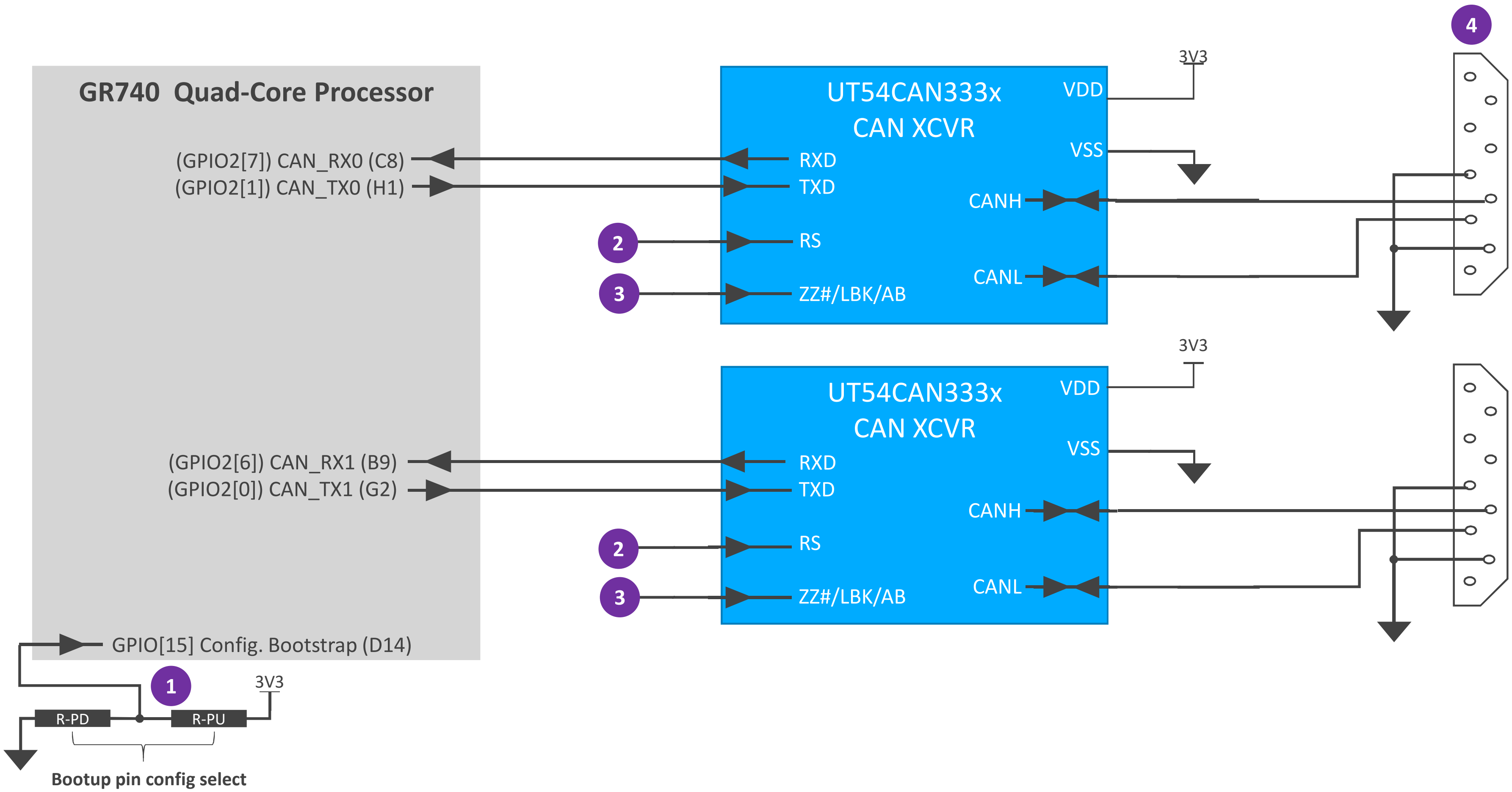

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GR740 CAN Transceiver Interface

Notes

1. The GR740 uses an alternate I/O muxing selection between PROMIO and selected peripheral functions such as MIL-STD-1553, UART0&1, CAN0&1, and SpW. The reset configuration of these pins can be defined by the state of GPIO[15] when exiting reset. For hardware defined activation of the peripherals, GPIO[15] shall be pulled high during reset. Else, holding GPIO[15] low during reset will start the GR740 with full PROMIO features enabled. In the latter configuration, software can enable the desired alternate functions that share the GPIO2[xx] PROMIO pins, such as CAN Transceiver Interface
2. The RS pin on the UT64CAN333x series CAN transceivers provides three functional modes of operation:
   - High-speed: The high-speed mode of operation is not compatible with the GR740 CAN 2.0 interface.
   - Slope control: The rise and fall slopes are adjusted by connecting a resistor to ground at RS (pin 8). The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor value between 10 kΩ to 100 kΩ, where these resistor values control the slew rates between ~2.0 V/µs to ~20 V/µs, respectively
   - Low-power standby mode: If RS is set to a high-level input (> 0.75*VDD), the transceiver enters a low current, listen only mode of operation. In this mode, the CAN bus driver is disabled and the receiver remains active. The CAN controller has ability to disable low-power standby mode once bus activity resumes
3. Along with the common functionality described, the UT64CAN333x family of transceivers includes three members, each with a unique mode of operation.
   - The UT64CAN3330, Figure 1, provides the option to place the transceiver into a low power sleep mode to conserve power when CAN activity is suspended. Sleep mode disables the driver and receiver circuit when the ZZ pin is biased ≤ VIL. The part resumes operations when the ZZ pin is biased ≥ VIH.
   - The UT64CAN3331, Figure 2, provides the option to isolate the transceiver bus connections to permit local node diagnostics, without interrupting operations on the bus. Diagnostic Loopback mode is enabled when the LBK pin is biased ≥ VIH. Diagnostic Loopback mode is disabled when the LBK pin is biased ≤ VIL. In the Diagnostic Loopback mode, the CANH/CANL output is placed in the recessive mode. Also, the connection between TXD and RXD is made through the mode logic and connection and the connections for TXD and RXD are isolated from CANH/CANL.
   - The UT64CAN3332, Figure 3, provides the option to automatically synchronize the baud rate of the transceiver by matching the bit timing to the traffic on the bus. The Auto Baud Loopback mode is enabled when the AB pin is biased ≥ VIH. Auto Baud Loopback mode is disabled when the AB pin is biased ≤ VIL. In the Auto-Baud mode, the CANH/CANL output is placed in the recessive mode.
4. Program will dictate the off-board interface and connector requirements. DB9 based configuration is proposed.

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GR740 Ecosystem –
- UT54LVDS454 1.25 Gbps Quad LVDS Repeater
- UT54LVDS328 400 Mbps Octal LVDS Repeater

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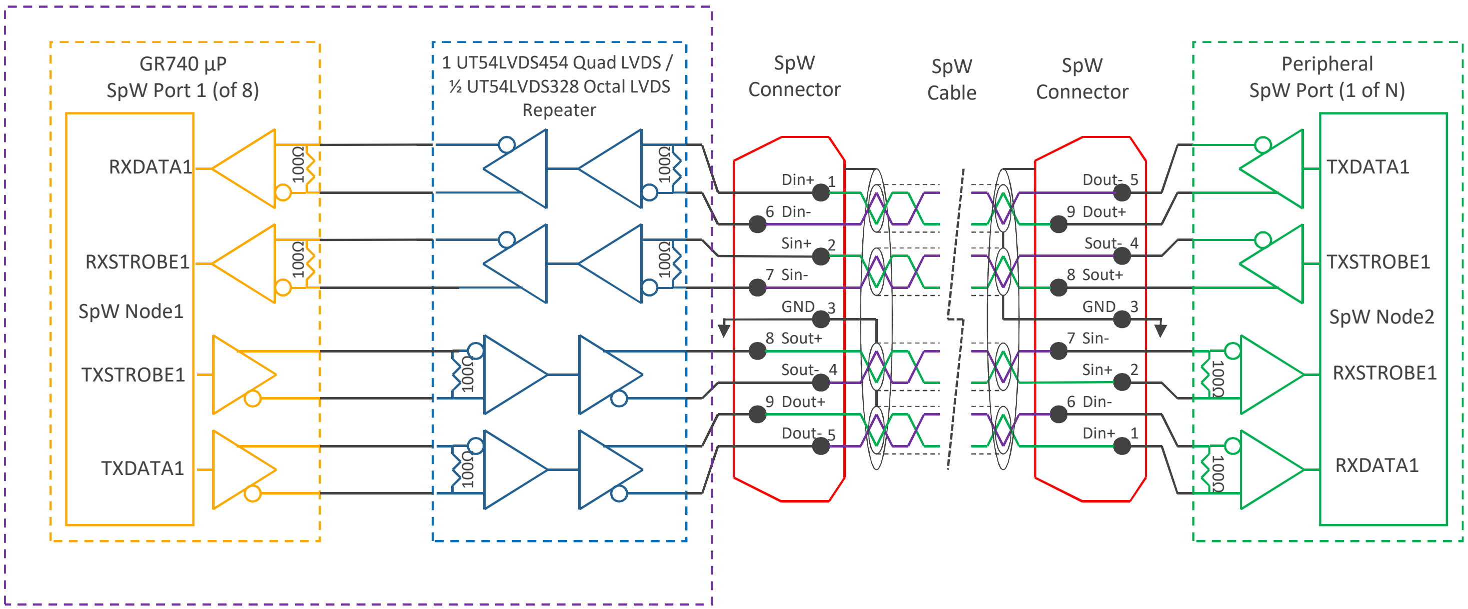
GR740 SpW/LVDS Repeater: x1 SpW Port



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GR740 SpW/LVDS Repeater
Notes

CAES UT54LVDS328 Octal 400 Mbps LVDS Repeater Device Features

- Data rates up to 400.0 Mbps per channel / 200 MHz clock channel
- 3.3V power supply
- 3.5mA LVDS TX output drive current
- Extends SpW channel reach
- x1 UT54LVDS328 octal LVDS repeater supports x2 SpW ports
- Cold sparing all pins
- 48-lead CFP package
- Total integrated dose (TID): 1Mrad(Si)

CAES UT54LVDS454 1.25 Gbps Dual, Full-Duplex / Quad, Simplex LVDS Repeater Device Features

- Data rates up to 1.25 Gbps per channel / protocol independent
- 2.5V power supply
- Selectable 3.5mA or 7.0mA TX output drive currents
- Extends SpW channel reach
- x1 UT54LVDS454 quad LVDS repeater supports x1 SpW port
- Cold sparing all pins
- 71-land C-CGA/C-LGA package
- Total integrated dose (TID): 100krad(Si)

GR740 to LVDS Repeater Design Considerations

- GR740 includes SpW router with x8 ports
- Single SpW port: One full-duplex LVDS lane (Lane = RX Ch. + TX Ch.): x1 lane for data and x1 lane for strobe
- Use UT54LVDS328 / UT54LVDS454 LVDS repeaters to extend SpW port link reach

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GR740 Ecosystem – Volatile Memory

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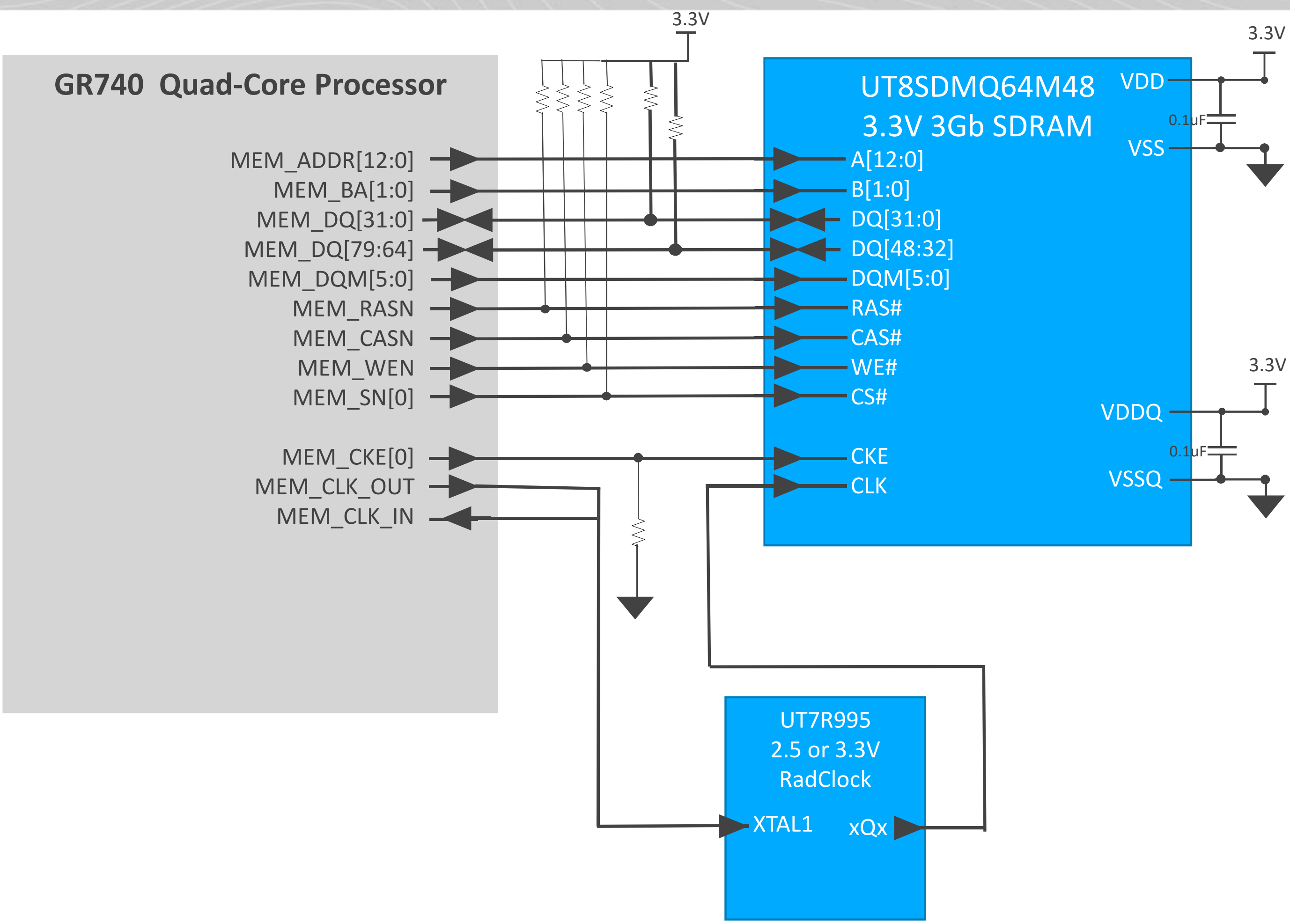
GR740 SDRAM w/EDAC Interface



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GR740 SDRAM w/EDAC Interface

Notes

CAES 3Gb SDRAM Device Features

- The CAES UT8SDMQ64M48 is one of the only QML qualified SDRAM or DRAM processor memory available.
- 3Gb organized as 64M x 48 (16M x 48 x 4 banks),
- Single 3.3V source device operates across -40°C to +105°C at a maximum frequency of 100MHz.
- Fully synchronized, all signals are registered on the positive edge of system clock.
- The 3Gb device is available in a 128-pin hermetic flatpack.
- The CAES SDRAM has been qualified to the following radiation operational environment:
  - Total Dose ≥ 100 krad (Si)
  - SEL immune to 111MeV-cm2/mg
  - SEU event rate of 1.3E-10 events/bit-day assuming geo orbit and Adam's 90% worst-case environment.

GR740 to SDRAM Design Considerations

- While the device is tested at 100MHz across temperature and voltage, a lot depends on board design to reach optimized level of operation.
  - The RadClock (or similar clock buffer) is recommended to optimize for clock rate above 50MHz especially if multiple devices are bussed.
    - Not all clock buffer connections shown for optimization (block diagram for reference only)
  - To insure that SDRAM timing is maintained, the clock and control signals traces should be matched.
  - All data and address signal traces should be matched.
  - Series resistors should be used on all SDRAM signals and placed as close to controlling output pins as possible.
  - Pull up/downs should be used on control signals to inactive state to avoid indeterminate states during power up and reset.
  - SDRAM address and data I/Os should be pulled to a known state to avoid floating inputs.
  - Decoupling capacitors should be placed as close as possible between each power and ground pin pair of the SDRAM.
- Bootstrap signal MEM_IFWIDTH is set high for 32 data bits and 16 check bits
  - Reference GR740 Data Sheet and User's Manual for other clocking, EDAC, and SDRAM operating options at https://www.gaisler.com/index.php/products/components/gr740

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GR740 Ecosystem – Non-Volatile Memory

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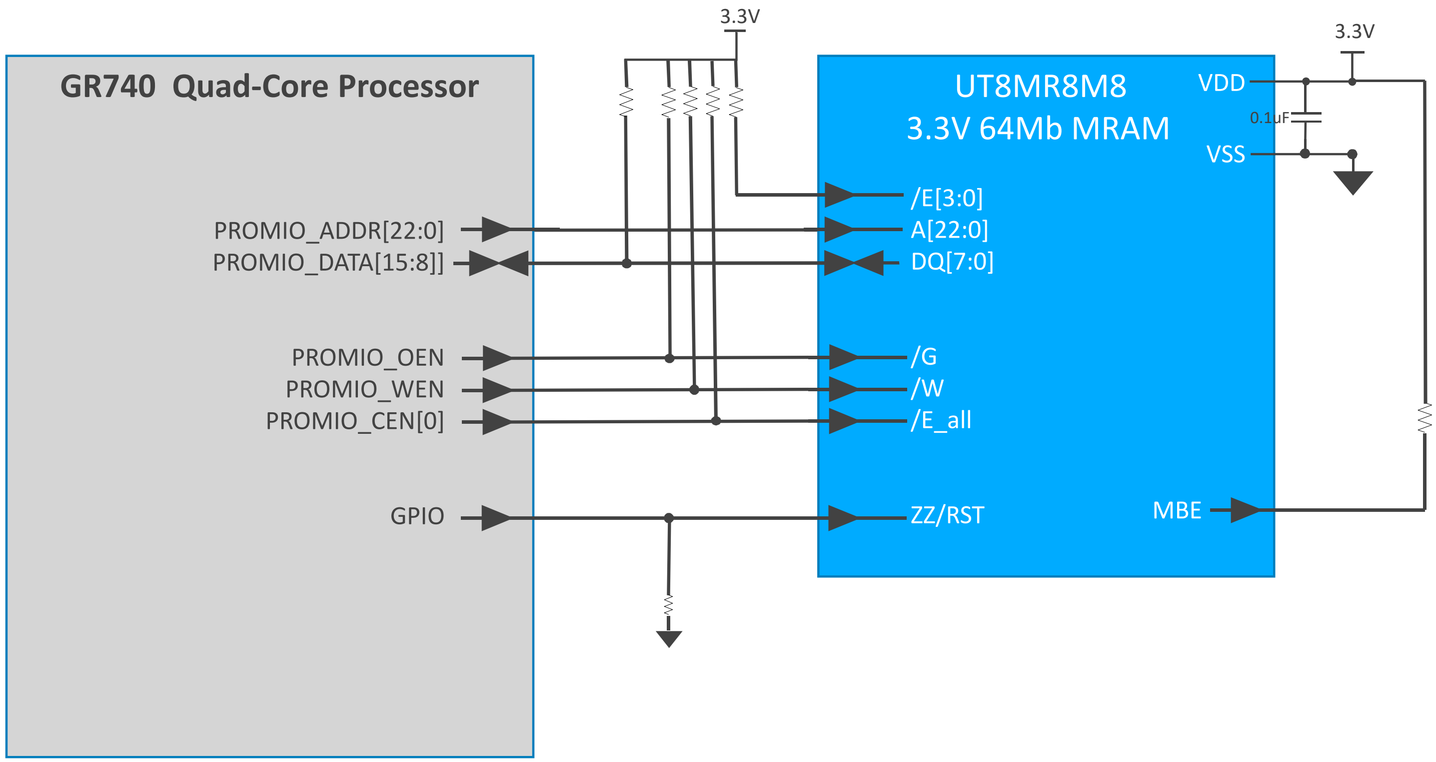
GR740 Non-Volatile MRAM w/EDAC Interface



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GR740 Non-Volatile MRAMw/EDAC Interface
Notes

64Mb MRAM Device Features

- The CAES UT8MR8M8 is one of few QML V qualified non-volatile memory available.
- The CAES MRAM provides unlimited 20 year read/write endurance and data retention (-40°C to +105°C)
- The CAES 64Mb MRAM uses a simplistic asynchronous parallel bus operation compatible with typical SRAM interfaces
- The CAES MRAM provides unique equally fast random write/read cycle access in a non-volatile memory.
- The CAES MRAM provides one of the highest TID hardness in a non-volatile memory
- The CAES MRAM provided unparalleled radiation performance for a on-volatile memory
    - Total Dose > 1 Mrad (Si)
    - SEL immune to 112MeV-cm2/mg @125°C
    - SEU immune memory cell to 112MeV-cm2/mg @125°C.

GR740 to MRAM Design Consideration

- Reference CAES application note for MRAMs
    - MRAM is sensitive to magnetic field exposure at the device surface, reference CAES Application Note AN-MEM-003, Magnetic Immunity of the MRAM Device
    - MRAM susceptible to once a mission possibility of SEFI, reference CAES Application note AN-MEM-004, SEFI work-Arounds for MRAM Device.
    - Additional information can be found on the MRAM FAQ
- The MRAM has two device enable schemes for design flexibility, reference the UT8MR8M8 for details.
- The MRAM MBE output is an open drain and requires an external pullup however the GR470 PROMIO EDAC has it own error scheme.
- Decoupling capacitors should be placed as close as possible between each power and ground pair of the MRAM.
- GR740 bootstrap signals GPIO[10] is 0 for x8 bit bus, GPIO[14] is 1 to enable EDAC after reset, GPIO[15] is 0 to select PROMIO interface after reset.
    - Reference GR740 Data Sheet and User's Manual for other PROMIO configuration and register setting at https://www.gaisler.com/index.php/products/components/gr7

GR740 Ecosystem – DC/DC Power Supply

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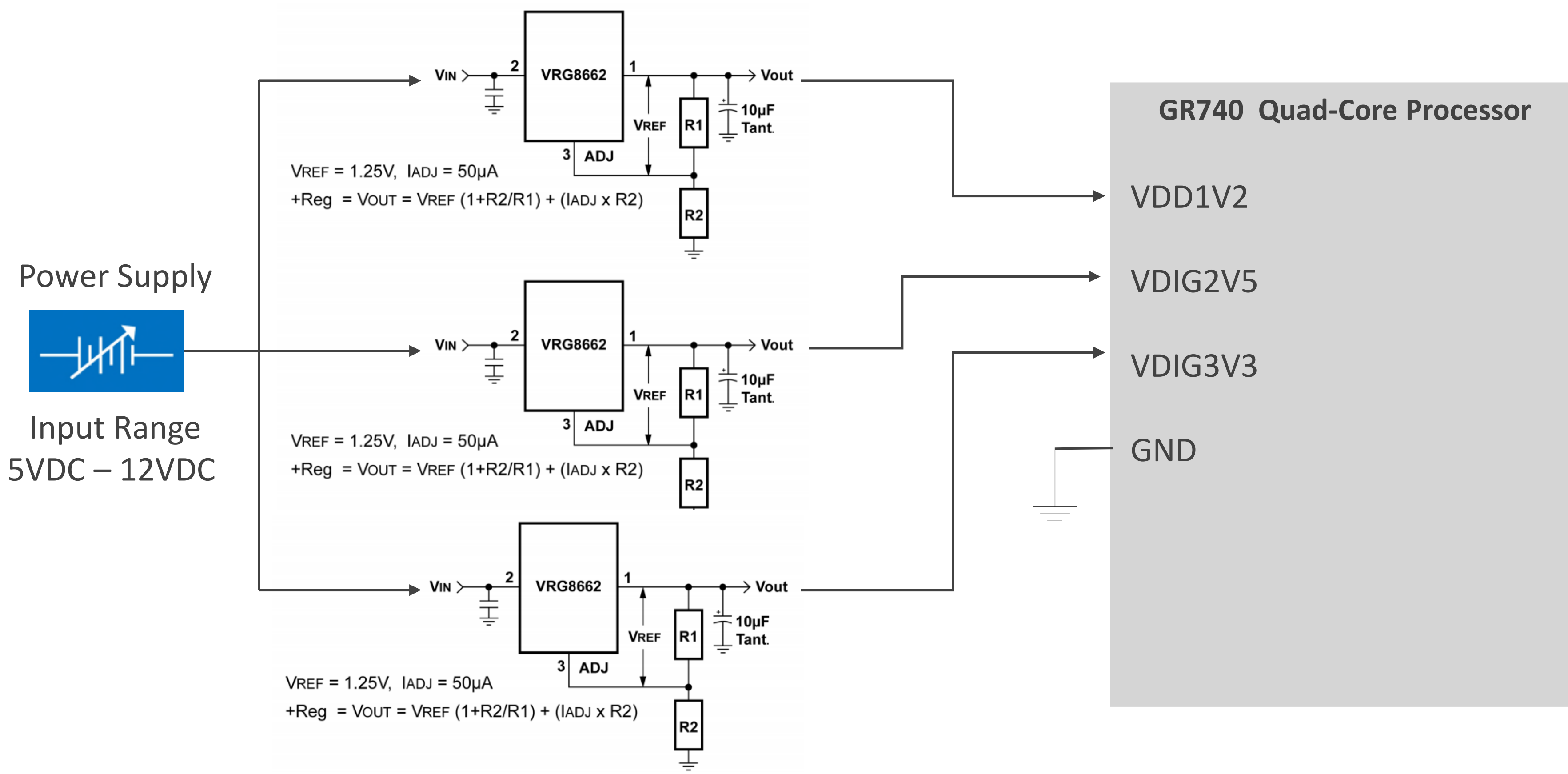
GR740 Power Supply Interface



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VRG8662 LDO Regulator

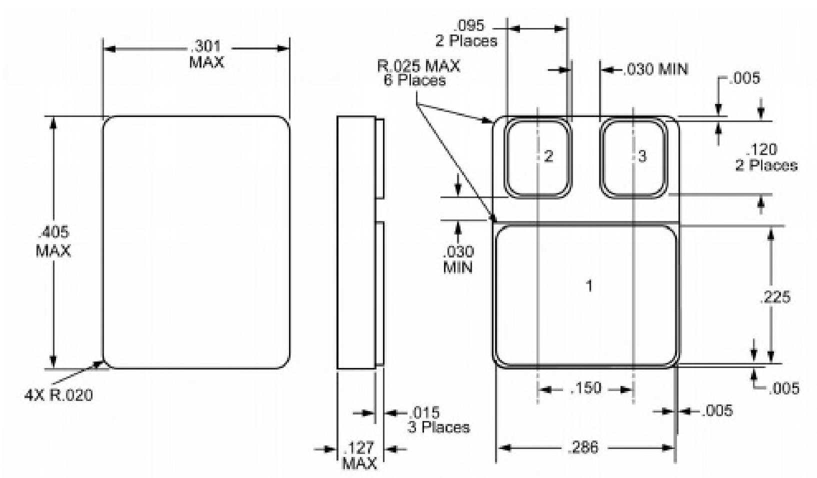

Figure 6 – Package Outline — Surface Mount

Notes:

1) Package & Lid are electrically isolated from signal pads
2) ESD symbol denotes Pin 1

SCD8662

1A LDO Adjustable Positive Voltage Regulator

VRG8662

Features

- Manufactured using Linear Technologies Space Qualified RH1086 die
- Radiation performance
  - Total dose: ≥ 100 krad(Si), Dose rate = 50-300 rad(Si)/s
  - ELDRS: ≥ 50 krad(Si), Dose rate = 0.01 rad(Si)/s
- Thermal shutdown
- Output voltage adjustable: 1.25V to 23V
- Dropout voltage: 1.3V at 1.0 Amps
- 3-Terminal
- Output current: 1.0A (See Note 1, pg 2)
- Voltage reference: 1.25V +2%, -3.2%
- Load regulation: 0.3% max
- Line regulation: 0.25% max
- Ripple rejection: >60dB
- Packaging – Hermetic Ceramic
  - SMD-0.5 Surface mount
  - 3 Pads, .400"L x .296"W x .120"Ht
  - Power package
  - Weight - 2 gm max
- Designed for aerospace and high reliability space applications
- **Radiation Hardness Assurance Plan: DLA Certified to MIL-PRF-38534, Appendix G.**

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Backup

For more info., please contact John Bratton at john.Bratton@CAES.com

Sent for compliance review: August 2, 2021

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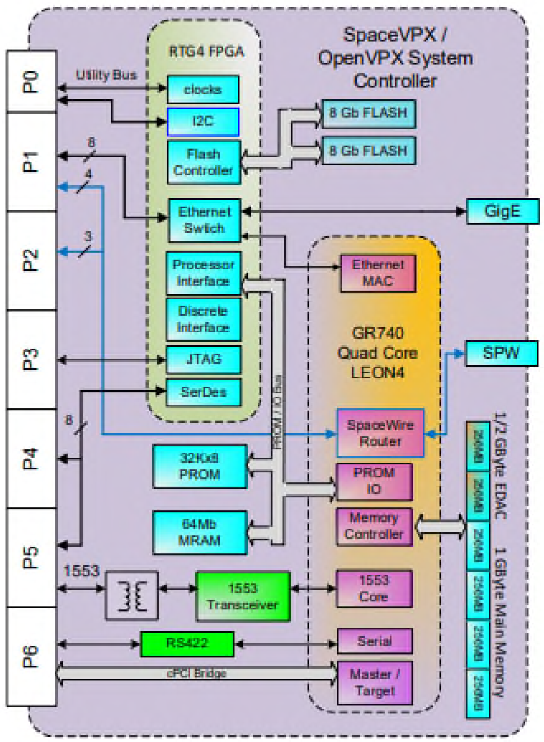
6U SpaceVPX Payload Processor Example



- Quad Core LEON4 / GR740 Processor
  - GFLOP performance
  - 1 Gbyte SDRAM / 0.5 Gbyte EDAC
  - 2 Gbytes Non-Volatile Storage
  - PROM / MRAM / SDRAM memory hierarchy
- VxWorks RT Operating System
- Reconfigurable RTG4 FPGA
- Common Space Grade Interfaces
  - SpaceWire
  - I2C
  - discrete IO
  - MIL-STD-1553B
  - high speed serial

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