DALLAS SEMICONDUCTOR

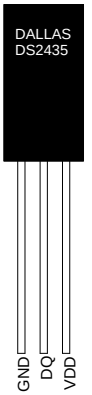
DS2435
Battery Identification Chip with Time/Temperature Histogram

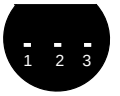
FEATURES

- Provides unique ID number to battery packs
- Eliminates thermistors by sensing battery temperature on–chip
- Elapsed time counter provides indication of battery usage/storage time
- Time/Temperature histogram function provides essential information for determining battery self–discharge
- 256–bit nonvolatile user memory available for storage of user data such as gas gauge and manufacturing information.
- Operating range of –40°C to +85°C
- Applications include portable computers, portable/ cellular phones, consumer electronics, and hand held instrumentation.

PACKAGE OUTLINE

PR–35 PACKAGE





BOTTOM VIEW

See Mech. Drawings Section

PIN DESCRIPTION

GND	–	Ground
DQ	–	Data In/Out
V_{DD}	–	Supply Voltage

DESCRIPTION

The DS2435 Battery Identification Chip provides a convenient method of tagging and identifying battery packs by manufacturer, chemistry, or other identifying parameters. The DS2435 allows the battery pack to be coded with a unique identification number, and also store information regarding the battery life and charge/discharge characteristics in its nonvolatile memory.

The DS2435 also performs the essential function of monitoring battery temperature, without the need for a thermistor in the battery pack. A time/temperature histogram function stores the amount of time that the battery has been in up to eight temperature bands, allowing more accurate self–discharge calculations to be carried out by the user for determining remaining battery capacity. In addition, the on–board elapsed time counter provides a method of determining the amount of time that a battery pack has been in storage, to allow more accurate self–discharge determination.

Information is sent to/from the DS2435 over a 1–wire™ interface, so that battery packs need only have three output connectors; power, ground, and the 1–wire interface.

DETAILED PIN DESCRIPTION

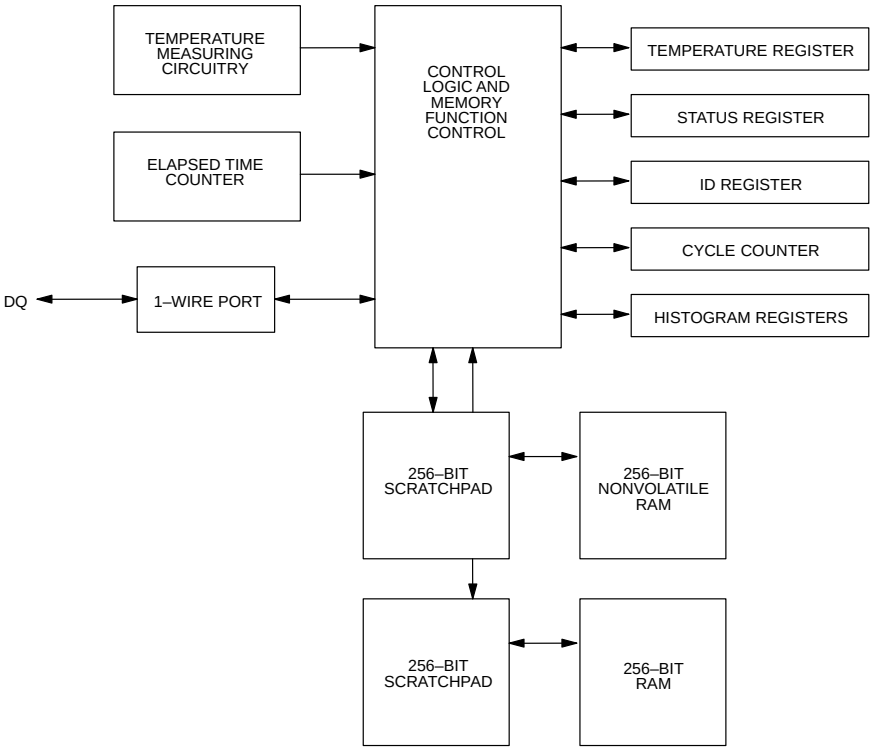
PIN	SYMBOL	DESCRIPTION
1	GND	**Ground pin**.
2	DQ	**Data Input/Output pin** for 1–wire communication port.
3	V_{DD}	**Supply pin** – input power supply.

OVERVIEW

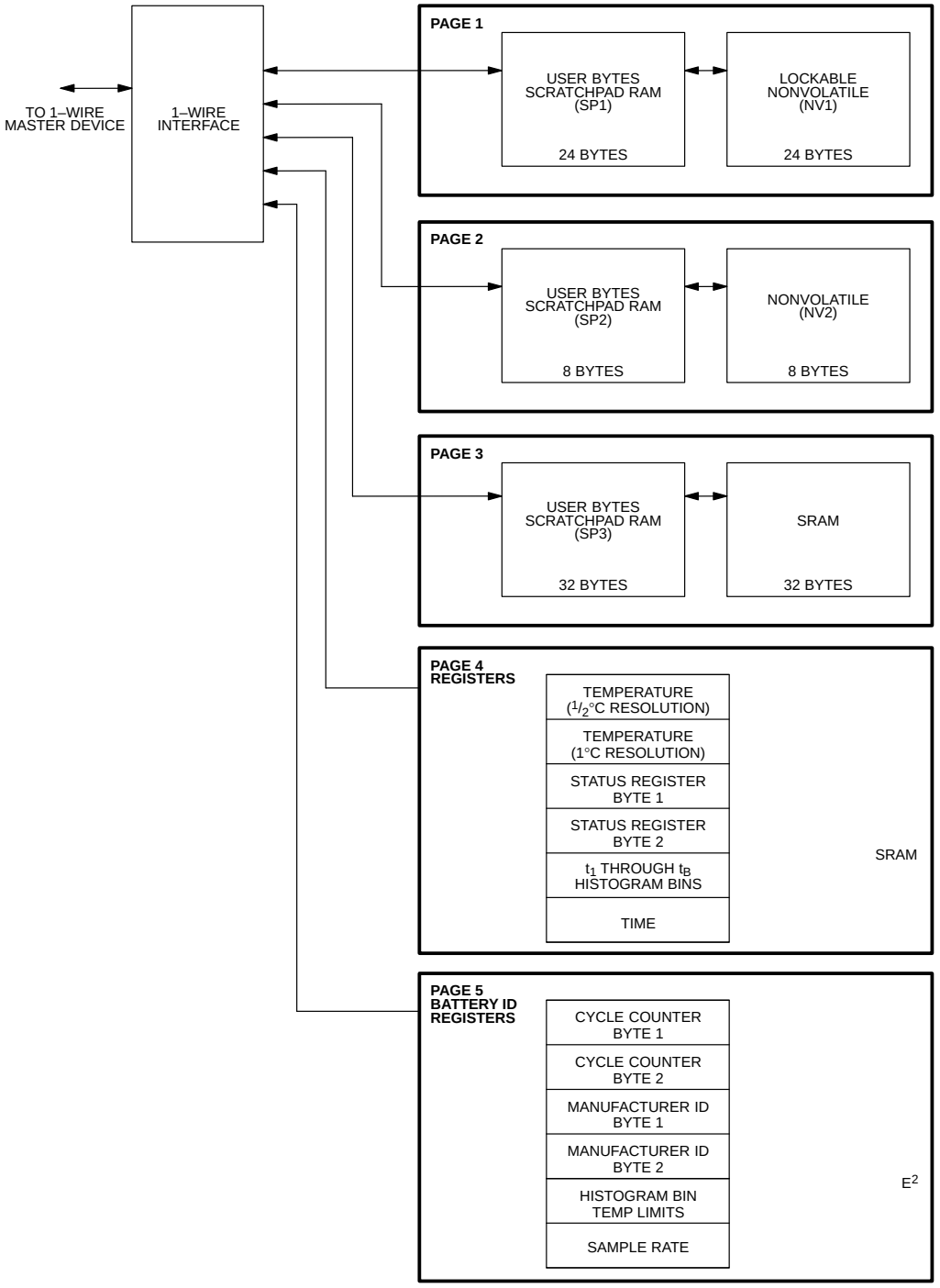
The DS2435 has six major components: 1) Scratchpad Memory, 2) Nonvolatile Memory, 3) On–board SRAM, 4) Temperature Sensor, 5) ID Register, and 6) elapsed time counter. All data is read and written least significant bit first.

Access to the DS2435 is over a 1–wire interface. Charging parameters and other data such as battery chemistry, gas gauge information, and other user data would be stored in the DS2435, allowing this information to be permanently stored in the battery pack. Nonvolatile (E^2) RAM holds information even if the battery goes dead; as long as the battery remains within typical charge/discharge operating range, the SRAM provides battery–backed storage of information.

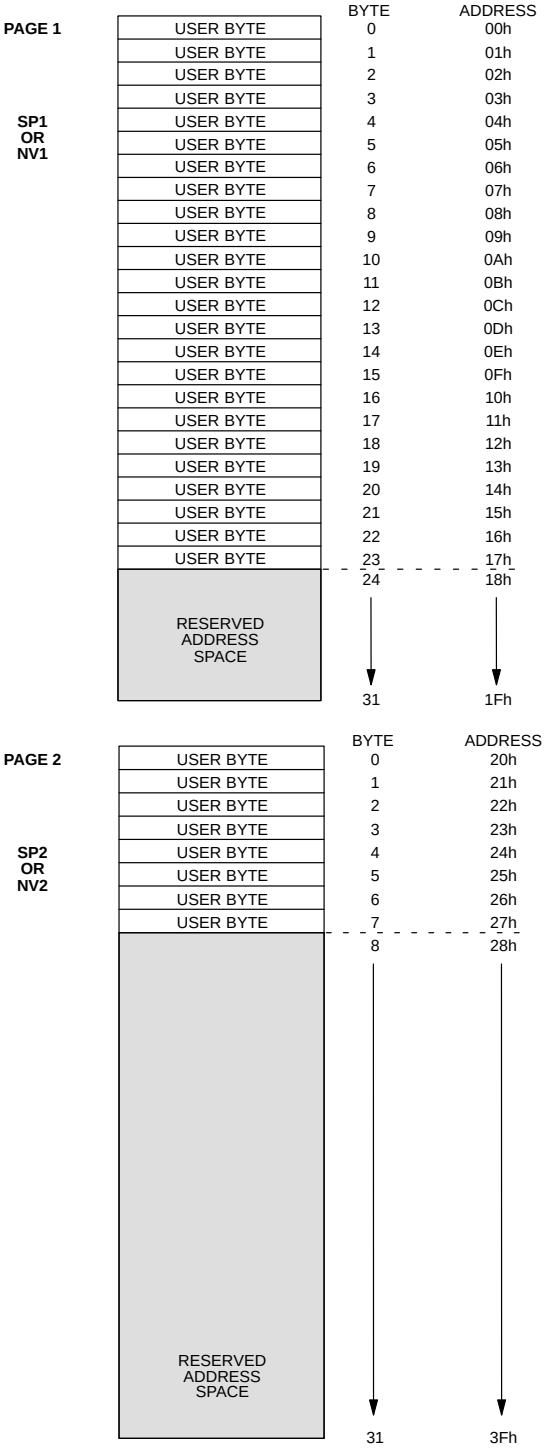
DS2435 BLOCK DIAGRAM Figure 1



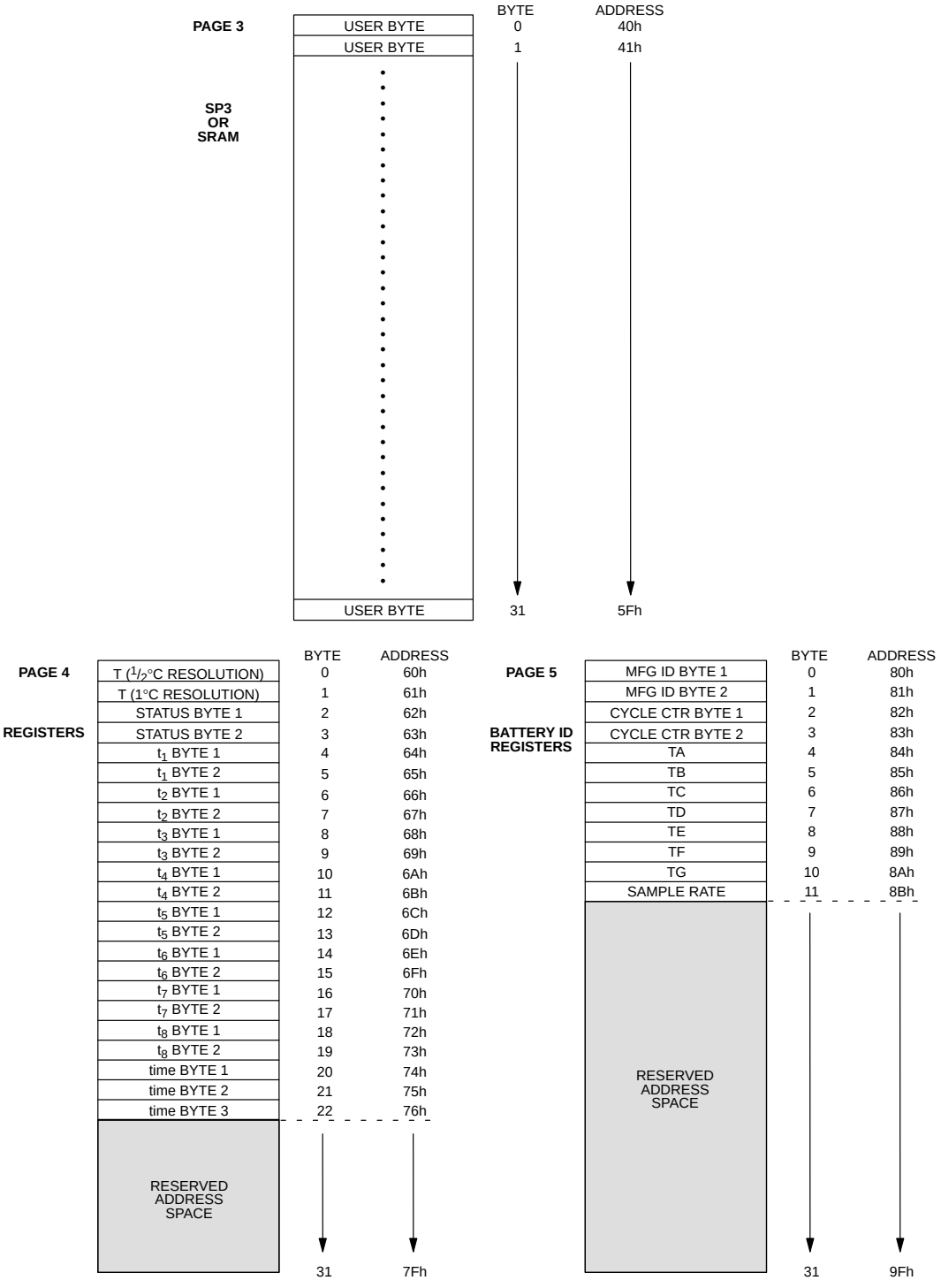
DS2435 MEMORY PARTITIONING Figure 2



DS2435 ADDRESSABLE RAM MEMORY MAP Figure 3



DS2435 ADDRESSABLE RAM MEMORY MAP (Cont'd) Figure 3



OVERVIEW – TIME/TEMPERATURE HISTOGRAM

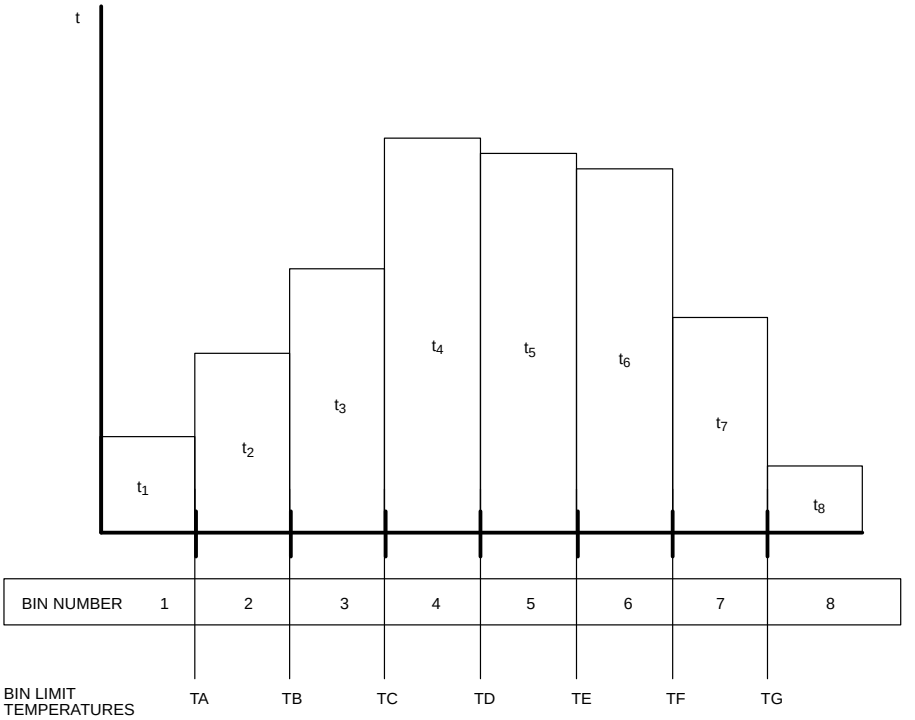
Periods of storage are normal for most battery applications. During this storage time, little or no current is actually drawn from the battery; however, batteries will lose capacity during this storage time due to parasitic side reactions in the cell, as well as other electrochemical mechanisms. This loss of capacity is termed self–discharge.

Since self–discharge is the result of electrochemical reactions, its rate is dependent upon the cell temperature. Knowing the time spent in certain temperature ranges during the storage time of the battery, these temperature effects may be factored into a calculation of self–discharge for the battery, thereby allowing a more accurate determination of retained battery capacity.

The DS2435 measures, tabulates and stores this information in the battery pack. The DS2435 periodically measures the battery temperature, and updates the appropriate temperature "bin" of the time/temperature histogram with the time spent in that temperature range. The resulting histogram data would appear graphically as shown in Figure 4.

The DS2435 allows for eight temperature ranges, or bins, to be specified by fixing the values of the bin limits, TA through TG. Once specified, the time spent in each of the bins (bin 1 being anything less than TA, bin 2 being temperature greater than or equal to TA but less than TB, etc., and bin 8 being anything greater than or equal to TG) is recorded (t_1 being the time spent in bin 1, t_2 the time spent in bin 2, etc.). Using this information and data from the battery manufacturer regarding retained capacity, the actual battery capacity remaining may be closely approximated by the user.

TIME/TEMPERATURE HISTOGRAM Figure 4



MEMORY

The DS2435's memory is divided into five pages, each page filling 32 bytes of address space. Not all of the available addresses are used, however. Refer to the memory map of Figure 3 to see actual addresses which are available for use.

The first three pages of memory consist of a scratchpad RAM and then either a nonvolatile RAM (pages 1 and 2) or SRAM (page 3). The scratchpads help insure data integrity when communicating over the 1–wire bus. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to the RAM (NV or SRAM). This process insures data integrity when modifying the memory.

The fourth page of memory consists of registers which contain the measured temperature value, time/temperature histogram registers, elapsed time counter, and status registers for the device; these registers are made from SRAM cells.

The fifth page of memory holds the ID number for the device, the cycle count registers and the histogram bin limits in E^2 RAM, making these registers nonvolatile under all power conditions.

PAGE 1

The first page of memory has 24 bytes. It consists of a scratchpad RAM and a nonvolatile (E^2) RAM. These 24 bytes may be used to store any data the user wishes; such as battery chemistry descriptors, manufacturing lot codes, gas gauge information, etc.

The nonvolatile portion of this page may be locked to prevent data stored here from being changed inadvertently.

Both the nonvolatile and the scratchpad portions are organized identically, as shown in the memory map of Figure 3. In this page, these two portions are referred to as NV1 and SP1, respectively.

PAGE 2

The second page of memory has 8 bytes. It consists of a scratchpad RAM and a nonvolatile (E^2) RAM. These eight bytes may be used to store any data the user wishes, such as battery chemistry descriptors, manufacturing lot codes, gas gauge information, etc.

PAGE 3

The third page of memory has a full 32 bytes. It consists of a scratchpad RAM and an SRAM. This address space may be used to store any data the user wishes, provided that, should the battery go dead and power to the DS2435 is lost, this data may also be lost without serious repercussions. Data which must remain even if power to the DS2435 is lost should be placed in either Page 1 or Page 2.

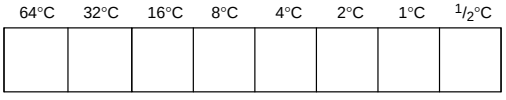
This section of memory may be used to store gas gauge and self discharge information. If the battery dies, and this information is lost, it is moot because the user can easily determine that the battery is dead.

PAGE 4

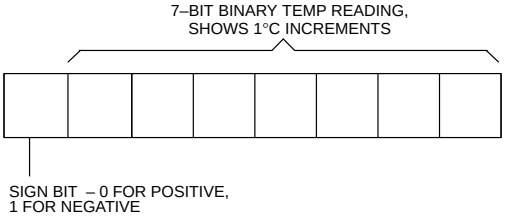
The fourth page of memory is used by the DS2435 to store the converted value of battery temperature, the time/temperature histogram data, and the elapsed time counter. A two–byte status register is also provided.

TEMPERATURE REGISTERS (60h–61h)

The DS2435 can measure temperature without external components. The resulting temperature measurement is placed into two temperature registers. These registers are SRAM, and therefore will hold the values placed in them until the battery voltage falls below the minimum V_{DD} specified. The first register, at address 60h, provides $^1/_2$°C resolution for temperatures between 0°C and 127 $^1/_2$°C, formatted as follows:



The second register, at address 61h, provides 1°C resolution over the –40°C to +85°C range, formatted as follows in the binary two's complement coding as shown in Table 1:



TEMPERATURE/DATA RELATIONSHIPS

Table 1

TEMPERATURE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+85°C	01010101	55h
+25°C	00011001	19h
1°C	00000001	01h
0°C	00000000	00h
–1°C	11111111	FFh
–25°C	11100111	E7h
–40°C	11011000	D8h

STATUS/CONTROL REGISTER (62h–63h)

The status register is a two byte register at addresses 62h and 63h (consisting of SRAM). Address 62h is the least significant byte of the status register, and is currently the only address with defined status bits; the other byte at address 63h is reserved for future use. The status register is formatted as follows:

STATUS REGISTER

							LSB	
X	X	X	X	X	LOCK	NVB	TB	62h
X	X	X	X	X	X	X	X	63h

where

X = Don't Care

TB = Temperature Busy flag. "1" = temperature conversion in progress; "0" = temperature conversion complete, valid data in temperature register.

NVB = Nonvolatile memory busy flag. "1" = Copy from scratchpad to NVRAM in progress, "0" = nonvolatile memory is not busy. A copy to NVRAM may take from 2 ms to 10 ms (taking longer at lower supply voltages).

LOCK = "1" indicates that NV1 is locked; "0" indicates that NV1 is unlocked.

t_1–t_8 REGISTERS (64h–73h)

These registers hold the accumulated time values for the time/temperature histogram. t_1 corresponds to the time spent in histogram bin 1, t_2 the time spent in bin 2, etc., where the bins are defined by the limits set in TA–TG as shown in Figure 4. The format for the time value stored in these two–byte registers depends upon the SAMPLE RATE, and is defined in the paragraph describing the SAMPLE RATE parameter.

t REGISTER (74n–76h)

This three–byte register is the elapsed time counter, formatted as follows:

ELAPSED TIME COUNTER

2^{23} min	2^{22} min	2^{21} min	2^{20} min	2^{19} min	2^{18} min	2^{17} min	2^{16} min	76h
32768 min	16384 min	8192 min	4096 min	2048 min	1024 min	512 min	256 min	75h
128 min	64 min	32 min	16 min	8 min	4 min	2 min	1 min	74h

The elapsed time counter has an LSB value of 1 minute; the total time which the counter can accommodate is 2^{24} minutes, or 31.92 years.

Issuing any protocol to the DS2435 prevents the incrementing of the elapsed time counter and histogram registers, until the protocol is cleared by issuing a reset. Therefore, it is imperative that any protocol issued to the DS2435 be followed by a reset (either after the protocol, if it requires no data, or immediately following data, if required by the protocol). This is necessary to avoid contention between the counter and histogram writing process and external processes.

PAGE 5

The fifth page of memory holds the battery manufacturer ID number, a two–byte counter for counting the number of battery charge/discharge cycles, histogram bin limits, and sample rate.

ID REGISTER (80h and 81h)

The ID Register is a 16–bit ROM register that can contain a unique identification code, if purchased from Dallas Semiconductor. This ID number is programmed by Dallas Semiconductor, is unchangeable, and is unique to each customer. This ID number may be used to assure that batteries containing a DS2435 have the same manufacturer ID number as a charger configured to operate with that battery pack. This feature may be used to prevent charging of batteries for which the charging circuit has not been designed.

CYCLE COUNTER (82h and 83h)

The cycle counter register gives an indication of the number of charge/discharge cycles the battery pack has been through. This nonvolatile (E^2) register is incremented by the user through the use of a protocol to the DS2435, and is reset by another protocol. The counter is a straight binary counter, formatted as follows:

CYCLE COUNTER

MSB

32768	16384	8192	4096	2048	1024	512	256

65h

LSB

128	64	32	16	8	4	2	0

64h

TA–TG REGISTERS (84h–8Ah)

These registers define the boundaries for the temperature bins in the time/temperature histogram, as shown in Figure 4. These temperature values are expressed in the same temperature format as shown in Table 1. These limits therefore may be positive or negative values, expressed with 1°C resolution. The bin limits must be specified in increasing order (i.e., TA<TB, TB<TC, etc.).

SAMPLE RATE (8Bh)

This register defines the periodic interval at which the DS2435 will take a temperature measurement for updating the histogram data. Note that this does not affect the actual time needed to perform a temperature conversion using the Convert T protocol; this sample rate refers only to the periodic interval at which histogram data is updated.

The sample rate is expressed as follows:

SAMPLE RATE

LSB

X	X	X	X	X	S2	S1	S0

S2	S1	S0	SAMPLE RATE
0	0	0	1/2 minute
0	0	1	1 minute
0	1	0	2 minutes
0	1	1	4 minutes
1	0	0	1/8 hour
1	0	1	1/4 hour
1	1	0	1/2 hour
1	1	1	1 hour

The interval specified in this register determines the LSB value for the time/temperature histogram registers, as shown in Figure 5. Examples of time expressions for a given sample rate are shown in Table 2.

HISTOGRAM REGISTER DATA GIVEN FOR SAMPLE RATE Figure 5

SAMPLE RATE — DATA STRUCTURE – NUMBERS EXPRESS MINUTES

16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	.	1/2 (LSB)

SAMPLE RATE — DATA STRUCTURE – NUMBERS EXPRESS HOURS

SAMPLE RATE																	
	BYTE 2								BYTE 1								
1/8	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	.	1/2	1/4	1/8 (LSB)
1/4	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	.	1/2	1/4 (LSB)
1/2	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	.	1/2 (LSB)
1	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	. (LSB)

EXAMPLE CODES FOR 771 HOURS, 22.5 MINUTES WITH DIFFERENT SAMPLE RATES Table 2

SAMPLE RATE	t_X BYTE 1	t_X BYTE 2
1/8	00011000	00011011
1/4	00001100	00001101
1/2	00000110	00000110
1	00000011	00000011

MEMORY FUNCTION COMMANDS

The protocols necessary for accessing the DS2435 are described in this section. These are summarized in Table 3, and examples of memory functions are provided in Tables 4 and 5.

PAGE 1 THROUGH PAGE 3 COMMANDS

Read Scratchpad [11h]

This command reads the contents of the scratchpad RAM on the DS2435. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin reading the data. The user may read data through the end of the scratchpad space (address 5Fh), with any reserved data bits reading all logic 1's and after which the data read will be a repeat of address 5FH.

Write Scratchpad [17h]

This command writes to the scratchpad RAM on the DS2435. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin writing data to the DS2435 scratchpad at the starting byte address.

Copy SP1 to NV1 [22h]

This command copies the entire contents (24 bytes) of Scratchpad 1 (SP1) to its corresponding nonvolatile memory (NV1). The nonvolatile RAM memory of the DS2435 cannot be written to directly by the bus master; however, the scratchpad RAM may be copied to the nonvolatile RAM. This prevents accidental overwriting of the nonvolatile RAM, and allows the data to be written first to the scratchpad, where it can be read back and verified before copying to the nonvolatile RAM. This command does not use a start address; the entire contents of the scratchpad will be copied to the nonvolatile RAM. The NVB bit will be set when the copy is in progress. NV1 is made with E^2 type memory cells that will accept at least 50000 changes.

Copy SP2 to NV2 [25h]

This command copies the entire contents (8 bytes) of SP2 (user bytes) to its corresponding nonvolatile memory (NV2). This command does not use a start address; the entire contents of SP2 will be copied to NV2. The NVB bit will be set when the copy is in progress. NV2 is made with E^2 type memory cells that will accept at least 50000 changes.

Copy SP3 to SRAM [28h]

This command copies the entire contents (32 bytes) of SP3 to its corresponding SRAM. This command does not use a start address; the entire contents of SP3 will be copied to the SRAM.

Copy NV1 to SP1 [71h]

This command copies the entire contents (24 bytes) of NV1 to its corresponding scratchpad RAM (SP1). This command does not use a start address; the entire contents of NV1 will be copied to SP1. The nonvolatile RAM memory of the DS2435 cannot be read directly by the bus master; however, the nonvolatile RAM may be copied to the scratchpad RAM.

Copy NV2 to SP2 [77h]

This command copies the entire contents (8 bytes) of NV2 (user bytes) to its corresponding scratchpad RAM (SP2). This command does not use a start address; the entire contents of NV2 will be copied to SP2. The nonvolatile RAM memory of the DS2435 cannot be read directly by the bus master; however, the nonvolatile RAM may be copied to the scratchpad RAM.

Copy SRAM to SP3 [7Ah]
This command copies the entire contents (32 bytes) of SRAM to its corresponding scratchpad RAM (SP3). This command does not use a start address; the entire contents of SRAM will be copied to SP3.The SRAM memory of the DS2435 cannot be read directly by the bus master; however, the SRAM may be copied to the scratchpad RAM.

Lock NV1 [43h]
This command prevents copying SP1 to NV1. This is done as an added measure of data security, preventing data from being changed inadvertently. NV1 may be copied up into SP1 while the part is locked. This allows NV1 to be read at any time. However, NV1 cannot be written to through a Copy SP1 to NV1 command without first unlocking the DS2435.

Unlock NV1 [44h]
This command unlocks NV1, to allow copying SP1 into NV1. This is done as an added measure of data security, preventing data from being changed inadvertently.

PAGE 4 AND 5 COMMANDS

Convert T [D2h]
This command instructs the DS2435 to initiate a temperature conversion cycle. This sets the TB flag. When the temperature conversion is done, the TB flag is reset and the current temperature value is placed in the temperature register. While a temperature conversion is taking place, all other memory functions are still available for use.

Reset Histogram [E1h]
This command resets the accumulated time in all of the histogram temperature registers to zero. In addition, this command also resets the elapsed time counter to zero. This command does not use a start address; no further data is required.

Set Clock [E6h]
This command sets the elapsed time counter to a preset value. This command is followed by three bytes of data, which will be stored at addresses 74h–76h. The transfer of this 3–byte value will occur after reception of the 24th bit following the protocol, at which time the elapsed time counter will begin incrementing the counter registers in 1 minute increments.

Write Registers [EFh]
This command allows writing directly to the TA–TG registers and the sample rate register. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin writing the data.

Read Registers [B2h]
This command reads the contents of the registers in Page 4 and 5. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin reading the data. The user may read data through the end of the register space (through address 76h in Page 4, address 8Bh in Page 5), after which the data read will be all logic 1's.

Increment Cycle [B5h]
This command increments the value in the cycle counter register. This command does not use a start address; no further data is required.

Reset Cycle Counter [B8h]
This command is used to reset the cycle counter register to zero, if desired.

DS2435 COMMAND SET Table 3

INSTRUCTION	DESCRIPTION	PROTOCOL	1–WIRE BUS MASTER STATUS AFTER ISSUING PROTOCOL	1–WIRE BUS DATA AFTER ISSUING PROTOCOL
PAGE 1 THROUGH PAGE 3 MEMORY COMMANDS				
Read Scratchpad	Reads bytes from DS2435 Scratchpad.	11h <addr (00h–5Fh)>	RX	<read data>
Write Scratchpad	Writes bytes to DS2435 Scratchpad.	17h <addr 00h–5Fh)>	TX	<write data>
Copy SP1 to NV1	Copies entire contents of SP1 to NV1.	22h	Idle	{NVB bit in Status Register=1 until copy complete (2–5ms, typ)}
Copy SP2 to NV2	Copies entire contents of SP2 to NV2.	25h	Idle	{NVB bit in Status Register=1 until copy complete (2–5ms, typ)}
Copy SP3 to SRAM	Copies entire contents of SP3 to SRAM.	28h	Idle	Idle
Copy NV1 to SP1	Copies entire contents of NV1 to SP1.	71h	Idle	Idle
Copy NV2 to SP2	Copies entire contents of NV2 to SP2.	77h	Idle	Idle
Copy SRAM to SP3	Copies entire contents of SRAM to SP3.	7Ah	Idle	Idle
Lock NV1	Locks 24 bytes of SP1 and NV1 from reading and writing.	43h	Idle	{NVB bit in Status Register=1 until copy complete (2–5ms, typ)}
Unlock NV1	Unlocks 24 bytes of SP1 and NV1 for reading and writing.	44h	Idle	{NVB bit in Status Register=1 until copy complete (2–5ms, typ)}
PAGE 4 AND PAGE 5 REGISTER COMMANDS				
Read Registers	Reads bytes from Temperature, Status and ID Registers.	B2h <addr (60h–76h, 80h–8Bh)>	RX	<read data>
Write Register	Write to TA–TG and Sample Rate Registers	EFh <addr 84h–8Bh>		
Reset Cycle Counter	Resets cycle counter registers to zero.	B8h	Idle	{NVB bit in Status Register=1 until copy complete (2–5ms, typ)}
Increment Cycle Counter	Increments the value in the cycle counter register.	B5h	Idle	{NVB bit in Status Register=1 until copy complete (2–5ms, typ)}
Reset Historgram	Resets all histogram registers to zero	E1h	Idle	Idle
Set Clock	Presets a value for elapsed time counter and begins timing.	E6h	TX	<3 bytes>
Convert T	Initiates temperature conversion.	D2h	Idle	{TB bit in Status Register=1 until conversion complete}

MEMORY FUNCTION EXAMPLE Table 4
Example: Bus Master writes 24 bytes of data to DS2435 scratchpad, then copies to it to NV1.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	17h	Issue “write scratchpad” command
TX	00h	Start address
TX	<24 bytes>	Write 24 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	11h	Issue “read scratchpad” command
TX	00h	Start address
RX	<24 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	22h	Issue “copy SP1 to NV1” command
RX	<busy indicator>	Wait until NVB in status register=1 (2–5 ms typical)
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

MEMORY FUNCTION EXAMPLE Table 5
Example: Bus Master initiates temperature conversion, then reads temperature.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	D2h	Issue “convert T” command
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	B2h	Issue “read registers” command; begin loop
TX	62h	Status register address
RX	<1 data byte>	Read status register and loop until TB=0
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	B2h	Issue “read registers” command
TX	61h	Temperature register address
RX	<1 data byte>	Read temperature register
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

1–WIRE BUS SYSTEM

The DS2435 1–wire bus is a system which has a single bus master and one slave. The DS2435 behaves as a slave. The DS2435 is not able to be multidropped, unlike other 1–wire devices from Dallas Semiconductor.

The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1–wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–wire bus must have open drain or 3–state outputs. The 1–wire port of the DS2435 is open drain with an internal circuit equivalent to that shown in Figure 6. The 1–wire bus requires a pull–up resistor of approximately 5KΩ.

The idle state for the 1–wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480 μs, all components on the bus will be reset.

TRANSACTION SEQUENCE

The protocol for accessing the DS2435 via the 1–wire port is as follows:

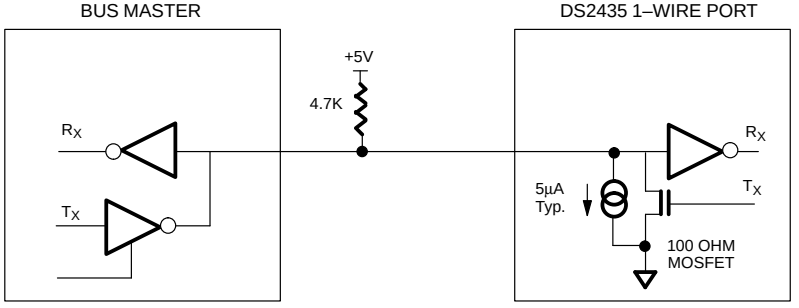
- Initialization
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1–wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS2435 is on the bus and is ready to operate. For more details, see the “I/O Signaling” section.

HARDWARE CONFIGURATION Figure 6



I/O SIGNALING

The DS2435 requires strict protocols to insure data integrity. The protocol consists of several types of signaling on one line: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. All of these signals, with the exception of the presence pulse, are initiated by the bus master.

The initialization sequence required to begin any communication with the DS2435 is shown in Figure 7. A reset pulse followed by a presence pulse indicates the DS2435 is ready to send or receive data given the correct memory function command.

The bus master transmits (TX) a reset pulse (a low signal for a minimum of 480 μs). The bus master then releases the line and goes into a receive mode (RX). The 1–wire bus is pulled to a high state via the 5K pull–up resistor. After detecting the rising edge on the I/O pin, the DS2435 waits 15–60 μs and then transmits the presence pulse (a low signal for 60–240 μs).

READ/WRITE TIME SLOTS

DS2435 data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction.

Write Time Slots

A write time slot is initiated when the host pulls the data line from a high logic level to a low logic level. There are two types of write time slots: Write One time slots and Write Zero time slots. All write time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual write cycles.

The DS2435 samples the I/O line in a window of 15 µs to 60 µs after the I/O line falls. If the line is high, a Write One occurs. If the line is low, a Write Zero occurs (see Figure 6).

For the host to generate a Write One time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 µs after the start of the write time slot.

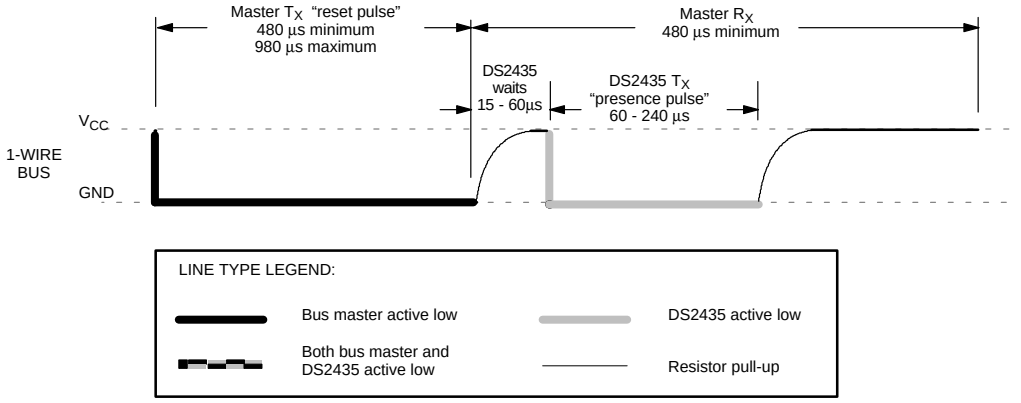
For the host to generate a Write Zero time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot.

Read Time Slots

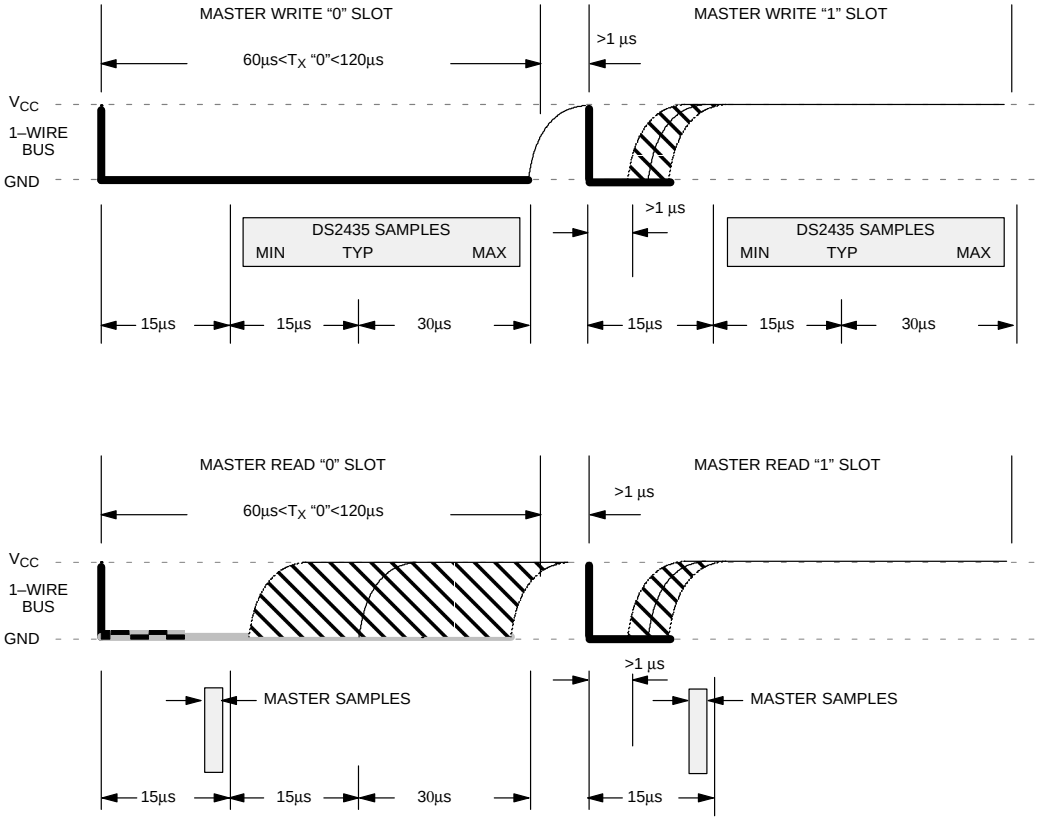
The host generates read time slots when data is to be read from the DS2435. A read time slot is initiated when the host pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of 1 µs; output data from the DS2435 is then valid for the next 14 µs maximum. The host therefore must stop driving the I/O pin low in order to read its state 15 µs from the start of the read slot (see Figure 8). By the end of the read time slot, the I/O pin will pull back high via the external pull–up resistor. All read time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual read slots.

Figure 9 shows that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15 µs. Figure 10 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as small as possible and by locating the master sample time towards the end of the 15 µs period.

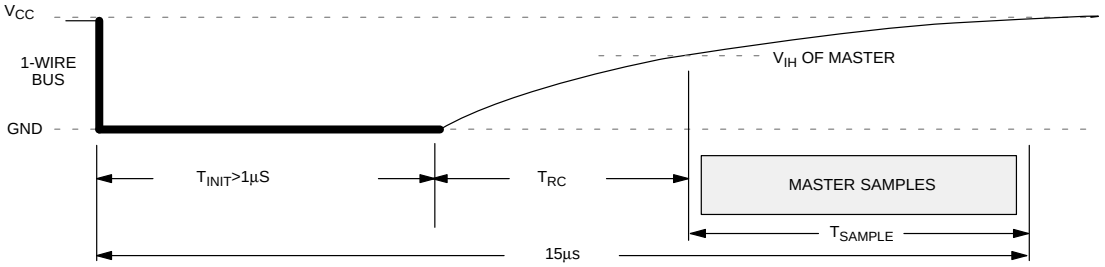
INITIALIZATION PROCEDURE “RESET AND PRESENCE PULSES” Figure 7



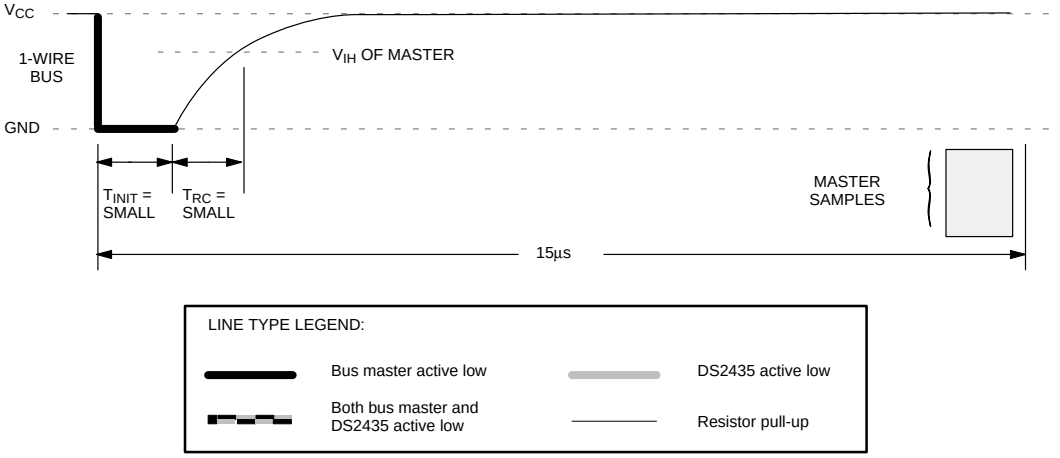
READ/WRITE TIMING DIAGRAM Figure 8



DETAILED MASTER READ "1" TIMING Figure 9



RECOMMENDED MASTER READ "1" TIMING Figure 10



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	I/O Functions	2.5		6.4	V	
		NV Copy Functions	2.7		6.4		
		$\pm 1/2$°C Accurate Temp. Conversions	3.6		6.4		1
Data Pin	$V_{I/O}$		–0.3		V_{DD}+0.3	V	

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{DD}=3.6V to 6.4V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Temperature Accuracy (=$T_{ACTUAL} - T_{MEASURED}$)		T_A=0°C to 70°C			$\pm 1/2$	°C	
		T_A=–40°C to 0°C and +70°C to +85°C			See typical curve		3
Input Logic High	V_{IH}	V_{DD}=4.8V	2.2		V_{DD}+0.3	V	
Input Logic Low	V_{IL}	V_{DD}=4.8V	–0.3		+0.8	V	
Sink Current	I_L	$V_{I/O}$=0.4V	–4.0			mA	
Standby Current	I_Q	Clock Running		10	25	µA	4
Active Current	I_{DD}	Temp Conversions			1.5	mA	4
Input Resistance	R_I			500		KΩ	2

NOTES:

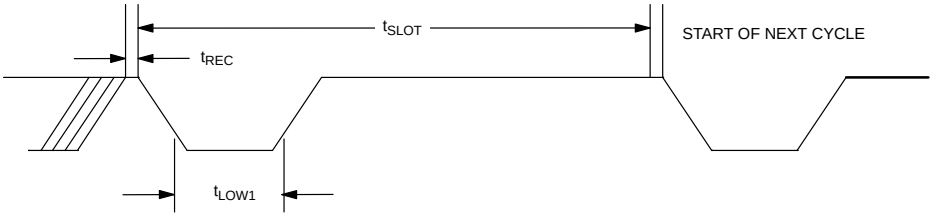
1. Temperature conversion will work with ±2°C accuracy down to V_{DD}=2.7V.
2. I/O line in “hi–Z” state and $I_{I/O}$=0. Resistance specified from I/O to ground.
3. See typical curve for specification limits outside 0°C to 70°C range. Thermometer error reflects sensor accuracy as tested during calibration.
4. Specified with DQ=V_{DD}.
5. The bus should not remain idle for more than 20 ms between bits or between a bit and a reset.

AC ELECTRICAL CHARACTERISTICS: 1–WIRE INTERFACE

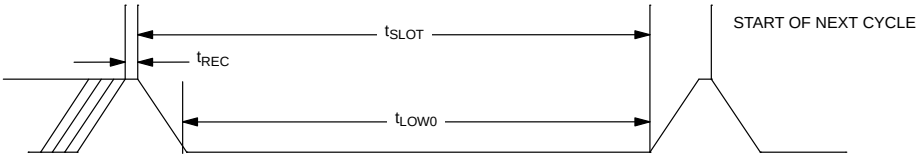
(–40°C to +85°C; V_{DD}=3.6V to 6.4V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	t_{CONV}		250	500	ms	
Time Slot	t_{SLOT}	60		120	µs	
Recovery Time	t_{REC}	1		20000	µs	5
Write 0 Low Time	t_{LOW0}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Read Data Valid	t_{RDV}			15	µs	
Reset Time High	t_{RSTH}	480			µs	
Reset Time Low	t_{RSTL}	480			µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	
Capacitance	$C_{IN/OUT}$			25	pF	
Timer Accuracy				±10	%	

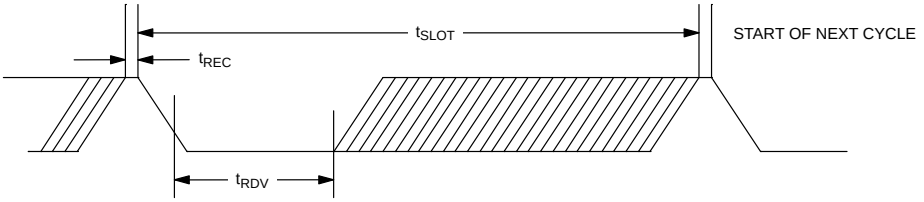
1–WIRE WRITE ONE TIME SLOT



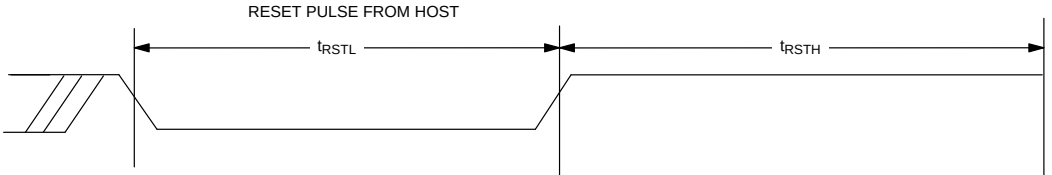
1–WIRE WRITE ZERO TIME SLOT



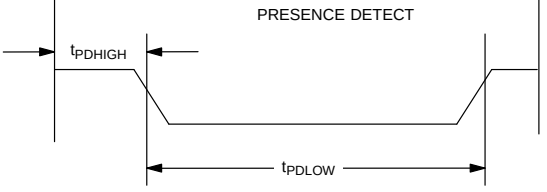
1-WIRE READ ZERO TIME SLOT



1-WIRE RESET PULSE



1-WIRE PRESENCE DETECT



TYPICAL PERFORMANCE CURVE

DS2435 DIGITAL THERMOMETER AND THERMOSTAT
TEMPERATURE READING ERROR