QUALITY SYSTEM

Product quality at Dallas Semiconductor results from a combination of design techniques, vendor controls, manufacturing methods, process monitors, and quality control inspections. SPC monitors placed at strategic points ensure that potential defects are detected promptly.

QUALITY CONTROL PROCESSES

- Incoming Quality Control (IQC): Piece parts and raw materials are inspected by IQC. New vendors and piece parts receive a First Article Inspection; subsequent incoming materials receive a sample inspection per MIL-STD-105.
- In-Process Inspections: Each manufacturing operation inspects its own work, ensuring immediate feedback and preventing deviations from going undetected due to subsequent processing.
- Statistical Process Control (SPC): Implemented in manufacturing, this process determines what inputs to the product flow are critical and how to track and control those inputs. Quality Engineering provides training, computer analysis, and feedback to manufacturing.
- In-Process Sample Tests: In order to guarantee the accuracy and completeness of in-process inspections and SPC monitors, QC Toll Gates at strategic locations perform sample inspections per MIL-STD-105.

RELIABILITY SYSTEM

Reliability is accomplished through a rigorous, comprehensive methodology of qualifying, analyzing, and monitoring new equipment, processes, products, and packages. A state-of-the-art environmental facility allows accelerated stresses to be performed and monitored inhouse. In addition, a metallurgical laboratory has been equipped to perform real-time x-ray, x-ray fluorescense, and solderability measurements.

To minimize the human influence on the outcome of the reliability activity, a dedicated group of technicians and assistants handle all reliability stressing and testing. Reliability data resides on a customized computer—based tracking and retrieval system. Technical support includes oven and chamber calibrations, 100% electrical board checks, and strict electrostatic protection.

PRODUCT QUALIFICATION

Product qualification activity at Dallas Semiconductor involves a series of accelerated stress tests applied to production—ready material and follows a defined qualification plan. Random samples from at least three production lots, equally representing the production version of the product, are tested to meet reliability requirements. Any device failures detected during production qualification or subsequent monitoring are fully analyzed in our Failure Analysis Laboratory.

Products at Dallas Semiconductor fall into one of three classifications: Prototype or Engineering Sample, Prequal, and Fully Qualified.

- Prototype or Engineering Sample: Prototype products have not been fully characterized to all data sheet limits. However, based upon limited data, these products will meet data sheet limits. Final test and all processes used to manufacture the product are under engineering control. Qualification of the product has not started. The brand on prototype products will be PROTO or ES.
- Prequal: Prequal products meet prototype requirements and are characterized to all data sheet limits.
 Final test and all processes used to manufacture the product are stable and under manufacturing control.
 Qualification of the product has started.
- Fully Qualified: Fully qualified products meet prototype and prequal requirements. The qualification requirements given in the next section have been completed. Product must statistically meet reliability failure rates and quality requirements as established by Quality and Reliability Engineering.

Tables 1, 2 and 3 list the tests which a Dallas Semiconductor product must pass in order to be classified as fully qualified.

RELIABILITY MONITOR PROGRAM

In order to maintain continuous qualification status on all products, Dallas Semiconductor has implemented an extensive Reliability Monitor Program (RMP). The RMP monitors all design, wafer fabrication, and assembly processes in the qualified products database. Product is selected monthly from finished goods and subjected to a series of reliability tests similar to those used in the original qualification. Any failures generated from these tests require analysis to root cause and corrective action.

Data from the RMP is published quarterly and is available on demand.

QUALITY AND RELIABILITY

FULL QUALIFICATION REQUIREMENTS FOR INTEGRATED CIRCUIT PRODUCTS Table 1

| STRESS/TEST | CONDITION | DURATION | ACCEPTANCE CRITERIA (LTPD) |
|------------------------------------|---------------------------------|----------------|----------------------------|
| Outgoing Elec. Test | Data Sheet | 0 Hr. | 0.15% |
| Infant Life | 125°C, 7.0V | 48 Hr. | 0.3% |
| High Temperature Operating Life | 125°C, 5.5V | 1000 Hr. | *0.4% |
| Use Condition Prediction | 55°C, 5.5V | 10 years | 50 Fits |
| High Voltage Life | 125°C, 7.0V | 1000 Hr. | *0.4% |
| High Temperature Storage | 150°C, No Bias | 1000 Hr. | 2.0% |
| Temperature Humidity Bias | 85°C/85% RH, 5.5V | 1000 Hr. | 1.0% |
| Autoclave | 121°C, 2 ATM Steam, Unbiased | 168 Hr. | 1.5% |
| Temperature Cycle | –55°C to +125°C | 1000 cycle | 1.0% |
| X–Ray | MIL-STD-883 Method 2012 | | 15% |
| Bond Pull | MIL-STD-883 Method 2011 | Premold | 1.5% |
| Dimensions | MIL-STD-883 Method 2016 | | 15% |
| Lead Integrity | MIL-STD-883 Method 2004 | | 3.0% |
| Solderability | MIL-STD-883 Method 2003 | 8 Hr. Steamage | 3.0% |
| ESD | MIL-STD-883 Method 3015 | | > ±1000 volts |
| Latch-up | JEDEC Std. 17 | | > 100 mW/pin |

^{*} Combined high voltage life and operating life requirement.

FULL QUALIFICATION REQUIREMENTS FOR MODULE PRODUCTS Table 2

| STRESS/TEST | CONDITION | DURATION | ACCEPTANCE CRITERIA (LTPD) |
|-------------------------------|----------------------------|----------------|----------------------------|
| Outgoing Elec. Test | Data Sheet | 0 Hr. | 0.15% |
| Use Condition Prediction | 55°C, 5.5V | 10 years | 50 Fits |
| High Temperature Storage | 85°C, No Bias | 1000 Hr. | 2.0% |
| *Temperature Humidity Bias | 85°C/85% RH, 5.5V | 959 Hr. | 1.0% |
| Temperature Cycle | –40°C to +85°C | 1000 cycle | 1.0% |
| X–Ray | MIL-STD-883 Method 2012 | | 15% |
| Dimensions | MIL-STD-883 Method 2016 | | 15% |
| Lead Integrity | MIL-STD-883 Method 2004 | | 3.0% |
| Solderability | MIL-STD-883 Method 2003 | 8 Hr. Steamage | 3.0% |

^{*} Selected products.

FULL QUALIFICATION REQUIREMENTS FOR SIPSTIK AND TOUCH MEMORY PRODUCTS Table 3

| STRESS/TEST | CONDITION | DURATION | ACCEPTANCE CRITERIA (LTPD) |
|--------------------------|----------------|-----------|----------------------------|
| Outgoing Elec. Test | Data Sheet | 0 Hr. | 0.15% |
| High Temperature Storage | 85°C, No Bias | 1000 Hr. | 7.0% |
| Temperature Humidity | 60°C/90% RH | 288 Hr. | 7.0% |
| Temperature Cycle | –40°C to +85°C | 500 cycle | 7.0% |