DALLAS SEMICONDUCTOR

DS229
Triple RS–232 Transmitter/Receiver

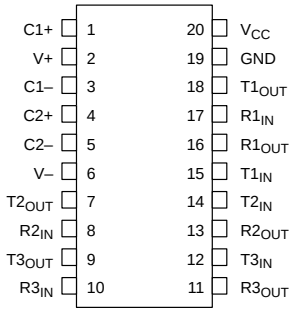
FEATURES

- Compatible with DS1229
- 5V operation
- 20–pin DIP or SOIC package
- 20–pin TSSOP package for height restricted applications
- Operate from single +5V power
- Meets all EIA–232E and V.28 specifications
- Uses small capacitors: 0.1 µF
- Optional industrial temperature range available (–40°C to +85°C)

ORDERING INFORMATION

DS229	20–pin DIP
DS229N	20–pin DIP (Industrial)
DS229S	20–pin SOIC
DS229SN	20–pin SOIC (Industrial)
DS229E	20–pin TSSOP
DS229EN	20–pin TSSOP (Industrial)

PIN ASSIGNMENT



20–PIN DIP, SOIC AND TSSOP

PIN DESCRIPTION

V_{CC}	– +5 Volt Supply
GND	– Ground
V+	– Positive Supply Output
V–	– Negative Supply Output
$T1_{IN}$, $T2_{IN}$, $T3_{IN}$	– RS–232 Driver Inputs
$T1_{OUT}$, $T2_{OUT}$, $T3_{OUT}$	– RS–232 Driver Outputs
$R1_{IN}$, $R2_{IN}$, $R3_{IN}$	– Receiver Inputs
$R1_{OUT}$, $R2_{OUT}$, $R3_{OUT}$	– Receiver Outputs
C1+, C1–	– Capacitor 1 Connections
C2+, C2–	– Capacitor 2 Connections

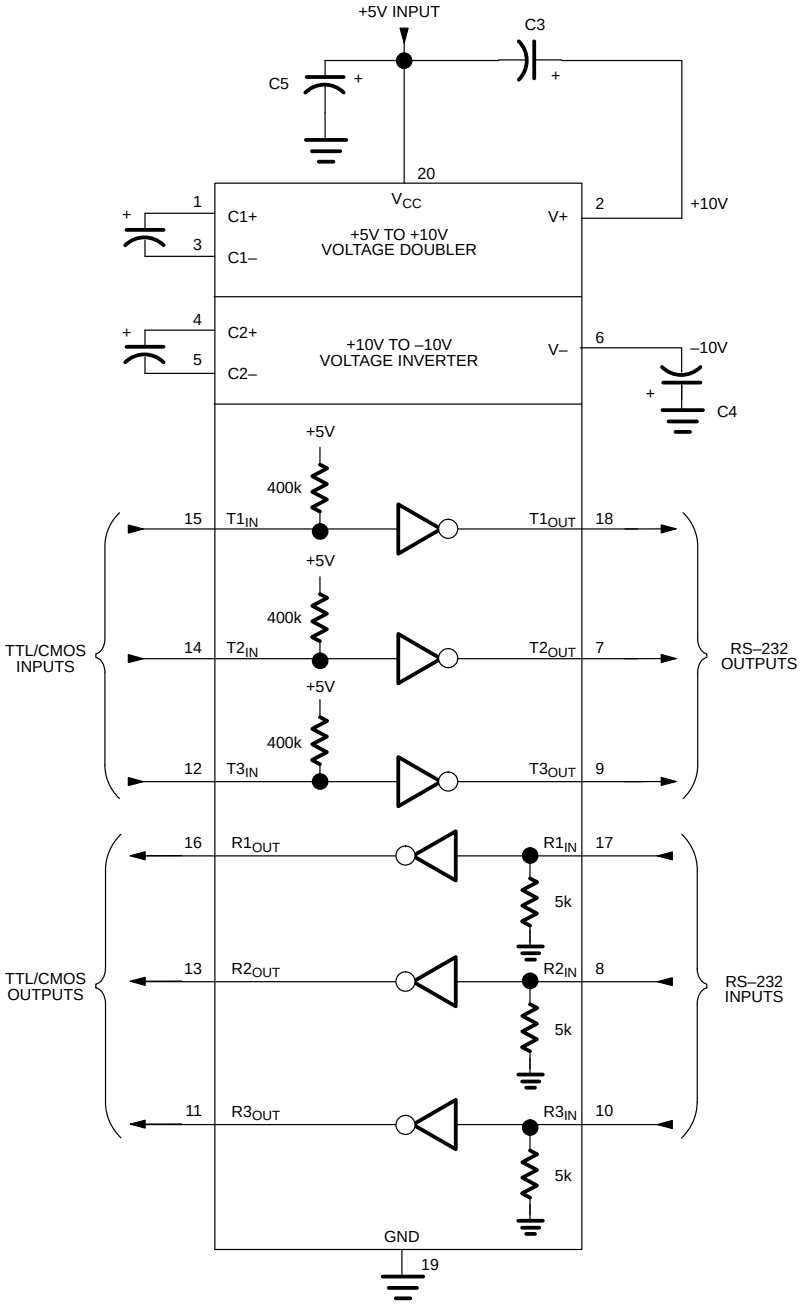
DESCRIPTION

The DS229 is a triple RS–232 driver/receiver pair that generates RS–232 voltage levels from a single +5 volt power supply. Additional ±12 volt supplies are not needed since the DS229 uses on–board charge pumps to convert the +5 volt supply to ±10 volts. The DS229 is fully compliant with EIA RS–232E and V.28/V.24 standards. The DS229 contains three drivers and three receivers. Driver slew rates and data rates are guaranteed up to 116 kbits/sec. The DS229 operates with only 0.1 µF charge pump capacitors.

OPERATION

The diagram in Figure 1 shows the main elements of the DS229. The following paragraphs describe the function of each pin.

FUNCTIONAL DIAGRAM OF DS229 Figure 1



NOTE: C5 is a recommended decoupling capacitor which is the same value as C1, C2, C3, and C4.

PIN DESCRIPTIONS

V_{CC}, GND: DC power is provided to the device on these pins. V_{CC} is the +5 volt input.

V+: Positive supply output (RS–232). V+ requires an external storage charge capacitor of at least 0.1 µF. A larger capacitor (up to 10 µF) can be used to reduce supply ripple.

V–: Negative supply output (RS–232). V– requires an external storage capacitor of at least 0.1 µF. A larger capacitor (up to 10 µF) can be used to reduce supply ripple.

$T1_{IN}$, $T2_{IN}$, $T3_{IN}$: Standard TTL/CMOS inputs for the RS–232 drivers. The inputs of unused drivers can be left unconnected since each input has a 400 kΩ pull–up resistor.

$T1_{OUT}$, $T2_{OUT}$, $T3_{OUT}$: Driver outputs at RS–232 levels. Driver output swing meets RS–232 levels for loads up to 3 kΩ. These driver outputs provide current necessary to meet RS–232 levels for loads up to 2500 pF.

$R1_{IN}$, $R2_{IN}$, $R3_{IN}$: Receiver inputs. These inputs accept RS–232 level signals (±25 volts) into a protected 5 kΩ terminating resistor. Each receiver provides 0.5V hysteresis (typical) for noise immunity.

$R1_{OUT}$, $R2_{OUT}$, $R3_{OUT}$: Receiver outputs at TTL/CMOS levels.

C1+, C1–, C2+, C2–: Charge pump capacitor inputs. These pins require two external capacitors (0.1 µF minimum, 10 µF maximum and should be the same size as C3 and C4). Capacitor 1 is connected between C1+ and C1–. Capacitor 2 is connected between C2+ and C2–. Capacitor C1 can be omitted if +12 volts is connected directly to V+. Likewise, C2 can be omitted if –12V is connected directly to V–.

DUAL CHARGE PUMP CONVERTERS

The DS229 has a two stage on–board charge pump circuit that is used to generate ±10 volts from a single +5 volt supply. In the first stage, capacitor C1 doubles the +5V supply to +10 volts which is then stored on capacitor C3. The second stage uses capacitor C2 to invert the +10V potential to –10V. This charge is then stored on capacitor C4. The ±10 volt supplies allow the DS229 to provide the necessary output levels for RS–232 communication. The DS229 will operate with charge pump capacitors as low as 0.1 µF. Larger capacitors (up to 10 µF) can be used to reduce supply ripple.

RS–232 DRIVERS

The three RS–232 drivers are powered by the internal ±10 volt supplies generated by the on–board charge pump. The driver inputs are both TTL and CMOS compatible. Each input has an internal 400 kΩ pull–up resistor so that unused transmitter inputs can be left unconnected. The open circuit output voltage swing is from (V+ – 0.6) to V– volts. Worst case conditions for EIA–232E/V.28 of ±5 volt driving a 3 kΩ load and 2500 pF are met at maximum operating temperature and V_{CC} equal to 4.5 volts. Typical voltage swings of ±8 volts occur when loaded with a nominal 5 kΩ RS–232 receiver. As required by EIA–232E and V.28 specifications, the slew rate at the output is limited to less than 30 volts/µs. Typical slew rates are 20 volts/µs unloaded and 12 volts/µs with 3 kΩ and 2500 pF load. These slew rates allow for bit rates of over 116 kbits/s. Driver outputs maintain high impedance when power is off.

RS–232 RECEIVERS

The three receivers conform fully to the RS–232E specifications. The input impedance is typically 5 kΩ and can withstand up to ±30 volts with or without V_{CC} applied. The input switching thresholds are within the ±3 volt limit of RS–232E specification with an input threshold low of 0.8 volts and an input threshold high of 2.4 volts. The receivers have 0.5 volts of hysteresis (typical) to improve noise rejection. The TTL/CMOS compatible outputs of the receivers will be low whenever the RS–232 input is greater than 2.4 volts. The receiver output will be high when the input is floating or driven between +0.8 volts and –25 volts.

ABSOLUTE MAXIMUM RATINGS*

Absolute Maximum Ratings

V_{CC}	–0.3V to +7.0V
V+	(V_{CC}–0.3V) to +14V
V–	+0.3V to –14V

Input Voltages

T_{IN}	–0.3V to (V_{CC}+0.3V)
R_{IN}	±30V

Output Voltages

T_{OUT}	(V+ + 0.3V) to (V– – 0.3V)
R_{OUT}	–0.3V to (V_{CC} + 0.3V)
Short Circuit Duration, T_{OUT}	Continuous

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Votlage	V_{CC}	4.5		5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current (No Load)	I_{CC1}		6	15	mA	
Power Supply Current (3 kΩ Load All Outputs)	I_{CC2}		22.5		mA	
RS–232 Transmitters						
Output Voltage Swing	V_{ORS}	±5	±8		V	2
Input Logic Threshold Low	V_{TTL}	0.8	1.4		V	
Input Logic Threshold High	V_{TTH}		1.4	2.0	V	
Data Rate	f_D		200	116	kbits/s	
Logic Pull–up/Input Current	I_{PU}		5	40	µA	
Transmitter Output Resistance	R_{OUT}	300	10M		Ω	3
Output Short–Circuit Current	I_{TSC}	±15	±30	±100	mA	4

DC ELECTRICAL CHARACTERISTICS (continued) (0°C to 70°C)

RS–232 Receivers						
RS–232 Input Voltage Operating Range	V_{IR}	±25	±30		V	
RS–232 Input Threshold Low	V_{RTL}	0.8	1.3		V	
RS–232 Input Threshold High	V_{RTH}		1.8	2.4	V	
RS–232 Input Hysteresis	V_{HY}	0.2	0.5	1	V	
RS–232 Input Resistance	R_{IN}	3	5	7	kΩ	
TTL/CMOS Output Voltage Low	V_{ROL}		0.2	0.4	V	5
TTL/CMOS Output Voltage High	V_{ROH}	3.5	V_{CC}–0.2		V	6
TTL/CMOS Output Short Circuit Current (V_{OUT}=GND)	I_{RSC}	–2	–10		mA	
TTL/CMOS Output Short Circuit Current (V_{OUT}=V_{CC})	I_{RSC}	10	30		mA	

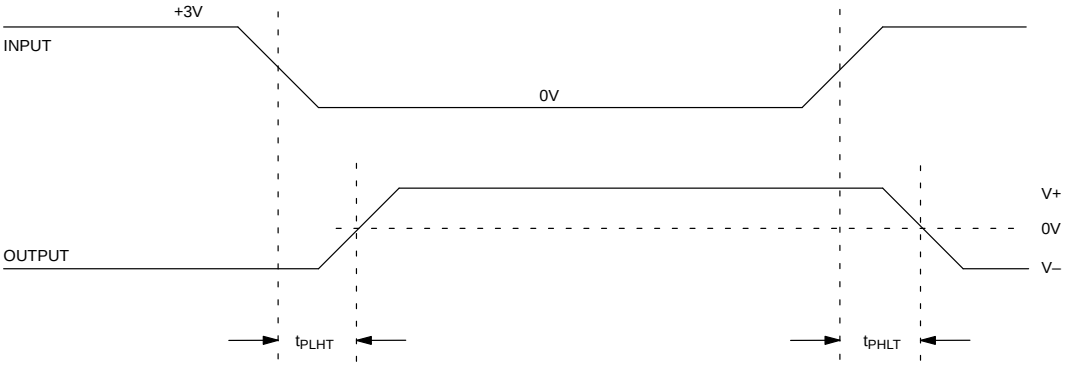
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C)

PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTES**
Transition Slew Rate	t_{SR}	6	12	30	V/µs	7
Transmitter Propagation Delay TTL to RS–232	t_{PHLT} t_{PLHT}		1.3 1.5	3.5 3.5	µs µs	
Receiver Propagation Delay RS–232 to TTL	t_{PHLR} t_{PLHR}		0.5 0.6	1 1	µs µs	
Transmitter + to – Propagation Delay Difference	t_{PHLT} $–t_{PLHT}$		300		ns	
Receiver + to – Propagation Delay Difference	t_{PHLR} $–t_{PLHR}$		100		ns	

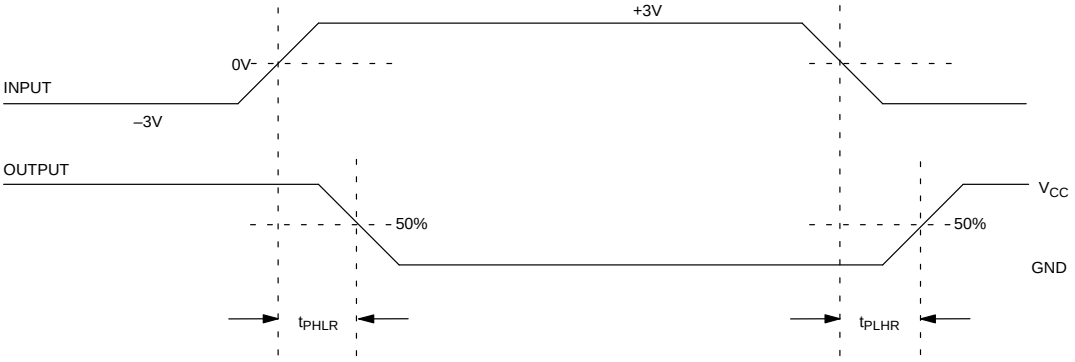
NOTES:

1. All voltages are referenced to ground.
2. All transmitter outputs loaded with 3 kΩ to ground.
3. V_{CC} = V+ = V– = 0V; V_{OUT} = ±2V .
4. V_{OUT} = 0V.
5. I_{OUT} = 3.2 mA.
6. I_{OUT} = –1.0 mA.
7. C_L = 50 pF – 2500 pF; RL = 3 kΩ – 7 kΩ; V_{CC} = 5V; TA = 25°C.

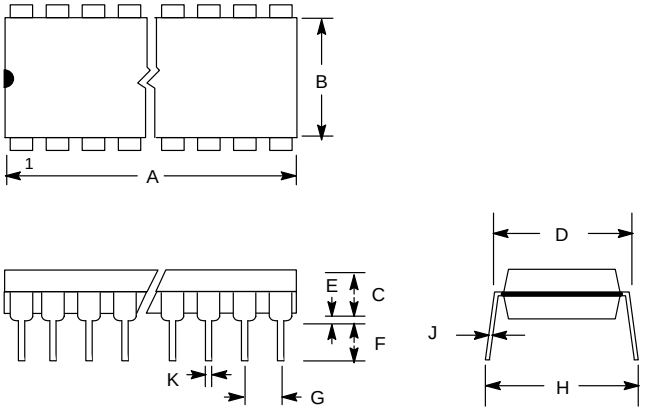
TRANSMITTER PROPAGATION DELAY TIMING Figure 2



RECEIVER PROPAGATION DELAY TIMING Figure 3

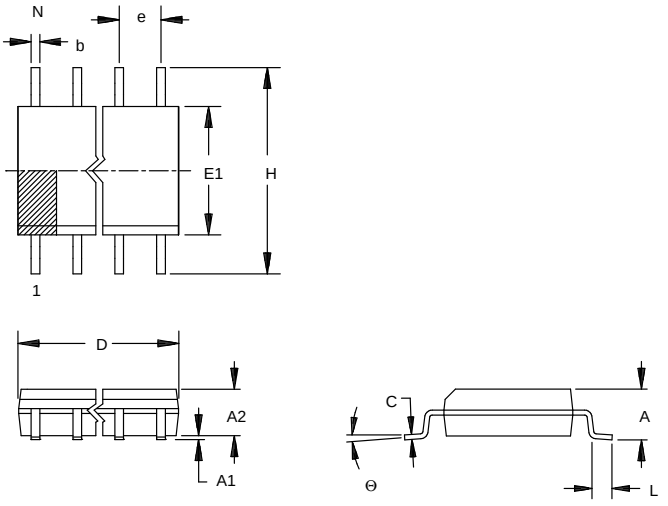


20–PIN DIP (300 MIL)



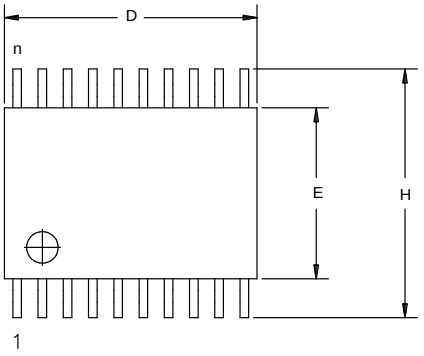
PKG	20-PIN	
DIM	**MIN**	**MAX**
A IN.	0.970	1.040
MM	24.63	26.42
B IN.	0.240	0.270
MM	6.09	6.86
C IN.	0.120	0.140
MM	3.05	3.56
D IN.	0.295	0.325
MM	7.49	8.26
E IN.	0.015	0.040
MM	0.38	1.02
F IN.	0.120	0.140
MM	3.04	3.56
G IN.	0.090	0.110
MM	2.23	2.79
H IN	0.310	0.390
MM	7.87	9.91
J IN	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

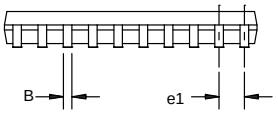
20–PIN SOIC (300 MIL)

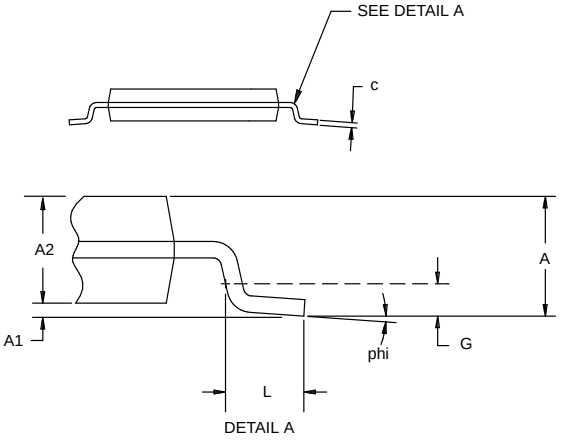


PKG	20–PIN	
DIM	MIN	MAX
A IN. MM	0.094 2.39	0.105 2.67
A1 IN. MM	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51
C IN. MM	0.009 0.229	0.013 0.33
D IN. MM	0.498 12.65	0.511 12.99
e IN. MM	0.050 BSC 1.27 BSC	
E1 IN MM	0.290 7.37	0.300 7.62
H IN MM	0.398 10.11	0.416 10.57
L IN. MM	0.016 0.40	0.040 1.02
Θ	0°	8°

20–PIN TSSOP







DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°