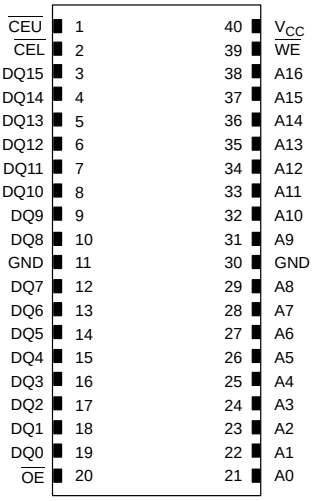
DALLAS SEMICONDUCTOR

DS1258Y/AB
128K x 16 Nonvolatile SRAM

FEATURES

- 10 year minimum data retention in the absence of external power
- Data is automatically protected during a power loss
- Separate upper byte and lower byte chip select inputs
- Unlimited write cycles
- Low–power CMOS
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% operating range (DS1258Y)
- Optional ±5% operating range (DS1258AB)

PIN ASSIGNMENT



40–PIN ENCAPSULATED PACKAGE
740 MIL EXTENDED

PIN DESCRIPTION

A0–A16	–	Address Inputs
DQ0–DQ15	–	Data In/Data Out
$\overline{CEU}$	–	Chip Enable Upper Byte
$\overline{CEL}$	–	Chip Enable Lower Byte
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
V_{CC}	–	Power Supply (+5V)
GND	–	Ground

DESCRIPTION

The DS1258 128K x 16 Nonvolatile SRAMs are 2,097,152–bit fully static, nonvolatile SRAMs, organized as 131,072 words by 16 bits. Each NV SRAM has a self contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out–of–tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. DIP–package DS1258 devices can be used in place of solutions which build nonvolatile 128K x 16 memory by utilizing a variety of discrete components. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing.

READ MODE

The DS1258 devices execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and either/both of $\overline{CEU}$ or $\overline{CEL}$ (Chip Enables) are active (low) and $\overline{OE}$ (Output Enable) is active (low). The unique address specified by the 17 address inputs (A0–A16) defines which of the 131,072 words of data is accessed. The status of $\overline{CEU}$ and $\overline{CEL}$ determines whether all or part of the addressed word is accessed. If $\overline{CEU}$ is active with $\overline{CEL}$ inactive, then only the upper byte of the addressed word is accessed. If $\overline{CEU}$ is inactive with $\overline{CEL}$ active, then only the lower byte of the addressed word is accessed. If both the $\overline{CEU}$ and $\overline{CEL}$ inputs are active (low), then the entire 16–bit word is accessed. Valid data will be available to the 16 data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CEU}$, $\overline{CEL}$ and $\overline{OE}$ access times are also satisfied. If $\overline{CEU}$, $\overline{CEL}$, and $\overline{OE}$ access times are not satisfied, then data access must be measured from the later occuring signal, and the limiting parameter is either t_{CO} for $\overline{CEU}$, $\overline{CEL}$, or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1258 devices execute a write cycle whenever $\overline{WE}$ and either/both of $\overline{CEU}$ or $\overline{CEL}$ are active (low) after address inputs are stable. The unique address specified by the 17 address inputs (A0–A16) defines which of the 131,072 words of data is accessed. The status of $\overline{CEU}$ and $\overline{CEL}$ determines whether all or part of the addressed word is accessed. If $\overline{CEU}$ is active with $\overline{CEL}$ inactive, then only the upper byte of the addressed word is accessed. If $\overline{CEU}$ is inactive with $\overline{CEL}$ active, then only the lower byte of the addressed word is accessed. If both the $\overline{CEU}$ and $\overline{CEL}$ inputs are active (low), then the entire 16–bit word is accessed. The write cycle is terminated by the earlier rising edge of $\overline{CEU}$ and/or $\overline{CEL}$, or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CEU}$ and/or $\overline{CEL}$, and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

READ/WRITE FUNCTION Table 1

$\overline{OE}$	$\overline{WE}$	$\overline{CEL}$	$\overline{CEU}$	V_{CC} CURRENT	DQ0–DQ7	DQ8–DQ15	CYCLE PERFORMED
H	H	X	X	I_{CCO}	High–Z	High–Z	Output Disabled
L	H	L	L	I_{CCO}	Output	Output	Read Cycle
L	H	L	H		Output	High–Z	
L	H	H	L		High–Z	Output	
X	L	L	L	I_{CCO}	Input	Input	Write Cycle
X	L	L	H		Input	High–Z	
X	L	H	L		High–Z	Input	
X	X	H	H	I_{CCS}	High–Z	High–Z	Output Disabled

DATA RETENTION MODE

The DS1258AB provides full functional capability for V_{CC} greater than 4.75 volts, and write protects by 4.5 volts. The DS1258Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power–up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for the DS1258AB and 4.5 volts for the DS1258Y.

FRESHNESS SEAL

The DS1258 devices are shipped from Dallas Semiconductor with the lithium energy sources disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A: 0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1258AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1258Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1258AB)
(t_A: 0°C to 70°C) (V_{CC}=5V ± 10% for DS1258Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	–2.0		+2.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	–1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	–1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CEU}$, $\overline{CEL}$=2.2V	I_{CCS1}		10	20	mA	
Standby Current $\overline{CEU}$, $\overline{CEL}$=V_{CC} – 0.5V	I_{CCS2}		6	10	mA	
Operating Current	I_{CCO1}			170	mA	
Write Protection Voltage (DS1258AB)	V_{TP}	4.50	4.62	4.75	V	
Write Protection Voltage (DS1258Y)	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE

(t_A = 25°C)

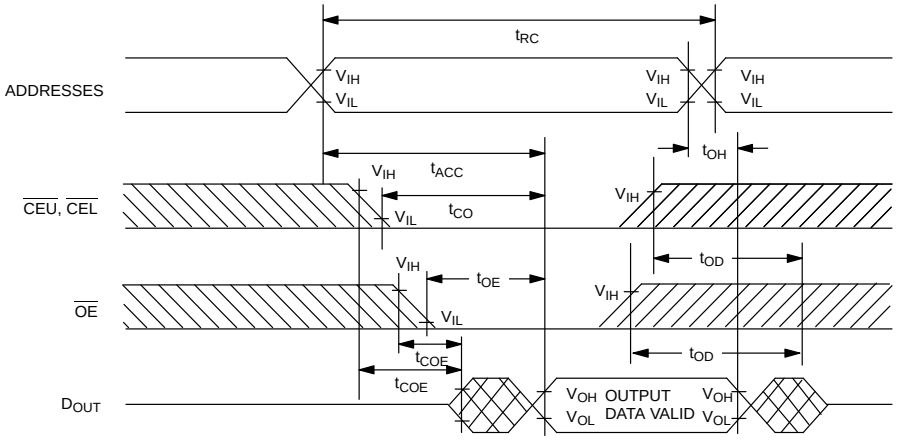
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		20	25	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 5% for DS1258AB)
(t_A: 0°C to 70°C) (V_{CC}=5V ± 10% for DS1258Y)

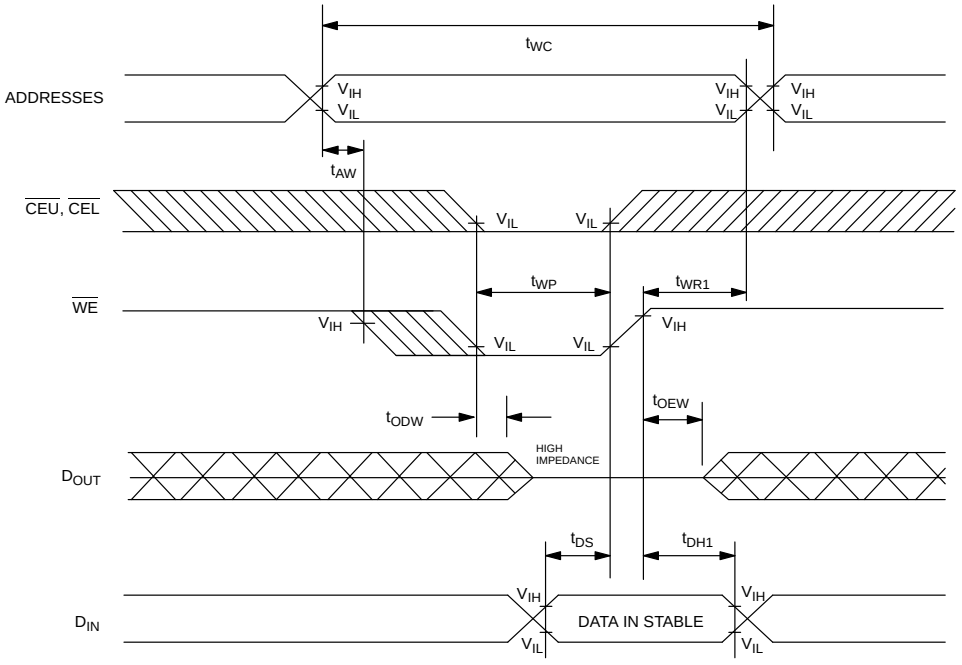
PARAMETER	SYMBOL	DS1258AB–70 DS1258Y–70		DS1258AB–100 DS1258Y–100		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		100		ns	
Access Time	t_{ACC}		70		100	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35		50	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70		100	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		100		ns	
Write Pulse Width	t_{WP}	55		75		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 15		5 15		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		25		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		40		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		ns ns	12 13

READ CYCLE



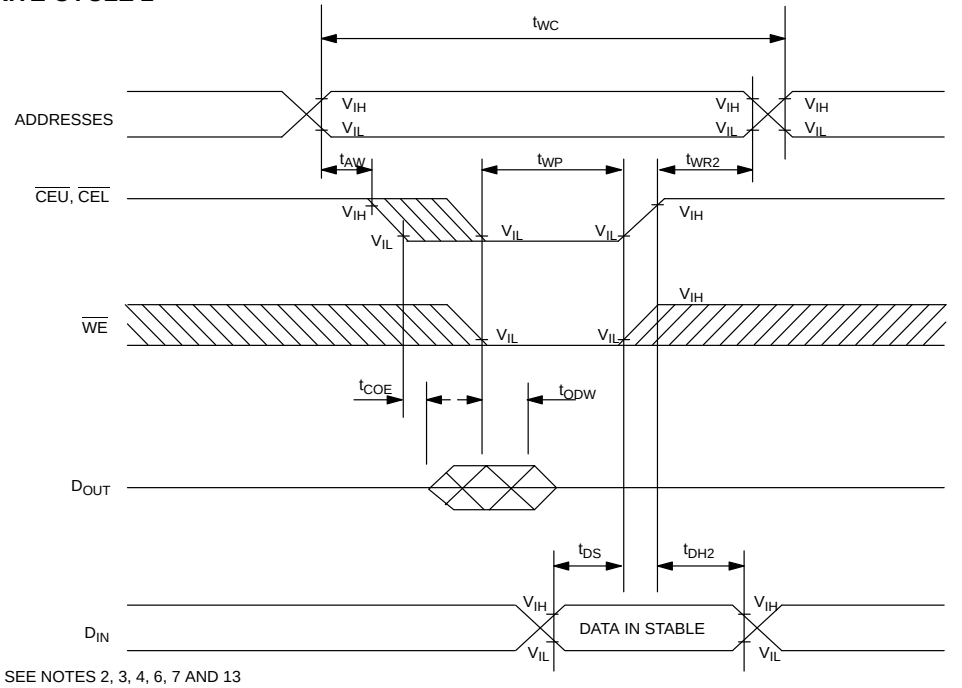
SEE NOTE 1

WRITE CYCLE 1



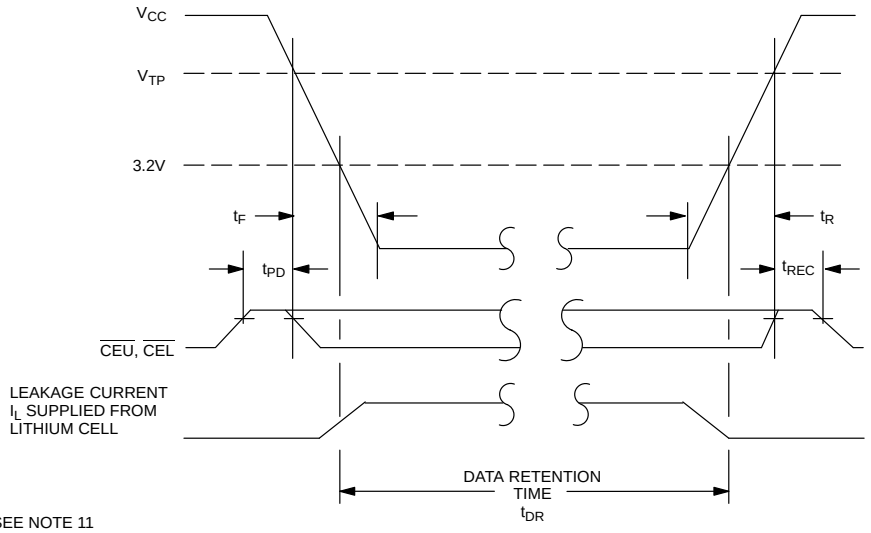
SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7 AND 13

POWER–DOWN/POWER–UP CONDITION



POWER–DOWN/POWER–UP TIMING

(t_A: 0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CEU}$, $\overline{CEL}$ at V_{IH} before Power–Down	t_{PD}	0			µs	11
V_{CC} Slew from V_{TP} to 0V	t_F	300			µs	
V_{CC} Slew from 0V to V_{TP}	t_R	300			µs	
$\overline{CEU}$, $\overline{CEL}$ or at V_{IH} after Power–Up	t_{REC}	2		125	ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CEU}$ or $\overline{CEL}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CEU}$, $\overline{CEL}$ or $\overline{WE}$ going low to the earlier of $\overline{CEU}$, $\overline{CEL}$ or $\overline{WE}$ going high.

4. t_{DS} is measured from the earlier of $\overline{CEU}$ or $\overline{CEL}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CEU}$ or $\overline{CEL}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in the output buffers remain in a high impedance state during this period.
7. If the $\overline{CEU}$ or $\overline{CEL}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CEU}$ or $\overline{CEL}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1258 has a built–in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range 0°C to 70°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2}, t_{DH2} are measured from $\overline{CEU}$ OR $\overline{CEL}$ going high.

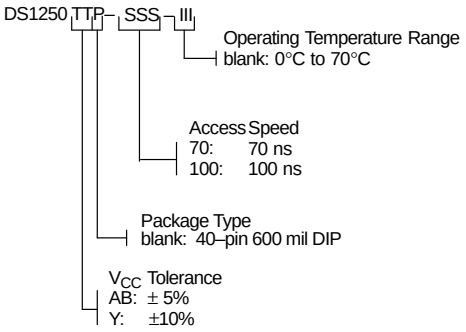
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns
All voltages are referenced to ground

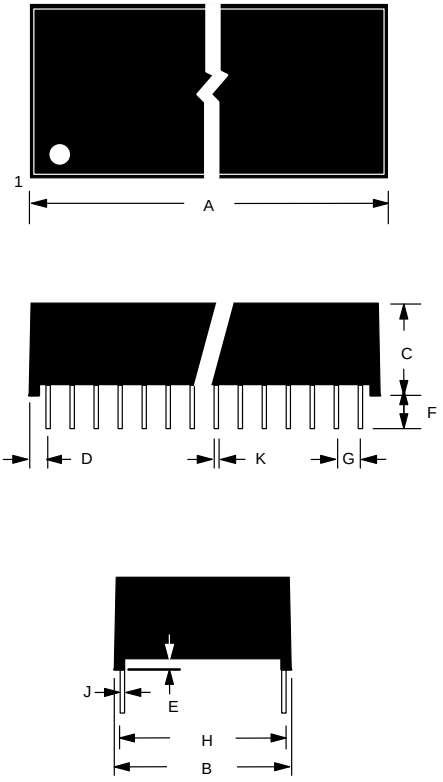
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels:
0.0 to 3.0 volts
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

ORDERING INFORMATION



DS1258Y/AB NONVOLATILE SRAM 40–PIN 740 MIL EXTENDED MODULE



PKG	40–PIN	
DIM	MIN	MAX
A IN. MM	2.080 52.83	2.100 53.34
B IN. MM	0.715 18.16	0.740 18.80
C IN. MM	0.345 8.76	0.365 9.27
D IN. MM	0.085 2.16	0.115 2.92
E IN. MM	0.015 0.38	0.030 0.76
F IN. MM	0.120 3.05	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.43	0.025 0.58