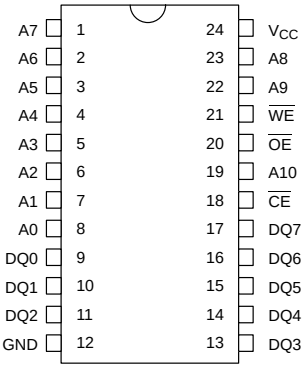
DALLAS SEMICONDUCTOR

DS2016
2K x 8 3V/5V Operation Static RAM

FEATURES

- Low power CMOS design
- Standby current
  - 50 nA max at t_A = 25°C V_{CC} = 3.0V
  - 100 nA max at t_A = 25°C V_{CC} = 5.5V
  - 1 µA max at t_A = 60°C V_{CC} = 5.5V
- Full operation for V_{CC} = 5.5V to 2.7V
- Data Retention Voltage = 5.5V to 2.0V
- Fast 5V access time
  - DS2016 – 100 100 ns
  - DS2016 – 150 150 ns
- Reduced–speed 3V access time
  - DS2016 – 100 250 ns
  - DS2016 – 150 250 ns
- Operating temperature range of –40°C to +85°C
- Full static operation
- TTL compatible inputs and outputs over voltage range of 5.5V to 2.7 volts.
- Available in 24–pin DIP and 24–pin SOIC packages
- Suitable for both battery operate and battery backup applications

PIN ASSIGNMENT



DS2016 24–PIN DIP (600 MIL)
DS2016S 24–PIN SOIC (330 MIL)

PIN DESCRIPTION

A0 – A10	–	Address Inputs
DQ0 – DQ7	–	Data Input/Output
$\overline{CE}$	–	Chip Enable Input
$\overline{WE}$	–	Write Enable Input
$\overline{OE}$	–	Output Enable Input
V_{CC}	–	Power Supply Input 2.7V – 5.5V
GND	–	Ground

DESCRIPTION

The DS2016 is a 16,384–bit, low–power, fully static random access memory organized as 2048 words by 8–bits using CMOS technology. The device operates from a single power supply with a voltage input between 2.7 and 5.5 volts. The chip enable input ($\overline{CE}$) is used for device selection and can be used in order to achieve the minimum standby current mode, which facilitates both battery operate and battery backup applications. The device provides access times as fast as 100 ns when operated from a 5 volt power supply input, and also provides relatively good performance of 250 ns access while operating from a 3 volt input. The device maintains TTL–level inputs and outputs over the input voltage range of 2.7 to 5.5 volts. The DS2016 is most suitable for low power applications where battery operation or battery backup for nonvolatility are required. The DS2016 is a JEDEC–standard 2K x 8 SRAM and is pin-compatible with ROM and EPROM of similar density.

OPERATION MODE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0–A10	DQ–DQ7	POWER
READ	L	L	H	STABLE	DATA OUT	I_{CCO}
WRITE	L	X	L	STABLE	DATA IN	I_{CCO}
DESELECT	L	H	H	X	HIGH–Z	I_{CCO}
STANDBY	H	X	X	X	HIGH–Z	I_{CCS}

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING
V_{CC}	Power Supply Voltage	–0.3V to +7.0V
V_{IN}, $V_{I/O}$	Input, Input/Output Voltage	–0.3 to V_{CC} + 0.3V
T_{STG}	Storage Temperature	–55°C to +125°C
T_{OPR}	Operating Temperature	–40°C to +85°C
T_{SOLDER}	Soldering Temperature/Time	260°C for 10 seconds

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	12	pF	

+5 VOLT OPERATION

RECOMMENDED DC OPERATING CONDITIONS

(t_A = –40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	–0.3		0.8	V	
Data Retention Voltage	V_{DR}	2.0		5.5	V	

DC CHARACTERISTICS

(t_A = –40°C to +85°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	$0V \le V_{IN} \le V_{CC}$			±0.1	µA
I/O Leakage Current	I_{LO}	$\overline{CE}=V_{IH}$, $0V \le V_{IO} \le V_{CC}$			±0.5	µA
Output High Current	I_{OH}	V_{OH} = 2.4V	–1.0			mA
Output Low Current	I_{OL}	V_{OL} = 0.4V	4.0			mA
Standby Current	I_{CCS1}	$\overline{CE}$ = 2.0V			0.3	mA
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.5V t_A=60°C			1	µA
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.5V t_A=25°C			100	nA
Operating Current	I_{CCO}	$\overline{CE}$=0.8V, 200 ns cycle			55	mA

AC CHARACTERISTICS READ CYCLE

(t_A = –40°C to +85°C; V_{CC} = 5V ± 10%)

		DS2016–100			DS2016–150				
PARAMETER	SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	100			150			ns	
Access Time	t_{ACC}			100			150	ns	
$\overline{OE}$ to Output Valid	t_{OE}			50			70	ns	
$\overline{CE}$ to Output Valid	t_{CO}			100			150	ns	
$\overline{CE}$ or $\overline{OE}$ to Output Active	t_{COE}	5			5			ns	
Output High–Z from Deselection	t_{OD}	5		35	10		60	ns	
Output Hold from Address Change	t_{OH}	5			10			ns	

AC CHARACTERISTICS WRITE CYCLE

(t_A = –40°C to +85°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	DS2016–100			DS2016–150			UNITS	NOTES
		MIN	TYP	MAX	MIN	TYP	MAX		
Write Cycle Time	t_{WC}	100			150			ns	
Write Pulse Width	t_{WP}	75			120			ns	
Address Setup Time	t_{AW}	0			0			ns	
Write Recovery Time	t_{WR}	10			10			ns	
Output High–Z from $\overline{WE}$	t_{ODW}			35			70	ns	
Output Active from $\overline{WE}$	t_{OEW}	5			5			ns	
Data Setup Time	t_{DS}	40			60			ns	
Data Hold Time	t_{DH}	0			0			ns	

DATA RETENTION CHARACTERISTICS

(t_A = –40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Supply Voltage	V_{DR}	$\overline{CE} \geq V_{CC} - 0.5V$	2.0		5.5	V
Data Retention Current at 5.5V	I_{CCR1}	$\overline{CE} \geq V_{CC} - 0.5V$		0.1*	1	µA
Data Retention Current at 2.0V	I_{CCR2}	$\overline{CE} \geq V_{CC} - 0.5V$		50*	750	nA
Chip Deselect to Data Retention	t_{CDR}		0			µs
Recovery Time	t_R		2			ms

* Typical values are at 25°C

+3 VOLT OPERATION

RECOMMENDED DC OPERATING CONDITIONS

(t_A = –40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	2.7	3.0	3.5	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	–0.3		0.6	V	
Data Retention Voltage	V_{DR}	2.0		3.5	V	

DC CHARACTERISTICS

(t_A = –40°C to +85°C; V_{CC} = 2.7V to 3.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	$0V \le V_{IN} \le V_{CC}$			±0.1	µA
I/O Leakage Current	I_{LO}	$\overline{CE}=V_{IH}$, $0V \le V_{IO} \le V_{CC}$			±0.5	µA
Output High Current	I_{OH}	V_{OH} = 2.2V	–0.5			mA
Output Low Current	I_{OL}	V_{OL} = 0.4V	4.0			mA
Standby Current	I_{CCS1}	$\overline{CE}$ = 2.0V			0.1	mA
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.3V t_A=60°C			500	nA
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.3V t_A=25°C			50	nA
Operating Current	I_{CCO}	$\overline{CE}$=0.6V min cycle			25	mA

AC CHARACTERISTICS READ CYCLE

(t_A = –40°C to +85°C; V_{CC} = 2.7V to 3.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
Access Time	t_{ACC}			250	ns	
$\overline{OE}$ to Output Valid	t_{OE}			120	ns	
$\overline{CE}$ to Output Valid	t_{CO}			250	ns	
$\overline{CE}$ or $\overline{OE}$ to Output Active	t_{COE}	15			ns	
Output High–Z from Deselection	t_{OD}	5		100	ns	
Output Hold from Address Change	t_{OH}	15			ns	

AC CHARACTERISTICS WRITE CYCLE

(t_A = –40°C to +85°C; V_{CC} = 2.7V to 3.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	190			ns	
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	25			ns	
Output High–Z from $\overline{WE}$	t_{ODW}			90	ns	
Output Active from $\overline{WE}$	t_{OEW}	5			ns	
Data Setup Time	t_{DS}	100			ns	
Data Hold Time	t_{DH}	0			ns	

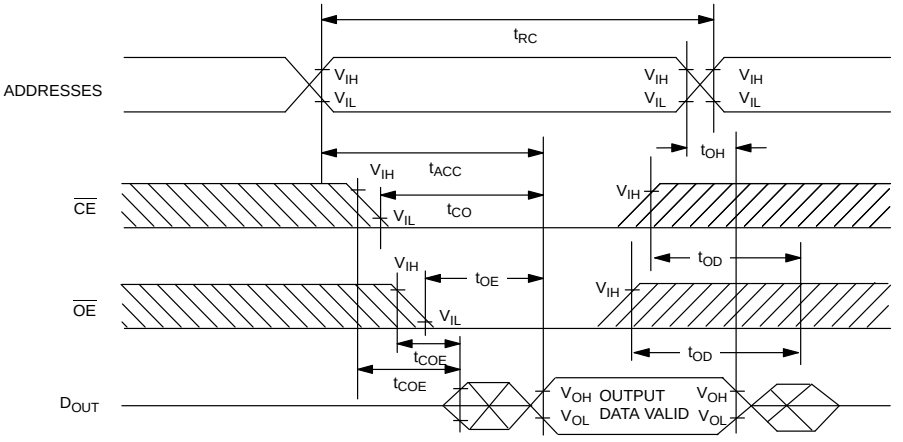
DATA RETENTION CHARACTERISTICS

(t_A = –40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Supply Voltage	V_{DR}	$\overline{CE} \geq V_{CC} - 0.3V$	2.0		3.5	V
Data Retention Current at 3.5V	I_{CCR1}	$\overline{CE} \geq V_{CC} - 0.3V$		50*	1000	nA
Data Retention Current at 2.0V	I_{CCR2}	$\overline{CE} \geq V_{CC} - 0.3V$		50*	750	nA
Chip Deselect to Data Retention	t_{CDR}		0			µs
Recovery Time	t_R		2			ms

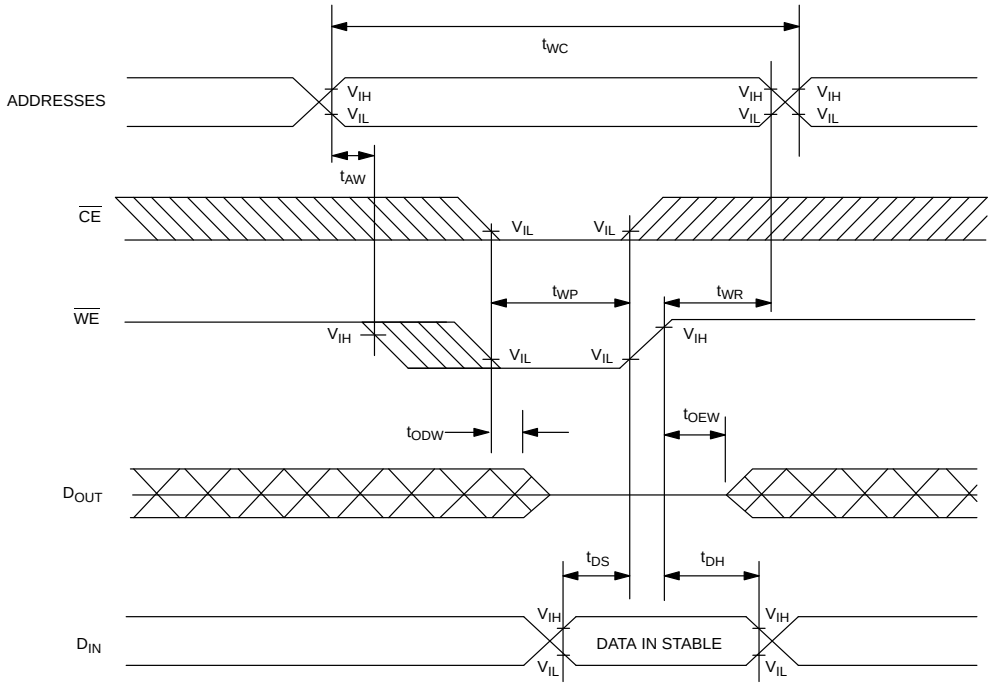
* Typical values are at 25°C

TIMING DIAGRAM: READ CYCLE



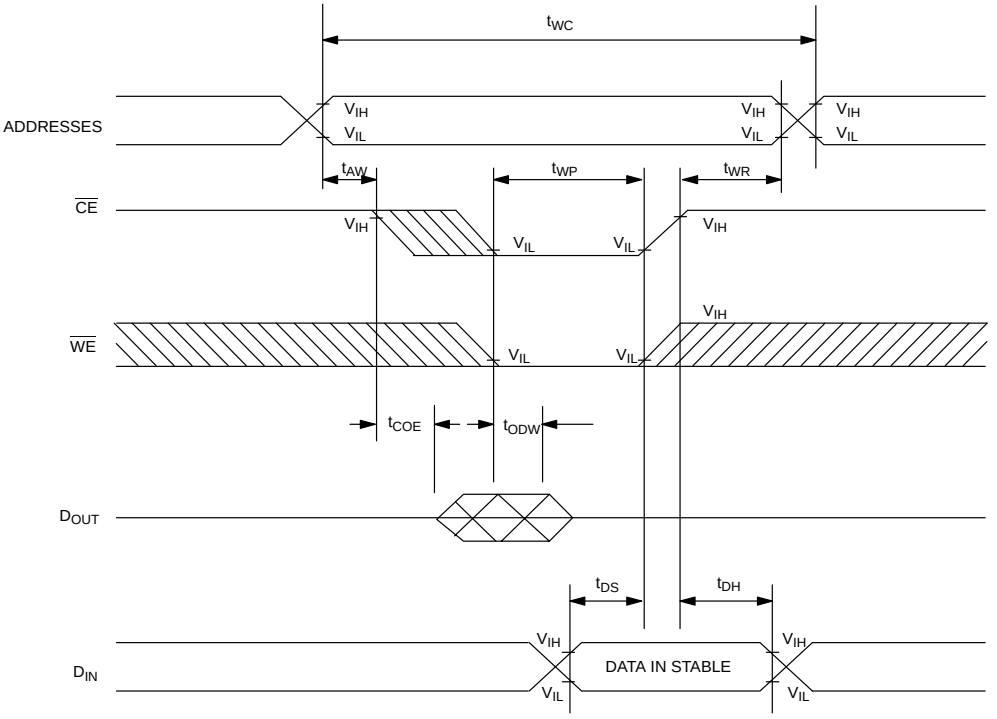
SEE NOTE 1

TIMING DIAGRAM: WRITE CYCLE 1



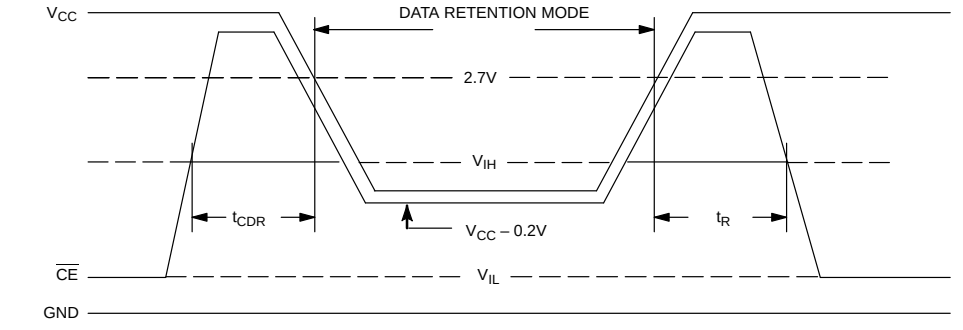
SEE NOTES 2, 3, 4, 5, 6 AND 7

TIMING DIAGRAM: WRITE CYCLE 2



SEE NOTES 2, 3, 4, 5, 6 AND 7

TIMING DIAGRAM: DATA RETENTION – POWER UP, POWER DOWN Figure 1



SEE NOTE 8

NOTES:

1. $\overline{WE}$ is high for read cycles.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH} and t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
6. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state.
7. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state.
8. If the V_{IH} level of $\overline{CE}$ is 2.0V during the period that V_{CC} voltage is going down from 4.5V to 2.7V, I_{CCS1} current flows.
9. The DS2016 maintains full operation from 5.5V to 2.7V. The electrical characteristics tables show two tested and guaranteed points of operation. For operation between 4.5V and 3.5 volts, used the composite worst case characteristics from both 5V and 3V operation for design purposes.

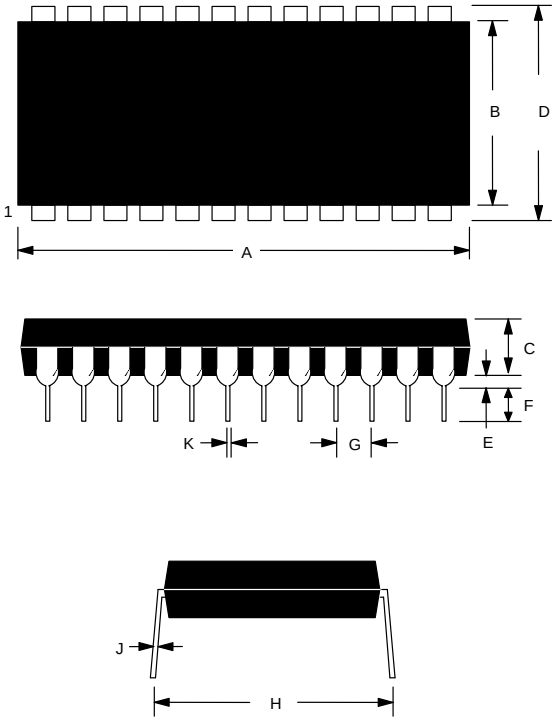
DC TEST CONDITIONS

Outputs Open
All voltages are referenced to ground.

AC TEST CONDITIONS

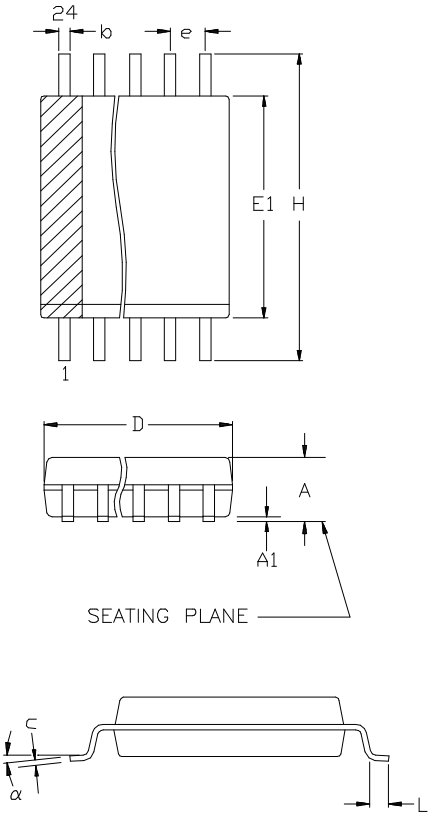
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0V – 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

DS2016 24–PIN DIP



PKG	24-PIN	
DIM	MIN	MAX
A IN.	1.245	1.270
MM	31.62	32.25
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.050
MM	0.380	1.27
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.56

DS2016S 24–PIN SOIC



PKG	24-PIN	
DIM	MIN	MAX
A IN. MM	0.080 2.04	0.120 3.05
A1 IN. MM	0.002 0.05	0.014 0.35
b IN. MM	0.012 0.30	0.020 0.50
C IN MM	0.004 0.10	0.0125 0.32
D IN. MM	0.595 15.1	0.634 16.1
e IN. MM	0.050 BSC 1.27 BSC	
E1 IN. MM	0.324 8.23	0.350 8.90
H IN MM	0.453 11.5	0.500 12.7
L IN MM	0.016 0.40	0.051 1.30
α	0°	10°

The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that 1/2 or more of its area is contained in the hatched zone.