SECTION 3: ARCHITECTURE

The High–Speed Microcontroller is based on the industry standard 80C52. The core is an accumulator based architecture using internal registers for data storage and peripheral control. It executes the standard 8051 instruction set. This section provides a brief description of each architecture feature. Details concerning the programming model, instruction set, and register descriptions are provided in Section 4.

ALU

The ALU is responsible for math functions, comparisons, and general decision making in the High–Speed Microcontroller. The ALU is not explicitly used by software. Instruction decoding prepares the ALU automatically and passes it the appropriate data. The ALU primarily uses two special function registers (SFRs) as the source and destination for all operations. These are the Accumulator and B register. The ALU also provides status information in the Program Status Register. The SFRs are described below.

SPECIAL FUNCTION REGISTERS

All peripherals and operations that are not explicit instructions in the High–Speed Microcontroller are controlled via Special Function Registers (SFRs). All SFRs are described in Section 4. The most commonly used registers that are basic to the architecture are also described below.

Accumulator

The Accumulator is the primary register used in the High–Speed Microcontroller. It is the source and destination of most math, data movement, decisions, and other operations. Although it can be bypassed, most high–speed instructions require the use of the Accumulator (ACC) as one argument.

B Register

The B register is used as the second 8–bit argument in multiply and divide operations. When not used for these purposes, the B register can be used as a general purpose register.

Program Status Word

The Program Status Word holds a selection of bit flags that include the Carry Flag, Auxiliary Carry Flag, General Purpose Flag, Register Bank Select, Overflow Flag, and Parity Flag.

Data Pointer(s)

The Data Pointer is used to designate a memory address for the MOVX instruction. This address can point to a MOVX RAM location, either on– or off–chip, or a memory mapped peripheral. When moving data from one memory area to another or from memory to a memory mapped peripheral, a pointer is needed for both the source and destination. Thus, the High–Speed Microcontroller offers two data pointers. The user selects the active pointer via a dedicated SFR bit.

Stack Pointer

The High–Speed Microcontroller provides a Stack in the scratchpad RAM area discussed below. The Stack Pointer denotes the register location at the top of the Stack, which is the last used value. The user can place the Stack anywhere in scratchpad RAM by setting the Stack Pointer to that location.

I/O Ports

The standard High–Speed Microcontroller offers four 8–bit I/O ports. ROMless versions use Port 0 and Port 2 as address and data busses. In those versions, only two ports are available for general purpose I/O. Each I/O port is a Special Function Register that can be written or read. The I/O port has a latch that retains the value which software writes. In general, during a read operation, software reads the state of the external pin. Each port is represented by an SFR location.

Timer/Counters

Three 16–bit Timer/Counters are available in the High–Speed Microcontroller. Each timer is contained in two SFR locations that can be written or read by software. The timers are controlled by other SFRs described in Section 4.

UARTs

The High–Speed Microcontroller provides one or two UARTs. These are controlled and accessed as SFRs. Each UART has an address that is used to read or write the UART. The same address is used for both read and write operations. The microcontroller distinguishes between a read and a write by the instruction. Each UART is controlled by its own SFR control register.

SCRATCHPAD REGISTERS (RAM)

The High–Speed Core provides 256 bytes of Scratchpad RAM for general purpose data and variable storage. The first 128 bytes are directly available to software. The second 128 are available through indirect addressing discussed below. Selected portions of this RAM have other optional functions.

Stack

The stack is a RAM area that the microcontroller uses to store return address information during Calls and Interrupts. The user can also place variables on the stack when necessary. The Stack Pointer mentioned above designates the RAM location that is the top of the stack. Thus, depending on the value of the Stack Pointer, the stack can be located anywhere in the 256 bytes of RAM. A common location would be in the upper 128 bytes of RAM, as these are accessible through indirect addressing only.

Working Registers

The first thirty two bytes of the Scratchpad RAM can be used as four banks of eight Working Registers for high speed data movement. Using four banks, software can quickly change context by simply changing to a different bank. In addition to the Accumulator, the Working Registers are commonly used as a data source or destination. Some of the Working Registers can also be used as pointers to other RAM locations (indirect addressing).

PROGRAM COUNTER

The Program Counter (PC) is a 16–bit value that designates the next program address to be fetched. On–chip hardware automatically increments the PC value to move to the next ROM location.

ADDRESS/DATA BUS

The High–Speed Microcontroller addresses a 64KB program and 64KB data memory area. In the ROMless versions, all memory is outside. Other versions use a combination of internal and external memory. When external memory is accessed, Ports 0 and 2 are used as a multiplexed address and data bus. Port 2 provides the address MSB. Even versions with internal memory can use the bus on Ports 0 and 2 to access more memory.

WATCHDOG TIMER

The Watchdog Timer provides a supervisory function for applications that cannot afford to run out of control. The Watchdog Timer is a programmable free running timer. If allowed to reach the termination of its count, if enabled, the Watchdog will reset the CPU. Software must prevent this by clearing or resetting the Watchdog prior to its time–out.

POWER MONITOR

Some members of the High–Speed Microcontroller family incorporate a band–gap reference and analog circuitry to monitor the power supply conditions. If V_{CC} begins to drop out of tolerance, the Power Monitor will issue an optional early warning Power–fail Interrupt. If power continues to fall, the Power Monitor will invoke a reset condition. This will remain until power returns to normal operating voltage. The Power Monitor also functions on power up, holding the microcontroller in a reset state until power is stable.

INTERRUPTS

The High–Speed Microcontroller is capable of evaluating a number of interrupt sources simultaneously. Each version of the High–Speed Microcontroller provides a different number of interrupt sources. Each interrupt has an associated interrupt vector, flag, priority, and enable. These interrupts can be globally enabled or disabled.

TIMING CONTROL

The High–Speed Microcontroller provides an on–chip oscillator for use with an external crystal. This can be bypassed by injecting a clock source into the XTAL1 pin. The clock source is used to create machine cycle timing (four clocks), ALE, $\overline{PSEN}$, Watchdog, Timer, and serial baud rate timing. In addition, some devices incorporate an on–chip ring oscillator which can be used to provide an approximately 2–4 MHz clock source.

REAL–TIME CLOCK

The DS87C530 incorporates a real–time clock (RTC), which is accessed via SFR locations. The RTC is divided into hour, minute, second, and subsecond registers, and also incorporates a 65536 day calendar. Alarm registers allow the RTC to issue interrupts at a specific time once per day, or as a recurring alarm every hour, minute, or second. An external watch crystal and lithium power source allow the processor to maintain timekeeping in the absence of V_{CC}.

FEATURE SUMMARY

The High–Speed Microcontroller family offers a combination of features and peripherals as shown in Table 3–1. This User's Guide is designed as a comprehensive guide covering all the features available in the High–Speed Microcontroller family. The designer should investigate the specific data sheet to determine which features are available on a particular device.

PRODUCT FEATURE MATRIX 3–1

FEATURE	DS80C310	DS80C320	DS80C323	DS83C520	DS87C520	DS87C530
Internal Program ROM				16KB Mask ROM	16KB EPROM	16KB EPROM
Internal Scratchpad RAM	256 bytes	256 bytes	256 bytes	256 bytes	256 bytes	256 bytes
Internal MOVX SRAM				1KB SRAM	1KB SRAM	1KB SRAM
Serial Ports	1	2	2	2	2	2
External Interrupts	6	6	6	6	6	6
16–bit Timers	3	3	3	3	3	3
Watchdog Timer		✓	✓	✓	✓	✓
Power–fail/Precision Reset		✓	✓	✓	✓	✓
Power–Fail Interrupt		✓	✓	✓	✓	✓
Data Pointers	2	2	2	2	2	2
Power Management Modes				✓	✓	✓
Ring Oscillator		✓	✓	✓	✓	✓
EMI Reduction Mode				✓	✓	✓
Real–Time Clock						✓
Nonvolatile SRAM						✓
Operating Voltage	4.5V–5.5V	4.5V–5.5V	2.7V–5.5	4.5V–5.5V	4.5V–5.5V	4.5V–5.5V