SECTION 4: PROGRAMMING MODEL

This section provides a programmer's overview of the High–Speed Microcontroller core. It includes information on the memory map, on–chip RAM, Special Function Registers (SFRs), and instruction set. The programming model of the High–Speed Microcontroller is very similar to that of the industry standard 80C52. The memory map is identical. It uses the same instruction set, though instruction timing is improved. Several new SFRs have been added.

MEMORY ORGANIZATION

The High–Speed Microcontroller, like the 8052, uses several distinct memory areas. These are Registers, program memory, and data memory. Registers serve to control on–chip peripherals and as RAM. Note that Registers (on–chip RAM) are separate from data memory. Registers are divided into three categories including directly addressed on–chip RAM, indirectly addressed on–chip RAM, and Special Function Registers. The program and data memory areas are discussed under Memory Map. The Registers are discussed under Register Map.

MEMORY MAP

The High–Speed Microcontroller uses a memory addressing scheme that separates program memory (ROM) from data memory (RAM). Each area is 64KB beginning at address 0000h and ending at FFFFh as shown in Figure 4–1. The program and data segments can overlap since they are accessed in different ways. Program memory is fetched by the microcontroller automatically. These addresses are never written by software. In fact, there are no instructions that allow the ROM area to be written. There is one instruction (MOVC) that is used to explicitly read the program area. This is commonly used to read look–up tables. The data memory area is accessed explicitly using the MOVX instruction. This instruction provides multiple ways of specifying the target address. It is used to access the 64KB of data memory.

The address and data range of devices with on–chip program and data memory overlap the 64K memory space. When on–chip memory is enabled, accessing memory in the on–chip range will cause the device to access internal memory. Memory accesses beyond the internal range will be addressed externally via ports 0 and 2.

The ROMSIZE feature allows software to dynamically configure the maximum address of on–chip program memory. This allows the device to act as a bootstrap loader for an external Flash or nonvolatile SRAM. Secondly, this method can also be used to increase the amount of available program memory from 64KB to 80KB without bank switching. For more information on this feature, please consult Section 6.

Program and data memory can also be increased beyond the 64KB limit using bank switching techniques. This is described in Application Note 81, Memory Expansion with the High–Speed Microcontroller family.

REGISTER MAP

The Register Map is illustrated in Figure 4–2. It is entirely separate from the program and data memory areas mentioned above. A separate class of instructions is used to access the registers. There are 256 potential register location values. In practice, the High–Speed Microcontroller has 256 bytes of Scratchpad RAM and up to 128 Special Function Registers (SFRs). This is possible since the upper 128 Scratchpad RAM locations can only be accessed indirectly. That is, the contents of a Working Register (described below) will designate the RAM location. Thus a direct reference to one of the upper 128 locations must be an SFR access. Direct RAM is reached at locations 0 to 7Fh (0 to 127). SFRs are accessed directly between 80h and FFh (128 to 255). The RAM locations between 128 and 255 can be reached through an indirect reference to those locations.

Scratchpad RAM is available for general purpose data storage. It is commonly used in place of off–chip RAM when the total data contents are small. When off–chip RAM is still needed, the Scratchpad area will still provide the fastest general purpose access. Within the 256 bytes of RAM, there are several special purpose areas. These are described as follows.

Bit Addressable Locations

In addition to direct register access, some individual bits are also accessible. There are individually addressable bits in both the RAM and SFR area. In the Scratchpad RAM area, registers 20h to 2Fh are bit addressable. This provides 128 (16 * 8) individual bits available to software. A bit access is distinguished from a full register access by the type of instruction. Addressing modes

are discussed in Section 5. In the SFR area, any register location ending in a 0 or 8 is bit addressable. Figure 4–3 shows details of the on–chip RAM addressing including the locations of individual RAM bits.

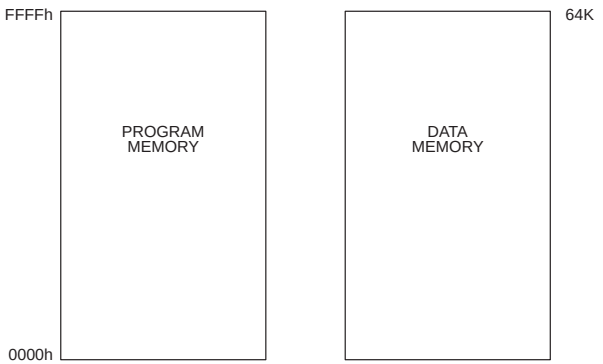
Working Registers

As part of the lower 128 bytes of RAM, there are four banks of eight Working Registers (each). The Working Registers are general purpose RAM locations that can be addressed in a special way. They are designated R0 through R7. Since there are four banks, the currently selected bank will be used by any instruction using R0–R7. This allows software to change context by simply switching banks. This is controlled via the Program Status Word register in the SFR area described below. The Working Registers also allow their contents to be used for indirect addressing of the upper 128 bytes of RAM. Thus an instruction can designate the value stored in R0 (for example) to address the upper RAM. This value might be the result of another calculation.

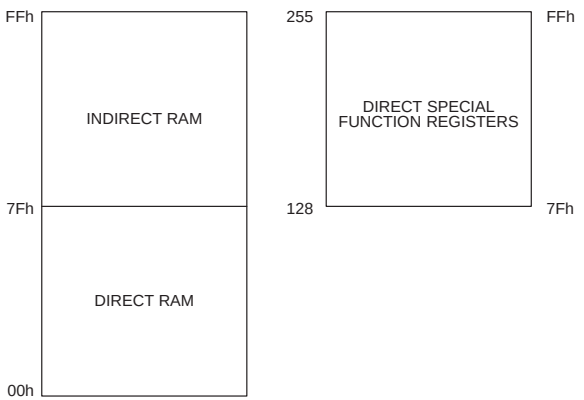
Stack

Another use of the Scratchpad area is for the programmer's stack. This area is selected using the Stack Pointer (SP,81h) SFR. Whenever a call or interrupt is invoked, the return address is placed on the Stack. It also is available to the programmer for variables, etc. Since the Stack can be moved, there is no fixed location within the RAM designated as Stack. The Stack Pointer will default to 07h on reset. The user can then move it as needed. A convenient location would be the upper RAM area (>7Fh) since this is only available indirectly. The SP will point to the last used value. Therefore, the next value placed on the Stack is put at SP + 1. Each PUSH or CALL will increment the SP by the appropriate value. Each POP or RET will decrement as well.

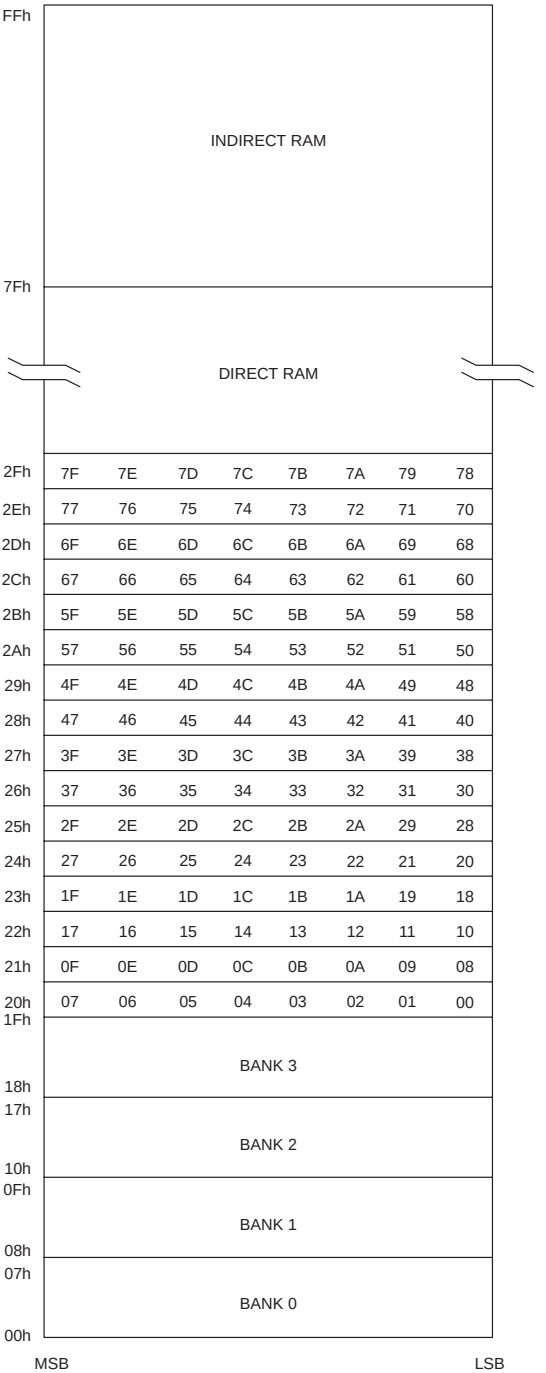
MEMORY MAP Figure 4–1



REGISTER MAP Figure 4–2



SCRATCHPAD REGISTER ADDRESSING Figure 4–3



SPECIAL FUNCTION REGISTERS

The High–Speed Microcontroller, like the 8051, uses Special Function Registers (SFRs) to control peripherals and modes. In many cases, an SFR will control individual functions or report status on individual functions. The SFRs reside in register locations 80h–FFh and are reached using direct addressing. SFRs that end in 0 or 8 are bit addressable.

All standard SFR locations from the original 8051 are duplicated in the High–Speed Microcontroller, with several additions. Following tables illustrate the locations of the SFRs for various devices. Following each table is a description of the default reset conditions of all SFR bits. The following section is a detailed description of each Special Function Register.

DS80C310 SPECIAL FUNCTION REGISTER LOCATIONS Table 4–1

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	0	0	0	0	0	0	0	SEL	86h
PCON	SMOD_0	SMOD0	–	–	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	–	–	T2M	T1M	T0M	MD2	MD1	MD0	8Eh
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	IE5	IE4	IE3	IE2	–	–	–	–	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	–	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	–	–	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
STATUS	0	HIP	LIP	1	1	1	1	1	C5h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	C8h
T2MOD	–	–	–	–	–	–	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	F1	P	D0h
WDCON	–	POR	–	–	–	–	–	–	D8h
ACC									E0h
EIE	–	–	–	–	EX5	EX4	EX3	EX2	E8h
B									F0h
EIP	–	–	–	–	PX5	PX4	PX3	PX2	F8h

DS80C310 SPECIAL FUNCTION REGISTER RESET VALUES Table 4–2

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
SP	0	0	0	0	0	1	1	1	81h
DPL	0	0	0	0	0	0	0	0	82h
DPH	0	0	0	0	0	0	0	0	83h
DPL1	0	0	0	0	0	0	0	0	84h
DPH1	0	0	0	0	0	0	0	0	85h
DPS	0	0	0	0	0	0	0	0	86h
PCON	0	0	–	–	0	0	0	0	87h
TCON	0	0	0	0	0	0	0	0	88h
TMOD	0	0	0	0	0	0	0	0	89h
TL0	0	0	0	0	0	0	0	0	8Ah
TL1	0	0	0	0	0	0	0	0	8Bh
TH0	0	0	0	0	0	0	0	0	8Ch
TH1	0	0	0	0	0	0	0	0	8Dh
CKCON	–	–	0	0	0	0	0	1	8Eh
P1	1	1	1	1	1	1	1	1	90h
EXIF	0	0	0	0	–	–	–	–	91h
SCON0	0	0	0	0	0	0	0	0	98h
SBUF0	0	0	0	0	0	0	0	0	99h
P2	1	1	1	1	1	1	1	1	A0h
IE	0	–	0	0	0	0	0	0	A8h
SADDR0	0	0	0	0	0	0	0	0	A9h
P3	1	1	1	1	1	1	1	1	B0h
IP	–	–	0	0	0	0	0	0	B8h
SADEN0	0	0	0	0	0	0	0	0	B9h
STATUS	0	0	0	1	1	1	1	1	C5h
T2CON	0	0	0	0	0	0	0	0	C8h
T2MOD	–	–	–	–	–	–	0	0	C9h
RCAP2L	0	0	0	0	0	0	0	0	CAh
RCAP2H	0	0	0	0	0	0	0	0	CBh
TL2	0	0	0	0	0	0	0	0	CCh
TH2	0	0	0	0	0	0	0	0	CDh
PSW	0	0	0	0	0	0	0	0	D0h
WDCON	–	SPECIAL	–	–	–	–	–	–	D8h
ACC	0	0	0	0	0	0	0	0	E0h
EIE	–	–	–	–	0	0	0	0	E8h
B	0	0	0	0	0	0	0	0	F0h
EIP	–	–	–	–	0	0	0	0	F8h

DS80C320/DS80C323 SPECIAL FUNCTION REGISTER LOCATIONS Table 4–3

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	0	0	0	0	0	0	0	SEL	86h
PCON	SMOD_0	SMOD0	–	–	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0	8Eh
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	IE5	IE4	IE3	IE2	–	RGMD	RGSL	**BGS**	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
SADDR1									AAh
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	–	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
SCON1	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	C0h
SBUF1									C1h
STATUS	PIP	HIP	LIP	1	1	1	1	1	C5h
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	C8h
T2MOD	–	–	–	–	–	–	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	F1	P	D0h
WDCON	SMOD_1	**POR**	EPFI	PFI	**WDIF**	WTRF	**EWT**	**RWT**	D8h
ACC									E0h
EIE	–	–	–	EWDI	EX5	EX4	EX3	EX2	E8h
B									F0h
EIP	–	–	–	PWDI	PX5	PX4	PX3	PX2	F8h

Shaded bits are Timed Access protected.

DS80C320/DS80C323 SPECIAL FUNCTION REGISTER RESET VALUES Table 4–4

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
SP	0	0	0	0	0	1	1	1	81h
DPL	0	0	0	0	0	0	0	0	82h
DPH	0	0	0	0	0	0	0	0	83h
DPL1	0	0	0	0	0	0	0	0	84h
DPH1	0	0	0	0	0	0	0	0	85h
DPS	0	0	0	0	0	0	0	0	86h
PCON	0	0	–	–	0	0	0	0	87h
TCON	0	0	0	0	0	0	0	0	88h
TMOD	0	0	0	0	0	0	0	0	89h
TL0	0	0	0	0	0	0	0	0	8Ah
TL1	0	0	0	0	0	0	0	0	8Bh
TH0	0	0	0	0	0	0	0	0	8Ch
TH1	0	0	0	0	0	0	0	0	8Dh
CKCON	0	0	0	0	0	0	0	1	8Eh
P1	1	1	1	1	1	1	1	1	90h
EXIF	0	0	0	0	–	0	SPECIAL	0	91h
SCON0	0	0	0	0	0	0	0	0	98h
SBUF0	0	0	0	0	0	0	0	0	99h
P2	1	1	1	1	1	1	1	1	A0h
IE	0	0	0	0	0	0	0	0	A8h
SADDR0	0	0	0	0	0	0	0	0	A9h
SADDR1	0	0	0	0	0	0	0	0	AAh
P3	1	1	1	1	1	1	1	1	B0h
IP	–	0	0	0	0	0	0	0	B8h
SADEN0	0	0	0	0	0	0	0	0	B9h
SADEN1	0	0	0	0	0	0	0	0	BAh
SCON1	0	0	0	0	0	0	0	0	C0h
SBUF1	0	0	0	0	0	0	0	0	C1h
STATUS	0	0	0	1	1	1	1	1	C5h
TA	1	1	1	1	1	1	1	1	C7h
T2CON	0	0	0	0	0	0	0	0	C8h
T2MOD	–	–	–	–	–	–	0	0	C9h
RCAP2L	0	0	0	0	0	0	0	0	CAh
RCAP2H	0	0	0	0	0	0	0	0	CBh
TL2	0	0	0	0	0	0	0	0	CCh
TH2	0	0	0	0	0	0	0	0	CDh
PSW	0	0	0	0	0	0	0	0	D0h
WDCON	0	SPECIAL	0	SPECIAL	0	SPECIAL	SPECIAL	0	D8h
ACC	0	0	0	0	0	0	0	0	E0h
EIE	–	–	–	0	0	0	0	0	E8h
B	0	0	0	0	0	0	0	0	F0h
EIP	–	–	–	0	0	0	0	0	F8h

DS83C520/DS87C520 SPECIAL FUNCTION REGISTER LOCATIONS Table 4–7

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	80h
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	0	0	0	0	0	0	0	SEL	86h
PCON	SMOD_0	SMOD0	–	–	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0	8Eh
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	IE5	IE4	IE3	IE2	XT/$\overline{RG}$	RGMD	RGSL	**BGS**	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
SADDR1									AAh
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	–	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
SCON1	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	C0h
SBUF1									C1h
ROMSIZE	–	–	–	–	–	RMS2	RMS1	RMS0	C2h
PMR	CD1	CD0	SWB	–	XTOFF	ALEOFF	DME1	DME0	C4h
STATUS	PIP	HIP	LIP	XTUP	SPTA1	SPRA1	SPTA0	SPRA0	C5h
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	C8h
T2MOD	–	–	–	–	–	–	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	F1	P	D0h
WDCON	SMOD_1	**POR**	EPFI	PFI	**WDIF**	WTRF	**EWT**	**RWT**	D8h
ACC									E0h
EIE	–	–	–	EWDI	EX5	EX4	EX3	EX2	E8h
B									F0h
EIP	–	–	–	PWDI	PX5	PX4	PX3	PX2	F8h

Shaded bits are Timed Access protected.

DS83C520/DS87C520 SPECIAL FUNCTION REGISTER RESET VALUES Table 4–8

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
P0	1	1	1	1	1	1	1	1	80h
SP	0	0	0	0	0	1	1	1	81h
DPL	0	0	0	0	0	0	0	0	82h
DPH	0	0	0	0	0	0	0	0	83h
DPL1	0	0	0	0	0	0	0	0	84h
DPH1	0	0	0	0	0	0	0	0	85h
DPS	0	0	0	0	0	0	0	0	86h
PCON	0	0	–	–	0	0	0	0	87h
TCON	0	0	0	0	0	0	0	0	88h
TMOD	0	0	0	0	0	0	0	0	89h
TL0	0	0	0	0	0	0	0	0	8Ah
TL1	0	0	0	0	0	0	0	0	8Bh
TH0	0	0	0	0	0	0	0	0	8Ch
TH1	0	0	0	0	0	0	0	0	8Dh
CKCON	0	0	0	0	0	0	0	1	8Eh
P1	1	1	1	1	1	1	1	1	90h
EXIF	0	0	0	0	SPECIAL	SPECIAL	SPECIAL	0	91h
SCON0	0	0	0	0	0	0	0	0	98h
SBUF0	0	0	0	0	0	0	0	0	99h
P2	1	1	1	1	1	1	1	1	A0h
IE	0	0	0	0	0	0	0	0	A8h
SADDR0	0	0	0	0	0	0	0	0	A9h
SADDR1	0	0	0	0	0	0	0	0	AAh
P3	1	1	1	1	1	1	1	1	B0h
IP	–	0	0	0	0	0	0	0	B8h
SADEN0	0	0	0	0	0	0	0	0	B9h
SADEN1	0	0	0	0	0	0	0	0	BAh
SCON1	0	0	0	0	0	0	0	0	C0h
SBUF1	0	0	0	0	0	0	0	0	C1h
ROMSIZE	–	–	–	–	–	1	0	1	C2h
PMR	0	1	0	–	0	0	0	0	C4h
STATUS	0	0	0	SPECIAL	0	0	0	0	C5h
TA	1	1	1	1	1	1	1	1	C7h
T2CON	0	0	0	0	0	0	0	0	C8h
T2MOD	–	–	–	–	–	–	0	0	C9h
RCAP2L	0	0	0	0	0	0	0	0	CAh
RCAP2H	0	0	0	0	0	0	0	0	CBh
TL2	0	0	0	0	0	0	0	0	CCh
TH2	0	0	0	0	0	0	0	0	CDh
PSW	0	0	0	0	0	0	0	0	D0h
WDCON	0	SPECIAL	0	SPECIAL	0	SPECIAL	SPECIAL	0	D8h
ACC	0	0	0	0	0	0	0	0	E0h
EIE	–	–	–	0	0	0	0	0	E8h
B	0	0	0	0	0	0	0	0	F0h
EIP	–	–	–	0	0	0	0	0	F8h

DS87C530 SPECIAL FUNCTION REGISTER LOCATIONS Table 4–9

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	80h
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	0	0	0	0	0	0	0	SEL	86h
PCON	SMOD_0	SMOD0	–	–	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0	8Eh
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	IE5	IE4	IE3	IE2	XT/$\overline{RG}$	RGMD	RGSL	**BGS**	91h
TRIM	**E4K**	**X12/$\overline{6}$**	**TRM2**	**$\overline{TRM2}$**	**TRM1**	**$\overline{TRM1}$**	**TRM0**	**$\overline{TRM0}$**	96h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
SADDR1									AAh
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	–	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
SCON1	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	C0h
SBUF1									C1h
ROMSIZE	–	–	–	–	–	**RMS2**	**RMS1**	**RMS0**	C2h
PMR	CD1	CD0	SWB	–	XTOFF	ALEOFF	DME1	DME0	C4h
STATUS	PIP	HIP	LIP	XTUP	SPTA1	SPRA1	SPTA0	SPRA0	C5h
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	C8h
T2MOD	–	–	–	–	–	–	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	F1	P	D0h
WDCON	SMOD_1	**POR**	EPFI	PFI	**WDIF**	WTRF	**EWT**	**RWT**	D8h
ACC									E0h
EIE	–	–	ERTCI	EWDI	EX5	EX4	EX3	EX2	E8h

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
B									F0h
RTASS									F2h
RTAS	0	0							F3h
RTAM	0	0							F4h
RTAH	0	0	0						F5h
EIP	–	–	PRTCI	PWDI	PX5	PX4	PX3	PX2	F8h
RTCC	SSCE	SCE	MCE	HCE	RTCRE	**RTCWE**	RTCIF	**RTCE**	F9h
RTCSS									FAh
RTCS	0	0							FBh
RTCM	0	0							FCh
RTCH									FDh
RTCD0									FEh
RTCD1									FFh

Shaded bits are Timed Access protected.

DS87C530 SPECIAL FUNCTION REGISTER RESET VALUES Table 4–10

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
P0	1	1	1	1	1	1	1	1	80h
SP	0	0	0	0	0	1	1	1	81h
DPL	0	0	0	0	0	0	0	0	82h
DPH	0	0	0	0	0	0	0	0	83h
DPL1	0	0	0	0	0	0	0	0	84h
DPH1	0	0	0	0	0	0	0	0	85h
DPS	0	0	0	0	0	0	0	0	86h
PCON	0	0	–	–	0	0	0	0	87h
TCON	0	0	0	0	0	0	0	0	88h
TMOD	0	0	0	0	0	0	0	0	89h
TL0	0	0	0	0	0	0	0	0	8Ah
TL1	0	0	0	0	0	0	0	0	8Bh
TH0	0	0	0	0	0	0	0	0	8Ch
TH1	0	0	0	0	0	0	0	0	8Dh
CKCON	0	0	0	0	0	0	0	1	8Eh
P1	1	1	1	1	1	1	1	1	90h
EXIF	0	0	0	0	SPECIAL	SPECIAL	SPECIAL	0	91h
TRIM	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	96h
SCON0	0	0	0	0	0	0	0	0	98h
SBUF0	0	0	0	0	0	0	0	0	99h
P2	1	1	1	1	1	1	1	1	A0h
IE	0	0	0	0	0	0	0	0	A8h
SADDR0	0	0	0	0	0	0	0	0	A9h
SADDR1	0	0	0	0	0	0	0	0	AAh
P3	1	1	1	1	1	1	1	1	B0h
IP	–	0	0	0	0	0	0	0	B8h
SADEN0	0	0	0	0	0	0	0	0	B9h
SADEN1	0	0	0	0	0	0	0	0	BAh

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
SCON1	0	0	0	0	0	0	0	0	C0h
SBUF1	0	0	0	0	0	0	0	0	C1h
ROMSIZE	–	–	–	–	–	1	0	1	C2h
PMR	0	1	0	–	0	0	0	0	C4h
STATUS	0	0	0	SPECIAL	0	0	0	0	C5h
TA	1	1	1	1	1	1	1	1	C7h
T2CON	0	0	0	0	0	0	0	0	C8h
T2MOD	–	–	–	–	–	–	0	0	C9h
RCAP2L	0	0	0	0	0	0	0	0	CAh
RCAP2H	0	0	0	0	0	0	0	0	CBh
TL2	0	0	0	0	0	0	0	0	CCh
TH2	0	0	0	0	0	0	0	0	CDh
PSW	0	0	0	0	0	0	0	0	D0h
WDCON	0	SPECIAL	0	SPECIAL	0	SPECIAL	SPECIAL	0	D8h
ACC	0	0	0	0	0	0	0	0	E0h
EIE	–	–	0	0	0	0	0	0	E8h
B	0	0	0	0	0	0	0	0	F0h
RTASS	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	F2h
RTAS	0	0	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	F3h
RTAM	0	0	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	F4h
RTAH	0	0	0	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	F5h
EIP	–	–	0	0	0	0	0	0	F8h
RTCC	SPECIAL	SPECIAL	SPECIAL	SPECIAL	0	0	SPECIAL	SPECIAL	F9h
RTCSS	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	FAh
RTCS	0	0	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	FBh
RTCM	0	0	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	FCh
RTCH	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	FDh
RTCD0	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	FEh
RTCD1	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	SPECIAL	FFh

SPECIAL FUNCTION REGISTERS

Most of the unique features of the High Speed Microcontroller family are controlled by bits in special function registers (SFRs) located in unused locations in the 8051 SFR map. This allows for increased functionality while maintaining complete instruction set compatibility.

The description for each bit indicates its read and write access, as well as its state after a power on reset. Bits which are affected by a no–battery reset are also indicated. Note that many bits and registers are unique to specific devices, and their functions will vary between different members of the High Speed Microcontroller Family.

Port 0 (P0)

	7	6	5	4	3	2	1	0
SFR 80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
	RW–1	RW–1	RW–1	RW–1	RW–1	RW–1	RW–1	RW–1

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

P0.7–0
Bits 7–0

Port 0. This port functions as a multiplexed address/data bus during external memory access, and as a general purpose I/O port on devices which incorporate internal program memory. During external memory cycles, this port will contain the LSB of the address when ALE is high, and data when ALE is low. When used as a general purpose I/O, this port is open–drain and requires pull–ups. Writing a 1 to any pin of this port will place it in a high impedance mode, which is necessary if the pin is to be used as an input. Pull–ups are not required when used as a memory interface. The Port 0 latch does not exist on devices with no internal program memory, such as the DS80C310 and DS80C320.

Stack Pointer (SP)

	7	6	5	4	3	2	1	0
SFR 81h	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–1	RW–1	RW–1

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

SP.7–0
Bits 7–0

Stack Pointer. The stack pointer identifies the location where the stack will begin. The stack pointer is incremented before every PUSH operation. This register defaults to 07h after reset.

Data Pointer Low 0 (DPL)

	7	6	5	4	3	2	1	0
SFR 82h	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

DPL.7–0
Bits 7–0

Data Pointer Low 0. This register is the low byte of the standard 80C32 16–bit data pointer. DPL and DPH are used to point to non–scratchpad data RAM.

Data Pointer High 0 (DPH)

	7	6	5	4	3	2	1	0
SFR 83h	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

DPH.7–0
Bits 7–0

Data Pointer High 0. This register is the high byte of the standard 80C32 16–bit data pointer. DPL and DPH are used to point to non–scratchpad data RAM.

Data Pointer Low 1 (DPL1)

	7	6	5	4	3	2	1	0
SFR 84h	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

DPL1.7–0
Bits 7–0

Data Pointer Low 1. This register is the low byte of the auxiliary 16–bit data pointer. When the SEL bit (DPS.0) is set, DPL1 and DPH1 are used in place of DPL and DPH during DPTR operations.

Data Pointer High 1 (DPH1)

	7	6	5	4	3	2	1	0
SFR 85h	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

DPH1.7–0
Bits 7–0

Data Pointer High 1. This register is the high byte of the auxiliary 16–bit data pointer. When the SEL bit (DPS.0) is set, DPL1 and DPH1 are used in place of DPL and DPH during DPTR operations.

Data Pointer Select (DPS)

	7	6	5	4	3	2	1	0
SFR 86h	0	0	0	0	0	0	0	SEL
	R–0	R–0	R–0	R–0	R–0	R–0	R–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

Bits 7–1

Reserved. These bits will read 0.

SEL
Bit 0

Data Pointer Select. This bit selects the active data pointer.
0=Instructions that use the DPTR will use DPL and DPH.
1=Instructions that use the DPTR will use DPL1 and DPH1.

Power Control (PCON)

	7	6	5	4	3	2	1	0
SFR 87h	SMOD_0	SMOD0	–	–	GF1	GF0	STOP	IDLE
	RW–0	RW–0			RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

SMOD_0
Bit 7
Serial Port 0 Baud Rate Doubler Enable. This bit enables/disables the serial baud rate doubling function for Serial Port 0.
0=Serial Port 0 baud rate will be that defined by baud rate generation equation.
1=Serial Port 0 baud rate will be double that defined by baud rate generation equation.

SMOD0
Bit 6
Framing Error Detection Enable. This bit selects function of the SCON0.7 and SCON1.7 bits.
0=SCON0.7 and SCON1.7 control the SM0 function defined for the SCON0 and SCON1 registers.
1=SCON0.7 and SCON1.7 are converted to the Framing Error (FE) flag for the respective Serial Port.

Bits 5–4
Reserved. Read data is indeterminate.

GF1
Bit 3
General Purpose User Flag 1. This is a bit–addressable, general purpose flag for software control.

GF0
Bit 2
General Purpose User Flag 0. This is a bit–addressable, general purpose flag for software control.

STOP
Bit 1
Stop Mode Select. Setting this bit will stop program execution, halt the CPU oscillator, and internal timers, and place the CPU in a low–power mode. This bit will always be read as a 0. Setting this bit while the Idle bit is set will place the device in an undefined state.

IDLE
Bit 0
Idle Mode Select. Setting this bit will stop program execution but leave the CPU oscillator, timers, serial ports, and interrupts active. This bit will always be read as a 0.

Timer/Counter Control (TCON)

	7	6	5	4	3	2	1	0
SFR 88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

TF1
Bit 7

Timer 1 Overflow Flag. This bit indicates when Timer 1 overflows its maximum count as defined by the current mode. This bit can be cleared by software and is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.
0=No Timer 1 overflow has been detected.
1=Timer 1 has overflowed its maximum count.

TR1
Bit 6

Timer 1 Run Control. This bit enables/disables the operation of Timer 1. Halting this timer will preserve the current count in TH1, TL1.
0=Timer 1 is halted.
1=Timer 1 is enabled.

TF0
Bit 5

Timer 0 Overflow Flag. This bit indicates when Timer 0 overflows its maximum count as defined by the current mode. This bit can be cleared by software and is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine or by software.
0=No Timer 0 overflow has been detected.
1=Timer 0 has overflowed its maximum count.

TR0
Bit 4

Timer 0 Run Control. This bit enables/disables the operation of Timer 0. Halting this timer will preserve the current count in TH0, TL0.
0=Timer 0 is halted.
1=Timer 0 is enabled.

IE1
Bit 3

Interrupt 1 Edge Detect. This bit is set when an edge/level of the type defined by IT1 is detected. If IT1=1, this bit will remain set until cleared in software or the start of the External Interrupt 1 service routine. If IT1=0, this bit will inversely reflect the state of the $\overline{INT1}$ pin.

IT1
Bit 2

Interrupt 1 Type Select. This bit selects whether the $\overline{INT1}$ pin will detect edge or level triggered interrupts.
0=$\overline{INT1}$ is level triggered.
1=$\overline{INT1}$ is edge triggered.

IE0
Bit 1

Interrupt 0 Edge Detect. This bit is set when an edge/level of the type defined by IT0 is detected. If IT0=1, this bit will remain set until cleared in software or the start of the External Interrupt 0 service routine. If IT0=0, this bit will inversely reflect the state of the $\overline{INT0}$ pin.

IT0
Bit 0

Interrupt 0 Type Select. This bit selects whether the $\overline{INT0}$ pin will detect edge or level triggered interrupts.
0=$\overline{INT0}$ is level triggered.
1=$\overline{INT0}$ is edge triggered.

Timer Mode Control (TMOD)

	7	6	5	4	3	2	1	0
SFR 89h	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

GATE
Bit 7

Timer 1 Gate Control. This bit enables/disables the ability of Timer 1 to increment.
0=Timer 1 will clock when TR1=1, regardless of the state of $\overline{INT1}$.
1=Timer 1 will clock only when TR1=1 and $\overline{INT1}$=1.

C/T
Bit 6

Timer 1 Counter/Timer Select.
0=Timer is incremented by internal clocks.
1=Timer is incremented by pulses on T1 when TR1 (TCON.6) is 1.

M1, M0
Bits 5–4

Timer 1 Mode Select. These bits select the operating mode of Timer 1.

M1	M0	Mode
0	0	Mode 0: 8 bits with 5–bit prescale
0	1	Mode 1: 16 bits
1	0	Mode 2: 8 bits with auto–reload
1	1	Mode 3: Timer 1 is halted, but holds its count.

GATE
Bit 3

Timer 0 Gate Control. This bit enables/disables the ability of Timer 0 to increment.
0=Timer 0 will clock when TR0=1, regardless of the state of $\overline{INT0}$.
1=Timer 0 will clock only when TR0=1 and $\overline{INT0}$=1.

C/$\overline{T}$
Bit 2

Timer 0 Counter/Timer Select.
0=Timer is incremented by internal clocks.
1=Timer is incremented by pulses on T0 when TR0 (TCON.4) is 1.

M1, M0
Bits 1–0

Timer 0 Mode Select. These bits select the operating mode of Timer 0. When timer 0 is in mode 3, TL0 is started/stopped by TR0 and TH0 is started/stopped by TR1. Run control for timer 1 is then provided via the timer 1 mode selection.

M1	M0	Mode
0	0	Mode 0: 8 bits with 5–bit prescale
0	1	Mode 1: 16 bits
1	0	Mode 2: 8 bits with auto–reload
1	1	Mode 3: Timer 0 is two 8 bit counters

Timer 0 LSB (TL0)

	7	6	5	4	3	2	1	0
SFR 8Ah	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

TL0.7–0 **Timer 0 LSB.** This register contains the least significant byte of Timer 0.
Bits 7–0

Timer 1 LSB (TL1)

	7	6	5	4	3	2	1	0
SFR 8Bh	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

TL1.7–0 **Timer 1 LSB.** This register contains the least significant byte of Timer 1.
Bits 7–0

Timer 0 MSB (TH0)

	7	6	5	4	3	2	1	0
SFR 8Ch	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

TH0.7–0 **Timer 0 MSB.** This register contains the most significant byte of Timer 0.
Bits 7–0

Timer 1 MSB (TH1)

	7	6	5	4	3	2	1	0
SFR 8Dh	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

TH1.7–0 **Timer 1 MSB.** This register contains the most significant byte of Timer 1.
Bits 7–0

Clock Control (CKCON)

	7	6	5	4	3	2	1	0
SFR 8Eh	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–1

R=Unrestricted Read, W= Unrestricted Write, –n=Value after Reset

WD1, WD0
Bits 7–6

Watchdog Timer Mode Select 1–0. These bits determine the watchdog timer time–out period. The timer divides the crystal frequency by a programmable value as shown below. The divider value is expressed in clock (crystal) cycles. The use of PMM1 or PMM2 will further divide the clock cycle count by either 16 or 256, respectively. Note that the reset time–out is 512 clocks longer than the interrupt, regardless of whether the interrupt is enabled.

WD1	WD0	Interrupt Divider	Reset Divider
0	0	2^{17}	2^{17} + 512
0	1	2^{20}	2^{20} + 512
1	0	2^{23}	2^{23} + 512
1	1	2^{26}	2^{26} + 512

T2M
Bit 5

Timer 2 Clock Select. This bit controls the division of the system clock that drives Timer 2. This bit has no effect when the timer is in baud rate generator or clock output modes. Clearing this bit to 0 maintains 80C32 compatibility. This bit has no effect on instruction cycle timing.
0=Timer 2 uses a divide by 12 of the crystal frequency.
1=Timer 2 uses a divide by 4 of the crystal frequency.

T1M
Bit 4

Timer 1 Clock Select. This bit controls the division of the system clock that drives Timer 1. Clearing this bit to 0 maintains 80C32 compatibility. This bit has no effect on instruction cycle timing.
0=Timer 1 uses a divide by 12 of the crystal frequency.
1=Timer 1 uses a divide by 4 of the crystal frequency.

T0M
Bit 3

Timer 0 Clock Select. This bit controls the division of the system clock that drives Timer 0. Clearing this bit to 0 maintains 80C32 compatibility. This bit has no effect on instruction cycle timing.
0=Timer 0 uses a divide by 12 of the crystal frequency.
1=Timer 0 uses a divide by 4 of the crystal frequency.

MD2, MD1, MD0
Bits 2–0

Stretch MOVX Select 2–0. These bits select the time by which external MOVX cycles are to be stretched. This allows slower memory or peripherals to be accessed without using ports or manual software intervention. The RD or WR strobe will be stretched by the specified interval, which will be transparent to the software except for the increased time to execute the MOVX instruction. All internal MOVX instructions on devices containing MOVX SRAM are performed at the 2 machine cycle rate.

MD2	MD1	MD0	Stretch Value	MOVX Duration
0	0	0	0	2 Machine Cycles
0	0	1	1	3 Machine Cycles (reset default)
0	1	0	2	4 Machine Cycles
0	1	1	3	5 Machine Cycles
1	0	0	4	6 Machine Cycles
1	0	1	5	7 Machine Cycles
1	1	0	6	8 Machine Cycles
1	1	1	7	9 Machine Cycles

Port 1 (P1)

	7	6	5	4	3	2	1	0
SFR 90h	P1.7 $\overline{\text{INT5}}$	P1.6 INT4	P1.5 $\overline{\text{INT3}}$	P1.4 INT2	P1.3 TXD1	P1.2 RXD1	P1.1 T2EX	P1.0 T2
	RW–1	RW–1	RW–1	RW–1	RW–1	RW–1	RW–1	RW–1

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

P1.7–0
Bits 7–0

General Purpose I/O Port 1. This register functions as a general purpose I/O port. In addition, all the pins have an alternative function listed below. P1.2–7 contain functions that are new to the 80C32 architecture. The timer 2 functions on pins P1.1–0 are available on the 80C32, but not the 80C31. Each of the functions is controlled by several other SFRs. The associated Port 1 latch bit must contain a logic one before the pin can be used in its alternate function capacity.

$\overline{\text{INT5}}$
Bit 7

External Interrupt 5. A falling edge on this pin will cause an external interrupt 5 if enabled.

INT4
Bit 6

External Interrupt 4. A rising edge on this pin will cause an external interrupt 4 if enabled.

$\overline{\text{INT3}}$
Bit 5

External Interrupt 3. A falling edge on this pin will cause an external interrupt 3 if enabled.

INT2
Bit 4

External Interrupt 2. A rising edge on this pin will cause an external interrupt 2 if enabled.

TXD1
Bit 3

Serial Port 1 Transmit. This pin transmits the serial port 1 data in serial port modes 1,2,3 and emits the synchronizing clock in serial port mode 0.

RXD1
Bit 2

Serial Port 1 Receive. This pin receives the serial port 1 data in serial port modes 1,2,3 and is a bi–directional data transfer pin in serial port mode 0.

T2EX
Bit 1

Timer 2 Capture/Reload Trigger. A 1 to 0 transition on this pin will cause the value in the T2 registers to be transferred into the capture registers if enabled by EXEN2 (T2CON.3). When in auto–reload mode, a 1 to 0 transition on this pin will reload the timer 2 registers with the value in RCAP2L and RCAP2H if enabled by EXEN2 (T2CON.3).

T2
Bit 0

Timer 2 External Input. A 1 to 0 transition on this pin will cause timer 2 to increment or decrement depending on the timer configuration.

External Interrupt Flag (EXIF)

	7	6	5	4	3	2	1	0
SFR 91h	IE5	IE4	IE3	IE2	XT/$\overline{RG}$	RGMD	RGSL	BGS
	RW–0	RW–0	RW–0	RW–0	RW–*	R–*	RW–*	RT–0

R=Unrestricted Read, W=Unrestricted Write, T=Timed Access Write Only, –n=Value after Reset, *=See description

IE5
Bit 7

External Interrupt 5 Flag. This bit will be set when a falling edge is detected on $\overline{INT5}$. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

IE4
Bit 6

External Interrupt 4 Flag. This bit will be set when a rising edge is detected on INT4. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

IE3
Bit 5

External Interrupt 3 Flag. This bit will be set when a falling edge is detected on $\overline{INT3}$. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

IE2
Bit 4

External Interrupt 2 Flag. This bit will be set when a rising edge is detected on INT2. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

XT/$\overline{RG}$
Bit 3

Crystal/Ring Source Select. This bit selects the crystal oscillator or ring oscillator as the desired clock source. This bit will be the inverse of RGMD except during the crystal warm–up period when executing a ring oscillator resume from Stop. XTUP (STATUS.4) must be set to 1 and XTOFF (PMR.3) must be cleared to 0 before this bit can be set. Attempts to modify this bit when these conditions are not met will be ignored. This bit must be cleared before XTOFF can be set to 1. This bit is set to 1 after a power–on reset, and unchanged by all other forms of reset. This bit is not used on the DS80C310 or DS80C320 and will be 1 when read.
0=The ring oscillator is selected as the clock source. This setting is unaffected by XTUP (STATUS.4) and XTOFF (PMR.3).
1=The crystal oscillator is selected as the clock source. This setting is invalid unless XTUP=1 and XTOFF=0.

RGMD
Bit 2

Ring Mode Status. This bit indicates the current clock source for the device. This bit is cleared to 0 after a power–on reset, and unchanged by all other forms of reset. The state of this bit will be undefined on devices which do not incorporate a ring oscillator.
0=Device is operating from the external crystal or oscillator.
1=Device is operating from the ring oscillator.

RGSL
Bit 1

Ring Oscillator Select. This bit selects the clock source following a resume from Stop mode. Using the ring oscillator to resume from Stop mode allows almost instantaneous start–up. This bit is cleared to 0 after a power–on reset, and unchanged by all other forms of reset. The state of this bit will be undefined on devices which do not incorporate a ring oscillator.
0=The device will hold operation until the crystal oscillator has warmed–up.
1=The device will begin operating from the ring oscillator, and when the crys-

tal warm–up is complete, will switch to the clock source indicated by the XT/$\overline{RG}$ bit.

BGS
Bit 0

Band–gap Select. This bit enables/disables the band–gap reference during Stop mode. Disabling the band–gap reference provides significant power savings in Stop mode, but sacrifices the ability to perform a power fail interrupt or power–fail reset while stopped. This bit can only be modified with a Timed Access procedure. The state of this bit will be undefined on devices which do not incorporate a band–gap reference.
0=The band–gap reference is disabled in Stop mode but will function during normal operation.
1=The band–gap reference will operate in Stop mode.

RTC Trim Register (TRIM)

	7	6	5	4	3	2	1	0
SFR 96h	E4K	X12/$\overline{6}$	TRM2	$\overline{TRM2}$	TRM1	$\overline{TRM1}$	TRM0	$\overline{TRM0}$
	RT–*	RT–*	RT–*	RT–*	RT–*	RT–*	RT–*	RT–*

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset, *=See description

E4K
Bit 7

External 4096 Hz RTC Signal Enable. This bit enables the output of a 4096 Hz signal on pin P1.7 derived from the RTC. Setting this bit overrides any other function of the pin. It is used for adjusting the frequency of the 32.768 RTC crystal oscillator using the trim bits. This bit is cleared to 0 after any reset, including a no–battery reset.
0=Calibration function disabled. P1.7 pin will function per the normal pin description.
1=4096 Hz signal output on P1.7

X12/$\overline{6}$
Bit 6

RTC Crystal Capacitance Select. This bit selects the internal loading capacitance of the RTC crystal amplifier. This bit is set to 1 after a no–battery reset, and unchanged by all other forms of reset.
0=RTC loading is set for 6 pF crystal.
1=RTC loading is set for 12.5 pF crystal.

TRM2
Bit 5

RTC Trim Bit 2. This bit controls the relative adjustment of the RTC internal capacitance. It is used to calibrate the RTC oscillator frequency. This bit is set to 1 after a no–battery reset, and unchanged by all other forms of reset.

$\overline{TRM2}$
Bit 4

RTC Inverted Trim Bit 2. This bit must always be set to the complement of the TRM2 bit. Incorrectly writing this bit will default bits TRIM.7, TRIM.5–0 to their no–battery reset value. This bit is cleared to 0 after a no–battery reset, and unchanged by all other forms of reset.

TRM1
Bit 3

RTC Trim Bit 1. This bit controls the relative adjustment of the RTC internal capacitance. It is used to calibrate the RTC oscillator frequency. This bit is set to 0 after a no–battery reset, and unchanged by all other forms of reset.

$\overline{TRM1}$
Bit 2

RTC Inverted Trim Bit 1. This bit must always be set to the complement of the TRM1 bit. Incorrectly writing this bit will default bits TRIM.7, TRIM.5–0 to their no–battery reset value. This bit is cleared to 1 after a no–battery reset, and unchanged by all other forms of reset.

TRM0
Bit 1

RTC Trim Bit 0. This bit controls the relative adjustment of the RTC internal capacitance. It is used to calibrate the RTC oscillator frequency. This bit is set to 0 after a no–battery reset, and unchanged by all other forms of reset.

$\overline{\text{TRM0}}$
Bit 0

RTC Inverted Trim Bit 0. This bit must always be set to the complement of the TRM0 bit. Incorrectly writing this bit will default bits TRIM.7, TRIM.5–0 to their no–battery reset value. This bit is cleared to 1 after a no–battery reset, and unchanged by all other forms of reset.

Serial Port 0 Control (SCON0)

	7	6	5	4	3	2	1	0
SFR 98h	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

SM0–2
Bits 7–5

Serial Port 0 Mode. These bits control the mode of serial port 0. In addition, the SM0 and SM2_0 bits have secondary functions as shown below.

SM0	SM1	SM2	MODE	FUNCTION	LENGTH	PERIOD
0	0	0	0	Synchronous	8 bits	12 t_{CLK}
0	0	1	0	Synchronous	8 bits	4 t_{CLK}
0	1	x	1	Asynchronous	10 bits	Timer 1 or 2 baud rate equation
1	0	0	2	Asynchronous	11 bits	64 t_{CLK} (SMOD=0) 32 t_{CLK} (SMOD=1)
1	0	1	2	Asynchronous w/ Multiprocessor communication	11 bits	64 t_{CLK} (SMOD=0) 32 t_{CLK} (SMOD=1)
1	1	0	3	Asynchronous	11 bits	Timer 1 or 2 baud rate equation
1	1	1	3	Asynchronous w/ Multiprocessor communication	11 bits	Timer 1 or 2 baud rate equation

SM0/FE_0
Bit 7

Framing Error Flag. When SMOD0 (PCON.6)=0, this bit (SM0) is used to select the mode for serial port 0. When SMOD0 (PCON.6)=1, this bit (FE) will be set upon detection of an invalid stop bit. When used as FE, this bit must be cleared in software. Once the SMOD0 bit is set, modifications to this bit will not affect the serial port mode settings. Although accessed from the same register, internally the data for bits SM0 and FE are stored in different locations.

SM1_0
Bit 6

No alternate function.

SM2_0
Bit 5

Multiple CPU Communications. The function of this bit is dependent on the serial port 0 mode.
Mode 0: Selects 12 t_{CLK} or 4 t_{CLK} period for synchronous serial port 0 data transfers.
Mode 1: When set, reception is ignored (RI_0 is not set) if invalid stop bit received.
Mode 2/3: When this bit is set, multiprocessor communications are enabled

in modes 2 and 3. This will prevent the RI_0 bit from being set, and an interrupt being asserted, if the 9th bit received is not 1.

REN_0
Bit 4

Receive Enable. This bit enables/disables the serial port 0 receiver shift register.
0=Serial port 0 reception disabled.
1=Serial port 0 receiver enabled (modes 1, 2, 3). Initiate synchronous reception (mode 0).

TB8_0
Bit 3

9th Transmission Bit State. This bit defines the state of the 9th transmission bit in serial port 0 modes 2 and 3.

RB8_0
Bit 2

9th Received Bit State. This bit identifies the state of the 9th reception bit of received data in serial port 0 modes 2 and 3. In serial port mode 1, when SM2_0=0, RB8_0 is the state of the stop bit. RB8_0 is not used in mode 0.

TI_0
Bit 1

Transmitter Interrupt Flag. This bit indicates that data in the serial port 0 buffer has been completely shifted out. In serial port mode 0, TI_0 is set at the end of the 8th data bit. In all other modes, this bit is set at the end of the last data bit. This bit must be manually cleared by software.

RI_0
Bit 0

Receiver Interrupt Flag. This bit indicates that a byte of data has been received in the serial port 0 buffer. In serial port mode 0, RI_0 is set at the end of the 8th bit. In serial port mode 1, RI_0 is set after the last sample of the incoming stop bit subject to the state of SM2_0. In modes 2 and 3, RI_0 is set after the last sample of RB8_0. This bit must be manually cleared by software.

Serial Data Buffer 0 (SBUF0)

	7	6	5	4	3	2	1	0
SFR 99h	SBUF0.7	SBUF0.6	SBUF0.5	SBUF0.4	SBUF0.3	SBUF0.2	SBUF0.1	SBUF0.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

SBUF0.7–0
Bits 7–0

Serial Data Buffer 0. Data for serial port 0 is read from or written to this location. The serial transmit and receive buffers are separate registers, but both are addressed at this location.

Port 2 (P2)

	7	6	5	4	3	2	1	0
SFR A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
	RW–1	RW–1	RW–1	RW–1	RW–1	RW–1	RW–1	RW–1

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

P2.7–0
Bits 7–0

Port 2. This port functions as an address bus during external memory access, and as a general purpose I/O port on devices which incorporate internal program memory. During external memory cycles, this port will contain the MSB of the address. The Port 2 latch does not control general purpose I/O pins on the DS80C310 and DS80C320, but is still used to hold the address MSB during register–indirect data memory operations such as MOVX A, @R1.

Interrupt Enable (IE)

	7	6	5	4	3	2	1	0
SFR A8h	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

EA
Bit 7

Global Interrupt Enable. This bit controls the global masking of all interrupts except Power–Fail Interrupt, which is enabled by the EPFI bit (WDCON.5).
0=Disable all interrupt sources. This bit overrides individual interrupt mask settings.
1=Enable all individual interrupt masks. Individual interrupts will occur if enabled.

ES1
Bit 6

Enable Serial Port 1 Interrupt. This bit controls the masking of the serial port 1 interrupt.
0=Disable all serial port 1 interrupts.
1=Enable interrupt requests generated by the RI_1 (SCON1.0) or TI_1 (SCON1.1) flags.

ET2
Bit 5

Enable Timer 2 Interrupt. This bit controls the masking of the Timer 2 interrupt.
0=Disable all Timer 2 interrupts.
1=Enable interrupt requests generated by the TF2 flag (T2CON.7).

ES0
Bit 4

Enable Serial port 0 Interrupt. This bit controls the masking of the serial port 0 interrupt.
0=Disable all serial port 0 interrupts.
1=Enable interrupt requests generated by the RI_0 (SCON0.0) or TI_0 (SCON0.1) flags.

ET1
Bit 3
Enable Timer 1 Interrupt. This bit controls the masking of the Timer 1 interrupt.
0=Disable all Timer 1 interrupts.
1=Enable interrupt requests generated by the TF1 flag (TCON.7).

EX1
Bit 2
Enable External Interrupt 1. This bit controls the masking of external interrupt 1.
0=Disable external interrupt 1.
1=Enable interrupt requests generated by the $\overline{\text{INT1}}$ pin.

ET0
Bit 1
Enable Timer 0 Interrupt. This bit controls the masking of the Timer 0 interrupt.
0=Disable all Timer 0 interrupts.
1=Enable interrupt requests generated by the TF0 flag (TCON.5).

EX0
Bit 0
Enable External Interrupt 0. This bit controls the masking of external interrupt 0.
0=Disable external interrupt 0.
1=Enable interrupt requests generated by the $\overline{\text{INT0}}$ pin.

Slave Address Register 0 (SADDR0)

	7	6	5	4	3	2	1	0
SFR A9h	SADDR0.7	SADDR0.6	SADDR0.5	SADDR0.4	SADDR0.3	SADDR0.2	SADDR0.1	SADDR0.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

SADDR0.7–0
Bits 7–0
Slave Address Register 0. This register is programmed with the given or broadcast address assigned to serial port 0.

Slave Address Register 1 (SADDR1)

	7	6	5	4	3	2	1	0
SFR AAh	SADDR1.7	SADDR1.6	SADDR1.5	SADDR1.4	SADDR1.3	SADDR1.2	SADDR1.1	SADDR1.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

SADDR1.7–0
Bits 7–0
Slave Address Register 1. This register is programmed with the given or broadcast address assigned to serial port 1.

Port 3 (P3)

	7	6	5	4	3	2	1	0
SFR B0h	P3.7 $\overline{RD}$	P3.6 $\overline{WR}$	P3.5 T1	P3.4 T0	P3.3 $\overline{INT1}$	P3.2 $\overline{INT0}$	P3.1 TXD0	P3.0 RXD0
	RW–1	RW–1	RW–1	RW–1	RW–1	RW–1	RW–1	RW–1

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

P3.7–0
Bits 7–0
General Purpose I/O Port 3. This register functions as a general purpose I/O port. In addition, all the pins have an alternative function listed below. Each of the functions is controlled by several other SFRs. The associated Port 1 latch bit must contain a logic one before the pin can be used in its alternate function capacity.

$\overline{RD}$
Bit 7
External Data Memory Read Strobe. This pin provides an active low read strobe to an external memory device.

$\overline{WR}$
Bit 6
External Data Memory Write Strobe. This pin provides an active low write strobe to an external memory device.

T1
Bit 5
Timer/Counter 1 External Input. A 1 to 0 transition on this pin will increment timer 1.

T0
Bit 4
Timer/Counter 0 External Input. A 1 to 0 transition on this pin will increment timer 0.

$\overline{INT1}$
Bit 3
External Interrupt 1. A falling edge/ low level on this pin will cause an external interrupt 1 if enabled.

$\overline{INT0}$
Bit 2
External Interrupt 0. A falling edge/ low level on this pin will cause an external interrupt 0 if enabled.

TXD0
Bit 1
Serial Port 0 Transmit. This pin transmits the serial port 0 data in serial port modes 1,2,3 and emits the synchronizing clock in serial port mode 0.

RXD0
Bit 0
Serial Port 0 Receive. This pin receives the serial port 0 data in serial port modes 1,2,3 and is a bi–directional data transfer pin in serial port mode 0.

Interrupt Priority (IP)

	7	6	5	4	3	2	1	0
SFR B8h	–	PS1	PT2	PS0	PT1	PX1	PT0	PX0
		RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

Bit 7
Reserved. Read data is indeterminate.

PS1
Bit 6
Serial Port 1 Interrupt. This bit controls the priority of the serial port 1 interrupt.
0=Serial port 1 priority is determined by the natural priority order.
1=Serial port 1 is a high priority interrupt.

PT2
Bit 5
Timer 2 Interrupt. This bit controls the priority of the Timer 2 interrupt.
0=Timer 2 priority is determined by the natural priority order.
1=Timer 2 is a high priority interrupt.

PS0
Bit 4
Serial port 0 Interrupt. This bit controls the priority of the serial port 0 interrupt.
0=Serial port 0 priority is determined by the natural priority order.
1=Serial port 0 is a high priority interrupt.

PT1
Bit 3
Timer 1 Interrupt. This bit controls the priority of the Timer 1 interrupt.
0=Timer 1 priority is determined by the natural priority order.
1=Timer 1 is a high priority interrupt.

PX1
Bit 2
External Interrupt 1. This bit controls the priority of external interrupt 1.
0=External interrupt 1 priority is determined by the natural priority order.
1=External interrupt 1 is a high priority interrupt.

PT0
Bit 1
Timer 0 Interrupt. This bit controls the priority of the Timer 0 interrupt.
0=Timer 0 priority is determined by the natural priority order.
1=Timer 0 is a high priority interrupt.

PX0
Bit 0
External Interrupt 0. This bit controls the priority of external interrupt 0.
0=External interrupt 0 priority is determined by the natural priority order.
1=External interrupt 0 is a high priority interrupt.

Slave Address Mask Enable Register 0 (SADEN0)

	7	6	5	4	3	2	1	0
SFR B9h	SADEN0.7	SADEN0.6	SADEN0.5	SADEN0.4	SADEN0.3	SADEN0.2	SADEN0.1	SADEN0.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

SADEN0.7–0
Bits 7–0
Slave Address Mask Enable Register 0. This register functions as a mask when comparing serial port 0 addresses for automatic address recognition. When a bit in this register is set, the corresponding bit location in the SADDR0 register will be exactly compared with the incoming serial port 0 data to determine if a receiver interrupt should be generated. When a bit in this register is cleared, the corresponding bit in the SADDR0 register becomes a don't care and is not compared against the incoming data. All incoming data will generate a receiver interrupt when this register is cleared.

Slave Address Mask Enable Register 1 (SADEN1)

	7	6	5	4	3	2	1	0
SFR BAh	SADEN1.7	SADEN1.6	SADEN1.5	SADEN1.4	SADEN1.3	SADEN1.2	SADEN1.1	SADEN1.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

SADEN1.7–0
Bits 7–0
Slave Address Mask Enable Register 1. This register functions as a mask when comparing serial port 1 addresses for automatic address recognition.

When a bit in this register is set, the corresponding bit location in the SADDR1 register will be exactly compared with the incoming serial port 1 data to determine if a receiver interrupt should be generated. When a bit in this register is cleared, the corresponding bit in the SADDR1 register becomes a don't care and is not compared against the incoming data. All incoming data will generate a receiver interrupt when this register is cleared.

Serial Port 1 Control (SCON1)

	7	6	5	4	3	2	1	0
SFR C0h	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

SM0–2,
Bits 7–5

Serial Port 1 Mode. These bits control the mode of serial port 1 as shown below. In addition, the SM0 and SM2 bits have secondary functions as shown below.

SM0	SM1	SM2	MODE	FUNCTION	LENGTH	PERIOD
0	0	0	0	Synchronous	8 bits	12 t_{CLK}
0	0	1	0	Synchronous	8 bits	4 t_{CLK}
0	1	x	1	Asynchronous	10 bits	Timer 1 baud rate equation
1	0	0	2	Asynchronous	11 bits	64 t_{CLK} (SMOD=0) 32 t_{CLK} (SMOD=1)
1	0	1	2	Asynchronous w/ Multiprocessor communication	11 bits	64 t_{CLK} (SMOD=0) 32 t_{CLK} (SMOD=1)
1	1	0	3	Asynchronous	11 bits	Timer 1 baud rate equation
1	1	1	3	Asynchronous w/ Multiprocessor communication	11 bits	Timer 1 baud rate equation

SM0/FE_1
Bit 7

Framing Error Flag. When SMOD0 (PCON.6)=0, this bit (SM0) is used to select the mode for serial port 1. When SMOD0 (PCON.6)=1, this bit (FE) will be set upon detection of an invalid stop bit. When used as FE, this bit must be cleared in software. Once the SMOD0 bit is set, modifications to this bit will not affect the serial port mode settings. Although accessed from the same register, internally the data for bits SM0 and FE are stored in different locations.

SM1_1
Bit 6

No alternate function.

SM2_1
Bit 5

Multiple CPU Communications. The function of this bit is dependent on the serial port 1 mode.
Mode 0: Selects 12 t_{CLK} or 4 t_{CLK} period for synchronous serial port 1 data transfers.
Mode 1: When this bit is set, reception is ignored (RI_1 is not set) if invalid stop bit received.
Mode 2/3: When this bit is set, multiprocessor communications are enabled

in modes 2 and 3. This will prevent the RI_1 bit from being set, and an interrupt being asserted, if the 9th bit received is not 1.

REN_1
Bit 4

Receive Enable. This bit enables/disables the serial port 1 receiver shift register.
0=Serial port 1 reception disabled.
1=Serial port 1 receiver enabled (modes 1, 2, 3). Initiate synchronous reception (mode 0).

TB8_1
Bit 3

9th Transmission Bit State. This bit defines the state of the 9th transmission bit in serial port 1 modes 2 and 3.

RB8_1
Bit 2

9th Received Bit State. This bit identifies the state of the 9th reception bit of received data in serial port 1 modes 2 and 3. In serial port mode 1, when SM2_1=0, RB8_1 is the state of the stop bit. RB8_1 is not used in mode 0.

TI_1
Bit 1

Transmitter Interrupt Flag. This bit indicates that data in the serial port 1 buffer has been completely shifted out. In serial port mode 0, TI_1 is set at the end of the 8th data bit. In all other modes, this bit is set at the end of the last data bit. This bit must be manually cleared by software.

RI_1
Bit 0

Receiver Interrupt Flag. This bit indicates that a byte of data has been received in the serial port 1 buffer. In serial port mode 1, RI_1 is set at the end of the 8th bit. In serial port mode 1, RI_1 is set after the last sample of the incoming stop bit subject to the state of SM2_1. In modes 2 and 3, RI_1 is set after the last sample of RB8_1. This bit must be manually cleared by software.

Serial Data Buffer 1 (SBUF1)

	7	6	5	4	3	2	1	0
SFR C1h	SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

SBUF1.7–0
Bits 7–0

Serial Data Buffer 1. Data for serial port 1 is read from or written to this location. The serial transmit and receive buffers are separate registers, but both are addressed at this location.

ROM Size Select (ROMSIZE)

	7	6	5	4	3	2	1	0
SFR C2h	–	–	–	–	–	RS2	RS1	RS0
						RT–1	RT–0	RT–1

R=Unrestricted Read, T=Timed Access Write Only, –n=Value after Reset

Bits 7–3

These bits are reserved. Read data is indeterminate.

ROMSIZE.2–0
Bits 2–0

ROM Size Select 2–0. This register is used to select the maximum on–chip decoded address for ROM. Care must be taken that the memory location of the current program counter will be valid both before and after modification.

These bits can only be modified using a timed access procedure. The $\overline{EA}$ pin will override the function of these bits when asserted, forcing the device to access external program memory only. Configuring this register to a setting that exceeds the maximum amount of internal memory may corrupt device operation. These bits will default on reset to the maximum amount of internal program memory (i.e. 16K for DS87C520).

RS2	RS1	RS0	MAXIMUM ON–CHIP ROM ADDRESS
0	0	0	0KB/Disable on–chip ROM
0	0	1	1KB/03FFh
0	1	0	2KB/07FFh
0	1	1	4KB/0FFFh
1	0	0	8KB/1FFFh
1	0	1	16KB/3FFFh
1	1	0	32KB/7FFFh
1	1	1	64KB/FFFFh

Power Management Register (PMR)

	7	6	5	4	3	2	1	0
SFR C4h	CD1	CD0	SWB	–	XTOFF	ALEOFF	DME1	DME0
	RW–0	RW–1	RW–0		RW*–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset, *=See description

CD1, CD0
Bits 7–6

Clock Divide Control 1–0. These bits select the number of crystal oscillator clocks required to generate one machine cycle. Switching between modes requires a transition through the divide by 4 mode (CD1, CD0=01). For example, to go from 64 to 1024 clocks per cycle the device must first go from 64 to 4 clocks per cycle, and then from 4 to 1024 clocks per cycle. Attempts to perform an invalid transition will be ignored. The setting of these bits will effect the timers and serial ports as shown below.

		OSC CYCLES PER MACH. CYCLE	OSC CYCLES PER TIMER 0/1/2 CLOCK		OSC CYCLES PER TIMER 2 CLK, BAUD RATE GEN.		OSC CYCLES PER SERIAL PORT CLK, MODE 0		OSC CYCLES PER SERIAL PORT CLK, MODE 2	
CD1	CD0		TxM=0	TxM=1	T2M=0	T2M=1	SM2=0	SM2=1	SDMO=0	SMOD=1
0	0	RESERVED								
0	1	4	12	4	2	2	12	4	64	32
1	0	64	192	64	32	32	192	64	1024	512
1	1	1024	3072	1024	512	512	3072	1024	16384	8192

SWB
Bit 5

Switchback Enable. This bit allows an enabled external interrupt or serial port activity to force the Clock Divide Control bits to the divide by 4 state (01). Upon internal acknowledgment of an external interrupt, the device will

switch modes at the start of the jump to the interrupt service routine. Note that this means that an external interrupt must actually be recognized (i.e. be enabled and not masked by higher priority interrupts) for the switchback to occur. For serial port reception, the switch occurs at the start of the instruction following the falling edge of the start bit.

Bit 4 — Reserved. When modifying the PMR register, software must write a 0 to this bit. Read data will be indeterminate.

XTOFF
Bit 3 — **Crystal Oscillator Disable.** This bit disables the CPU crystal oscillator. It can only be set to 1 while running from the ring oscillator (XT/$\overline{RG}$=0). Clearing this bit restarts the crystal amplifier, resets the crystal warm–up counter, and after 65,536 external crystal cycles the XTUP bit will be set.
0=Crystal oscillator is enabled
1=Crystal oscillator is disabled

ALEOFF
Bit 2 — **ALE Disable.** This bit disables the expression of the ALE signal on the device pin during all on–board program and data memory accesses. External memory accesses will automatically enable ALE independent of ALEOFF.
0=ALE expression is enabled
1=ALE expression is disabled

DME1, DME0
Bits 1–0 — **Data Memory Enable 1–0.** These bits determine the functional relationship of the first 1024 bytes of data memory. Three memory configurations are supported to allow either external data memory access through the expanded multiplexed address/data bus of Ports 0 and Port 2, internal SRAM data memory access, or read–only access to EPROM programming information. Note these bits are cleared after a reset, so access to the internal SRAM is prohibited until these bits are modified.

DME1	DME0	DATA MEMORY ADDRESS RANGE	MEMORY ACCESS
0	0	0000h – FFFFh	External Data Memory (default)
0	1	0000h – 03FFh 0400h – FFFFh	Internal SRAM Data Memory External Data Memory
1	0	Reserved	Reserved
1	1	0000h – 03FFh 0400h – FFFBh FFFCh FFFDh – FFFFh	Internal SRAM Data Memory Reserved System Control Byte (EPROM Read Only) Reserved

The System Control Byte is a special EPROM location that contains nonvolatile system information. This byte is set during EPROM programming and is not alterable by software. This register can only be read when both Data Memory Enable bits are set. The user must be sure that this location is programmed by the use of a special programming utility supplied with the programming device.

System Control Byte Description (EPROM; FFFCh)

Bits 7–3 — Reserved. These bits will read 1. These bits should be set to 1 during EPROM programming.

LB3, LB2, LB1
Bits 2–0 — **EPROM Program Lock Bit 3–1.** These bits show the status of the firmware security of the on–board EPROM. Bit combinations other than shown are illegal.

LB3	LB2	LB1	EPROM PROTECTION MODE
0	0	0	Unconditional verification, full external operation. Additional EPROM programming allowed without full device erasure.
0	0	1	Verification using encryption, execution of external MOVC instruction on internal program memory is disabled. All other program execution and data memory access allowed. Device must be fully erased before EPROM can be programmed again.
0	1	1	Verification disabled, execution of external MOVC instruction on internal program memory is disabled, and access to internal MOVX data from external program is prohibited. All other program execution and data memory access allowed. Device must be fully erased before EPROM can be programmed again.
1	1	1	Verification disabled, external program execution prohibited. Device must be fully erased before EPROM can be programmed again.

Status Register (STATUS)

	7	6	5	4	3	2	1	0
SFR C5h	PIP	HIP	LIP	XTUP	SPTA1	SPRA1	SPTA0	SPRA0
	R–0	R–0	R–0	R–*	R–0	R–0	R–0	R–0

R=Unrestricted Read, –n=Value after Reset, *=See description

PIP
Bit 7 — **Power Fail Priority Interrupt Status.** When set, this bit indicates that software is currently servicing a power–fail interrupt. It is cleared when the program executes the corresponding RETI instruction. This bit is indeterminate on devices which do not incorporate the power–fail interrupt.

HIP
Bit 6 — **High Priority Interrupt Status.** When set, this bit indicates that software is currently servicing a high priority interrupt. It is cleared when the program executes the corresponding RETI instruction.

LIP
Bit 5 — **Low Priority Interrupt Status.** When set, this bit indicates that software is currently servicing a low priority interrupt. It is cleared when the program executes the corresponding RETI instruction.

XTUP
Bit 4 — **Crystal Oscillator Warm–up Status.** This bit indicates whether the CPU crystal oscillator has completed the 65,536 cycle warm–up and is ready to operate from the external crystal or oscillator. This bit is cleared each time the crystal oscillator is restarted following an exit from Stop mode or the XTOFF bit (PMR.3) is set. While cleared, this bit prevents software from setting the XT/$\overline{RG}$ bit (EXIF.3) to enable operation from the crystal. Note that XTUP differs from the RGMD bit (EXIF.2) in that XTUP shows the status of

the crystal while RGMD shows the current clock source. This bit is set to 1 following a power–on reset, but is unaffected by other forms of reset.

SPTA1
Bit 3

Serial Port 1 Transmit Activity Monitor. When set, this bit indicates that data is currently being transmitted by serial port 1. It is cleared when the internal hardware sets the TI_1 bit. Do not alter the Clock Divide Control bits (PMR.7–6) while this bit is set or serial port data may be lost.

SPRA1
Bit 2

Serial Port 1 Receive Activity Monitor. When set, this bit indicates that data is currently being received by serial port 1. It is cleared when the internal hardware sets the RI_1 bit. Do not alter the Clock Divide Control bits (PMR.7–6) while this bit is set or serial port data may be lost.

SPTA0
Bit 1

Serial Port 0 Transmit Activity Monitor. When set, this bit indicates that data is currently being transmitted by serial port 0. It is cleared when the internal hardware sets the TI_0 bit. Do not alter the Clock Divide Control bits (PMR.7–6) while this bit is set or serial port data may be lost.

SPRA0
Bit 0

Serial Port 0 Receive Activity Monitor. When set, this bit indicates that data is currently being received by serial port 0. It is cleared when the internal hardware sets the RI_0 bit. Do not alter the Clock Divide Control bits (PMR.7–6) while this bit is set or serial port data may be lost.

Timed Access Register (TA)

	7	6	5	4	3	2	1	0
SFR C7h	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0
	W–1	W–1	W–1	W–1	W–1	W–1	W–1	W–1

W=Unrestricted Write, –n=Value after Reset

TA.7–0
Bits 7–0

Timed Access. Correctly accessing this register permits modification of timed access protected bits. Write AAh to this register first, followed within 3 cycles by writing 55h. Timed access protected bits can then be modified for a period of 3 cycles measured from the writing of the 55h.

Timer 2 Control (T2CON)

	7	6	5	4	3	2	1	0
SFR C8h	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/RL2
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

TF2
Bit 7

Timer 2 Overflow Flag. This flag will be set when Timer 2 overflows from FFFFh or the count equal to the capture register in down count mode. It must be cleared by software. TF2 will only be set if RCLK and TCLK are both cleared to 0.

EXF2
Bit 6

Timer 2 External Flag. A negative transition on the T2EX pin (P1.1) or timer 2 underflow/overflow will cause this flag to set based on the CP/$\overline{RL2}$ (T2CON.0), EXEN2 (T2CON.3), and DCEN (T2MOD.0) bits. If set by a neg-

ative transition, this flag must be cleared to 0 by software. Setting this bit in software or detection of a negative transition on the T2EX pin will force a timer interrupt if enabled.

CP/$\overline{RL2}$	EXEN2	DCEN	RESULT
1	0	x	Negative transitions on P1.1 will not affect this bit.
1	1	x	Negative transitions on P1.1 will set this bit.
0	0	0	Negative transitions on P1.1 will not affect this bit.
0	1	0	Negative transitions on P1.1 will set this bit.
0	x	1	Bit toggles whenever timer 2 underflows/over-flows and can be used as a 17th bit of resolution. In this mode, EXF2 will not cause an interrupt.

RCLK
Bit 5

Receive Clock Flag. This bit determines the serial port 0 timebase when receiving data in serial modes 1 or 3.
0=Timer 1 overflow is used to determine receiver baud rate for serial port 0.
1=Timer 2 overflow is used to determine receiver baud rate for serial port 0.
Setting this bit will force timer 2 into baud rate generation mode. The timer will operate from a divide by 2 of the external clock.

TCLK
Bit 4

Transmit Clock Flag. This bit determines the serial port 0 timebase when transmitting data in serial modes 1 or 3.
0=Timer 1 overflow is used to determine transmitter baud rate for serial port 0.
1=Timer 2 overflow is used to determine transmitter baud rate for serial port 0. Setting this bit will force timer 2 into baud rate generation mode. The timer will operate from a divide by 2 of the external clock.

EXEN2
Bit 3

Timer 2 External Enable. This bit enables the capture/ reload function on the T2EX pin if Timer 2 is not generating baud rates for the serial port.
0=Timer 2 will ignore all external events at T2EX.
1=Timer 2 will capture or reload a value if a negative transition is detected on the T2EX pin.

TR2
Bit 2

Timer 2 Run Control. This bit enables/disables the operation of timer 2. Halting this timer will preserve the current count in TH2, TL2.
0=Timer 2 is halted.
1=Timer 2 is enabled.

C/$\overline{T2}$
Bit 1

Counter/Timer Select. This bit determines whether timer 2 will function as a timer or counter. Independent of this bit, timer 2 runs at 2 clocks per tick when used in either baud rate generator or clock output mode.
0=Timer 2 function as a timer. The speed of timer 2 is determined by the T2M bit (CKCON.5).
1=Timer 2 will count negative transitions on the T2 pin (P1.0).

CP/$\overline{RL2}$
Bit 0

Capture/Reload Select. This bit determines whether the capture or reload function will be used for timer 2. If either RCLK or TCLK is set, this bit will not function and the timer will function in an auto–reload mode following each overflow.
0=Auto–reloads will occur when timer 2 overflows or a falling edge is detected on T2EX if EXEN2=1.

1=Timer 2 captures will occur when a falling edge is detected on T2EX if EXEN2=1.

Timer 2 Mode (T2MOD)

	7	6	5	4	3	2	1	0
SFR C9h	–	–	–	–	–	–	T2OE	DCEN
							RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

Bits 7–2 Reserved. Read data will be indeterminate.

T2OE Bit 1 **Timer 2 Output Enable.** This bit enables/disables the clock output function of the T2 pin (P1.0).
0=The T2 pin functions as either a standard port pin or as a counter input for timer 2.
1=Timer 2 will drive the T2 pin with a clock output if C/$\overline{T2}$=0. Also, timer 2 rollovers will not cause interrupts.

DCEN Bit 0 **Down Count Enable.** This bit, in conjunction with the T2EX pin, controls the direction that timer 2 counts in 16–bit auto–reload mode.

DCEN	T2EX	DIRECTION
1	1	Up
1	0	Down
0	x	Up

Timer 2 Capture LSB (RCAP2L)

	7	6	5	4	3	2	1	0
SFR CAh	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

RCAP2L.7–0 Bits 7–0 **Timer 2 Capture LSB.** This register is used to capture the TL2 value when timer 2 is configured in capture mode. RCAP2L is also used as the LSB of a 16–bit reload value when timer 2 is configured in auto–reload mode.

Timer 2 Capture MSB (RCAP2H)

	7	6	5	4	3	2	1	0
SFR CBh	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

RCAP2H.7–0
Bits 7–0

Timer 2 Capture MSB. This register is used to capture the TH2 value when timer 2 is configured in capture mode. RCAP2H is also used as the MSB of a 16–bit reload value when timer 2 is configured in auto–reload mode.

Timer 2 LSB (TL2)

	7	6	5	4	3	2	1	0
SFR CCh	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

TL2.7–0
Bits 7–0

Timer 2 LSB. This register contains the least significant byte of Timer 2.

Timer 2 MSB (TH2)

	7	6	5	4	3	2	1	0
SFR CDh	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

TH2.7–0
Bits 7–0

Timer 2 MSB. This register contains the most significant byte of Timer 2.

Program Status Word (PSW)

	7	6	5	4	3	2	1	0
SFR D0h	CY	AC	F0	RS1	RS0	OV	F1	PARITY
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

CY
Bit 7

Carry Flag. This bit is set when if the last arithmetic operation resulted in a carry (during addition) or a borrow (during subtraction). Otherwise it is cleared to 0 by all arithmetic operations.

AC
Bit 6

Auxiliary Carry Flag. This bit is set to 1 if the last arithmetic operation resulted in a carry into (during addition), or a borrow (during subtraction) from the high order nibble. Otherwise it is cleared to 0 by all arithmetic operations.

F0
Bit 5

User Flag 0. This is a bit–addressable, general purpose flag for software control.

RS1, RS0
Bits 4–3

Register Bank Select 1–0. These bits select which register bank is addressed during register accesses.

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00h – 07h
0	1	1	08h – 0Fh
1	0	2	10h – 17h
1	1	3	18h – 1Fh

OV
Bit 2

Overflow Flag. This bit is set to 1 if the last arithmetic operation resulted in a carry (addition), borrow (subtraction), or overflow (multiply or divide). Otherwise it is cleared to 0 by all arithmetic operations.

F1
Bit 1

User Flag 1. This is a bit–addressable, general purpose flag for software control.

PARITY
Bit 0

Parity Flag. This bit is set to 1 if the modulo–2 sum of the eight bits of the accumulator is 1 (odd parity); and cleared to 0 on even parity.

Watchdog Control (WDCON)

	7	6	5	4	3	2	1	0
SFR D8h	SMOD	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
	RW–0	RT–*	RW–0	RW–*	RT–0	RW–*	RT–*	RT–0

R=Unrestricted Read, W=Unrestricted Write, T=Timed Access Write Only, –n=Value after Reset, *=See description

SMOD
Bit 7

Serial Modification. This bit controls the doubling of the serial port 1 baud rate in modes 1, 2, and 3.
0=Serial port 1 baud rate operates at normal speed
1=Serial port 1 baud rate is doubled.

POR
Bit 6

Power–on Reset Flag. This bit indicates whether the last reset was a power–on reset. This bit is typically interrogated following a reset to determine if the reset was caused by a power–on reset. It must be cleared by a Timed Access write before the next reset of any kind or the software may erroneously determine that another power–on reset has occurred. This bit is set following a power–on reset and unaffected by all other resets. Note: This bit is not Timed Access protected on the DS80C310.
0=Last reset was from a source other than a power–on reset
1=Last reset was a power–on reset.

EPFI
Bit 5

Enable Power fail Interrupt. This bit enables/disables the ability of the internal band–gap reference to generate a power–fail interrupt when V_{CC} falls below approximately 4.5 volts. While in Stop mode, both this bit and the Band–gap Select bit, BGS (EXIF.0), must be set to enable the power–fail interrupt.
0=Power–fail interrupt disabled.
1=Power–fail interrupt enabled during normal operation. Power–fail interrupt enabled in Stop mode if BGS is set.

PFI
Bit 4

Power fail Interrupt Flag. When set, this bit indicates that a power–fail interrupt has occurred. This bit must be cleared in software before exiting the interrupt service routine, or another interrupt will be generated. Setting this bit in software will generate a power–fail interrupt, if enabled.

WDIF
Bit 3

Watchdog Interrupt Flag. This bit, in conjunction with the Watchdog Timer Interrupt Enable bit, EWDI (EIE.4), and Enable Watchdog Timer Reset bit (WDCON.1), indicates if a watchdog timer event has occurred and what action will be taken. This bit must be cleared in software before exiting the interrupt service routine, or another interrupt will be generated. Setting this bit in software will generate a watchdog interrupt if enabled. This bit can only be modified using a Timed Access Procedure.

EWT	EWDI	WDIF	RESULT
x	x	0	No watchdog event has occured.
0	0	1	Watchdog time–out has expired. No interrupt has been generated.
0	1	1	Watchdog interrupt has occured.
1	0	1	Watchdog time–out has expired. No interrupt has been generated. Watchdog timer reset will occur in 512 cycles if RWT is not strobed.
1	1	1	Watchdog interrupt has occurred. Watchdog timer reset will occur in 512 cycles if RWT is not set using a Timed Access procedure.

WTRF
Bit 2

Watchdog Timer Reset Flag. When set, this bit indicates that a watchdog timer reset has occurred. It is typically interrogated to determine if a reset was caused by watchdog timer reset. It is cleared by a power–on reset, but otherwise must be cleared by software before the next reset of any kind or software may erroneously determine that a watchdog timer reset has occurred. Setting this bit in software will not generate a watchdog timer reset. If the EWT bit is cleared, the watchdog timer will have no effect on this bit.

EWT
Bit 1

Enable Watchdog Timer Reset. This bit enables/disables the ability of the watchdog timer to reset the device. This bit has no effect on the ability of the watchdog timer to generate a watchdog interrupt. The time–out period of the watchdog timer is controlled by the Watchdog Timer Mode Select bits (CKCON.7–6). Clearing this bit will disable the ability of the watchdog timer to generate a reset, but have no affect on the timer itself, or its ability to generate a watchdog timer interrupt. This bit can only be modified using a Timed Access Procedure. The default power–on reset state of this bit is 0 on the

ROMless devices. If the device contains EPROM program memory, the default power–on reset state of EWT is determined by the Watchdog Default POR State bit (WDPOR) located in the System Control Byte. If the device contains mask ROM program memory, the default power–on reset state is determined by a mask option.
0=A timeout of the watchdog timer will not cause the device to reset.
1=A timeout of the watchdog timer will cause the device to reset.

RWT
Bit 0

Reset Watchdog Timer. Setting this bit will reset the watchdog timer count. This bit must be set using a Timed Access procedure before the watchdog timer expires, or a watchdog timer reset and/or interrupt will be generated if enabled. The time–out period is defined by the Watchdog Timer Mode Select bits (CKCON.7–6). This bit will always be 0 when read.

Accumulator (A or ACC)

	7	6	5	4	3	2	1	0
SFR E0h	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

ACC.7–0
Bits 7–0

Accumulator. This register serves as the accumulator for arithmetic operations. It is functionally identical to the accumulator found in the 80C32.

Extended Interrupt Enable (EIE)

	7	6	5	4	3	2	1	0
SFR E8h	–	–	ERTCI	EWDI	EX5	EX4	EX3	EX2
			RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

Bit 7–6

Reserved. Read data will be indeterminate.

ERTCI
Bit 5

Real Time Clock Interrupt Enable. This bit enables/disables the real–time clock interrupt on the DS87C530. This bit will read 0 on all other devices.
0=Disable the real–time clock interrupt.
1=Enable interrupt requests generated by the real–time clock.

EWDI
Bit 4

Watchdog Interrupt Enable. This bit enables/disables the watchdog interrupt.
0=Disable the watchdog interrupt.
1=Enable interrupt requests generated by the watchdog timer.

EX5
Bit 3

External Interrupt 5 Enable. This bit enables/disables external interrupt 5.
0=Disable external interrupt 5.
1=Enable interrupt requests generated by the $\overline{\text{INT5}}$ pin

EX4
Bit 2

External Interrupt 4 Enable. This bit enables/disables external interrupt 4.
0=Disable external interrupt 4.
1=Enable interrupt requests generated by the INT4 pin

EX3
Bit 1

External Interrupt 3 Enable. This bit enables/disables external interrupt 3.
0=Disable external interrupt 3.
1=Enable interrupt requests generated by the $\overline{INT3}$ pin.

EX2
Bit 0

External Interrupt 2 Enable. This bit enables/disables external interrupt 2.
0=Disable external interrupt 2.
1=Enable interrupt requests generated by the INT2 pin.

B Register (B)

	7	6	5	4	3	2	1	0
SFR F0h	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

B.7–0
Bits 7–0

B Register. This register serves as a second accumulator for certain arithmetic operations. It is functionally identical to the B register found in the 80C32.

Real Time Alarm Subsecond Register (RTASS)

	7	6	5	4	3	2	1	0
SFR F2h	RTASS.7	RTASS.6	RTASS.5	RTASS.4	RTASS.3	RTASS.2	RTASS.1	RTASS.0
	RW–*	RW–*	RW–*	RW–*	RW–*	RW–*	RW–*	RW–*

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset, *=See description

RTASS.7–0
Bits 7–0

Real Time Alarm Subsecond. These bits represent the subsecond alarm which will be compared against the RTC Subsecond register (RTCSS;FAh). The ability of a match between the two registers to cause an alarm is controlled by the RTC Subsecond Register Compare Enable bit (RTCC.7). The contents of this register will be indeterminate following a no–battery reset, and unchanged by all other forms of reset.

Real Time Alarm Second Register (RTAS)

	7	6	5	4	3	2	1	0
SFR F3h	0	0	RTAS.5	RTAS.4	RTAS.3	RTAS.2	RTAS.1	RTAS.0
	R–0	R–0	RW–*	RW–*	RW–*	RW–*	RW–*	RW–*

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset, *=See description

Bits 7–6

Reserved. These bits will be 0 when read.

RTAS.5–0
Bits 5–0

Real Time Alarm Second. These bits represent the second alarm which will be compared against the RTC Second register (RTCS;FBh). The ability of a match between the two registers to cause an alarm is controlled by the RTC Second Register Compare Enable bit (RTCC.6). This register should only be loaded with values from 0 to 3Bh (0 to 59 seconds). The contents of this register will be indeterminate following a no–battery reset (except bits 7, 6), and unchanged by all other forms of reset.

Real Time Alarm Minute Register (RTAM)

	7	6	5	4	3	2	1	0
SFR F4h	0	0	RTAM.5	RTAM.4	RTAM.3	RTAM.2	RTAM.1	RTAM.0
	R–0	R–0	RW–*	RW–*	RW–*	RW–*	RW–*	RW–*

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset, *=See description

Bits 7–6 Reserved. These bits will be 0 when read.

RTAM.5–0
Bits 5–0 **Real Time Alarm Minute.** These bits represent the minute alarm which will be compared against the RTC Minute register (RTCM;FCh). The ability of a match between the two registers to cause an alarm is controlled by the RTC Minute Register Compare Enable bit (RTCC.5).). This register should only be loaded with values from 0 to 3Bh (0 to 59 minutes). The contents of this register will be indeterminate following a no–battery reset (except bits 7, 6), and unchanged by all other forms of reset.

Real Time Alarm Hour Register (RTAH)

	7	6	5	4	3	2	1	0
SFR F5h	0	0	0	RTAH.4	RTAH.3	RTAH.2	RTAH.1	RTAH.0
	R–0	R–0	R–0	RW–*	RW–*	RW–*	RW–*	RW–*

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset, *=See description

Bits 7–5 Reserved. These bits will be 0 when read.

RTAH.4–0
Bits 4–0 **Real Time Alarm Hour.** These bits represent the hour alarm which will be compared against the RTC Hour register (RTCH;FDh). The ability of a match between the two registers to cause an alarm is controlled by the RTC Hour Register Compare Enable bit (RTCC.4). This register should only be loaded with values from 0 to 17h (0 to 23 hours). The day of week bits DOW2–0, located in RTCH.7–5 do not have a corresponding alarm feature. The contents of this register will be indeterminate following a no–battery reset (except bits 7, 6, 5), and unchanged by all other forms of reset.

Extended Interrupt Priority (EIP)

	7	6	5	4	3	2	1	0
SFR F8h	–	–	PRTCI	PWDI	PX5	PX4	PX3	PX2
			RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset

Bit 7–6 Reserved. Read data will be indeterminate.

PRTCI
Bit 5 **Real Time Clock Interrupt Priority.** This bit controls the priority of the real–time clock interrupt on the DS87C530. This bit will read 0 on all other devices.
0=The real–time clock interrupt is a low priority interrupt.
1=The real–time clock interrupt is a high priority interrupt.

PWDI
Bit 4

Watchdog Interrupt Priority. This bit controls the priority of the watchdog interrupt.
0=The watchdog interrupt is a low priority interrupt.
1=The watchdog interrupt is a high priority interrupt.

PX5
Bit 3

External Interrupt 5 Priority. This bit controls the priority of external interrupt 5.
0=External interrupt 5 is a low priority interrupt.
1=External interrupt 5 is a high priority interrupt.

PX4
Bit 2

External Interrupt 4 Priority. This bit controls the priority of external interrupt 4.
0=External interrupt 4 is a low priority interrupt.
1=External interrupt 4 is a high priority interrupt.

PX3
Bit 1

External Interrupt 3 Priority. This bit controls the priority of external interrupt 3.
0=External interrupt 3 is a low priority interrupt.
1=External interrupt 3 is a high priority interrupt.

PX2
Bit 0

External Interrupt 2 Priority. This bit controls the priority of external interrupt 2.
0=External interrupt 2 is a low priority interrupt.
1=External interrupt 2 is a high priority interrupt.

Real Time Clock Control Register (RTCC)

	7	6	5	4	3	2	1	0
SFR F9h	SSCE	SCE	MCE	HCE	RTCRE	RTCWE	RTCIF	RTCE
	RW–*	RW–*	RW–*	RW–*	RW*–0	RT*–0	R*–*	RT–*

R=Unrestricted Read, W=Unrestricted Write, T=Timed Access Write Only, –n=Value after Reset, *=See description

SSCE
Bit 7

RTC Subsecond Register Compare Enable. This bit enables a match between the Real Time Alarm Subsecond Register (RTASS;F2h) and the Real Time Clock Subsecond Register (RTCSS;FAh) to contribute to the RTC interrupt request. This bit will be indeterminate following a no–battery reset, and is unaffected by all other resets.
0=The subsecond value is a Don't Care when evaluating the RTC alarm. If any other alarm register compare bits are enabled, this will cause one interrupt per subsecond tick (1/256 second) for as long as the other registers match.
1=Include the subseconds along with any other registers when evaluating alarm compare conditions.

SCE
Bit 6

RTC Second Register Compare Enable. This bit enables a match between the Real Time Alarm Second Register (RTAS;F3h) and the Real Time Clock Second Register (RTCS;FBh) to contribute to the RTC interrupt request. This bit will be indeterminate following a no–battery reset, and is unaffected by all other resets.
0=The second value is a Don't Care when evaluating an RTC alarm. If any other alarm register compare bits are enabled, this will cause one interrupt per second as long as the other registers match.
1=Include the second along with any other registers when evaluating alarm compare conditions.

MCE
Bit 5

RTC Minute Register Compare Enable. This bit enables a match between the Real Time Alarm Minute Register (RTAM;F4h) and the Real Time Clock Minute Register (RTCM;FCh) to contribute to the RTC interrupt request. This bit will be indeterminate following a no–battery reset, and is unaffected by all other resets.
0=The minute value is a Don't Care when evaluating an RTC alarm. If any other alarm register compare bits are enabled, this will cause one interrupt per minute as long as the other registers match.
1=Include the minute along with any other registers when evaluating alarm compare conditions.

HCE
Bit 4

RTC Hour Register Compare Enable. This bit enables a match between the Real Time Alarm Hour Register (RTAH;F5h) and the Real Time Clock Hour Register (RTCH;FDh) to contribute to the RTC interrupt request. This bit will be indeterminate following a no–battery reset, and is unaffected by all other resets.
0=The hour value is a Don't Care when evaluating an RTC alarm. If any other alarm register compare bits are enabled, this will cause one interrupt per hour for as long as the other registers match.
1=Include the hour along with any other registers when evaluating alarm compare conditions.

RTCRE
Bit 3

RTC Read Enable. This bit temporarily halts internal updating of the RTC to allow software to read the current time. No loss of time will occur. This bit will be cleared to 0 following any reset. Attempts to set the RTCRE and RTCWE bits simultaneously will be ignored. When this bit is cleared, software must wait 4 machine cycles before setting either the RTCRE or RTCWE bit again.
0=Reads of the RTC clock registers (RTCSS;FAh, RTCS;FBh, RTCM;FCh, RTCH;FDh, RTCD0;FEh, RTCD1;FFh) are prohibited and will return erroneous values.
1=Reads of the RTC clock registers are permitted during a 1 ms window starting from the time the bit is set. Immediately after setting this bit, software must wait 4 machine cycles to allow all time registers to synchronize. This bit should be cleared by the user when the desired reads are complete, although it will clear automatically within 1.95 ms if not cleared in software.

RTCWE
Bit 2

RTC Write Enable. This bit temporarily halts the RTC to allow software to update the current time. No loss of time will occur. This bit can only be modified using a Timed Access procedure. Changing this bit from 1 to 0 will reset the RTCSS register to 00h.This bit will be cleared to 0 following any reset.
0=Writes to the RTC clock registers (RTCSS;FAh, RTCS;FBh, RTCM;FCh, RTCH;FDh, RTCD0;FEh, RTCD1;FFh) are ignored. Attempts to set the RTCRE and RTCWE bits simultaneously will be ignored. When this bit is cleared, software must wait 4 machine cycles before setting either the RTCRE or RTCWE bit again.
1=Writes to the RTC clock registers are permitted during a 1 ms window starting from the time this bit is set. Immediately after setting this bit, software must wait 4 machine cycles to allow all time registers to synchronize. This bit should be cleared by the user when the desired updates are complete, although it will clear automatically after 1.95 ms if not cleared in software.

RTCIF
Bit 1

RTC Interrupt Flag. This bit indicates that a RTC alarm match has been made between all the enabled alarm registers and their corresponding clock registers. This bit will generate an RTC Interrupt if the ERTCI bit (EIE.5) is set, and must be cleared by software following an interrupt. RTC interrupts cannot be generated by setting this bit. Clearing all alarm compare enable bits (RTCC.7–4) will also clear this bit. This bit will be indeterminate following a no–battery reset, and is unaffected by all other resets. This bit cannot be set in software.
0=No RTC interrupts are pending.
1=RTC Interrupt is pending/active.

RTCE
Bit 0

RTC Enable. This bit enables/disables the RTC oscillator, halting the RTC. This bit must be accessed using a Timed Access procedure. This bit will be indeterminate following a no–battery reset, and is unaffected by all other resets. If RTC operation is desired, it must be enabled following battery application.
0=RTC oscillator is disabled.
1=RTC oscillator is enabled.

Real Time Clock Subsecond Register (RTCSS)

	7	6	5	4	3	2	1	0
SFR FAh	RTCSS.7	RTCSS.6	RTCSS.5	RTCSS.4	RTCSS.3	RTCSS.2	RTCSS.1	RTCSS.0
	R*–*	R*–*	R*–*	R*–*	R*–*	R*–*	R*–*	R*–*

R=Unrestricted Read, –n=Value after Reset, *=See description

RTCSS.7–0
Bits 7–0

Real Time Clock Subseconds. This register represents the subsecond value of the RTC. It can be read only when the RTCRE bit is set, and writes are not permitted. It is reset to 00h when the RTCWE bit is cleared. The register counts from 0h to FFh.

Real Time Clock Second Register (RTCS)

	7	6	5	4	3	2	1	0
SFR FBh	0	0	RTCS.5	RTCS.4	RTCS.3	RTCS.2	RTCS.1	RTCS.0
	R*–0	R*–0	R*W*–*	R*W*–*	R*W*–*	R*W*–*	R*W*–*	R*W*–*

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset, *=See description

Bits 7–6

Reserved. These bits will be 0 when read.

RTCS.5–0
Bits 5–0

Real Time Clock Seconds. This register represents the second value of the RTC. This register can be read only when the RTCRE bit is set, and can only be modified when the RTCWE bit is set. Consult the description of the RTCWE bit for the programming protocol for this register. This register counts from 0h to 3Bh (0 to 59 seconds), and any writes to this register outside of that range will generate an inaccurate count.

Real Time Clock Minute Register (RTCM)

	7	6	5	4	3	2	1	0
SFR FCh	0	0	RTCM.5	RTCM.4	RTCM.3	RTCM.2	RTCM.1	RTCM.0
	R*–0	R*–0	R*W*–*	R*W*–*	R*W*–*	R*W*–*	R*W*–*	R*W*–*

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset, *=See description

Bits 7–6 Reserved. These bits will be 0 when read.

RTCM.5–0
Bits 5–0 **Real Time Clock Minutes.** This register represents the minute value of the RTC. This register can be read only when the RTCRE bit is set, and can only be modified when the RTCWE bit is set. Consult the description of the RTCWE bit for the programming protocol for this register. This register counts from 0h to 3Bh (0 to 59 minutes), and any writes to this register outside of that range will generate an inaccurate count.

Real Time Clock Hour Register (RTCH)

	7	6	5	4	3	2	1	0
SFR FDh	DOW2	DOW1	DOW0	RTCH.4	RTCH.3	RTCH.2	RTCH.1	RTCH.0
	R*W*–*	R*W*–*	R*W*–*	R*W*–*	R*W*–*	R*W*–*	R*W*–*	R*W*–*

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset, *=See description

DOW2–0
Bits 7–5 **Real Time Clock Day of the Week.** These bits represent the current day of the week. This register can be read only when the RTCRE bit is set, and can only be modified when the RTCWE bit is set. Consult the description of the RTCWE bit for the programming protocol for this register. This register counts from 1h to 7h, and increments when the hour value of the RTC (RTCH.4–0) rolls over from 17h to 0h. Writing a 0h to these bits will disable the day of week function and the count will remain 0. No alarm corresponds to these bits.

RTCH.4–0
Bits 4–0 **Real Time Clock Hours.** These bits represent the hour value of the RTC. This register can be read only when the RTCRE bit is set, and can only be modified when the RTCWE bit is set. Consult the description of the RTCWE bit for the programming protocol for this register. This register counts from 0h to 17h (0 to 23 hours), and any writes outside of that range will generate an inaccurate count.

Real Time Clock Day Register 0 (RTCD0)

	7	6	5	4	3	2	1	0
SFR FEh	RTCD0.7	RTCD0.6	RTCD0.5	RTCD0.4	RTCD0.3	RTCD0.2	RTCD0.1	RTCD0.0
	R*W*–*	R*W*–*	R*W*–*	R*W*–*	R*W*–*	R*W*–*	R*W*–*	R*W*–*

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset, *=See description

RTCD0.7–0
Bits 7–0

Real Time Clock Day Register 0. This register contains the least significant byte of the 16–bit current day count. This is not an absolute value tied to a specific calendar date, but rather a relative day count defined by the user. This register can be read only when the RTCRE bit is set, and can only be modified when the RTCWE bit is set. Consult the description of the RTCWE bit for the programming protocol for this register. The register counts from 0h to FFh. No alarm corresponds to these bits.

Real Time Clock Day Register 1 (RTCD1)

	7	6	5	4	3	2	1	0
SFR FFh	RTCD1.7	RTCD1.6	RTCD1.5	RTCD1.4	RTCD1.3	RTCD1.2	RTCD1.1	RTCD1.0
	R*W*–*	R*W*–*	R*W*–*	R*W*–*	R*W*–*	R*W*–*	R*W*–*	R*W*–*

R=Unrestricted Read, W=Unrestricted Write, –n=Value after Reset, *=See description

RTCD1.7–0
Bits 7–0

Real Time Clock Day Register 1. This register contains the most significant byte of the 16–bit current day count. This is not an absolute value tied to a specific calendar date, but rather a relative day count defined by the user. This register can be read only when the RTCRE bit is set, and can only be modified when the RTCWE bit is set. Consult the description of the RTCWE bit for the programming protocol for this register. The register counts from 0h to FFh. A rollover of this register will clear RTCD1 and RTCD0. No alarm corresponds to these bits.

INSTRUCTION TIMING

All instructions in the High–Speed Microcontroller perform the same functions as their 80C32 counterparts. Their effect on bits, flags, and other status functions is identical. However, the timing of each instruction is different. This applies both in absolute terms of nanoseconds for a given crystal, and in relative terms of clocks.

For absolute timing of real–time events, the timing of software loops will need to be calculated using the data provided in Section 16, Instruction Set Details. However, timers default to run at the older 12 clocks per timer increment. Therefore, while software runs at higher speed, timer–based events need no modification.

The relative time of two instructions might be different in the new architecture than it was previously. For example, both the one–byte, two–cycle "MOVX A, @DPTR" instruction and the three–byte, two–cycle "MOV direct, direct" instruction used two cycles. Therefore, they required the same amount of time. In the High–Speed Microcontroller, the MOVX instruction uses two cycles but the "MOV direct, direct" uses three cycles. While both are faster than their original counterparts, they now have different execution times from each other. This is because the High–Speed Microcontroller typically uses one cycle for each byte. This is generally true for all instructions except for MUL, DIV, MOVC, MOVX, and branch type instructions. These require more cycles than the number of bytes involved. The timing of each instruction should be examined for familiarity with the changes. Note that a machine cycle now requires just four clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV.

ADDRESSING MODES

The High–Speed Microcontroller uses the standard 8051 instruction set which is supported by a wide range of third party assemblers and compilers. Like the 8051, the High–Speed Microcontroller uses three memory areas. These are program memory, data memory, and Registers. Both the program and data areas are 64KB each. They extend from 0000h to FFFFh. The register areas are located between 00h and FFh, but do not overlap with the program and data segments. This is because the High–Speed Microcontroller uses different modes of addressing to reach each memory segment. These modes are described below.

Program memory is the area from which all instructions are fetched. It is inherently read only. This is because the 8051 instruction set provides no instructions that write to this area. Read/write access is for data memory and Registers only. No special action is required to fetch from program memory. Each instruction fetch will be performed automatically by the on–chip hardware. In versions that contain on–chip memory, the hardware will decide whether the fetch is on–chip or off–chip based on the address.

Explicit addressing modes are needed for the data memory and register areas. These modes determine which register area is accessed or if off–chip data memory is used.

The High–Speed Microcontroller supports eight addressing modes. They are:

- Register Addressing
- Direct Addressing
- Register Indirect Addressing
- Immediate Addressing
- Register Indirect Addressing with Displacement
- Relative Addressing
- Page Addressing
- Extended Addressing

Five of the eight are used to address operands. The remainder are used for program control and branching. When writing assembly language instructions that use arguments, the convention is destination, source. Each mode of addressing is summarized below. Note that many instructions (such as ADD) have multiple addressing modes available..

Register Addressing

Register Addressing is used for operands that are located in one of the eight Working Registers (R7–R0). These are the currently selected Working Register bank, which reside in the lower 32 bytes of Scratchpad RAM. A register bank is selected using two bits in the Program Status Word (PSW;D0h). This addressing mode is powerful, since it uses the active bank without knowing which bank is selected. Thus one instruction can have multiple uses by simply switching banks. Register Addressing is also a high–speed instruction, requiring only one machine cycle. Two examples of Register Addressing are provided below.

```
ADD     A, R4       ;Add Accumulator to register R4

INC     R2          ;Increment the value in register R2
```

In the first case, the value in R4 is the source of the operation. In the later, R2 is the destination. These instructions do not consider the absolute address of the register. They will act on whichever bank has been selected.

Any Working Register may also be accessed by Direct Addressing, described below. To do this, the absolute address must be specified.

Direct Addressing

Direct Addressing is the mode used to access the entire lower 128 bytes of Scratchpad RAM and the SFR area. It is commonly used to move the value in one register to another. Two examples are shown below.

```
MOV     72h, 74h    ;Move the value in register 74 to
                    ; register 72.

MOV     90h, 20h    ;Move the value in register 20 to
                    ; the SFR at 90h (Port 1)
```

Note that there is no instruction difference between a RAM access and an SFR access. The SFRs are simply register locations above 7Fh.

Direct Addressing also extends to bit addressing. There is a group of instructions that explicitly use bits. The address information provided to such an instruction is the bit location, rather than the register address. Registers between 20h and 2Fh contain bits that are individually addressable. SFRs that end in 0 or 8 are bit addressable. An example of Direct Bit Addressing is as follows.

```
SETB    00h         ;Set bit 00 in the RAM. This is the
                    ; LSb of the register at address 20h
                    ; as shown in Section 4.

MOV     C, 0B7h     ;Move the contents of bit B7 to the
                    ; Carry flag. Bit B7 is the MSb of
                    ; register B0 (Port 3).
```

Register Indirect Addressing

This mode is used to access the Scratchpad RAM locations above 7Fh. It can also be used to reach the lower RAM (0h – 7Fh) if needed. The address is supplied by the contents of the Working Register specified in the instruction. Thus one instruction can be used to reach many values by altering the contents of the designated Working Register. Note that in general, only R0 and R1 can be used as pointers. An example of Register Indirect Addressing is as follows.

```
ANL     A, @R0      ;Logical AND the Accumulator
                    ; with the contents of the register
                    ; pointed to by the value stored in
                    ; R0.
```

This mode is also used for Stack manipulation. This is because all Stack references are directed by the value in the Stack Pointer register. The Push and Pop instructions use this method of addressing. An example is as follows.

```
PUSH    A           ;Saves the contents of the
                    ; accumulator on the stack.
```

Register Indirect Addressing is used for all off–chip data memory accesses. These involve the MOVX instruction. The pointer registers can be R0, R1, DPTR0 and DPTR1. Both R0 and R1 reside in the Working Register area of the Scratchpad RAM. They can be used to reference a 256 byte area of off–chip data memory. When using this type of addressing, the upper address byte is supplied by the value in the Port 2 latch. This value must be selected by software prior to the MOVX instruction. An example is as follows.

```
MOVX    @R0, A      ;Write the value in the accumulator
                    ; to the address pointed to by R0 in
                    ; the page pointed to by P2.
```

The 16–bit Data pointers (DPTRs) can be used as an absolute off–chip reference. This gives access to the entire 64KB data memory map. An example is as follows.

```
MOVX @DPTR, A   ;Write the value in the accumulator
                ; to the address referenced by the
                ; selected data pointer.
```

Immediate Addressing

Immediate Addressing is used when one of the operands is predetermined and coded into the software. This mode is commonly used to initialize SFRs and to mask particular bits without affecting others. An example is as follows.

```
ORL     A, #40h     ;Logical OR the Accumulator
                    ; with 40h.
```

Register Indirect with Displacement

Register Indirect Addressing with Displacement is used to access data in lookup tables in program memory space. The location is created using a base address with an index. The base address can be either the PC or the DPTR. The index is the accumulator. The result is stored in the accumulator. An example is as follows.

```
MOVC  A, @A+DPTR    ;Load the accumulator with the
                    ; contents of program memory
                    ; pointed to by the contents of
                    ; the DPTR plus the value in
                    ; the accumulator.
```

Relative Addressing

Relative Addressing is used to determine a destination address for Conditional branch. Each of these instructions includes an 8–bit value that contains a two's complement address offset (–127 to +128) which is added to the PC to determine the destination address. This destination is branched to when the tested condition is true. The PC points to the program memory location immediately following the branch instruction when the offset is added. If the tested condition is not true, the next instruction is performed. An example is as follows.

```
JZ      $–20        ;Branch to the location (PC+2)–20
                    ; if the contents of the accumulator
                    ;=0.
```

Page Addressing

Page Addressing is used by the Branching instructions to specify a destination address within the same 2KB block as the next contiguous instruction. The full 16–bit address is calculated by taking the five highest order bits for the next instruction (PC+2) and concatenating them with the lowest order 11 bit field contained in the current instruction. An example is as follows.

```
0870h   ACALL100h   ;Call to the subroutine at
                    ; address 100h plus the
                    ; current page address.
```

In this example, the current page address is 800h, so the destination address is 900h.

Extended Addressing

Extended Addressing is used by the Branching instructions to specify a 16–bit destination address within the 64KB address space. The destination address is fixed in software as an absolute value. An example is as follows.

```
LJMP    0F732h      ; Jump to address 0F732h.
```

PROGRAM STATUS FLAGS

All Program Status Flags are contained in the Program Status Word at SFR location D0h. It contains flags that reflect the status of the CPU and the result of selected operations. The flags are summarized below. The following table shows the instructions that affect each flag.

Bit Description :

PSW.7 **C**
Carry
Set when the previous operation resulted in a carry (during addition) or a borrow (during subtraction), otherwise cleared.

PSW.6 **AC**
Auxiliary Carry
Set when the previous operation resulted in a carry (during addition) or a borrow (during subtraction) from the high order nibble. Otherwise cleared.

PSW.2 **OV**
Overflow
Set when a carry was generated into the high order bit but not a carry out of the high order bit. OV is normally used with 2's complement arithmetic.

PSW.0 **P**
Parity
Set to logic 1 to indicate an odd number of ones in the accumulator (odd parity). Cleared for an even number of ones. This produces even parity.

All of these bits are cleared to a logic 0 for all resets.

INSTRUCTIONS THAT AFFECT FLAG SETTINGS Table 4–4

INSTRUCTION	FLAGS			INSTRUCTION	FLAGS		
	C	OV	AC		C	OV	AC
ADD	X	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C, bit	X		
MUL	0	X		ANL C, $\overline{bit}$	X		
DIV	0	X		ORL C, bit	X		
DA	X			ORL C, $\overline{bit}$	X		
RRC	X			MOV C, bit	X		
RLC	X			CJNE	X		
SETB C	1						

X indicates the modification is according to the result of the instruction.