SECTION 8: RESET CONDITIONS

The High–Speed Microcontroller provides several ways to place the CPU in a reset state. It also offers the means for software to determine the cause of a reset. The reset state of most processor bits is not dependent on the type of reset, but selected bits do depend on the reset source. The reset sources and the reset state are described below.

RESET SOURCES

The High–Speed Microcontroller has three ways of entering a reset state. Each reset source is described below. They are:

Power–on/Power Fail Reset
Watchdog Timer Reset
External Reset

Power–on/Fail Reset

Members of the High–Speed Microcontroller family incorporate an internal voltage reference which holds the CPU in the power–on reset state while V_{CC} is out of tolerance. Once V_{CC} has risen above the threshold, the microcontroller will restart the oscillation of the external crystal and count 65536 clock cycles. The processor will then begin software execution at location 0000h.

The voltage at which the reset state is entered depends on the specific device. If the device does not contain a precision voltage reference, the power–on reset threshold may be anywhere between 0.8V and V_{CCMIN}. If the device incorporates a precision voltage reference, the threshold will be as specified by the V_{RST} parameter in the data sheet. This helps the system maintain reliable operation by only permitting processor operation when voltage is in a know good state.

The processor will exit the reset condition automatically once the above conditions are met. This happens automatically, needing no external components or action. Execution begins at the standard reset vector address of 0000h. Software can determine that a Power–on Reset has occurred using the Power–on Reset flag (POR). It is located at WDCON.6. Since all resets cause a vector to location 0000h, the POR flag allows software to acknowledge that power failure was the reason for a reset.

Software should clear the POR bit after reading it. When a reset occurs, software will be able to determine if a power cycle was the cause. In this way, processing may take a different course for each of the three resets if applicable. When power fails (drops below V_{RST}), the power monitor will invoke the reset state again. This reset condition will remain while power is below the threshold. When power returns above the reset threshold, a full power–on reset will be performed. Thus a brownout that causes V_{CC} to drop below V_{RST} appears the same as a power up.

Watchdog Timer Reset

The Watchdog Timer is a free running timer with a programmable interval. Software can clear the timer at any time, causing the interval to begin again. The Watchdog supervises CPU operation by requiring software to clear it before the time–out expires. If the timer is enabled and software fails to clear it before this interval expires, the CPU is placed into a reset state. The reset state will be maintained for two machine cycles. Once the reset is removed, the software will resume execution at 0000h.

The Watchdog Timer is fully described in Section 11. Software can determine that a Watchdog time–out was the reason for the reset by using the Watchdog Timer Reset flag (WTRF). WTRF is located at WDCON.2. Hardware will set this bit to a logic 1 when the Watchdog times out without being cleared by software if EWT=1. If a Watchdog Timer reset occurs, software should clear this flag manually. This allows software to detect the event if it occurs again.

External Reset

If the RST input is taken to a logic 1, the CPU will be forced into a reset state. This will not occur instantaneously, as the condition must be detected and then clocked into the microcontroller. It requires a minimum of two machine cycles to detect and invoke the reset state. Thus the reset is a synchronous operation and the crystal must be running to cause an external reset.

Once the reset state is invoked, it will be maintained as long as RST=1. When the RST is removed, the CPU will exit the reset state within two machine cycles and begin execution at address 0000h. All registers will default to their power–on reset state. There is no flag to indicate that an external reset was applied. However, since the other two sources have associated flags, the RST pin is the default source when neither POR or WTRF is set.

If a RST is applied while the processor is in the Stop mode, the scenario changes slightly. As mentioned above, the reset is synchronous and requires a clock to

be running. Since the Stop mode stops all clocks, the RST will first cause the oscillator to begin running and force the program counter to 0000h. Rather than a two machine cycle delay as described above, the processor will apply the full power–on delay (65536 clocks) to allow the oscillator to stabilize.

RESET STATE

Regardless of the source of the reset, the state of the microcontroller is the same while in reset. When in reset, the oscillator is running, but no program execution is allowed. When the reset source is external, the user must remove the reset stimulus. When power is applied to the device, the power–on delay removes the stimulus automatically.

Resets do not affect the Scratchpad RAM. Thus any data stored in RAM will be preserved. The contents of internal MOVX data memory will also remain unaffected by a reset. Note that if the power supply dips below approximately 2V, the RAM contents may be lost. The minimum voltage required for RAM data retention in not specified. Since it is impossible to determine if the power was lower than 2V prior to the power–on reset, RAM must be assumed lost when POR is set.

The reset state of SFR bits are described in Section 4. Bits which are marked SPECIAL have conditions which can affect their reset state. Consult the individual bit descriptions for more information. Note that the stack pointer will also be reset. Thus the stack is effectively lost during a reset even though the RAM contents are not altered. Interrupts and Timers are disabled. The state of the Watchdog Timer is dependent on the specific device in use. Note that the Watchdog time out defaults to its shortest interval on any reset. I/O Ports are taken to a weak high state (FFh). This leaves each port pin configured with the data latch set to a 1. Ports do not go to the 1 state instantly when a reset is applied, but will be taken high within two machine cycles of asserting a reset. When the reset stimulus is removed, program execution begins at address 0000h.

NO–BATTERY RESET

The battery backup feature of the DS87C530 introduces a new type of reset condition. Most SFR bits are automatically reset to their default state upon a power–on reset. The external backup battery feature makes some bits non–volatile, however, and these battery–backed bits will not change state when a power–on reset is applied. Upon the loss or initial connection of battery power these bits will default to the state shown in Table 8–1. Any bits not listed below are either unchanged or set to their default state by a power–on reset.

NO–BATTERY RESET DEFAULT Table 8–1

BIT NAME	LOCATION	NO–BATTERY RESET STATE
E4K	TRIM.7	0
X12/6	TRIM.6	1
TRM2	TRIM.5	1
TRM2	TRIM.4	0
TRM1	TRIM.3	0
TRM1	TRIM.2	1
TRM0	TRIM.1	0
TRM0	TRIM.0	1
RTASS.7–0	RTASS.7–0	Indeterminate
RTAS.7–0	RTAS.7–0	Indeterminate
RTAM.7–0	RTAM.7–0	Indeterminate
RTAH.7–0	RTAH.7–0	Indeterminate
SSCE	RTCC.7	Indeterminate
SCE	RTCC.6	Indeterminate
MCE	RTCC.5	Indeterminate
HCE	RTCC.4	Indeterminate
RTCIF	RTCC.1	Indeterminate
RTCE	RTCC.0	Indeterminate
RTCSS.7–0	RTCSS.7–0	Indeterminate
RTCS.7–0	RTCS.7–0	Indeterminate
RTCM.7–0	RTCM.7–0	Indeterminate
RTCH.7–0	RTCH.7–0	Indeterminate
RTCD0.7–0	RTCD1.7–0	Indeterminate
RTCD1.7–0	RTCD1.7–0	Indeterminate

IN–SYSTEM DISABLE MODE

The High Speed Microcontroller Family supports in–circuit debugging of designs. The In–System Disable (ISD) feature allows the device to be tristated for in–circuit emulation or board testing. During ISD mode, the device pins will take on the following states:

DEVICE PIN	STATE DURING ISD
Port 0, 1, 2, 3 RST, $\overline{EA}$	True Tristate
ALE, $\overline{PSEN}$	Weak Pull–up ($\sim$10KΩ)
XTAL1, XTAL2	Oscillator remains active

The following procedure is used to enter ISD mode:

1. Assert reset by pulling RST high,
2. Pull ALE low and pull $\overline{PSEN}$ high,
3. Verify that P2.7, P2.6, P2.5 are not being driven low,
4. Release RST,
5. Hold ALE low and $\overline{PSEN}$ high for at least 2 machine cycles,
6. Device is now in ISD mode. Release ALE and $\overline{PSEN}$ if desired.

Note that pins P2.7, P2.6, P2.5 should not be driven low when RST is released. This will place the device into a reserved test mode. Because these pins have a weak pull–up during reset, they can be left floating. The test mode is only sampled on the falling edge of RST, and once RST is released their state will not effect device operation. In a similar manner, the $\overline{PSEN}$ and RST pins can be released once ISD mode is invoked, and their state will not effect device operation. The RST pin will also be in a tristate mode, but asserting it in ISD mode will return the device to normal operation.