SECTION 13: PROGRAMMABLE TIMERS

FUNCTIONAL DESCRIPTION

The Secure Microcontroller incorporates two 16–bit timers called Timer 0 and Timer 1. Both can be used to generate precise time intervals, measure external pulse widths, or count externally applied pulses.

Each programmable timer operates either as a "timer" in which time periodic interrupts may be generated or as a "counter", in which the timer register is incremented when transitions are detected on an external input pin.

When a programmable timer is operating as a "timer", the least–significant timer register is incremented once every machine cycle or at 1/12 the frequency of the clock oscillator. When a 12 MHz crystal is used, the register will be incremented once every 1 μs.

When "counter" operation is selected, the least–significant timer register is incremented each time that a 1–to–0 transition is detected on the corresponding input pin that may be assigned for the timer (T0 for Timer 0, T1 for Timer 1). These pins are the optional function of P3.4 and P3.5 respectively. The timing of the "counter" mode is internally synchronized to the machine cycles. During S5P2 of every machine cycle, the external input pin is sampled. A 1–to–0 transition is defined as a 1 detected during a machine cycle followed by a 0 detected in the S5P2 clock phase of the next machine cycle. The new count value in the timer register will be present during clock phase S3P1 of the next successive (or third) machine cycle. See the section on timing for details.

The TMOD and TCON Special Function registers are used to control the initialization of the two programmable timers. A summary of the bits contained in TMOD is shown in Figure 13–1. The relevant TCON register bits are depicted in Figure 13–2. Each Timer has four control bits associated with it including C/$\overline{T}$, GATE, M1, and M0. C/$\overline{T}$=1 selects counter operation and C/$\overline{T}$=0 selects timer operation.

A separate GATE bit in the TMOD register is provided for each timer. These bits enable an associated external interrupt input pin as a gating control for the timer or counter function. The P3.2 ($\overline{INT0}$) pin operates in conjunction with Timer 0 while the P3.3 ($\overline{INT1}$) pin operates with Timer 1. When the Timer Run bit (TRn) and GATE are both set to a 1, the timer or counter function will be enabled only during the times that the associated interrupt input pin is at a 1 level. When the Timer function is selected, the GATE bit provides a means of measuring the widths of logic 1 pulses applied to the interrupt pin in units of machine cycles. When the counter function is selected, the pulse is measured in units of 1–to–0 transitions detected on the external counter input pin.

Both of the programmable timers have M1,M0 control bits in the TMOD register which are used to select one of the four operating modes described below.

TMOD REGISTER CONTROL BIT SUMMARY Figure 13–1

Bit Description

TMOD.7 (Timer 1);
TMOD.3 (Timer 0): **GATE**

"Gate Control": When set to 1 with TRns=1, timer/counter's input count pulses will only be delivered while a 1 is present on the $\overline{INT}$ pin. When cleared to 0, counter pulses will always be received by the timer/counter as long as TRn=1.

Initialization: Cleared to 0 on any reset.

TMOD.6 (Timer 1);
TMOD.2 (Timer 0): **C/$\overline{T}$**

"Counter/Timer Select": When set to a 1, the counter function is selected for the associated programmable timer; when cleared to 0, the timer function is selected.

Initialization: Cleared to 0 on any reset.

TMOD.5, TMOD.4: **Timer 1 Mode Control**

"Mode Select" These bit select the operating mode of the associated timer/counter as follows:

M1	M0	
0	0	Mode 0: Eight bits with 5–bit prescale
0	1	Mode 1: 16 bits with no prescale
1	0	Mode 2: Eight bits with auto–reload
1	1	Mode 3: Timer 1 – Stopped

Initialization**:** Cleared to 0 on any reset.

TMOD.1, TMOD.0: **Timer 0 Mode Control**

"Mode Select" These bit select the operating mode of the associated timer/counter as follows:

M1	M0	
0	0	Mode 0: Eight bits with 5–bit prescale
0	1	Mode 1: 16 bits with no prescale
1	0	Mode 2: Eight bits with auto–reload
1	1	Mode 3: Timer 0 – Two 8–bit timers

Initialization**:** Cleared to 0 on any reset.

TCON REGISTER CONTROL/STATUS BITS Figure 13–2

Bit Description:

TCON.7: **TF1**

"Timer 1 Overflow Flag": Status bit set to 1 when Timer 1 overflows from a previous count value of all 1's. Cleared to 0 when CPU vectors to Timer 1 Interrupt service routine.

Initialization: Cleared to 0 on any type of reset.

TCON.6: **TR1**

"Timer 1 Run Control"**:** When set to a 1 by software, Timer 1 operation will be enabled. Timer 1 is disabled when cleared to 0.

Initialization: Cleared to 0 on any type of reset.

TCON.5: **TF0**

"Timer 0 Overflow": Status bit set to 1 when Timer 0 overflows from a previous count value of all 1's. Cleared to 0 when CPU vectors to Timer 0 interrupt service routine.

Initialization: Cleared to 0 on ay type of reset.

TCON.4: **TR0**

"Timer 0 Run Control": When set to a 1 by a software, Timer 0 operation is enabled. Timer 0 is disabled when cleared to 0.

Initialization: Cleared to 0 on any type of reset.

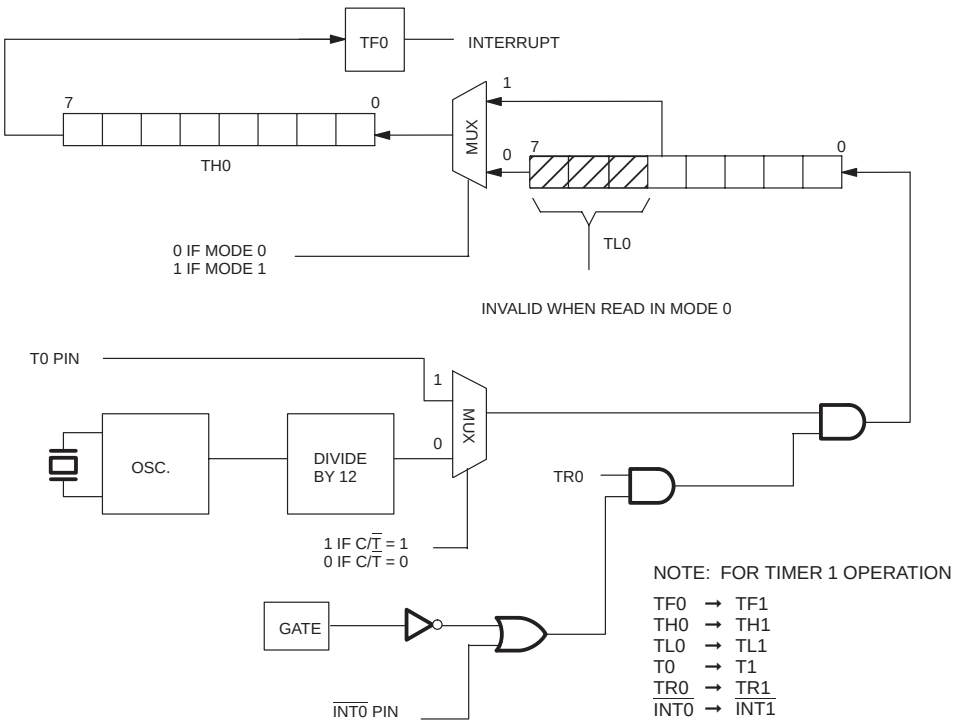
Mode 0

Figure 13–3 is a block diagram of a timer/counter operating in Mode 0. Mode 0 configures either programmable timer for operation as a 13–bit timer/counter. For Timer 0, selection of Mode 0 configures bit 4 – 0 of TL0 as bits 4 – 0 respectively of the 13–bit timer/counter register. In addition, bits 7 – 0 of TH0 are configured as bits 12 – 5 respectively of the 13–bit timer/counter register. Bits 7 – 5 of TL0 are indeterminate and should be ignored when read. All of the timer/counter bits are cleared to 0 by a hardware reset. When the TR0 bit is set with either GATE=0 or $\overline{INT0}$=1, the 13–bit register will be incremented as each count is received. The previous value of the 13–bit register is unchanged when the TR0 bit is set to a 1 from a previous 0 condition.

When the 13–bit timer/counter reaches a value of 1FFFH (all 1's) the next count received will cause the value to roll over to 0000 and the TF0 flag will be set. Additionally, an interrupt will be generated if it had been enabled.

Mode 0 operation for Timer 1 is functionally identical to that described for Timer 0. TH1 and TL1 are used to form the 13–bit register as just described for Timer 0. Likewise, TR1, TF1, and INT1 perform the functions described for TR0, TF0, and $\overline{INT0}$.

TIMER/COUNTER MODE 0 AND 1 OPERATION Figure 13–3



Mode 1

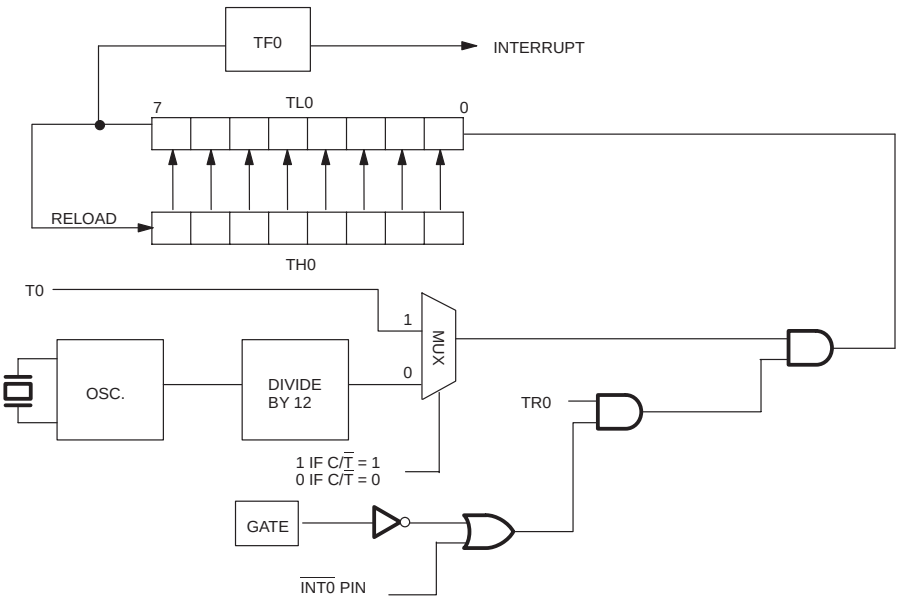
Mode 1 for both programmable timers operates in an identical fashion described for Mode 0, except Mode 1 configures a 16–bit timer/counter register. In this case, for Timer 0, TH0 contains the most significant eight bits of the count value while TL0 holds the least significant eight bits. Timer 1 uses TH1, TL1 in an identical fashion in Mode 1. Figure 13–3 is also a diagram depicting operation in Mode 1 for the timer/counters.

Mode 2

The selection of Mode 2 configures an 8–bit timer/counter with automatic reload of a value preset by software. Figure 13–4 illustrates a functional block diagram of this operational mode. When Timer 0 is used in Mode 2, TL0 is incremented as each count is received. When the value of 0FFH (all 1's) is reached, TF0 will be set on the next count and the reload value held in TH0 will be transferred into TL0. TH0 remains unchanged until it is modified by the application software.

Timer 1 operates in an identical fashion when it is set for operation in Mode 2.

TIMER/COUNTER MODE 2 OPERATION Figure 13–4



Mode 3

When Timer 0 is selected for operation in Mode 3, both TH0 and TL0 are configured independently as an 8–bit timer/counter and as an 8–bit timer. Figure 13–5 illustrates the function of Timer 0 for Mode 3 operation.

For Timer 0 in Mode 3, TL0 becomes an 8–bit timer/counter which is controlled by the Timer 0 control bits (TR0 and TF0) in the TMOD and TCON registers. TL0's count input may be assigned to either the 12 t_{CLK} signal or to the external T0 pin via C/$\overline{T}$ for Timer 0. In addition, the count input may be gated as a function of the $\overline{INT0}$ pin using Timer 0's GATE bit in TMOD.

TH0 becomes an 8–bit timer when Mode 3 is selected for Timer 0. TH0's input can only be the 12 t_{CLK} signal. TR1 and TF1 are assigned for use with TH0 as is the interrupt for Timer 1, which will be generated when TH0 overflows from all 1's.

When Timer 1 is selected for operation in Mode 3, it stops counting and holds its current value. This action is the same as setting TR1=0. When Timer 0 is selected in Mode 3, Timer 1's control bits are stolen as described above. As a result, Timer 1's functions are limited in this MODE. It is forced to operate as a timer whose clock input is 12 t_{CLK} and it cannot generate an interrupt on overflow. In addition, it also cannot be used with the GATE function. However, it can be started and stopped by switching it into or out of Mode 3 or it can be assigned as a baud rate generator for the serial port.

TIMER 0 MODE 3 OPERATION Figure 13–5