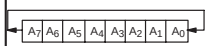
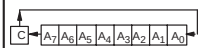
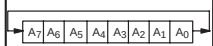
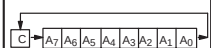
SECTION 19: INSTRUCTION SET DETAILS

	MNEMONIC	INSTRUCTION CODE								HEX	BYTE	CYCLE	EXPLANATION
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				
ARITHMETIC OPERATION	ADD A, Rn	0	0	1	0	1	n_2	n_1	n_0	28–2F	1	1	(A) = (A) + (Rn)
	ADD A, direct	0	0	1	0	0	1	0	1	25	2	1	(A) = (A) + (direct)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	Byte 2			
	ADD A, @Ri	0	0	1	0	0	1	1	i	26–27	1	1	(A) = (A) + ((Ri))
	ADD A, #data	0	0	1	0	0	1	0	0	24	2	1	(A) = (A) + #data
		d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	Byte 2			
	ADDC A, Rn	0	0	1	1	1	n_2	n_1	n_0	38–3F	1	1	(A) = (A)+(C)+(Rn)
	ADDCA,direct	0	0	1	1	0	1	0	1	35	2	1	(A) = (A)+(C)+(direct)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	Byte 2			
	ADDC A, @Ri	0	0	1	1	0	1	1	i	36–37	1	1	(A) = (A)+(C)+((Ri))
	ADDC A,#data	0	0	1	1	0	1	0	0	34	2	1	(A) = (A)+(C)+#data
		d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	Byte 2			
	SUBB A, Rn	1	0	0	1	1	n_2	n_1	n_0	98–9F	1	1	(A) = (A)–(C)–(Rn)
	SUBB A,direct	1	0	0	1	0	1	0	1	95	2	1	(A) = (A)–(C)–(direct)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	Byte 2			
	SUBB A, @Ri	1	0	0	1	0	1	1	i	96–97	1	1	(A) = (A)–(C)–((Ri))
	SUBB A,#data	1	0	0	1	0	1	0	0	94	2	1	(A) = (A)-(C)-#data
		d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	Byte 2			
	INC A	0	0	0	0	0	1	0	0	04	1	1	(A) = (A) + 1
	INC Rn	0	0	0	0	1	n_2	n_1	n_0	08–0F	1	1	(Rn) = (Rn) + 1
	INC direct	0	0	0	0	0	1	0	1	05	2	1	(direct) = (direct)+1
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	Byte 2			
	INC @Ri	0	0	0	0	0	1	1	i	06–07	1	1	((Ri)) = ((Ri)) + 1
	INC DPTR	1	0	1	0	0	0	1	1	A3	1	2	(DPTR)=(DPTR)+1
	DEC A	0	0	0	1	0	1	0	0	14	1	1	(A) = (A) – 1
	DEC Rn	0	0	0	1	1	n_2	n_1	n_0	18–1F	1	1	(Rn) = (Rn) – 1
	DEC direct	0	0	0	1	0	1	0	1	15	2	1	(direct) = (direct)–1
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	Byte 2			
	DEC @Ri	0	0	0	1	0	1	1	i	16–17	1	1	((Ri)) = ((Ri)) –1
	MUL AB	1	0	1	0	0	1	0	0	A4	1	4	$(B_{15–8})$, $(A_{7–0})$ = (A) X (B)
	DIV AB	1	0	0	0	0	1	0	0	84	1	4	$(A_{15–8})$, $(A_{7–0})$ = (A) ÷ (B)

	MNEMONIC	INSTRUCTION CODE								HEX	BYTE	CYCLE	EXPLANATION
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				
ARITHMETIC OPER.	DA A	1	1	0	1	0	1	0	0	D4	1	1	Contents of Accumulator are BCD, IF [[(A_{3-0}) > 9] OR [(AC) = 1]] THEN $(A_{3-0}) = (A_{3-0}) + 6$ AND IF [[(A_{7-4}) > 9] OR [(C) = 1]] THEN $(A_{7-4}) = (A_{7-4}) + 6$
LOGICAL OPERATION	ANL A, Rn	0	1	0	1	1	n_2	n1	n_0	58–5F	1	1	(A) = (A) AND (Rn)
	ANL A, direct	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	0 a_1	1 a_0	55 Byte 2	2	1	(A) = (A) AND (direct)
	ANL A, @Ri	0	1	0	1	0	1	1	i	56–57	1	1	(A) = (A) AND ((Ri))
	ANL A, #data	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	1 d_2	0 d_1	0 d_0	54 Byte 2	2	1	(A)=(A) AND #data
	ANL direct, A	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	52 Byte 2	2	1	(direct) = (direct) AND A
	ANL direct, #data	0 a_7 d_7	1 a_6 d_6	0 a_5 d_5	1 a_4 d_4	0 a_3 d_3	0 a_2 d_2	1 a_1 d_1	1 a_0 d_0	53 Byte 2 Byte 3	3	2	(direct) = (direct) AND #data
	ORL A, Rn	0	1	0	0	1	n_2	n_1	n_0	48–4F	1	1	(A) = (A) OR (Rn)
	ORL A, direct	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	0 a_1	1 a_0	45 Byte 2	2	1	(A) = (A) OR (direct)
	ORL A, @Ri	0	1	0	0	0	1	1	i	46–47	1	1	(A) = (A) OR ((Ri))
	ORL A, #data	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	1 d_2	0 d_1	0 d_0	44 Byte 2	2	1	(A) = (A) OR #data
	ORL direct, A	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	0 a_2	1 a_1	0 a_0	42 Byte 2	2	1	(direct) = (direct) OR (A)
	ORL direct,#data	0 a_7 d_7	1 a_6 d_6	0 a_5 d_5	0 a_4 d_4	0 a_3 d_3	0 a_2 d_2	1 a_1 d_1	1 a_0 d_0	43 Byte 2 Byte 3	3	2	(direct) = (direct) OR #data
	XRL A, Rn	0	1	1	0	1	n_2	n_1	n_0	68–6F	1	1	(A) = (A) XOR (Rn)
	XRL A, direct	0 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	0 a_1	1 a_0	65 Byte 2	2	1	(A) = (A) XOR (direct)
	XRL A, @ Ri	0	1	1	0	0	1	1	i	66–67	1	1	(A) = (A) XOR ((Ri))
	XRL A, #data	0 d_7	1 d6	1 d5	0 d_4	0 d_3	1 d_2	0 d_1	0 d_0	64 Byte 2	2	1	(direct) = (A) XOR #data
	XRL direct, A	0 a_7	1 a_6	1 a_5	0 a_4	0 a_3	0 a_2	1 a_1	0 a_0	62 Byte 2	2	1	(direct) = (direct) XOR (A)
	XRL direct, #data	0 a_7 d_7	1 a_6 d_6	1 a_5 d_5	0 a_4 d_4	0 a_3 d_3	0 a_2 d_2	1 a_1 d_1	1 a_0 d_0	63 Byte 2 Byte 3	3	2	(direct) = (direct) XOR #data
	CLR A	1	1	1	0	0	1	0	0	E4	1	1	(A) = 0
	CPL A	1	1	1	1	0	1	0	0	F4	1	1	(A) = $(\overline{A})$

	MNEMONIC	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX	BYTE	CYCLE	EXPLANATION
LOGICAL OPERATION	RL A	0	0	1	0	0	0	1	1	23	1	1	 The contents of the accumulator are rotated left by one bit.
	RLC A	0	0	1	1	0	0	1	1	33	1	1	 The contents of the accumulator are rotated left by one bit.
	RR A	0	0	0	0	0	0	1	1	03	1	1	 The contents of the accumulator are rotated right by one bit.
	RRC A	0	0	0	1	0	0	1	1	13	1	1	 The contents of the accumulator are rotated right by one bit.
	SWAP A	1	1	0	0	0	1	0	0	C4	1	1	$(A_{3-0}) \leftrightarrows (A_{7-4})$
DATA TRANSFER	MOV A, Rn	1	1	1	0	1	n_2	n_1	n_0	E8–EF	1	1	(A) = (Rn)
	MOV A, direct	1 a_7	1 a_6	1 a_3	0 a_4	0 a_3	1 a_2	0 a_1	1 a_0	E5 Byte 2	2	1	(A) = (direct)
	MOV A, @Ri	1	1	1	0	0	1	1	i	E6–E7	1	1	(A) = ((Ri))
	MOV A, #data	0 d_7	1 d_6	1 d_5	1 d_4	0 d_3	1 d_2	0 d_1	0 d_0	74 Byte 2	2	1	(A) = #data
	MOV Rn, A	1	1	1	1	1	n_2	n_1	n_0	F8–FF	1	1	(Rn) = (A)
	MOV Rn, direct	1 a_7	0 a_6	1 a_5	0 a_4	1 a_3	n_2 a_2	n_1 a_1	n_0 a_0	A8–AF Byte 2	2	2	(Rn) = (direct)
	MOV Rn, #data	0 d_7	1 d_6	1 d_5	1 d_4	1 d_3	n_2 d_2	n_1 d_1	n_0 d_0	78–7F Byte 2	2	1	(Rn) = #data
	MOV direct, A	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	0 a_1	1 a_0	F5 Byte 2	2	1	(direct) = (A)
	MOV direct, Rn	1 a_7	0 a_6	0 a_5	0 a_4	1 a_3	n_2 a_2	n_1 a_1	n_0 a_0	88–8F Byte 2	2	2	(direct) = (Rn)
	MOV direct1, direct2	1 a_7 a_7	0 a_6 a_6	0 a_5 a_5	0 a_4 a_4	0 a_3 a_3	1 a_2 a_2	0 a_1 a_1	1 a_0 a_0	85 Byte 2 Byte 3	3	2	(direct1) = (direct2) (source) (destination)
	MOV direct, @Ri	1 a_7	0 a_6	0 a_5	0 a4	0 a_3	1 a_2	1 a_1	i a_0	86–87 Byte 2	2	2	(direct) = ((Ri))

	MNEMONIC	INSTRUCTION CODE								HEX	BYTE	CYCLE	EXPLANATION
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				
DATA TRANSFER	MOV direct, #data	0 a_7 d_7	1 a_6 d_6	1 a_5 d_5	1 a_4 d_4	0 a_3 d_3	1 a_2 d_2	0 a_1 d_1	1 a_0 d_0	75 Byte 2 Byte 3	3	2	(direct) = #data
	MOV @Ri, A	1	1	1	1	0	1	1	i	F6–F7	1	1	((Ri)) = A
	MOV @Ri, direct	1 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	i a_0	A6–A7 Byte 2	2	2	((Ri)) = (direct)
	MOV @Ri, #data	0 d_7	1 d_6	1 d_5	1 d_4	0 d_3	1 d_2	1 d1	i d_0	76–77 Byte 2	2	1	((Ri)) = #data
	MOV DPTR, #data16	1 d_7 d_7	0 d_6 d_6	0 d_5 d_5	1 d4 d_4	0 d_3 d_3	0 d_2 d_2	0 d_1 d_1	0 d_0 d_0	90 Byte 2 Byte 3	3	2	(DPTR) = $\#data_{15–0}$ (DPH) = $\#data_{15–8}$ (DPL) = $\#data_{7–0}$
	MOVC A, @A + DPTR	1	0	0	1	0	0	1	1	93	1	2	(A)=((A) + (DPTR))
	MOVC A, @A + PC	1	0	0	0	0	0	1	1	83	1	2	(A) = ((A) + (PC))
	MOVX A, @Ri	1	1	1	0	0	0	1	i	E2–E3	1	2	(A) = ((Ri))
	MOVX @DPTR	1	1	1	0	0	0	0	0	E0	1	2	(A) = ((DPTR))
	MOVX @Ri, A	1	1	1	1	0	0	1	i	F2–F3	1	2	((Ri)) = (A)
	MOVX @DPTR,A	1	1	1	1	0	0	0	0	F0	1	2	((DPTR)) = (A)
	PUSH direct	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	0 a_2	0 a_1	0 a_0	C0 Byte 2	2	2	(SP) = (SP) + 1 ((SP)) = (direct)
	POP direct	1 a_7	1 a_6	0 a_5	1 a_4	0 a_3	0 a_2	0 a_1	0 a_0	D0 Byte 2	2	2	(direct) = ((SP)) (SP) = (SP) – 1
	XCH A, Rn	1	1	0	0	1	n_2	n_1	n_0	C8–CF	1	1	(A) = (Rn)
	XCH A, direct	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	0 a_1	1 a_0	C5 Byte 2	2	1	(A) = (direct)
	XCH A, @Ri	1	1	0	0	0	1	1	i	C6–C7	1	1	(A) = ((Ri))
	XCHD A, @Ri	1	1	0	1	0	1	1	i	D6–D7	1	1	$(A_{3-0}) = ((Ri_{3–0}))$

	MNEMONIC	INSTRUCTION CODE								HEX	BYTE	CYCLE	EXPLANATION
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				
BOOLEAN VARIABLE MANIPULATION	CLR C	1	1	0	0	0	0	1	1	C3	1	1	(C) = 0
	CLR bit	1 b_7	1 b_6	0 b_5	0 b_4	0 b_3	0 b_2	1 b_1	0 b_0	C2 Byte 2	2	1	(bit) = 0
	SETB C	1	1	0	1	0	0	1	1	D3	1	1	(C) = 1
	SETB bit	1 b_7	1 b_6	0 b_5	1 b_4	0 b_3	0 b_2	1 b_1	0 b_0	D2 Byte 2	2	1	(bit) = 1
	CPL C	1	0	1	1	0	0	1	1	B3	1	1	(C) = ($\overline{C}$)
	CPL bit	1 b_7	0 b_6	1 b_5	1 b_4	0 b_3	0 b_2	1 b_1	0 b_0	B2 Byte 2	2	1	(bit) = ($\overline{bit}$)
	ANL C, bit	1 b_7	0 b_6	0 b_5	0 b_4	0 b_3	0 b_2	1 b_1	0 b_0	82 Byte 2	2	2	(C) = (C) AND (bit)
	ANL C, $\overline{bit}$	1 b_7	0 b_6	1 b_5	1 b_4	0 b_3	0 b_2	0 b_1	0 b_0	B0 Byte 2	2	2	(C) = (C) AND ($\overline{bit}$)
	ORL C, bit	0 b_7	1 b6	1 b_5	1 b_4	0 b_3	0 b_2	1 b_1	0 b_0	72 Byte 2	2	2	(C) = (C) OR (bit)
	ORL C, $\overline{bit}$	1 b_7	0 b_6	1 b_5	0 b_4	0 b_3	0 b_2	0 b_1	0 b_0	A0 Byte 2	2	2	(C) = (C) OR ($\overline{bit}$)
	MOV C, bit	1 b_7	0 b_6	1 b_5	0 b_4	0 b_3	0 b_2	1 b_1	0 b_0	A2 Byte 2	2	1	(C) = (bit)
	MOV bit, C	1 b_7	0 b_6	0 b_5	1 b_4	0 b_3	0 b_2	1 b_1	0 b_0	92 Byte 2	2	2	(bit) = (C)

	MNEMONIC	INSTRUCTION CODE								HEX	BYTE	CYCLE	EXPLANATION
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				
PROGRAM BRANCHING	ACALL addr 11	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	0 a_2	0 a_1	1 a_0	Byte 1 Byte 2	2	2	(PC) = (PC) + 2 (SP) = (SP) + 1 ((SP)) = ($PC_{7–0}$) (SP) = (SP) + 1 ((SP)) = ($PC_{15–8}$) (PC)=page address
	LCALL addr 16	0 a_{15} a_7	0 a_{14} a_6	0 a_{13} a_5	1 a_{12} a_4	0 a_{11} a_3	0 a_{10} a_2	1 a_9 a_1	0 a_8 a_0	12 Byte 2 Byte 3	3	2	(PC) = (PC) + 3 (SP) = (SP) + 1 ((SP)) = ($PC_{7–0}$) (SP) = (SP) + 1 ((SP)) = ($PC_{15–8}$) (PC) = $addr_{15–0}$
	RET	0	0	1	0	0	0	1	0	22	1	2	($PC_{15–8}$) = ((SP)) (SP) = (SP) – 1 ($PC_{7–0}$) = ((SP)) (SP) = (SP) – 1
	RETI	0	0	1	1	0	0	1	0	32	1	2	($PC_{15–8}$) = ((SP)) (SP) = (SP) – 1 (PC_{7-0}) = ((SP)) (SP) = (SP) – 1
	AJMP addr 11	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	0 a_2	0 a_1	1 a_0	Byte 1 Byte 2	2	2	(PC) = (PC) + 2 (PC_{10-0}) = page addr
	LJMP addr 16	0 a_{15} a_7	0 a_{14} a_6	0 a_{13} a_5	0 a_{12} a_4	0 a_{11} a_3	0 a_{10} a_2	1 a_9 a_1	0 a_8 a_0	02 Byte 2 Byte 3	3	2	(PC) = addr15-0
	SJMP rel	1 r_7	0 r_6	0 r_5	0 r_4	0 r_3	0 r_2	0 r_1	0 r_0	80 Byte 2	2	2	(PC) = (PC) + 2 (PC) = (PC) + rel
	JMP @A + DPTR	0	1	1	1	0	0	1	1	73	1	2	(PC) = (A) + (DPTR)
	JZ rel	0 r_7	1 r_6	1 r_5	0 r_4	0 r_3	0 r_2	0 r_1	0 r_0	60 Byte 2	2	2	(PC) = (PC) + 2 IF (A) = 0 THEN (PC) = (PC) + rel
	JNZ rel	0 r_7	1 r_6	1 r_5	1 r_4	0 r_3	0 r_2	0 r_1	0 r_0	70 Byte 2	2	2	(PC) = (PC) + 2 IF (A) $\neq$ 0 THEN (PC) = (PC) + rel
	JC rel	0 r_7	1 r_6	0 r_5	0 r_4	0 r_3	0 r_2	0 r_1	0 r_0	40 Byte 2	2	2	(PC) = (PC) + 2 IF (C) = 1 THEN (PC) = (PC) + rel
	JC rel	0 r_7	1 r_6	0 r_5	0 r_4	0 r_3	0 r_2	0 r_1	0 r_0	40 Byte 2	2	2	(PC) = (PC) + 2 IF (C) = 1 THEN (PC) = (PC) + rel
	JNC rel	0 r_7	1 r_6	0 r_5	1 r_4	0 r_3	0 r_2	0 r_1	0 r_0	50 Byte 2	2	2	(PC) = (PC) + 2 IF (C) $\neq$ 0 THEN (PC) = (PC) + rel
	JB bit, rel	0 b_7 r_7	0 b_6 r_6	1 b_5 r_5	0 b_4 r_4	0 b_3 r_3	0 b_2 r_2	0 b_1 r_1	0 b_0 r_0	20 Byte 2 Byte 3	3	2	(PC) = (PC) + 3 IF (bit) = 1 THEN (PC) = (PC) + rel

	MNEMONIC	INSTRUCTION CODE								HEX	BYTE	CYCLE	EXPLANATION
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				
PROGRAM BRANCHING	JNB bit, rel	0 b_7 r_7	0 b_6 r_6	1 b_5 r_5	1 b_4 r_4	0 b_3 r_3	0 b_2 r_2	0 b_1 r_1	0 b_0 r_0	30 Byte 2 Byte 3	3	2	(PC) = (PC) + 3 IF (bit) = 0 THEN (PC) = (PC) + rel
	JBC bit, direct rel	0 b_7 r_7	0 b_6 r_6	0 b_5 r_5	1 b_4 r_4	0 b_3 r_3	0 b_2 r_2	0 b_1 r_1	0 b_0 r_0	10 Byte 2 Byte 3	3	2	(PC) = (PC) + 3 IF (bit) = 1 THEN (bit) = 0 (PC) = (PC) + rel
	CJNE A, direct rel	1 a7 r_7	0 a6 r_6	1 a5 r_5	1 ad r_4	0 a3 r_3	1 a2 r_2	0 a1 r_1	1 a0 r_0	B5 Byte 2 Byte 3	3	2	(PC) = (PC) + 3 IF (direct) < (A) THEN (PC) = (PC) + rel and (C) = 0 OR IF (direct) > (A) THEN (PC) = (PC) + rel and (C) = 1
	CJNE A, #data rel	1 d7 r_7	0 d6 r_6	1 d5 r_5	1 d4 r_4	0 d3 r_3	1 d2 r_2	0 d1 r_1	0 d0 r_0	B4 Byte 2 Byte 3	3	2	(PC) = (PC) + 3 IF #data < (A) THEN (PC) = (PC) + rel and (C) = 0 OR IF #data > (A) THEN (PC) = (PC) + rel and (C) = 1
	CJNE Rn, #data rel	1 d7 r_7	0 d6 r_6	1 d5 r_5	1 d4 r_4	1 d3 r_3	n_2 d2 r_2	n_1 d1 r_1	n_0 d0 r_0	B8-BF Byte 2 Byte 3	3	2	(PC) = (PC) + 3 IF #data < (Rn) THEN (PC) = (PC) + rel and (C) = 0 OR IF #data > (Rn) THEN (PC) = (PC) + rel and (C) = 1
	CJNE @Ri, #data rel	1 d7 r_7	0 d6 r_6	1 d5 r_5	1 d4 r_4	0 d3 r_3	1 d2 r_2	1 d1 r_1	i d0 r_0	B6-B7 Byte 2 Byte 3	3	2	(PC) = (PC) + 3 IF #data < ((Ri)) THEN (PC) = (PC) + rel and (C) = 0 OR IF #data > ((Ri)) THEN (PC) = (PC) + rel and (C) = 1
	DJNZ Rn, rel	1 r_7	1 r_6	0 r_5	1 r_4	1 r_3	n_2 r_2	n_1 r_1	n_0 r_0	D8-Df Byte 2	2	2	(PC) = (PC) + 2 (Rn) = (Rn) – 1 IF (Rn) 0 THEN (PC) = (PC) + rel
	DJNZ direct rel	1 a_7 r_7	1 a_6 r_6	0 a_5 r_5	1 a_4 r_4	0 a_3 r_3	1 a_2 r_2	0 a_1 r_1	1 a_0 r_0	D5 Byte 2 Byte 3	3	2	(PC) = (PC) + 3 (direct) = (direct)–1 IF (direct)≠0 THEN (PC) = (PC) + rel
	NOP	0	0	0	0	0	0	0	0	00	1	1	(PC) = (PC) + 1

SECURE MICROCONTROLLER DATA SHEETS

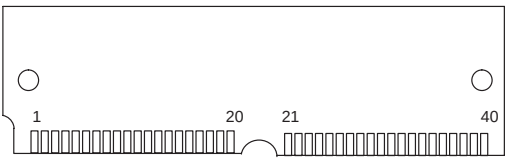
DALLAS SEMICONDUCTOR

DS2250(T)
Soft Microcontroller Module

FEATURES

- 8–bit 8051 compatible microcontroller adapts to task–at–hand:
  - 8K, 32K, or 64K bytes of nonvolatile RAM for program and/or data memory storage
  - Initial downloading of software in end system via on–chip serial port
  - Capable of modifying its own program and/or data memory in end use
- High–reliability operation:
  - Maintains all nonvolatile resources for 10 years in the absence of V_{CC}
  - Power–fail reset
  - Early warning power–fail interrupt
  - Watchdog timer
- Software Security Feature:
  - Executes encrypted software to prevent unauthorized disclosure
- On–chip, full–duplex serial I/O ports
- Two on–chip timer/event counters
- 32 parallel I/O lines
- Compatible with industry standard 8051 instruction set
- Permanently Powered real time clock

PIN ASSIGNMENT



40–PIN SIMM

DESCRIPTION

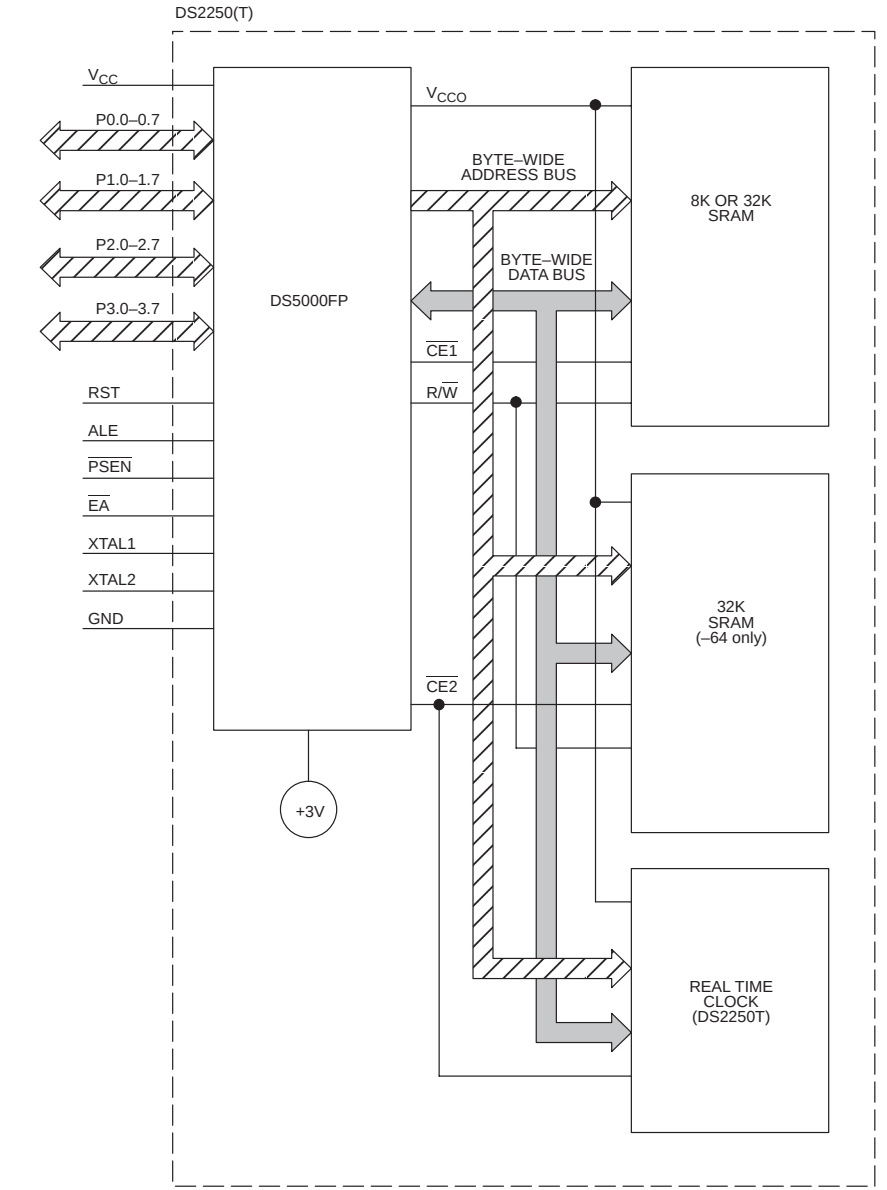
The DS2250(T) Soft Microcontroller Module is a fully 8051 compatible 8–bit CMOS microcontroller that offers “softness” in all aspects of its application. This is accomplished through the comprehensive use of nonvolatile technology to preserve all information in the absence of system V_{CC}. The internal program/data memory space is implemented using 8K, 32K, or 64K bytes of nonvolatile CMOS SRAM. Furthermore, internal data registers and key configuration registers are also nonvolatile. An optional real time clock gives permanently powered timekeeping. The clock keeps time to a hundredth of a second using an on–board crystal. All nonvolatile memory and resources are maintained for over 10 years at room temperature in the absence of power.

ORDERING INFORMATION

PART NUMBER	RAM SIZE	MAX CRYSTAL SPEED	TIMEKEEPING?
DS2250–8–16	8K bytes	16 MHz	No
DS2250–32–16	32K bytes	16 MHz	No
DS2250–64–16	64K bytes	16 MHz	No
DS2250T–8–16	8K bytes	16 MHz	Yes
DS2250T–32–16	32K bytes	16 MHz	Yes
DS2250T–64–16	64K bytes	16 MHz	Yes

Operating information is contained in the User's Guide section of the Secure Microcontroller Data Book. This data sheet provides ordering information, pinout, and electrical specifications.

DS2250(T) BLOCK DIAGRAM Figure 1



PIN DESCRIPTION

PIN	DESCRIPTION
1, 3, 5, 7, 9, 11, 13, 15	**P1.0 – P1.7.** General purpose I/O Port 1
17	**RST** – Active high reset input. A logic 1 applied to this pin will activate a reset state. This pin is pulled down internally so this pin can be left unconnected if not used. An RC power–on reset circuit is not needed and is not recommended.
19	**P3.0 RXD.** General purpose I/O port pin 3.0. Also serves as the receive signal for the on board UART. This pin should not be connected directly to a PC COM port.
21	**P3.1 TXD.** General purpose I/O port pin 3.1. Also serves as the transmit signal for the on board UART. This pin should not be connected directly to a PC COM port.
23	**P3.2 $\overline{\text{INT0}}$.** General purpose I/O port pin 3.2. Also serves as the active low External Interrupt 0.
25	**P3.3 $\overline{\text{INT1}}$.** General purpose I/O port pin 3.3. Also serves as the active low External Interrupt 1.
27	**P3.4 T0.** General purpose I/O port pin 3.4. Also serves as the Timer 0 input.
29	**P3.5 T1.** General purpose I/O port pin 3.5. Also serves as the Timer 1 input.
31	**P3.6 $\overline{\text{WR}}$.** General purpose I/O port pin. Also serves as the write strobe for Expanded bus operation.
33	**P3.7 $\overline{\text{RD}}$.** General purpose I/O port pin. Also serves as the read strobe for Expanded bus operation.
35, 37	**XTAL2, XTAL1.** Used to connect an external crystal to the internal oscillator. XTAL1 is the input to an inverting amplifier and XTAL2 is the output.
39	**GND** – Logic ground.
26, 28, 30, 32, 34, 36, 38, 40	**P2.7–P2.0.** General purpose I/O Port 2. Also serves as the MSB of the Expanded Address bus.
24	**$\overline{\text{PSEN}}$** – Program Store Enable. This active low signal is used to enable an external program memory when using the Expanded bus. It is normally an output and should be unconnected if not used. $\overline{\text{PSEN}}$ also is used to invoke the Bootstrap Loader. At this time, $\overline{\text{PSEN}}$ will be pulled down externally. This should only be done once the DS2250(T) is already in a reset state. The device that pulls down should be open drain since it must not interfere with $\overline{\text{PSEN}}$ under normal operation.
22	**ALE** – Address Latch Enable. Used to de–multiplex the multiplexed Expanded Address/Data bus on Port 0. This pin is normally connected to the clock input on a '373 type transparent latch. When using a parallel programmer, this pin also assumes the $\overline{\text{PROG}}$ function for programming pulses.
20	**$\overline{\text{EA}}$** – External Access. This pin forces the DS2250(T) to behave like an 8031. No internal memory (or clock) will be available when this pin is at a logic low. Since this pin is pulled down internally, it should be connected to +5V to use NV RAM. In an parallel programmer, this pin also serves as V_{PP} for super voltage pulses.

PIN	DESCRIPTION
4, 6, 8, 10, 12, 14, 16, 18	**P0.0–P0.7.** General purpose I/O Port 0. This port is open–drain and can not drive a logic 1. It requires external pull–ups. Port 0 is also the multiplexed Expanded Address/Data bus. When used in this mode, it does not require pull–ups.
2	**V_{CC} +** – 5 volts.

INSTRUCTION SET

The DS2250(T) executes an instruction set which is object code compatible with the industry standard 8051 microcontroller. As a result, software development packages which have been written for the 8051 are compatible with the DS2250(T), including cross–assemblers, high–level language compilers, and debugging tools. Note that the DS2250(T) is functionally identical to the DS5000(T) except for package and the 64K memory option.

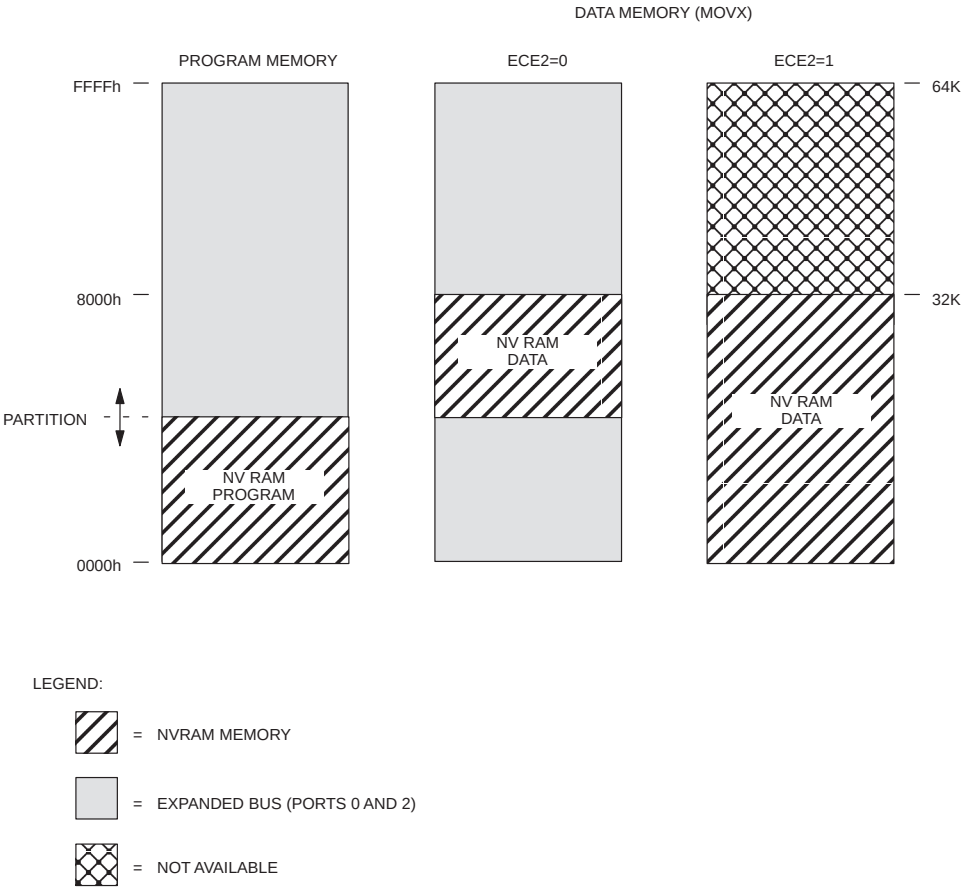
A complete description for the DS2250(T) instruction set is available in the User's Guide section of the Secure Microcontroller Data Book.

MEMORY ORGANIZATION

Figure 2 illustrates the address spaces which are accessed by the DS2250(T). As illustrated in the figure, separate address spaces exist for program and data memory. Since the basic addressing capability of the machine is 16 bits, a maximum of 64K bytes of program memory and 64K bytes of data memory can be accessed by the DS2250(T) CPU. The 8K or 32K byte RAM area inside of the DS2250(T) can be used to contain both program and data memory. A second 32K RAM is available for data only.

The Real Time Clock (RTC) in the DS2250(T) is reached in the memory map by setting a SFR bit. The MCON.2 bit (ECE2) is used to select an alternate data memory map. While ECE2=1, all MOVXs will be routed to this alternate memory map. The real time clock is a serial device that resides in this area. A full description of the RTC access and example software is given in the User's Guide section of the Secure Microcontroller Data Book.

DS2250(T) MEMORY MAP Figure 2



PROGRAM LOADING

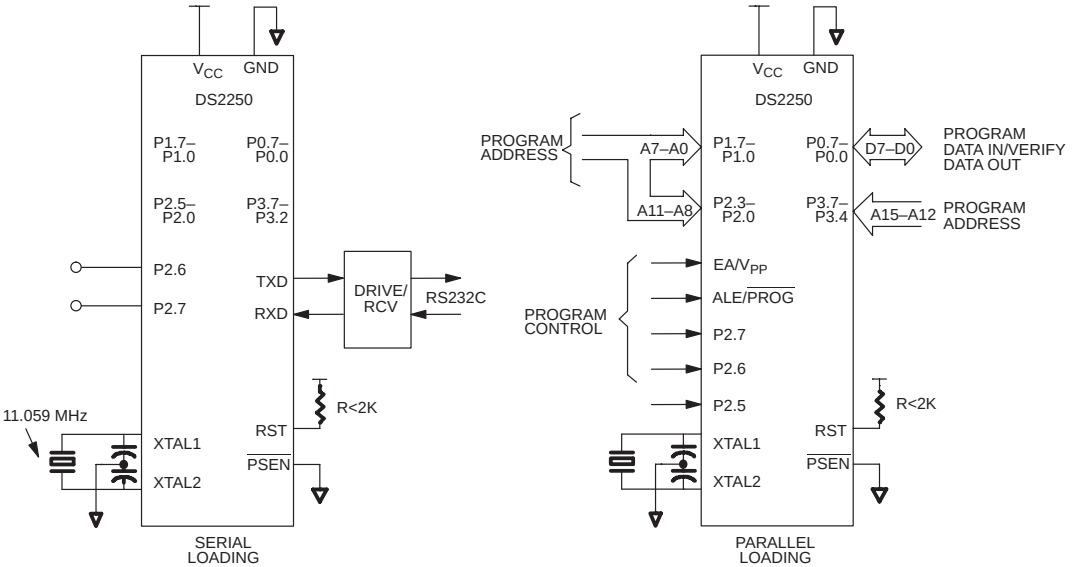
The Program Load Modes allow initialization of the NV RAM Program/Data Memory. This initialization may be performed in one of two ways:

1. Serial Program Loading which is capable of performing Bootstrap Loading of the DS2250(T). This feature allows the loading of the application program to be delayed until the DS2250(T) is installed in the end system.
2. Parallel Program Load cycles which perform the initial loading from parallel address/data information presented on the I/O port pins. This mode is timing–set compatible with the 87C51H microcontroller programming mode.

The DS2250(T) is placed in its Program Load configuration by simultaneously applying a logic 1 to the RST pin and forcing the $\overline{\text{PSEN}}$ line to a logic 0 level. Immediately following this action, the DS2250(T) will look for a parallel Program Load pulse, or a serial ASCII carriage return (0DH) character received at 9600, 2400, 1200, or 300 bps over the serial port.

The hardware configurations used to select these modes of operation are illustrated in Figure 3.

PROGRAM LOADING CONFIGURATIONS Figure 3



SERIAL BOOTSTRAP LOADER

The Serial Program Load Mode is the easiest, fastest, most reliable, and most complete method of initially loading application software into the DS2250(T) nonvolatile RAM. Communication can be performed over a standard asynchronous serial communications port. A typical application would use a simple RS232C serial interface to program the DS2250(T) as a final production procedure. The hardware configuration which is required for the Serial Program Load mode is illustrated in Figure 3. Port pins 2.7 and 2.6 must be either open or pulled high to avoid placing the device in a parallel load cycle. Although an 11.0592 MHz crystal is shown in Figure 3, a variety of crystal frequencies and loader baud rates are supported, shown in Table 2. The serial loader is designed to operate across a three–wire interface from a standard UART. The receive, transmit, and ground wires are all that are necessary to establish communication with the DS2250(T).

The Serial Bootstrap Loader implements an easy–to–use command line interface which allows an application program in an Intel hex representation to be loaded into and read back from the device. Intel hex is the typical format which existing 8051 cross–assemblers output.

The serial loader responds to single character commands which are summarized below:

COMMAND	FUNCTION
C	Return CRC–16 checksum of embedded RAM
D	Dump Intel Hex File
F	Fill embedded RAM block with constant
K	Load 40–bit Encryption Key
L	Load Intel Hex File
R	Read MCON register
T	Trace (Echo) incoming Intel Hex data
U	Clear Security Lock
V	Verify Embedded RAM with incoming Intel Hex
W	Write MCON register
Z	Set Security Lock
P	Put a value to a port
G	Get a value from a port

Table 1 summarizes the selection of the available Parallel Program Load cycles. The timing associated with these cycles is illustrated in the electrical specs.

PARALLEL PROGRAM LOAD CYCLES Table 1

MODE	RST	$\overline{\text{PSEN}}$	$\overline{\text{PROG}}$	$\overline{\text{EA}}$	P2.7	P2.6	P2.5
Program	1	0	0	V_{PP}	1	0	X
Security Set	1	0	0	V_{PP}	1	1	X
Verify	1	X	X	1	0	0	X
Prog Expanded	1	0	0	V_{PP}	0	1	0
Verify Expanded	1	0	1	1	0	1	0
Prog MCON or Key registers	1	0	0	V_{PP}	0	1	1
Verify MCON registers	1	0	1	1	0	1	1

The Parallel Program Cycle is used to load a byte of data into a register or memory location within the DS2250(T). The Verify Cycle is used to read this byte back for comparison with the originally loaded value to verify proper loading. The Security Set Cycle may be used to enable and the Software Security feature. One may also enter bytes for the MCON register or for the five encryption registers using the Program MCON cycle. When using this cycle, the absolute register address must be presented at Ports 1 and 2 as in the normal program cycle (Port 2 should be 00H). The MCON contents can likewise be verified using the Verify MCON cycle.

When the DS2250(T) first detects a Parallel Program Strobe pulse or a Security Set Strobe pulse while in the Program Load Mode following a Power–On Reset, the internal hardware of the device is initialized so that an existing 4K byte program can be programmed into a DS2250(T) with little or no modification. This initialization automatically sets the Range Address for 8K bytes and maps the lowest 4K byte bank of Embedded RAM as program memory. The next 4K bytes of Embedded RAM are mapped as Data Memory.

In order to program more than 4K bytes of program code, the Program/Verify Expanded cycles can be used. Up to 32K bytes of program code can be entered and verified. Note that the expanded 32K byte Program/Verify cycles take much longer than the normal 4K byte Program/Verify cycles.

A typical parallel loading session would follow this procedure. First, set the contents of the MCON register with the correct range and partition only if using expanded programming cycles. Next, the encryption registers can be loaded to enable encryption of the program/data memory (not required). Then, program the DS2250(T) using either normal or expanded program cycles and check the memory contents using Verify cycles. The last operation would be to turn on the security lock feature by either a Security Set cycle or by explicitly writing to the MCON register and setting MCON.0 to a 1.

SERIAL LOADER BAUD RATES FOR DIFFERENT CRYSTAL FREQUENCIES Table 2

CRYSTAL FREQ (MHz)	BAUD RATE					
	300	1200	2400	9600	19200	57600
14.7456		Y	Y	Y	Y	
11.0592	Y	Y	Y	Y	Y	Y
9.21600	Y	Y	Y	Y		
7.37280	Y	Y	Y	Y		
5.52960	Y	Y	Y	Y		
1.84320	Y	Y	Y	Y		

ADDITIONAL INFORMATION

A complete description for all operational aspects of the DS2250(T) is provided in the User's Guide section of the Secure Microcontroller Data Book.

DEVELOPMENT SUPPORT

Dallas Semiconductor offers a kit package for developing and testing user code. The DS5000TK Evaluation Kit allows the user to download Intel hex formatted code directly to the DS2250(T) from a PC–XT/AT or compatible computer. The kit consists of a DS5000T–32–12, an interface pod, demo software, and an RS232 connector that attaches to the COM1 or COM2 serial port of a PC. The kit can be used with a DS2250(T). A mechanical adaptor, the DS9075–40V, allows a DS2250(T) to be used in the DS5000TK. See the Secure Microcontroller User's Guide for further details.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC CHARACTERISTICS

(t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

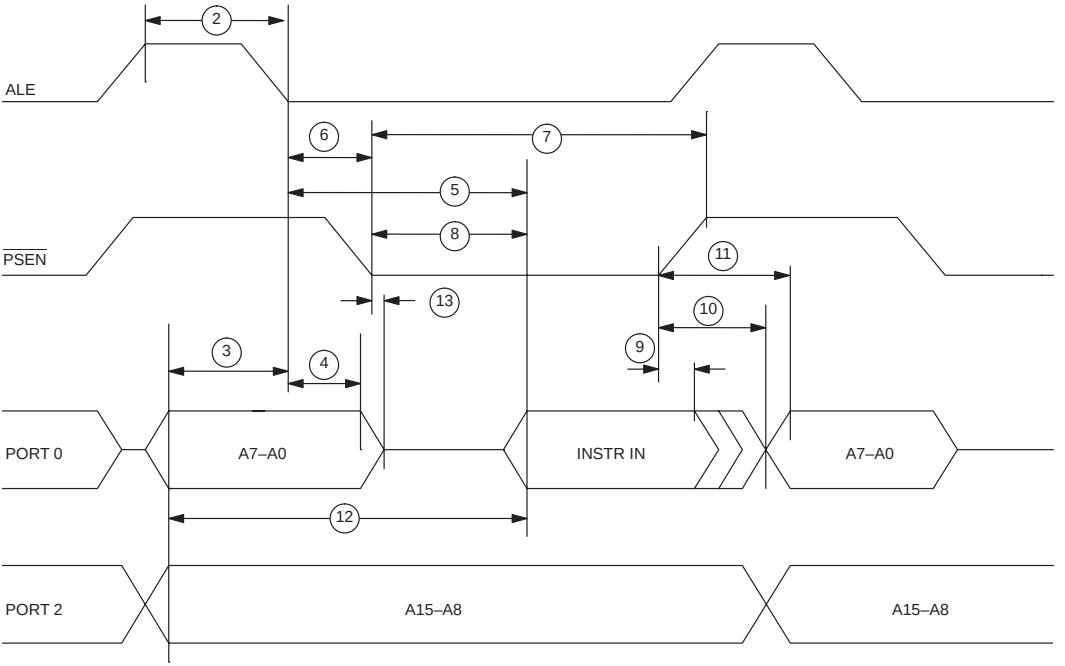
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Low Voltage	V_{IL}	–0.3		+0.8	V	1
Input High Voltage	V_{IH1}	2.0		V_{CC} +0.3	V	1
Input High Voltage RST, XTAL1	V_{IH2}	3.5		V_{CC} +0.3	V	1
Output Low Voltage @ I_{OL}=1.6 mA (Ports 1, 2, 3)	V_{OL1}		0.15	0.45	V	
Output Low Voltage @ I_{OL}=3.2 mA (Ports 0, ALE, $\overline{PSEN}$)	V_{OL2}		0.15	0.45	V	1
Output High Voltage @ I_{OH}=–80 µA (Ports 1, 2, 3)	V_{OH1}	2.4	4.8		V	1
Output High Voltage @I_{OH}=–400 µA (Ports 0, ALE, $\overline{PSEN}$)	V_{OH2}	2.4	4.8		V	1
Input Low Current V_{IN} = 0.45V (Ports 1, 2, 3)	I_{IL}			–50	µA	
Transition Current; 1 to 0 V_{IN} = 2.0V (Ports 1, 2, 3)	I_{TL}			–500	µA	
Input Leakage Current 0.45 < V_{IN} < V_{CC} (Port 0)	I_L			±10	µA	
RST, $\overline{EA}$ Pulldown Resistor	R_{RE}	40		125	KΩ	
Stop Mode Current	I_{SM}			80	µA	4
Power Fail Warning Voltage	V_{PFW}	4.15	4.6	4.75	V	1
Minimum Operating Voltage	V_{CCmin}	4.05	4.5	4.65	V	1
Programming Supply Voltage (Parallel Program Mode)	V_{PP}	12.5		13	V	1
Program Supply Current	I_{PP}		15	20	mA	
Operating Current DS2250–8K DS2250–32K @ 12 MHz DS2250(T)–64–16 @ 16 MHz	I_{CC}			43 48 54	mA	2
Idle Mode Current @ 8 MHz	I_{CC}			6.2	mA	3

AC CHARACTERISTICS
EXPANDED BUS MODE TIMING SPECIFICATIONS

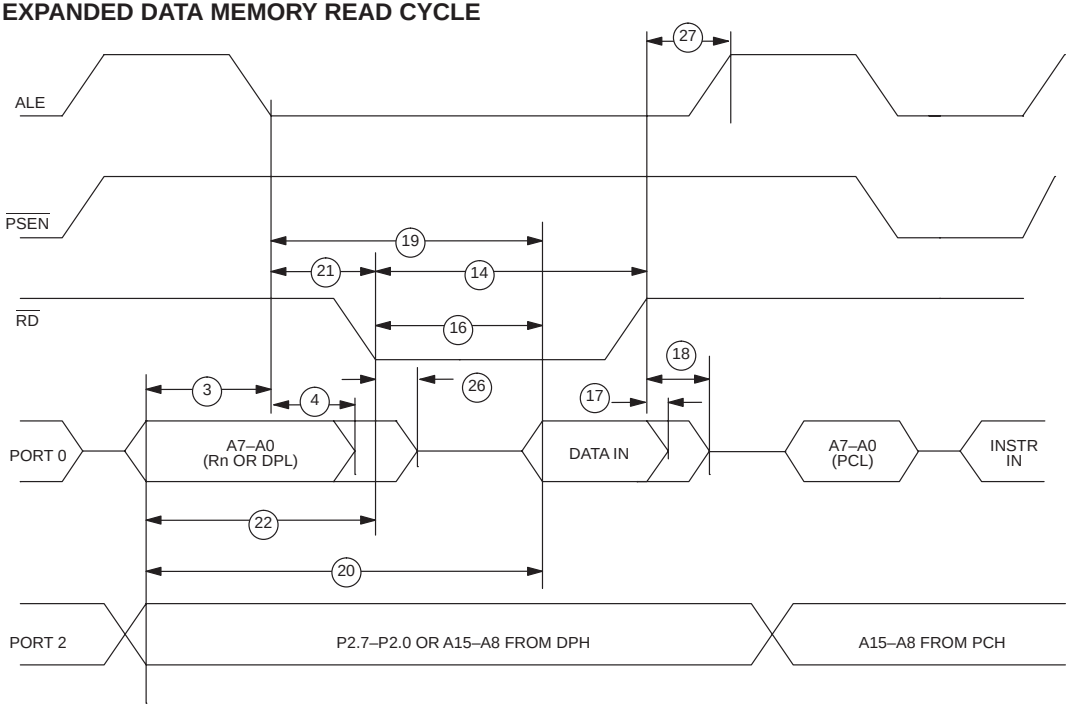
(t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
1	Oscillator Frequency	$1/t_{CLK}$	1.0	16 (–16)	MHz
2	ALE Pulse Width	t_{ALPW}	$2t_{CLK}$ –40		ns
3	Address Valid to ALE Low	t_{AVALL}	t_{CLK} –40		ns
4	Address Hold After ALE Low	t_{AVAAV}	t_{CLK} –35		ns
5	ALE Low to Valid Instr. In @12 MHz @16 MHz	t_{ALLVI}		$4t_{CLK}$ –150 $4t_{CLK}$ –90	ns
6	ALE Low to $\overline{PSEN}$ Low	t_{ALLPSL}	t_{CLK} –25		ns
7	$\overline{PSEN}$ Pulse Width	t_{PSPW}	$3t_{CLK}$ –35		ns
8	$\overline{PSEN}$ Low to Valid Instr. In @12 MHz @16 MHz	t_{PSLVI}		$3t_{CLK}$ –150 $3t_{CLK}$ –90	ns ns
9	Input Instr. Hold after $\overline{PSEN}$ Going High	t_{PSIV}	0		ns
10	Input Instr. Float after $\overline{PSEN}$ Going High	t_{PSIX}		t_{CLK} –20	ns
11	Address Hold after $\overline{PSEN}$ Going High	t_{PSAV}	t_{CLK} –8		ns
12	Address Valid to Valid Instr. In @12 MHz @16 MHz	t_{AVVI}		$5t_{CLK}$ –150 $5t_{CLK}$ –90	ns ns
13	$\overline{PSEN}$ Low to Address Float	t_{PSLAZ}	0		ns
14	$\overline{RD}$ Pulse Width	t_{RDPW}	$6t_{CLK}$ –100		ns
15	$\overline{WR}$ Pulse Width	t_{WRPW}	$6t_{CLK}$ –100		ns
16	$\overline{RD}$ Low to Valid Data In @12 MHz @16 MHz	t_{RDLDV}		$5t_{CLK}$ –165 $5t_{CLK}$ –105	ns ns
17	Data Hold after $\overline{RD}$ High	t_{RDHDV}	0		ns
18	Data Float after $\overline{RD}$ High	t_{RDHDZ}		$2t_{CLK}$ –70	ns
19	ALE Low to Valid Data In @12 MHz @16 MHz	t_{ALLVD}		8_{CLK} –150 $8t_{CLK}$ –90	ns ns
20	Valid Addr. to Valid Data In @12 MHz @16 MHz	t_{AVDV}		$9t_{CLK}$ –165 $9t_{CLK}$ –105	ns ns
21	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{ALLRDL}	$3t_{CLK}$ –50	$3t_{CLK}$ +50	ns
22	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVRDL}	$4t_{CLK}$ –130		ns
23	Data Valid to $\overline{WR}$ Going Low	t_{DVWRL}	t_{CLK} –60		ns
24	Data Valid to $\overline{WR}$ High @12 MHz @16 MHz	t_{DVWRH}	$7t_{CLK}$ –150 $7t_{CLK}$ –90		ns ns
25	Data Valid after $\overline{WR}$ High	t_{WRHDV}	t_{CLK} –50		ns
26	$\overline{RD}$ Low to Address Float	t_{RDLAZ}		0	ns
27	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{RDHALH}	t_{CLK} –40	t_{CLK} +50	ns

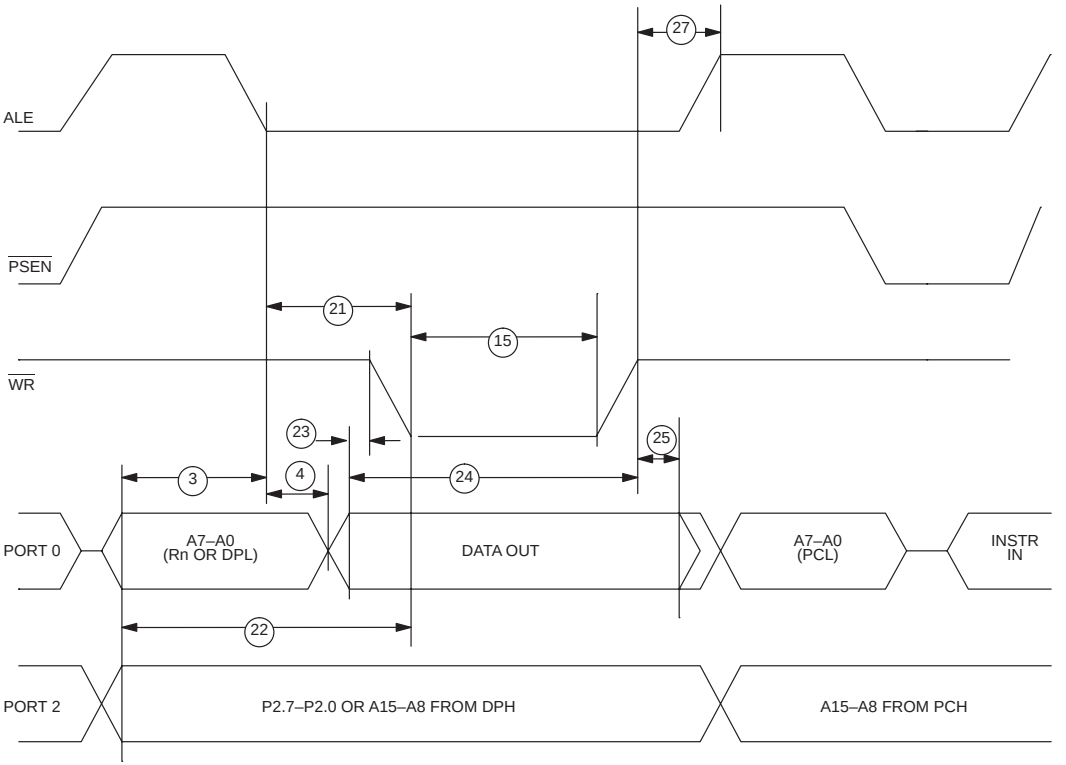
EXPANDED PROGRAM MEMORY READ CYCLE



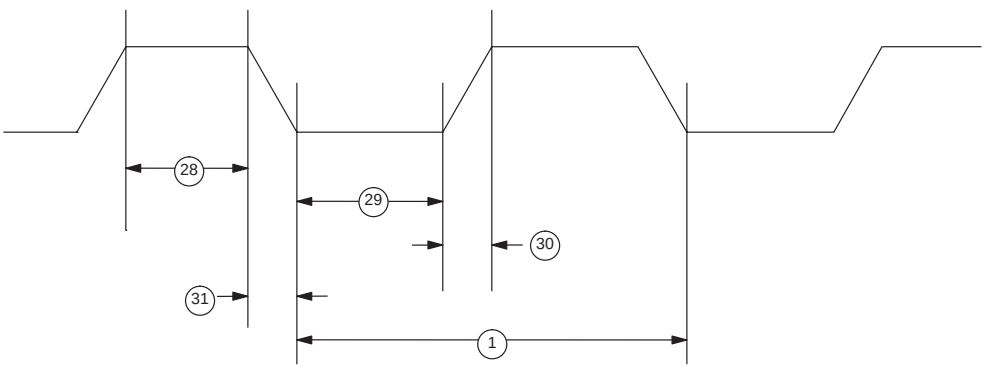
EXPANDED DATA MEMORY READ CYCLE



EXPANDED DATA MEMORY WRITE CYCLE



EXTERNAL CLOCK TIMING



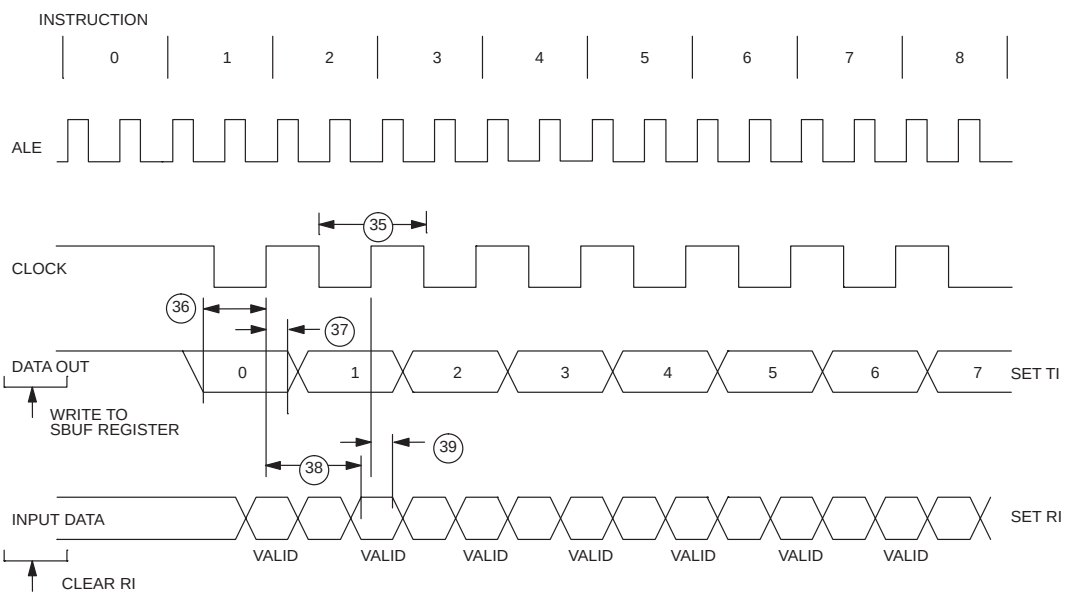
AC CHARACTERISTICS (cont'd)
EXTERNAL CLOCK DRIVE (t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

#	PARAMETER		SYMBOL	MIN	MAX	UNITS
28	External Clock High Time	@12 MHz @16 MHz	t_{CLKHPW}	20 15		ns ns
29	External Clock Low Time	@12 MHz @16 MHz	t_{CLKLPW}	20 15		ns ns
30	External Clock Rise Time	@12 MHz @16 MHz	t_{CLKR}		20 15	ns ns
31	External Clock Fall Time	@12 MHz @16 MHz	t_{CLKF}		20 15	ns ns

AC CHARACTERISTICS (cont'd)
SERIAL PORT TIMING – MODE 0 (t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
35	Serial Port Cycle Time	t_{SPCLK}	$12t_{CLK}$		µs
36	Output Data Setup to Rising Clock Edge	t_{DOCH}	$10t_{CLK}$ –133		ns
37	Output Data Hold after Rising Clock Edge	t_{CHDO}	$2t_{CLK}$ –117		ns
38	Clock Rising Edge to Input Data Valid	t_{CHDV}		$10t_{CLK}$ –133	ns
39	Input Data Hold after Rising Clock Edge	t_{CHDIV}	0		ns

SERIAL PORT TIMING – MODE 0

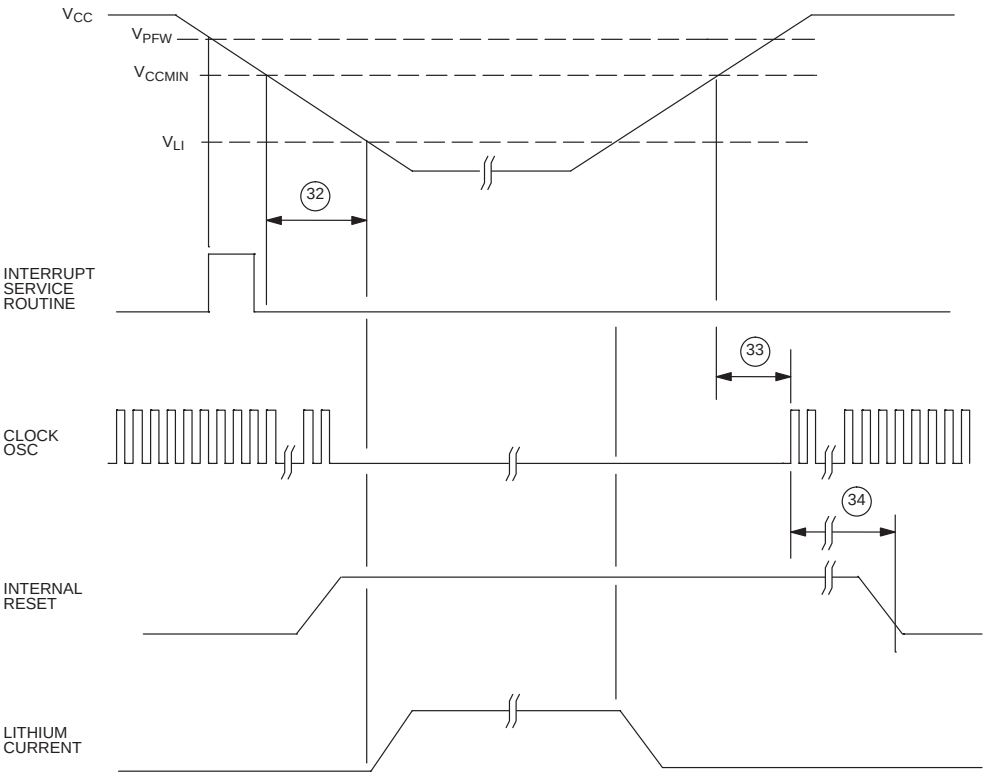


AC CHARACTERISTICS (cont'd)
POWER CYCLING TIMING

(t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
32	Slew Rate from V_{CCmin} to 3.3V	t_F	40		µs
33	Crystal Start–up Time	t_{CSU}		(note 5)	
34	Power–On Reset Delay	t_{POR}		21504	t_{CLK}

POWER CYCLE TIMING

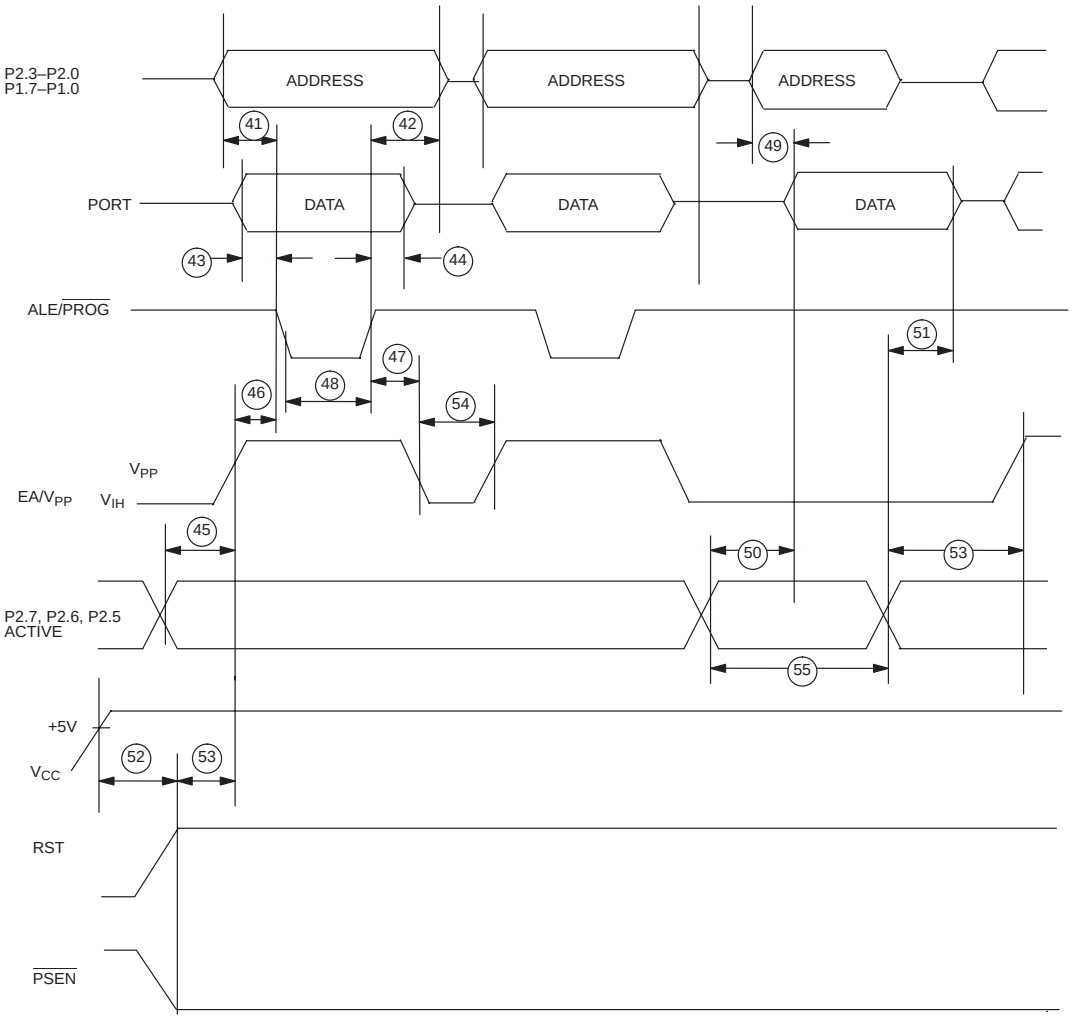


AC CHARACTERISTICS (cont'd)
PARALLEL PROGRAM LOAD TIMING (t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
40	Oscillator Frequency	$1/t_{CLK}$	1.0	12.0	MHz
41	Address Setup to $\overline{PROG}$ Low	t_{AVPRL}	0		
42	Address Hold after $\overline{PROG}$ High	t_{PRHAV}	0		
43	Data Setup to $\overline{PROG}$ Low	t_{DVPRL}	0		
44	Data Hold after $\overline{PROG}$ High	t_{PRHDV}	0		
45	P2.7, 2.6, 2.5 Setup to V_{PP}	t_{P27HVP}	0		
46	V_{PP} Setup to $\overline{PROG}$ Low	t_{VPHPRL}	0		
47	V_{PP} Hold after $\overline{PROG}$ Low	t_{PRHVPL}	0		
48	$\overline{PROG}$ Width Low	t_{PRW}	2400		t_{CLK}
49	Data Output from Address Valid	t_{AVDV}		48 1800*	t_{CLK}
50	Data Output from P2.7 Low	t_{DVP27L}		48 1800*	t_{CLK}
51	Data Float after P2.7 High	t_{P27HDZ}	0	48 1800*	t_{CLK}
52	Delay to Reset/$\overline{PSEN}$ Active after Power On	t_{PORPV}	21504		t_{CLK}
53	Reset/$\overline{PSEN}$ Active (or Verify Inactive) to V_{PP} High	t_{RAVPH}	1200		t_{CLK}
54	V_{PP} Inactive (Between Program Cycles)	t_{VPPPC}	1200		t_{CLK}
55	Verify Active Time	t_{VFT}	48 2400*		t_{CLK}

* Second set of numbers refers to expanded memory programming up to 32K bytes.

PARALLEL PROGRAM LOAD TIMING

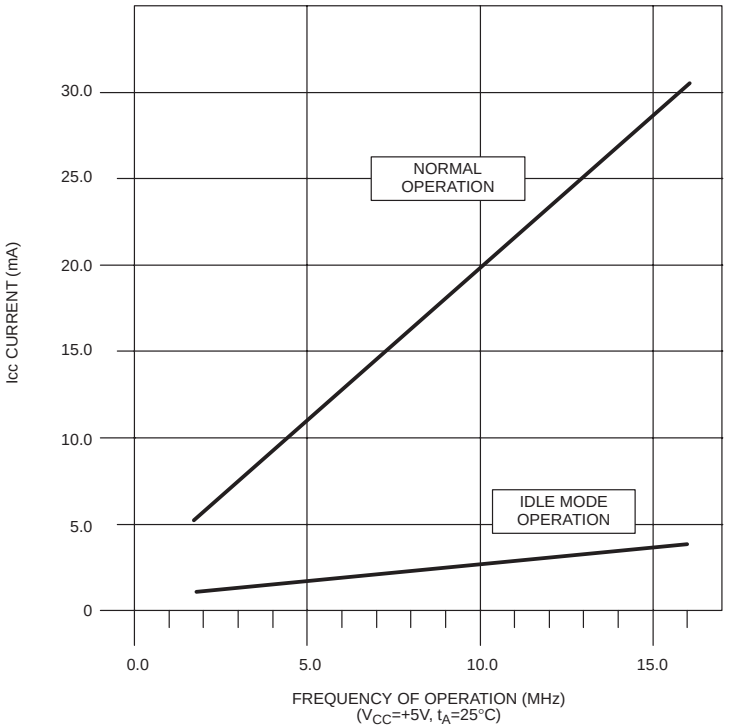


CAPACITANCE

(test frequency = 1 MHz; t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Capacitance	C_O			10	pF	
Input Capacitance	C_I			10	pF	

DS2250(T) TYPICAL I_{CC} VS. FREQUENCY



Normal operation is measured using:

1) External crystals on XTAL1 and 2
2) All port pins disconnected
3) RST=0 volts and EA=V_{CC}
4) Part performing endless loop writing to internal memory

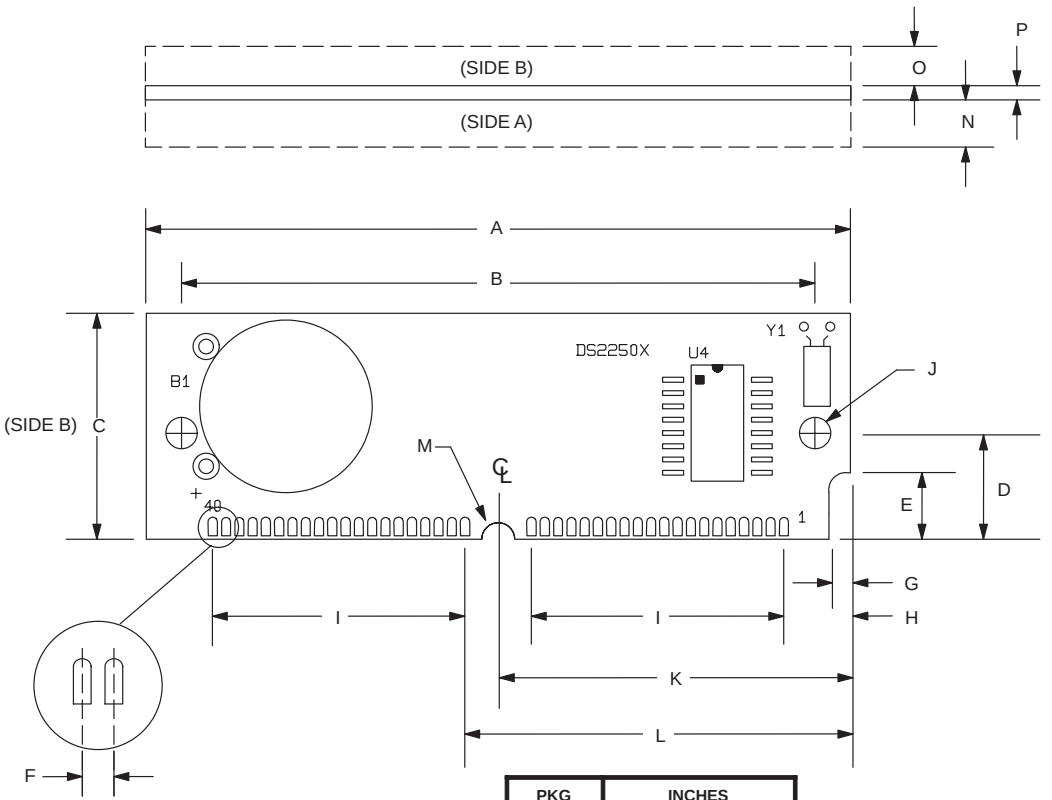
Idle mode operation is measured using:

1) External clock source at XTAL1; XTAL2 floating
2) All port pins disconnected
3) RST=0 volts and EA=V_{CC}
4) Part set in IDLE mode by software

NOTES:

1. All voltages are referenced to ground.
2. Maximum operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF}=10 ns, V_{IL} = 0.5V; XTAL2 disconnected; $\overline{EA}$ = RST = PORT0 = V_{CC}.
3. Idle mode I_{CC} is measured with all output pins disconnected; XTAL1 driven at 8 MHz with t_{CLKR}, t_{CLKF} = 10 ns, V_{IL} = 0.5V; XTAL2 disconnected; $\overline{EA}$ = PORT0 = V_{CC}, RST = V_{SS}.
4. Stop mode I_{CC} is measured with all output pins disconnected; $\overline{EA}$ = PORT0 = V_{CC}; XTAL2 not connected; RST = V_{SS}.
5. Crystal start–up time is the time required to get the mass of the crystal into vibrational motion from the time that power is first applied to the circuit until the first clock pulse is produced by the on–chip oscillator. The user should check with the crystal vendor for the worst case spec on this time.

PACKAGE DRAWING



PKG	INCHES	
DIM	MIN	MAX
A	2.645	2.655
B	2.379	2.389
C	0.845	0.855
D	0.395	0.405
E	0.245	0.255
F	0.050 BSC	
G	0.075	0.085
H	0.245	0.255
I	0.950 BSC	
J	0.120	0.130
K	1.320	1.330
L	1.445	1.455
M	0.057	0.067
N	–	0.160
O	–	0.195
P	0.047	0.054

DATA SHEET REVISION SUMMARY

The following represent the key differences between 12/13/95 and 08/16/96 version of the DS2250(T) data sheet. Please review this summary carefully.

1. Correct Figure 3 to show RST active high.
2. Add minimum value to PCB thickness.

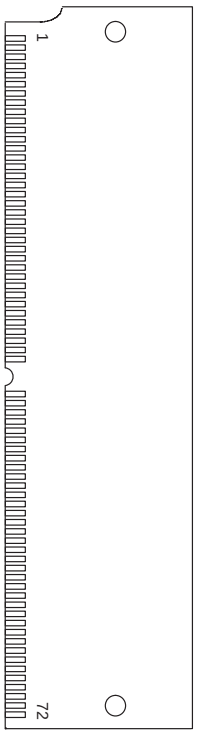
DALLAS SEMICONDUCTOR

DS2251T
128K Soft Microcontroller Module

FEATURES

- 8051 compatible microcontroller adapts to its task
  - 32K, 64K, or 128K bytes of nonvolatile SRAM for program and/or data storage
  - In–system programming via on–chip serial port
  - Capable of modifying its own program or data memory in the end system
  - Provides separate Byte–wide bus for peripherals
  - Performs CRC–16 check of NV RAM memory
- High–reliability Operation
  - Maintains all nonvolatile resources for over 10 years in the absence of power
  - Power–fail reset
  - Early Warning Power–fail Interrupt
  - Watchdog Timer
  - Lithium backed memory remembers system state
  - Precision reference for power monitor
- Fully 8051 Compatible
  - 128 bytes scratchpad RAM
  - Two timer/counters
  - On–chip serial port
  - 32 parallel I/O port pins
- Permanently powered real time clock

PACKAGE OUTLINE



72–PIN SIMM

DESCRIPTION

The DS2251T is an 8051 compatible microcontroller module based on nonvolatile RAM technology. It is designed for systems that need large quantities of nonvolatile memory. Like other members of the Secure Microcontroller family, it provides full compatibility with the 8051 instruction set, timers, serial port, and parallel I/O ports. By using NV RAM instead of ROM, the user can program, then reprogram the microcontroller while in–system. The application software can even change its own operation. This allows frequent software upgrades, adaptive programs, customized systems, etc. In addition, by using NV RAM, the DS2251T is ideal for data logging applications. The powerful real time clock includes interrupts for time stamp and date. It keeps time to one hundredth of second using its on–board 32 KHz crystal.

The DS2251T provides the benefits of NV RAM without using I/O resources. Between 32K bytes and 128K bytes of on–board NV RAM are available. A non–multiplexed Byte–wide address and data bus is used for memory access. This bus, which is available at the connector, can perform all memory access and also provides decoded chip enables for off–board memory

mapped peripherals. This leaves the 32 I/O port pins free for application use.

The DS2251T provides high–reliability operation in portable systems or systems with unreliable power. These features include the ability to save the operating state, Power–fail Reset, Power–fail Interrupt, and Watchdog Timer. All nonvolatile memory and resources are maintained for over 10 years at room temperature in the absence of power.

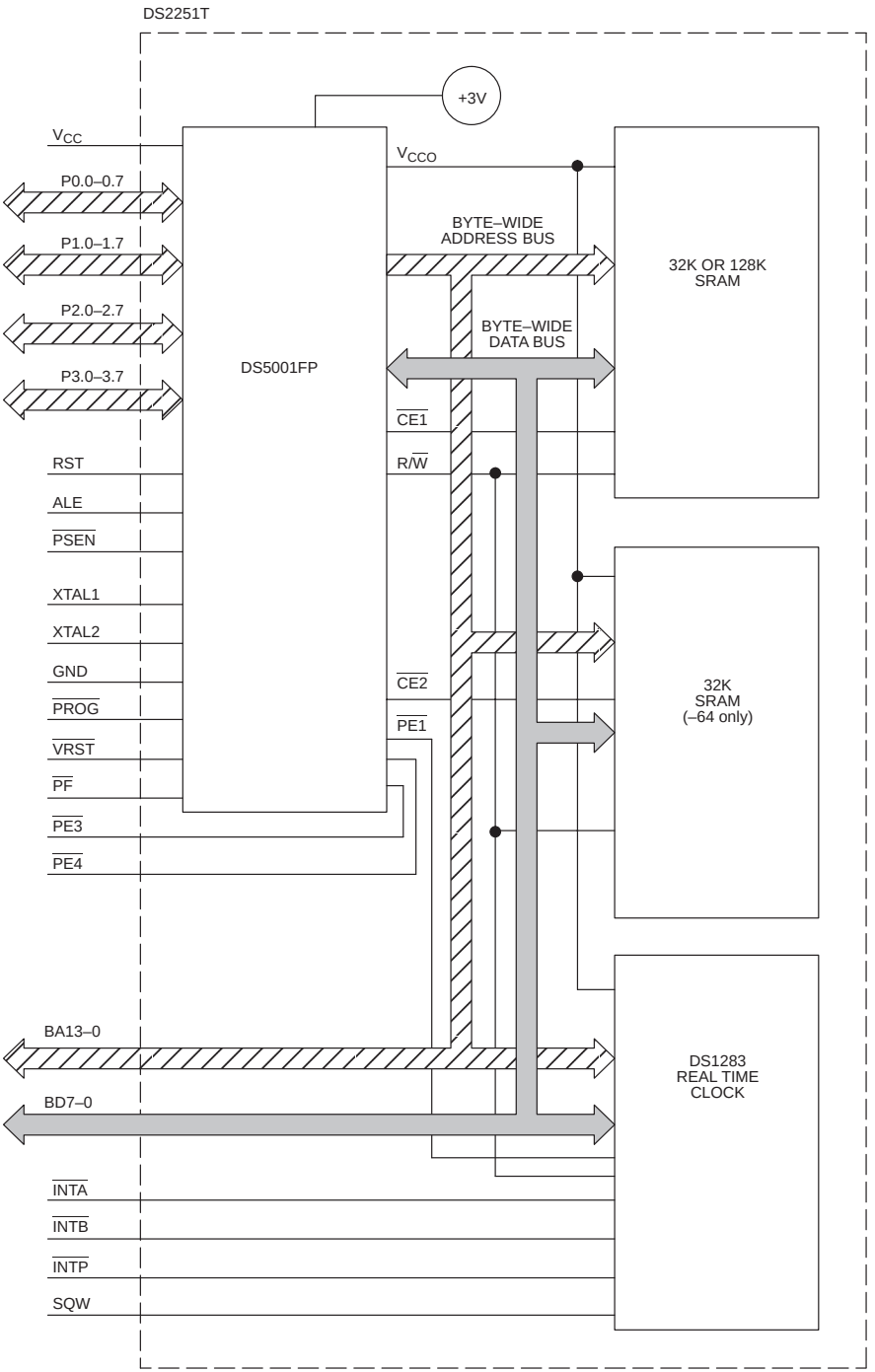
A user loads programs into the DS2251T via its on–chip Serial Bootstrap Loader. This function supervises the loading of software into NV RAM, validates it, then becomes transparent to the user. Software is stored in on–board CMOS SRAM. Using its internal Partitioning, the DS2251T can divide a common RAM into user selectable program and data segments. This Partition can be selected at program loading time, but can be modified anytime later. The microprocessor will decode memory access to the SRAM, access memory via its Byte–wide bus and write–protect the memory portion designated as program (ROM).

ORDERING INFORMATION

PART NUMBER	RAM SIZE	MAX CRYSTAL SPEED	TIMEKEEPING?
DS2251T–32–16	32K bytes	16 MHz	Yes
DS2251T–64–16	64K bytes	16 MHz	Yes
DS2251T–128–16	128K bytes	16 MHz	Yes

Operating information is contained in the User's Guide section of the Secure Microcontroller Data Book. This data sheet provides ordering information, pinout, and electrical specifications.

DS2251T BLOCK DIAGRAM Figure 1



PIN ASSIGNMENT

1	P1.0	19	XTAL2	37	P0.2	55	$\overline{\text{INTB}}$
2	P1.1	20	GND	38	P0.1	56	BD0
3	P1.2	21	P2.0	39	P0.0	57	BD1
4	P1.3	22	P2.1	40	V_{CC}	58	BD2
5	P1.4	23	P2.2	41	BA0	59	BD3
6	P1.5	24	P2.3	42	BA1	60	BD4
7	P1.6	25	P2.4	43	BA2	61	BD5
8	P1.7	26	P2.5	44	BA3	62	BD6
9	RST	27	P2.6	45	BA4	63	BD7
10	P3.0 RXD	28	P2.7	46	BA5	64	R/$\overline{\text{W}}$
11	P3.1 TXD	29	$\overline{\text{PSEN}}$	47	BA6	65	$\overline{\text{PF}}$
12	P3.2 $\overline{\text{INT0}}$	30	ALE	48	BA7	66	$\overline{\text{PE3}}$
13	P3.3 $\overline{\text{INT1}}$	31	$\overline{\text{PROG}}$	49	BA8	67	$\overline{\text{PE4}}$
14	P3.4 T0	32	P0.7	50	BA9	68	$\overline{\text{INTP}}$
15	P3.5 T1	33	P0.6	51	BA10	69	$\overline{\text{INTA}}$
16	P3.6 $\overline{\text{WR}}$	34	P0.5	52	BA11	70	SQW
17	P3.7 $\overline{\text{RD}}$	35	P0.4	53	BA12	71	$\overline{\text{VRST}}$
18	XTAL1	36	P0.3	54	BA13	72	BA15

PIN DESCRIPTION

PIN	DESCRIPTION
39–32	**P0.0 – P0.7.** General purpose I/O Port 0. This port is open–drain and can not drive a logic 1. It requires external pull–ups. Port 0 is also the multiplexed Expanded Address/Data bus. When used in this mode, it does not require pull–ups.
1–8	**P1.0 – P1.7.** General purpose I/O Port 1.
21–28	**P2.0 – P2.7.** General purpose I/O Port 2. Also serves as the MSB of the Expanded Address bus.
10	**P3.0 RXD.** General purpose I/O port pin 3.0. Also serves as the receive signal for the on board UART. This pin should NOT be connected directly to a PC COM port.
11	**P3.1 TXD.** General purpose I/O port pin 3.1. Also serves as the transmit signal for the on board UART. This pin should NOT be connected directly to a PC COM port.
12	**P3.2 $\overline{\text{INT0}}$.** General purpose I/O port pin 3.2. Also serves as the active low External Interrupt 0.
13	**P3.3 $\overline{\text{INT1}}$.** General purpose I/O port pin 3.3. Also serves as the active low External Interrupt 1.
14	**P3.4 T0.** General purpose I/O port pin 3.4. Also serves as the Timer 0 input.
15	**P3.5 T1.** General purpose I/O port pin 3.5. Also serves as the Timer 1 input.
16	**P3.6 $\overline{\text{WR}}$.** General purpose I/O port pin. Also serves as the write strobe for Expanded bus operation.
17	**P3.7 $\overline{\text{RD}}$.** General purpose I/O port pin. Also serves as the read strobe for Expanded bus operation.

PIN	DESCRIPTION
9	**RST –** Active high reset input. A logic 1 applied to this pin will activate a reset state. This pin is pulled down internally, can be left unconnected if not used. An RC power–on reset circuit is not needed and is NOT recommended.
29	**$\overline{\text{PSEN}}$ –** Program Store Enable. This active low signal is used to enable an external program memory when using the Expanded bus. It is normally an output and should be unconnected if not used.
30	**ALE –** Address Latch Enable. Used to de–multiplex the multiplexed Expanded Address/Data bus on Port 0. This pin is normally connected to the clock input on a '373 type transparent latch.
19, 18	**XTAL2, XTAL1.** Used to connect an external crystal to the internal oscillator. XTAL1 is the input to an inverting amplifier and XTAL2 is the output.
20	**GND –** Logic ground.
40	**V_{CC} – +5V**.
72	**BA15 –** Monitor test point to reflect the logical value of A15. Not needed for memory access.
54–41	**BA13 – 0.** Byte–wide Address bus bits 13–0. This bus is combined with the non–multiplexed data bus (BD7–0) to access on–board NV SRAM and off–board peripherals. Peripheral decoding is performed using $\overline{\text{PE3}}$ and $\overline{\text{PE4}}$. These are on 16K boundaries, so BA14 or BA15 are not needed. Read/write access is controlled by R/$\overline{\text{W}}$. BA13–0 connect directly to memory mapped peripherals.
63–56	**BD7 – 0.** Byte–wide Data bus bits 7–0. This 8–bit bi–directional bus is combined with the non–multiplexed address bus (BA14–0) to access on–board NV SRAM and off–board peripherals.
64	**R/$\overline{\text{W}}$ –** Read/Write. This signal provides the write enable to the SRAMs on the Byte–wide bus. It is controlled by the memory map and Partition. The blocks selected as Program (ROM) will be write protected. This signal is also used for the write enable to off–board peripherals.
66	**$\overline{\text{PE3}}$ –** Peripheral Enable 3. Accesses data memory between addresses 8000h and BFFFh when the PES bit is set to a logic 1. $\overline{\text{PE3}}$ is not lithium backed and can be connected to any type of peripheral function.
67	**$\overline{\text{PE4}}$ –** Peripheral Enable 4. Accesses data memory between addresses C000h and FFFFh when the PES bit is set to a logic 1. $\overline{\text{PE4}}$ is not lithium backed and can be connected to any type of peripheral function.
31	**$\overline{\text{PROG}}$ –** Invokes the Bootstrap loader on a falling edge. This signal should be debounced so that only one edge is detected. If connected to ground, the micro will enter Bootstrap loading on power–up. This signal is pulled up internally.
71	**$\overline{\text{VRST}}$ –** This I/O pin (open–drain with internal pull–up) indicates that the power supply (V_{CC}) has fallen below the V_{CCMIN} level and the micro is in a reset state. When this occurs, the DS2251T will drive this pin to a logic 0. Because the micro is lithium backed, this signal is guaranteed even when V_{CC}=0V. Because it is an I/O pin, it will also force a reset if pulled low externally. This allows multiple parts to synchronize their power–down resets.
65	**$\overline{\text{PF}}$ –** This output goes to a logic 0 to indicate that the micro has switched to lithium backup. It corresponds to $V_{CC} < V_{LI}$. Because the micro is lithium backed, this signal is guaranteed even when V_{CC}=0V.
55	**$\overline{\text{INTB}}$ –** $\overline{\text{INTB}}$ from the real time clock. This output may be connected to a micro interrupt input.
68	**$\overline{\text{INTP}}$ –** $\overline{\text{INTP}}$ from the real time clock. This open–drain output requires a pull–up and may beconnected to a micro interrupt input.

PIN	DESCRIPTION
69	**$\overline{\text{INTA}}$ –** $\overline{\text{INTA}}$ from the real time clock. This output may be connected to a micro interrupt input.
70	**SQW –** SQW output from the DS1283 Real Time Clock. Can be programmed to output an 1024 Hz square wave.

INSTRUCTION SET

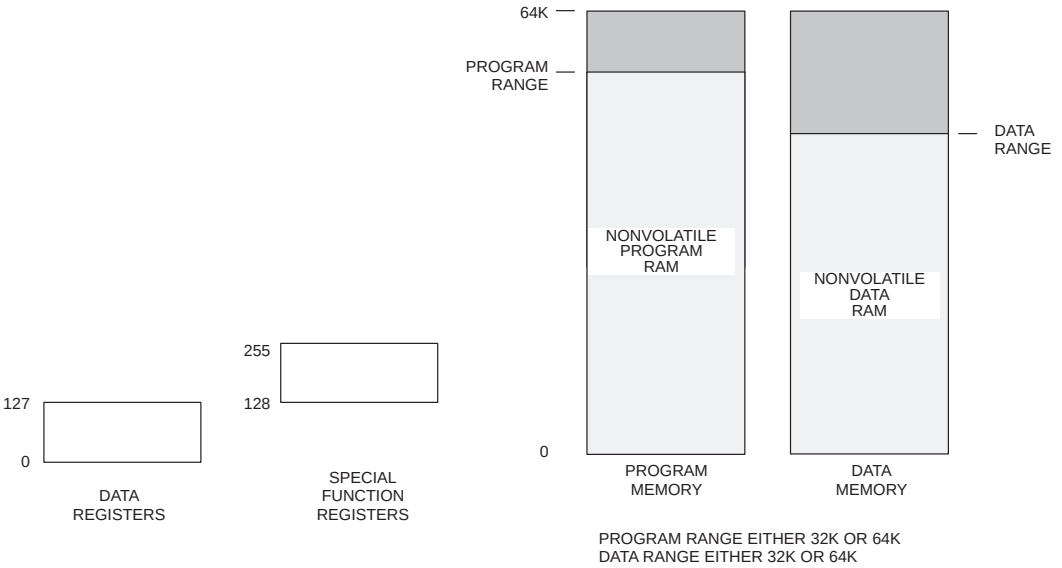
The DS2251T executes an instruction set that is object code compatible with the industry standard 8051 microcontroller. As a result, software development packages such as assemblers and compilers that have been written for the 8051 are compatible with the DS2251T.

A complete description of the instruction set and operation are provided in the User's Guide section of the Secure Microcontroller Data Book.

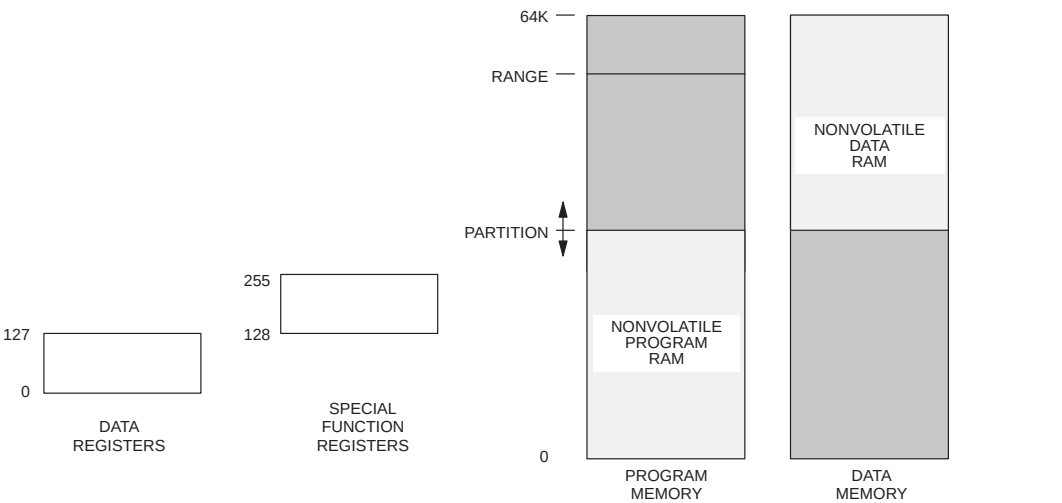
MEMORY ORGANIZATION

Figure 2 illustrates the memory map accessed by the DS2251T. The entire 64K of program and 64K of data are available to the Byte–wide bus. This preserves the I/O ports for application use. The user controls the portion of memory that is actually mapped to the Byte–wide bus by selecting the Program Range and Data Range. Any area not mapped into the NV RAM is reached via the Expanded bus on Ports 0 and 2. An alternate configuration allows dynamic Partitioning of a 64K space as shown in Figure 3. Selecting PES=1 provides access to the real time clock on the DS2251T and enables $\overline{\text{PE3}}$ and $\overline{\text{PE4}}$ for peripheral access as shown in Figure 4. These selections are made using Special Function Registers. The memory map and its controls are covered in detail in the User's Guide section of the Secure Microcontroller Data Book.

DS2251T MEMORY MAP IN NON–PARTITIONABLE MODE (PM=1) Figure 2



DS2251T MEMORY MAP IN PARTITIONABLE MODE (PM=0) Figure 3



NOTE: PARTITIONABLE MODE IS NOT SUPPORTED IN 128KB MODE.

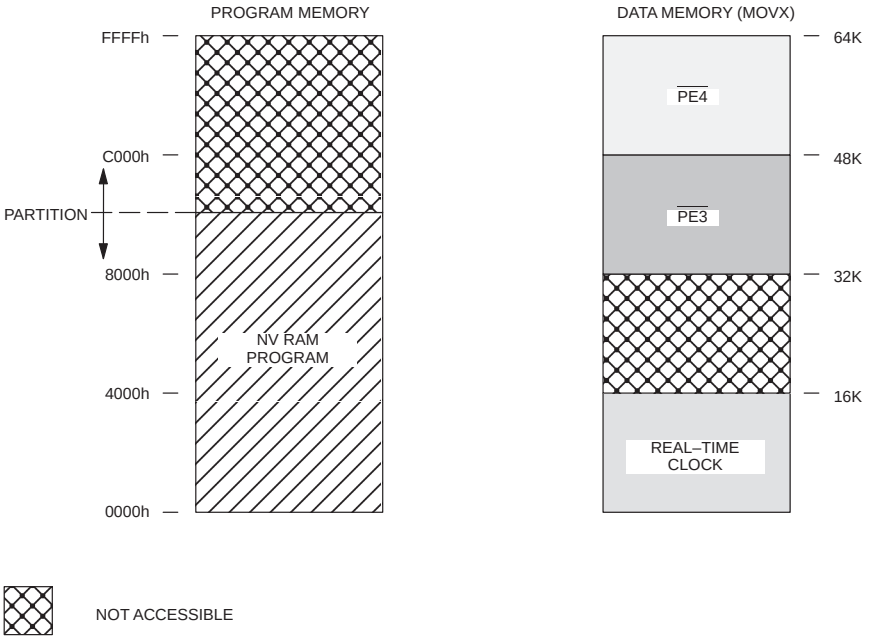
LEGEND:

= ON–CHIP REGISTERS

= ACCESSED VIA BYTEWIDE BUS

= ACCESSED VIA EXPANDED BUS (PORTS 0 AND 2)

DS2251T MEMORY MAP WITH (PES=1) Figure 4



POWER MANAGEMENT

The DS2251T monitors V_{CC} to provide Power–fail Reset, early warning Power–fail Interrupt, and switch over to lithium backup. It uses an internal band–gap reference in determining the switch points. These are called V_{PFW}, V_{CCMIN}, and V_{LI} respectively. When V_{CC} drops below V_{PFW}, the DS2251T will perform an interrupt vector to location 2Bh if the power–fail warning was enabled. Full processor operation continues regardless. When power falls further to V_{CCMIN}, the DS2251T invokes a reset state. No further code execution will be performed unless power rises back above V_{CCMIN}. All decoded chip enables and the R/$\overline{W}$ signal go to an inactive (logic 1) state. The $\overline{VRST}$ signal will be driven to a a logic 0. V_{CC} is still the power source at this time. When V_{CC} drops further to below V_{LI}, internal circuitry will switch to the built–in lithium cell for power. The majority of internal circuits will be disabled and the remaining nonvolatile states will be retained. $\overline{PF}$ will be driven to a logic 0. The User's Guide has more information on this topic. The trip points V_{CCMIN} and V_{PFW} are listed in the electrical specifications.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC CHARACTERISTICS

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

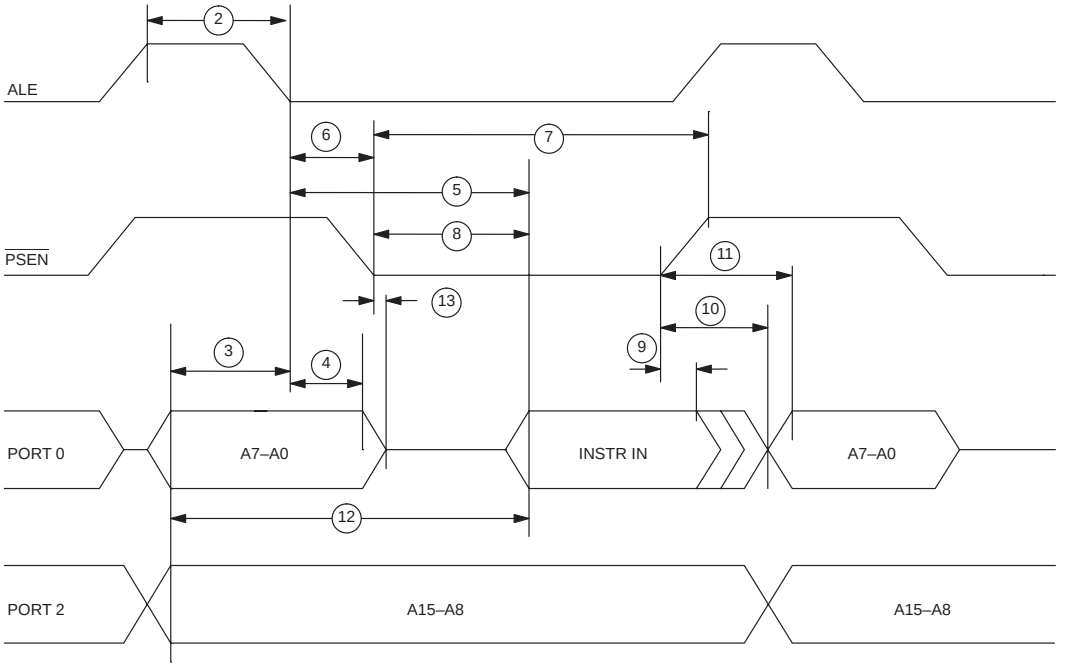
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Low Voltage	V_{IL}	–0.3		+0.8	V	1
Input High Voltage	V_{IH1}	2.0		V_{CC} +0.3	V	1
Input High Voltage RST, XTAL1 $\overline{PROG}$	V_{IH2}	3.5		V_{CC} +0.3	V	1
Output Low Voltage @ I_{OL}=1.6 mA (Ports 1, 2, 3)	V_{OL1}		0.15	0.45	V	1
Output Low Voltage @ I_{OL}=3.2 mA (Ports 0, ALE, $\overline{PSEN}$, $\overline{PF}$, BA13–0, BD7–0, R/$\overline{W}$, $\overline{PE}$3–4)	V_{OL2}		0.15	0.45	V	1
Output High Voltage @ I_{OH}= –80 µA (Ports 1, 2, 3)	V_{OH1}	2.4	4.8		V	1
Output High Voltage @ I_{OH}= –400 µA (Ports 0, ALE, $\overline{PSEN}$, $\overline{PF}$, BA13–0, BD7–0, R/$\overline{W}$, $\overline{PE}$3–4)	V_{OH2}	2.4	4.8		V	1
Input Low Current V_{IN} = 0.45V (Ports 1, 2, 3)	I_{IL}			–50	µA	
Transition Current; 1 to 0 V_{IN} = 2.0V (Ports 1, 2, 3)	I_{TL}			–500	µA	
Input Leakage Current 0.45 < V_{IN} < V_{CC} (Port 0)	I_{IL}			±10	µA	
RST Pull–down Resistor	R_{RE}	40		150	KΩ	
$\overline{VRST}$ Pull–up Resistor	R_{VR}		4.7		KΩ	
$\overline{PROG}$ Pull–up Resistor	R_{PR}		40		KΩ	
Power–Fail Warning Voltage	V_{PFW}	4.25	4.37	4.50	V	1
Minimum Operating Voltage	V_{CCmin}	4.00	4.12	4.25	V	1
Operating Current @ 16 MHz	I_{CC}			45	mA	2
Idle Mode Current @ 12 MHz	I_{IDLE}			7.0	mA	3
Stop Mode Current	I_{STOP}			80	µA	4
Pin Capacitance	C_{IN}			10	pF	5
Reset Trip Point in Stop Mode w/BAT=3.0V w/BAT=3.3V		 4.0 4.4		 4.25 4.65	V	1

AC CHARACTERISTICS
EXPANDED BUS MODE TIMING SPECIFICATIONS

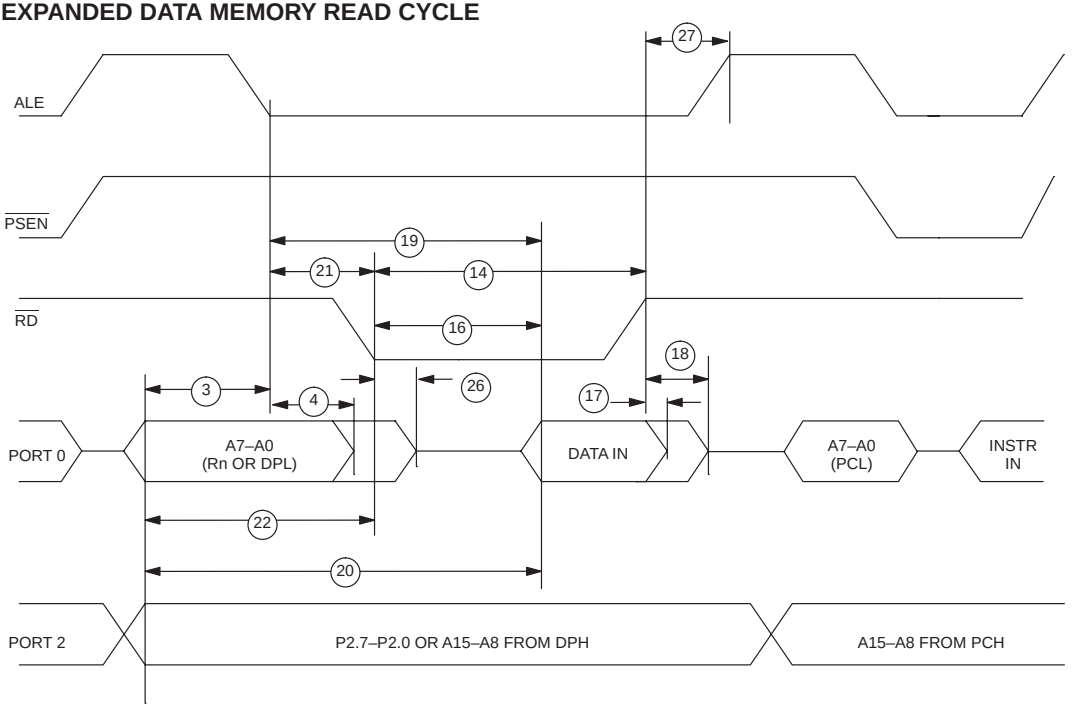
(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
1	Oscillator Frequency	$1/t_{CLK}$	1.0	16 (–16)	MHz
2	ALE Pulse Width	t_{ALPW}	$2t_{CLK}$–40		ns
3	Address Valid to ALE Low	t_{AVALL}	t_{CLK}–40		ns
4	Address Hold After ALE Low	t_{AVAAV}	t_{CLK}–35		ns
5	ALE Low to Valid Instr. In @12 MHz @16 MHz	t_{ALLVI}		$4t_{CLK}$–150 $4t_{CLK}$–90	ns
6	ALE Low to $\overline{PSEN}$ Low	t_{ALLPSL}	t_{CLK}–25		ns
7	$\overline{PSEN}$ Pulse Width	t_{PSPW}	$3t_{CLK}$–35		ns
8	$\overline{PSEN}$ Low to Valid Instr. In @12 MHz @16 MHz	t_{PSLVI}		$3t_{CLK}$–150 $3t_{CLK}$–90	ns ns
9	Input Instr. Hold after $\overline{PSEN}$ Going High	t_{PSIV}	0		ns
10	Input Instr. Float after $\overline{PSEN}$ Going High	t_{PSIX}		t_{CLK}–20	ns
11	Address Hold after $\overline{PSEN}$ Going High	t_{PSAV}	t_{CLK}–8		ns
12	Address Valid to Valid Instr. In @12 MHz @16 MHz	t_{AVVI}		$5t_{CLK}$–150 $5t_{CLK}$–90	ns ns
13	$\overline{PSEN}$ Low to Address Float	t_{PSLAZ}	0		ns
14	$\overline{RD}$ Pulse Width	t_{RDPW}	$6t_{CLK}$–100		ns
15	$\overline{WR}$ Pulse Width	t_{WRPW}	$6t_{CLK}$–100		ns
16	$\overline{RD}$ Low to Valid Data In @12 MHz @16 MHz	t_{RDLDV}		$5t_{CLK}$–165 $5t_{CLK}$–105	ns ns
17	Data Hold after $\overline{RD}$ High	t_{RDHDV}	0		ns
18	Data Float after $\overline{RD}$ High	t_{RDHDZ}		$2t_{CLK}$–70	ns
19	ALE Low to Valid Data In @12 MHz @16 MHz	t_{ALLVD}		$8t_{CLK}$–150 $8t_{CLK}$–90	ns ns
20	Valid Addr. to Valid Data In @12 MHz @16 MHz	t_{AVDV}		$9t_{CLK}$–165 $9t_{CLK}$–105	ns ns
21	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{ALLRDL}	$3t_{CLK}$–50	$3t_{CLK}$+50	ns
22	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVRDL}	$4t_{CLK}$–130		ns
23	Data Valid to $\overline{WR}$ Going Low	t_{DVWRL}	t_{CLK}–60		ns
24	Data Valid to $\overline{WR}$ High @12 MHz @16 MHz	t_{DVWRH}	$7t_{CLK}$–150 $7t_{CLK}$–90		ns ns
25	Data Valid after $\overline{WR}$ High	t_{WRHDV}	t_{CLK}–50		ns
26	$\overline{RD}$ Low to Address Float	t_{RDLAZ}		0	ns
27	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{RDHALH}	t_{CLK}–40	t_{CLK}+50	ns

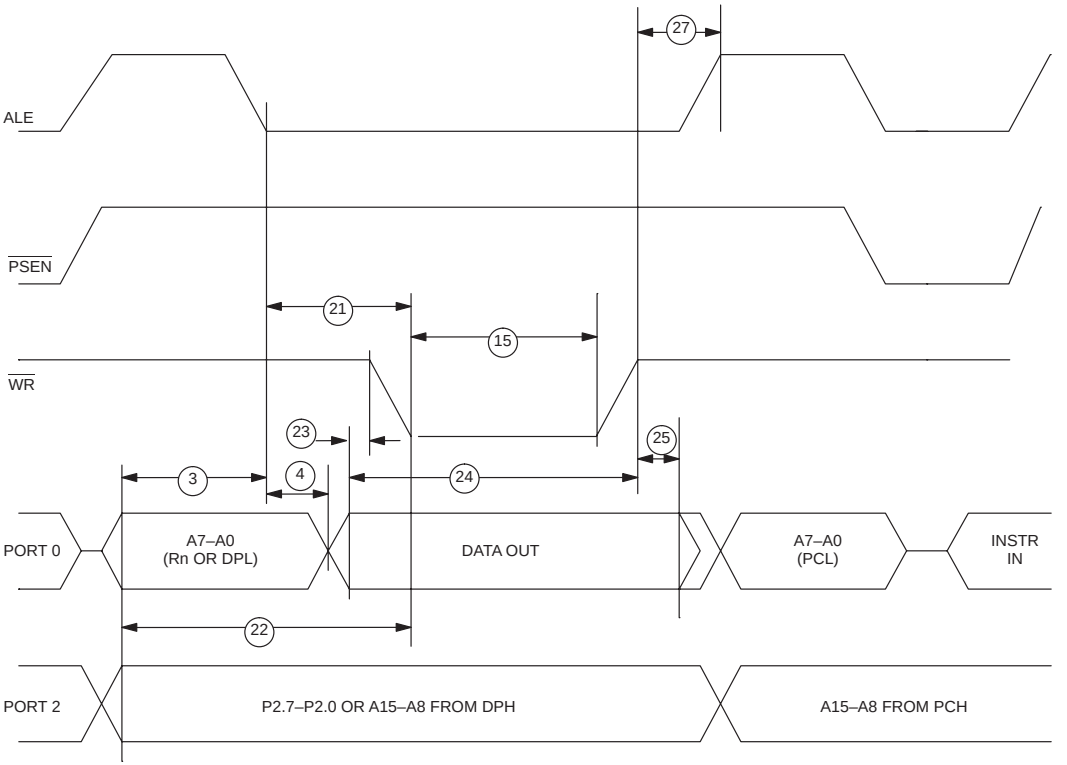
EXPANDED PROGRAM MEMORY READ CYCLE



EXPANDED DATA MEMORY READ CYCLE



EXPANDED DATA MEMORY WRITE CYCLE

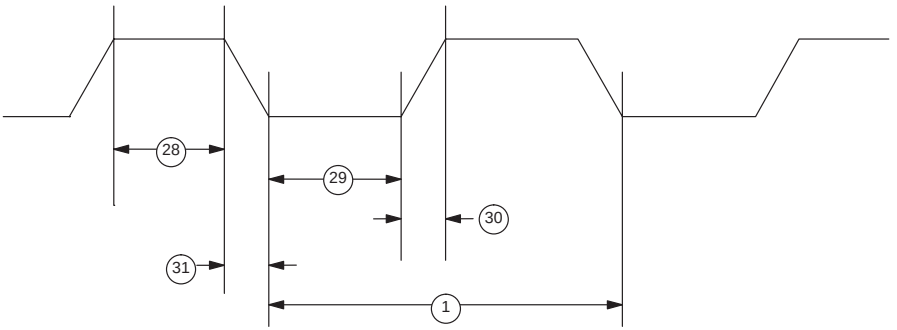


AC CHARACTERISTICS (cont'd)
EXTERNAL CLOCK DRIVE

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
28	External Clock High Time @12 MHz @16 MHz	t_{CLKHPW}	20 15		ns ns
29	External Clock Low Time @12 MHz @16 MHz	t_{CLKLPW}	20 15		ns ns
30	External Clock Rise Time @12 MHz @16 MHz	t_{CLKR}		20 15	ns ns
31	External Clock Fall Time @12 MHz @16 MHz	t_{CLKF}		20 15	ns ns

EXTERNAL CLOCK TIMING

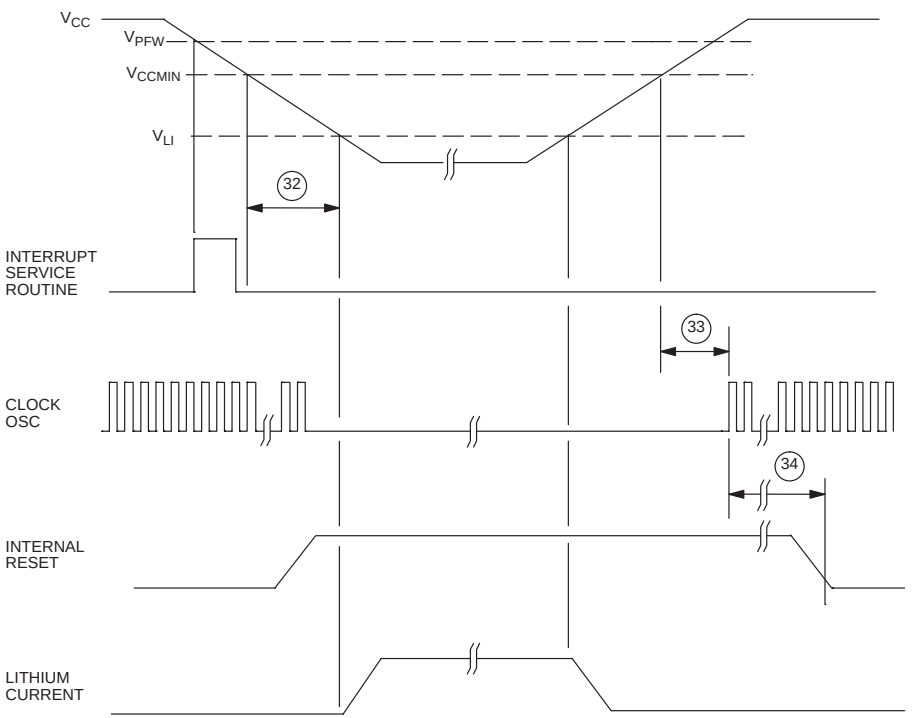


AC CHARACTERISTICS (cont'd)
POWER CYCLING TIMING

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
32	Slew Rate from V_{CCMIN} to 3.3V	t_F	130		µs
33	Crystal Start up Time	t_{CSU}		(note 6)	
34	Power On Reset Delay	t_{POR}		21504	t_{CLK}

POWER CYCLE TIMING

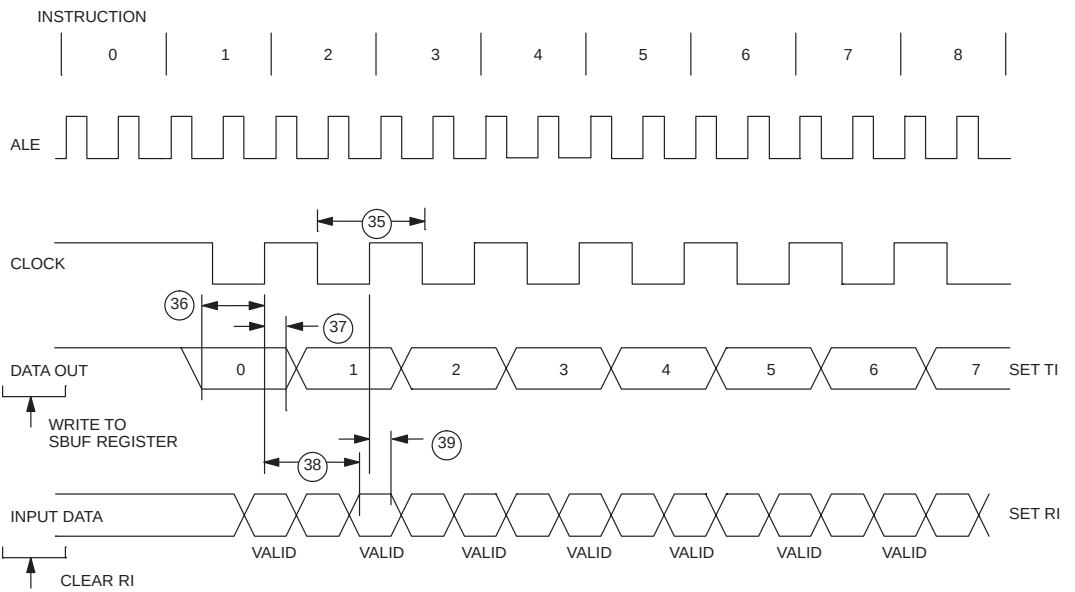


AC CHARACTERISTICS (cont'd)
SERIAL PORT TIMING – MODE 0

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
35	Serial Port Clock Cycle Time	t_{SPCLK}	$12t_{CLK}$		µs
36	Output Data Setup to Rising Clock Edge	t_{DOCH}	$10t_{CLK}$–133		ns
37	Output Data Hold after Rising Clock Edge	t_{CHDO}	$2t_{CLK}$–117		ns
38	Clock Rising Edge to Input Data Valid	t_{CHDV}		$10t_{CLK}$–133	ns
39	Input Data Hold after Rising Clock Edge	t_{CHDIV}	0		ns

SERIAL PORT TIMING – MODE 0



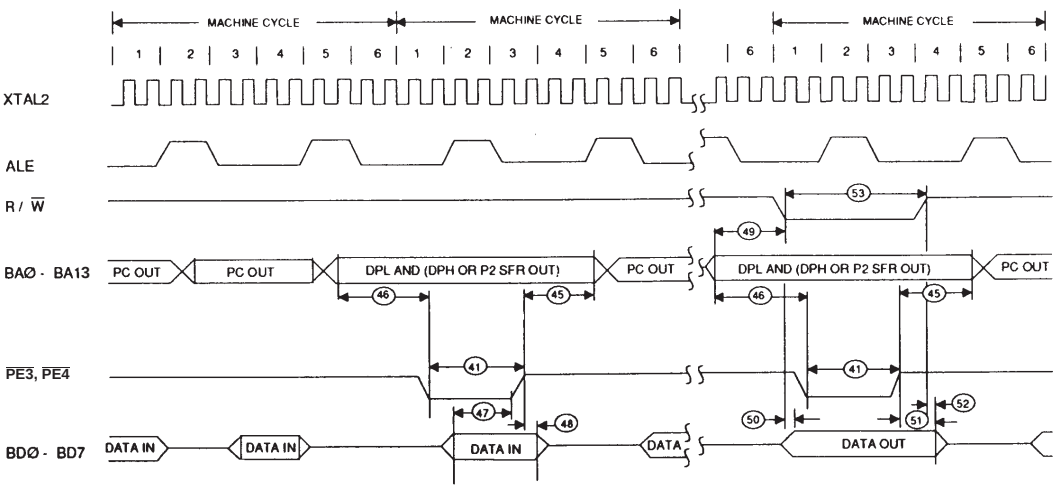
AC CHARACTERISTICS (cont'd)

PARALLEL PROGRAM LOAD TIMING

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
41	Pulse Width of $\overline{PE}$3–4	t_{CEPW}	$4t_{CLK}$–35		ns
45	Byte–wide Address Hold after $\overline{PE}$3–4 High During MOVX	t_{CEHDA}	$4t_{CLK}$–30		ns
46	Delay from Byte–wide Address Valid $\overline{PE}$3–4 Low During MOVX	t_{CELDA}	$4t_{CLK}$–35		ns
47	Byte–wide Data Setup to $\overline{PE}$3–4 High During MOVX (read)	t_{DACEH}	$1t_{CLK}$+40		ns
48	Byte–wide Data Hold after $\overline{PE}$3–4 High During MOVX (read)	t_{CEHDV}	10		ns
49	Byte–wide Address Valid to R/$\overline{W}$ Active During MOVX (write)	t_{AVRWL}	$3t_{CLK}$–35		ns
50	Delay from R/$\overline{W}$ Low to Valid Data Out During MOVX (write)	t_{RWLDV}	20		ns
51	Valid Data Out Hold Time from $\overline{PE}$3–4 High	t_{CEHDV}	$1t_{CLK}$–15		ns
52	Valid Data Out Hold Time from R/$\overline{W}$ High	t_{RWHDV}	0		ns
53	Write Pulse Width (R/$\overline{W}$ Low Time)	t_{RWLPW}	$6t_{CLK}$–20		ns

BYTE–WIDE BUS TIMING



RPC AC CHARACTERISTICS – DBB READ

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
54	$\overline{CS}$, A_0 Setup to $\overline{RD}$	t_{AR}	0		ns
55	$\overline{CS}$, A_0 Hold After $\overline{RD}$	t_{RA}	0		ns
56	$\overline{RD}$ Pulse Width	t_{RR}	160		ns
57	$\overline{CS}$, A_0 to Data Out Delay	t_{AD}		130	ns
58	$\overline{RD}$ to Data Out Delay	t_{RD}	0	130	ns
59	$\overline{RD}$ to Data Float Delay	t_{RDZ}		85	ns

RPC AC CHARACTERISTICS – DBB WRITE

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

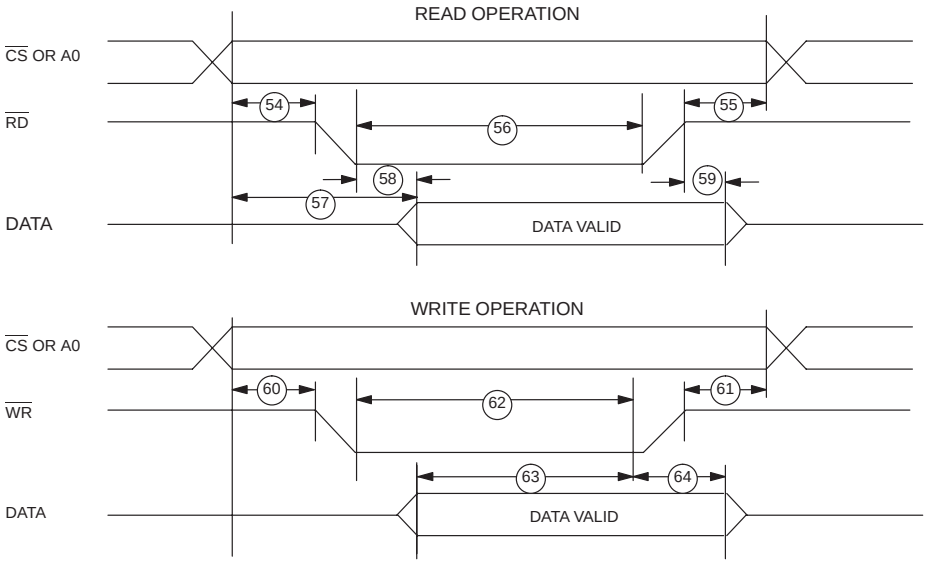
#	PARAMETER	SYMBOL	MIN	MAX	UNITS
60	$\overline{CS}$, A_0 Setup to $\overline{WR}$	t_{AW}	0		ns
61A	$\overline{CS}$, Hold After $\overline{WR}$	t_{WA}	0		ns
61B	A_0, Hold After $\overline{WR}$	t_{WA}	20		ns
62	$\overline{WR}$ Pulse Width	t_{WW}	20		ns
63	Data Setup to $\overline{WR}$	t_{DW}	130		ns
64	Data Hold After $\overline{WR}$	t_{WD}	20		ns

AC CHARACTERISTICS – DMA

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
65	$\overline{DACK}$ to $\overline{WR}$ or $\overline{RD}$	t_{ACC}	0		ns
66	$\overline{RD}$ or $\overline{WR}$ to $\overline{DACK}$	t_{CAC}	0		ns
67	$\overline{DACK}$ to Data Valid	t_{ACD}	0	130	ns
68	$\overline{RD}$ or $\overline{WR}$ to DRQ Cleared	t_{CRQ}		110	ns

RPC TIMING MODE 16

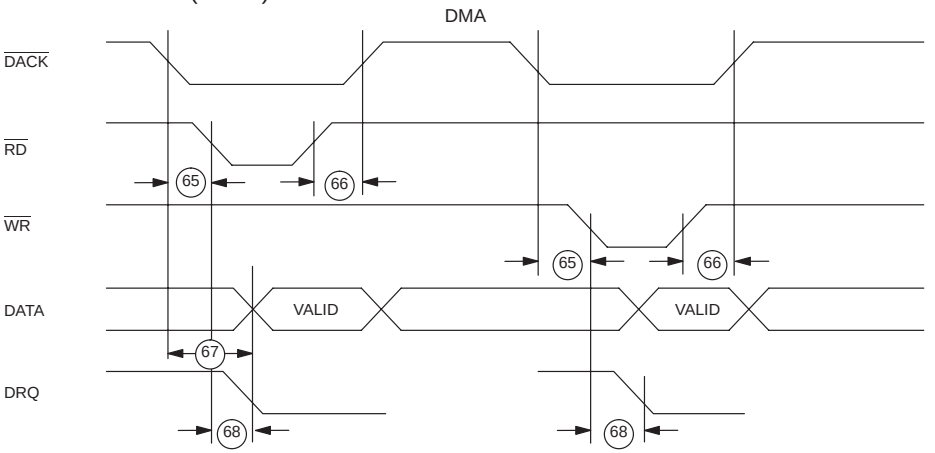


AC CHARACTERISTICS – PROG

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
69	PROG Low to Active	t_{PRA}	48		CLKS
70	PROG High to Inactive	t_{PRI}	48		CLKS

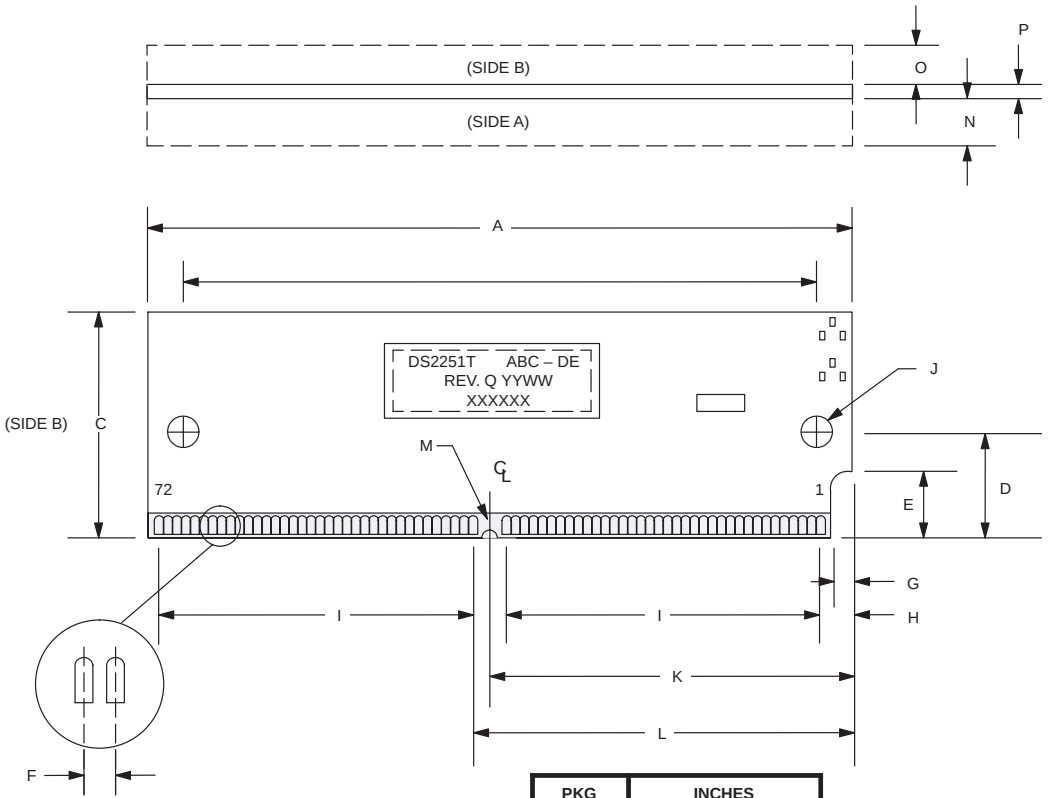
RPC TIMING MODE 16 (cont'd)



NOTES:

1. All voltages are referenced to ground.
2. Maximum operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF}=10 ns, V_{IL} = 0.5V; XTAL2 disconnected; RST = PORT0 = V_{CC}.
3. Idle mode I_{IDLE} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF} = 10 ns, V_{IL} = 0.5V; XTAL2 disconnected; PORT0 = V_{CC}, RST = V_{SS}.
4. Stop mode I_{STOP} is measured with all output pins disconnected; PORT0 = V_{CC}; XTAL2 not connected; RST = XTAL1 = V_{SS}.
5. Pin capacitance is measured with a test frequency – 1 MHz, t_A = 25°C.
6. Crystal start–up time is the time required to get the mass of the crystal into vibrational motion from the time that power is first applied to the circuit until the first clock pulse is produced by the on–chip oscillator. The user should check with the crystal vendor for a worst case specification on this time.

PACKAGE DRAWING



PKG	INCHES	
DIM	MIN	MAX
A	4.245	4.255
B	3.979	3.989
C	0.995	1.005
D	0.395	0.405
E	0.245	0.255
F	0.050 BSC	
G	0.075	0.085
H	0.245	0.255
I	1.750 BSC	
J	0.120	0.130
K	2.120	2.130
L	2.245	2.255
M	0.057	0.067
N	–	0.275
O	–	0.145
P	0.047	0.054

DATA SHEET REVISION SUMMARY

The following represent the key differences between 12/13/95 and 08/13/96 version of the DS2251T data sheet. Please review this summary carefully.

1. Change V_{CC} slew rate definition to reference 3.3V instead of V_{LI}.
2. Add minimum value to PCB thickness.

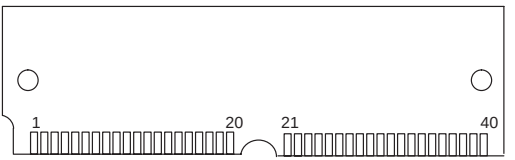
DALLAS SEMICONDUCTOR

DS2252T
Secure Microcontroller Module

FEATURES

- 8051 compatible microcontroller for secure/sensitive applications
  - 32K, 64K, or 128K bytes of nonvolatile SRAM for program and/or data storage
  - In–system programming via on–chip serial port
  - Capable of modifying its own program or data memory in the end system
- Firmware Security Features:
  - Memory stored in encrypted form
  - Encryption using on–chip 64–bit key
  - Automatic true random key generator
  - SDI Self Destruct Input
  - Improved security over previous generations
  - Protects memory contents from piracy
- Crashproof Operation
  - Maintains all nonvolatile resources for over 10 years in the absence of power
  - Power–fail Reset
  - Early Warning Power–fail Interrupt
  - Watchdog Timer
  - Precision reference for power monitor
- Fully 8051 Compatible
  - 128 bytes scratchpad RAM
  - Two timer/counters
  - On–chip serial port
  - 32 parallel I/O port pins
- Permanently powered real time clock

PACKAGE OUTLINE



40–PIN SIMM

DESCRIPTION

The DS2252T is an 8051 compatible microcontroller based on nonvolatile RAM technology. It is designed for systems that need to protect memory contents from disclosure. This includes key data, sensitive algorithms, and proprietary information of all types. Like other members of the Secure Microcontroller family, it provides full compatibility with the 8051 instruction set, timers, serial port, and parallel I/O ports. By using NV RAM instead of ROM, the user can program, then reprogram the microcontroller while in–system. This allows frequent changing of sensitive processes with minimal effort. The DS2252T provides an array of mechanisms to prevent an attacker from examining the memory. It is designed to resist all levels of threat including observation, analysis, and physical attack. As a result, a massive effort would be required to obtain any information about memory contents. Furthermore, the “Soft” nature of the DS2252T allows frequent modification of secure information. This minimizes that value of any information that is obtained.

Using a security system based on the DS5002FP, the DS2252T protects the memory contents from disclosure. It loads program memory via its serial port and encrypts it in real–time prior to storing it in SRAM. Once encrypted, the RAM contents and the program flow are unintelligible. The real data exists only inside the processor chip after being decrypted. Any attempt to discover the on–chip data, encryption keys, etc., results in its destruction. Extensive use of nonvolatile lithium backed technology create a microcontroller that retains

data for over 10 years at room temperature, but which can be erased instantly if tampered with. The DS2252T even interfaces directly to external tamper protection hardware.

The DS2252T provides a permanently powered real time lock with interrupts for time stamp and date. It keeps time to one hundredth of a second using its on–board 32 KHz crystal.

Like other Secure Microcontrollers in the family, the DS2252T provides crashproof operation in portable systems or systems with unreliable power. These features include the ability to save the operating state, Power–fail Reset, Power–fail Interrupt, and Watchdog Timer. All nonvolatile memory and resources are maintained for over 10 years at room temperature in the absence of power.

A user loads programs into the DS2252T via its on–chip Serial Bootstrap Loader. This function supervises the loading of software into NV RAM, validates it, then becomes transparent to the user. It also manages the loading of new encryption keys automatically. Software is stored in on–board CMOS SRAM. Using its internal Partitioning, the DS2252T can divide a common RAM into user selectable program and data segments. This Partition can be selected at program loading time, but can be modified anytime later. The microcontroller will decode memory access to the SRAM, access memory via its Byte–wide bus and write–protect the memory portion designated as program (ROM).

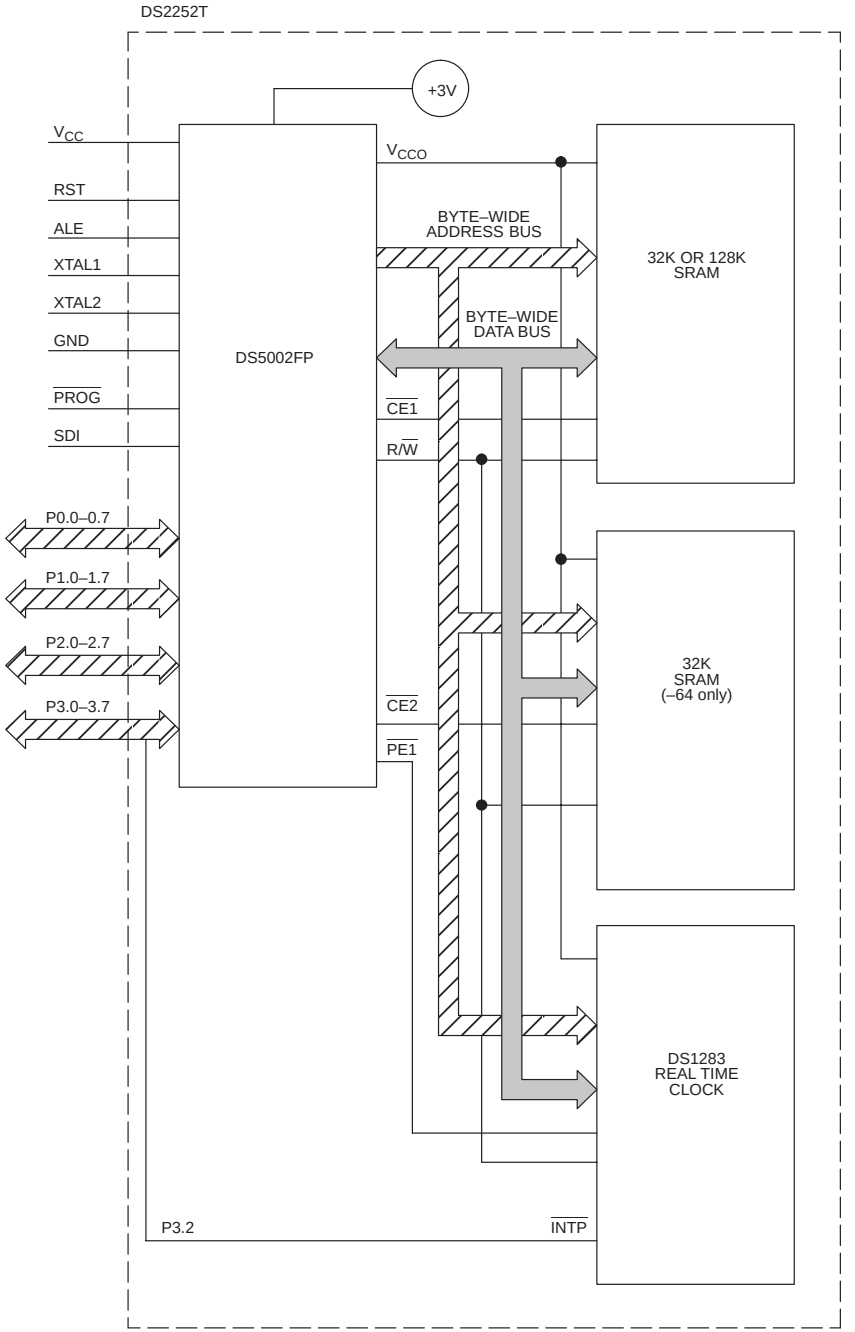
A detailed summary of the security features is provided in the User's Guide section of the Secure Microcontroller data book. An overview is also available in the DS5002FP data sheet.

ORDERING INFORMATION

PART NUMBER	RAM SIZE	MAX CRYSTAL SPEED	TIMEKEEPING?
DS2252T–32–16	32K bytes	16 MHz	Yes
DS2252T–64–16	64K bytes	16 MHz	Yes
DS2252T–128–16	128K bytes	16 MHz	Yes

Operating information is contained in the User's Guide section of the Secure Microcontroller Data Book. This data sheet provides ordering information, pinout, and electrical specifications.

DS2252T BLOCK DIAGRAM Figure 1



PIN ASSIGNMENT

1	P1.0	11	P1.5	21	P3.1 TXD	31	P3.6 $\overline{WR}$
2	V_{CC}	12	P0.4	22	ALE	32	P2.4
3	P1.1	13	P1.6	23	P3.2 $\overline{INT0}$	33	P3.7 $\overline{RD}$
4	P0.0	14	P0.5	24	$\overline{PROG}$	34	P2.3
5	P1.2	15	P1.7	25	P3.3 $\overline{INT1}$	35	XTAL2
6	P0.1	16	P0.6	26	P2.7	36	P2.2
7	P1.3	17	RST	27	P3.4 T0	37	XTAL1
8	P0.2	18	P0.7	28	P2.6	38	P2.1
9	P1.4	19	P3.0 RXD	29	P3.5 T1	39	GND
10	P0.3	20	SDI	30	P2.5	40	P2.0

PIN DESCRIPTION

PIN	DESCRIPTION
4, 6, 8, 10, 12, 14, 16, 18	**P0.0 – P0.7.** General purpose I/O Port 0. This port is open–drain and can not drive a logic 1. It requires external pull–ups. Port 0 is also the multiplexed Expanded Address/Data bus. When used in this mode, it does not require pull–ups.
1, 3, 5, 7, 9, 11, 13, 15	**P1.0 – P1.7.** General purpose I/O Port 1.
40, 38, 36, 34, 32, 30, 28, 26	**P2.0 – P2.7.** General purpose I/O Port 2. Also serves as the MSB of the Expanded Address bus.
19	**P3.0 RXD.** General purpose I/O port pin 3.0. Also serves as the receive signal for the on board UART. This pin should NOT be connected directly to a PC COM port.
21	**P3.1 TXD.** General purpose I/O port pin 3.1. Also serves as the transmit signal for the on board UART. This pin should NOT be connected directly to a PC COM port.
23	**P3.2 $\overline{INT0}$.** General purpose I/O port pin 3.2. Also serves as the active low External Interrupt 0. This pin is also connected to the $\overline{INTP}$ output of the DS1283 Real Time Clock.
25	**P3.3 $\overline{INT1}$.** General purpose I/O port pin 3.3. Also serves as the active low External Interrupt 1.
27	**P3.4 T0.** General purpose I/O port pin 3.4. Also serves as the Timer 0 input.
29	**P3.5 T1.** General purpose I/O port pin 3.5. Also serves as the Timer 1 input.
31	**P3.6 $\overline{WR}$.** General purpose I/O port pin. Also serves as the write strobe for Expanded bus operation.
33	**P3.7 $\overline{RD}$.** General purpose I/O port pin. Also serves as the read strobe for Expanded bus operation.
17	**RST** – Active high reset input. A logic 1 applied to this pin will activate a reset state. This pin is pulled down internally, can be left unconnected if not used. An RC power–on reset circuit is not needed and is NOT recommended.
22	**ALE** – Address Latch Enable. Used to de–multiplex the multiplexed Expanded Address/Data bus on Port 0. This pin is normally connected to the clock input on a '373 type transparent latch.

PIN	DESCRIPTION
35, 37	**XTAL2, XTAL1.** Used to connect an external crystal to the internal oscillator. XTAL1 is the input to an inverting amplifier and XTAL2 is the output.
39	**GND –** Logic ground.
2	**V_{CC} – +5V**.
24	**$\overline{\text{PROG}}$** – Invokes the Bootstrap loader on a falling edge. This signal should be debounced so that only one edge is detected. If connected to ground, the microcontroller will enter Bootstrap loading on power up. This signal is pulled up internally.
20	**SDI** – Self Destruct Input. A logic 1 applied to this input causes a hardware unlock. This involves the destruction of Encryption Keys, Vector RAM, and the momentary removal of power from V_{CCO}. This pin should be grounded if not used.

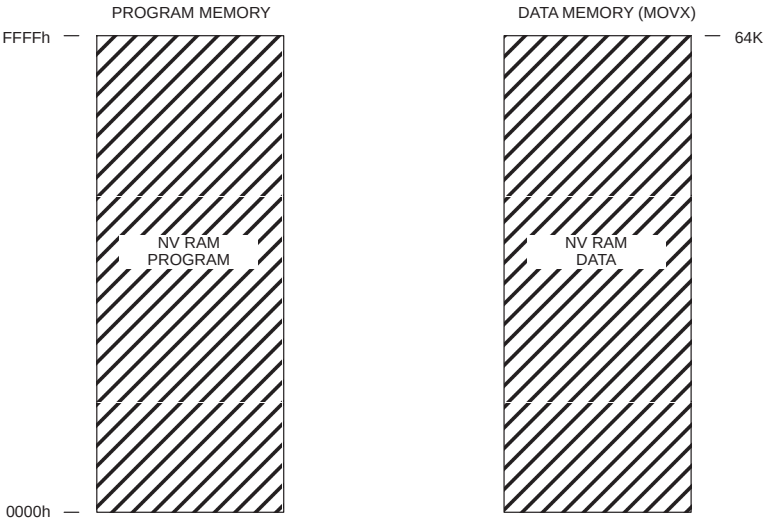
INSTRUCTION SET

The DS2252T executes an instruction set that is object code compatible with the industry standard 8051 microcontroller. As a result, software development packages such as assemblers and compilers that have been written for the 8051 are compatible with the DS2252T. A complete description of the instruction set and operation are provided in the User's Guide section of the Secure Microcontroller Data Book.

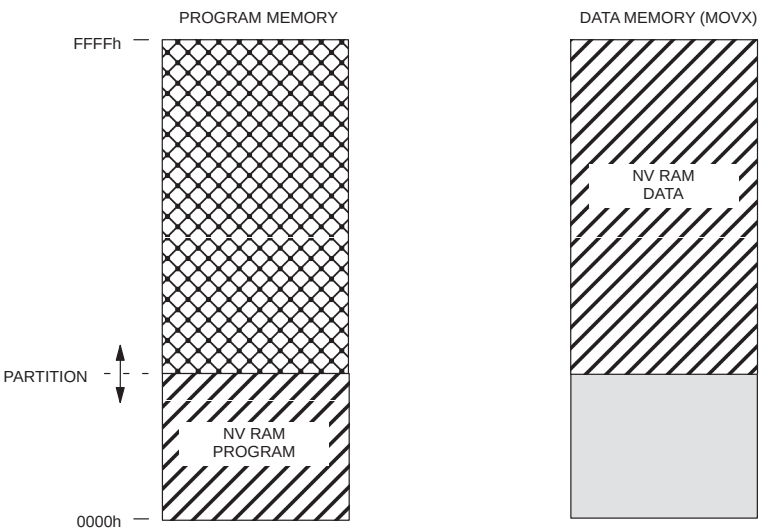
MEMORY ORGANIZATION

Figure 2 illustrates the memory map accessed by the DS2252T. The entire 64K of program and 64K of data are available to the Byte–wide bus. This preserves the I/O ports for application use. An alternate configuration allows dynamic Partitioning of a 64K space as shown in Figure 3. Any data area not mapped into the NV RAM is reached via the Expanded bus on Ports 0 and 2. Off–board program memory is not available for security reasons. Selecting PES=1 provides access to the Real Time Clock as shown in Figure 4. These selections are made using Special Function Registers. The memory map and its controls are covered in detail in the User's Guide section of the Secure Microcontroller Data Book.

DS2252T MEMORY MAP IN NON–PARTITIONABLE MODE (PM=1) Figure 2



DS2252T MEMORY MAP IN PARTITIONABLE MODE (PM=0) Figure 3



NOTE: PARTITIONABLE MODE IS NOT SUPPORTED ON THE 128KB VERSION OF THE DS2252T.

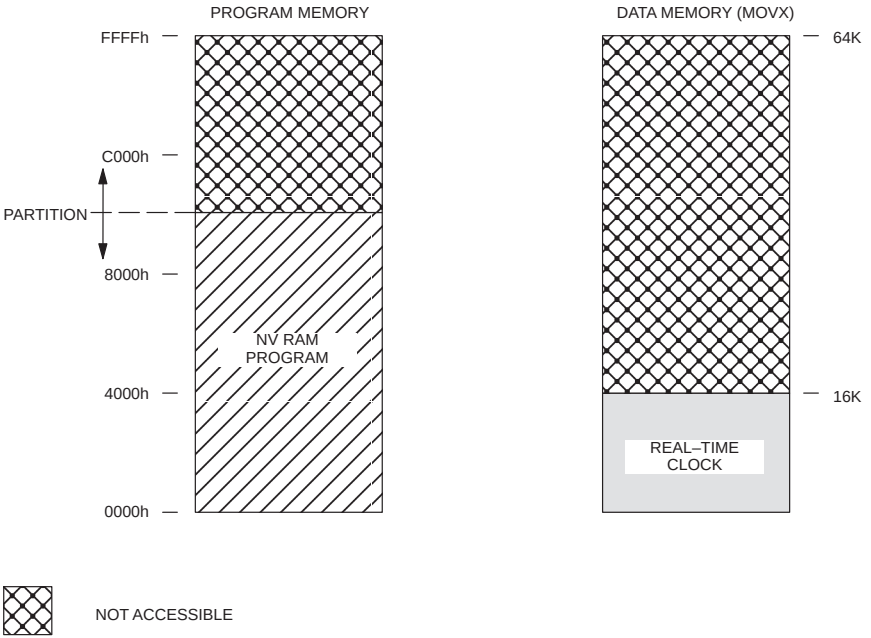
LEGEND:

= NV RAM MEMORY

= NOT AVAILABLE

= EXPANDED BUS (PORTS 0 AND 2)

DS2252T MEMORY MAP WITH (PES=1) Figure 4



POWER MANAGEMENT

The DS2252T monitors V_{CC} to provide Power–fail Reset, early warning Power–fail Interrupt, and switch over to lithium backup. It uses an internal band–gap reference in determining the switch points. These are called V_{PFW}, V_{CCMIN}, and V_{LI} respectively. When V_{CC} drops below V_{PFW}, the DS2252T will perform an interrupt vector to location 2Bh if the power–fail warning was enabled. Full processor operation continues regardless. When power falls further to V_{CCMIN}, the DS2252T invokes a reset state. No further code execution will be performed unless power rises back above V_{CCMIN}. All decoded chip enables and the R/$\overline{W}$ signal go to an inactive (logic 1) state. V_{CC} is still the power source at this time. When V_{CC} drops further to below V_{LI}, internal circuitry will switch to the built–in lithium cell for power. The majority of internal circuits will be disabled and the remaining nonvolatile states will be retained. The User's Guide has more information on this topic. The trip points V_{CCMIN} and V_{PFW} are listed in the electrical specifications.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC CHARACTERISTICS

(t_A=0°C to 70°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Low Voltage	V_{IL}	–0.3		+0.8	V	1
Input High Voltage	V_{IH1}	2.0		V_{CC}+0.3	V	1
Input High Voltage (RST, XTAL1, PROG)	V_{IH2}	3.5		V_{CC}+0.3	V	1
Output Low Voltage @ I_{OL}=1.6 mA (Ports 1, 2, 3)	V_{OL1}		0.15	0.45	V	1
Output Low Voltage @ I_{OL}=3.2 mA (Ports 0, ALE)	V_{OL2}		0.15	0.45	V	1
Output High Voltage @ I_{OH}=–80 µA (Ports 1, 2, 3)	V_{OH1}	2.4	4.8		V	1
Output High Voltage @ I_{OH}=–400 µA (Ports 0, ALE)	V_{OH2}	2.4	4.8		V	1
Input Low Current V_{IN}=0.45V (Ports 1, 2, 3)	I_{IL}			–50	µA	
Transition Current; 1 to 0 V_{IN}=2.0V (Ports 1, 2, 3)	I_{TL}			–500	µA	
Input Leakage Current 0.45<V_{IN}<V_{CC} (Port 0)	I_{IL}			±10	µA	
RST Pulldown Resistor	R_{RE}	40		150	KΩ	
Power Fail Warning Voltage	V_{PRW}	4.25	4.37	4.50	V	1
Minimum Operating Voltage	V_{CCMIN}	4.00	4.12	4.25	V	1
Operating Current @ 16 MHz	I_{CC}			45	mA	4
Idle Mode Current @ 12 MHz	I_{IDLE}			7.0	mA	5
Stop Mode current	I_{STOP}			80	µA	6
Pin Capacitance	C_{IN}			10	pF	7
Reset Trip Point in Stop Mode w/BAT=3.0V w/BAT=3.3V		 4.0 4.4		 4.25 4.65	V	1
SDI Input Low Voltage	V_{ILS}			0.4	V	1
SDI Input High Voltage	V_{IHS}	2.0		V_{CC}	V	1, 2
SDI Input High Voltage	V_{IHS}	2.0		3.5	V	1, 2
SDI Pull–Down Resistor	R_{SDI}	25		60	KΩ	

AC CHARACTERISTICS

(t_A = 0°C to70°C; V_{CC}=0V to 5V)

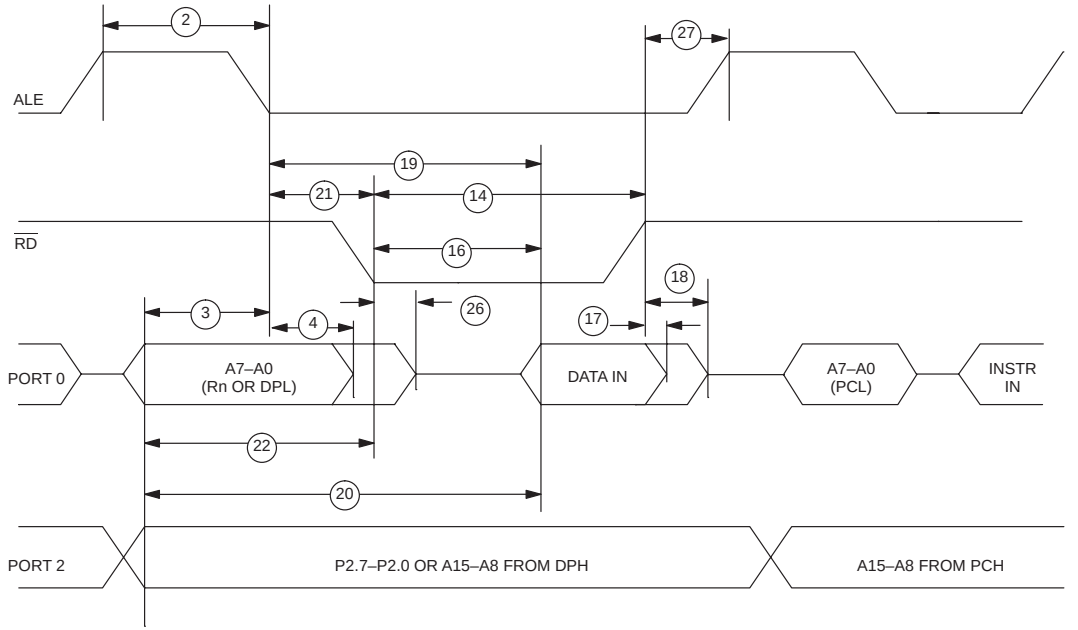
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SDI Pulse Reject	t_{SPR}			2	µs	3
SDI Pulse Accept	t_{SPA}	10			µs	3

AC CHARACTERISTICS
EXPANDED BUS MODE TIMING SPECIFICATIONS

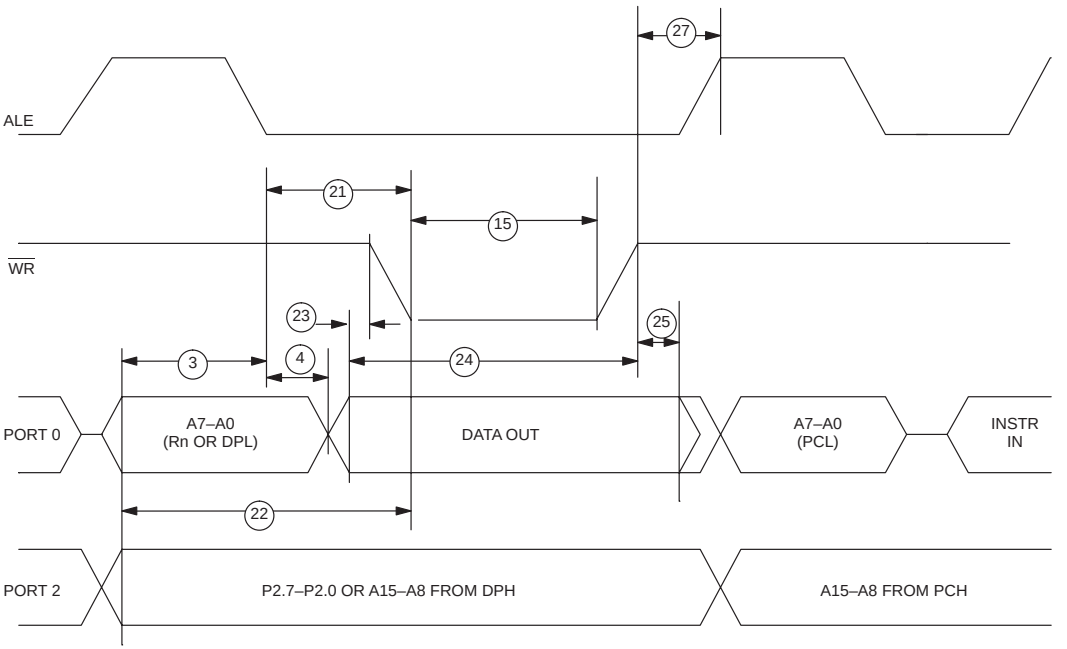
(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
1	Oscillator Frequency	$1/t_{CLK}$	1.0	16 (–16)	MHz
2	ALE Pulse Width	t_{ALPW}	$2t_{CLK}$–40		ns
3	Address Valid to ALE Low	t_{AVALL}	t_{CLK}–40		ns
4	Address Hold After ALE Low	t_{AVAAV}	t_{CLK}–35		ns
14	$\overline{RD}$ Pulse Width	t_{RDPW}	$6t_{CLK}$–100		ns
15	$\overline{WR}$ Pulse Width	t_{WRPW}	$6t_{CLK}$–100		ns
16	$\overline{RD}$ Low to Valid Data In @12 MHz @16 MHz	t_{RDLDV}		$5t_{CLK}$–165 $5t_{CLK}$–105	ns ns
17	Data Hold after $\overline{RD}$ High	t_{RDHDV}	0		ns
18	Data Float after $\overline{RD}$ High	t_{RDHDZ}		$2t_{CLK}$–70	ns
19	ALE Low to Valid Data In @12 MHz @16 MHz	t_{ALLVD}		$8t_{CLK}$–150 $8t_{CLK}$–90	ns ns
20	Valid Addr. to Valid Data In @12 MHz @16 MHz	t_{AVDV}		$9t_{CLK}$–165 $9t_{CLK}$–105	ns ns
21	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{ALLRDL}	$3t_{CLK}$–50	$3t_{CLK}$+50	ns
22	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVRDL}	$4t_{CLK}$–130		ns
23	Data Valid to $\overline{WR}$ Going Low	t_{DVWRL}	t_{CLK}–60		ns
24	Data Valid to $\overline{WR}$ High @12 MHz @16 MHz	t_{DVWRH}	$7t_{CLK}$–150 $7t_{CLK}$–90		ns ns
25	Data Valid after $\overline{WR}$ High	t_{WRHDV}	t_{CLK}–50		ns
26	$\overline{RD}$ Low to Address Float	t_{RDLAZ}		0	ns
27	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{RDHALH}	t_{CLK}–40	t_{CLK}+50	ns

EXPANDED DATA MEMORY READ CYCLE



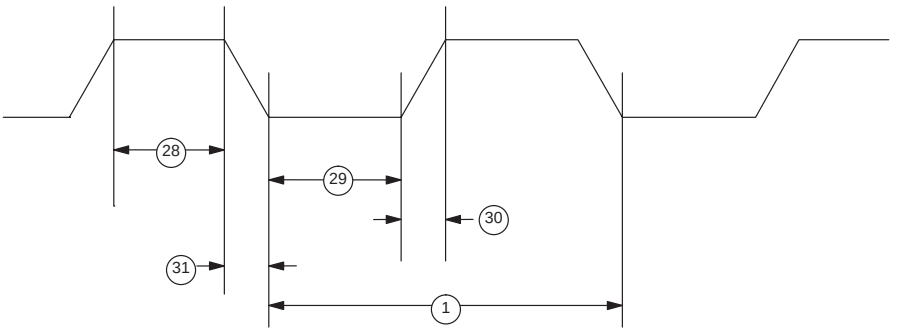
EXPANDED DATA MEMORY WRITE CYCLE



AC CHARACTERISTICS (cont'd)
EXTERNAL CLOCK DRIVE (t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
28	External Clock High Time @12 MHz @16 MHz	t_{CLKHPW}	20 15		ns ns
29	External Clock Low Time @12 MHz @16 MHz	t_{CLKLPW}	20 15		ns ns
30	External Clock Rise Time @12 MHz @16 MHz	t_{CLKR}		20 15	ns ns
31	External Clock Fall Time @12 MHz @16 MHz	t_{CLKF}		20 15	ns ns

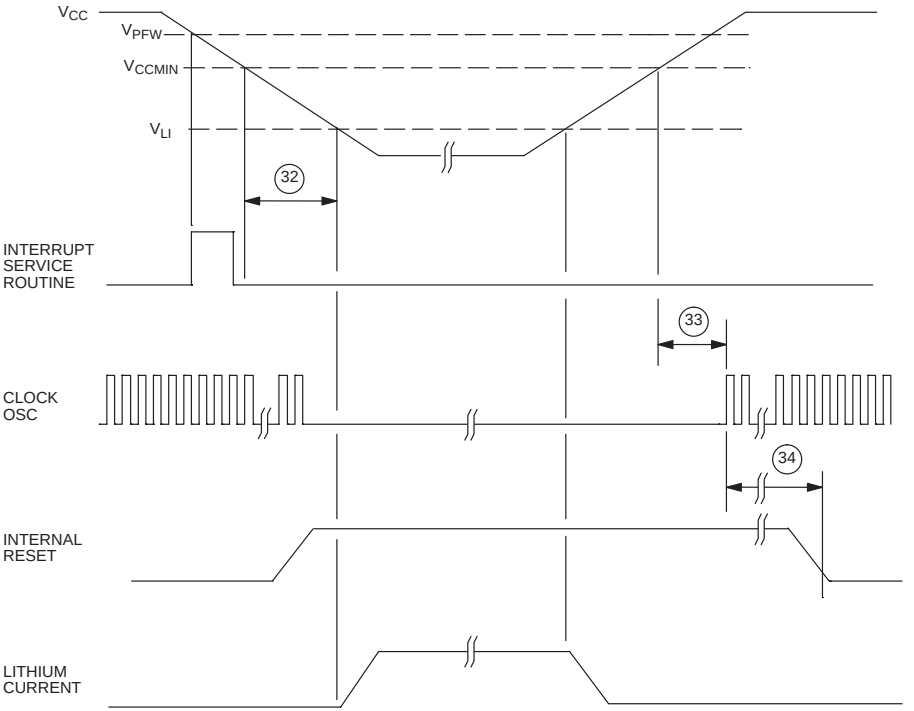
EXTERNAL CLOCK TIMING



AC CHARACTERISTICS (cont'd)
POWER CYCLING TIMING (t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
32	Slew Rate from V_{CCMIN} to 3.3V	t_F	130		µs
33	Crystal Start–up Time	t_{CSU}		(note 8)	
34	Power–On Reset Delay	t_{POR}		21504	t_{CLK}

POWER CYCLE TIMING



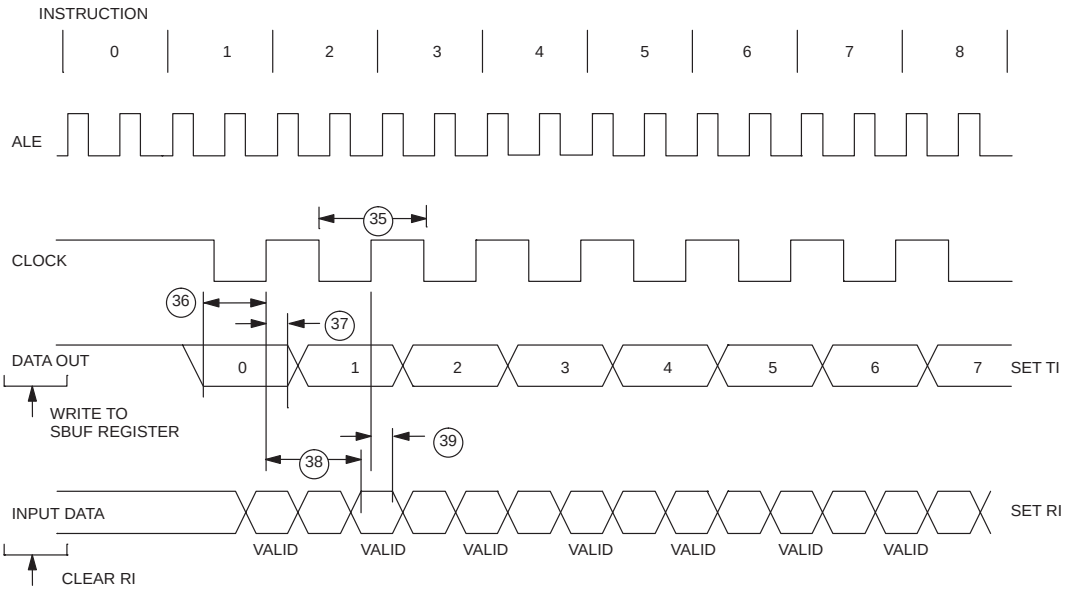
AC CHARACTERISTICS (cont'd)

SERIAL PORT TIMING – MODE 0

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
35	Serial Port Clock Cycle Time	t_{SPCLK}	$12t_{CLK}$		µs
36	Output Data Setup to Rising Clock Edge	t_{DOCH}	$10t_{CLK}$–133		ns
37	Output Data Hold after Rising Clock Edge	t_{CHDO}	$2t_{CLK}$–117		ns
38	Clock Rising Edge to Input Data Valid	t_{CHDV}		$10t_{CLK}$–133	ns
39	Input Data Hold after Rising Clock Edge	t_{CHDIV}	0		ns

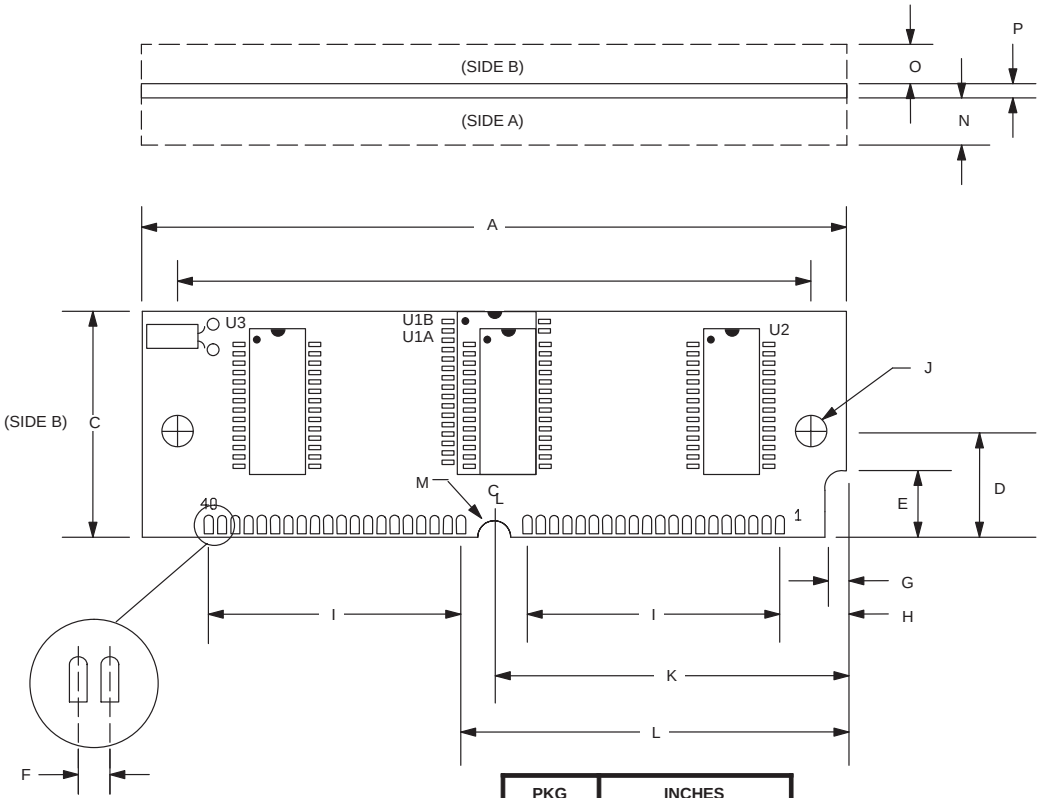
SERIAL PORT TIMING – MODE 0



NOTES:

1. All voltage referenced to ground.
2. SDI should be taken to a logic high when V_{CC}=+5V, and to approximately 3V when V_{CC}<3V.
3. SDI is deglitched to prevent accidental destruction. The pulse must be longer than t_{SPR} to pass the deglitcher, but SDI is not guaranteed unless it is longer than t_{SPA}.
4. Maximum operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF}=10 ns, V_{IL} = 0.5V; XTAL2 disconnected; RST = PORT0 = V_{CC}.
5. Idle mode I_{IDLE} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF} = 10 ns, V_{IL} = 0.5V; XTAL2 disconnected; PORT0 = V_{CC}, RST = V_{SS}.
6. Stop mode I_{STOP} is measured with all output pins disconnected; PORT0 = V_{CC}; XTAL2 not connected; RST = XTAL1 = V_{SS}.
7. Pin capacitance is measured with a test frequency – 1 MHz, t_A = 25°C.
8. Crystal start–up time is the time required to get the mass of the crystal into vibrational motion from the time that power is first applied to the circuit until the first clock pulse is produced by the on–chip oscillator. The user should check with the crystal vendor for a worst case specification on this time.

PACKAGE DRAWING



PKG	INCHES	
DIM	MIN	MAX
A	2.645	2.655
B	2.379	2.389
C	0.995	1.005
D	0.395	0.405
E	0.245	0.255
F	0.050 BSC	
G	0.075	0.085
H	0.245	0.255
I	0.950 BSC	
J	0.120	0.130
K	1.320	1.330
L	1.445	1.455
M	0.057	0.067
N	–	0.300
O	–	0.165
P	0.047	0.054

DATA SHEET REVISION SUMMARY

The following represent the key differences between 12/13/95 and 08/16/96 version of the DS2252T data sheet. Please review this summary carefully.

1. Change V_{CC} slew rate specification to reference 3.3V instead of V_{LI}.
2. Add minimum value to PCB thickness.

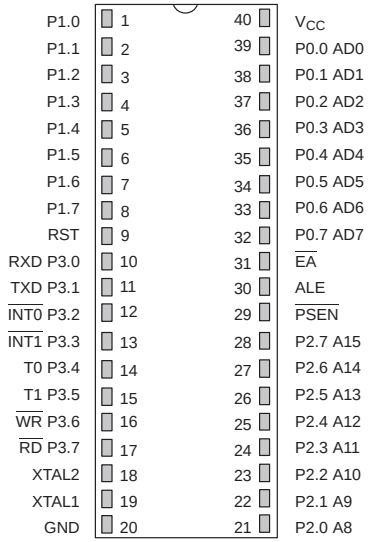
DALLAS SEMICONDUCTOR

DS5000(T)
Soft Microcontroller Module

FEATURES

- 8–bit 8051 compatible Microcontroller adapts to task–at–hand:
  - 8 or 32K bytes of nonvolatile RAM for program and/or data memory storage
  - Initial downloading of software in end system via on–chip serial port
  - Capable of modifying its own program and/or data memory in end use
- Crashproof operation:
  - Maintains all nonvolatile resources for 10 years in the absence of V_{CC}
  - Power–fail reset
  - Early warning power–fail interrupt
  - Watchdog timer
- Software Security Feature:
  - Executes encrypted software to prevent unauthorized disclosure
- On–chip, full–duplex serial I/O ports
- Two on–chip timer/event counters
- 32 parallel I/O lines
- Compatible with industry standard 8051 instruction set and pinout
- Optional Permanently Powered Real–Time Clock (DS5000T)

PIN ASSIGNMENT



40–PIN ENCAPSULATED PACKAGE

DESCRIPTION

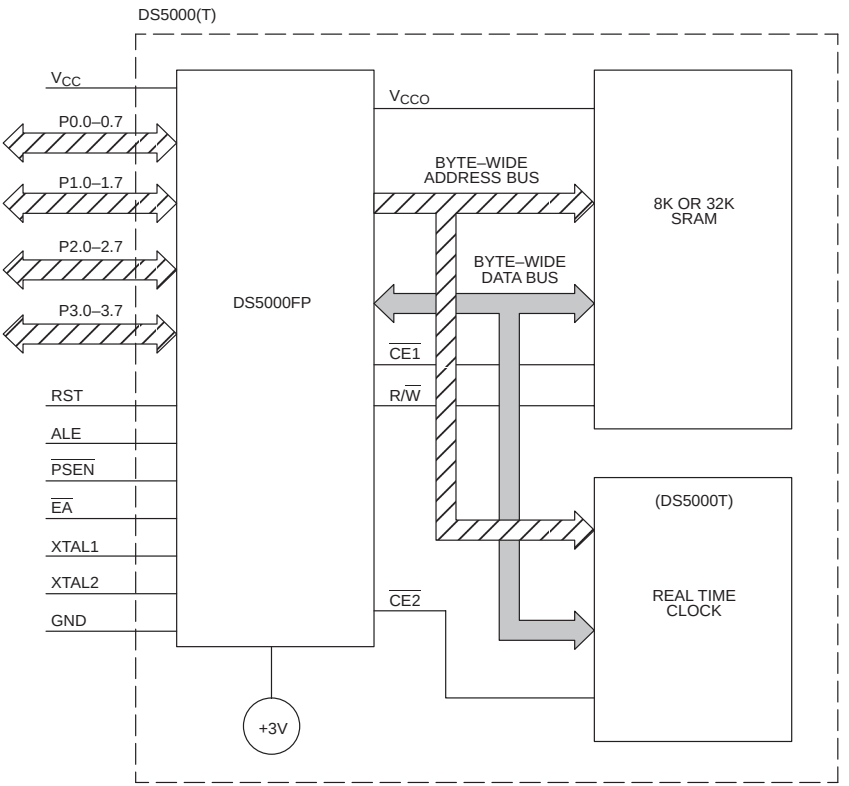
The DS5000(T) Soft Microcontroller Module is a fully 8051 compatible 8–bit CMOS microcontroller that offers “softness” in all aspects of its application. This is accomplished through the comprehensive use of nonvolatile technology to preserve all information in the absence of system V_{CC}. The internal program/data memory space is implemented using either 8K or 32K bytes of nonvolatile CMOS SRAM. Furthermore, internal data registers and key configuration registers are also nonvolatile. An optional real time clock gives permanently powered timekeeping. The clock keeps time to a hundredth of a second using an on–board crystal.

ORDERING INFORMATION

PART NUMBER	RAM SIZE	MAX CRYSTAL SPEED	TIMEKEEPING?
DS5000–8–16	8K bytes	16 MHz	No
DS5000–32–16	32K bytes	16 MHz	No
DS5000–8–16	8K bytes	16 MHz	Yes
DS5000T–32–16	32K bytes	16 MHz	Yes

Operating information is contained in the User's Guide section of the Secure Microcontroller Data Book. This data sheet provides ordering information, pinout, and electrical specification.

DS5000(T) BLOCK DIAGRAM Figure 1



PIN DESCRIPTION

PIN NUMBER	DESCRIPTION
1–8	**P1.0 – P1.7.** General purpose I/O Port 1.
9	**RST –** Active high reset input. A logic 1 applied to this pin will activate a reset state. This pin is pulled down internally so this pin can be left unconnected if not used.
10	**P3.0 RXD.** General purpose I/O port pin 3.0. Also serves as the receive signal for the on board UART. This pin should not be connected directly to a PC COM port.
11	**P3.1 TXD.** General purpose I/O port pin 3.1. Also serves as the transmit signal for the on board UART. This pin should not be connected directly to a PC COM port.
12	**P3.2 $\overline{\text{INT0}}$.** General purpose I/O port pin 3.2. Also serves as the active low External Interrupt 0.
13	**P3.3 $\overline{\text{INT1}}$.** General purpose I/O port pin 3.3. Also serves as the active low External Interrupt 1.
14	**P3.4 T0.** General purpose I/O port pin 3.4. Also serves as the Timer 0 input.
15	**P3.5 T1.** General purpose I/O port pin 3.5. Also serves as the Timer 1 input.
16	**P3.6 $\overline{\text{WR}}$.** General purpose I/O port pin. Also serves as the write strobe for Expanded bus operation.
17	**P3.7 $\overline{\text{RD}}$.** General purpose I/O port pin. Also serves as the read strobe for Expanded bus operation.
18, 19	**XTAL2, XTAL1.** Used to connect an external crystal to the internal oscillator. XTAL1 is the input to an inverting amplifier and XTAL2 is the output.
20	**GND.** Logic ground.
21–28	**P2.0–P2.7.** General purpose I/O Port 2. Also serves as the MSB of the Expanded Address bus.
29	**$\overline{\text{PSEN}}$ –** Program Store Enable. This active low signal is used to enable an external program memory when using the Expanded bus. It is normally an output and should be unconnected if not used. $\overline{\text{PSEN}}$ also is used to invoke the Bootstrap Loader. At this time, $\overline{\text{PSEN}}$ will be pulled down externally. This should only be done once the DS5000(T) is already in a reset state. The device that pulls down should be open drain since it must not interfere with $\overline{\text{PSEN}}$ under normal operation.
30	**ALE –** Address Latch Enable. Used to de–multiplex the multiplexed Expanded Address/Data bus on Port 0. This pin is normally connected to the clock input on a '373 type transparent latch. When using a parallel programmer, this pin also assumes the $\overline{\text{PROG}}$ function for programming pulses.
31	**$\overline{\text{EA}}$ –** External Access. This pin forces the DS5000(T) to behave like an 8031. No internal memory (or clock) will be available when this pin is at a logic low. Since this pin is pulled down internally, it should be connected to +5V to use NV RAM. In a parallel programmer, this pin also serves as V_{PP} for super voltage pulses.

PIN NUMBER	DESCRIPTION
32–39	**P0.7–P0.0.** General purpose I/O Port 0. This port is open–drain and can not drive a logic 1. It requires external pull–ups. Port 0 is also the multiplexed Expanded Address/Data bus. When used in this mode, it does not require pull–ups.
40	**V_{CC} – +5 volts.**

INSTRUCTION SET

The DS5000(T) executes an instruction set which is object code compatible with the industry standard 8051 microcontroller. As a result, software development packages which have been written for the 8051 are compatible with the DS5000(T), including cross–assemblers, high–level language compilers, and debugging tools.

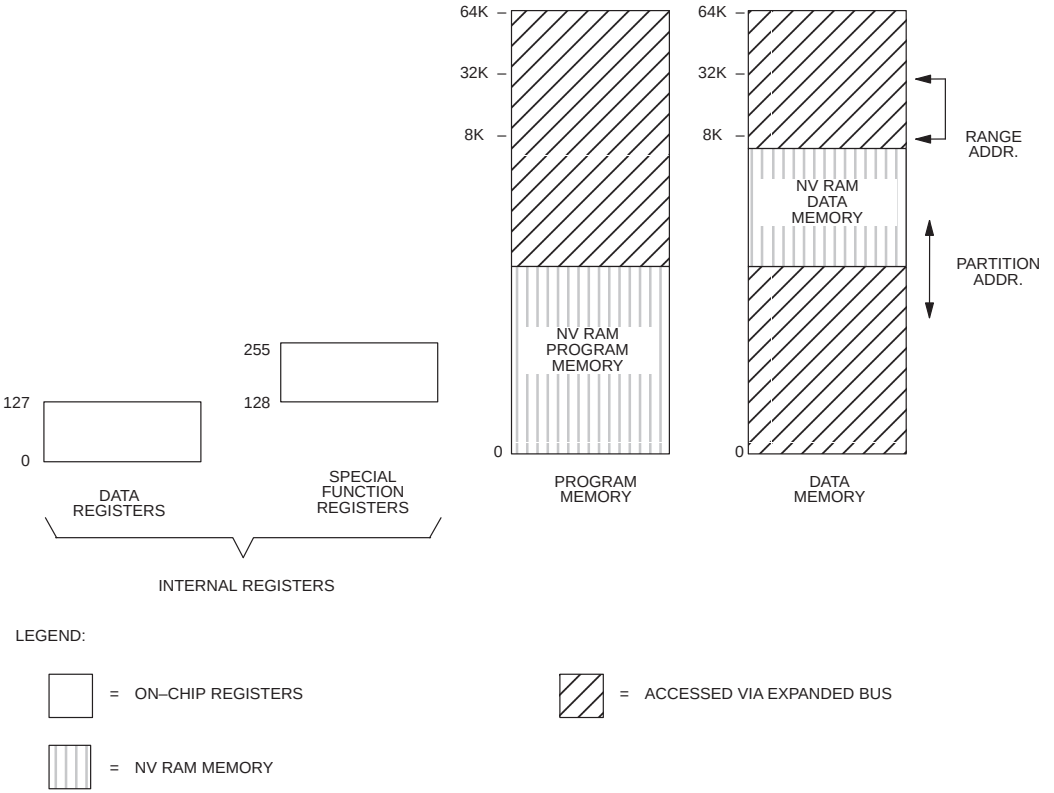
A complete description for the DS5000(T) instruction set is available in the User's Guide section of the Secure Microcontroller Data Book.

MEMORY ORGANIZATION

Figure 2 illustrates the address spaces which are accessed by the DS5000(T). As illustrated in the figure, separate address spaces exist for program and data memory. Since the basic addressing capability of the machine is 16 bits, a maximum of 64K bytes of program memory and 64K bytes of data memory can be accessed by the DS5000(T) CPU. The 8K or 32K byte RAM area inside of the DS5000(T) can be used to contain both program and data memory.

The Real time Clock (RTC) in the DS5000T is reached in the memory map by setting a SFR bit. The MCON.2 bit (ECE2) is used to select an alternate data memory map. While ECE2=1, all MOVXs will be routed to this alternate memory map. The real time clock is a serial device that resides in this area. A full description of the RTC access and example software is given in the User's Guide section of the Secure Microcontroller Data Book. If the ECE2 bit is set on a DS5000 without a timekeeper, the MOVXs will simply go to a nonexistent memory. Software execution would not be affected otherwise.

DS5000(T) LOGICAL ADDRESS SPACES Figure 2



PROGRAM LOADING

The Program Load Modes allow initialization of the NV RAM Program/Data Memory. This initialization may be performed in one of two ways:

1. Serial Program Loading which is capable of performing Bootstrap Loading of the DS5000(T). This feature allows the loading of the application program to be delayed until the DS5000(T) is installed in the end system. Dallas Semiconductor strongly recommends the use of serial program loading because of its versatility and ease of use.
2. Parallel Program Load cycles which perform the initial loading from parallel address/data information presented on the I/O port pins. This mode is timing–set compatible with the 8751H microcontroller programming mode.

The DS5000(T) is placed in its Program Load configuration by simultaneously applying a logic 1 to the RST pin and forcing the $\overline{\text{PSEN}}$ line to a logic 0 level. Immediately following this action, the DS5000(T) will look for a parallel Program Load pulse, or a serial ASCII carriage return (0DH) character received at 9600, 2400, 1200, or 300 bps over the serial port.

The hardware configurations used to select these modes of operation are illustrated in Figure 3.

PROGRAM LOADING CONFIGURATIONS Figure 3

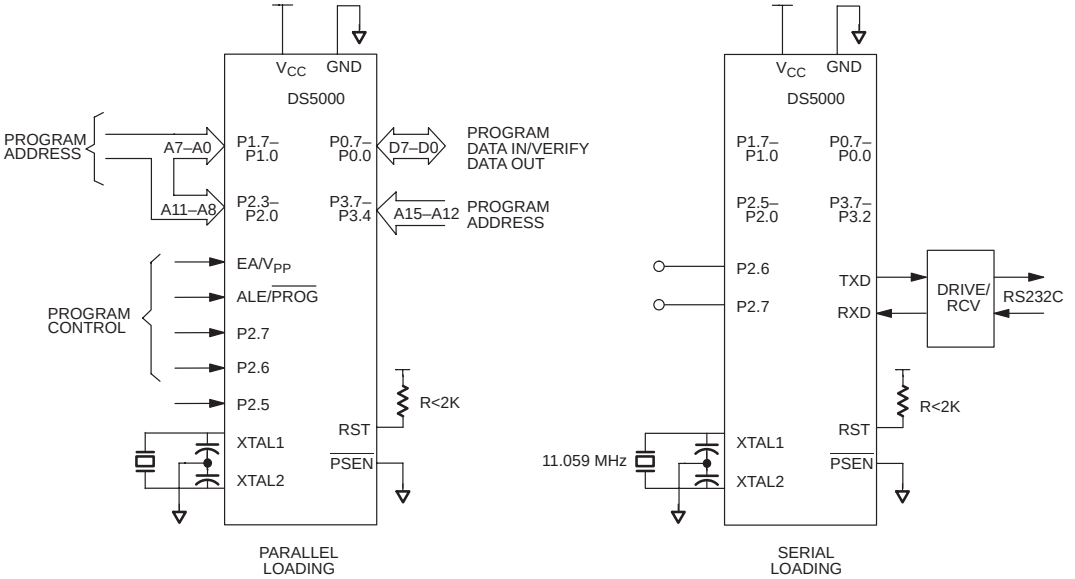


Table 1 summarizes the selection of the available Parallel Program Load cycles. The timing associated with these cycles is illustrated in the electrical specs.

SERIAL BOOTSTRAP LOADER

The Serial Program Load Mode is the easiest, fastest, most reliable, and most complete method of initially loading application software into the DS5000(T) nonvolatile RAM. Communication can be performed over a standard asynchronous serial communications port. A typical application would use a simple RS232C serial interface to program the DS5000(T) as a final production procedure. The hardware configuration which is required for the Serial Program Load mode is illustrated in Figure 3. Port pins 2.7 and 2.6 must be either open or pulled high to avoid placing the DS5000(T) in a parallel load cycle. Although an 11.0592 MHz crystal is shown in Figure 3, a variety of crystal frequencies and loader baud rates are supported, shown in Table 2. The serial loader is designed to operate across a three–wire interface from a standard UART. The receive, transmit, and ground wires are all that are necessary to establish communication with the DS5000(T).

The Serial Bootstrap Loader implements an easy–to–use command line interface which allows an application program in an Intel hex representation to be loaded into and read back from the device. Intel hex is the typical format which existing 8051 cross–assemblers output. The serial loader responds to single character commands which are summarized below:

COMMAND	FUNCTION
C	Return CRC–16 checksum of embedded RAM
D	Dump Intel Hex File
F	Fill embedded RAM block with constant
K	Load 40–bit Encryption Key
L	Load Intel Hex File
R	Read MCON register
T	Trace (Echo) incoming Intel Hex data
U	Clear Security Lock
V	Verify Embedded RAM with incoming Intel Hex
W	Write MCON register
Z	Set Security Lock
P	Put a value to a port
G	Get a value from a port

PARALLEL PROGRAM LOAD CYCLES Table 1

MODE	RST	$\overline{\text{PSEN}}$	$\overline{\text{PROG}}$	$\overline{\text{EA}}$	P2.7	P2.6	P2.5
Program	1	0	0	V_{PP}	1	0	X
Security Set	1	0	0	V_{PP}	1	1	X
Verify	1	X	X	1	0	0	X
Prog Expanded	1	0	0	V_{PP}	0	1	0
Verify Expanded	1	0	1	1	0	1	0
Prog MCON or Key registers	1	0	0	V_{PP}	0	1	1
Verify MCON registers	1	0	1	1	0	1	1

The Parallel Program Cycle is used to load a byte of data into a register or memory location within the DS5000(T). The Verify Cycle is used to read this byte back for comparison with the originally loaded value to verify proper load ing. The Security Set Cycle may be used to enable and the Software Security feature of the DS5000(T). One may also enter bytes for the MCON register or for the five encryption registers using the Program MCON cycle. When using this cycle, the absolute register address must be presented at Ports 1 and 2 as in the normal program cycle (Port 2 should be 00H). The MCON contents can likewise be verified using the Verify MCON cycle.

When the DS5000(T) first detects a Parallel Program Strobe pulse or a Security Set Strobe pulse while in the Program Load Mode following a Power–On Reset, the internal hardware of the DS5000(T) is initialized so that an existing 4K byte program can be programmed into a DS5000(T) with little or no modification. This initialization automatically sets the Range Address for 8K bytes and maps the lowest 4K byte bank of Embedded RAM as program memory. The next 4K bytes of Embedded RAM are mapped as Data Memory.

In order to program more than 4K bytes of program code, the Program/Verify Expanded cycles can be used. Up to 32K bytes of program code can be entered and verified. Note that the expanded 32K byte Program/Verify cycles take much longer than the normal 4K byte Program/Verify cycles.

A typical parallel loading session would follow this procedure. First, set the contents of the MCON register with the correct range and partition only if using expanded programming cycles. Next, the encryption registers can be loaded to enable encryption of the program/data memory (not required). Then, program the DS5000(T) using either normal or expanded program cycles and check the memory contents using Verify cycles. The last operation would be to turn on the security lock feature by either a Security Set cycle or by explicitly writing to the MCON register and setting MCON.0 to a 1.

SERIAL LOADER BAUD RATES FOR DIFFERENT CRYSTAL FREQUENCIES Table 2

CRYSTAL FREQ (MHz)	BAUD RATE					
	300	1200	2400	9600	19200	57600
14.7456		Y	Y	Y	Y	
11.0592	Y	Y	Y	Y	Y	Y
9.21600	Y	Y	Y	Y		
7.37280	Y	Y	Y	Y		
5.52960	Y	Y	Y	Y		
1.84320	Y	Y	Y	Y		

ADDITIONAL INFORMATION

A complete description for all operational aspects of the DS5000(T), is provided in the User's Guide section of the Secure Microcontroller Data Book.

DEVELOPMENT SUPPORT

Dallas Semiconductor offers a kit package for developing and testing user code. The DS5000TK Evaluation Kit allows the user to download Intel hex formatted code directly to the DS5000(T) from a PC–XT/AT or compatible computer. The kit consists of a DS5000T–32, an interface pod, demo software, and an RS232 connector that attaches to the COM1 or COM2 serial port of a PC. See the Development Tools section of the Secure Microcontroller Data Book for further details.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC CHARACTERISTICS

(t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

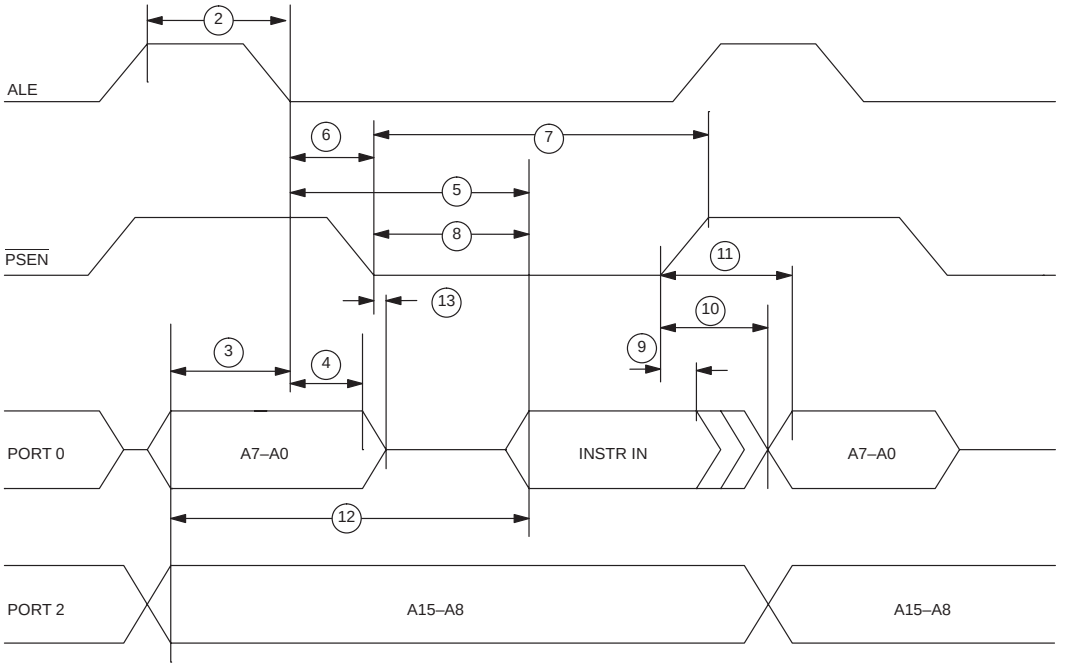
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Low Voltage	V_{IL}	–0.3		0.8	V	1
Input High Voltage	V_{IH1}	2.0		V_{CC} +0.3	V	1
Input High Voltage RST, XTAL1	V_{IH2}	3.5		V_{CC} +0.3	V	1
Output Low Voltage @ I_{OL}=1.6 mA (Ports 1, 2, 3)	V_{OL1}		0.15	0.45	V	
Output Low Voltage @ I_{OL}=3.2 mA (Ports 0, ALE, $\overline{PSEN}$)	V_{OL2}		0.15	0.45	V	1
Output High Voltage @ I_{OH}=–80 µA (Ports 1, 2, 3)	V_{OH1}	2.4	4.8		V	1
Output High Voltage @ I_{OH}=–400 µA (Ports 0, ALE, $\overline{PSEN}$)	V_{OH2}	2.4	4.8		V	1
Input Low Current V_{IN} = 0.45V (Ports 1, 2, 3)	I_{IL}			–50	µA	
Transition Current; 1 to 0 V_{IN} = 2.0V (Ports 1, 2, 3)	I_{TL}			–500	µA	
Input Leakage Current 0.45 < V_{IN} < V_{CC} (Port 0)	I_L			±10	µA	
RST, $\overline{EA}$ Pulldown Resistor	R_{RE}	40		125	KΩ	
Stop Mode Current	I_{SM}			80	µA	4
Power–Fail Warning Voltage	V_{PFW}	4.15	4.6	4.75	V	1
Minimum Operating Voltage	V_{CCmin}	4.05	4.5	4.65	V	1
Programming Supply Voltage (Parallel Program Mode)	V_{PP}	12.5		13	V	1
Program Supply Current	I_{PP}		15	20	mA	
Operating Current DS5000–8K@8 MHz DS5000–32K @ 12 MHz DS5000T–32–16 @ 16 MHz	I_{CC}		25.2 35.7 45.6	43 48 54	mA	2
Idle Mode Current @ 12 MHz	I_{CC}		4.5	6.2	mA	3

AC CHARACTERISTICS
EXPANDED BUS MODE TIMING SPECIFICATIONS

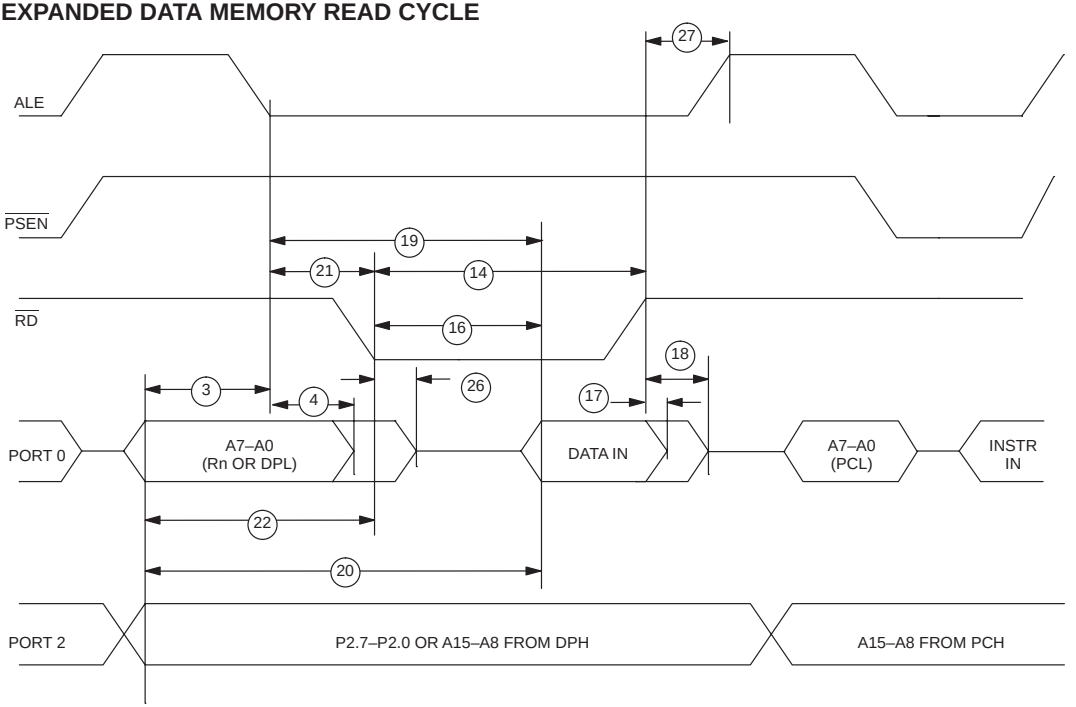
(t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
1	Oscillator Frequency	$1/t_{CLK}$	1.0	16	MHz
2	ALE Pulse Width	t_{ALPW}	$2t_{CLK}$ –40		ns
3	Address Valid to ALE Low	t_{AVALL}	t_{CLK} –40		ns
4	Address Hold After ALE Low	t_{AVAAV}	t_{CLK} –35		ns
5	ALE Low to Valid Instr. In @12 MHz @16 MHz	t_{ALLVI}		$4t_{CLK}$ –150 $4t_{CLK}$ –90	ns ns
6	ALE Low to $\overline{PSEN}$ Low	t_{ALLPSL}	t_{CLK} –25		ns
7	$\overline{PSEN}$ Pulse Width	t_{PSPW}	$3t_{CLK}$ –35		ns
8	$\overline{PSEN}$ Low to Valid Instr. In @12 MHz @16 MHz	t_{PSLVI}		$3t_{CLK}$ –150 $3t_{CLK}$ –90	ns ns
9	Input Instr. Hold after $\overline{PSEN}$ Going High	t_{PSIV}	0		ns
10	Input Instr. Float after $\overline{PSEN}$ Going High	t_{PSIX}		t_{CLK} –20	ns
11	Address Hold after $\overline{PSEN}$ Going High	t_{PSAV}	t_{CLK} –8		ns
12	Address Valid to Valid Instr. In @12 MHz @16 MHz	t_{AVVI}		$5t_{CLK}$ –150 $5t_{CLK}$ –90	ns ns
13	$\overline{PSEN}$ Low to Address Float	t_{PSLAZ}	0		ns
14	$\overline{RD}$ Pulse Width	t_{RDPW}	$6t_{CLK}$ –100		ns
15	$\overline{WR}$ Pulse Width	t_{WRPW}	$6t_{CLK}$ –100		ns
16	$\overline{RD}$ Low to Valid Data In @12 MHz @16 MHz	t_{RDLDV}		$5t_{CLK}$ –165 $5t_{CLK}$ –105	ns ns
17	Data Hold after $\overline{RD}$ High	t_{RDHDV}	0		ns
18	Data Float after $\overline{RD}$ High	t_{RDHDZ}		$2t_{CLK}$ –70	ns
19	ALE Low to Valid Data In @12 MHz @16 MHz	t_{ALLVD}		8_{CLK} –150 $8t_{CLK}$ –90	ns ns
20	Valid Addr. to Valid Data In @12 MHz @16 MHz	t_{AVDV}		$9t_{CLK}$ –165 $9t_{CLK}$ –105	ns ns
21	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{ALLRDL}	$3t_{CLK}$ –50	$3t_{CLK}$ +50	ns
22	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVRDL}	$4t_{CLK}$ –130		ns
23	Data Valid to $\overline{WR}$ Going Low	t_{DVWRL}	t_{CLK} –60		ns
24	Data Valid to $\overline{WR}$ High @12 MHz @16 MHz	t_{DVWRH}	$7t_{CLK}$ –150 $7t_{CLK}$ –90		ns ns
25	Data Valid after $\overline{WR}$ High	t_{WRHDV}	t_{CLK} –50		ns
26	$\overline{RD}$ Low to Address Float	t_{RDLAZ}		0	ns
27	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{RDHALH}	t_{CLK} –40	t_{CLK} +50	ns

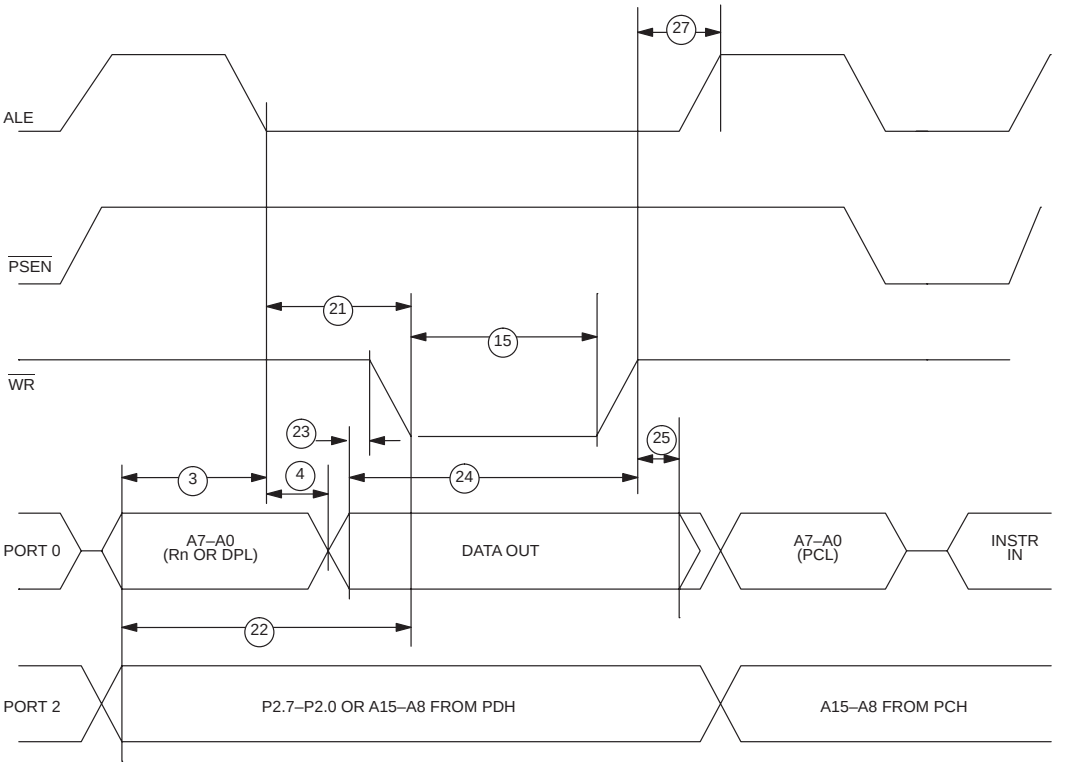
EXPANDED PROGRAM MEMORY READ CYCLE



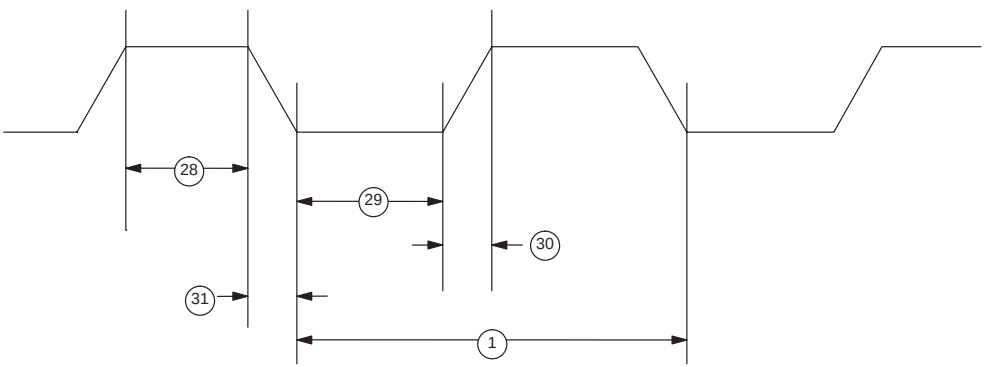
EXPANDED DATA MEMORY READ CYCLE



EXPANDED DATA MEMORY WRITE CYCLE



EXTERNAL CLOCK TIMING



AC CHARACTERISTICS (cont'd)
EXTERNAL CLOCK DRIVE

(t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

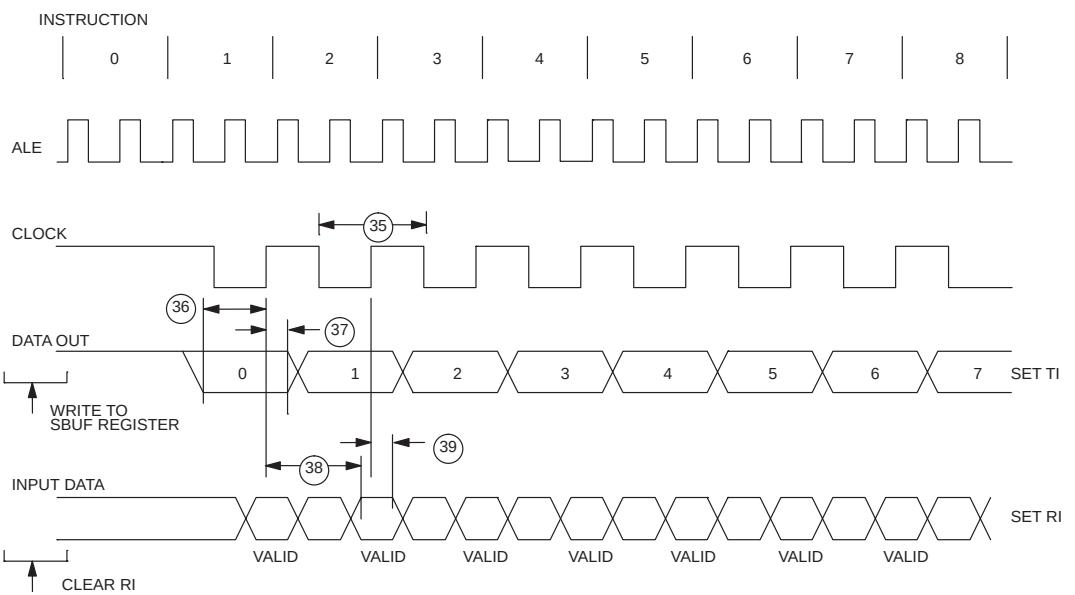
#	PARAMETER		SYMBOL	MIN	MAX	UNITS
28	External Clock High Time	@12 MHz @16 MHz	t_{CLKHPW}	20 15		ns ns
29	External Clock Low Time	@12 MHz @16 MHz	t_{CLKLPW}	20 15		ns ns
30	External Clock Rise Time	@12 MHz @16 MHz	t_{CLKR}		20 15	ns ns
31	External Clock Fall Time	@12 MHz @16 MHz	t_{CLKF}		20 15	ns ns

AC CHARACTERISTICS (cont'd)
SERIAL PORT TIMING – MODE 0

(t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
35	Serial Port Cycle Time	t_{SPCLK}	$12t_{CLK}$		µs
36	Output Data Setup to Rising Clock Edge	t_{DOCH}	$10t_{CLK}$ –133		ns
37	Output Data Hold after Rising Clock Edge	t_{CHDO}	$2t_{CLK}$ –117		ns
38	Clock Rising Edge to Input Data Valid	t_{CHDV}		$10t_{CLK}$ –133	ns
39	Input Data Hold after Rising Clock Edge	t_{CHDIV}	0		ns

SERIAL PORT TIMING – MODE 0

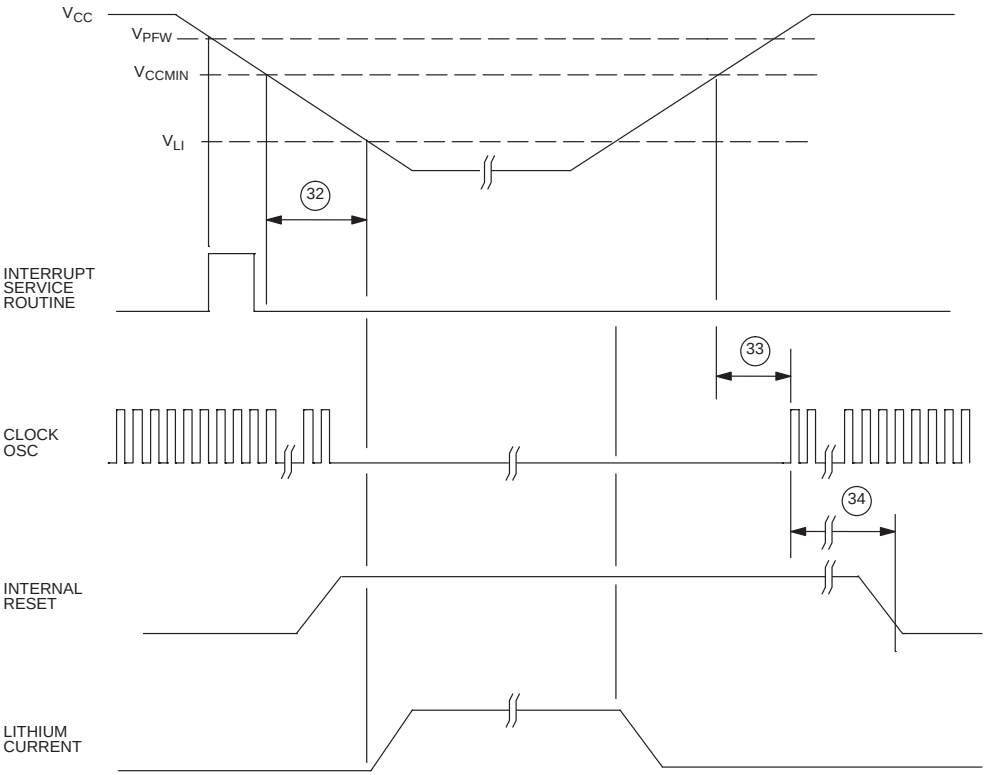


AC CHARACTERISTICS (cont'd)
POWER CYCLING TIMING

(t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
32	Slew Rate from V_{CCmin} to 3.3V	t_F	40		µs
33	Crystal Start up Time	t_{CSU}		(note 5)	
34	Power–On Reset Delay	t_{POR}		21504	t_{CLK}

POWER CYCLE TIMING

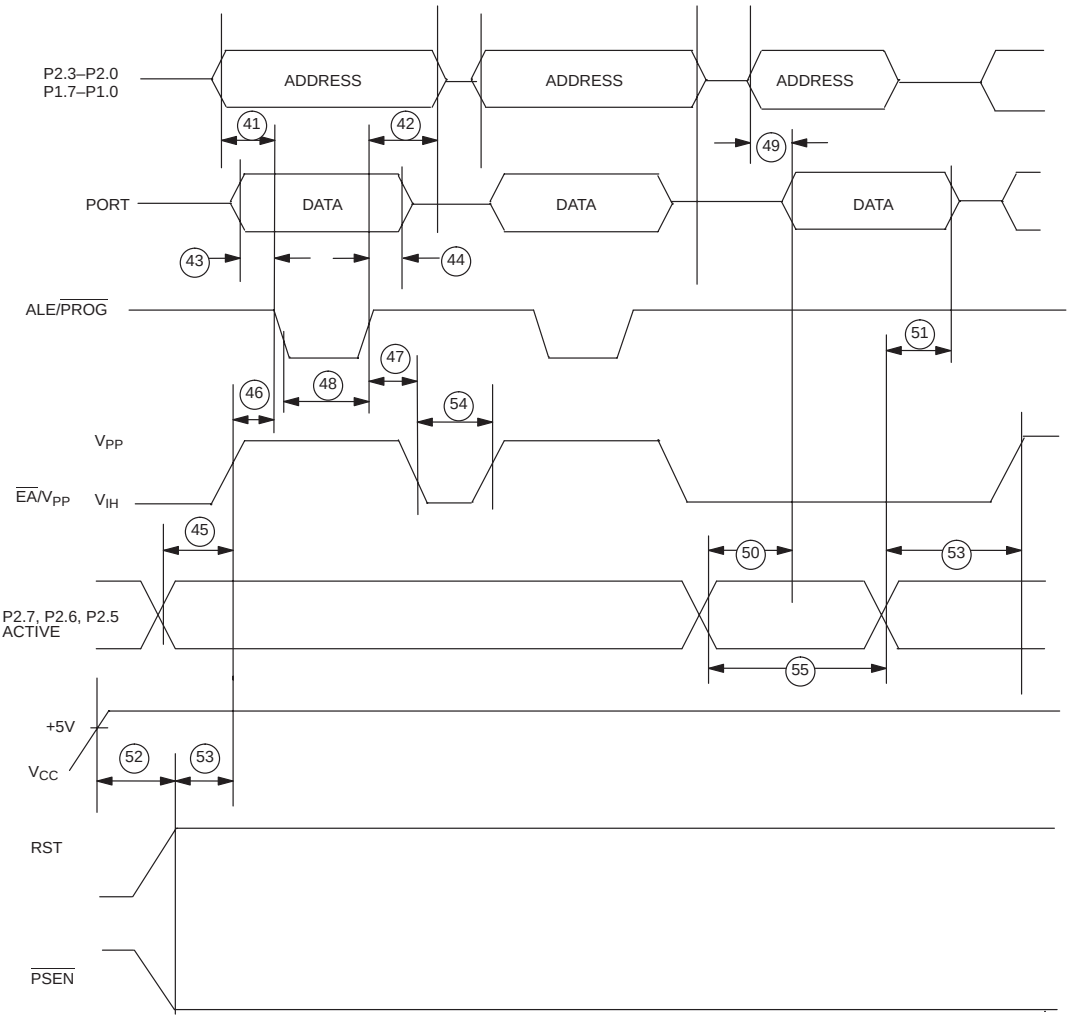


AC CHARACTERISTICS (cont'd)
PARALLEL PROGRAM LOAD TIMING (t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
40	Oscillator Frequency	$1/t_{CLK}$	1.0	12.0	MHz
41	Address Setup to $\overline{PROG}$ Low	t_{AVPRL}	0		
42	Address Hold after $\overline{PROG}$ High	t_{PRHAV}	0		
43	Data Setup to $\overline{PROG}$ Low	t_{DVPRL}	0		
44	Data Hold after $\overline{PROG}$ High	t_{PRHDV}	0		
45	P2.7, 2.6, 2.5 Setup to V_{PP}	t_{P27HVP}	0		
46	V_{PP} Setup to $\overline{PROG}$ Low	t_{VPHPRL}	0		
47	V_{PP} Hold after $\overline{PROG}$ Low	t_{PRHVPL}	0		
48	$\overline{PROG}$ Width Low	t_{PRW}	2400		t_{CLK}
49	Data Output from Address Valid	t_{AVDV}		48 1800*	t_{CLK}
50	Data Output from P2.7 Low	t_{DVP27L}		48 1800*	t_{CLK}
51	Data Float after P2.7 High	t_{P27HDZ}	0	48 1800*	t_{CLK}
52	Delay to Reset/$\overline{PSEN}$ Active after Power–On	t_{PORPV}	21504		t_{CLK}
53	Reset/$\overline{PSEN}$ Active (or Verify Inactive) to V_{PP} High	t_{RAVPH}	1200		t_{CLK}
54	V_{PP} Inactive (Between Program Cycles)	t_{VPPPC}	1200		t_{CLK}
55	Verify Active Time	t_{VFT}	48 2400*		t_{CLK}

* Second set of numbers refers to expanded memory programming up to 32K bytes.

PARALLEL PROGRAM LOAD TIMING

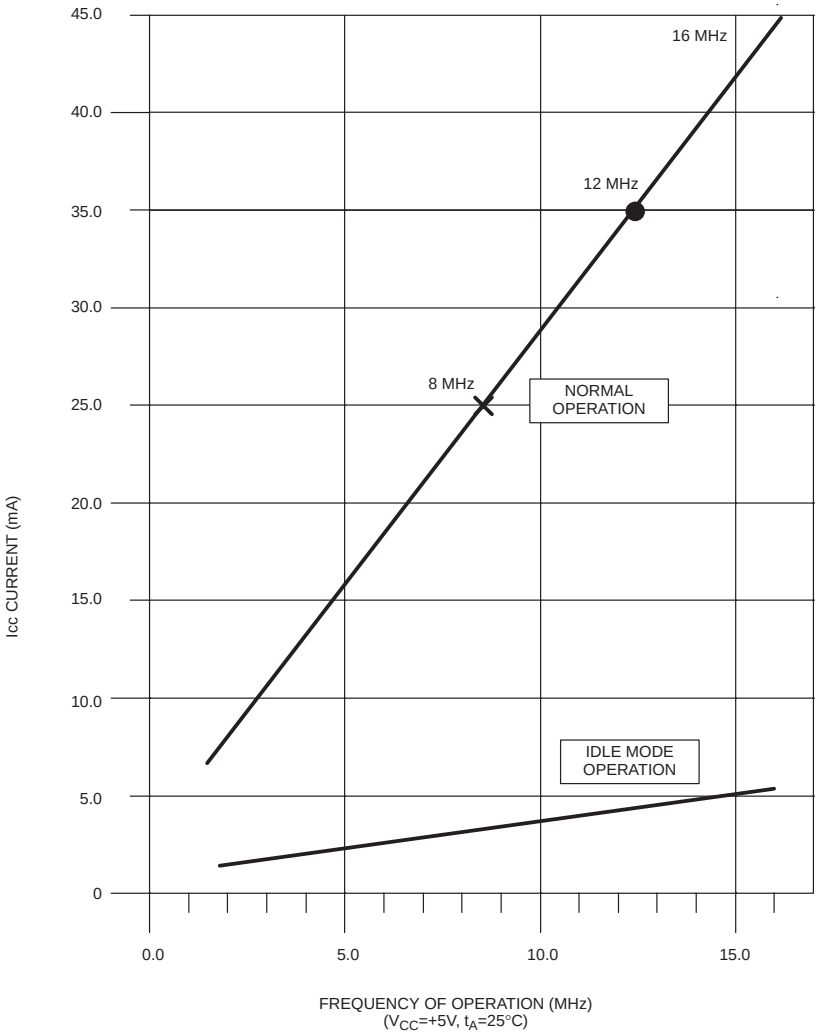


CAPACITANCE

(test frequency = 1 MHz; t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Capacitance	C_O			10	pF	
Input Capacitance	C_I			10	pF	

DS5000(T) TYPICAL I_{CC} VS. FREQUENCY



Normal operation is measured using:

1) External crystals on XTAL1 and 2
2) All port pins disconnected
3) RST=0 volts and EA=V_{CC}
4) Part performing endless loop writing to internal memory.

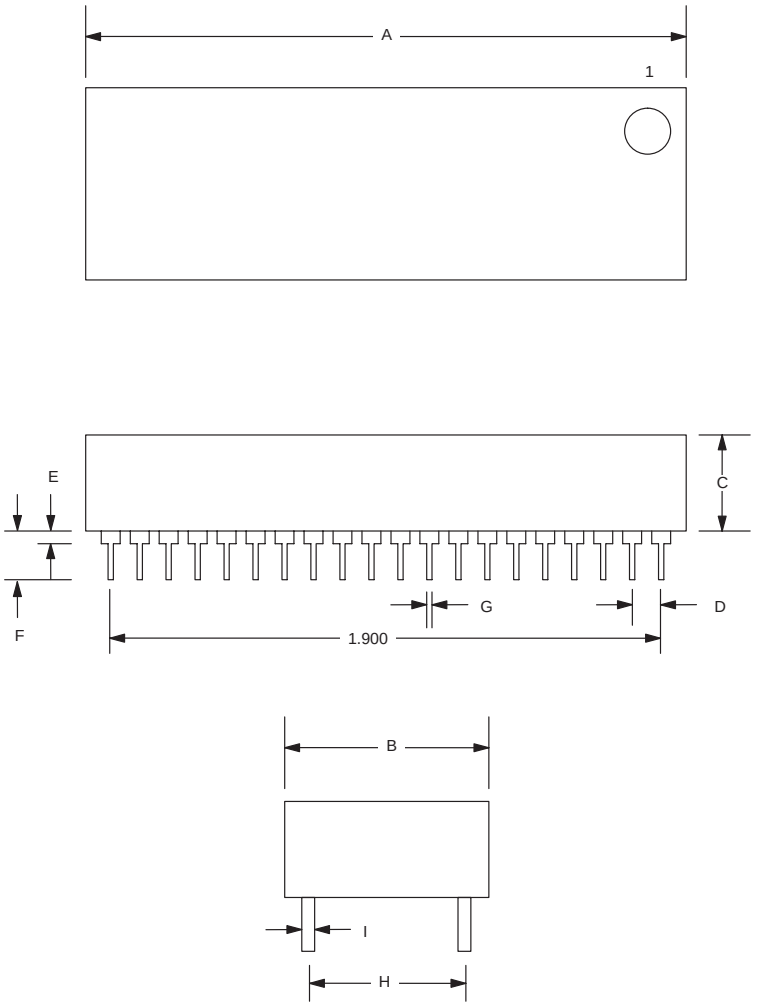
Idle mode operation is measured using:

1) External clock source at XTAL1; XTAL2 floating
2) All port pins disconnected
3) RST=0 volts and EA=V_{CC}
4) Part set in IDLE mode by software.

NOTES:

1. All voltages are referenced to ground.
2. Maximum operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF}=10 ns, V_{IL} = 0.5V; XTAL2 disconnected; $\overline{EA}$ = RST = PORT0 = V_{CC}.
3. Idle mode I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF} = 10 ns, V_{IL} = 0.5V; XTAL2 disconnected; $\overline{EA}$ = PORT0 = V_{CC}, RST = V_{SS}.
4. Stop mode I_{CC} is measured with all output pins disconnected; $\overline{EA}$ = PORT0 = V_{CC}; XTAL2 not connected; RST = V_{SS}.
5. Crystal start–up time is the time required to get the mass of the crystal into vibrational motion from the time that power is first applied to the circuit until the first clock pulse is produced by the on–chip oscillator. The user should check with the crystal vendor for the worst case spec on this time.

PACKAGE DRAWING



DIM	INCHES	
	MIN	MAX
A IN.	2.080	2.100
B IN.	0.680	0.700
C IN.	0.290	0.325
D IN.	0.090	0.110
E IN.	0.030	0.060
F IN.	0.145	0.185
G IN.	0.016	0.020
H IN.	0.590	0.610
I IN.	0.009	0.015

DATA SHEET REVISION SUMMARY

The following represent the key differences between the dates 07/20/95 to 07/24/96 of the DS5000(T) data sheet. Please review this summary carefully.

1. Correct Figure 3 to show RST active high.
2. Add Data Sheet Revision Summary.

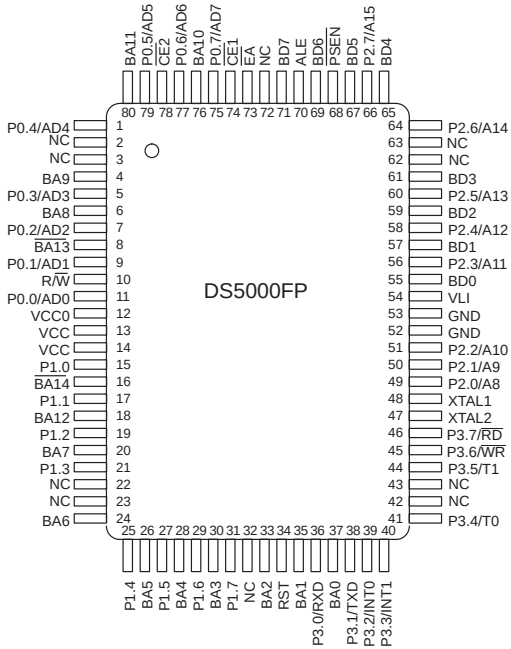
DALLAS SEMICONDUCTOR

DS5000FP
Soft Microprocessor Chip

FEATURES

- 8051 compatible microprocessor adapts to its task
  - Accesses between 8K and 64K bytes of nonvolatile SRAM
  - In–system programming via on–chip serial port
  - Can modify its own program or data memory
  - Accesses memory on a separate Byte–wide bus
- Crashproof Operation
  - Maintains all nonvolatile resources for over 10 years
  - Power–fail Reset
  - Early Warning Power–fail Interrupt
  - Watchdog Timer
  - User supplied Lithium battery backs user SRAM for program/data storage
- Software Security
  - Executes encrypted programs to prevent observation
  - Security Lock prevents download
  - Unlocking destroys contents
- Fully 8051 Compatible
  - 128 bytes scratchpad RAM
  - Two timer/counters
  - On–chip serial port
  - 32 parallel I/O port pins

PIN ASSIGNMENT



DESCRIPTION

The DS5000FP is an 8051 compatible processor based on nonvolatile RAM technology. It is substantially more flexible than a standard 8051, yet provides full compatibility with the 8051 instruction set, timers, serial port, and parallel I/O ports. By using NV RAM instead of ROM, the user can program, then reprogram the microcontroller while in–system. The application software can even change its own operation. This allows frequent software upgrades, adaptive programs, customized systems, etc. In addition, by using NV SRAM, the DS5000FP is ideal for data logging applications. It connects easily to a Dallas Real Time Clock for time stamp and date.

The DS5000FP provides the benefits of NV RAM without using I/O resources. It uses a non–multiplexed Byte–wide address and data bus for memory access. This bus can perform all memory access and provides decoded chip enables for SRAM. This leaves the 32 I/O port pins free for application use. The DS5000FP uses ordinary SRAM and battery backs the memory contents with a user's external lithium cell. Data is maintained for

over 10 years with a very small lithium cell. A DS5000FP also provides crashproof operation in portable systems or systems with unreliable power. These features include the ability to save the operating state, Power–fail Reset, Power–fail Interrupt, and Watchdog Timer.

A user loads programs into the DS5000FP via its on–chip Serial Bootstrap Loader. This function supervises the loading of code into NV RAM, validates it, then becomes transparent to the user. Software can be stored in an 8K byte or 32K byte CMOS SRAM. Using its internal Partitioning, the DS5000FP will divide this common RAM into user programmable code and data segments. This Partition can be selected at program loading time, but can be modified anytime later. It will decode memory access to the SRAM, communicate via its Byte–wide bus and write–protect the memory portion designated as ROM. Combining program and data storage in one device saves board space and cost. The DS5000FP can also access a second 32K bytes of NV RAM but this area is restricted to data memory. For a user that wants a pre–constructed module using the DS5000FP, RAM, lithium cell, and optional real time clock; the DS2250(T) and DS5000(T) are available and described in separate data sheets. More details are also contained in the User's Guide section of the Secure Microcontroller Data Book.

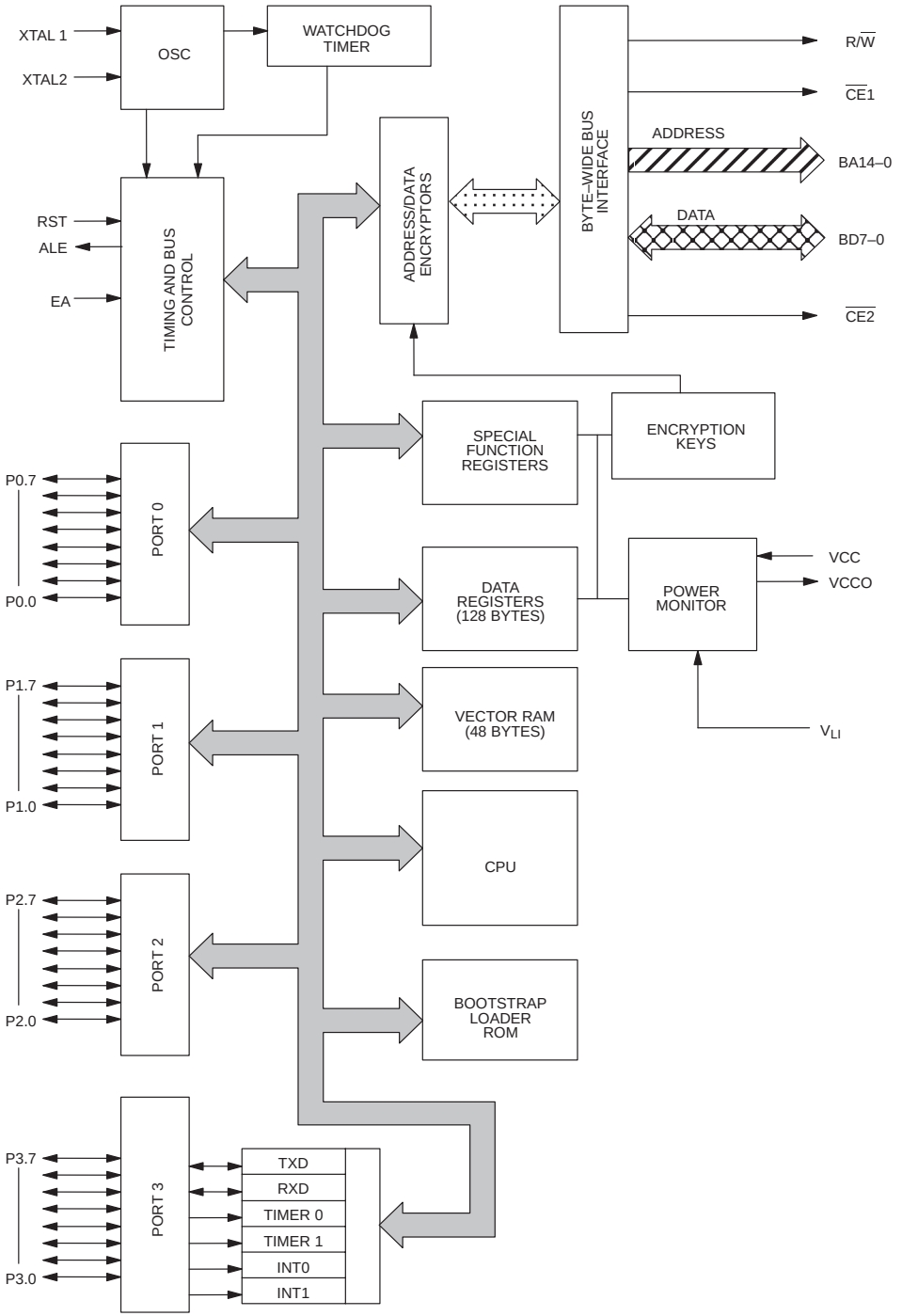
ORDERING INFORMATION

The following devices are available as standard products from Dallas Semiconductor:

PART #	DESCRIPTION
DS5000FP–16	80–pin QFP, Max. clock speed 16 MHz, 0° to 70°C operation

Operating information is contained in the User's Guide section of the Secure Microcontroller Data Book. This data sheet provides ordering information, pin–out, and electrical specifications.

DS5000FP BLOCK DIAGRAM Figure 1



PIN DESCRIPTION

PIN NUMBER	DESCRIPTION
15, 17, 19, 21, 25, 27, 29, 31	**P1.0 – P1.7.** General purpose I/O Port 1.
34	**RST –** Active high reset input. A logic 1 applied to this pin will activate a reset state. This pin is pulled down internally so this pin can be left unconnected if not used.
36	**P3.0 RXD.** General purpose I/O port pin 3.0. Also serves as the receive signal for the on board UART. This pin should not be connected directly to a PC COM port.
38	**P3.1 TXD.** General purpose I/O port pin 3.1. Also serves as the transmit signal for the on board UART. This pin should not be connected directly to a PC COM port.
39	**P3.2 $\overline{\text{INT0}}$.** General purpose I/O port pin 3.2. Also serves as the active low External Interrupt 0.
40	**P3.3 $\overline{\text{INT1}}$.** General purpose I/O port pin 3.3. Also serves as the active low External Interrupt 1.
41	**P3.4 T0.** General purpose I/O port pin 3.4. Also serves as the Timer 0 input.
44	**P3.5 T1.** General purpose I/O port pin 3.5. Also serves as the Timer 1 input.
45	**P3.6 $\overline{\text{WR}}$.** General purpose I/O port pin. Also serves as the write strobe for Expanded bus operation.
46	**P3.7 $\overline{\text{RD}}$.** General purpose I/O port pin. Also serves as the read strobe for Expanded bus operation.
47, 48	**XTAL2, XTAL1.** Used to connect an external crystal to the internal oscillator. XTAL1 is the input to an inverting amplifier and XTAL2 is the output.
52, 53	**GND.** Logic ground.
49, 50, 51, 56, 58, 60, 64, 66	**P2.0–P2.7.** General purpose I/O Port 2. Also serves as the MSB of the Expanded Address bus.
68	**$\overline{\text{PSEN}}$ –** Program Store Enable. This active low signal is used to enable an external program memory when using the Expanded bus. It is normally an output and should be unconnected if not used. $\overline{\text{PSEN}}$ is also used to invoke the Bootstrap Loader. At this time, $\overline{\text{PSEN}}$ will be pulled down externally. This should only be done once the DS5000FP is already in a reset state. The device that pulls down should be open drain since it must not interfere with $\overline{\text{PSEN}}$ under normal operation.
70	**ALE –** Address Latch Enable. Used to de–multiplex the multiplexed Expanded Address/Data bus on Port 0. This pin is normally connected to the clock input on a '373 type transparent latch. When using a parallel programmer, this pin also assumes the $\overline{\text{PROG}}$ function for programming pulses.
73	**$\overline{\text{EA}}$ –** External Access. This pin forces the DS5000FP to behave like an 8031. No internal memory (or clock) will be available when this pin is at a logic low. Since this pin is pulled down internally, it should be connected to +5V to use NV RAM. In a parallel programmer, this pin also serves as V_{PP} for super voltage pulses.
11, 9, 7, 5, 1, 79, 77, 75	**P0.0–P0.7.** General purpose I/O Port 0. This port is open–drain and can not drive a logic 1. It requires external pull–ups. Port 0 is also the multiplexed Expanded Address/Data bus. When used in this mode, it does not require pull–ups.

PIN NUMBER	DESCRIPTION
13, 14	**V_{CC} – +5V**
16, 8, 18, 80, 76, 4, 6, 20, 24, 26, 28, 30, 33, 35, 37	**BA14–0.** Byte–wide Address bus bits 14–0. This 15 bit bus is combined with the non–multiplexed data bus (BD7–0) to access NV SRAM. Decoding is performed on $\overline{CE1}$ and $\overline{CE2}$. Read/write access is controlled by R/$\overline{W}$. BA14–0 connect directly to an 8K or 32K SRAM. If an 8K RAM is used, BA13 and BA14 will be unconnected. Note BA13 and BA14 are inverted from the true logical address. Also note that BA14 is lithium backed.
71, 69, 67, 65, 61, 59, 57, 55	**BD7–0.** Byte–wide Data bus bits 7–0. This 8–bit bi–directional bus is combined with the non–multiplexed address bus (BA14–0) to access NV SRAM. Decoding is performed on $\overline{CE1}$ and $\overline{CE2}$. Read/write access is controlled by R/$\overline{W}$. BD7–0 connect directly to an 8K or 32K SRAM, and optionally to a Real–time Clock.
10	**R/$\overline{W}$ –** Read/Write. This signal provides the write enable to the SRAMs on the Byte–wide bus. It is controlled by the memory map and Partition. The blocks selected as Program (ROM) will be write protected.
74	**$\overline{CE1}$ –** Chip Enable 1. This is the primary decoded chip enable for memory access on the Byte–wide bus. It connects to the chip enable input of one SRAM. $\overline{CE1}$ is lithium backed. It will remain in a logic high inactive state when V_{CC} falls below V_{LI}.
78	**$\overline{CE2}$ –** Chip Enable 2. This chip enable is provided to bank switch to a second block of 32K bytes of nonvolatile data memory. It connects to the chip enable input of one SRAM or one lithium backed peripheral such a DS1283 clock. $\overline{CE2}$ is lithium backed. It will remain in a logic high inactive state when V_{CC} falls below V_{LI}.
12	**V_{CCO} –** V_{CC} Output. This is switched between V_{CC} and V_{LI} by internal circuits based on the level of V_{CC}. When power is above the lithium input, power will be drawn from V_{CC}. The lithium cell remains isolated from a load. When V_{CC} is below V_{LI}, the V_{CCO} switches to the V_{LI} source. V_{CCO} is connected to the V_{CC} pin of an SRAM.
54	**V_{LI}L –** Lithium Voltage Input. Connect to a lithium cell greater than V_{LImin} and no greater than V_{LImax} as shown in the electrical specifications. Nominal value is +3V.
2, 3, 22, 23, 32, 42, 43, 62, 63, 72	**NC do not connect.**

INSTRUCTION SET

The DS5000FP executes an instruction set that is object code compatible with the industry standard 8051 microcontroller. As a result, software development packages such as assemblers and compilers that have been written for the 8051 are compatible with the DS5000FP. A complete description of the instruction set and operation are provided in the User's Guide section of the Secure Microcontroller Data Book.

Also note that the DS5000FP is embodied in the DS5000(T) and DS2250(T) modules. The DS5000(T) combines the DS5000FP with one SRAM of either 8K or 32K bytes and a lithium cell. An optional Real Time Clock is also available in the DS5000T. This is packaged in a 40–pin DIP module. The DS2250(T) is an identical function in a SIMM form factor. It also offers the option of a second 32K SRAM mapped as data on Chip Enable 2.

MEMORY ORGANIZATION

Figure 2 illustrates the memory map accessed by the DS5000FP. The entire 64K of program and 64K of data is available. The DS5000FP maps 32K of this space into the SRAM connected to the Byte–wide bus. This is the area from 0000h to 7FFFh (32K) and is reached via $\overline{CE1}$. Any area not mapped into the NV RAM is reached via the Expanded bus on Ports 0 & 2. Selecting $\overline{CE2}$ provides another 32K of potential data storage. When $\overline{CE2}$ is used, no data is available on the ports. The memory

map is covered in detail in the User's Guide section of the Secure Microcontroller Data Book.

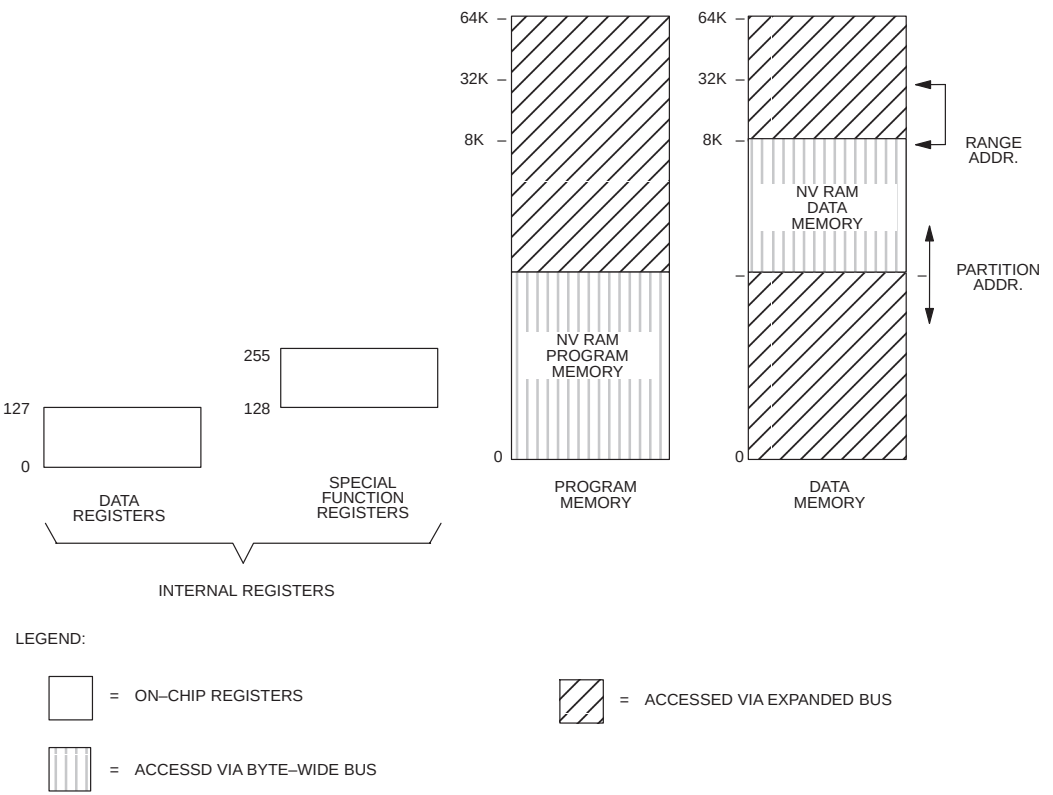
Figure 3 illustrates a typical memory connection for a system using 8K bytes of SRAM. Figure 4 shows a similar system with 32K bytes. The Byte–wide Address bus connects to the SRAM address lines. The bi–directional Byte–wide data bus connects the data I/O lines of the SRAM. $\overline{CE1}$ provides the chip enable and R/$\overline{W}$ is the write enable. An additional RAM could be connected to $\overline{CE2}$, with common connections for R/$\overline{W}$, BA14–0, and BD7–0.

POWER MANAGEMENT

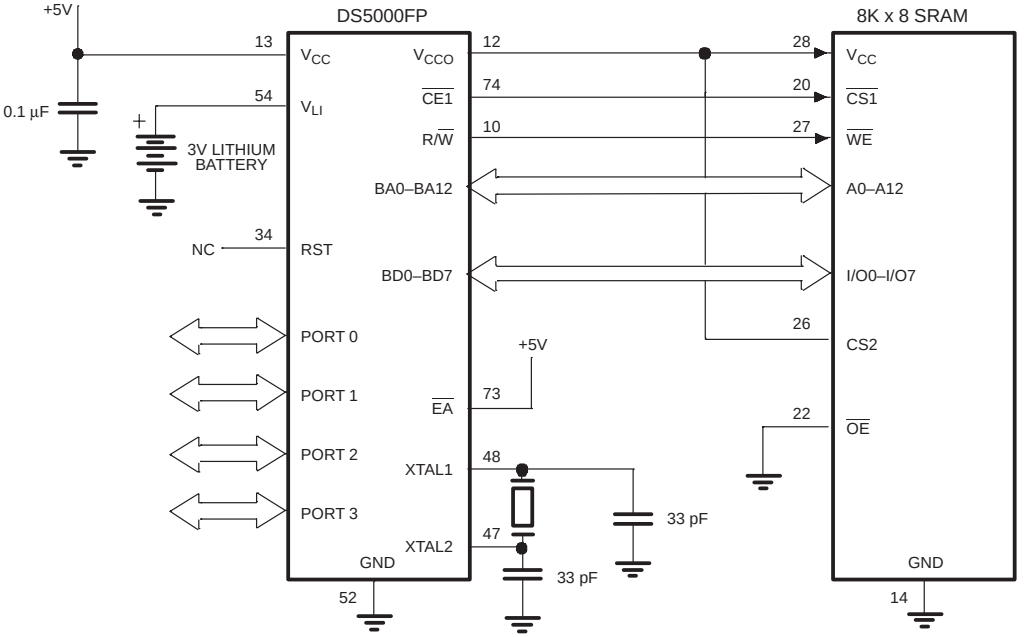
The DS5000FP monitors power to provide Power–fail Reset, early warning Power–fail Interrupt, and switch over to lithium backup. It uses the Lithium cell at V_{LI} as a reference in determining the switch points. These are called V_{PFW}, V_{CCMIN}, and V_{LI} respectively. When V_{CC} drops below V_{PFW}, the DS5000FP will perform an interrupt vector to location 2Bh if the power–fail warning was enabled. Full processor operation continues regardless. When power falls further to V_{CCMIN}, the DS5000FP invokes a reset state. No further code execution will be performed unless power rises back above V_{CCMIN}. $\overline{CE1}$, $\overline{CE2}$, R/$\overline{W}$ go to an inactive (logic 1) state. Any address lines that are high (due to encryption) will follow V_{CC}, except for BA14 which is lithium backed. V_{CC} is still the power source at this time. When V_{CC} drops further to below V_{LI}, internal circuitry will switch to the lithium cell for power. The majority of internal circuits will be disabled and the remaining nonvolatile states will be retained. Any devices connected to V_{CCO} will be powered by the lithium cell at this time. V_{CCO} will be at the lithium battery voltage less a diode drop. This drop will vary depending on the load. Low leakage SRAMs should be used for this reason. When a module is used, the lithium cell is selected by Dallas so absolute specifications are provided for the switch thresholds. When using the DS5000FP, the user must select the appropriate battery. The following formulas apply to the switch function.

$V_{PFW} = 1.45 * V_{LI}$
$V_{CCMIN} = 1.40 * V_{LI}$
V_{LI} Switch $= 1.0 * V_{LI}$

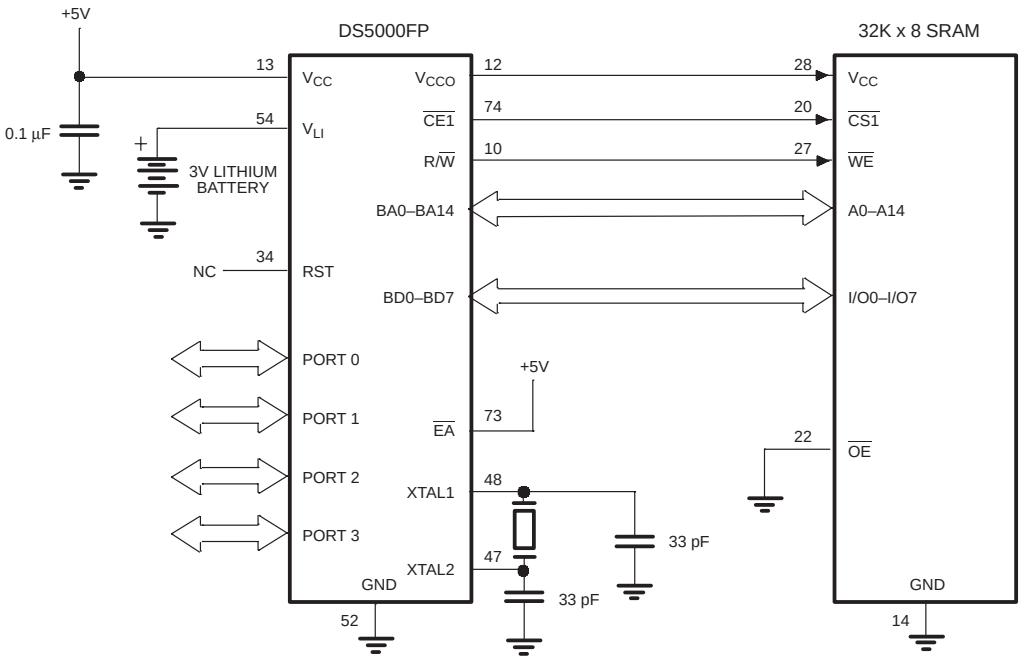
MEMORY MAP OF THE DS5000FP Figure 2



DS5000FP CONNECTION TO 8K X 8 SRAM Figure 3



DS5000FP CONNECTION TO 32K X 8 SRAM Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC CHARACTERISTICS

(t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Low Voltage	V_{IL}	–0.3		0.8	V	1
Input High Voltage	V_{IH1}	2.0		V_{CC} +0.3	V	1
Input High Voltage RST, XTAL1	V_{IH2}	3.5		V_{CC} +0.3	V	1
Output Low Voltage @ I_{OL}=1.6 mA (Ports 1, 2, 3)	V_{OL1}		0.15	0.45	V	
Output Low Voltage @ I_{OL}=3.2 mA (Ports 0, ALE, PSEN, BA14–0, BD7–0, R/$\overline{W}$, $\overline{CE}$1–2).	V_{OL2}		0.15	0.45	V	1
Output High Voltage @ I_{OH}=–80 µA (Ports 1, 2, 3)	V_{OH1}	2.4	4.8		V	1
Output High Voltage @ I_{OH}=–400 µA (Ports 0, ALE, PSEN, BA14–0, BD7–0, R/$\overline{W}$, $\overline{CE}$1–2).	V_{OH2}	2.4	4.8		V	1
Input Low Current V_{IN} = 0.45V (Ports 1, 2, 3)	I_{IL}			–50	µA	
Transition Current; 1 to 0 V_{IN} = 2.0V (Ports 1, 2, 3)	I_{TL}			–500	µA	
Input Leakage Current 0.45 < V_{IN} < V_{CC} (Port 0)	I_L			±10	µA	
RST, $\overline{EA}$ Pulldown Resistor	R_{RE}	40		125	KΩ	
Stop Mode Current	I_{SM}			80	µA	4
Power–Fail Warning Voltage	V_{PFW}	4.15	4.6	4.75	V	1, 6
Minimum Operating Voltage	V_{CCmin}	4.05	4.5	4.65	V	1, 6
Lithium Supply Voltage	V_{LI}	2.9		3.3	V	1
Programming Supply Voltage (Parallel Program Mode)	V_{PP}	12.5		13	V	1
Program Supply Current	I_{PP}		15	20	mA	
Operating Current @ 16 MHz	I_{CC}			36	mA	2
Idle Mode Current @ 12 MHz	I_{IDLE}			6.2	mA	3
Output Supply Voltage	V_{CCO1}	V_{CC}–0.3			V	1
Output Supply Voltage (Battery–backed mode)	V_{CCO2}	V_{LI}–0.65	V_{LI}–0.5		V	8

DC CHARACTERISTICS (cont'd) (t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Supply Current @ $V_{CCO} = V_{CC}–0.3V$	I_{CCO1}		80		mA	2
Battery–Backed Quiescent Current	I_{LI}		5	75	nA	7

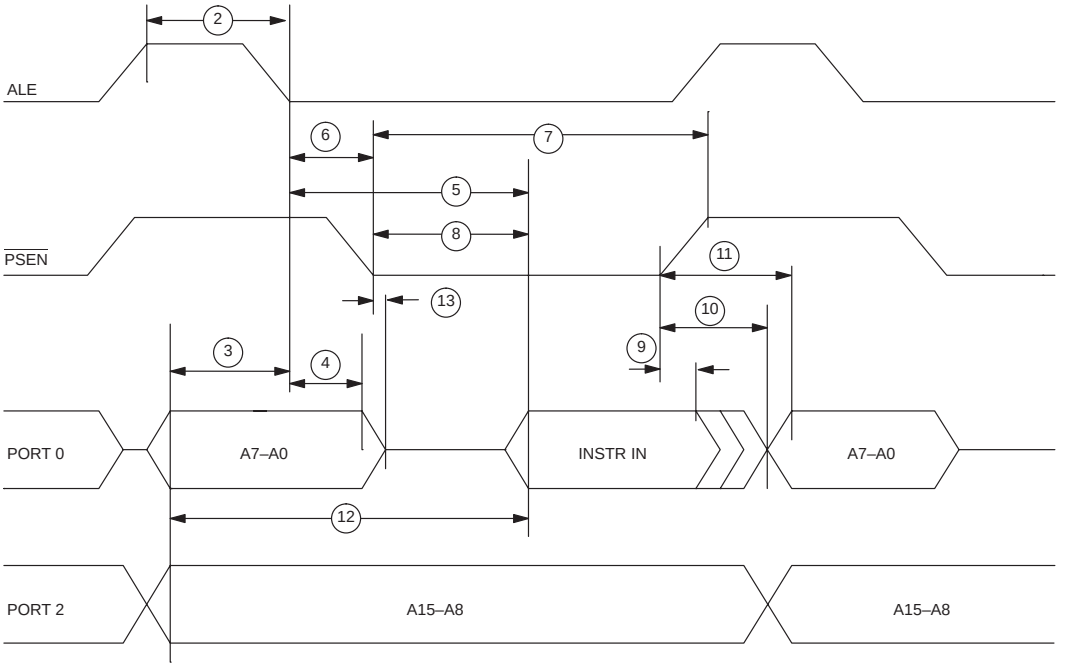
AC CHARACTERISTICS
EXPANDED BUS MODE TIMING SPECIFICATIONS (t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
1	Oscillator Frequency	$1/t_{CLK}$	1.0	16	MHz
2	ALE Pulse Width	t_{ALPW}	$2t_{CLK}–40$		ns
3	Address Valid to ALE Low	t_{AVALL}	$t_{CLK}–40$		ns
4	Address Hold After ALE Low	t_{AVAAV}	$t_{CLK}–35$		ns
5	ALE Low to Valid Instr. In @12 MHz @16 MHz	t_{ALLVI}		$4t_{CLK}–150$ $4t_{CLK}–90$	ns ns
6	ALE Low to $\overline{PSEN}$ Low	t_{ALLPSL}	$t_{CLK}–25$		ns
7	$\overline{PSEN}$ Pulse Width	t_{PSPW}	$3t_{CLK}–35$		ns
8	$\overline{PSEN}$ Low to Valid Instr. In @12 MHz @16 MHz	t_{PSLVI}		$3t_{CLK}–150$ $3t_{CLK}–90$	ns ns
9	Input Instr. Hold after $\overline{PSEN}$ Going High	t_{PSIV}	0		ns
10	Input Instr. Float after $\overline{PSEN}$ Going High	t_{PSIX}		$t_{CLK}–20$	ns
11	Address Hold after $\overline{PSEN}$ Going High	t_{PSAV}	$t_{CLK}–8$		ns
12	Address Valid to Valid Instr. In @12 MHz @16 MHz	t_{AVVI}		$5t_{CLK}–150$ $5t_{CLK}–90$	ns ns
13	$\overline{PSEN}$ Low to Address Float	t_{PSLAZ}	0		ns
14	$\overline{RD}$ Pulse Width	t_{RDPW}	$6t_{CLK}–100$		ns
15	$\overline{WR}$ Pulse Width	t_{WRPW}	$6t_{CLK}–100$		ns
16	$\overline{RD}$ Low to Valid Data In @12 MHz @16 MHz	t_{RDLDV}		$5t_{CLK}–165$ $5t_{CLK}–105$	ns ns
17	Data Hold after $\overline{RD}$ High	t_{RDHDV}	0		ns
18	Data Float after $\overline{RD}$ High	t_{RDHDZ}		$2t_{CLK}–70$	ns
19	ALE Low to Valid Data In @12 MHz @16 MHz	t_{ALLVD}		$8t_{CLK}–150$ $8t_{CLK}–90$	ns ns
20	Valid Addr. to Valid Data In @12 MHz @16 MHz	t_{AVDV}		$9t_{CLK}–165$ $9t_{CLK}–105$	ns ns
21	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{ALLRDL}	$3t_{CLK}–50$	$3t_{CLK}$ +50	ns
22	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVRDL}	$4t_{CLK}–130$		ns
23	Data Valid to $\overline{WR}$ Going Low	t_{DVWRL}	$t_{CLK}–60$		ns
24	Data Valid to $\overline{WR}$ High @12 MHz @16 MHz	t_{DVWRH}	$7t_{CLK}–150$ $7t_{CLK}–90$		ns ns
25	Data Valid after $\overline{WR}$ High	t_{WRHDV}	$t_{CLK}–50$		ns

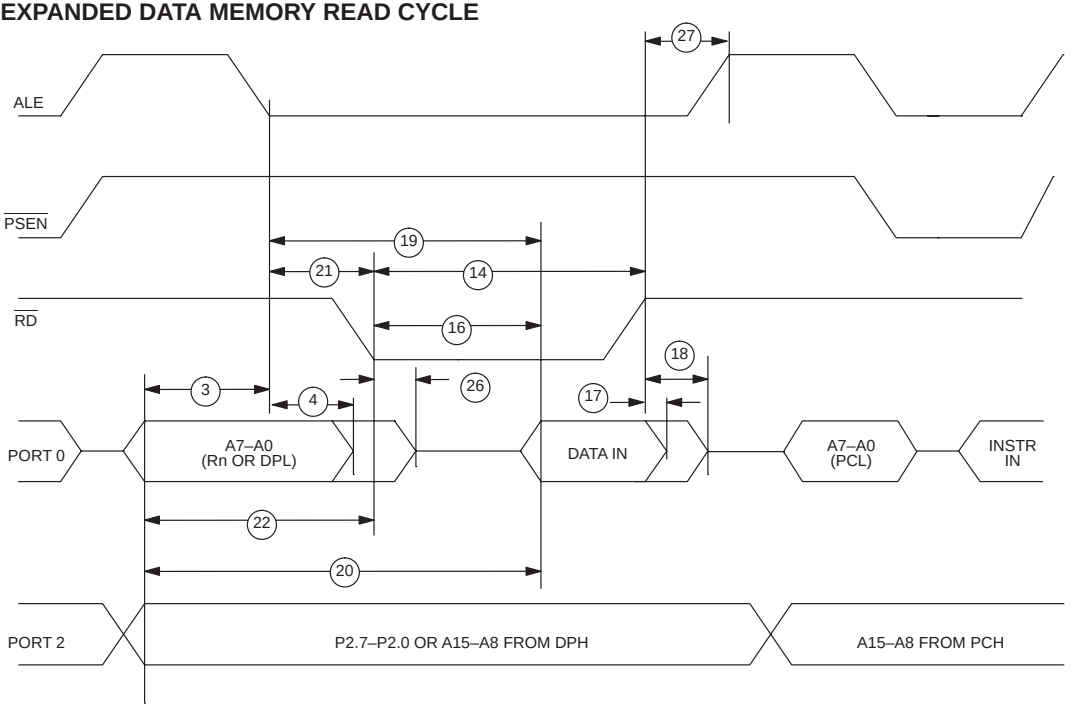
AC CHARACTERISTICS
EXPANDED BUS MODE TIMING SPECIFICATIONS (cont'd) (t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
26	$\overline{RD}$ Low to Address Float	t_{RDLAZ}		0	ns
27	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{RDHALH}	t_{CLK}–40	t_{CLK}+50	ns

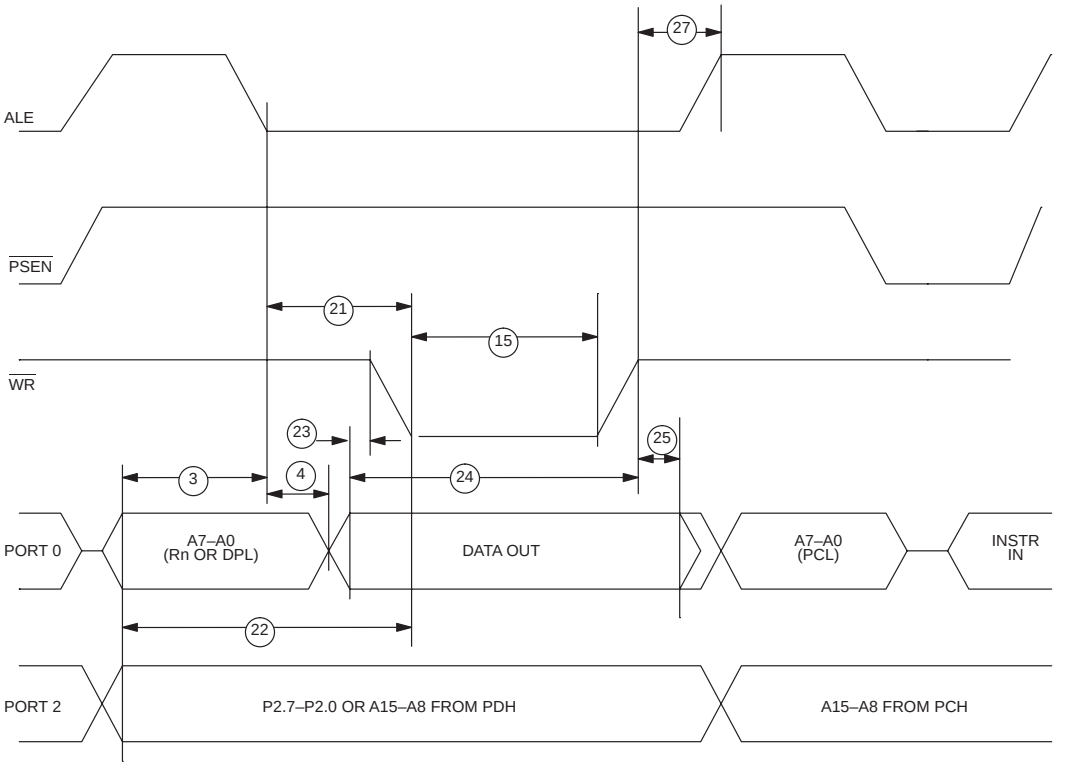
EXPANDED PROGRAM MEMORY READ CYCLE



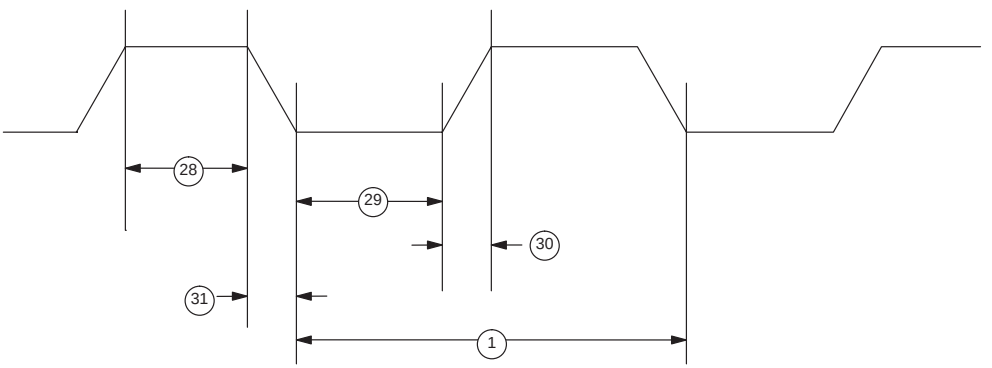
EXPANDED DATA MEMORY READ CYCLE



EXPANDED DATA MEMORY WRITE CYCLE



EXTERNAL CLOCK TIMING



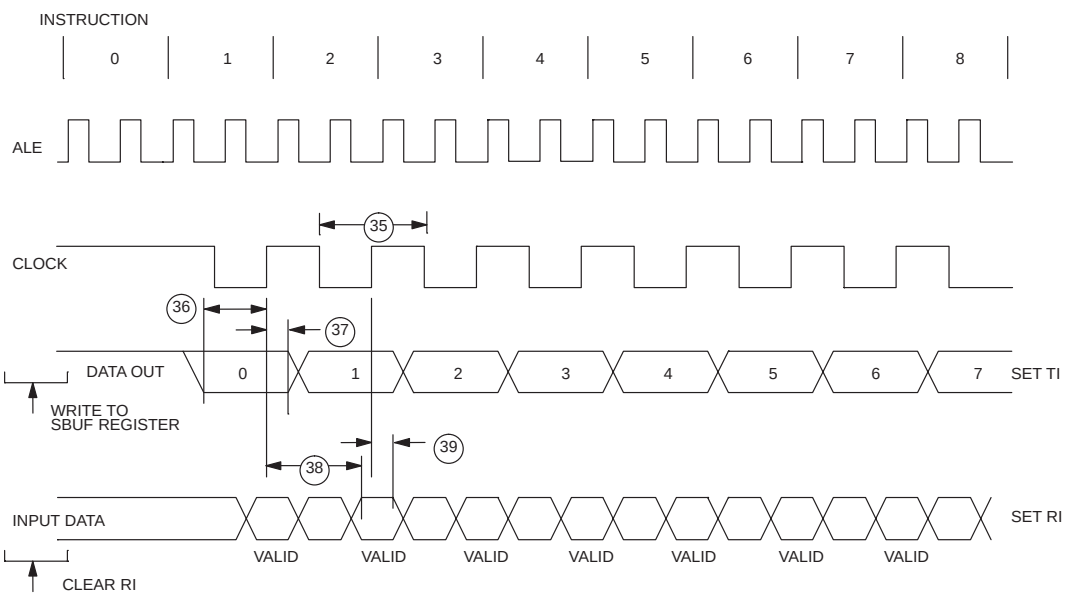
AC CHARACTERISTICS (cont'd)
EXTERNAL CLOCK DRIVE (t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

#	PARAMETER		SYMBOL	MIN	MAX	UNITS
28	External Clock High Time	@12 MHz @16 MHz	t_{CLKHPW}	20 15		ns ns
29	External Clock Low Time	@12 MHz @16 MHz	t_{CLKLPW}	20 15		ns ns
30	External Clock Rise Time	@12 MHz @16 MHz	t_{CLKR}		20 15	ns ns
31	External Clock Fall Time	@12 MHz @16 MHz	t_{CLKF}		20 15	ns ns

AC CHARACTERISTICS (cont'd)
SERIAL PORT TIMING – MODE 0 (t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
35	Serial Port Cycle Time	t_{SPCLK}	$12t_{CLK}$		µs
36	Output Data Setup to Rising Clock Edge	t_{DOCH}	$10t_{CLK}$–133		ns
37	Output Data Hold after Rising Clock Edge	t_{CHDO}	$2t_{CLK}$–117		ns
38	Clock Rising Edge to Input Data Valid	t_{CHDV}		$10t_{CLK}$–133	ns
39	Input Data Hold after Rising Clock Edge	t_{CHDIV}	0		ns

SERIAL PORT TIMING – MODE 0

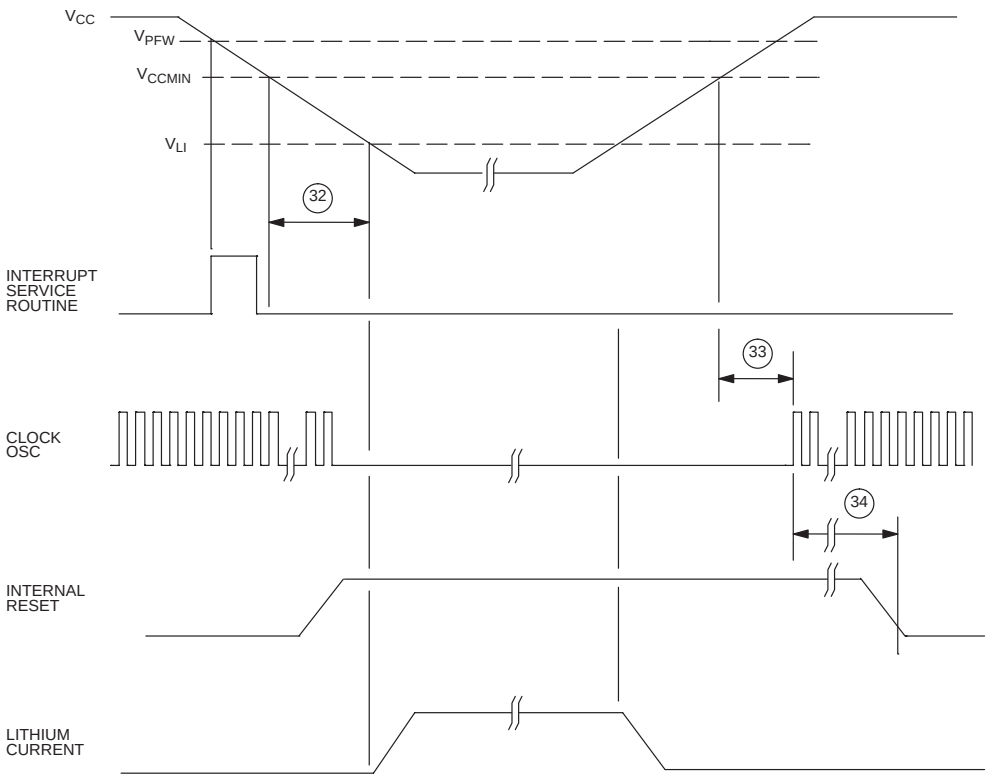


AC CHARACTERISTICS (cont'd)
POWER CYCLING TIMING

(t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
32	Slew Rate from V_{CCmin} to V_{LImax}	t_F	40		µs
33	Crystal Start up Time	t_{CSU}		(note 5)	
34	Power–On Reset Delay	t_{POR}		21504	t_{CLK}

POWER CYCLE TIMING

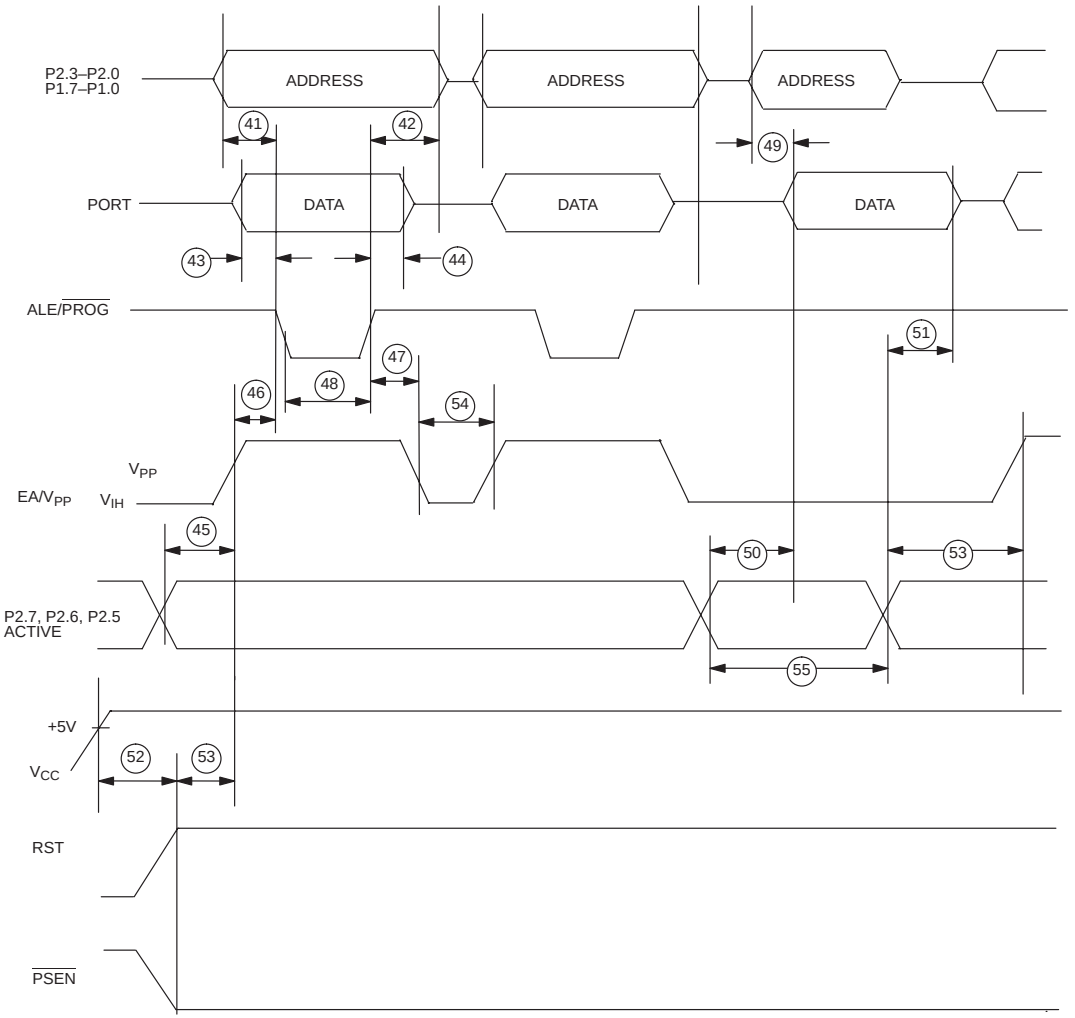


AC CHARACTERISTICS (cont'd)
PARALLEL PROGRAM LOAD TIMING (t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
40	Oscillator Frequency	$1/t_{CLK}$	1.0	12.0	MHz
41	Address Setup to $\overline{PROG}$ Low	t_{AVPRL}	0		
42	Address Hold after $\overline{PROG}$ High	t_{PRHAV}	0		
43	Data Setup to $\overline{PROG}$ Low	t_{DVPRL}	0		
44	Data Hold after $\overline{PROG}$ High	t_{PRHDV}	0		
45	P2.7, 2.6, 2.5 Setup to V_{PP}	t_{P27HVP}	0		
46	V_{PP} Setup to $\overline{PROG}$ Low	t_{VPHPRL}	0		
47	V_{PP} Hold after $\overline{PROG}$ Low	t_{PRHVPL}	0		
48	$\overline{PROG}$ Width Low	t_{PRW}	2400		t_{CLK}
49	Data Output from Address Valid	t_{AVDV}		48 1800*	t_{CLK}
50	Data Output from P2.7 Low	t_{DVP27L}		48 1800*	t_{CLK}
51	Data Float after P2.7 High	t_{P27HDZ}	0	48 1800*	t_{CLK}
52	Delay to Reset/$\overline{PSEN}$ Active after Power–On	t_{PORPV}	21504		t_{CLK}
53	Reset/$\overline{PSEN}$ Active (or Verify Inactive) to V_{PP} High	t_{RAVPH}	1200		t_{CLK}
54	V_{PP} Inactive (Between Program Cycles)	t_{VPPPC}	1200		t_{CLK}
55	Verify Active Time	t_{VFT}	48 2400*		t_{CLK}

* Second set of numbers refers to expanded memory programming up to 32K bytes.

PARALLEL PROGRAM LOAD TIMING



CAPACITANCE

(test frequency = 1 MHz; t_A = 25°C)

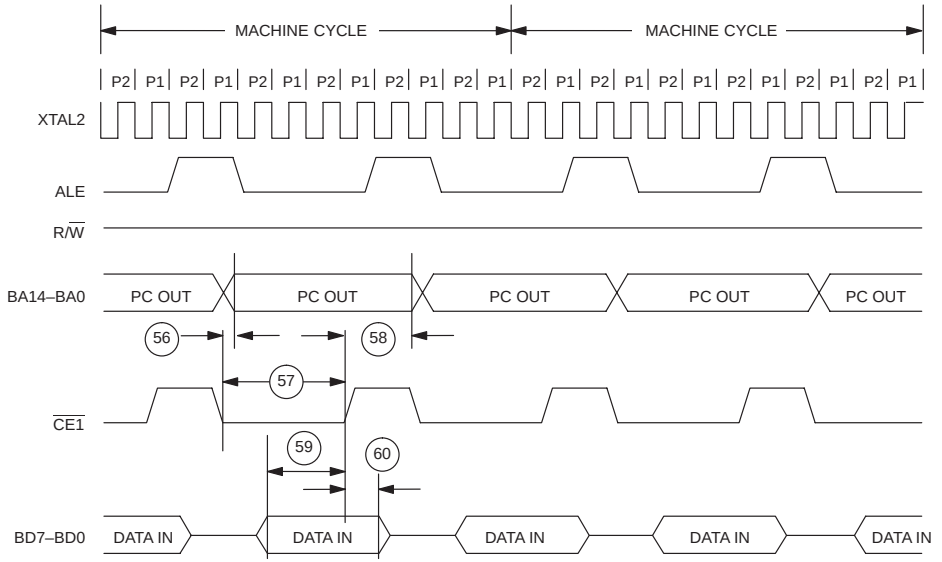
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Capacitance	C_O			10	pF	
Input Capacitance	C_I			10	pF	

BYTE–WIDE ADDRESS/DATA BUS TIMING
AC CHARACTERISTICS

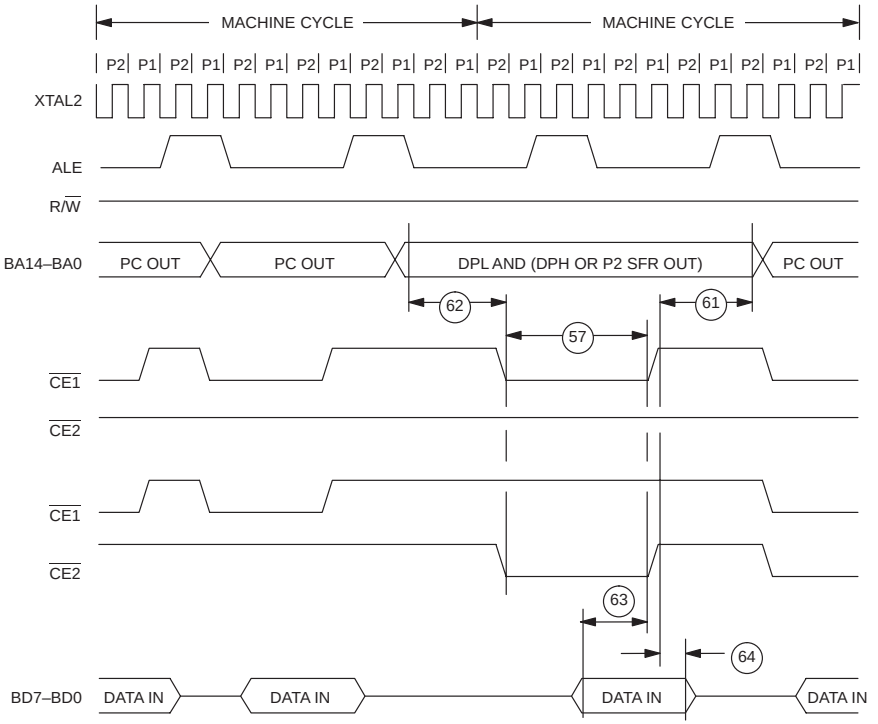
(t_A = 0°C to70°C; V_{CC} = 5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
56	Delay to Embedded Address Valid from $\overline{CE1}$ Low During Opcode Fetch	t_{CE1LPA}		20	ns
57	$\overline{CE1}$ or $\overline{CE2}$ Pulse Width	t_{CEPW}	$4t_{CLK}$–15		ns
58	Embedded Address Hold after $\overline{CE1}$ High During Opcode Fetch	t_{CE1HPA}	$2t_{CLK}$–20		ns
59	Embedded Data Setup to $\overline{CE1}$ High During Opcode Fetch	t_{OVCE1H}	$1t_{CLK}$+40		ns
60	Embedded Data Hold after $\overline{CE1}$ High During Opcode Fetch	t_{CE1HOV}	10		ns
61	Embedded Address Hold after $\overline{CE1}$ or $\overline{CE2}$ High During MOVX	t_{CEHDA}	$4t_{CLK}$–30		ns
62	Delay from Embedded Address Valid to $\overline{CE1}$ or $\overline{CE2}$ Low During MOVX	t_{CELDA}	$4t_{CLK}$–25		ns
63	Embedded Data Hold Setup to $\overline{CE1}$ or $\overline{CE2}$ High During MOVX (read)	t_{DACEH}	$1t_{CLK}$+40		ns
64	Embedded Data Hold after $\overline{CE1}$ or $\overline{CE2}$ High During MOVX (read)	t_{CEHDV}	10		ns
65	Embedded Address Valid to R/$\overline{W}$ Active During MOVX (write)	t_{AVRWL}	$3t_{CLK}$–35		ns
66	Delay from R/$\overline{W}$ Low to Valid Data Out During MOVX (write)	t_{RWLDV}	20		ns
67	Valid Data Out Hold Time from $\overline{CE1}$ or $\overline{CE2}$ High	t_{CEHDV}	$1t_{CLK}$–15		ns
68	Valid Data Out Hold Time from R/$\overline{W}$ High	t_{RWHDV}	0		ns
69	Write Pulse Width (R/$\overline{W}$ low time)	t_{RWLPW}	$6t_{CLK}$–20		ns

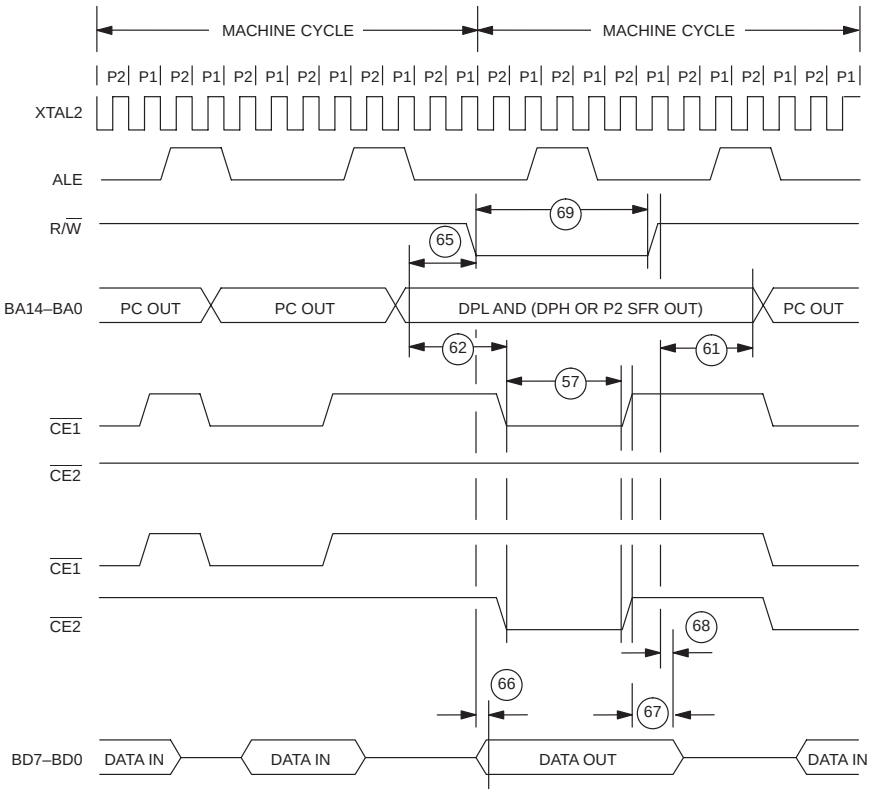
BYTE–WIDE ADDRESS/DATA BUS OPCODE FETCH CYCLE



BYTE–WIDE ADDRESS/DATA BUS OPCODE FETCH WITH DATA MEMORY READ



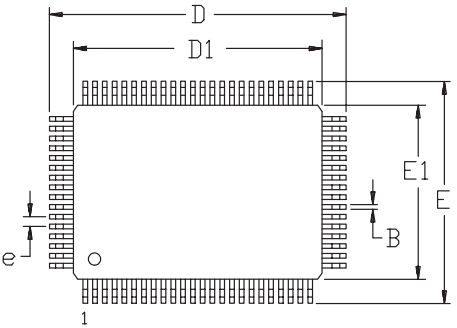
BYTE–WIDE ADDRESS/DATA BUS OPCODE FETCH WITH DATA MEMORY WRITE

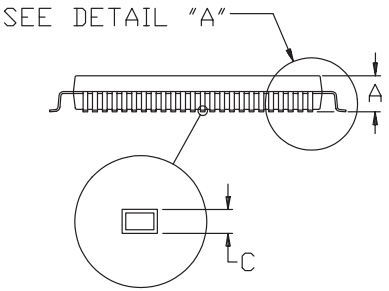


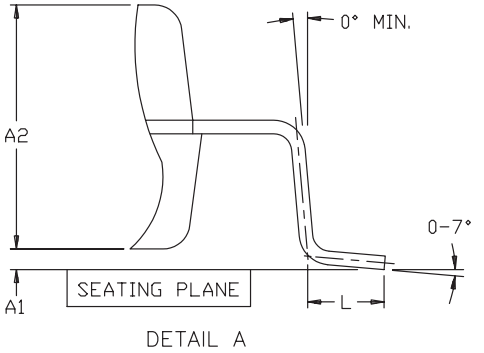
NOTES:

1. All voltages are referenced to ground.
2. Maximum operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF}=10 ns, V_{IL} = 0.5V; XTAL2 disconnected; $\overline{EA}$ = RST = PORT0 = V_{CC}.
3. Idle mode I_{CC} is measured with all output pins disconnected; XTAL1 driven at 12 MHz with t_{CLKR}, t_{CLKF}=10 ns, V_{IL} = 0.5V; XTAL2 disconnected; $\overline{EA}$ = PORT0 = V_{CC}, RST = V_{SS}.
4. Stop mode I_{CC} is measured with all output pins disconnected; $\overline{EA}$ = PORT0 = V_{CC}; XTAL2 not connected; RST = V_{SS}.
5. Crystal start–up time is the time required to get the mass of the crystal into vibrational motion from the time that power is first applied to the circuit until the first clock pulse is produced by the on–chip oscillator. The user should check with the crystal vendor for the worst case spec on this time.
6. Assumes V_{LI}=3.3V maximum.
7. I_{LI} is the current drawn from V_{LI} when V_{CC}=0V and V_{CCO} is disconnected.
8. I_{CCO}=10 µA.

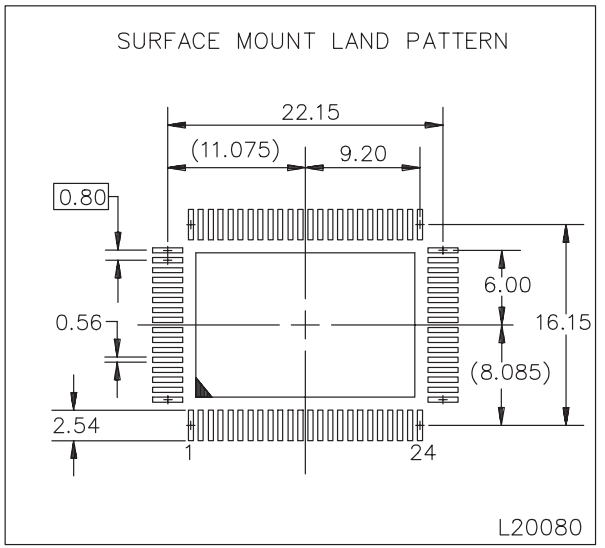
DS5000FP CMOS MICROPROCESSOR







DETAIL A



DIM	MILLIMETERS	
	MIN	MAX
A	–	3.15
A1	0.25	–
A2	2.55	2.87
B	0.30	0.50
C	0.13	0.23
D	23.70	24.10
D1	19.90	20.10
E	17.40	18.10
E1	13.90	14.10
e	0.80 BSC	
L	0.65	0.95

56–G4005–001

DATA SHEET REVISION SUMMARY

The following represent the key differences between 07/27/95 and 07/24/96/96 version of the DS5000FP data sheet. Please review this summary carefully.

1. Add V_{CCO2} Minimum Specification (PCN F62501).
2. Add embedded bus DC specifications.
3. Update mechanical specifications.

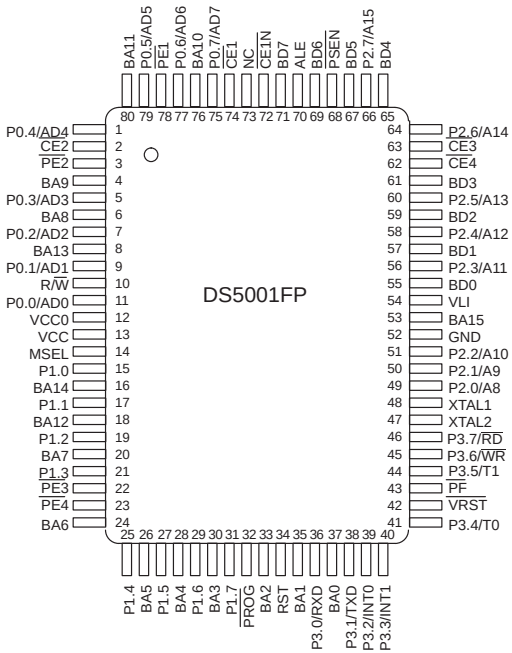
DALLAS SEMICONDUCTOR

DS5001FP
128K Soft Microprocessor Chip

FEATURES

- 8051 compatible microprocessor adapts to its task
  - Accesses up to 128K bytes of nonvolatile SRAM
  - In–system programming via on–chip serial port
  - Can modify its own program or data memory
  - Accesses memory on a separate Byte–wide bus
  - Performs CRC–16 check of NV RAM memory
  - Decodes memory and peripheral chip enables
- Crashproof Operation
  - Maintains all nonvolatile resources for over 10 years
  - Power–fail Reset
  - Early Warning Power–fail Interrupt
  - Watchdog Timer
  - Lithium backs user SRAM for program/data storage
  - Precision band–gap reference for power monitor
- Fully 8051 Compatible
  - 128K bytes scratchpad RAM
  - Two timer/counters
  - On–chip serial port
  - 32 parallel I/O port pins
- Software Security Available with DS5002FP Secure Microprocessor

PIN ASSIGNMENT



DESCRIPTION

The DS5001FP is an 8051 compatible microprocessor based on nonvolatile RAM technology. It is designed for systems that need large quantities of nonvolatile memory. Like its predecessor the DS5000(T), the DS5001FP is substantially more flexible than a standard 8051. It provides full compatibility with the 8051 instruction set, timers, serial port, and parallel I/O ports. By using NV RAM instead of ROM, the user can program, then reprogram the microprocessor while in–system. The application software can even change its own operation. This allows frequent software upgrades, adaptive programs, customized systems, etc. In addition, by using NV SRAM, the DS5001FP is ideal for data logging applications. It also connects easily to a Dallas Real Time Clock for time stamp and date.

The DS5001FP provides the benefits of NV RAM without using I/O resources. It uses a non–multiplexed Byte–wide address and data bus for memory access. This bus can perform all memory access and provides decoded chip enables for SRAM. This leaves the 32 I/O port pins free for application use. The DS5001FP uses ordinary SRAM and battery backs the memory contents with an external lithium cell. Data is maintained for over 10 years at room temperature with a very small lithium cell. A DS5001FP also provides crashproof operation in portable systems or systems with unreliable power. These features include the ability to save the operating state, Power–fail Reset, Power–fail Interrupt, and Watchdog Timer.

A user loads programs into the DS5001FP via its on–chip Serial Bootstrap Loader. This function supervises the loading of software into NV RAM, validates it, then becomes transparent to the user. Software can be stored in multiple 32K or one 128K byte CMOS SRAM(s). Using its internal Partitioning, the DS5001FP can divide a common RAM into user selectable program and data segments. This Partition can be selected at program loading time, but can be modified anytime later. The microprocessor will decode memory access to the SRAM, access memory via its Byte–wide bus and write–protect the memory portion designated as ROM. Combining program and data storage in one device saves board space and cost.

The DS5001FP offers several bank switches for access to even more memory. In addition to the primary data area of 64K bytes, a peripheral selector creates a second 64K byte data space with four accompanying chip enables. This area can be used for memory mapped peripherals or more data storage. The DS5001FP can also use its Expanded bus on Ports 0 and 2 (like an 8051) to access an additional 64K bytes of data space. Lastly, the DS5001FP provides one additional bank switch that changes up to 60K bytes of the NV RAM program space into data memory. Thus with a small amount of logic, the DS5001 accesses up to 252K bytes of data memory.

For a user that wants a pre–constructed module using the DS5001FP, RAM, lithium cell, and a real time clock; the DS2251T is available and described in separate data sheet. More details are also contained in the User's Guide section of the Secure Microcontroller Data Book. For users that desire software security, the DS5002FP is functionally identical to the DS5001FP but provides the best firmware security available.

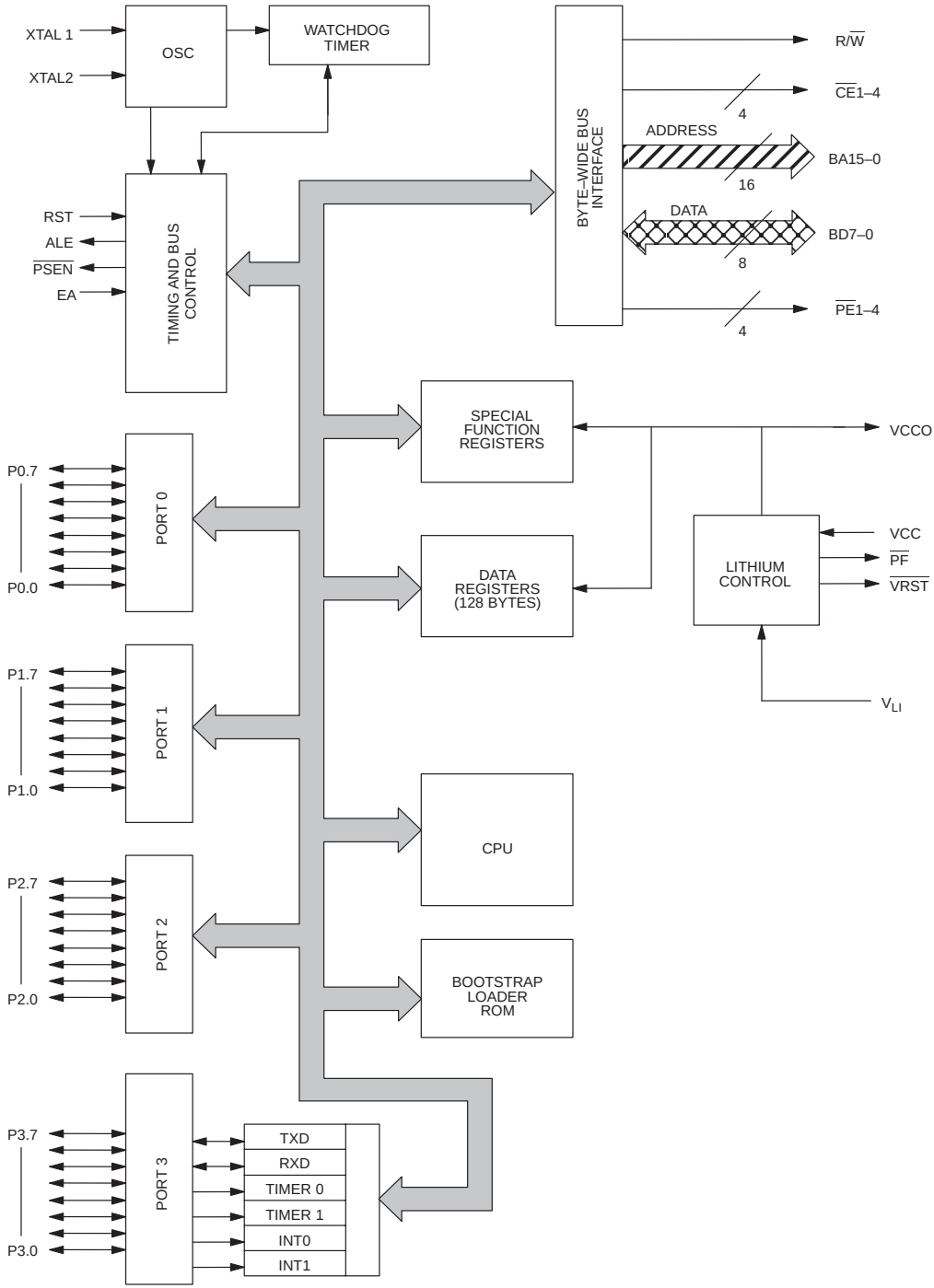
ORDERING INFORMATION

The following devices are available as standard products from Dallas Semiconductor:

PART #	DESCRIPTION
DS5001FP–16	80–pin QFP Max. clock speed 16 MHz, 0°C to +75°C operation

Operating information is contained in the User's Guide section of the Secure Microcontroller Data Book. This data sheet provides ordering information, pinout, and electrical specifications.

DS5001FP BLOCK DIAGRAM Figure 1



PIN DESCRIPTION

PIN	DESCRIPTION
11, 9, 7, 5, 1, 79, 77, 75	**P0.0 – P0.7.** General purpose I/O Port 0. This port is open–drain and can not drive a logic 1. It requires external pull–ups. Port 0 is also the multiplexed Expanded Address/Data bus. When used in this mode, it does not require pull–ups.
15, 17, 19, 21, 25, 27, 29, 31	**P1.0 – P1.7.** General purpose I/O Port 1.
49, 50, 51, 56, 58, 60, 64, 66	**P2.0 – P2.7.** General purpose I/O Port 2. Also serves as the MSB of the address in expanded memory accesses, and as pins of the RPC mode when used.
36	**P3.0 RXD.** General purpose I/O port pin 3.0. Also serves as the receive signal for the on board UART. This pin should NOT be connected directly to a PC COM port.
38	**P3.1 TXD.** General purpose I/O port pin 3.1. Also serves as the transmit signal for the on board UART. This pin should NOT be connected directly to a PC COM port.
39	**P3.2 $\overline{\text{INT0}}$.** General purpose I/O port pin 3.2. Also serves as the active low External Interrupt 0.
40	**P3.3 $\overline{\text{INT1}}$.** General purpose I/O port pin 3.3. Also serves as the active low External Interrupt 1.
41	**P3.4 T0.** General purpose I/O port pin 3.4. Also serves as the Timer 0 input.
44	**P3.5 T1.** General purpose I/O port pin 3.5. Also serves as the Timer 1 input.
45	**P3.6 $\overline{\text{WR}}$.** General purpose I/O port pin. Also serves as the write strobe for Expanded bus operation.
46	**P3.7 $\overline{\text{RD}}$.** General purpose I/O port pin. Also serves as the read strobe for Expanded bus operation.
34	**RST** – Active high reset input. A logic 1 applied to this pin will activate a reset state. This pin is pulled down internally so this pin can be left unconnected if not used. An RC power–on reset circuit is not needed and is NOT recommended.
68	**$\overline{\text{PSEN}}$** – Program Store Enable. This active low signal is used to enable an external program memory when using the Expanded bus. It is normally an output and should be unconnected if not used. $\overline{\text{PSEN}}$ also is used to invoke the Bootstrap Loader. At this time, $\overline{\text{PSEN}}$ will be pulled down externally. This should only be done once the DS5001FP is already in a reset state. The device that pulls down should be open drain since it must not interfere with $\overline{\text{PSEN}}$ under normal operation.
70	**ALE** – Address Latch Enable. Used to de–multiplex the multiplexed Expanded Address/Data bus on Port 0. This pin is normally connected to the clock input on a '373 type transparent latch.
47, 48	**XTAL2, XTAL1.** Used to connect an external crystal to the internal oscillator. XTAL1 is the input to an inverting amplifier and XTAL2 is the output.
52	**GND** – Logic ground.
13	**V_{CC} – +5V.**
12	**V_{CCO}** – V_{CC} Output. This is switched between V_{CC} and V_{LI} by internal circuits based on the level of V_{CC}. When power is above the lithium input, power will be drawn from V_{CC}. The lithium cell remains isolated from a load. When V_{CC} is below V_{LI}, the V_{CCO} switches to the V_{LI} source. V_{CCO} should be connected to the V_{CC} pin of an SRAM.
54	**V_{LI}** – Lithium Voltage Input. Connect to a lithium cell greater than V_{LImin} and no greater than V_{LImax} as shown in the electrical specifications. Nominal value is +3V.

PIN	DESCRIPTION
53, 16, 8, 18, 80, 76, 4, 6, 20, 24, 26, 28, 30, 33, 35, 37	**BA15 – 0.** Byte–wide Address bus bits 15–0. This bus is combined with the non–multiplexed data bus (BD7–0) to access NV SRAM. Decoding is performed using $\overline{CE1}$ through $\overline{CE4}$. Therefore, BA15 is not actually needed except for monitoring and debugging. Read/write access is controlled by R/$\overline{W}$. BA14–0 connect directly to an 8K, 32K, or 128K SRAM. If an 8K RAM is used, BA13 and BA14 will be unconnected. If a 128K SRAM is used, the micro converts $\overline{CE2}$ and $\overline{CE3}$ to serve as A16 and A15 respectively.
71, 69, 67, 65, 61, 59, 57, 55	**BD7 – 0.** Byte–wide Data bus bits 7–0. This 8 bit bi–directional bus is combined with the non–multiplexed address bus (BA14–0) to access NV SRAM. BD7–0 connect directly to an SRAM, and optionally to a Real Time Clock or other peripheral.
10	**R/$\overline{W}$** – Read/Write. This signal provides the write enable to the SRAMs on the Byte–wide bus. It is controlled by the memory map and Partition. The blocks selected as Program (ROM) will be write protected.
74	**$\overline{CE1}$** – Chip Enable 1. This is the primary decoded chip enable for memory access on the Byte–wide bus. It connects to the chip enable input of one SRAM. $\overline{CE1}$ is lithium backed. It will remain in a logic high inactive state when V_{CC} falls below V_{LI}.
72	**$\overline{CE1N}$** – Non battery backed version of chip enable 1. This can be used with a 32K byte EPROM. It should not be used with a battery backed chip.
2	**$\overline{CE2}$** – Chip Enable 2. This chip enable is provided to access a second 32K block of memory. It connects to the chip enable input of one SRAM. When MSEL=0, the micro converts $\overline{CE2}$ into A16 for a 128K x 8 SRAM. $\overline{CE2}$ is lithium backed and will remain at a logic high when V_{CC} falls below V_{LI}.
63	**$\overline{CE3}$** – Chip Enable 3. This chip enable is provided to access a third 32K block of memory. It connects to the chip enable input of one SRAM. When MSEL=0, the micro converts $\overline{CE3}$ into A15 for a 128K x 8 SRAM. $\overline{CE3}$ is lithium backed and will remain at a logic high when V_{CC} falls below V_{LI}.
62	**$\overline{CE4}$** – Chip Enable 4. This chip enable is provided to access a fourth 32K block of memory. It connects to the chip enable input of one SRAM. When MSEL=0, this signal is unused. $\overline{CE4}$ is lithium backed and will remain at a logic high when V_{CC} falls below V_{LI}.
78	**$\overline{PE1}$** – Peripheral Enable 1. Accesses data memory between addresses 0000h and 3FFFh when the PES bit is set to a logic 1. Commonly used to chip enable a Byte–wide Real Time Clock such as the DS1283. $\overline{PE1}$ is lithium backed and will remain at a logic high when V_{CC} falls below V_{LI}. Connect $\overline{PE1}$ to battery backed functions only.
3	**$\overline{PE2}$** – Peripheral Enable 2. Accesses data memory between addresses 4000h and 7FFFh when the PES bit is set to a logic 1. $\overline{PE2}$ is lithium backed and will remain at a logic high when V_{CC} falls below V_{LI}. Connect $\overline{PE2}$ to battery backed functions only.
22	**$\overline{PE3}$** – Peripheral Enable 3. Accesses data memory between addresses 8000h and BFFFh when the PES bit is set to a logic 1. $\overline{PE3}$ is not lithium backed and can be connected to any type of peripheral function. If connected to a battery backed chip, it will need additional circuitry to maintain the chip enable in an inactive state when $V_{CC} < V_{LI}$.
23	**$\overline{PE4}$** – Peripheral Enable 4. Accesses data memory between addresses C000h and FFFFh when the PES bit is set to a logic 1. $\overline{PE4}$ is not lithium backed and can be connected to any type of peripheral function. If connected to a battery backed chip, it will need additional circuitry to maintain the chip enable in an inactive state when $V_{CC} < V_{LI}$.
32	**$\overline{PROG}$** – Invokes the Bootstrap Loader on a falling edge. This signal should be debounced so that only one edge is detected. If connected to ground, the micro will enter Bootstrap loading on power up. This signal is pulled up internally.
42	**$\overline{VRST}$** – This I/O pin (open drain with internal pull–up) indicates that the power supply (V_{CC}) has fallen below the V_{CCmin} level and the micro is in a reset state. When this occurs, the DS5001FP will drive this pin to a logic 0. Because the micro is lithium backed, this signal is guaranteed even when V_{CC}=0V. Because it is an I/O pin, it will also force a reset if pulled low externally. This allows multiple parts to synchronize their power–down resets.

PIN	DESCRIPTION
43	**$\overline{PF}$** – This output goes to a logic 0 to indicate that the micro has switched to lithium backup. This corresponds to $V_{CC} < V_{LI}$. Because the micro is lithium backed, this signal is guaranteed even when V_{CC}=0V. The normal application of this signal is to control lithium powered current to isolate battery backed functions from non–battery backed functions.
14	**MSEL** – Memory select. This signal controls the memory size selection. When MSEL= +5V, the DS5001FP expects to use 32K x 8 SRAMs. When MSEL = 0V, the DS5001FP expects to use a 128K x 8 SRAM. MSEL must be connected regardless of Partition, Mode, etc.
73	**NC** – Do not connect.

INSTRUCTION SET

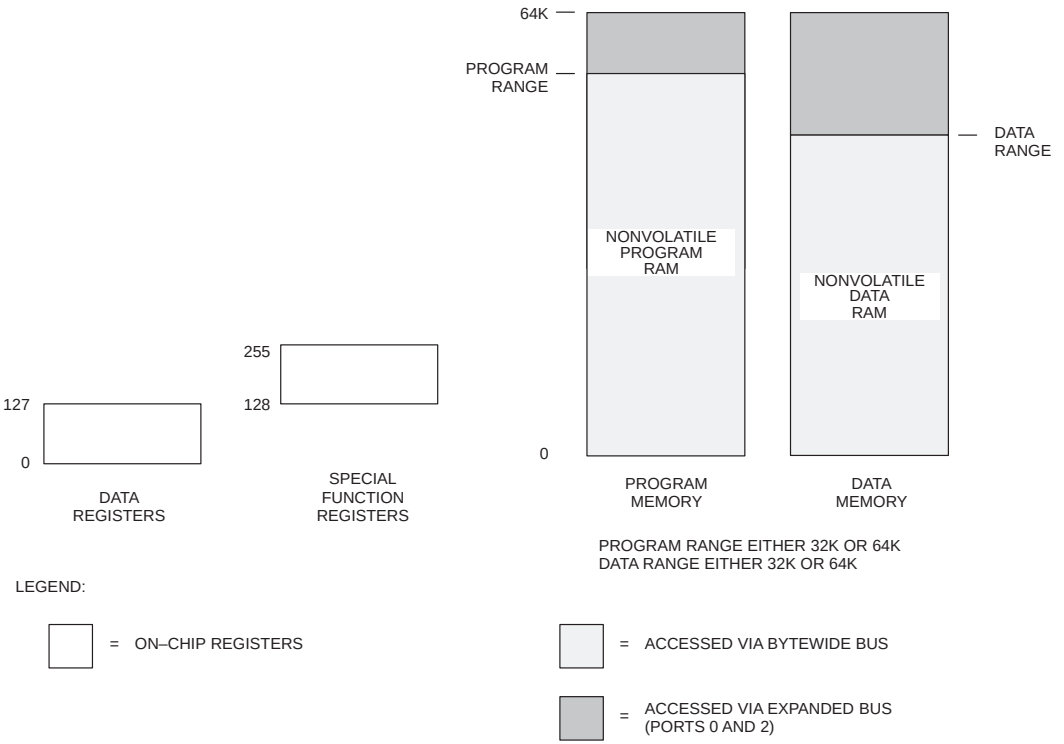
The DS5001FP executes an instruction set that is object code compatible with the industry standard 8051 microcontroller. As a result, software development packages such as assemblers and compilers that have been written for the 8051 are compatible with the DS5001FP. A complete description of the instruction set and operation are provided in the User's Guide section of the Secure Microcontroller Data Book.

Also note that the DS5001FP is embodied in the DS2251T module. The DS2251T combines the DS5001FP with between 32K and 128K of SRAM, a lithium cell, and a real time clock. This is packaged in a 72–pin SIMM module.

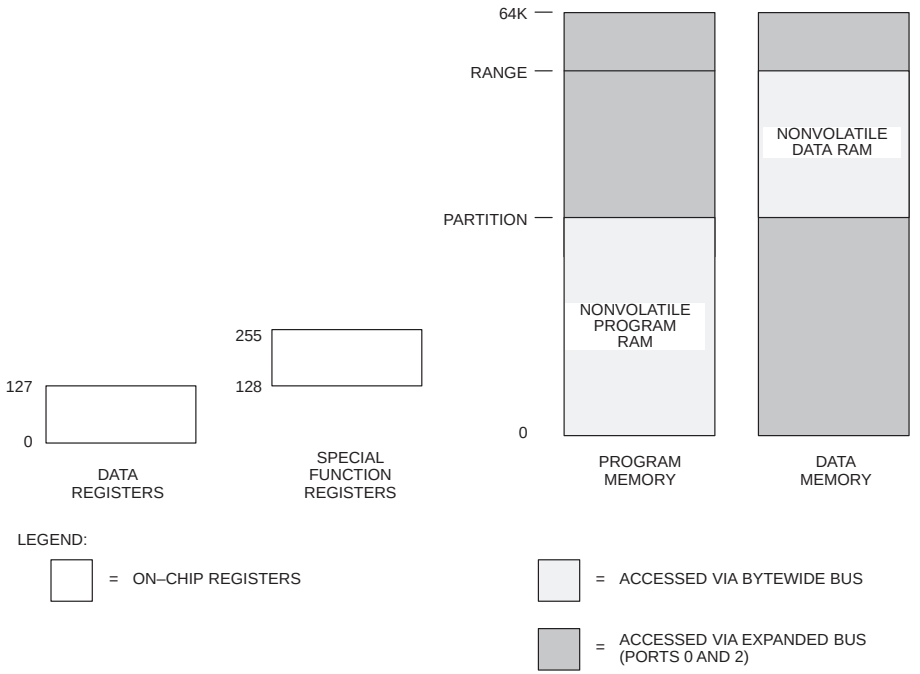
MEMORY ORGANIZATION

Figure 2 illustrates the memory map accessed by the DS5001FP. The entire 64K of program and 64K of data are potentially available to the Byte–wide bus. This preserves the I/O ports for application use. The user controls the portion of memory that is actually mapped to the Byte–wide bus by selecting the Program Range and Data Range. Any area not mapped into the NV RAM is reached via the Expanded bus on Ports 0 and 2. An alternate configuration allows dynamic Partitioning of a 64K space as shown in Figure 3. Selecting PES=1 provides another 64K of potential data storage or memory mapped peripheral space as shown in Figure 4. These selections are made using Special Function Registers. The memory map and its controls are covered in detail in the User's Guide section of the Secure Microcontroller Data Book.

DS5001FP MEMORY MAP IN NON–PARTITIONABLE MODE (PM=1) Figure 2



DS5001FP MEMORY MAP IN PARTITIONABLE MODE (PM=0) Figure 3



NOTE: Partitionable mode is not supported when MSEL pin = 0 (128KB mode).

DS5001FP MEMORY MAP WITH PES=1 Figure 4

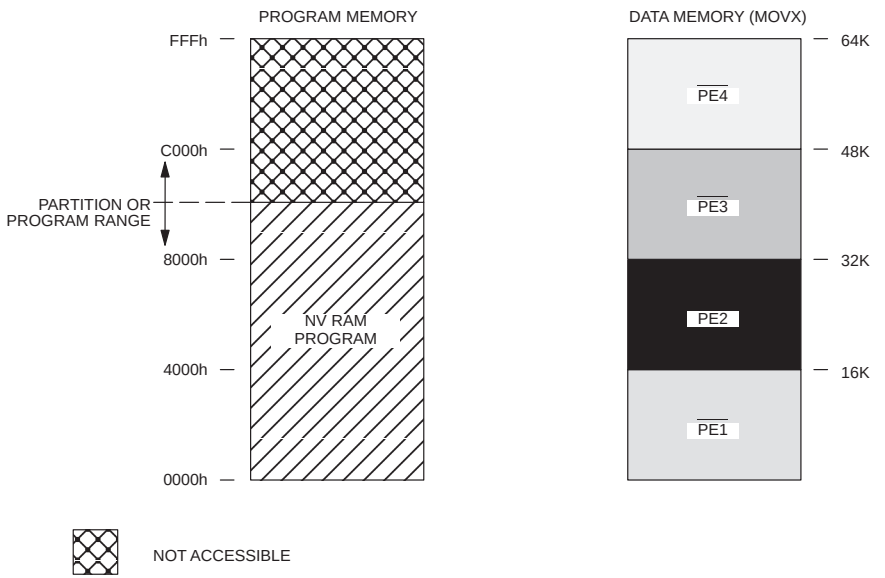
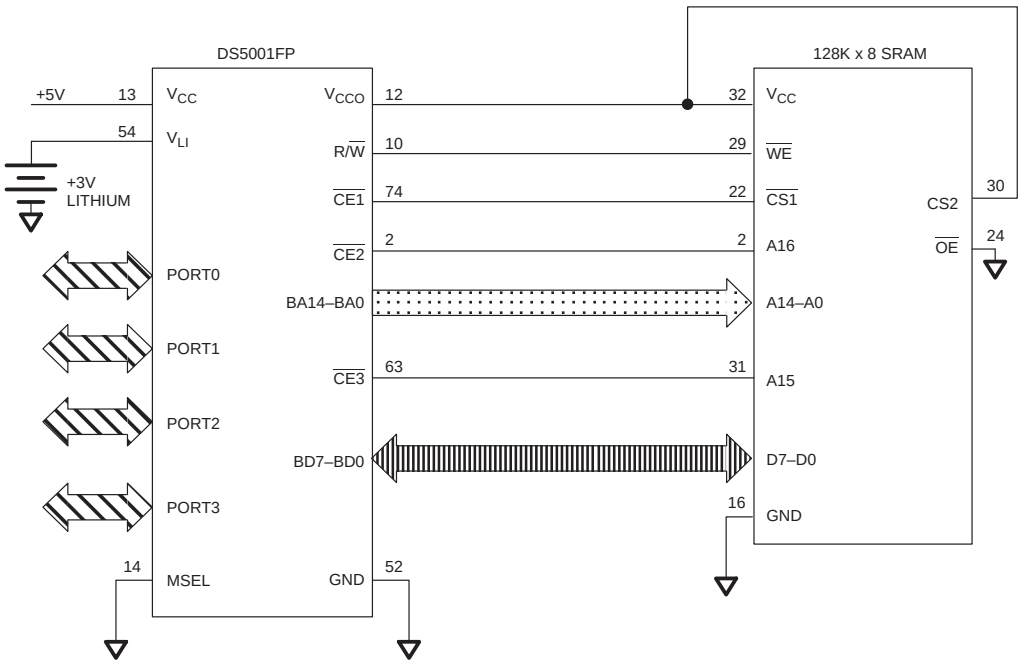
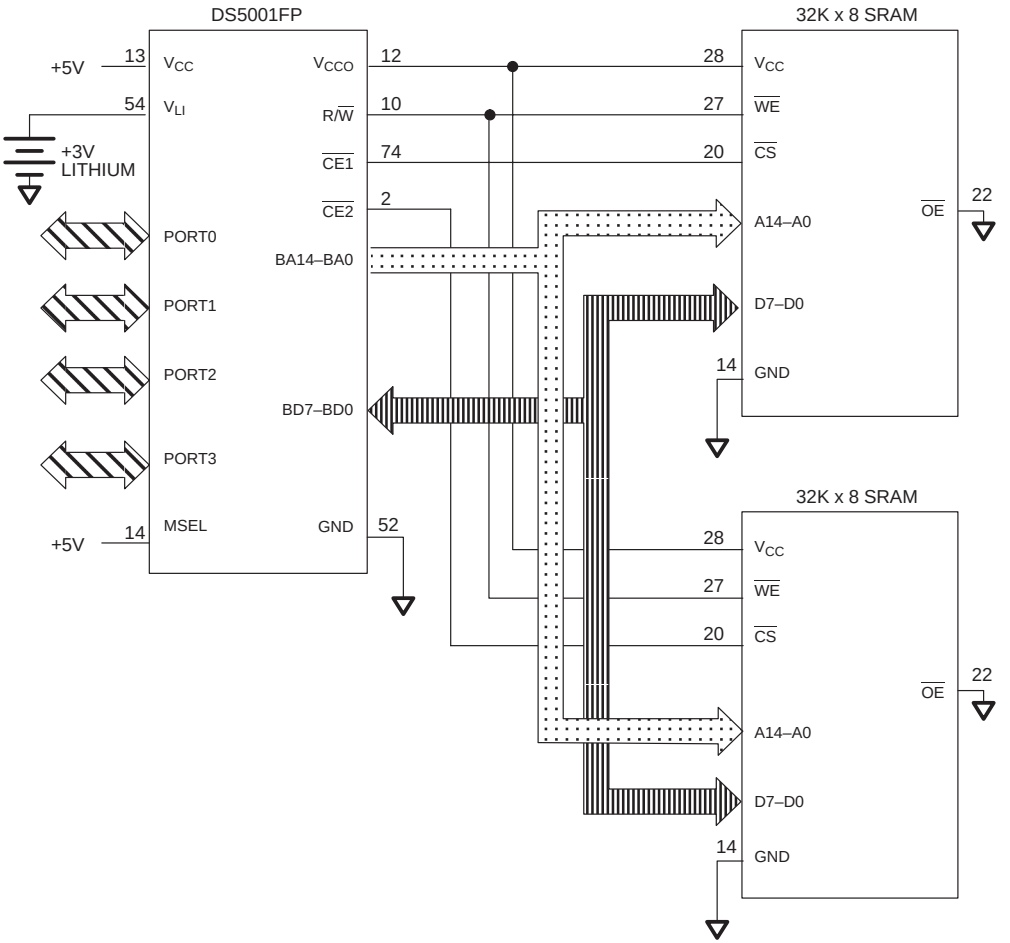


Figure 5 illustrates a typical memory connection for a system using a 128K byte SRAM. Note that in this configuration, both program and data are stored in a common RAM chip Figure 6 shows a similar system with using two 32K byte SRAMs. The Byte–wide Address bus connects to the SRAM address lines. The bi–directional Byte–wide data bus connects the data I/O lines of the SRAM.

DS5001FP CONNECTION TO 128K X 8 SRAM Figure 5



DS5001FP CONNECTION TO 64K X 8 SRAM Figure 6



POWER MANAGEMENT

The DS5001FP monitors V_{CC} to provide Power–fail Reset, early warning Power–fail Interrupt, and switch over to lithium backup. It uses an internal band–gap reference in determining the switch points. These are called V_{PFW}, V_{CCMIN}, and V_{LI} respectively. When V_{CC} drops below V_{PFW}, the DS5001FP will perform an interrupt vector to location 2Bh if the power fail warning was enabled. Full processor operation continues regardless. When power falls further to V_{CCMIN}, the DS5001FP invokes a reset state. No further code execution will be performed unless power rises back above V_{CCMIN}. All decoded chip enables and the R/$\overline{W}$ signal go to an inactive (logic 1) state. V_{CC} is still the power source at this time. When V_{CC} drops further to below V_{LI}, internal circuitry will switch to the lithium cell for power. The majority of internal circuits will be disabled and the remaining nonvolatile states will be retained. Any devices connected to V_{CCO} will be powered by the lithium cell at this time. V_{CCO} will be at the lithium battery voltage less a diode drop. This drop will vary depending on the load. Low power SRAMs should be used for this reason. When using the DS5001FP, the user must select the appropriate battery to match the RAM data retention current and the desired backup lifetime. Note that the lithium cell is only loaded when $V_{CC} < V_{LI}$. The User's Guide has more information on this topic. The trip points V_{CCMIN} and V_{PFW} are listed in the electrical specifications.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC CHARACTERISTICS

(t_A=0°C to 70°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Low Voltage	V_{IL}	–0.3		+0.8	V	1
Input High Voltage	V_{IH1}	2.0		V_{CC}+0.3	V	1
Input High Voltage (RST, XTAL1, $\overline{PROG}$)	V_{IH2}	3.5		V_{CC}+0.3	V	1
Output Low Voltage @ I_{OL}=1.6 mA (Ports 1, 2, 3)	V_{OL1}		0.15	0.45	V	
Output Low Voltage @ I_{OL}=3.2 mA (Port 0, ALE, $\overline{PSEN}$, $\overline{PF}$, BA15–0, BD7–0, R/$\overline{W}$, $\overline{CE1N}$, $\overline{CE}$1–4, $\overline{PE}$1–4, V_{RST})	V_{OL2}		0.15	0.45	V	1
Output High Voltage @ I_{OH}=–80 µA (Ports 1, 2, 3)	V_{OH1}	2.4	4.8		V	1
Output High Voltage @ I_{OH}=–400 µA (Ports 0, ALE, $\overline{PSEN}$, $\overline{PF}$, BA15–0, BD7–0, R/$\overline{W}$, $\overline{CE1N}$, $\overline{CE}$1–4, $\overline{PE}$1–4)	V_{OH2}	2.4	4.8		V	1
Input Low Current V_{IN}=0.45V (Ports 1, 2, 3)	I_{IL}			–50	µA	
Transition Current; 1 to 0 V_{IN}=2.0V (Ports 1, 2, 3) (0°C to 70°C)	I_{TL}			–500	µA	
Transition Current; 1 to 0 V_{IN}=2.0V (Ports 1, 2, 3) (–40°C to +85°C)	I_{TL}			–600	µA	10

DC CHARACTERISTICS (cont'd) (t_A=0°C to 70°C; V_{CC}=5V ± 10%)

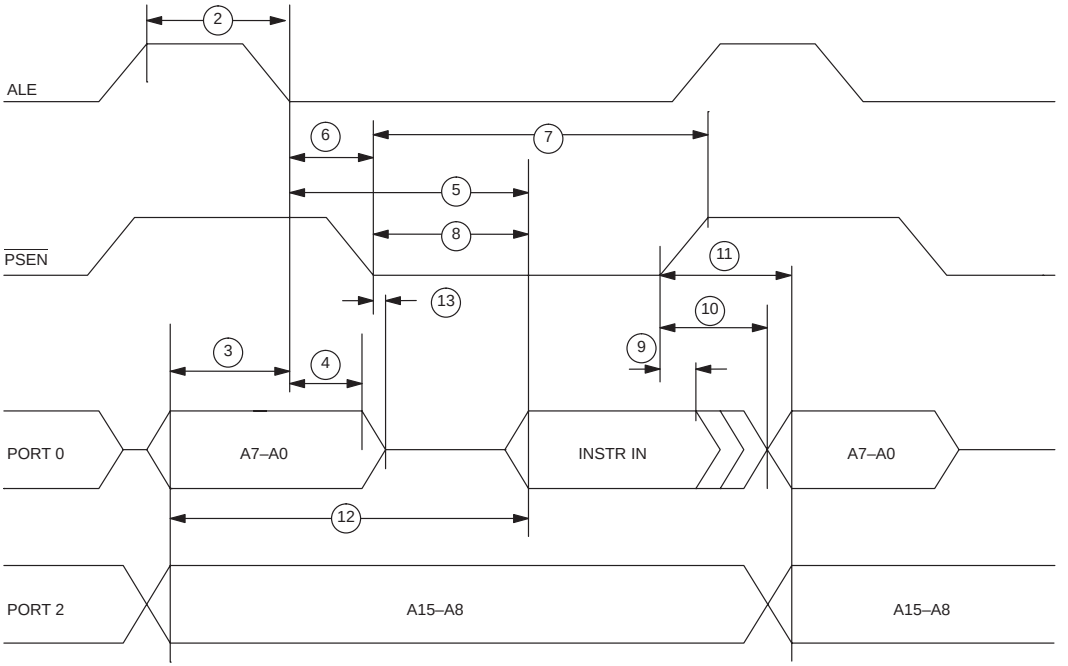
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current 0.45 < V_{IN} < V_{CC} (Port 0, MSEL)	I_{IL}			±10	µA	
RST Pull–down Resistor (0°C to 70°C)	R_{RE}	40		150	KΩ	
RST Pull–down Resistor (–40°C to +85°C)	R_{RE}	40		180	KΩ	10
$\overline{VRST}$ Pull–up Resistor	R_{VR}		4.7		KΩ	
$\overline{PROG}$ Pull–up Resistor	R_{PR}		40		KΩ	
Power–Fail Warning Voltage (0°C to 70°C)	V_{PFW}	4.25	4.37	4.50	V	1
Power–Fail Warning Voltage (–40°C to +85°C)	V_{PFW}	4.1	4.37	4.5	V	1, 10
Minimum Operating Voltage (0°C to 70°C)	V_{CCMIN}	4.00	4.12	4.25	V	1
Minimum Operating Voltage (–40°C to +85°C)	V_{CCMIN}	3.85	4.09	4.25	V	1, 10
Lithium Supply Voltage	V_{LI}	2.5		4.0	V	1
Operating Current @ 16 MHz	I_{CC}			36	mA	2
Idle Mode Current @ 12 MHz (0°C to 70°C)	I_{IDLE}			7.0	mA	3
Idle Mode Current @ 12 MHz (–40°C to +85°C)	I_{IDLE}			8.0	mA	3, 10
Stop Mode Current	I_{STOP}			80	µA	4
Pin Capacitance	C_{IN}			10	pF	5
Output Supply Voltage (V_{CCO})	V_{CCO1}	V_{CC}–0.35			V	1, 2
Output Supply Battery–backed Mode (V_{CCO}, $\overline{CE}$1–4, $\overline{PE}$1–2) (0°C to 70°C)	V_{CCO2}	V_{LI}–0.65			V	1, 8
Output Supply Battery–backed Mode (V_{CCO}, $\overline{CE}$1–4, $\overline{PE}$1–2) (–40°C to +85°C)	V_{CCO2}	V_{LI}–0.9			V	1, 8, 10
Output Supply Current @ V_{CCO}=V_{CC} – 0.3V	I_{CCO1}			75	mA	6
Lithium–backed Quiescent Current	I_{LI}		5	75	nA	7
Reset Trip Point in Stop Mode w/BAT=3.0V (0°C to 70°C) w/BAT=3.0V (–40°C to +85°C) w/BAT=3.3V (0°C to 70°C)		 4.0 3.85 4.4		 4.25 4.25 4.65		 1 1, 10 1

AC CHARACTERISTICS
EXPANDED BUS MODE TIMING SPECIFICATIONS

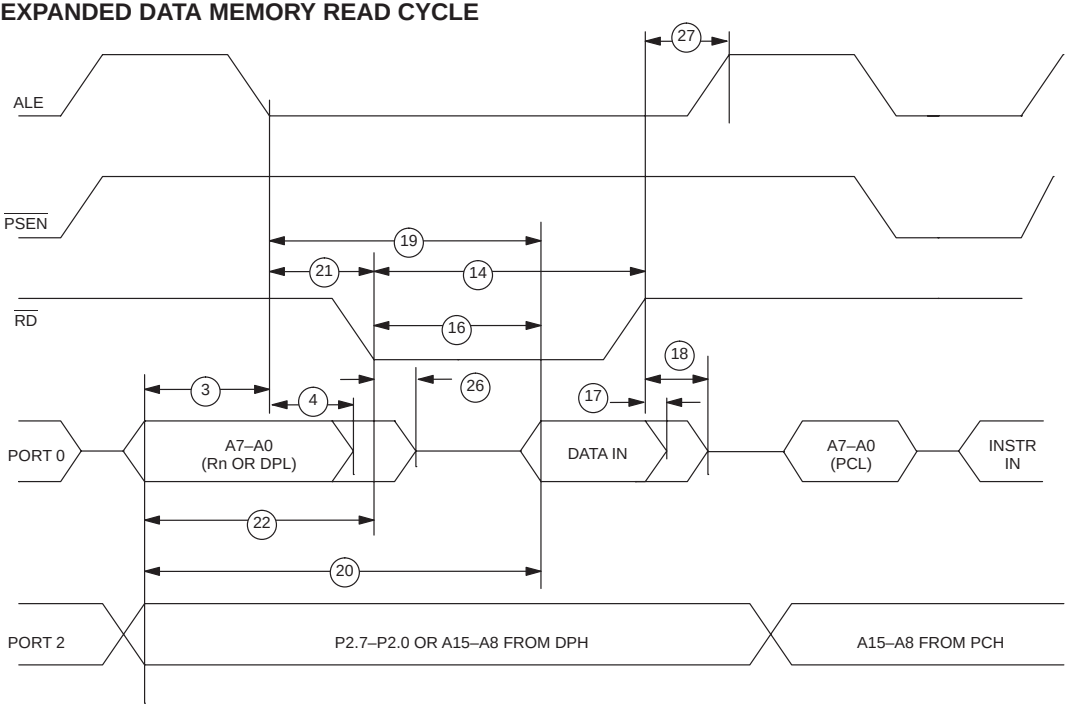
(t_A=0°C to70°C; V_{CC}=5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
1	Oscillator Frequency	$1/t_{CLK}$	1.0	16	MHz
2	ALE Pulse Width	t_{ALPW}	$2t_{CLK}$–40		ns
3	Address Valid to ALE Low	t_{AVALL}	t_{CLK}–40		ns
4	Address Hold After ALE Low	t_{AVAAV}	t_{CLK}–35		ns
5	ALE Low to Valid Instr. In @12 MHz @16 MHz	t_{ALLVI}		$4t_{CLK}$–150 $4t_{CLK}$–90	ns
6	ALE Low to $\overline{PSEN}$ Low	t_{ALLPSL}	t_{CLK}–25		ns
7	$\overline{PSEN}$ Pulse Width	t_{PSPW}	$3t_{CLK}$–35		ns
8	$\overline{PSEN}$ Low to Valid Instr. In @12 MHz @16 MHz	t_{PSLVI}		$3t_{CLK}$–150 $3t_{CLK}$–90	ns ns
9	Input Instr. Hold after $\overline{PSEN}$ Going High	t_{PSIV}	0		ns
10	Input Instr. Float after $\overline{PSEN}$ Going High	t_{PSIX}		t_{CLK}–20	ns
11	Address Hold after $\overline{PSEN}$ Going High	t_{PSAV}	t_{CLK}–8		ns
12	Address Valid to Valid Instr. In @12 MHz @16 MHz	t_{AVVI}		$5t_{CLK}$–150 $5t_{CLK}$–90	ns ns
13	$\overline{PSEN}$ Low to Address Float	t_{PSLAZ}	0		ns
14	$\overline{RD}$ Pulse Width	t_{RDPW}	$6t_{CLK}$–100		ns
15	$\overline{WR}$ Pulse Width	t_{WRPW}	$6t_{CLK}$–100		ns
16	$\overline{RD}$ Low to Valid Data In @12 MHz @16 MHz	t_{RDLDV}		$5t_{CLK}$–165 $5t_{CLK}$–105	ns ns
17	Data Hold after $\overline{RD}$ High	t_{RDHDV}	0		ns
18	Data Float after $\overline{RD}$ High	t_{RDHDZ}		$2t_{CLK}$–70	ns
19	ALE Low to Valid Data In @12 MHz @16 MHz	t_{ALLVD}		$8t_{CLK}$–150 $8t_{CLK}$–90	ns ns
20	Valid Addr. to Valid Data In @12 MHz @16 MHz	t_{AVDV}		$9t_{CLK}$–165 $9t_{CLK}$–105	ns ns
21	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{ALLRDL}	$3t_{CLK}$–50	$3t_{CLK}$+50	ns
22	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVRDL}	$4t_{CLK}$–130		ns
23	Data Valid to $\overline{WR}$ Going Low	t_{DVWRL}	t_{CLK}–60		ns
24	Data Valid to $\overline{WR}$ High @12 MHz @16 MHz	t_{DVWRH}	$7t_{CLK}$–150 $7t_{CLK}$–90		ns ns
25	Data Valid after $\overline{WR}$ High	t_{WRHDV}	t_{CLK}–50		ns
26	$\overline{RD}$ Low to Address Float	t_{RDLAZ}		0	ns
27	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{RDHALH}	t_{CLK}–40	t_{CLK}+50	ns

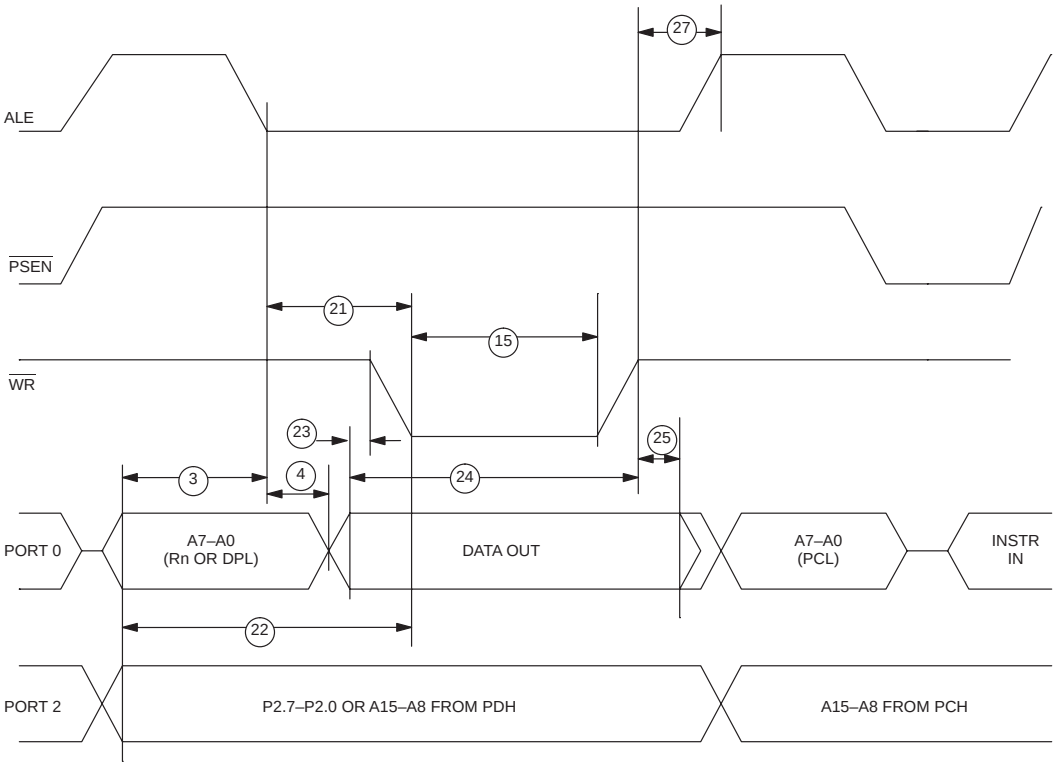
EXPANDED PROGRAM MEMORY READ CYCLE



EXPANDED DATA MEMORY READ CYCLE



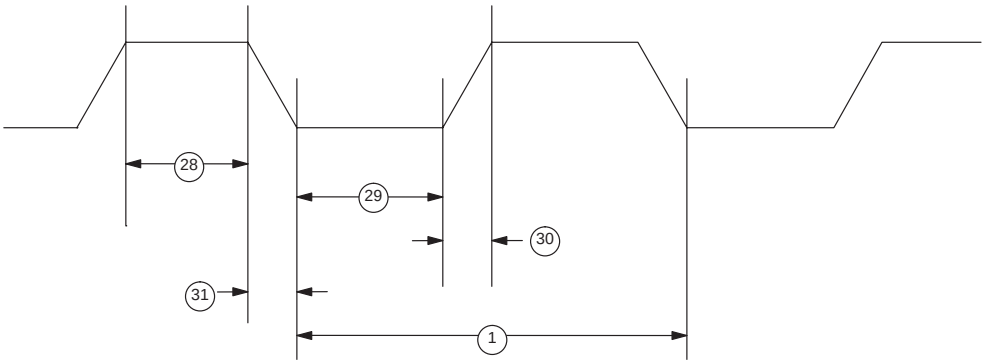
EXPANDED DATA MEMORY WRITE CYCLE



AC CHARACTERISTICS (cont'd)
EXTERNAL CLOCK DRIVE (t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER		SYMBOL	MIN	MAX	UNITS
28	External Clock High Time	@12 MHz @16 MHz	t_{CLKHPW}	20 15		ns ns
29	External Clock Low Time	@12 MHz @16 MHz	t_{CLKLPW}	20 15		ns ns
30	External Clock Rise Time	@12 MHz @16 MHz	t_{CLKR}		20 15	ns ns
31	External Clock Fall Time	@12 MHz @16 MHz	t_{CLKF}		20 15	ns ns

EXTERNAL CLOCK TIMING



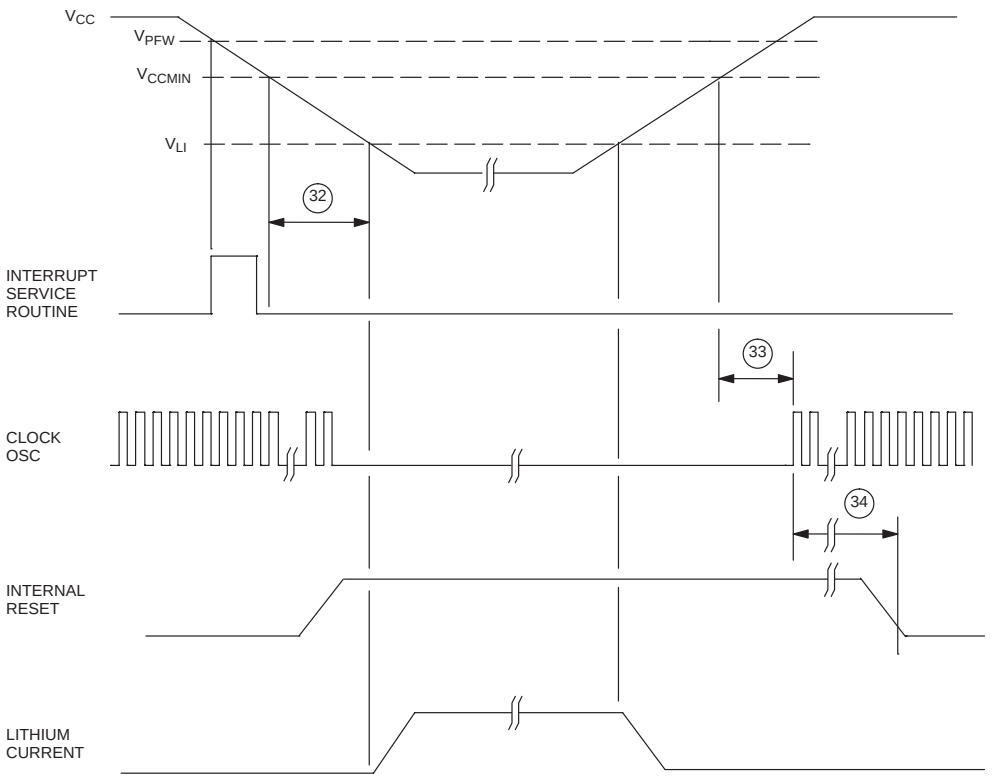
AC CHARACTERISTICS (cont'd)

POWER CYCLING TIMING

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
32	Slew Rate from V_{CCmin} to V_{LI}	t_F	130		µs
33	Crystal Start–up Time	t_{CSU}		(note 9)	
34	Power–On Reset Delay	t_{POR}		21504	t_{CLK}

POWER CYCLE TIMING

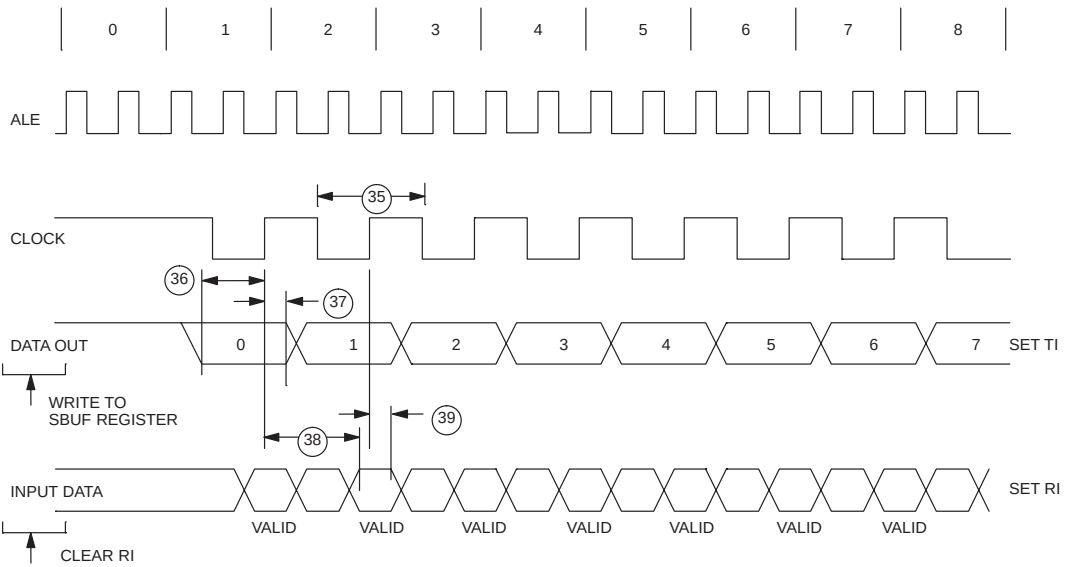


AC CHARACTERISTICS (cont'd)
SERIAL PORT TIMING – MODE 0

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
35	Serial Port Clock Cycle Time	t_{SPCLK}	$12t_{CLK}$		µs
36	Output Data Setup to Rising Clock Edge	t_{DOCH}	$10t_{CLK}$–133		ns
37	Output Data Hold after Rising Clock Edge	t_{CHDO}	$2t_{CLK}$–117		ns
38	Clock Rising Edge to Input Data Valid	t_{CHDV}		$10t_{CLK}$–133	ns
39	Input Data Hold after Rising Clock Edge	t_{CHDIV}	0		ns

SERIAL PORT TIMING – MODE 0

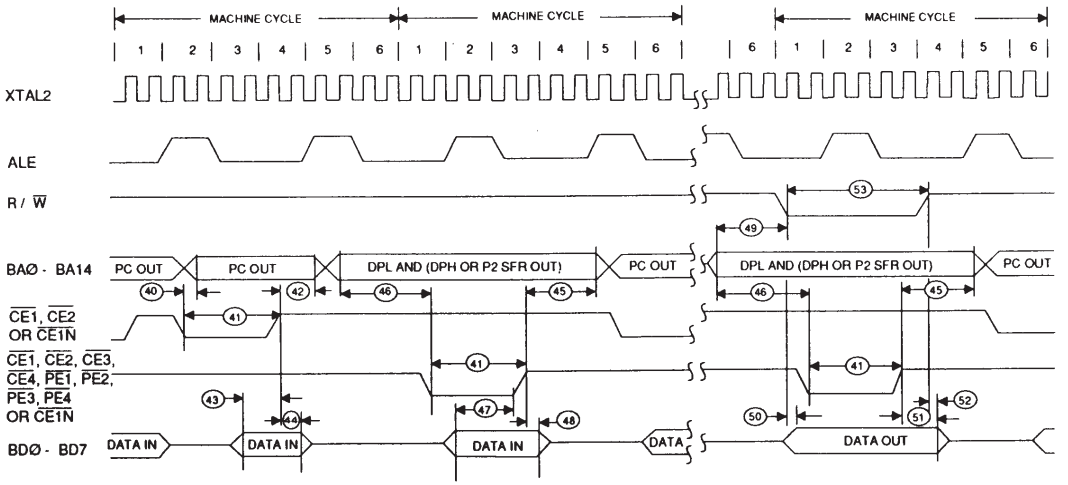


AC CHARACTERISTICS
BYTEWIDE ADDRESS/DATA BUS TIMING

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
40	Delay to Byte–wide Address Valid from $\overline{CE1}$, $\overline{CE2}$ or $\overline{CE1N}$ Low During Opcode Fetch	t_{CE1LPA}		30	ns
41	Pulse Width of $\overline{CE}$1–4, $\overline{PE}$1–4 or $\overline{CE1N}$	t_{CEPW}	$4t_{CLK}$–35		ns
42	Byte–wide Address Hold After $\overline{CE1}$, $\overline{CE2}$ or $\overline{CE1N}$ High During Opcode Fetch	t_{CE1HPA}	$2t_{CLK}$–20		ns
43	Byte–wide Data Setup to $\overline{CE1}$, $\overline{CE2}$ or $\overline{CE1N}$ High During Opcode Fetch	t_{OVCE1H}	$1t_{CLK}$+40		ns
44	Byte–wide Data Hold After $\overline{CE1}$, $\overline{CE2}$ or $\overline{CE1N}$ High During Opcode Fetch	t_{CE1HOV}	10		ns
45	Byte–wide Address Hold After $\overline{CE}$1–4, $\overline{PE}$1–4, or $\overline{CE1N}$ High During MOVX	t_{CEHDA}	$4t_{CLK}$–30		ns
46	Delay from Bytewide Address Valid $\overline{CE}$1–4, $\overline{PE}$1–4, or $\overline{CE1N}$ Low During MOVX	t_{CELDA}	$4t_{CLK}$–35		ns
47	Bytewide Data Setup to $\overline{CE}$1–4, $\overline{PE}$1–4, or $\overline{CE1N}$ High During MOVX (read)	t_{DACEH}	$1t_{CLK}$+40		ns
48	Bytewide Data Hold After $\overline{CE}$1–4, $\overline{PE}$1–4, or $\overline{CE1N}$ High During MOVX (read)	t_{CEHDV}	10		ns
49	Bytewide Address Valid to R/$\overline{W}$ Active During MOVX (write)	t_{AVRWL}	$3t_{CLK}$–35		ns
50	Delay from R/$\overline{W}$ Low to Valid Data Out During MOVX (write)	t_{RWLDV}	20		ns
51	Valid Data Out Hold Time from $\overline{CE}$1–4, $\overline{PE}$1–4, or $\overline{CE1N}$ High	t_{CEHDV}	$1t_{CLK}$–15		ns
52	Valid Data Out Hold Time from R/$\overline{W}$ High	t_{RWHDV}	0		ns
53	Write Pulse Width (R/$\overline{W}$ Low Time)	t_{RWLPW}	$6t_{CLK}$–20		ns

BYTEWIDE BUS TIMING



RPC AC CHARACTERISTICS – DBB READ

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
54	$\overline{CS}$, A_0 Setup to $\overline{RD}$	t_{AR}	0		ns
55	$\overline{CS}$, A_0 Hold After $\overline{RD}$	t_{RA}	0		ns
56	$\overline{RD}$ Pulse Width	t_{RR}	160		ns
57	$\overline{CS}$, A_0 to Data Out Delay	t_{AD}		130	ns
58	$\overline{RD}$ to Data Out Delay	t_{RD}	0	130	ns
59	$\overline{RD}$ to Data Float Delay	t_{RDZ}		85	ns

RPC AC CHARACTERISTICS – DBB WRITE (t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
60	$\overline{CS}$, A_0 Setup to $\overline{WR}$	t_{AW}	0		ns
61A	$\overline{CS}$, Hold After $\overline{WR}$	t_{WA}	0		ns
61B	A_0, Hold After $\overline{WR}$	t_{WA}	20		ns
62	$\overline{WR}$ Pulse Width	t_{WW}	160		ns
63	Data Setup to $\overline{WR}$	t_{DW}	130		ns
64	Data Hold After $\overline{WR}$	t_{WD}	20		ns

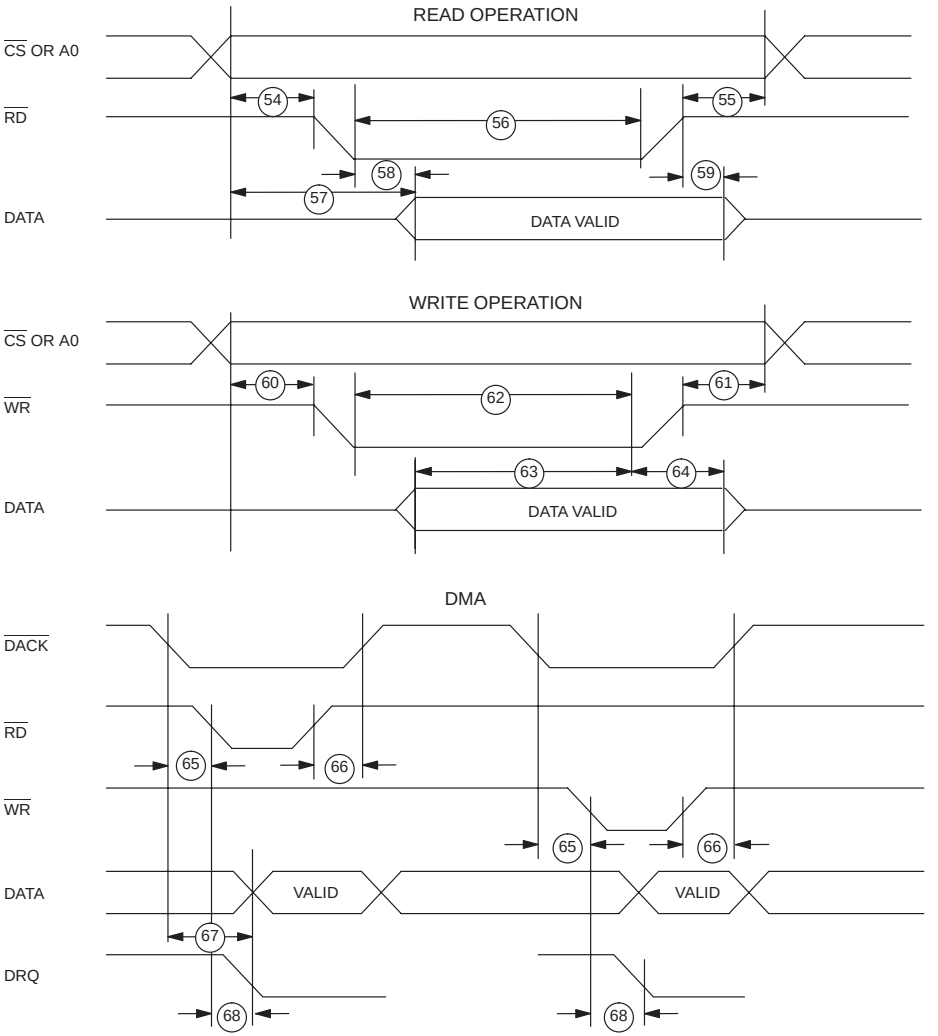
AC CHARACTERISTICS – DMA (t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
65	$\overline{DACK}$ to $\overline{WR}$ or $\overline{RD}$	t_{ACC}	0		ns
66	$\overline{RD}$ or $\overline{WR}$ to $\overline{DACK}$	t_{CAC}	0		ns
67	$\overline{DACK}$ to Data Valid	t_{ACD}	0	130	ns
68	$\overline{RD}$ or $\overline{WR}$ to DRQ Cleared	t_{CRQ}		110	ns

AC CHARACTERISTICS – $\overline{PROG}$ (t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
69	$\overline{PROG}$ Low to Active	t_{PRA}	48		CLKS
70	$\overline{PROG}$ High to Inactive	t_{PRI}	48		CLKS

RPC TIMING MODE

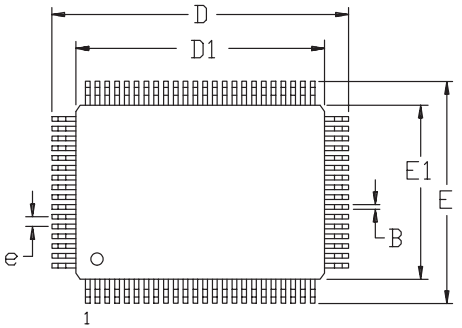


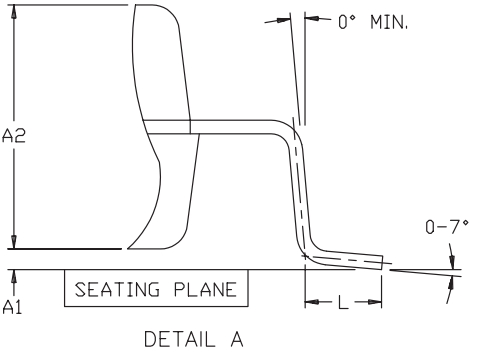
NOTES:
All parameters apply to both commercial and industrial temperature operation unless otherwise noted.

4. All voltages are referenced to ground.
5. Maximum operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF}=10 ns, V_{IL} = 0.5V; XTAL2 disconnected; RST = PORT0 = V_{CC}, MSEL = V_{SS}.
6. Idle mode I_{IDLE} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF} = 10 ns, V_{IL} = 0.5V; XTAL2 disconnected; PORT0 = V_{CC}, RST = MSEL = V_{SS}.
7. Stop mode I_{STOP} is measured with all output pins disconnected; PORT0 = V_{CC}; XTAL2 not connected; RST = MSEL = XTAL1 = V_{SS}.

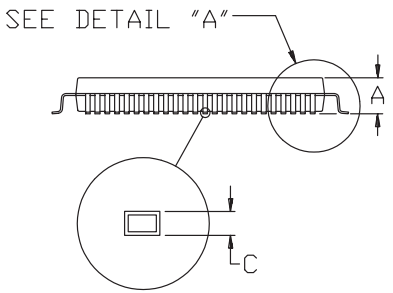
8. Pin Capacitance is measured with a test frequency – 1 MHz, t_A = 25°C.
9. I_{CCO1} is the maximum average operating current that can be drawn from V_{CCO} in normal operation.
10. I_{LI} is the current drawn from V_{LI} input when V_{CC} = 0V and V_{CCO} is disconnected.
11. V_{CCO2} is measured with $V_{CC} < V_{LI}$, and a maximum load of 10 µA on V_{CCO}.
12. Crystal start–up time is the time required to get the mass of the crystal into vibrational motion from the time that power is first applied to the circuit until the first clock pulse is produced by the on–chip oscillator. The user should check with the crystal vendor for a worst case specification on this time.
13. This parameter applies to industrial temperature operation.

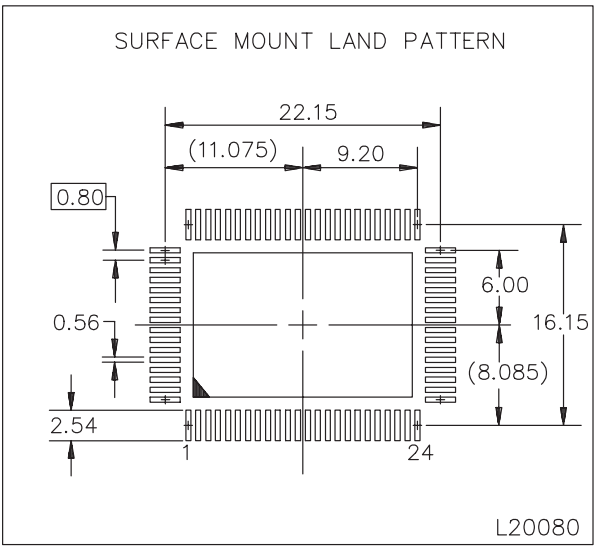
DS50001FP CMOS MICROPROCESSOR





DETAIL A





DIM	MILLIMETERS	
	MIN	MAX
A	–	3.15
A1	0.25	–
A2	2.55	2.87
B	0.30	0.50
C	0.13	0.23
D	23.70	24.10
D1	19.90	20.10
E	17.40	18.10
E1	13.90	14.10
e	0.80 BSC	
L	0.65	0.95

56–G4005–001

DATA SHEET REVISION SUMMARY

The following represent the key differences between 11/27/95 and 07/24/96 version of the DS50001FP data sheet. Please review this summary carefully.

1. Change V_{CC02} specification from V_{LI} – 0.5 to V_{LI} – 0.65 (PCN F62501).
2. Update mechanical specifications.

The following represent the key differences between 07/24/96 and 11/19/96 version of the DS50001FP data sheet. Please review this summary carefully.

1. Change V_{CC01} from V_{CC}–0.3 to V_{CC}–0.35.

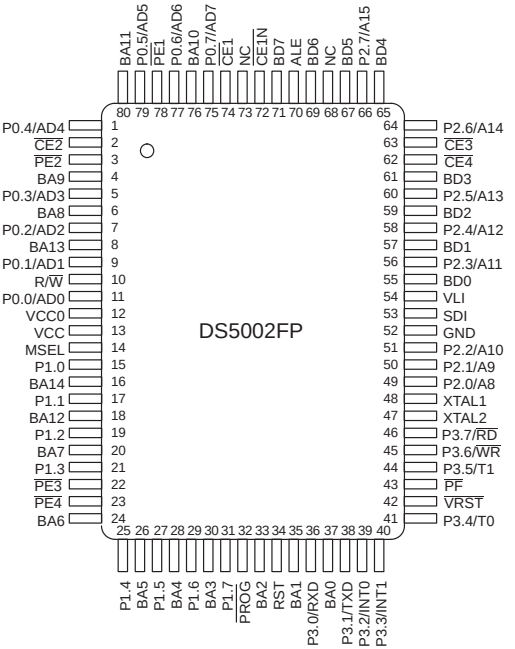
DALLAS SEMICONDUCTOR

DS5002FP
Secure Microprocessor Chip

FEATURES

- 8051 compatible microprocessor for secure/sensitive applications
  - Access 32K, 64K, or 128K bytes of nonvolatile SRAM for program and/or data storage
  - In–system programming via on–chip serial port
  - Capable of modifying its own program or data memory in the end system
- Firmware Security Features:
  - Memory stored in encrypted form
  - Encryption using on–chip 64–bit key
  - Automatic true random key generator
  - SDI Self Destruct Input
  - Optional top coating prevents microprobe (DS5002FPM)
  - Improved security over previous generations
  - Protects memory contents from piracy
- Crashproof Operation
  - Maintains all nonvolatile resources for over 10 years in the absence of power
  - Power–fail Reset
  - Early Warning Power–fail Interrupt
  - Watchdog Timer

PIN ASSIGNMENT



DESCRIPTION

The DS5002FP Secure Microprocessor Chip is a secure version of the DS5001FP 128K Soft Microprocessor Chip. In addition to the memory and I/O enhancements of the DS5001FP, the Secure Microprocessor Chip incorporates the most sophisticated security features available in any processor. The security features of the DS5002FP include an array of mechanisms which are designed to resist all levels of threat, including observation, analysis, and physical attack. As a result, a massive effort would be required to obtain any information about memory contents. Furthermore, the "soft" nature of the DS5002FP allows frequent modification of the secure information, thereby minimizing the value of any secure information obtained by such a massive effort.

The DS5002FP implements a security system which is an improved version of its predecessor, the DS5000FP. Like the DS5000FP, the DS5002FP loads and executes application software in encrypted form. Up to 128K x 8 bytes of standard SRAM can be accessed via its Byte–wide bus. This RAM is converted by the DS5002FP into lithium–backed nonvolatile storage for program and data. Data is maintained for over 10 years at room temperature with a very small lithium cell. As a result, the contents of the RAM and the execution of the software

appear unintelligible to the outside observer. The encryption algorithm uses an internally stored and protected key. Any attempt to discover the key value results in its erasure, rendering the encrypted contents of the RAM useless.

The Secure Microprocessor Chip offers a number of major enhancements to the software security implemented in the previous generation DS5000FP. First, the DS5002FP provides a stronger software encryption algorithm which incorporates elements of DES encryption. Second, the encryption is based on a 64–bit key word, as compared to the DS5000FP's 40–bit key. Third, the key can only be loaded from an on–chip true random number generator. As a result, the true key value is never known by the user. Fourth, a Self–Destruct input pin (SDI) is provided to interface to external tamper detection circuitry. With or without the presence of V_{CC}, activation of the SDI pin has the same effect as resetting the Security Lock: immediate erasure of the key word and the 48–byte Vector RAM area. Fifth, an optional top–coating of the die prevents access of information using microprobing techniques. Finally, customer–specific versions of the DS5002FP are available which incorporate a one–of–a–kind encryption algorithm.

When implemented as a part of a secure system design, a system based on the DS5002FP can typically provide a level of security which requires more time and resources to defeat than it is worth to unauthorized individuals who have reason to try. For a user who wants a pre–constructed module using the DS5002FP, RAM, lithium cell, and a real time clock, the DS2252T is available and described in a separate data sheet.

ORDERING INFORMATION

The following devices are available as standard products from Dallas Semiconductor:

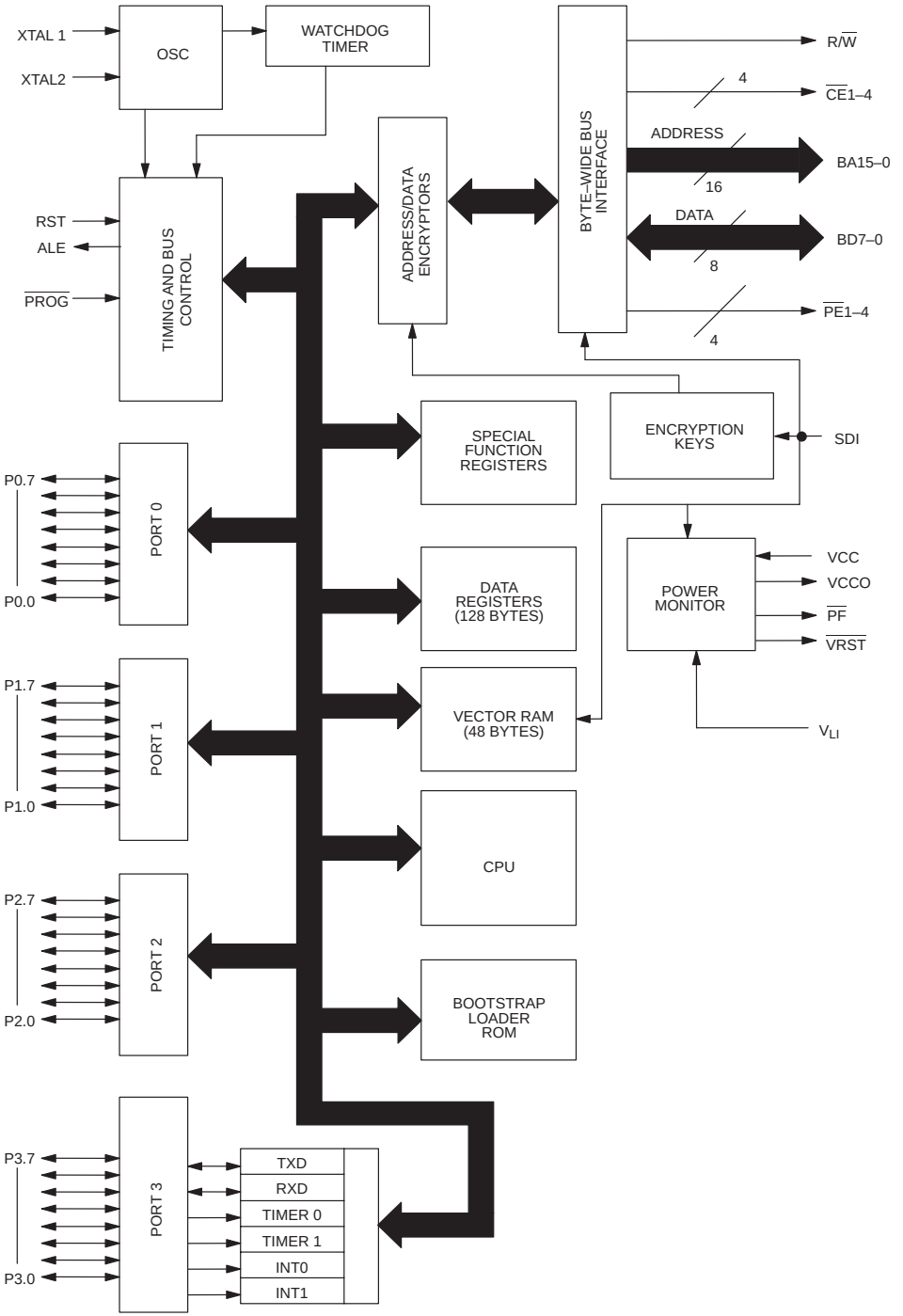
PART #	DESCRIPTION
DS5002FP–16	80–pin QFP, Max. clock speed 16 MHz, 0°C to 70°C operation
DS5002FPM–16	80–pin QFP, Max. clock speed 16 MHz, 0°C to 70°C operation, Internal microprobe shield

Operating information is contained in the User's Guide Section of the Secure Microprocessor Data Book. This data sheet provides ordering information, pin–out, and electrical specifications.

BLOCK DIAGRAM

Figure 1 is a block diagram illustrating the internal architecture of the DS5002FP. The DS5002FP is a secure implementation of the DS5001FP 128K Soft Microprocessor Chip. As a result, It operates in an identical fashion to the DS5001FP except where indicated. See the DS5001FP Data Sheet for operating details.

DS5002FP BLOCK DIAGRAM Figure 1



PIN DESCRIPTION

PIN	DESCRIPTION
11, 9, 7, 5, 1, 79, 77, 75	**P0.0 – P0.7.** General purpose I/O Port 0. This port is open–drain and can not drive a logic 1. It requires external pull–ups. Port 0 is also the multiplexed Expanded Address/Data bus. When used in this mode, it does not require pull–ups.
15, 17, 19, 21, 25, 27, 29, 31	**P1.0 – P1.7.** General purpose I/O Port 1.
49, 50, 51, 56, 58, 60, 64, 66	**P2.0 – P2.7.** General purpose I/O Port 2. Also serves as the MSB of the Expanded Address bus.
36	**P3.0 RXD.** General purpose I/O port pin 3.0. Also serves as the receive signal for the on board UART. This pin should NOT be connected directly to a PC COM port.
38	**P3.1 TXD.** General purpose I/O port pin 3.1. Also serves as the transmit signal for the on board UART. This pin should NOT be connected directly to a PC COM port.
39	**P3.2 $\overline{\text{INT0}}$.** General purpose I/O port pin 3.2. Also serves as the active low External Interrupt 0.
40	**P3.3 $\overline{\text{INT1}}$.** General purpose I/O port pin 3.3. Also serves as the active low External Interrupt 1.
41	**P3.4 T0.** General purpose I/O port pin 3.4. Also serves as the Timer 0 input.
44	**P3.5 T1.** General purpose I/O port pin 3.5. Also serves as the Timer 1 input.
45	**P3.6 $\overline{\text{WR}}$.** General purpose I/O port pin. Also serves as the write strobe for Expanded bus operation.
46	**P3.7 $\overline{\text{RD}}$.** General purpose I/O port pin. Also serves as the read strobe for Expanded bus operation.
34	**RST –** Active high reset input. A logic 1 applied to this pin will activate a reset state. This pin is pulled down internally so this pin can be left unconnected if not used. An RC power–on reset circuit is not needed and is NOT recommended.
70	**ALE –** Address Latch Enable. Used to de–multiplex the multiplexed Expanded Address/Data bus on Port 0. This pin is normally connected to the clock input on a '373 type transparent latch.
47, 48	**XTAL2, XTAL1.** Used to connect an external crystal to the internal oscillator. XTAL1 is the input to an inverting amplifier and XTAL2 is the output.
52	**GND –** Logic ground.
13	**V_{CC} –** +5V
12	**V_{CCO} –** V_{CC} Output. This is switched between V_{CC} and V_{LI} by internal circuits based on the level of V_{CC}. When power is above the lithium input, power will be drawn from V_{CC}. The lithium cell remains isolated from a load. When V_{CC} is below V_{LI}, the V_{CCO} switches to the V_{LI} source. V_{CCO} should be connected to the V_{CC} pin of an SRAM.
54	**V_{LI} –** Lithium Voltage Input. Connect to a lithium cell greater than V_{LImin} and no greater than V_{LImax} as shown in the electrical specifications. Nominal value is +3V.
16, 8, 18, 80, 76, 4, 6, 20, 24, 26, 28, 30, 33, 35, 37	**BA14 – 0.** Byte–wide Address bus bits 14–0. This bus is combined with the non–multiplexed data bus (BD7–0) to access NVSRAM. Decoding is performed using $\overline{\text{CE1}}$ through $\overline{\text{CE4}}$. Therefore, BA15 is not actually needed. Read/write access is controlled by R/$\overline{\text{W}}$. BA14–0 connect directly to an 8K, 32K, or 128K SRAM. If an 8K RAM is used, BA13 and BA14 will be unconnected. If a 128K SRAM is used, the micro converts $\overline{\text{CE2}}$ and $\overline{\text{CE3}}$ to serve as A16 and A15 respectively.

PIN	DESCRIPTION
71, 69, 67, 65, 61, 59, 57, 55	**BD7 – 0.** Byte–wide Data bus bits 7–0. This 8–bit bi–directional bus is combined with the non–multiplexed address bus (BA14–0) to access NV SRAM. Decoding is performed on $\overline{CE1}$ and $\overline{CE2}$. Read/write access is controlled by R/$\overline{W}$. BD7–0 connect directly to an SRAM, and optionally to a Real–time Clock or other peripheral.
10	**R/$\overline{W}$** – Read/Write. This signal provides the write enable to the SRAMs on the Byte–wide bus. It is controlled by the memory map and Partition. The blocks selected as Program (ROM) will be write protected.
74	**$\overline{CE1}$** – Chip Enable 1. This is the primary decoded chip enable for memory access on the Byte–wide bus. It connects to the chip enable input of one SRAM. $\overline{CE1}$ is lithium backed. It will remain in a logic high inactive state when V_{CC} falls below V_{LI}.
2	**$\overline{CE2}$** – Chip Enable 2. This chip enable is provided to access a second 32K block of memory. It connects to the chip enable input of one SRAM. When MSEL=0, the micro converts $\overline{CE2}$ into A16 for a 128K x 8 SRAM. $\overline{CE2}$ is lithium backed and will remain at a logic high when V_{CC} falls below V_{LI}.
63	**$\overline{CE3}$** – Chip Enable 3. This chip enable is provided to access a third 32K block of memory. It connects to the chip enable input of one SRAM. When MSEL=0, the micro converts $\overline{CE3}$ into A15 for a 128K x 8 SRAM. $\overline{CE3}$ is lithium backed and will remain at a logic high when V_{CC} falls below V_{LI}.
62	**$\overline{CE4}$** – Chip Enable 4. This chip enable is provided to access a fourth 32K block of memory. It connects to the chip enable input of one SRAM. When MSEL=0, this signal is unused. $\overline{CE4}$ is lithium backed and will remain at a logic high when V_{CC} falls below V_{LI}.
78	**$\overline{PE1}$** – Peripheral Enable 1. Accesses data memory between addresses 0000h and 3FFFh when the PES bit is set to a logic 1. Commonly used to chip enable a Byte–wide Real Time Clock such as the DS1283. $\overline{PE1}$ is lithium backed and will remain at a logic high when V_{CC} falls below V_{LI}. Connect $\overline{PE1}$ to battery backed functions only.
3	**$\overline{PE2}$** – Peripheral Enable 2. Accesses data memory between addresses 4000h and 7FFFh when the PES bit is set to a logic 1. $\overline{PE2}$ is lithium backed and will remain at a logic high when V_{CC} falls below V_{LI}. Connect $\overline{PE2}$ to battery backed functions only.
22	**$\overline{PE3}$** – Peripheral Enable 3. Accesses data memory between addresses 8000h and BFFFh when the PES bit is set to a logic 1. $\overline{PE3}$ is not lithium backed and can be connected to any type of peripheral function. If connected to a battery backed chip, it will need additional circuitry to maintain the chip enable in an inactive state when $V_{CC} < V_{LI}$.
23	**$\overline{PE4}$** – Peripheral Enable 4. Accesses data memory between addresses C000h and FFFFh when the PES bit is set to a logic 1. $\overline{PE4}$ is not lithium backed and can be connected to any type of peripheral function. If connected to a battery backed chip, it will need additional circuitry to maintain the chip enable in an inactive state when $V_{CC} < V_{LI}$.
32	**$\overline{PROG}$** – Invokes the Bootstrap Loader on a falling edge. This signal should be debounced so that only one edge is detected. If connected to ground, the micro will enter Bootstrap loading on power up. This signal is pulled up internally.
42	**$\overline{VRST}$** – This I/O pin (open drain with internal pull–up) indicates that the power supply (V_{CC}) has fallen below the V_{CCmin} level and the micro is in a reset state. When this occurs, the DS5002FP will drive this pin to a logic 0. Because the micro is lithium backed, this signal is guaranteed even when V_{CC}=0V. Because it is an I/O pin, it will also force a reset if pulled low externally. This allows multiple parts to synchronize their power–down resets.
43	**$\overline{PF}$** – This output goes to a logic 0 to indicate that the micro has switched to lithium backup. This corresponds to $V_{CC} < V_{LI}$. Because the micro is lithium backed, this signal is guaranteed even when V_{CC}=0V. The normal application of this signal is to control lithium powered current to isolate battery backed functions from non–battery backed functions.

PIN	DESCRIPTION
14	**MSEL** – Memory select. This signal controls the memory size selection. When MSEL= +5V, the DS5002FP expects to use 32K x 8 SRAMs. When MSEL = 0V, the DS5002FP expects to use a 128K x 8 SRAM. MSEL must be connected regardless of Partition, Mode, etc.
53	**SDI** – Self–Destruct Input. An active high on this pin causes an unlock procedure. This results in the destruction of Vector RAM, Encryption Keys, and the loss of power from V_{CCO}. This pin should be grounded if not used.
72	**$\overline{\text{CE1N}}$** – This is a non–battery backed version of $\overline{\text{CE1}}$. It is not generally useful since the DS5002FP can not be used with EPROM due to its encryption.
73	**NC** – Do not connect.

SECURE OPERATION OVERVIEW

The DS5002FP incorporates encryption of the activity on its Byte–wide Address/Data bus to prevent unauthorized access to the program and data information contained in the nonvolatile RAM. Loading an application program in this manner is performed via the Bootstrap Loader using the general sequence described below:

1. Clear Security Lock
2. Set memory map configuration as for DS5001FP
3. Load application software
4. Set Security Lock
5. Exit Loader

Loading of application software into the program/data RAM is performed while the DS5002FP is in its Bootstrap Load mode. Loading is only possible when the Security Lock is clear. If the Security Lock has previously set, then it must be cleared by issuing the “Z” command from the Bootstrap Loader. Resetting the Security Lock instantly clears the previous key word and the contents of the Vector RAM. In addition, the Bootstrap ROM writes zeroes into the first 32K of external RAM.

The user’s application software is loaded into external CMOS SRAM via the “L” command in “scrambled” form through on–chip encryptor circuits. Each external RAM address is an encrypted representation of an on–chip logical address. Thus, the sequential instructions of an ordinary program or data table are stored non–sequentially in RAM memory. The contents of the program/data RAM are also encrypted. Each byte in RAM is encrypted by a key– and address–dependent encryptor circuit such that identical bytes are stored as different values in different memory locations.

The encryption of the program/data RAM is dependent on an on–chip 64–bit key word. The key is loaded by the ROM firmware just prior to the time that the application software is loaded, and is retained as nonvolatile information in the absence of V_{CC} by the lithium backup circuits. After loading is complete, the key is protected by setting the on–chip Security Lock, which is also retained as nonvolatile information in the absence of V_{CC}. Any attempt to tamper with the key word and thereby gain access to the true program/data RAM contents results in the erasure of the key word as well as the RAM contents.

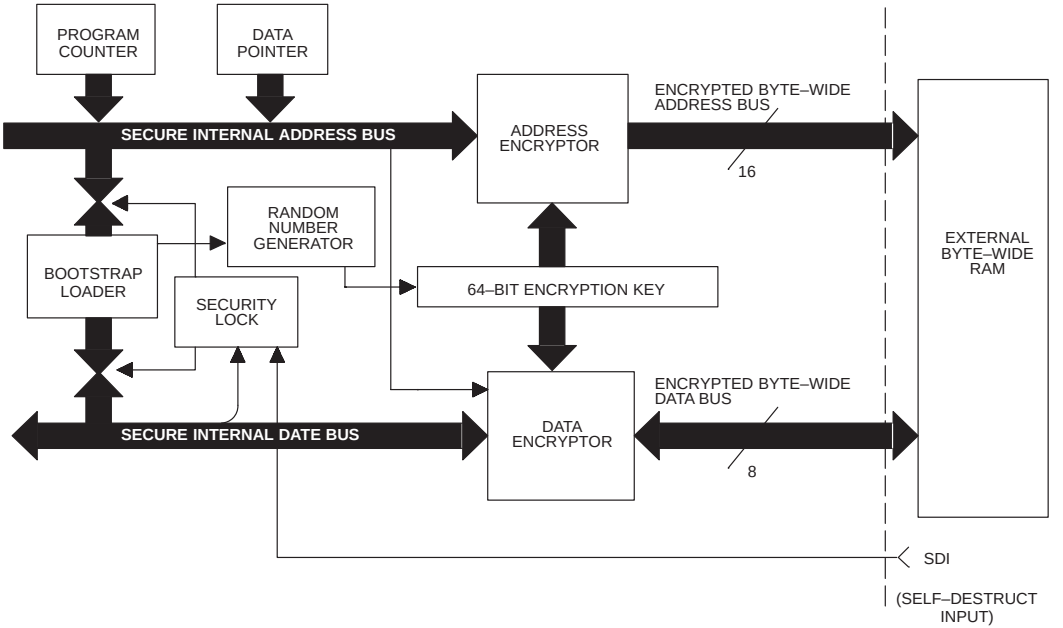
During execution of the application software, logical addresses on the DS5002FP that are generated from the program counter or data pointer registers are encrypted before they are presented on the Byte–wide Address Bus. Opcodes and data are read back and decrypted before they are operated on by the CPU. Similarly, data values written to the external nonvolatile RAM storage during program execution are encrypted before they are presented on the Byte–wide data bus during the write operation. This encryption/decryption process is performed in real time such that no execution time is lost as compared to the non–encrypted DS5001FP or 8051 running at the same clock rate. As a result, operation of the encryptor circuitry is transparent to the application software.

Unlike the DS5000FP, the DS5002FP chip’s security feature is always enabled.

SECURITY CIRCUITRY

The on–chip functions associated with the DS5002FP’s software security feature are depicted in Figure 2. Encryption logic consists of an address encryptor and a data encryptor. Although each encryptor uses its own algorithm for encrypting data, both depend on the 64–bit key word which is contained in the Encryption Key registers. Both the encryptors operate during loading of the application software and also during its execution.

DS5002FP SECURITY CIRCUITRY Figure 2



The address encryptor translates each “logical” address, i.e., the normal sequence of addresses that are generated in the logical flow of program execution, into an encrypted address (or “physical” address) at which the byte is actually stored. Each time a logical address is generated, either during program loading or during program execution, the address encryptor circuitry uses the value of the 64–bit key word and of the address itself to form the physical address which will be presented on the address lines of the RAM. The encryption algorithm is such that there is one and only one physical address for every possible logical address. The address encryptor operates over the entire memory range which is configured during Bootstrap Loading for access on the Byte–wide Bus.

As Bootstrap Loading of the application software is performed, the Data Encryptor logic transforms the opcode, operand, or data byte at any given memory location into an encrypted representation. As each byte is read back to the CPU during program execution, the internal Data Encryptor restores it to its original value. When a byte is written to the external nonvolatile program/data RAM during program execution, that byte is stored in encrypted form as well. The data encryption logic uses the value of the 64–bit key, the logical address to which the data is being written, and the value of the data itself to form the encrypted data which is written to the nonvolatile program/data RAM. The encryption algorithm is repeatable, such that for a given data value, Encryption Key value, and logical address the encrypted byte will always be the same. However, there are many possible encrypted data values for each possible true data value due to the algorithm’s dependency on the values of the logical address and Encryption Key.

When the application software is executed, the internal CPU of the DS5002FP operates as normal. Logical addresses are calculated for opcode fetch cycles and also data read and write operations. The DS5002FP has the ability to perform address encryption on logical addresses as they are generated internally during the normal course of program execution. In a similar fashion, data is manipulated by the CPU in its true representation. However, it is also encrypted when it is written to the external program/data RAM, and is restored to its original value when it is read back.

When an application program is stored in the format described above, it is virtually impossible to disassemble opcodes or to convert data back into its true representa-

tion. Address encryption has the effect that the opcodes and data are not stored in the contiguous form in which they were assembled, but rather in seemingly random locations in memory. This in itself makes it virtually impossible to determine the normal flow of the program. As an added protection measure, the Address Encryptor also generates “dummy” read access cycles whenever time is available during program execution.

DUMMY READ CYCLES

Like the DS5000FP, the DS5002FP generates a “dummy” read access cycle to non–sequential addresses in external RAM memory whenever time is available during program execution. This action has the effect of further complicating the task of determining the normal flow of program execution. During these pseudo–random dummy cycles, the RAM is read to all appearance, but the data is not used internally. Through the use of a repeatable exchange of dummy and true read cycles, it is impossible to distinguish a dummy cycle from a real one.

ENCRYPTION ALGORITHM

The DS5002FP incorporates a proprietary algorithm implemented in hardware which performs the scrambling of address and data on the Byte–wide bus to the static RAM. This algorithm has been greatly strengthened with respect to its DS5000FP predecessor. Improvements include:

1. 64–bit Encryption Key
2. Incorporation of DES–like operations to provide a greater degree of nonlinearity
3. Customizable encryption

The encryption circuitry uses a 64–bit key value (compared to the DS5000FP’s 40–bit key) which is stored on the DS5002FP die and protected by the Security Lock function described below. In addition, the algorithm has been strengthened to incorporate certain operations used in DES encryption, so that the encryption of both the addresses and data is highly nonlinear. Unlike the DS5000FP, the encryption circuitry in the DS5002FP is always enabled.

Dallas Semiconductor can customize the encryption circuitry by laser programming the die to insure that a unique encryption algorithm is delivered to the customer. In addition, the customer–specific version can be branded as specified by the customer. Please contact Dallas Semiconductor for ordering information of customer–specific versions.

ENCRYPTION KEY

As described above, the on–chip 64–bit Encryption Key is the basis of both the address and data encryptor circuits. The DS5002FP provides a key management system which is greatly improved over the DS5000FP. The DS5002FP does not give the user the ability to select a key. Instead, when the loader is given certain commands, the key is set based on the value read from an on–chip hardware random number generator. This action is performed just prior to actually loading the code into the external RAM. This scheme prevents characterization of the encryption algorithm by continuously loading new, known keys. It also frees the user from the burden of protecting the key selection process.

The random number generator circuit uses the asynchronous frequency differences of two internal ring oscillator and the processor master clock (determined by XTAL1 and XTAL2). As a result, a true random number is produced.

VECTOR RAM

A 48–byte Vector RAM area is incorporated on–chip, and is used to contain the reset and interrupt vector code in the DS5002FP. It is included in the architecture to help insure the security of the application program.

If reset and interrupt vector locations were accessed from the external nonvolatile program/data RAM during the execution of the program, then it would be possible to determine the encrypted value of known addresses. This could be done by forcing an interrupt or reset condition and observing the resulting addresses on the Byte–wide address/data bus. For example, it is known that when a hardware reset is applied the logical program address is forced to location 0000H and code is executed starting from this location. It would then be possible to determine the encrypted value (or physical address) of the logical address value 0000H by observing the address presented to the external RAM following a hardware reset. Interrupt vector address relationships could be determined in a similar fashion. By using the on–chip Vector RAM to contain the interrupt and reset vectors, it is impossible to observe such relationships. Although it is very unlikely that an application program could be deciphered by observing vector address rela-

tionships, the Vector RAM eliminates this possibility. Note that the dummy accesses mentioned above are conducted while fetching from Vector RAM.

The Vector RAM is automatically loaded with the user's reset and interrupt vectors during bootstrap loading.

SECURITY LOCK

Once the application program has been loaded into the DS5002FP's NV RAM, the Security Lock may be enabled by issuing the "Z" command in the Bootstrap Loader. While the Security Lock is set, no further access to program/ data information is possible via the on–chip ROM. Access is prevented by both the Bootstrap Loader firmware and the DS5002FP encryptor circuits.

Access to the NVRAM may only be regained by clearing the Security Lock via the "U" command in the Bootstrap Loader. This action triggers several events which defeat tampering. First, the Encryption Key is instantaneously erased. Without the Encryption Key, the DS5002FP is no longer able to decrypt the contents of the RAM. Therefore, the application software can no longer be correctly executed, nor can it be read back in its true form via the Bootstrap Loader. Second, the Vector RAM area is also instantaneously erased, so that the reset and vector information is lost. Third, the Bootstrap Loader firmware sequentially erases the encrypted RAM area. Lastly, the loader creates and loads a new random key.

The Security Lock bit itself is constructed using a multiple–bit latch which is interlaced for self–destruct in the event of tampering. The lock is designed to set–up a "domino–effect" such that erasure of the bit will result in an unstoppable sequence of events that clears critical data including Encryption Key and Vector RAM. In addition, this bit is protected from probing by the top–coating feature mentioned below.

SELF–DESTRUCT INPUT

The Self–Destruct Input (SDI) pin is an active high input which is used to reset the Security Lock in response to an external event. The SDI input is intended to be used with external tamper detection circuitry. It can be activated with or without operating power applied to the V_{CC} pin. Activation of the SDI pin instantly resets the Security Lock and causes the same sequence of events described above for this action. In addition, power is momentarily removed from the Byte–wide bus interface including the V_{CCO} pin, resulting in the loss of data in external RAM.

TOP LAYER COATING

The DS5002FPM is provided with a special top–layer coating that is designed to prevent a probe attack. This coating is implemented with second–layer metal added through special processing of the microcontroller die. This additional layer is not a simple sheet of metal, but rather a complex layout that is interwoven with power and ground which are in turn connected to logic for the Encryption Key and the Security Lock. As a result, any attempt to remove the layer or probe through it will result in the erasure of the Security Lock and/or the loss of Encryption Key bits.

BOOTSTRAP LOADING

Initial loading of application software into the DS5002FP is performed by firmware within the on–chip Bootstrap Loader communicating with a PC via the on–chip serial port in a manner which is almost identical to that for the DS5001FP. The user should consult the DS5001FP data sheet as a basis of operational characteristics of this firmware. Certain differences in loading procedure exist in order to support the security feature. These differences are documented below. Table 1 summarizes the commands accepted by the bootstrap loader.

When the Bootstrap Loader is invoked, portions of the 128–byte scratchpad RAM area are automatically overwritten with zeroes, and then used for variable storage for the bootstrap firmware. Also, a set of eight bytes are generated using the random number generator circuitry and are saved as a potential word for the 64–bit Encryption Key.

Any read or write operation to the DS5002FP's external program/data SRAM can only take place if the Security Lock bit is in a cleared state. Therefore, the first step which is taken in the loading of a program should be the clearing of the Security Lock bit through the "U" command.

DS5002FP SERIAL BOOTSTRAP LOADER COMMANDS Table 1

COMMAND	FUNCTION
C	Return CRC–16 of the program/data NV RAM
D	Dump Intel Hex file
F	Fill program/data NV RAM
G	Get Data from P1, P2, and P3
I	N/A on the DS5002FP
L	Load Intel Hex file
M	Toggle modem available bit
N	Set Freshness Seal – All program and data will be lost
P	Put data into P0, P1, P2, and P3
R	Read status of NVSFRs (MCON, RPCTL, MSL, CALIB)
T	Trace (echo) incoming Intel Hex code
U	Clear Security Lock
V	Verify program/data NV RAM with incoming Intel Hex data
W	Write Special Function Registers – (MCON, RPCTL, MSL, CALIB)
Z	Set Security Lock

Execution of certain Bootstrap Loader commands will result in the loading of the newly generated 64–bit random number into the Encryption Key word. These commands are as follows:

Fill	F
Load	L
Dump	D
Verify	V
CRC	C

Execution of the Fill and Load commands will result in the data loaded into the NV RAM in an encrypted form determined by the value of the newly–generated key word. The subsequent execution of the Dump command within the same bootstrap session will cause the contents of the encrypted RAM to be read out and transmitted back to the host PC in decrypted form. Similarly, execution of the Verify command within the same bootstrap session will cause the incoming absolute hex data to be compared against the true contents of the encrypted RAM, and the CRC command will return the CRC value calculated from the true contents of the encrypted RAM. As long as any of the above commands are executed within the same bootstrap session, the loaded key value will remain the same and contents of the encrypted program/data NV RAM may be read or written normally and freely until the Security Lock bit is set.

When the Security Lock bit is set using the Z command, no further access to the true RAM contents is possible using any bootstrap command or by any other means.

INSTRUCTION SET

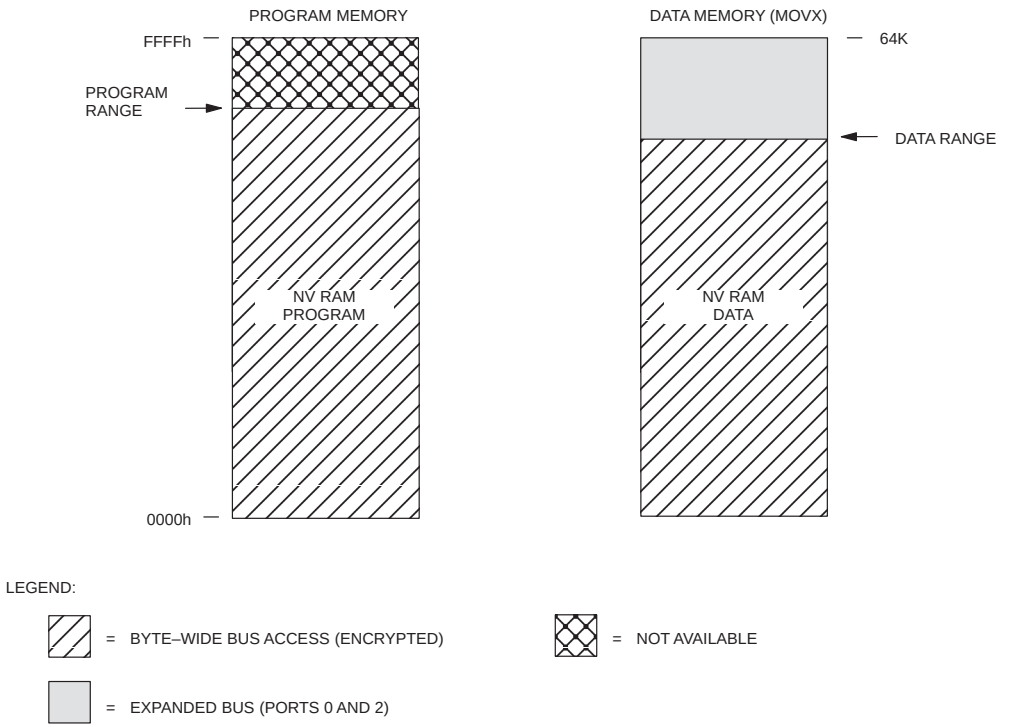
The DS5002FP executes an instruction set that is object code compatible with the industry standard 8051 microcontroller. As a result, software development packages such as assemblers and compilers that have been written for the 8051 are compatible with the DS5002FP. A complete description of the instruction set and operation are provided in the User's Guide section of the Secure Microcontroller Data Book.

Also note that the DS5002FP is embodied in the DS2252T module. The DS2252T combines the DS5002FP with between 32K and 128K of SRAM, a lithium cell, and a real time clock. This is packaged in a 40–pin SIMM module.

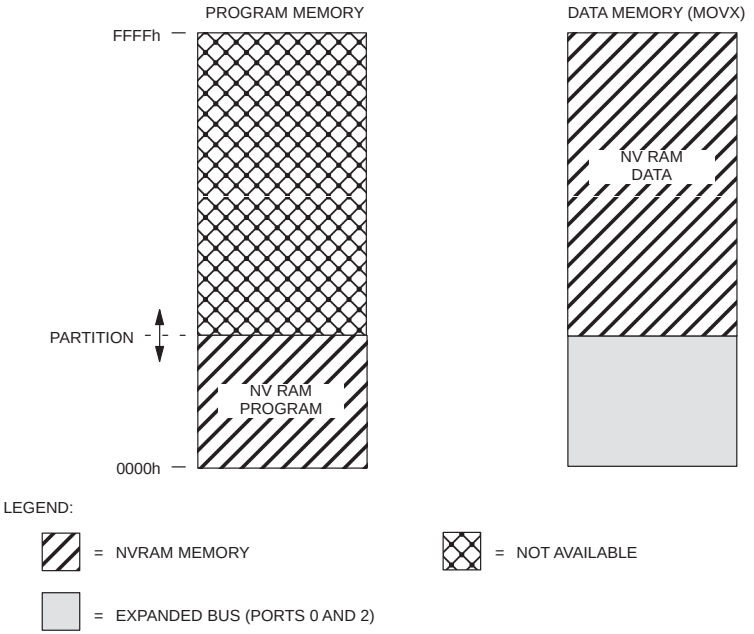
MEMORY ORGANIZATION

Figure 3 illustrates the memory map accessed by the DS5002FP. The entire 64K of program and 64K of data are potentially available to the Byte–wide bus. This preserves the I/O ports for application use. The user controls the portion of memory that is actually mapped to the Byte–wide bus by selecting the Program Range and Data Range. Any area not mapped into the NV RAM is reached via the Expanded bus on Ports 0 and 2. An alternate configuration allows dynamic Partitioning of a 64K space as shown in Figure 4. Selecting PES=1 provides another 64K of potential data storage or memory mapped peripheral space as shown in Figure 5. These selections are made using Special Function Registers. The memory map and its controls are covered in detail in the User's Guide section of the Secure Microcontroller Data Book.

DS5002FP MEMORY MAP IN NON–PARTITIONABLE MODE (PM=1) Figure 3



DS5002FP MEMORY MAP IN PARTITIONABLE MODE (PM=0) Figure 4



NOTE: Partitionable mode is not supported when MSEL=0 (128KB mode).

DS5002FP MEMORY MAP WITH PES=1 Figure 5

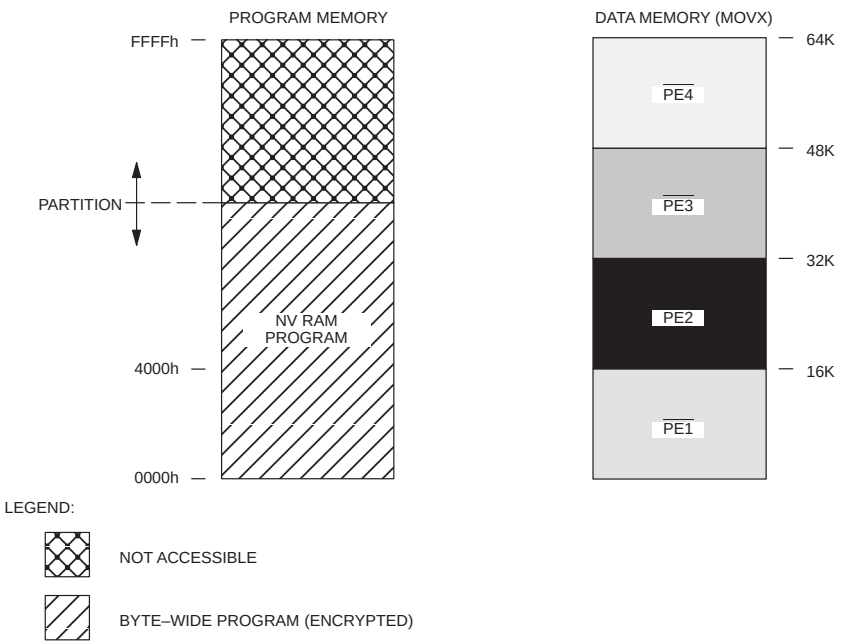
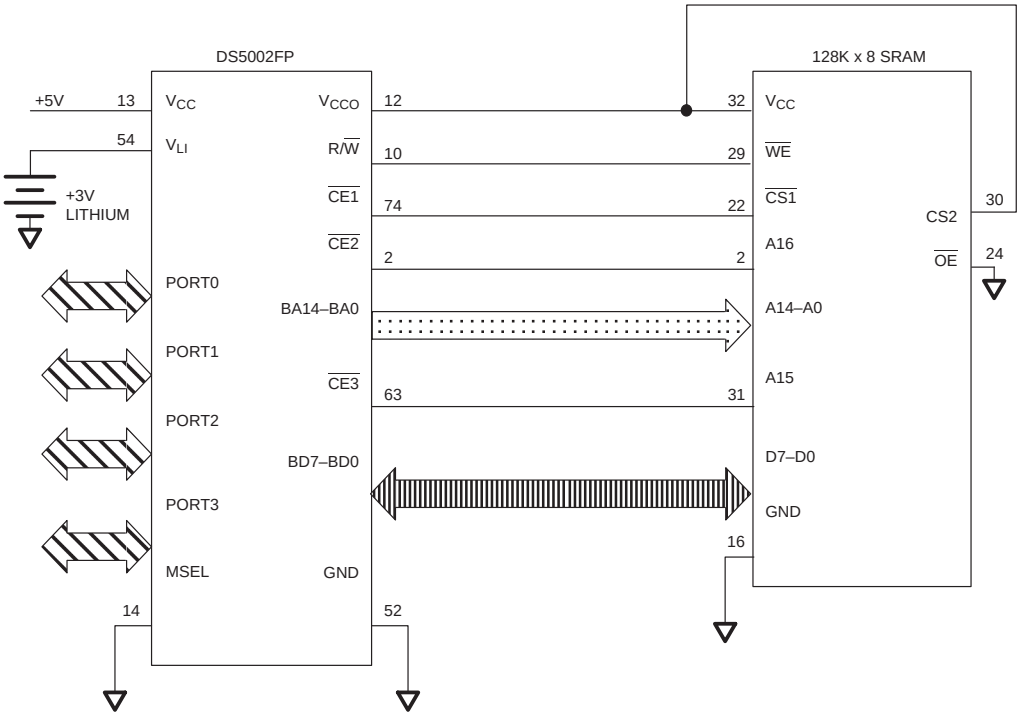
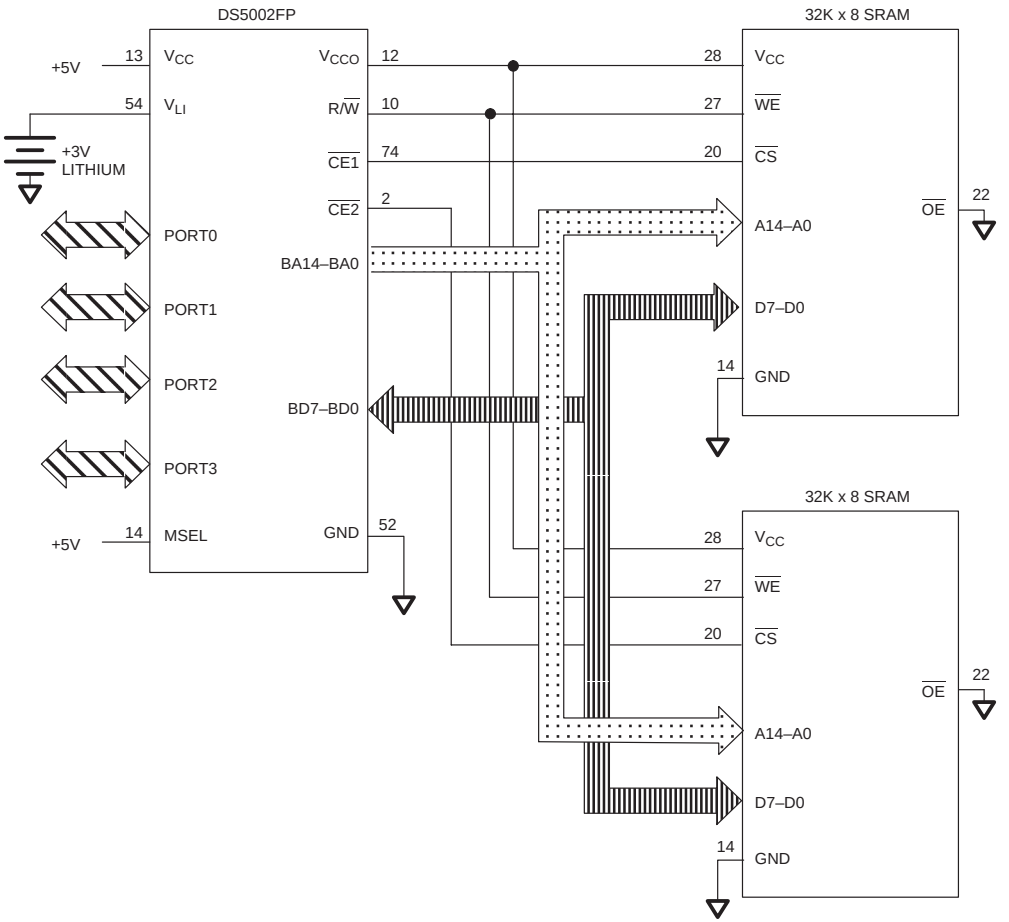


Figure 6 illustrates a typical memory connection for a system using a 128K byte SRAM. Note that in this configuration, both program and data are stored in a common RAM chip Figure 7 shows a similar system with using two 32K byte SRAMs. The Byte–wide Address bus connects to the SRAM address lines. The bi–directional Byte–wide data bus connects the data I/O lines of the SRAM.

DS5002FP CONNECTION TO 128K X 8 SRAM Figure 6



DS5002FP CONNECTION TO 64K X 8 SRAM Figure 7



POWER MANAGEMENT

The DS5002FP monitors V_{CC} to provide Power–fail Reset, early warning Power–fail Interrupt, and switch over to lithium backup. It uses an internal band–gap reference in determining the switch points. These are called V_{PFW}, V_{CCMIN}, and V_{LI} respectively. When V_{CC} drops below V_{PFW}, the DS5002FP will perform an interrupt vector to location 2Bh if the power–fail warning was enabled. Full processor operation continues regardless. When power falls further to V_{CCMIN}, the DS5002FP invokes a reset state. No further code execution will be performed unless power rises back above V_{CCMIN}. All decoded chip enables and the R/$\overline{W}$ signal go to an inactive (logic 1) state. V_{CC} is still the power source at this time. When V_{CC} drops further to below V_{LI}, internal circuitry will switch to the lithium cell for power. The majority of internal circuits will be disabled and the remaining nonvolatile states will be retained. Any devices connected to V_{CCO} will be powered by the lithium cell at this time. V_{CCO} will be at the lithium battery voltage less a diode drop. This drop will vary depending on the load. Low power SRAMs should be used for this reason. When using the DS5002FP, the user must select the appropriate battery to match the RAM data retention current and the desired backup lifetime. Note that the lithium cell is only loaded when $V_{CC} < V_{LI}$. The User's Guide has more information on this topic. The trip points V_{CCMIN} and V_{PFW} are listed in the electrical specifications.

ELECTRICAL SPECIFICATIONS

The DS5002FP adheres to all AC and DC electrical specifications published for the DS5001FP. The absolute maximum ratings and unique specifications for the DS5002FP are listed below.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC CHARACTERISTICS

(t_A = 0°C to 70°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Low Voltage	V_{IL}	–0.3		+0.8	V	1
Input High Voltage	V_{IH1}	2.0		V_{CC}+0.3	V	1
Input High Voltage (RST, XTAL1, PROG)	V_{IH2}	3.5		V_{CC}+0.3	V	1
Output Low Voltage @ I_{OL}=1.6 mA (Ports 1, 2, 3)	V_{OL1}		0.15	0.45	V	1
Output Low Voltage @ I_{OL}=3.2 mA (Port 0, ALE, PF, BA15–0, BD7–0, R/W, CE1N, CE1–4, PE1–4, V_{RST})	V_{OL2}		0.15	0.45	V	1
Output High Voltage @ I_{OH}=–80 µA (Ports 1, 2, 3)	V_{OH1}	2.4	4.8		V	1
Output High Voltage @ I_{OH}=–400 µA (Ports 0, ALE, PF, BA15–0, BD7–0, R/W, CE1N, CE1–4, PE1–4)	V_{OH2}	2.4	4.8		V	1
Input Low Current V_{IN}=0.45V (Ports 1, 2, 3)	I_{IL}			–50	µA	
Transition Current; 1 to 0 V_{IN}=2.0V (Ports 1, 2, 3) (0°C to 70°C)	I_{TL}			–500	µA	
Transition Current; 1 to 0 V_{IN}=2.0V (Ports 1, 2, 3) (–40°C to +85°C)	I_{TL}			–600	µA	12
SDI Input Low Voltage	V_{ILS}			0.4	V	1
SDI Input High Voltage	V_{IHS}	2.0		V_{CCO}	V	1, 11
SDI Pull–Down Resistor	R_{SDI}	25		60	KΩ	
Battery–Backup Quiescent Current	I_{BAT}		5	75	nA	7

DC CHARACTERISTICS (cont'd) (t_A = 0°C to 70°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current 0.45 < V_{IN} < V_{CC} (Port 0, MSEL)	I_{IL}			±10	µA	
RST Pull–down Resistor (0°C to 70°C)	R_{RE}	40		150	KΩ	
RST Pull–down Resistor (–40°C to +85°C)	R_{RE}	40		180	KΩ	12
$\overline{VRST}$ Pull–up Resistor	R_{VR}		4.7		KΩ	
$\overline{PROG}$ Pull–up Resistor	R_{PR}		40		KΩ	
Power–Fail Warning Voltage (0°C to 70°C)	V_{PFW}	4.25	4.37	4.50	V	1
Power–Fail Warning Voltage (–40°C to +85°C)	V_{PFW}	4.1	4.37	4.5	V	1, 12
Minimum Operating Voltage (0°C to 70°C)	V_{CCMIN}	4.00	4.12	4.25	V	1
Minimum Operating Voltage (–40°C to +85°C)	V_{CCMIN}	3.85	4.09	4.25	V	1, 12
Lithium Supply Voltage	V_{LI}	2.5		4.0	V	1
Operating Current @ 16 MHz	I_{CC}			36	mA	2
Idle Mode Current @ 12 MHz (0°C to 70°C)	I_{IDLE}			7.0	mA	3
Idle Mode Current @ 12 MHz (–40°C to +85°C)	I_{IDLE}			8.0	mA	3, 12
Stop Mode Current	I_{STOP}			80	µA	4
Pin Capacitance	C_{IN}			10	pF	5
Output Supply Voltage (V_{CCO})	V_{CCO1}	V_{CC}–0.35			V	1, 2
Output Supply Battery–backed Mode (V_{CCO}, $\overline{CE}$1–4, $\overline{PE}$1–2) (0°C to 70°C)	V_{CCO2}	V_{LI}–0.65			V	1, 8
Output Supply Battery–backed Mode (V_{CCO}, $\overline{CE}$1–4, $\overline{PE}$1–2) (–40°C to +85°C)	V_{CCO2}	V_{LI}–0.9			V	1, 8, 12
Output Supply Current @ V_{CCO}=V_{CC} – 0.3V	I_{CCO1}			75	mA	6
Lithium–backed Quiescent Current	I_{LI}		5	75	nA	7
Reset Trip Point in Stop Mode w/BAT=3.0V (0°C to 70°C) w/BAT=3.0V (–40°C to +85°C) w/BAT=3.3V (0°C to 70°C)		 4.0 3.85 4.4		 4.25 4.25 4.65		 1 1, 12 1

AC CHARACTERISTICS

(t_A = 0°C to70°C; V_{CC}=0V to 5V)

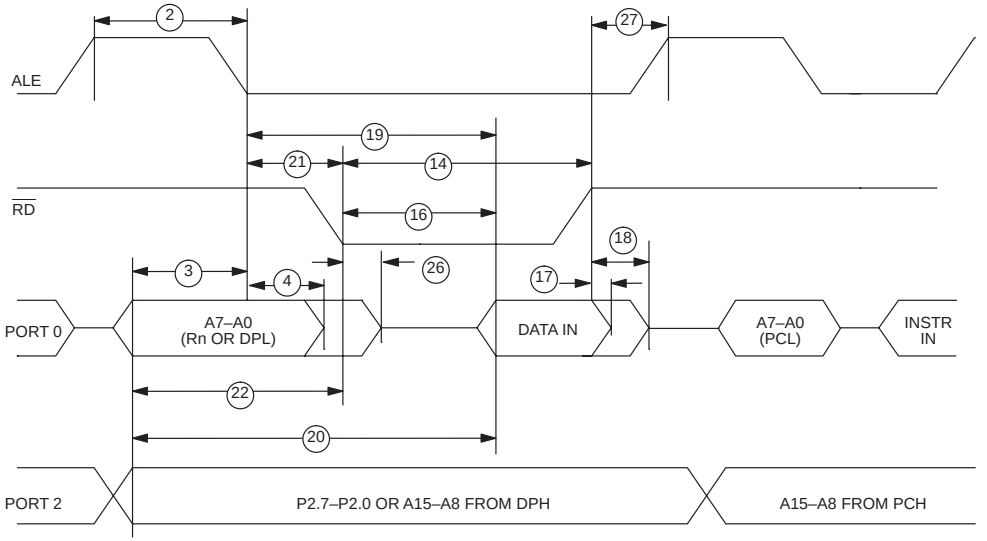
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SDI Pulse Reject	t_{SPR}			2	µs	10
SDI Pulse Accept	t_{SPA}	10			µs	10

AC CHARACTERISTICS
EXPANDED BUS MODE TIMING SPECIFICATIONS

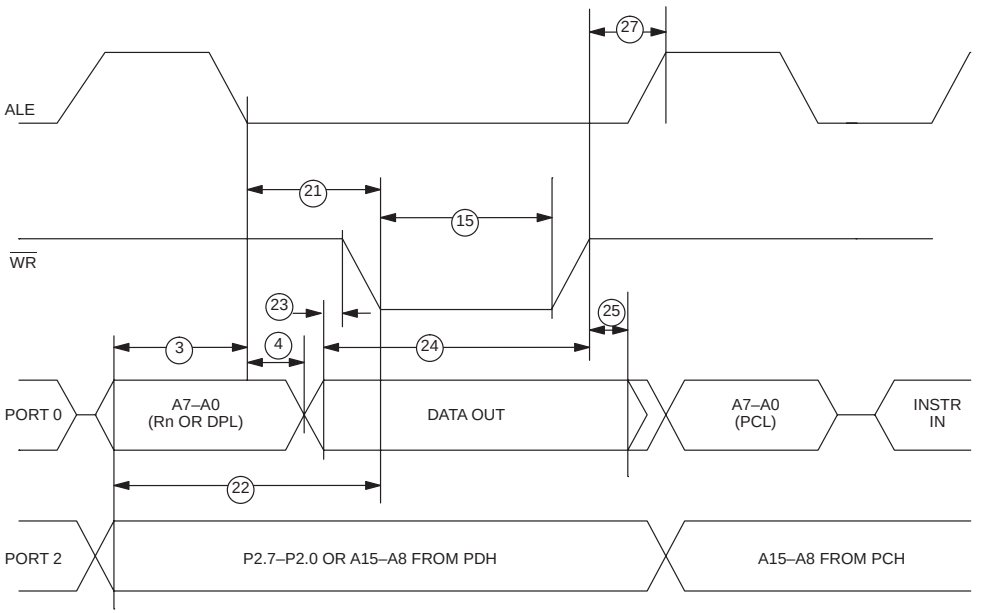
(t_A = 0°C to70°C; V_{CC}=5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
1	Oscillator Frequency	$1/t_{CLK}$	1.0	16	MHz
2	ALE Pulse Width	t_{ALPW}	$2t_{CLK}$–40		ns
3	Address Valid to ALE Low	t_{AVALL}	t_{CLK}–40		ns
4	Address Hold After ALE Low	t_{AVAAV}	t_{CLK}–35		ns
14	$\overline{RD}$ Pulse Width	t_{RDPW}	$6t_{CLK}$–100		ns
15	$\overline{WR}$ Pulse Width	t_{WRPW}	$6t_{CLK}$–100		ns
16	$\overline{RD}$ Low to Valid Data In @12 MHz @16 MHz	t_{RDLDV}		$5t_{CLK}$–165 $5t_{CLK}$–105	ns ns
17	Data Hold after $\overline{RD}$ High	t_{RDHDV}	0		ns
18	Data Float after $\overline{RD}$ High	t_{RDHDZ}		$2t_{CLK}$–70	ns
19	ALE Low to Valid Data In @12 MHz @16 MHz	t_{ALLVD}		$8t_{CLK}$–150 $8t_{CLK}$–90	ns ns
20	Valid Addr. to Valid Data In @12 MHz @16 MHz	t_{AVDV}		$9t_{CLK}$–165 $9t_{CLK}$–105	ns ns
21	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{ALLRDL}	$3t_{CLK}$–50	$3t_{CLK}$+50	ns
22	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVRDL}	$4t_{CLK}$–130		ns
23	Data Valid to $\overline{WR}$ Going Low	t_{DVWRL}	t_{CLK}–60		ns
24	Data Valid to $\overline{WR}$ High @12 MHz @16 MHz	t_{DVWRH}	$7t_{CLK}$–150 $7t_{CLK}$–90		ns ns
25	Data Valid after $\overline{WR}$ High	t_{WRHDV}	t_{CLK}–50		ns
26	$\overline{RD}$ Low to Address Float	t_{RDLAZ}		0	ns
27	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{RDHALH}	t_{CLK}–40	t_{CLK}+50	ns

EXPANDED DATA MEMORY READ CYCLE



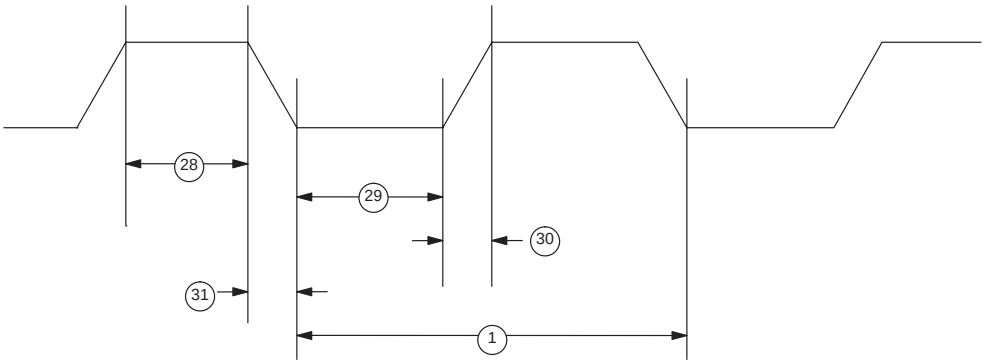
EXPANDED DATA MEMORY WRITE CYCLE



AC CHARACTERISTICS (cont'd)
EXTERNAL CLOCK DRIVE (t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER		SYMBOL	MIN	MAX	UNITS
28	External Clock High Time	@12 MHz @16 MHz	t_{CLKHPW}	20 15		ns ns
29	External Clock Low Time	@12 MHz @16 MHz	t_{CLKLPW}	20 15		ns ns
30	External Clock Rise Time	@12 MHz @16 MHz	t_{CLKR}		20 15	ns ns
31	External Clock Fall Time	@12 MHz @16 MHz	t_{CLKF}		20 15	ns ns

EXTERNAL CLOCK TIMING

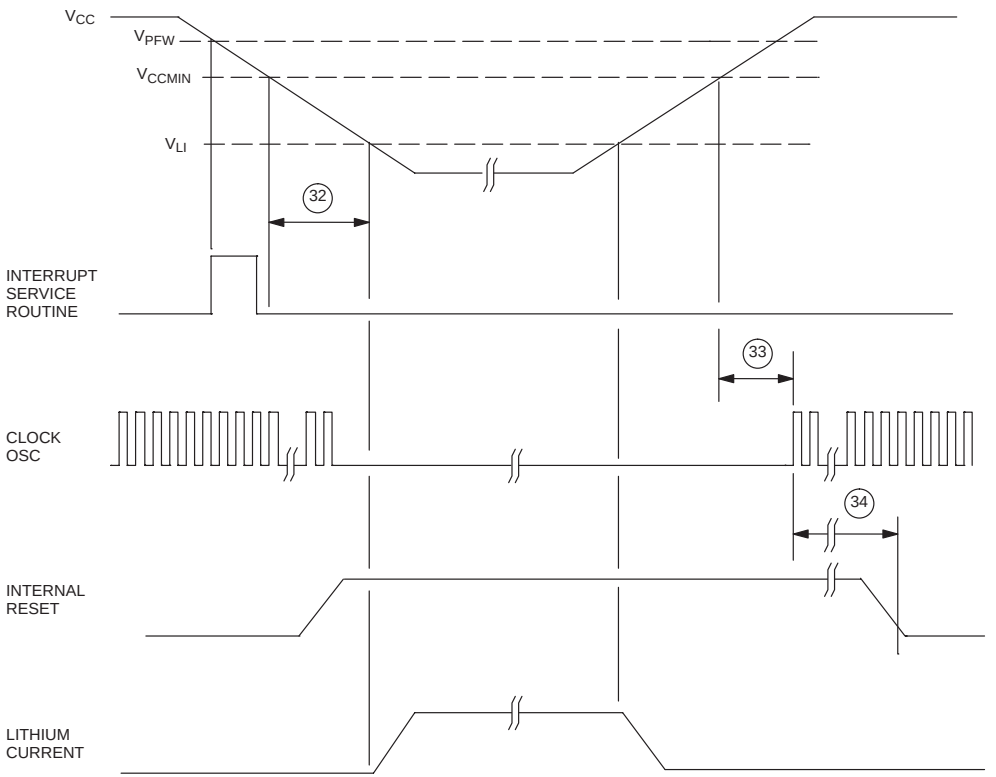


AC CHARACTERISTICS (cont'd)
POWER CYCLING TIMING

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
32	Slew Rate from V_{CCmin} to V_{LI}	t_F	130		µs
33	Crystal Start up Time	t_{CSU}		(note 9)	
34	Power On Reset Delay	t_{POR}		21504	t_{CLK}

POWER CYCLE TIMING

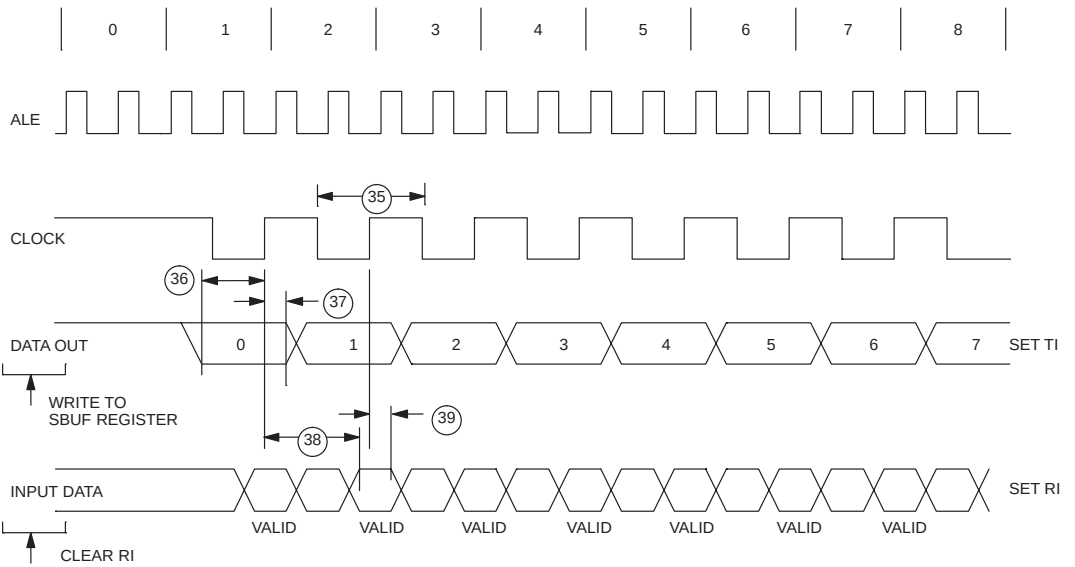


AC CHARACTERISTICS (cont'd)
SERIAL PORT TIMING – MODE 0

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
35	Serial Port Clock Cycle Time	t_{SPCLK}	$12t_{CLK}$		µs
36	Output Data Setup to Rising Clock Edge	t_{DOCH}	$10t_{CLK}$–133		ns
37	Output Data Hold after Rising Clock Edge	t_{CHDO}	$2t_{CLK}$–117		ns
38	Clock Rising Edge to Input Data Valid	t_{CHDV}		$10t_{CLK}$–133	ns
39	Input Data Hold after Rising Clock Edge	t_{CHDIV}	0		ns

SERIAL PORT TIMING – MODE 0

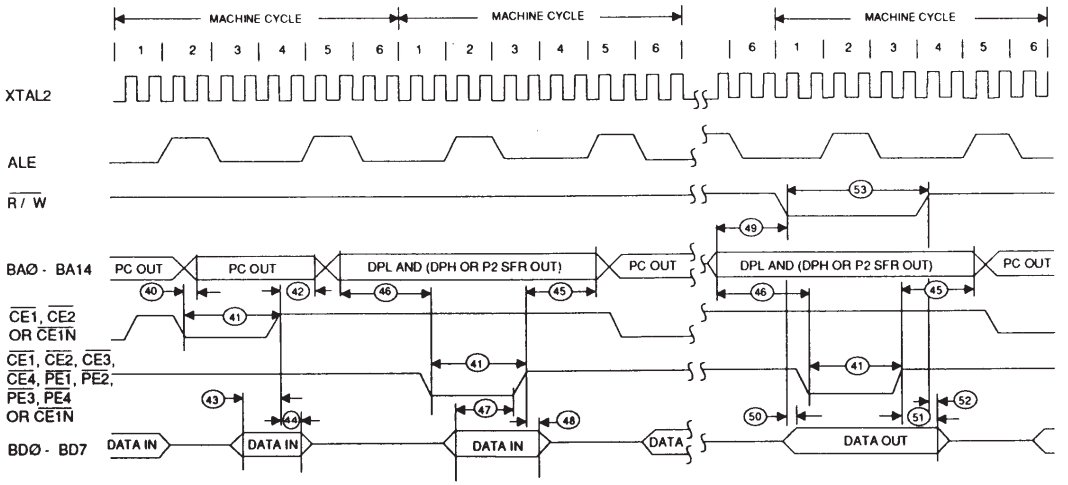


AC CHARACTERISTICS
BYTEWIDE ADDRESS/DATA BUS TIMING

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
40	Delay to Byte–wide Address Valid from $\overline{CE1}$, $\overline{CE2}$ or $\overline{CE1N}$ Low During Opcode Fetch	t_{CE1LPA}		30	ns
41	Pulse Width of $\overline{CE}$1–4, $\overline{PE}$1–4 or $\overline{CE1N}$	t_{CEPW}	$4t_{CLK}$–35		ns
42	Byte–wide Address Hold After $\overline{CE1}$, $\overline{CE2}$ or $\overline{CE1N}$ High During Opcode Fetch	t_{CE1HPA}	$2t_{CLK}$–20		ns
43	Byte–wide Data Setup to $\overline{CE1}$, $\overline{CE2}$ or $\overline{CE1N}$ High During Opcode Fetch	t_{OVCE1H}	$1t_{CLK}$+40		ns
44	Byte–wide Data Hold After $\overline{CE1}$, $\overline{CE2}$ or $\overline{CE1N}$ High During Opcode Fetch	t_{CE1HOV}	10		ns
45	Byte–wide Address Hold After $\overline{CE}$1–4, $\overline{PE}$1–4, or $\overline{CE1N}$ High During MOVX	t_{CEHDA}	$4t_{CLK}$–30		ns
46	Delay from Bytewide Address Valid $\overline{CE}$1–4, $\overline{PE}$1–4, or $\overline{CE1N}$ Low During MOVX	t_{CELDA}	$4t_{CLK}$–35		ns
47	Byte–wide Data Setup to $\overline{CE}$1–4, $\overline{PE}$1–4, or $\overline{CE1N}$ High During MOVX (read)	t_{DACEH}	$1t_{CLK}$+40		ns
48	Byte–wide Data Hold After $\overline{CE}$1–4, $\overline{PE}$1–4, or $\overline{CE1N}$ High During MOVX (read)	t_{CEHDV}	10		ns
49	Byte–wide Address Valid to R/$\overline{W}$ Active During MOVX (write)	t_{AVRWL}	$3t_{CLK}$–35		ns
50	Delay from R/$\overline{W}$ Low to Valid Data Out During MOVX (write)	t_{RWLDV}	20		ns
51	Valid Data Out Hold Time from $\overline{CE}$1–4, $\overline{PE}$1–4, or $\overline{CE1N}$ High	t_{CEHDV}	$1t_{CLK}$–15		ns
52	Valid Data Out Hold Time from R/$\overline{W}$ High	t_{RWHDV}	0		ns
53	Write Pulse Width (R/$\overline{W}$ Low Time)	t_{RWLPW}	$6t_{CLK}$–20		ns

BYTEWIDE BUS TIMING



RPC AC CHARACTERISTICS – DBB READ

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
54	$\overline{CS}$, A_0 Setup to $\overline{RD}$	t_{AR}	0		ns
55	$\overline{CS}$, A_0 Hold After $\overline{RD}$	t_{RA}	0		ns
56	$\overline{RD}$ Pulse Width	t_{RR}	160		ns
57	$\overline{CS}$, A_0 to Data Out Delay	t_{AD}		130	ns
58	$\overline{RD}$ to Data Out Delay	t_{RD}	0	130	ns
59	$\overline{RD}$ to Data Float Delay	t_{RDZ}		85	ns

RPC AC CHARACTERISTICS – DBB WRITE (t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
60	$\overline{CS}$, A_0 Setup to $\overline{WR}$	t_{AW}	0		ns
61A	$\overline{CS}$, Hold After $\overline{WR}$	t_{WA}	0		ns
61B	A_0, Hold After $\overline{WR}$	t_{WA}	20		ns
62	$\overline{WR}$ Pulse Width	t_{WW}	160		ns
63	Data Setup to $\overline{WR}$	t_{DW}	130		ns
64	Data Hold After $\overline{WR}$	t_{WD}	20		ns

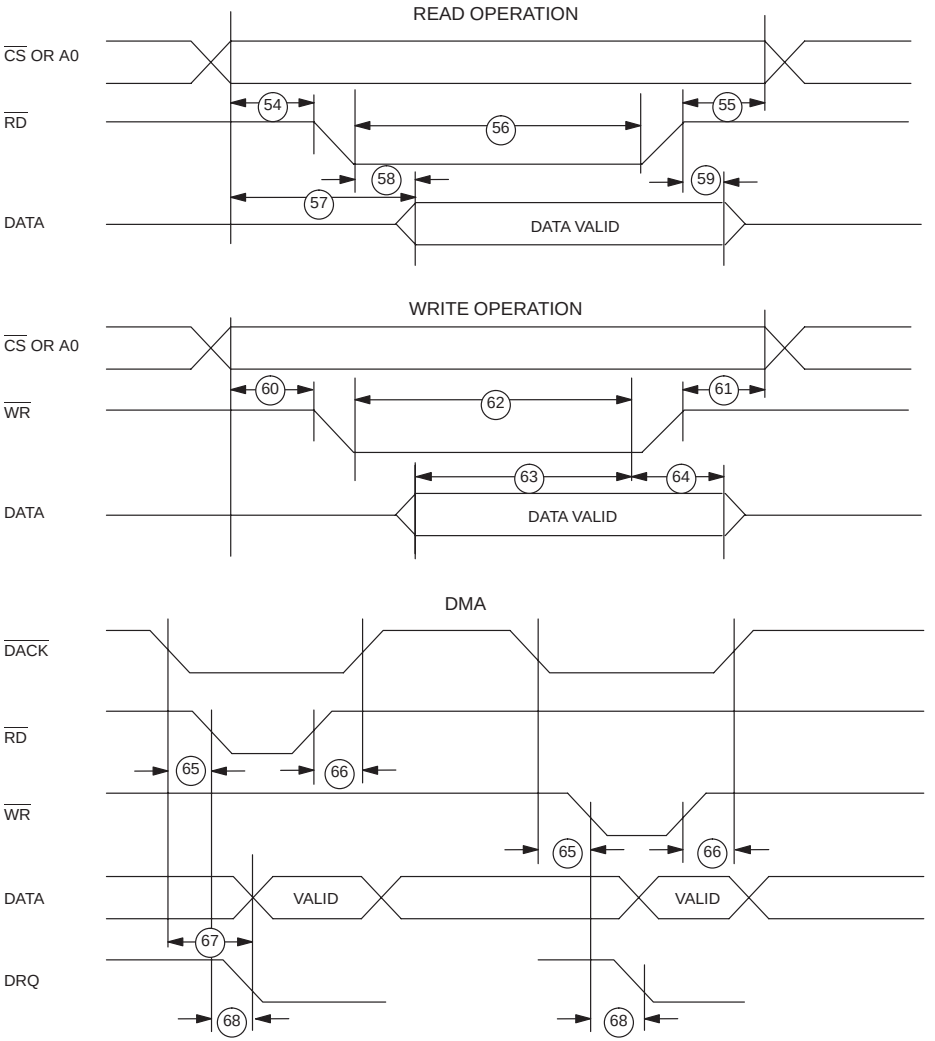
AC CHARACTERISTICS – DMA (t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
65	$\overline{DACK}$ to $\overline{WR}$ or $\overline{RD}$	t_{ACC}	0		ns
66	$\overline{RD}$ or $\overline{WR}$ to $\overline{DACK}$	t_{CAC}	0		ns
67	$\overline{DACK}$ to Data Valid	t_{ACD}	0	130	ns
68	$\overline{RD}$ or $\overline{WR}$ to DRQ Cleared	t_{CRQ}		110	ns

AC CHARACTERISTICS – $\overline{PROG}$ (t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
69	$\overline{PROG}$ Low to Active	t_{PRA}	48		CLKS
70	$\overline{PROG}$ High to Inactive	t_{PRI}	48		CLKS

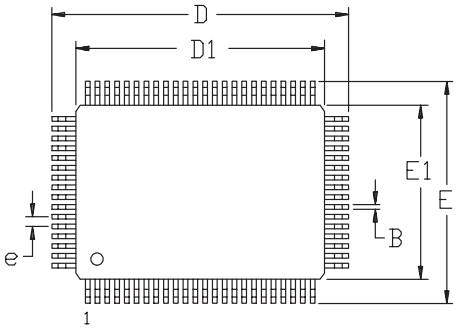
RPC TIMING MODE

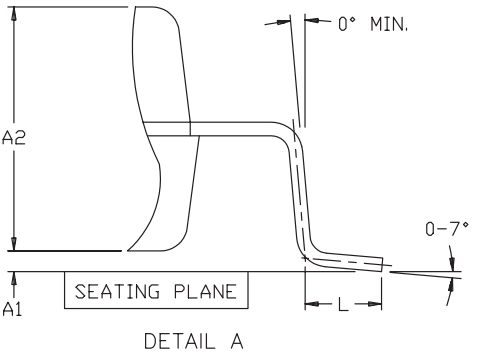


NOTES:
All parameters apply to both commercial and industrial temperature operation unless otherwise noted.

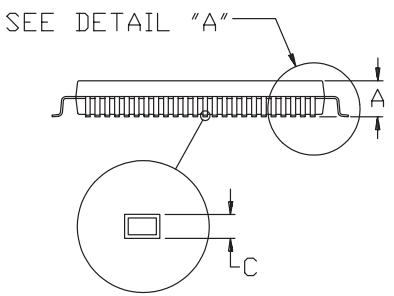
1. All voltages are referenced to ground.
2. Maximum operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF}=10 ns, V_{IL} = 0.5V; XTAL2 disconnected; RST = PORT0 = V_{CC}, MSEL = V_{SS}.
3. Idle mode I_{IDLE} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF} = 10 ns, V_{IL} = 0.5V; XTAL2 disconnected; PORT0 = V_{CC}, RST = MSEL = V_{SS}.
4. Stop mode I_{STOP} is measured with all output pins disconnected; PORT0 = V_{CC}; XTAL2 not connected; RST = MSEL = XTAL1 = V_{SS}.
5. Pin Capacitance is measured with a test frequency – 1 MHz, t_A = 25°C.
6. I_{CCO1} is the maximum average operating current that can be drawn from V_{CCO} in normal operation.
7. I_{LI} is the current drawn from V_{LI} input when V_{CC} = 0V and V_{CCO} is disconnected. Battery–backed mode: 2.5V ≤ V_{BAT} ≤ 4.0; V_{CC} ≤ V_{BAT}; V_{SDI} should be ≤ V_{ILS} for I_{BAT} max.
8. V_{CCO2} is measured with V_{CC} < V_{LI}, and a maximum load of 10 µA on V_{CCO}.
9. Crystal start–up time is the time required to get the mass of the crystal into vibrational motion from the time that power is first applied to the circuit until the first clock pulse is produced by the on–chip oscillator. The user should check with the crystal vendor for a worst case specification on this time.
10. SDI is deglitched to prevent accidental destruction. The pulse must be longer than t_{SPR} to pass the deglitcher, but SDI is not guaranteed unless it is longer than t_{SPA}.
11. V_{IHS} minimum is 2.0V or V_{CCO}, whichever is lower.
12. This parameter applies to industrial temperature operation.

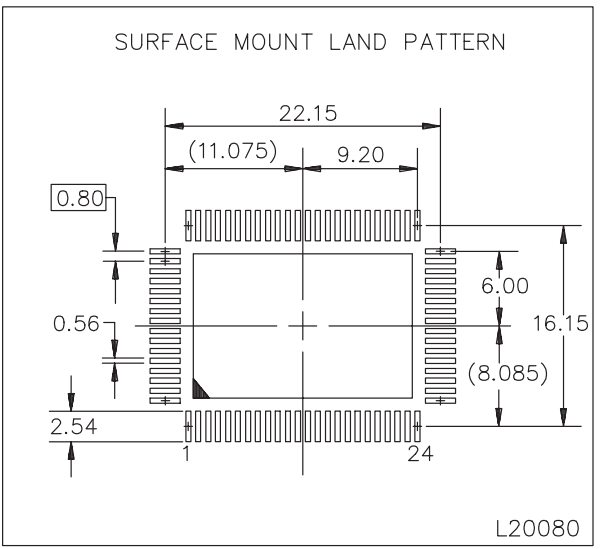
DS5002FP CMOS MICROPROCESSOR





DETAIL A





DIM	MILLIMETERS	
	MIN	MAX
A	–	3.40
A1	0.25	–
A2	2.55	2.87
B	0.30	0.50
C	0.13	0.23
D	23.70	24.10
D1	19.90	20.10
E	17.70	18.10
E1	13.90	14.10
e	0.80 BSC	
L	0.65	0.95

56–G4005–001

DATA SHEET REVISION SUMMARY

The following represent the key differences between 11/27/95 and 07/30/96 version of the DS5002FP data sheet. Please review this summary carefully.

1. Change V_{CC02} specification from V_{LI} –0.5 to V_{LI} –0.65 (PCN F62501).
2. Update mechanical specifications.

The following represent the key differences between 07/30/96 and 11/19/96 version of the DS5002FP data sheet. Please review this summary carefully.

1. Change V_{CC01} from V_{CC}–0.3 to V_{CC}–0.35.

SECURE MICROCONTROLLER APPLICATION NOTES

DALLAS SEMICONDUCTOR

Application Note 91
Microcontroller Design Guidelines for Reducing ALE Signal Noise

OVERVIEW

The 8051 architecture allows for external program and data access through the use of Port 0 and Port 2 as an external memory interface. The 8051 architecture multiplexes the data and LSB of address on Port 0, requiring a 74373 latch for demultiplexing. This means that Port 0 will be directly connected to at least two devices. More devices may be placed on the bus if an external data SRAM or memory–mapped peripherals are used.

Because Port 0 must switch quickly between address and data, it requires strong current drive characteristics. The need to quickly switch many loads requires strong drive characteristics on Port 0. Unfortunately, the high instantaneous current requirements of quickly switching all the pins of Port 0 can induce noise on the ALE signal. In some instances, this noise can interfere with program and data accesses by causing the external hardware to latch an incorrect address. This is a relatively rare occurrence, and most designers will not encounter it. The magnitude of this problem is directly related to several issues associated with both the system and software. Devices which do not access external memory via Port 0 and Port 2 will not experience this problem.

This application note will discuss ways the system designer can reduce the effects of Port 0 switching on device operation. It is applicable to any ROMless 8051 microcontroller which accesses external memory via Port 0 and Port 2, including the DS80C310 and DS80C320. It is also applicable to any microcontroller with internal program memory that accesses external memory.

ALE NOISE GENERATION

Under certain system conditions, noise induced on ALE can cause an incorrect LSB address to be latched when using the multiplexed address/data bus. The noise, as seen in Figure 1, is generated by the high speed switching of Port 0 when the processor stops driving a memory address and begins driving data during a MOVX write. The noise pulse can, under the right conditions, rise above the V_{IH} input threshold of TTL, LS, FS and HCT logic. In this case, the 74373 latch may be falsely triggered, latching an incorrect address and disturb the LSB address of the MOVX write.

DATA MEMORY WRITE (IDEAL TIMING) Figure 1

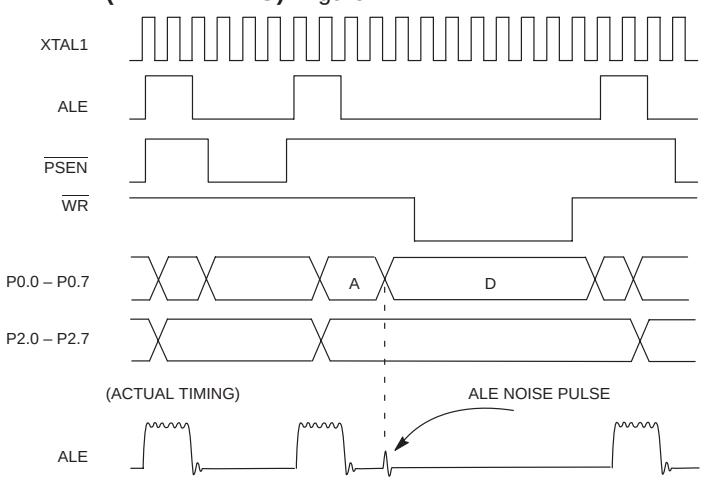
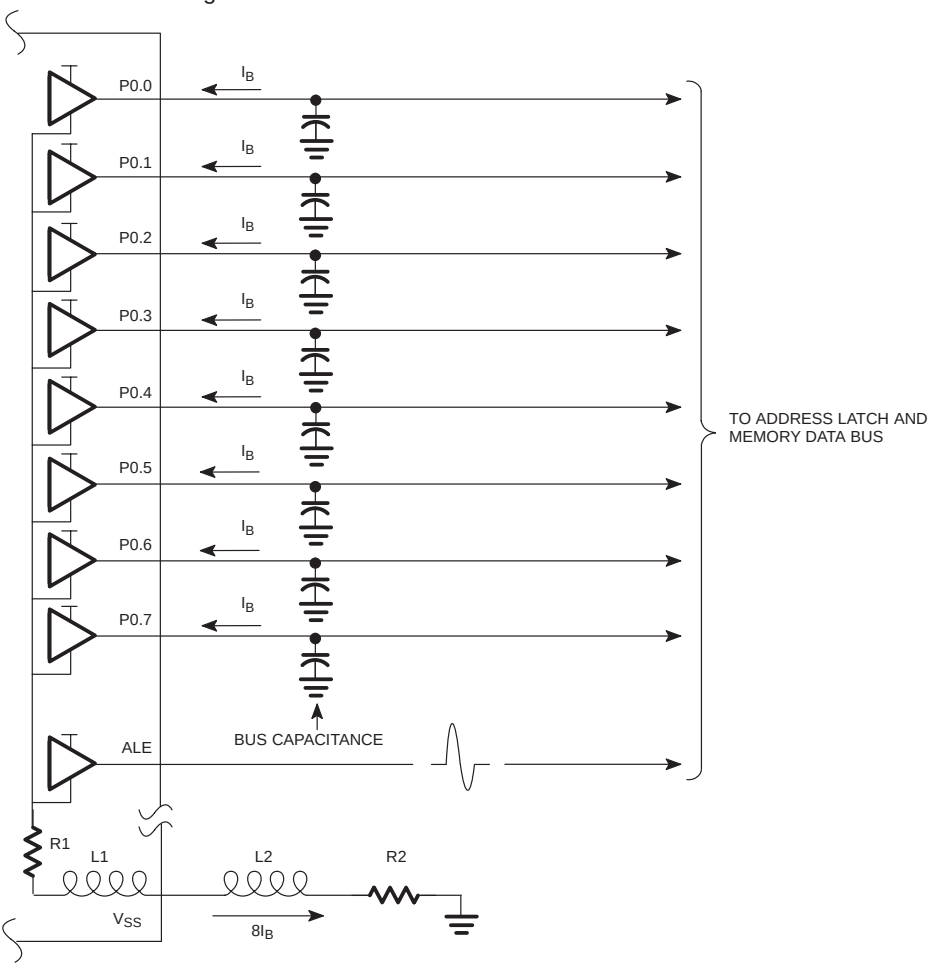


Figure 2 shows a system diagram of how the noise pulse is generated. The noise pulse is produced when the processor drives a Port 0 pin with a high address (see “A ” in Figure 1) followed by a low for data (see “D” in Figure 1). The device must sink a relatively large amount of current on each pin (I_B) to take the line from a high to low state. It is obvious that the more pins which change from a high to a low, the larger the noise. The worst case will be during a MOVX write instruction with an LSB address of FF (Hex) and a data byte of 00 (Hex). Because all eight port pins are switching simultaneously, the maximum amount of current will be drawn into the microcontroller. The combined inductance and resistance both inside the processor and in the system result in the processor internal ground rising above the system ground. This in turn induces the noise seen on ALE. The case of a MOVX read does not involve the sinking of current by the processor and should not induce significant noise on the ALE signal. System elements which have a direct relationship to the magnitude of the noise are:

1. Port 0 bus capacitance
2. System ground inductance (L2) and resistance (R2)
3. System supply voltage (V_{CC})

ALE NOISE SOURCE Figure 2



NOISE REDUCTION

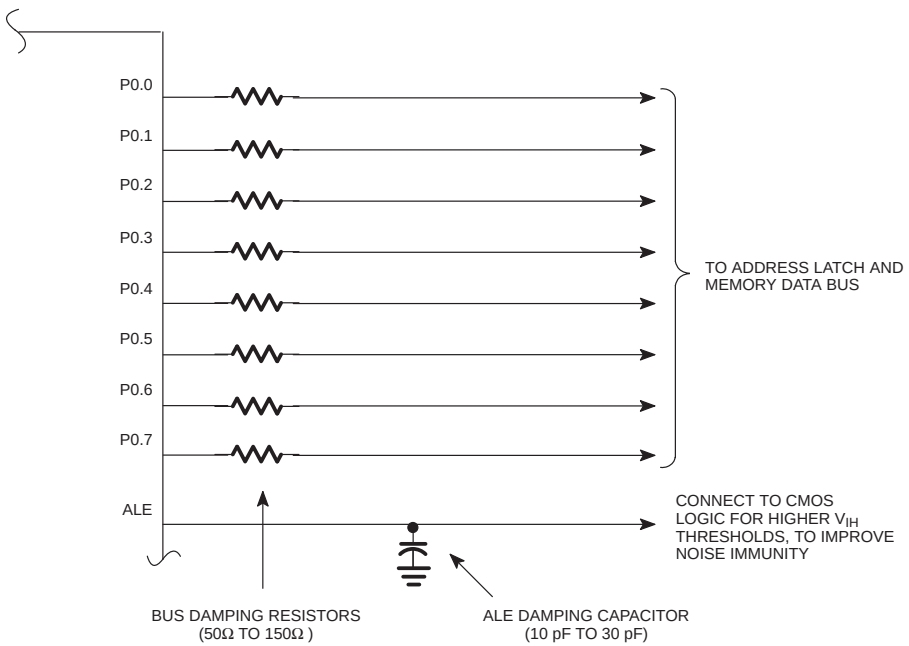
There are several techniques that can be used to minimize the effect of Port 0 switching on ALE noise. Reducing bus capacitance reduces the energy required to be discharged which results in lower peak currents and reduced peak voltages in the noise pulse. Reducing the external ground resistance and inductance also reduces the noise level, by reducing the resistive and inductive voltage drop.

The supply voltage is also directly proportional to the voltage level of the noise pulse. Maintaining V_{CC} within recommended specifications will limit the noise voltage level.

Adding low impedance resistors in series with Port 0, as seen in Figure 3, reduces the noise level by limiting the peak current drawn into the microcontroller. Care must be taken to verify that these resistors do not adversely effect the slew rate or final input voltage level to the memory as the processor writes to external memory. Values in the range of 50Ω to 150Ω can generally be used without disturbing write cycle times. Actual values for the series resistance should be verified in the end system.

Use of a capacitor on the ALE signal line will also significantly reduce the noise pulse. Again, values must be verified in the system, with care used in not reducing the slew rate of the ALE signal to a point that memory access is no longer valid. Generally a capacitance of between 10 and 30 pF is sufficient to reduce the noise level without effecting normal system operation.

NOISE REDUCTION Figure 3



INPUT THRESHOLDS

The simplest and most reliable method of eliminating the address latch related noise is to select a logic family with a high input threshold. Standard TTL, LS, FS, and HCT logic parts have a V_{IH} threshold of approximately 2.0 volts. HC (High–Speed CMOS) or AC (Advanced CMOS) logic, on the other hand, has a V_{IH} of approximately 3.5 volts at a supply voltage of 5 volts. The higher threshold level of the HC or AC CMOS logic increases the noise immunity by approximately 1.5 volts. This is generally all that is needed to prevent the undesired latching by ALE.

One disadvantage of using CMOS logic is that it is slower than other logic families. Propagation delays through CMOS logic are generally in the range of 18 ns for HC and 10 ns for AC, compared with 2 to 4 ns for FS logic when using a supply of 5 volts. For slower microcontrollers such as the DS5000, DS5001, and DS5002, the propagation delay is usually not an issue because of the slow clock rate. Faster microcontrollers such as the High–Speed Microcontrollers should carefully consider the timing effects of slower logic. In any event, testing should be done in the final application to verify the effects using slower CMOS logic.

DALLAS SEMICONDUCTOR

Application Note 92
DS5002FP Memory Expansion Techniques

OVERVIEW

All members of the Soft Microcontroller Family are designed to directly address up to 64KB of program and data memory. Occasionally, however, an application will require more memory than is available through the 64KB memory map. The Soft Microcontroller Family includes many features which make it easy to address program and/or data memory greater than 64KB. Bit–addressable I/O ports allow single instruction modification of control lines, which can be used to bank switch or page between multiple memory devices. This application note discusses the expansion of both program and data memory. It begins with an introduction to bank switching and software support techniques

BANK SWITCHING THEORY

Expanded memory access beyond 64KB is done through bank switching. This technique uses one or more general purpose I/O lines as decode lines to address more memory. If a single large–capacity memory device is used, the additional signals can be used directly as address lines. If several smaller capacity memory devices are used, the signals can be used as chip selects. The basic unit of memory switched by the decode logic is called a bank or page. For example, if an I/O line was used to switch between two 64KB EPROMs, the memory would consist of two 64KB banks.

One difficulty in implementing a bank switching scheme is the placement of the interrupt vector table. During most of the device operation, software can perform an orderly switch between banks. When an interrupt occurs, however, the device will immediately jump to the appropriate vector address, below 0030h. The software has no control over the bank configuration at this point, and the device will attempt to jump to the low end of the current bank to seek the vector table. This means that the interrupt vector table must be duplicated in each 64KB bank, so it will be available regardless of the current memory configuration. Additional space may be required if duplication of interrupt service routines is desired on each bank.

Program efficiency is maximized when bank switching is kept to a minimum, i.e. executing straight runs of code. Code efficiency will be improved if the interrupt routines (not just the vectors) are small enough to be duplicated on each bank as well. Data tables or strings accessed with MOVC instructions should be located on the same bank as the instruction.

DESIGNING A BANK SWITCHING SCHEME

The approach described in this application note selects a new memory bank without modifying the program counter. This means that the starting location in the new bank will be relative to the location of the bank switch routine in the “old” bank. Consequently, instruction location between banks is critical. Table 1 shows the timing relationship between a MOV P1, #data instruction and the switching of the bank select signal. In this example, the MOV instruction is located at location 1000h, and the first instruction on the new bank is located at 1004h. The port pin which controls the bank selection will change during the last cycle of the MOV instruction. During this cycle, the DS5002FP will already be pre–fetching the NOP instruction at location 1003h from the same bank which contains the MOV instruction. The first fetch from the new bank will be at the address following the NOP, 1004h.

There are other ways of modifying port pins, and this scheme will work with 2 cycle instructions such as MOV *direct*, *direct,* and 1 cycle instructions such as SETB *bit*. The only requirement on the bank switching instructions is that the first instruction on the new bank must be at the address following the NOP as described above.

Current Bank		New Bank	
Address	Instruction	Address	Instruction
1000h	MOV P1, #01h	1000h	??
1001h	(second byte)	1001h	??
1002h	(third byte)	1002h	??
1003h	NOP	1003h	NOP
1004h	??	1004h	[First instr.]

For bank switching to work, it is necessary to fragment the code into banks and provide a means for the software to switch between banks. The software techniques presented here show how to switch program banks "on the fly." This approach causes program execution to jump directly from one bank to another without modifying the program counter. One must exercise caution so that the bank switch will occur at a location that corresponds to the start of the next instruction in the next bank. Failure correctly align the instructions may cause the next opcode fetch to occur in the middle of a multi–byte instruction, resulting in loss of program control.

Immediately following a reset, all port pins will go to a logic one state. This means that upon a hardware reset the device will begin operating from the bank which is selected when the port pins are high. Make sure that this bank contains the correct startup code to properly initialize your application.

Many compilers and linkers directly support bank switching, and many of them include library functions for bank switching. The documentation accompanying your compiler will provide information concerning its expanded memory support.

BANK LOGIC SELECTION Table 1

P1.0	P1.1	P1.2	P1.3	Memory Selected
0	1	1	1	Program Bank 0
1	1	1	1	Program Bank 1 (default)
0	0	0	1	Program Bank 2
1	0	0	1	Program Bank 3
0	0	1	0	Program Bank 4
1	0	1	0	Program Bank 5
0	X	X	X	Data Bank 0
1	X	X	X	Data Bank 1

PROGRAMMING

The serial bootloader is designed to program one 64 KB bank of memory at a time. Multiple banks can be programmed by using the serial bootloader software to manipulate the general-purpose port pins which control bank switching. In terminal mode, this is done via the "P" command, and via the "PUT_PORT" command using the K2.EXE software available to load the DS5002FP using the DS5000TK Evaluation Kit. To properly load the program memory, the MSL bit must be cleared via the bootloader. This is done by the K2.EXE software with the RANGE 128 command or by clearing the MSL bit in terminal mode. To initialize data memory, the MSL bit should be set before doing a load operation. The procedure to load multiple banks is as follows:

1. Start the bootstrap loader.
2. Make sure the memory configuration is correct.
3. Modify the appropriate port pins to select the appropriate 64KB bank.
4. Load the software for that bank.
5. Exit the bootstrap loader.

INTERFACING TO BATTERY–BACKED SIGNALS

The memory expansion method described in this paper uses port pins in a simple fashion as bank selection controls. Please note that the port pins are not battery backed, and as such special care must be used when interfacing non–battery backed signals to battery backed circuits. This is especially important when external logic such as NAND and NOR gates are used in the address or chip select decode circuitry. The low leakage current of 74HCXX logic makes it appropriate for use in battery–backed circuits, as long as all gates of the 74HCXX logic are driven to either a high or low state during the battery backed mode. This is because the input stage of CMOS logic can draw very high current if the input is between the V_{IL} and V_{IH} levels.

The problem of floating CMOS inputs often arises in memory expansion circuits because the DS5002FP general purpose port pins (Ports 0, 1, 2, and 3) are used as inputs to battery backed logic. During battery backed mode, the port pins are tri–stated, and will float to an indeterminate state. Analog CMOS transmission gate logic can be used to isolate battery backed and non–battery logic since the source and drain of the transmis-

sion gate do not connect to the gates in the 74HCXX logic. Controls to these transmission gates, however, must be connected to battery backed signals.

A related problem can arise if battery–backed signals are connected to unpowered logic. During data retention mode, the $\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$, and $\overline{CE4}$ signals are driven to their inactive (high) state. These signals should not be connected to unpowered logic during data retention mode, or the DS5002FP will source an excessive amount of current and shorten battery life.

BANK SWITCHING EXAMPLES

Two examples are presented on the following pages. Both utilize 128KB SRAMs. This is the most cost–efficient method of implementing large amounts of memory. In this configuration, $\overline{CE3}$ serves as the A15 signal to the SRAMs, and $\overline{CE2}$ serves as A16, which is active during data memory operations. The first example is a relatively simple scheme which employs 128KB of program and 128K of data memory. Two general purpose port pins are used to select the appropriate 64KB bank in program and data memory. The second example expands this to 192KB of program and 128KB of data memory. The more complicated memory configuration of the second example requires a 74HC4053 analog switch latch to isolate the bank select signals (P1.0–3) in data retention mode.

Figure 1 shows the memory map for the first example. The P1.0 signal is used to select one of two 64KB blocks of program memory. Note that immediately following a hardware reset, bank 1 will be selected because the P1.0 signal will be high. This bank should contain the code to be executed immediately following reset. P1.1 selects which of two 64KB blocks of data memory will be used by MOVX instructions. Figure 2 shows the interconnection scheme of the hardware.

SIMPLE BANK SWITCHING EXAMPLE MEMORY MAP Figure 1

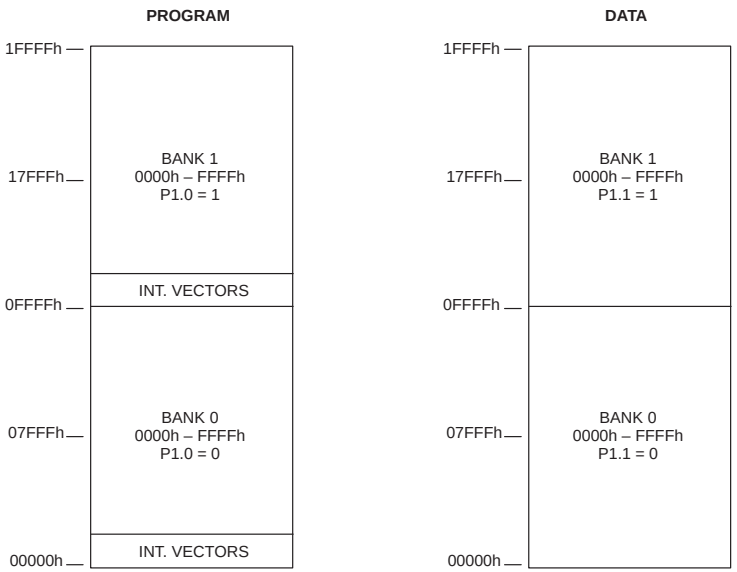
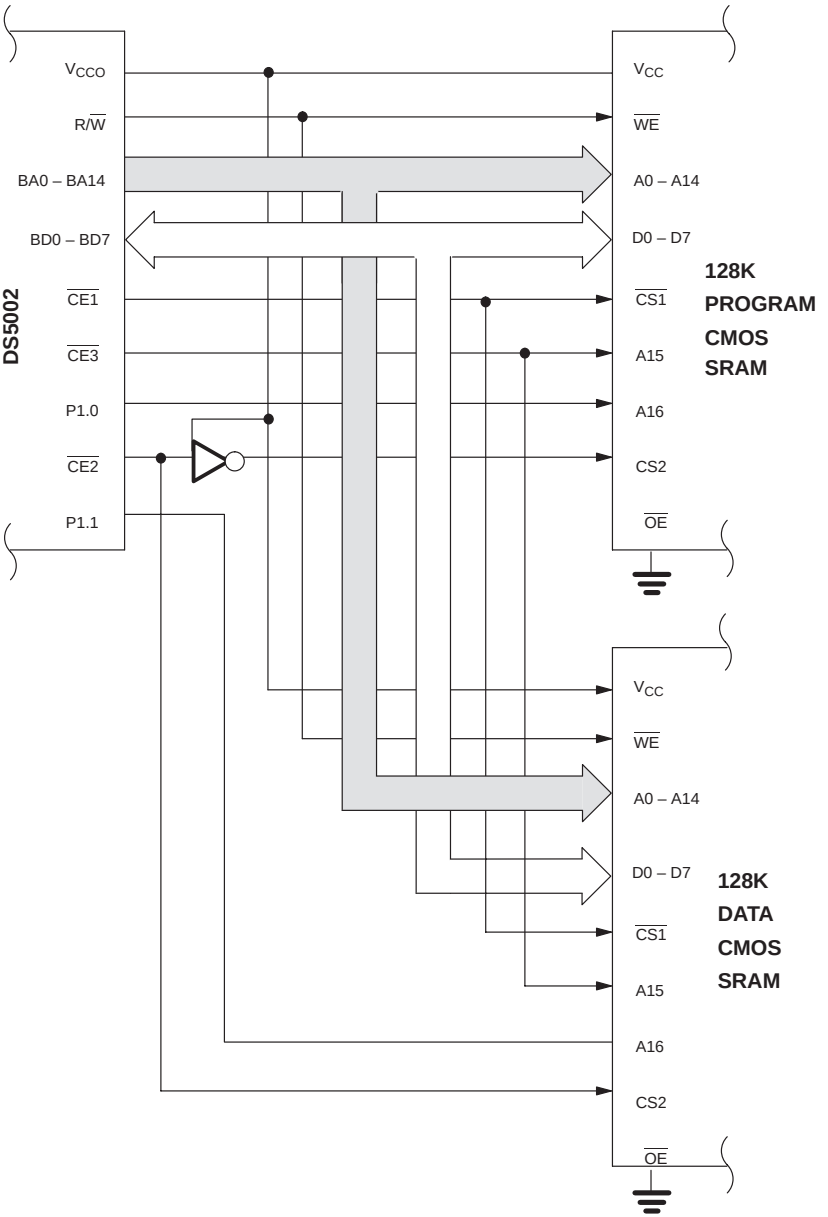


Figure 2


DS5002
VCCO
R/W
BA0 – BA14
BD0 – BD7
CE1
CE3
P1.0
CE2
P1.1
VCC
WE
A0 – A14
D0 – D7
CS1
A15
A16
CS2
OE
128K
PROGRAM
CMOS
SRAM
VCC
WE
A0 – A14
D0 – D7
CS1
A15
A16
CS2
OE
128K
DATA
CMOS
SRAM

ADVANCED BANK SWITCHING EXAMPLE MEMORY MAP Figure 3

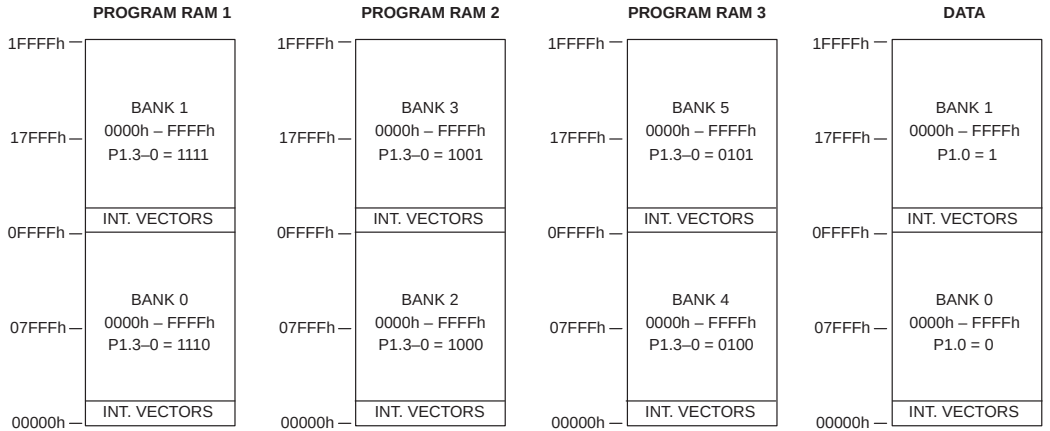
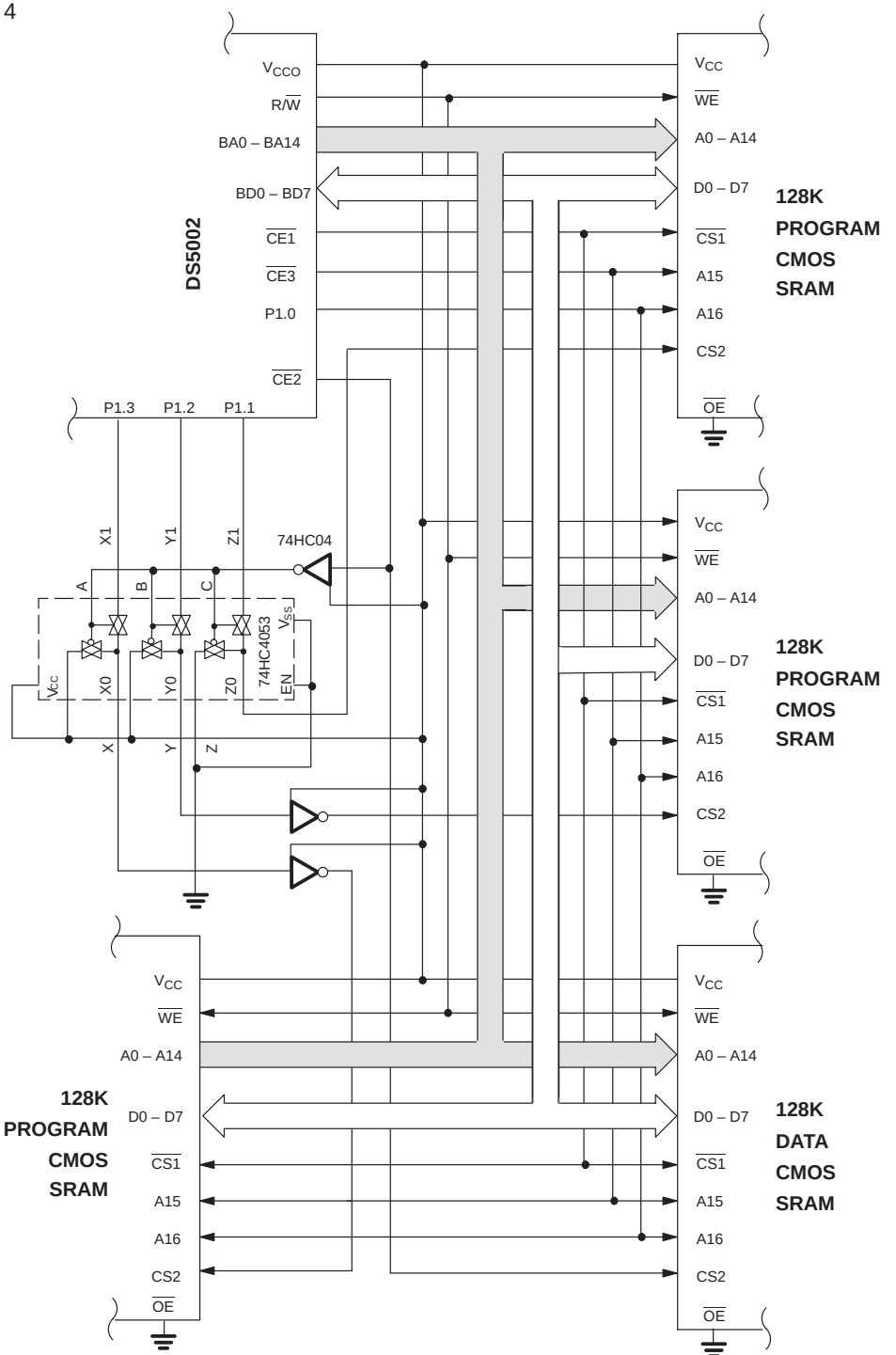


Figure 3 shows the memory map for the second example. The P1.0–3 signals are used to select one of six 64KB blocks of program memory. Note that immediately following a hardware reset, bank 1 will be selected because all port pins will be high. This bank should contain the code to be executed immediately following reset.

The decode logic through the 74HC4053 is designed so that each port pin selects one device. The bank select logic is described in Table 1. P1.0 selects which of two 64KB blocks of data memory will be used by MOVX instructions. Figure 4 shows the interconnection scheme of the hardware.

Figure 4


DS5002
VCCO
R/W
BA0 – BA14
BD0 – BD7
CE1
CE3
P1.0
CE2
P1.3
P1.2
P1.1
X1
Y1
Z1
74HC04
A
B
C
VCC
X0
Y0
Z0
74HC4053
VSS
LEN
X
Y
Z
VCC
WE
A0 – A14
D0 – D7
CS1
A15
A16
CS2
OE
128K PROGRAM CMOS SRAM
128K PROGRAM CMOS SRAM
128K DATA CMOS SRAM

DALLAS SEMICONDUCTOR

Application Note 93
Design Guidelines for Microcontrollers Incorporating NV RAM

OVERVIEW

Microcontrollers which incorporates battery–backed, nonvolatile SRAM (NV RAM) have found wide acceptance in the embedded marketplace. Unlike Flash memory or EEPROM technology, nonvolatile SRAM has no write limitations, which makes it ideal for real-time data logging applications. In products such as the Dallas Semiconductor Secure Microcontroller family, NV RAM can be used to provide in–system reprogrammable program memory.

This application note discusses design guidelines for microcontroller products which incorporate NV RAM. A number of design suggestions are presented to improve the reliability of microcontrollers which incorporate NV RAM. It should be stressed that battery–backed memory is as reliable as nonvolatile memory as long as standard CMOS design guidelines are used. This application note is applicable to the Secure Microcontroller family of products (DS5000, DS5001FP, DS5002FP, DS2250(T), DS2251T, DS2252T) as well as the DS87C530 High–Speed Microcontroller.

OUT–OF–TOLERANCE VOLTAGE SPIKES

The“real world” is a harsh place; electrostatic discharge (ESD), electrical noise, etc., can enter into a system. Many of these phenomena can induce negative voltages on one or more device pins. CMOS design guidelines require that no pin be taken above V_{CC} or below V_{SS}. Violation of this guideline can result in a hard failure (damage to the silicon inside the device) or a soft failure (unintentional modification of memory contents).

Negative voltage spikes are a particular problem for CMOS devices. When a negative voltage spike is experienced, one or more parasitic diodes inside the device can become forward–biased. This will cause the device to consume a large amount of current, and can cause the device to latch–up. In general, the only way to reverse CMOS latch–up is to remove power from the device. If the supply to the device is not limited, the excessive current draw can cause irreparable damage to the device.

Less severe, but just as troublesome, is the effect this can have on nonvolatile memory. When a parasitic diode forms, a high–current path will form. This will drain current away from the device, and may cause the voltage to sag internally. If the internal voltage drops below the minimum needed to maintain the memory, soft errors may be experienced.

In a practical application, it is often difficult or impossible to remove all voltages above V_{CC} or below V_{SS}. Realistically, overshoots or undershoots of 0.3V can be tolerated by most devices. The following cases discuss common causes of such conditions and ways to minimize their effect on systems.

PROTECTING I/O PINS

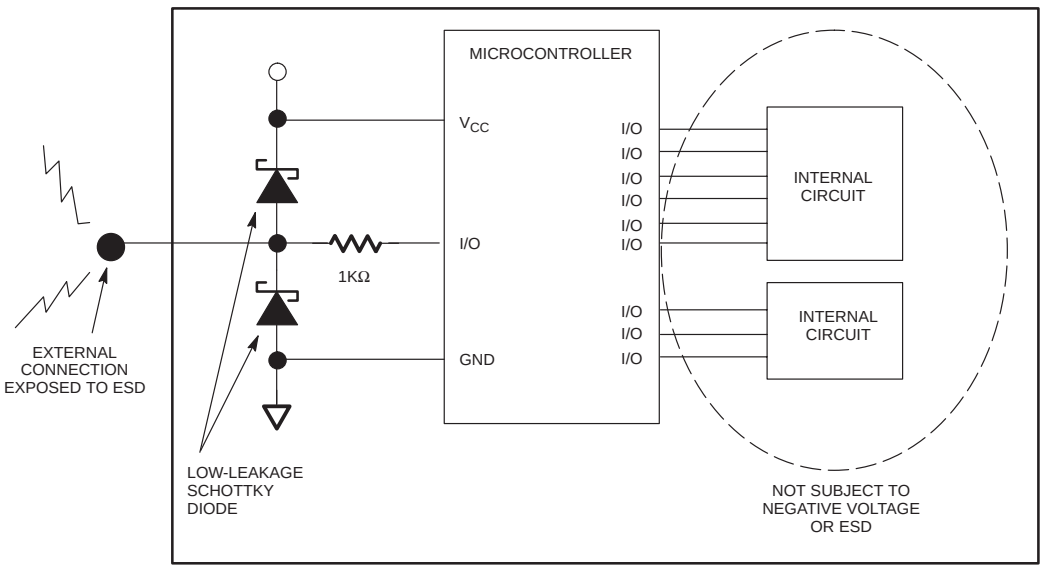
The most common way that a device experiences negative voltage spikes is through its general–purpose I/O pins. These are usually the only contact that the microcontroller has with the “outside world.” Devices such as electrical motors and keypads can generate large amounts of electrical noise. The shock that one experiences when touching a doorknob, for example, can be as much as 30KV. If this voltage is transmitted from a keypad into a microcontroller system, it can seriously damage electronic components.

Figure 1 demonstrates a diode protection scheme that can be used to protect the I/O pins of a microcontroller. The scheme relies on the use of Schottky diode and current limiting resistor to reduce the effect of current spikes on the device. When the voltage approaching the device pin exceeds V_{CC} or V_{SS} by more than 0.1V – 0.2V, the Schottky diodes will become forward biased, conducting the excess voltage away from the device pins. The current limiting resistors will also help dampen the effect of the voltage spike on the microcontroller.

The protection diodes shown in Figure 1 must be chosen carefully. Most Schottky diodes, such as the popular 1N5817, are suitable at room temperature. At high temperatures, however, their reverse bias leakage will begin to load the I/O line, making it difficult for the device to drive a logic one. For example, a DS87C520 can drive a logic one with a maximum current of 50 µA. At room temperature, the reverse leakage of a typical 1N5817 is 30 µA. At 70° C, however, the reverse leakage is greater than 100 µA. The microcontroller will be unable to source enough current to maintain a CMOS logic high of 2.4V.

Any Schottky diode used should have a leakage well below the maximum drive current of the sourcing device. Diodes with low reverse leakage currents are available from many vendors. Examples include the SC311 and SC015 diodes from Fuji Semiconductor.

EXTERNAL I/O PROTECTION SCHEME Figure 1

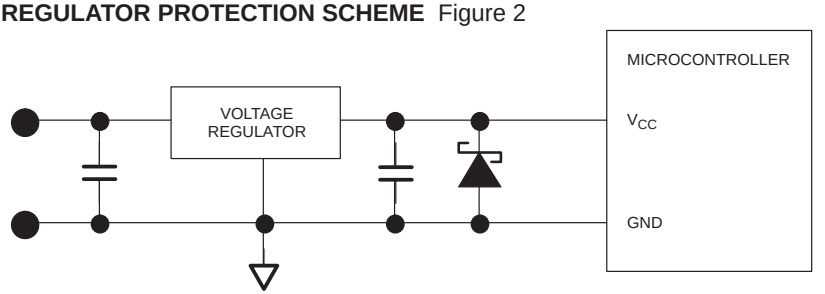


NEGATIVE POWER SUPPLY TRANSIENTS

Another source of voltage spikes is the power supply. Many simple voltage regulators, such as a 7805 5V regular are notorious for generating voltage spikes as they power up. Care must be exercised when designing the power supply so that it does not generates excessive noise when powering up or when switching loads in and out of the system.

The problem of power supply transients can be lessened by using a reverse biased Schottky diode across V_{CC} and GND, similar to that used for protecting I/O pins. Figure 2 shows one such scheme.

VOLTAGE REGULATOR PROTECTION SCHEME Figure 2



DALLAS SEMICONDUCTOR

Application Note 94
Using the Secure Microcontroller with EPROM/ROM

OVERVIEW

The Soft Microcontroller family is designed to take advantage of the many features provided by NV RAM technology. Occasionally a designer may wish to use an EPROM or other non–battery backed technology for program storage. While this sacrifices features such as the Bootstrap loader and program encryption, it will still allow a designer to use Soft Microcontroller features such as the power–fail monitor, watchdog timer and the I/O pins made available by the use of the embedded byte–wide bus. This application note addresses considerations when designing such a system using the DS5000FP and DS5001FP Soft Microcontrollers. This application note is not applicable to the DS5002FP Secure Microcontroller as it must use NV RAM to support the encryption features.

USING THE SOFT MICROCONTROLLER WITHOUT A BATTERY

The Soft Microcontroller will work reliably without a battery if a few design precautions are taken. The V_{BAT} input must be tied to V_{SS} if a battery will not be used in the design. A floating V_{BAT} input will cause unreliable device operation and/or a spontaneous reset.

Note that on DS5000FP devices revision D5 or earlier, the power–fail interrupt and power–fail reset will not work properly if V_{BAT} is tied to V_{SS}. On these devices, the V_{BAT} signal is used as a voltage reference to determine the reset trip point. The revision level is marked on each device as follows: xxxxRR–16, where RR is the revision level.

The lack of a battery means that registers that are typically nonvolatile will default to their no V_{LI} reset state. The registers shown in Table 1 should be reinitialized as part of a power–on reset routine to ensure that they are properly set. Note that upon a no V_{LI} reset the DS5001FP will be configured for a partition of 64KB and a range of 32KB. Although this is an invalid setting, the device will operate correctly below the 32KB boundary. This will allow the application software to properly configure the memory map before further execution.

NONVOLATILE REGISTERS Table 1

PCON	87h
MCON	C6h
Encryption Key	N/A
RPCTL	D8h
CRC	C1h

MIXING NVRAM AND ROM MEMORY

Many of the memory interface signals output from the Soft Microcontrollers are battery–backed in data retention mode. This ensures that the memory is write protected in the battery–backed state. While this is beneficial when using NV RAM, it can cause a problem if these signals are connected to memory which will be powered off in data retention mode.

The DS5001FP has a special version of the $\overline{CE1}$ signal that is not battery backed in data retention mode. This signal, $\overline{CE1N}$ can be directly connected to an external memory such as EPROM that will not be battery backed during data retention mode. In addition, $\overline{PE3}$ and $\overline{PE4}$ are not battery backed and can be attached to any kind of peripheral. During data retention mode the address and data lines of the microcontroller are driven to a low state, and so will not be affected by external logic.

Occasionally a design may require the connection of battery–backed signals to logic that will be unpowered during data retention mode. This is often the case if external decode logic is used to bank switch memory devices. In such instances an analog switch such as a 74HC4053 can be used to isolate the signals.

DALLAS SEMICONDUCTOR

Application Note 101
Using the Secure Microcontroller Watchdog Timer

OVERVIEW

Microcontrollers are often used in harsh environments where power supply transients, electromagnetic–magnetic interference (EMI), and electrostatic discharge (ESD) are abundant. Program corruption caused by bus corruption and electromagnetic discharges can cause a microprocessor to execute erroneous instructions. In these environments, a watchdog timer is a useful peripheral that can help catch and reset a microcontroller that has gone “out–of–control”.

A watchdog timer is a simple countdown timer which is used to reset a microprocessor after a specific interval of time. In a properly operating system, software will periodically “pet” or restart the watchdog timer. After being restarted, the watchdog will begin timing another predetermined interval. When software or the device is not functioning correctly, software will not restart the watchdog timer before it times out. When the watchdog timer times out, it will cause a reset of the microcontroller. If the system software has been designed correctly, and there has been no hardware failure, the reset will cause the system to operate properly again. The reset condition must be a “safe” state. For instance, it would not be wise to have the reset state of a magnetic stripe card reader enabling the write head.

Many systems have been designed using an external watchdog timer. The Secure Microcontroller family eliminates the need for external components by incorporating an internal watchdog timer. By moving the watchdog timer inside the microcontroller, the number of devices in the system is reduced, increasing the overall system reliability. The watchdog timer can take advantage of the high–precision crystal oscillator used by the microcontroller, rather than the imprecise RC oscillator used by most independent watchdog timers. The operation of the watchdog timer is independent of the microcontroller, unless specifically addressed via the Timed Access procedure. The possibility of an out–of–control microcontroller accidentally disabling the watchdog timer is less than 1 in 7.2×10^{16}. This application note describes the features and use of the Secure Microcontroller’s watchdog timer.

GENERAL USE OF A WATCHDOG TIMER

The primary application of a watchdog timer is as a system monitor to detect and reset an “out–of–control” microprocessor. When program execution goes awry it will not properly execute the code that restarts the watchdog. In such a case the watchdog timer will time–out and cause a microcontroller reset. In a properly designed system, the reset will correct the error.

Regardless of how capable a watchdog timer might be, there are certain failures that cannot be corrected by a reset. For instance, a watchdog timer cannot prevent or detect the corruption of data memory. Unless corruption of data affects program flow, or some extra measures are taken, data corruption will not cause a watchdog time–out. Of course, self–diagnostic software can be written in such a way as to make restarting the watchdog contingent on verification of data memory. While many applications implement such a data verification scheme, it is beyond the scope of this document.

It should be remembered that a watchdog timer cannot detect a fault instantaneously. By definition, the watchdog timer must reach the end of its time out interval before it resets the processor. The system designer should be aware of the maximum time interval that can occur between the execution of a bad instruction and the watchdog timer reset.

PLACING THE RESTART INSTRUCTIONS

In the Secure Microcontroller family, the watchdog timer is driven by the main system clock. The time–out interval is fixed at 122,800 machine cycles (1,473,600 external clock cycles). When the time–out is reached a reset will occur. Table 1 shows the reset time intervals associated with different crystal frequencies.

WATCHDOG TIME–OUT INTERVALS Table 1

CLOCK FREQUENCY	TIME–OUT INTERVAL
16.0000 MHz	92 ms
14.7456 MHz	100 ms
11.0592 MHz	133 ms
7.73280 MHz	191 ms
5.52960 MHz	266 ms
1.84320 MHz	800 ms

A primary concern is the location of the watchdog timer reset command (setting the RWT bit) in the software. The most desirable approach is to have a single location within the main loop of the system software that restarts the watchdog timer periodically. The time required to pass through the main program loop must be less than the time–out interval or the device will reset itself during normal operation. In some systems, however, the program flow is not linear enough to allow the placement of a single watchdog timer reset function. Multiple reset functions should be placed in the code, corresponding to the longest software paths.

Often a system will need to know if a watchdog timer reset has occurred. The WTR bit (PCON.4) will be set whenever this occurs, and software can test for this early in the reset sequence if a system fault has occurred. If so, the system may decide to go into a “safe” mode and alert the user to an error condition.

WATCHDOG RESET EXAMPLE

A short program illustrating the initialization and basic function of the watchdog timer is shown below. It illustrates the Timed Access feature, which prevents the accidental modification of the watchdog control bits. A Timed Access operation is a sequence of steps that must be executed together, in sequence, otherwise the access fails. The example program shows the timed access being used for restarting the watchdog and enabling its reset. Further details on Timed Access operation may be found in the Secure Microcontroller User’s Guide. The watchdog timer bits that are protected by the Timed Access procedure are the Enable Watchdog Timer Reset (EWT;PCON.2) and Restart Watchdog Timer (RWT;IP.7) bits.

```
;                WD_RST.ASM Program
;
;   This program demonstrates the use of the watchdog timer.
;   When running, the program counts on port 1 to indicate the device is
;   running and periodically resetting the watchdog timer. After counting
;   to 16, it stops resetting the watchdog timer, simulating a system fault.
;
;   The program begins by checking to see if the WTR bit is set. If so, the
;   reset was caused by the watchdog timer, and the program will execute
;   the FAULT subroutine. Port 1 is set to F0h to indicate this condition.
;   If the WTR bit is not set, the reset was caused by another source and
;   execution should continue normally.
;***********************************
RWT     EQU     0BFh            ;Reset Watchdog Timer bit
TA      EQU     0C7h            ;Timed Access Register
PCON    EQU     87h             ;Power Control Register
ACC     EQU     0E0h            ;Accumulator
P1      EQU     090h            ;Port 1

        ORG     00h             ;Reset Vector
        SJMP    START

;***********************************
        ORG     080h           ;Program starts at 80h in this example.
START:  MOV     A, PCON        ;If reset was caused by watchdog time–out,
        JB      ACC.4, FAULT   ; (WTR bit =1) execute fault subroutine.

;*********************************
;A normal power–on reset has occurred. Start initialization sequence.
        MOV     P1, #00h       ;Clear P1 to signal start of program.
```

```
;Watchdog timer initialization sequence
       MOV      TA, #0AAh     ;First restart the Watchdog timer
       MOV      TA, #055h     ;  using timed
       SETB     RWT           ;  access.

       MOV      TA, #0AAh     ;Next enable the Watchdog timer reset
       MOV      TA, #055h     ;  function using timed
       ORL      PCON, #04h    ;   access.

;*********************************
;Main program loop. This simulates a program that is operating
; correctly and then goes awry. After the program has counted to 16
; on Port 1 it will skip over the watchdog timer reset function. This
; will simulate a fault and allow the watchdog timer reset to be asserted.
;*********************************
MAIN:  MOV      R1, #0FFh     ;Create a delay loop. This simulates
LOOP1: MOV      R2, #0FFh     ; a device actually "doing something."

LOOP2: JB       P1.4, SKIP_WD_RST ;Have we been through loop 16 times?

       MOV      TA, #0AAh     ;Watchdog timer reset. In a user application it
       MOV      TA, #055h     ; should be placed at strategic locations
       SETB     RWT           ; where it will be executed periodically.

SKIP_WD_RST:
       DJNZ     R2, LOOP2
       DJNZ     R1, LOOP1

       INC      P1            ;Increment counter.
       SJMP     MAIN          ;Go back to main program loop.
;*********************************
;Watchdog time-out fault. This subroutine would normally have special
; routines to be executed in the event of a system fault. In this example,
; it disables the watchdog reset and sets Port 1 to F0h to indicate a fault.
; In a real application, this routine could either clear the fault and
; restart the software, or signal a fault and halt further operation.
;*********************************
FAULT: MOV      P1, #0F0h     ;Signal a fault
       MOV      TA, #0AAh     ;Disable watchdog timer reset
       MOV      TA, #55h      ; using timed
       ANL      PCON, #0FBh   ; access.
       SJMP     $             ;Halt further operation.
```

SUMMARY

A number of considerations must go into any design that uses a watchdog as a monitor. Once the time–out period is determined, the system software must be analyzed to determine where to locate the watchdog restart instructions. For an effective design, the number of watchdog restarts should be kept to a minimum, and some consideration should be given to the likelihood of incorrectly executing a restart. As mentioned previously, some system software is too convoluted or data dependent to ensure that all software flow paths are covered by a watchdog restart. This may dictate that a self–diagnostic software approach might be required. If there is an expected failure mechanism such as a periodic EMI burst or power supply glitch, the watchdog time–out should consider this period.

SECURE MICROCONTROLLER DEVELOPMENT TOOLS

DEVELOPMENT SUPPORT

TECHNICAL SUPPORT

Dallas Semiconductor has a wide range of service designed to support its customers. Microcontroller applications engineers are available to provide technical support from 8 am to 5 pm Central Standard Time. They can be reached by telephone and electronic mail. In addition, technical data sheets and application notes are available from the Dallas Semiconductor Fax–On–Demand service 24 hours per day. The service is operated by entering responses on a Touch Tone phone, and users should first obtain a copy of the index before ordering specific documents.

Dallas Semiconductor operates a bulletin board system which contains software examples for many of its products. The modem operates at standard baud rates up to a maximum rate of 14.4kb/s, with the settings of no parity, 8 data bits, one stop bit. It can be accessed using standard communication software.

Application Support:	(972) 371–4167 (voice)
	(972) 371–3715 (fax)
Fax–On–Demand:	(972) 371–4441
Bulletin Board:	(972) 371–4169
E–mail	micro. support@dalsemi.com

Dallas Semiconductor also maintains a presence on the Internet, with both a World Wide Web home page and anonymous ftp site. Data sheets are subject to revision, and these services contain the most current data sheet information available. The home page has access to company information, data sheets, application notes, and product information. The ftp server contains data sheets and application notes

World Wide Web home page:	http://www.dalsemi.com
Anonymous FTP:	ftp.dalsemi.com

DEVELOPMENT TOOLS

The following incomplete list of Secure Microcontroller development tool vendors is provided as a service to our customers to assist them in locating aids for use with Dallas Semiconductor microcontroller products. Dallas Semiconductor neither recommends, warrants for suitable use, nor provides technical support for any product not manufactured by Dallas Semiconductor. The inclusion or exclusion of any vendor from this list is in no way a reflection of the vendor or the product. Contact Dallas Semiconductor for a list of third–party hardware and software tool vendors.

ASSEMBLERS

The Secure Microcontroller family is 8051 instruction set and object code compatible. This means that standard 8051 assemblers will generate the correct code. Dallas Semiconductor microcontrollers have numerous extra features, but no extra instructions. The unique features are all accessed via Special Function Registers. These should be defined in the user's software via equate statements. In this way, the user identifies the new registers, allowing the full range of instruction operations. Once defined by the user, the new SFR will receive the same treatment as any of the standard ones. The assembler has no knowledge of the actual hardware associated with any SFR.

An Intel Hex file format is required by the Bootstrap Loader built into each device. This is a standard out put file format for all 8051 compatible assemblers. Note, a utility may be required to create the Intel hex file. That is, some assemblers generate a binary file as the standard output. This file may then pass through a utility that converts object to hex. In all cases, the utility will be included with the assembler.

For the convenience of the user, the following is a list of the SFRs that are unique to the Secure Microcontroller family and their equate locations. Simply include the relevant values in the program source file.

Name	Symbol	Equate Location
RPC Status	STATUS	0DAh
RPC Control	RPCTL	0D8h
Random Number	RNR	0CFh
Timed Access	TA	0C7h
Memory Control	MCON	0C6h
CRC High Value	CRC_HIGH	0C3h
CRC Low Value	CRC_LOW	0C2h
CRC Control	CRC	0C1h

HIGH LEVEL LANGUAGE COMPILERS

There are two languages that are commonly used in microcontroller system design. They are BASIC and C. Although BASIC interpreters have been created for the 8051 family, a compiler is normally preferable. A BASIC compiler specifically for the Secure Microcontroller family is available from Systronix. Systronix package supports Soft Micro memory mapping, Watchdog Timer, Real–time Clock and other features in addition to BASIC language support for the 8051 family.

Like assembly language, standard 8051 C compilers can be used with the Secure Microcontroller family. The compiler must be informed of the existence and location of new SFRs that it will be accessing. There is one important note. When using C, it is commonly necessary to identify the starting address for various read/write segments such as XDATA and STACK. This may be done using a start–up file. When using a device with a Partitioned memory map, the default value of 0000h for such segments is not advisable. The NV RAM area will begin at the logical Partition address. Therefore, the segments that require RAM beyond the 128 scratchpad locations should be located in the memory map at an address that is above the Partition. For example, if the Partition is located at address 4000, this is also a suitable beginning address for the STACK.

PROGRAMMERS

The Secure Microcontroller provides its own built–in programming support with its Bootstrap Loader. This allows the device to be programmed while installed in system or in a simple user fixture. Serial programming is preferred as a general technique as the easiest and fastest method. The DS5000TK Evaluation Kit available from Dallas Semiconductor can also be used as a programmer. For more information please consult the DS5000TK Evaluation Kit User's Guide in the back of this data book.

EMULATORS

A Secure Microcontroller emulator is available from Nohau Corp. The Nohau emulator provides development support for the 80–pin QFP version of the DS5000FP or DS5001FP. Using the QFP, a breadboard can be constructed of the user's system, even if the end version will use a module. Simply follow the guidelines for memory connection in the User's Guide section of this book. The DS5001FP, essentially a DS5002FP without security features, can be used to emulate the DS5002FP if needed.

DALLAS SEMICONDUCTOR

DS907x
SIP Stik Connectors

FEATURES

- Provides snap–in connection between SIP Stiks and motherboard
- Low insertion force, redundant contacts
- Contact manufacturer directly for more detailed specifications:
  - AMP Inc. 1–800–522–6752, +1–717–986–7777
  - Molex Inc. 1–800–786–6539, +1–630–969–4747

Part Number	Description	Ref. Mfg. Part #	Length (in.)
DS9072–40V	40 contact vertical position 050" pitch	MOLEX 15–82–0796	2.950
DS9072H–40R	40 contact high profile right angle position .050" pitch	AMP 4–382486–0	2.950
DS9072L–40R	40 contact low profile right angle position .050" pitch	AMP 4–382480–0	2.950
DS9072–72V	72 contact vertical position 050" pitch	AMP 821824–8	4.550
DS9072H–72R	72 contact high profile right angle position .050" pitch	AMP 7–382486–2	4.550
DS9072L–72R	72 contact low profile right angle position .050" pitch	AMP 7–382480–2	4.550

40–position DIP–to–SIP and SIP–to–DIP adaptors for development of DS2250 Micro Stik products.

Part Number	Description
DS9075 – 40V	SIP–to–DIP Adaptor 40 contact, horizontal DIP plug with 40 contact, low profile verical position, .050 pitch SIMM connector
DS9076 – 40	DIP–to–SIP Adaptor 40 contact, .050 pitch, vertical SIMM edge card with 40 contact, vertical DIP socket.

DALLAS SEMICONDUCTOR

DS907x
SIP Stik Connectors

FEATURES

- Provides snap–in connection between SIP Stiks and motherboard
- Low insertion force, redundant contacts
- Contact manufacturer directly for more detailed specifications:
  - AMP Inc. 1–800–522–6752, +1–717–986–7777
  - Molex Inc. 1–800–786–6539, +1–630–969–4747

Part Number	Description	Ref. Mfg. Part #	Length (in.)
DS9072–40V	40 contact vertical position 050" pitch	MOLEX 15–82–0796	2.950
DS9072H–40R	40 contact high profile right angle position .050" pitch	AMP 4–382486–0	2.950
DS9072L–40R	40 contact low profile right angle position .050" pitch	AMP 4–382480–0	2.950
DS9072–72V	72 contact vertical position 050" pitch	AMP 821824–8	4.550
DS9072H–72R	72 contact high profile right angle position .050" pitch	AMP 7–382486–2	4.550
DS9072L–72R	72 contact low profile right angle position .050" pitch	AMP 7–382480–2	4.550

40–position DIP–to–SIP and SIP–to–DIP adaptors for development of DS2250 Micro Stik products.

Part Number	Description
DS9075 – 40V	SIP–to–DIP Adaptor 40 contact, horizontal DIP plug with 40 contact, low profile verical position, .050 pitch SIMM connector
DS9076 – 40	DIP–to–SIP Adaptor 40 contact, .050 pitch, vertical SIMM edge card with 40 contact, vertical DIP socket.