SECTION 5: MEMORY INTERCONNECT

The Secure Microcontroller family is divided between chips and modules. This sections illustrates the memory interconnect for the various chips and shows block diagrams of selected modules. The Soft Microprocessor chips are 80–pin QFP packages that connect to low power CMOS SRAM. The SRAM connection is made through the Byte–wide bus. When using a chip, the user must connect this Byte–wide bus to the RAM as shown in this section. In module form, the bus is connected inside the package. Table 5–1 shows some of the preferred RAM choices. Note that any standard SRAM will work, but data retention lifetime is dependent on RAM data retention current and battery capacity. Lower currents naturally allow the use of smaller batteries. This is covered in detail in Section 6.

RECOMMENDED SRAMs FOR USE WITH SOFT MICROCONTROLLERS Table 5–1

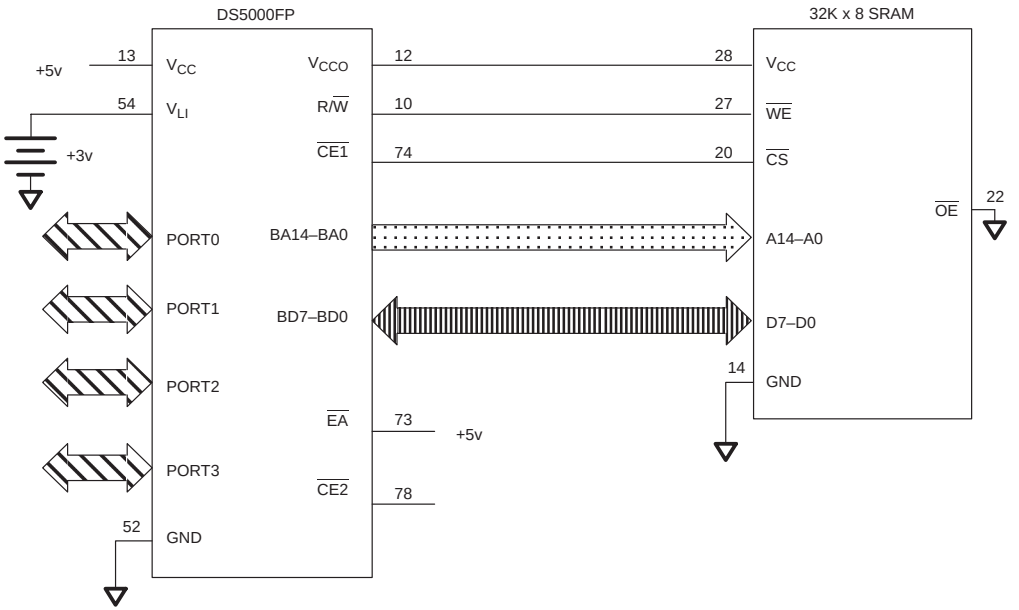
RAM SIZE	VENDOR	PART NUMBER	DATA RETENTION CURRENT 25°C	DATA RETENTION CURRENT 40°C	DATA RETENTION CURRENT 70°C
8K x 8	Dallas	DS2064	0.05 µA	–	–
8K x 8	Sharp	LH5168	–	–	0.6 µA
32K x 8	Hitachi	HM62256LP–SL	–	3 µA	10 µA
32K x 8	Mitsubishi	M5M5256BP–LL	1 µA	–	10 µA
32K x 8	Sony	CXK58257AP–LX	1 µA	2 µA	10 µA
32K x 8	Sony	CXK58527AP–LLX	0.3 µA	0.6 µA	3 µA
128K x 8	Hitachi	HM628128LP–SL	1 µA	–	10 µA
128K x 8	Mitsubishi	M5M51008P–LL	1 µA	–	10 µA
128K x 8	Sony	CXK581000P–LL	1.2 µA	2.4 µA	12 µA

Recommended RAMs are given with the manufacturers specified data retention current at 3V. Missing numbers are conditions unspecified by the manufacturer.

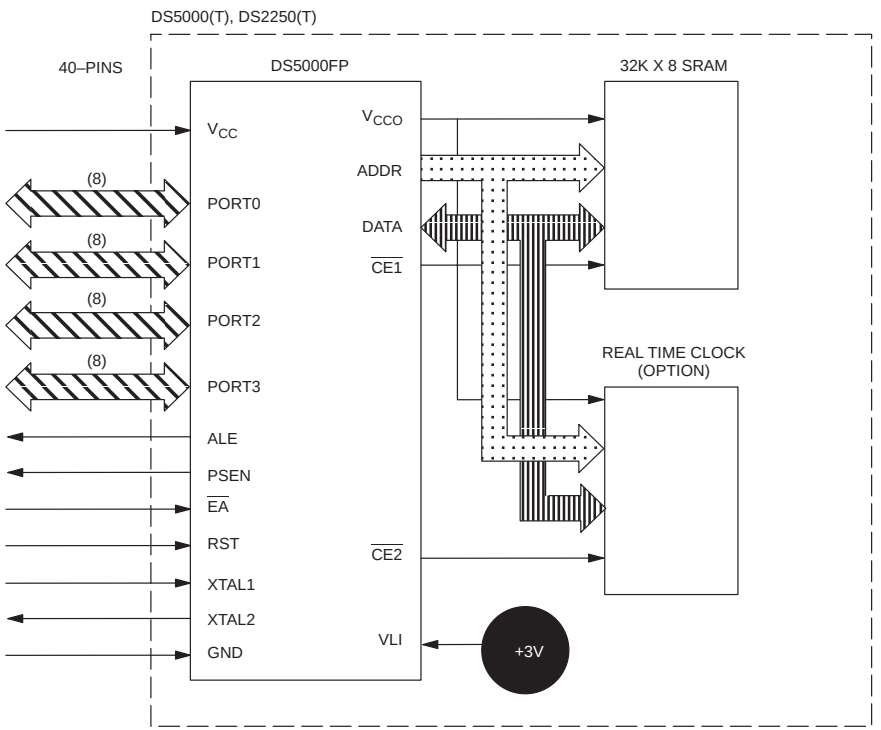
In the case of the DS5000FP, the microprocessor can connect to either one or two SRAMs. They can be 8K bytes or 32K bytes, though the case of two 8K RAMs is unlikely from a cost perspective. Figure 5–1 illustrates the memory connection of a DS5000FP connected to one 32K x 8. $\overline{CE1}$ provides the chip select, and R/$\overline{W}$ supplies the $\overline{WE}$ signal. A second RAM could be added by simply using $\overline{CE2}$ as the chip enable with a common connection for the other signals.

In the case of DS5000 based modules including DS5000(T) and DS2250T, the SRAM is connected as described above. Connections running between the micro chip and RAM are not available at the pins. The DS2250–64 has a second SRAM on $\overline{CE2}$. The timekeeping versions also have the real–time clock connected to $\overline{CE2}$. A block diagram in Figure 5–2 shows the module configuration with 32K RAM and a real–time clock. This is identical for DS2250 or DS5000 modules. These are functionally identical and only differ in form factor.

MEMORY INTERCONNECT OF THE DS5000FP Figure 5–1



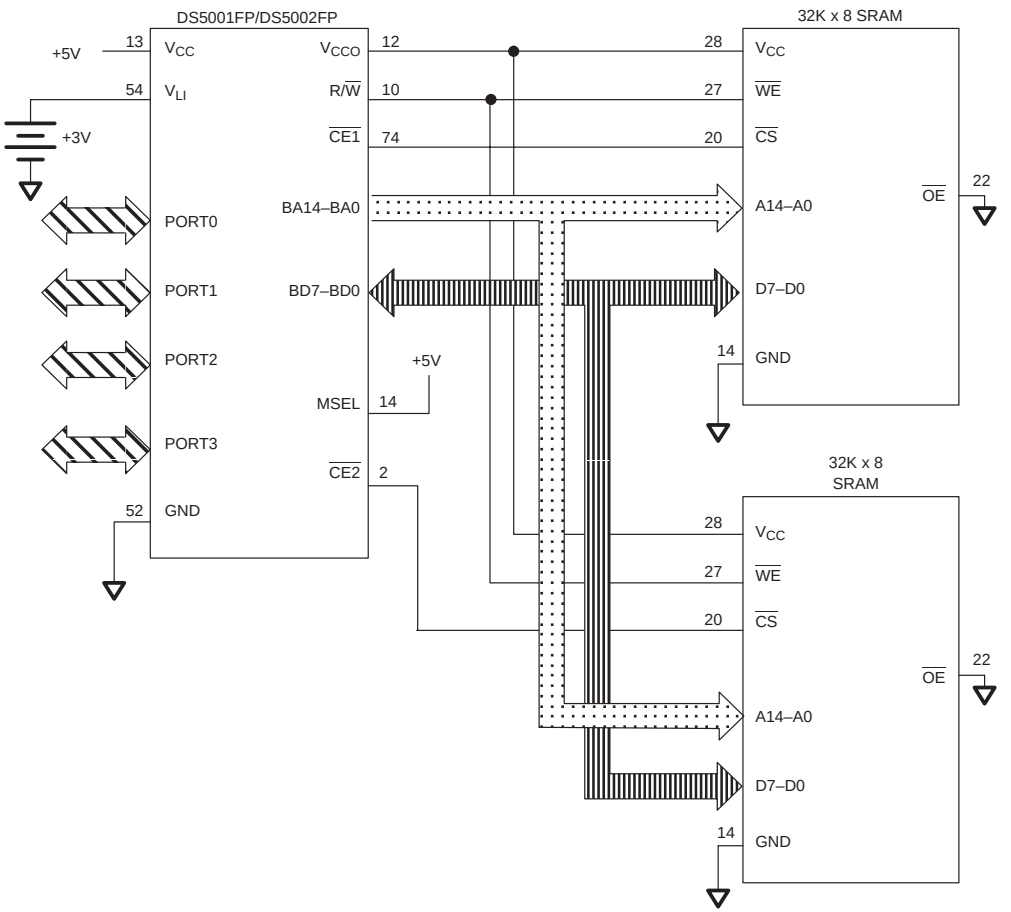
DS5000 SERIES MODULE BLOCK DIAGRAM Figure 5–2



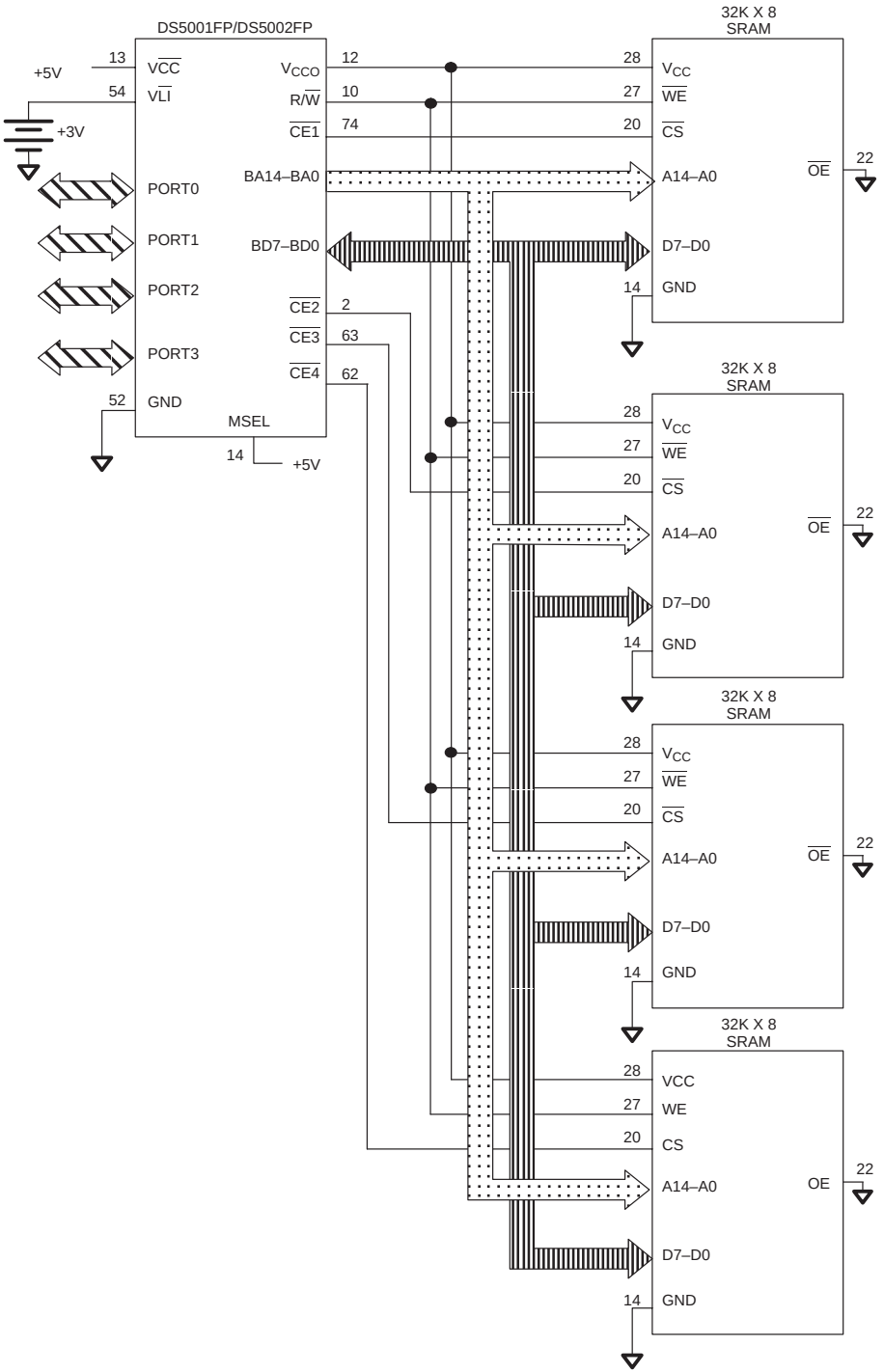
The DS5001FP has several memory options. It can be connected to between one 8K byte SRAM and four 32K byte SRAMs. It will also support one 128K byte SRAM. In most cases the DS5001FP is used for its greater memory access so it will not be used with 8K RAMs. In the Partitionable mode (see Section 4), the DS5001FP can be connected to one or two SRAMs. Figure 5–3 illustrates the connection of two 32K x 8 SRAMs. Each RAM has its own chip enable, with a common $\overline{WE}$ generated by the DS5001FP R/$\overline{W}$ signal. When using the DS5001FP with only one RAM, the second chip enable will simply remain unconnected. This solution provides a total of 64K bytes of memory which the user can partitions into program and data segments. The Partition setting has no impact on the interconnect. Using the Partition, the microcontroller determines which memory blocks are program and write protects the appropriate addresses.

In the non–partitionable case, the DS5001FP can be connected to three or four 32K x 8 SRAMs. The four RAM case is shown in Figure 5–4. Each RAM has its own chip enable. To use three RAMs, simply omit the unused chip enable ($\overline{CE2}$ or 4) as described in Section 4. In other ways, this hardware configuration is similar to the Partitionable mode discussed above. While this provides the full 128K bytes of memory, it requires more space and cost than the version shown in Figure 5–5. This uses the 128K byte SRAM. All program and data memory is contained within the single chip. The DS5001 manages the addressing and decoding. Note the MSEL signal is connected to ground to initiate this mode. The PM bit and Range must still be configured by the user during program loading.

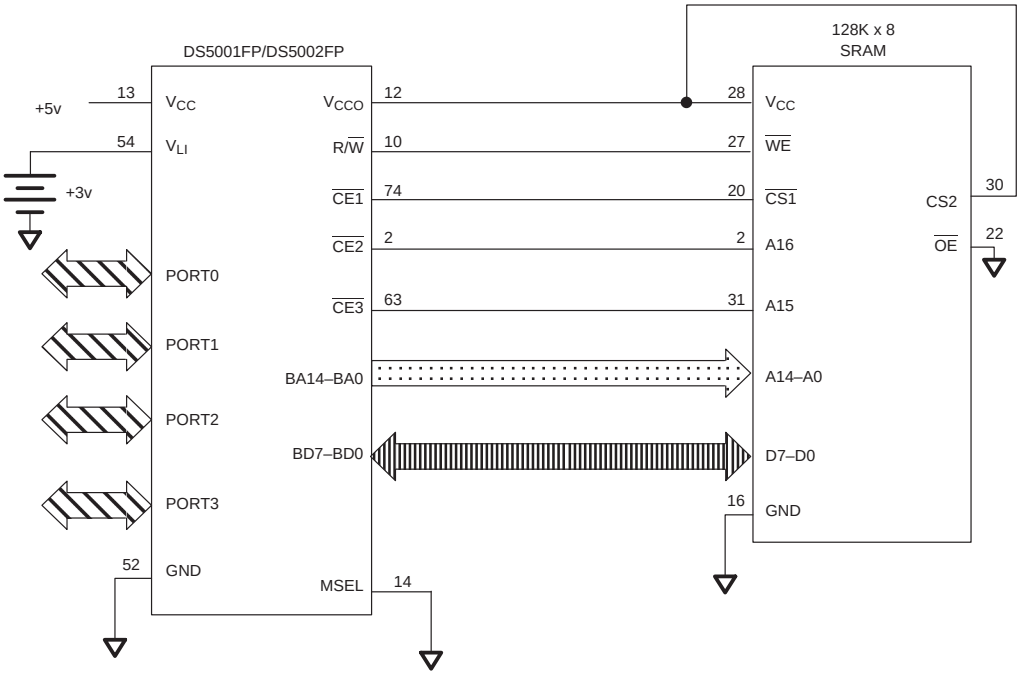
MEMORY INTERCONNECT OF THE PARTITIONABLE DS5001/DS5002 Figure 5–3



MEMORY INTERCONNECT OF THE NON–PARTITIONABLE DS5001FP, DS5002FP Figure 5–4



MEMORY INTERCONNECT USING THE 128K SRAM Figure 5–5

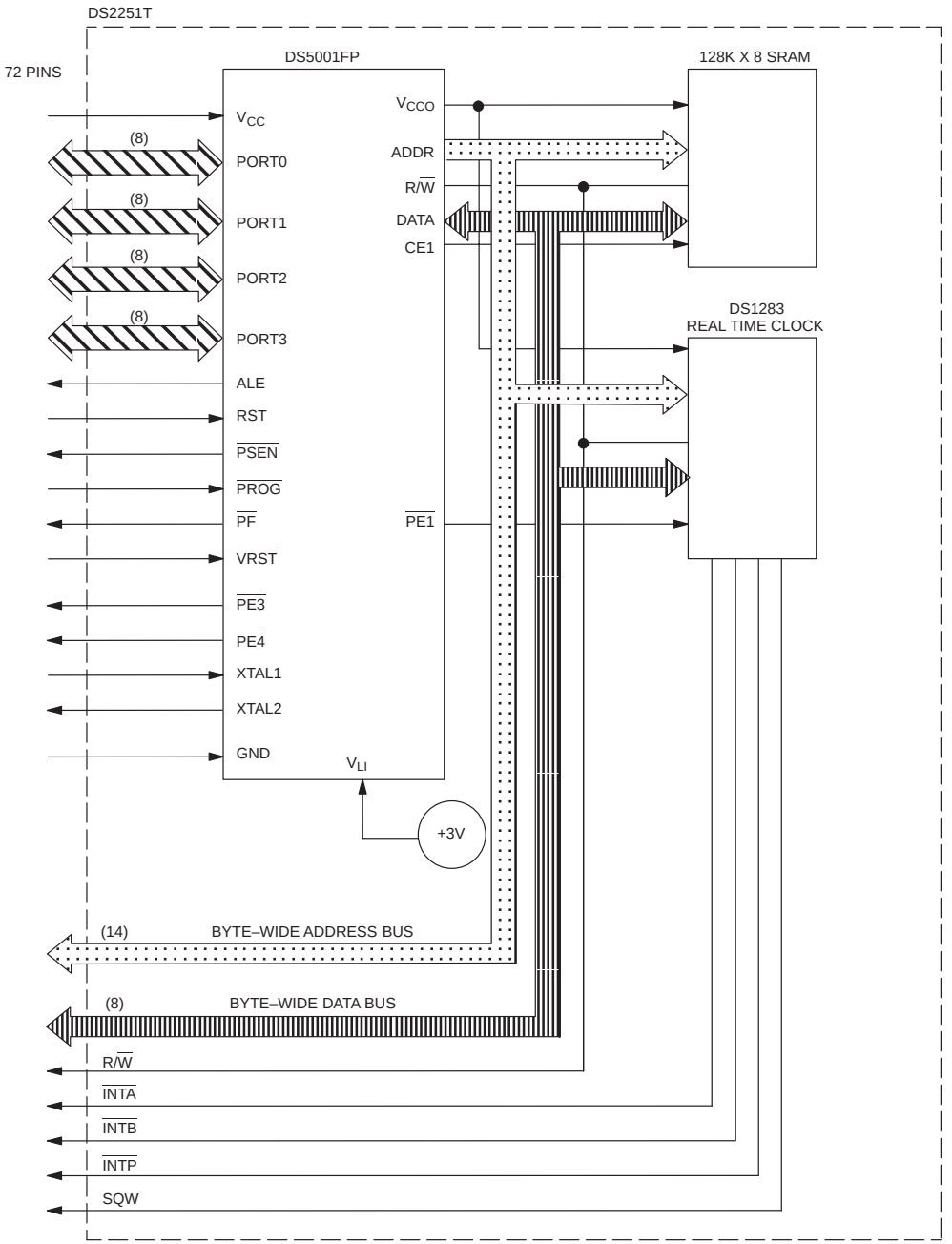


In the 128K x 8 configuration, the microprocessor converts the $\overline{CE3}$ into A15 and $\overline{CE2}$ into A16. Grounding the MSEL pin causes this configuration. The physical location of program memory will be between addresses 00000 to 0FFFFh. Data memory will be located between 10000h and 1FFFFh. These physical locations are transparent to the user. From a software perspective, both program and data are located between 0000 and FFFFh. When the MSEL pin is grounded, the device cannot be partitioned. The MSL bit accessed through the bootstrap loader is used to select access to the 64KB data or 64KB program segment via the loader in the 128K x 8 configuration.

The Soft Microcontroller line has two modules based on the DS5001 series. The DS2251T 128K Micro Stik uses a DS5001FP. The DS2252T Secure Micro Stik is based on the DS5002FP. All computing features are derived from the DS5001. The DS5002 device provides memory security features in addition. The modules are available in 32K, 64K, and 128K byte versions. Two example block diagrams are shown below.

Figure 5–6 is a block diagram of the DS2251T with 128K bytes of NV RAM. This part can also be built with 32K or 64K bytes. In this case, the 128K RAM is replaced with one or two 32K byte RAMs. Figure 5–7 shows a DS2252T with 32K bytes of RAM. This part is also available in 64K or 128K byte versions. For 64K, two RAMs are used. For 128K, the single 128K SRAM is used. This is entirely transparent to the user and is provided for completeness.

DS2251T–128 BLOCK DIAGRAM Figure 5–6



DS2252T–32 BLOCK DIAGRAM Figure 5–7