DALLAS SEMICONDUCTOR

Application Note 1
Pulse–Doublers Using the DS1012 Delay Line with Logic

FEATURES

- All Silicon Delay Line with logic
- Low Power Operation: 53 μW max quiescent mode
- Two input device/four independent buffered delays
- TTL/CMOS compatible
- Quick turn prototypes available through LPP
- Custom delays and logic options available
- Logic Options: AND, NAND, OR, NOR, XOR, XNOR, HALF–XOR, HALF–XNOR
- Delay tolerance: ±1.5 ns (delays: 3–10 ns)
  ±2.0 ns (delays: 11–40 ns)
- Vapor phase, IR and Wave Solderability
- Small Outline Packaging Available (150 mil Mini–SOIC)

APPLICATIONS

- Pulse Doublers
- Voltage Control Oscillator (VCO)
- Waveform Generation
- Manchester Encoder

DS1012 BACKGROUND

Description

The DS1012 delay line is probably one of the most unique product offerings in the Dallas Semiconductor delay line family. Not only can simple delays be obtained from the device, but also delays combined with logic functions. Figure 1 presents the general logic diagram for the DS1012 Delay Line. As shown, the device is provided with two inputs and four outputs. Outputs 1 and 2 are straight delays of inputs 1 and 2, respectively. These outputs can also be configured to provide delayed complements of the inputs if desired. Outputs 3 and 4 are combinations of inputs 1 and 2 having both a delayed and logic relationship. Function F3 can provide the functions AND, HALF–XOR, a straight delay of D3 or a complement of these functions. Similarly, function F4 can provide the functions OR, XOR, a straight delay or their complements.

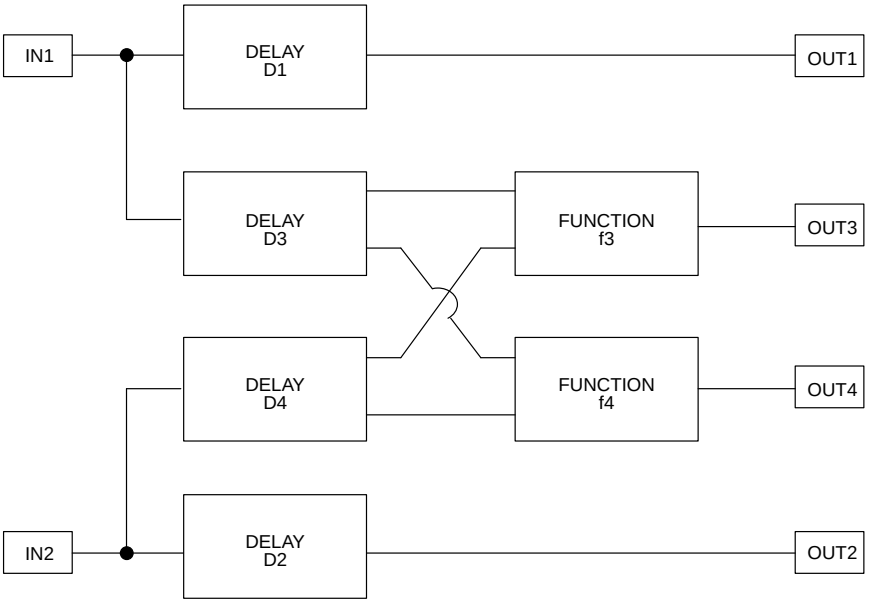
Specifying a Custom DS1012

As a product, the DS1012 has seen most use in custom applications where users of this device wish to develop custom waveforms by specifying both delay and logic combinations. Dallas Semiconductor, through late package programming (LPP), has the ability of providing (to customer specifications) customized parts for evaluation and testing usually within a 10–day period.

The DS1012, as shown in Figure 1, can be configured with numerous options ranging from simple delayed outputs to delayed outputs combined with logic. When determining new applications for the DS1012, delay and/or logic specifications must adhere to rules provided in Table 1 and/or Device Notes. There exist two major considerations which must be made when selecting the device for a particular application; namely, operating frequency and delay/logic available. The operating frequency (input signal, duty cycles, etc.) is in large part dependent of delay values chosen. Additionally, delay values D1, D3 and D2, D4 are related in terms of what values can be selected for the pairs. In any configuration D1 and D2 can be specified between the range of 4 ns and 10 ns, and D3 and D4 can be specified between the range of 4 ns and 40 ns. However, if D1 is greater than 10 ns, then D3 must be equal to D1. Similarly, if D2 is greater than 10 ns then D4 must be equal to D2. Table 1 and the Device Notes should be used to check the validity for values of delay and logic chosen.

Once the values of D1, D2, D3, and D4 have been made, determination of input pulse width and period can be made. For example, the DS1012–001 is configured with delays D1=5 ns, D2=5 ns, D3=10 ns and D4=10 ns. The minimum input pulse width, t_{WI}, for the device is specified by three times the longer of D1, D2, D3, or D4 or in this case 30 ns. The minimum period, T, will be equal to twice t_{WI} or 60 ns. Pulse doublers are configured to exceed the limitations of minimum period and input pulse width as shown in the Device Notes. Here the minimum input pulse width approximates the longer of the delays D1, D2, D3 or D4.

DS1012 LOGIC DIAGRAM Figure 1



AC ELECTRICAL CHARACTERISTICS Table 1

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}				ns	1
Input to Output (leading edge)	t_{D1}, t_{D2}, t_{D3}, t_{D4}				ns	2
Power-up Time	t_{PU}			0	ns	3
Period	T	2(t_{WI})			ns	

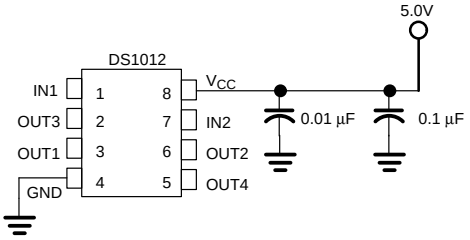
Device Notes

1. For specified accuracy, t_{WI} (min) is the longer of $3(t_{D1})$, $3(t_{D2})$, $3(t_{D3})$, or $3(t_{D4})$. Pulse doublers designed for single frequency use will meet specified accuracies at 50% duty cycle; i.e., $2(t_{WI})$ = 1/FREQ = PERIOD. Customs will be adjusted to be accurate at customer input width specifications when t_{WI} is longer than t_{D1}, t_{D2}, t_{D3}, and t_{D4}.
2. V_{CC} = 5V @ 25°C. Delays referenced to leading (input rising) edges are accurate within ±1.5 ns for values between 3 to 10 ns and ±2 ns for values between 11 to 40 ns. Delays referenced to trailing (input falling) edges will typically equal the corresponding leading edge delay within ±1 ns.
3. On power-up, the DS1012 will supply timing and logic functions with specified accuracy as soon as V_{CC} achieves nominal value.

Power Supply Conditioning

The DS1012 is recommended for operation with supply voltages between 4.75V (min) and 5.25V (max). Output delay is typically affected by supply voltage and can vary 15% over the 4.75V to 5.25V range. In most applications it is recommended that the power supply be decoupled as shown in Figure 2.

POWER SUPPLY CONDITIONING Figure 2



Package Options

The DS1012 is available in two different package options, the 8–pin DIP (300 mil, DS1012M–xxx) and the 8–pin mini–SOIC (150 mil, DS1012Z–xxx). Package dimensions can be found in the appropriate Dallas Semiconductor data book.

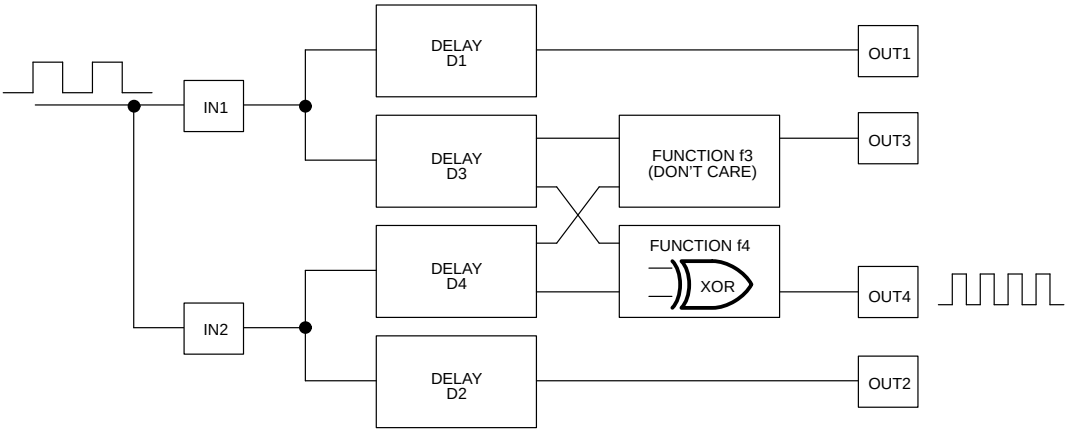
PULSE–DOUBLER APPLICATIONS

The function of a pulse doubler is to produce two output pulses from a single input pulse. Pulse and frequency doublers are implemented in a variety of ways. Some devices use PLL technology to double the frequency of the input. These devices require synchronization and lock times in the tens to 100s of milliseconds to generate the doubled output. Some designs employ the use of discrete delays, buffers, and logic to generate the desired output. Discretes provide the feature of no synchronization and lock times, however, multiple components, and additional board space are required. The DS1012 can be configured to provide, through a combination of logic and delay, a pulse doubler for a specified input waveform. Unlike the discrete approach, all device technology resides in one package (see Figure 1). Additionally, the device does not use PLL technology and thus requires no synchronization or lock times for generating the pulse doubler output.

A logic diagram of the DS1012 configured as a pulse–doubler is presented in Figure 3. Inputs 1 and 2 are driven by the same input signal. Delays D3 and D4 are typically set so that the time difference between the two is equal to a quarter period of the input wave to be doubled. This setup gives an output waveform of 50% duty cycle as shown in Figure 4a. Figures 4b and 4c show waveform outputs as the time difference between delays D3 and D4 change with respect to the period of the input waveform. These figures illustrate how output waveforms can be shaped in addition to doubling. The doubled output is taken from OUT4. If delay D1 and D3 are equal in value, the OUT1 and the doubled output, OUT4, will be in–phase. OUT3 in the doubler application is most often a don't care. A circuit diagram of this configuration is shown in Figure 5.

The D–series of DS1012s (DS1012–D16, DS1012–D20, DS1012–D25, and DS1012–D33) have been configured through delay and logic selection to operate as pulse doublers; a function that is finding considerable use in the PC upgrade market. The typical requirement for the PC upgrade market is to make use of the existing system clock by using some combination of delay and logic to double the clock for use with a faster processor. The DS1012 is an ideal platform to provide the doubler function since a combination of delay and logic is present in the same package. Additional board space and cost savings can be realized by using the tiny 150 mil mini–SOIC package.

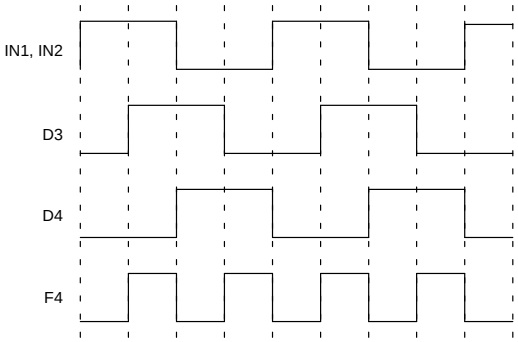
DS1012 PULSE–DOUBLER LOGIC DIAGRAM Figure 3



|D3–D4| = T/4, where T = period of the input pulse.

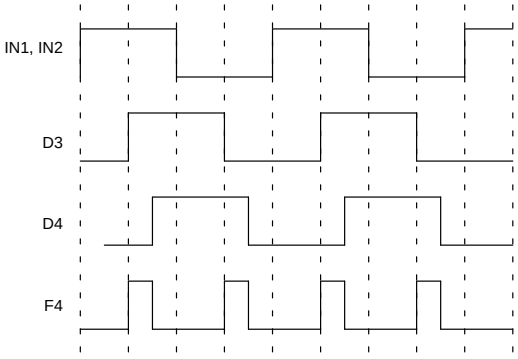
DELAY TIMING DIAGRAM Figure 4

(a)



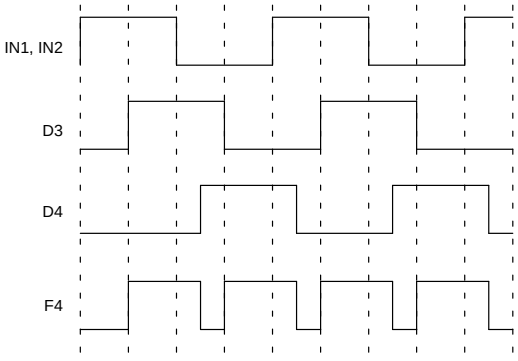
|D3–D4| = T/4 where T = period

(b)



|D3–D4| < T/4 where T = period

(c)



|D3–D4| > T/4 where T = period

DS1012 PULSE–DOUBLER CIRCUIT DIAGRAM Figure 5