

DALLAS
SEMICONDUCTOR

Application Note 345
DS2141A, DS2151, DS2152
Programming, SLC-96^R

In a SLC-96 based transmission scheme, the standard Fs bit pattern is robbed to make room for a set of message fields. The SLC-96 multiframe is made up of six D4 superframes, hence it is 72 frames long. In the 72 frame SLC-96 multiframe, 36 of the framing bits are the normal Ft pattern and the other 36 bits are divided into alarm, maintenance, spoiler, and concentrator bits as well as 12 bits of the normal Fs pattern. Please see the BellCore document TR-TSY-000008 for more details about SLC-96.

Receive Side SLC-96 Applications

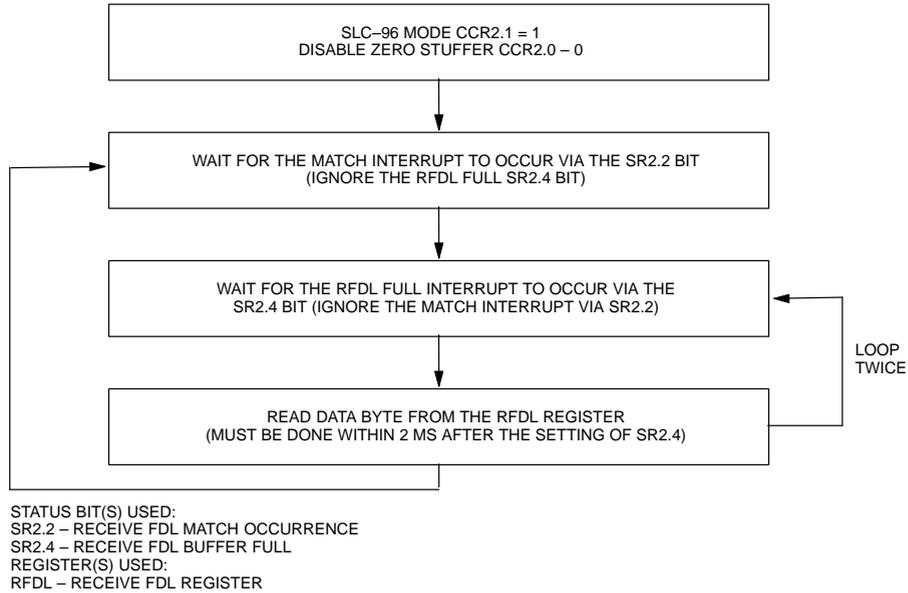
To enable the DS2141A, DS2151 or DS2152 to synchronize onto a SLC-96 pattern, the following configuration should be used:

set to D4 framing mode	CCR2.3 = 0
set to cross-couple Ft & Fs bits	RCR1.3 = 1
set to minimum sync time	RCR1.2 = 0

The user has the option to either extract the SLC-96 message fields from the onboard RFDL register or via the external RLINK pin. The information is always available at both locations. If the user wishes to extract the message bits via the RLINK pin, then some hardware must be added to decode the bits. The SLC-96 message bits can be extracted via the RFDL register without any additional hardware and it is this method that this Application Note addresses.

Figure 1 describes the method used to extract the SLC-96 message bits. The DS2141A, DS2151, and DS2152 contain an onboard SLC-96 synchronizer that is enabled when the CCR2.1 bit is set to one. In this mode, the Match flag (SR2.2) takes on a new meaning; it will indicate when the framer has received the 12-bit Fs pattern that exists in SLC-96 multiframe. In each SLC-96 multiframe, the user will read the RFDL register three times. The external controller will wait for the Match flag to be set. Once set, the controller will then wait for the RFDL to fill. Figure 2 details how the SLC-96 fields will be represented in the RFDL register on each read. Since the RFDL is also used in the ESF framing mode, the zero destuffer should be disabled (CCR2.0 = 0). (note: the Match registers (RFDLM1 & RFDLM2) are not used in SLC-96 mode and can be programmed with any value).

SLC-96 MESSAGE FIELD EXTRACTION VIA RFDL Figure 1



RFDL REGISTER BYTE SEQUENCE Figure 2

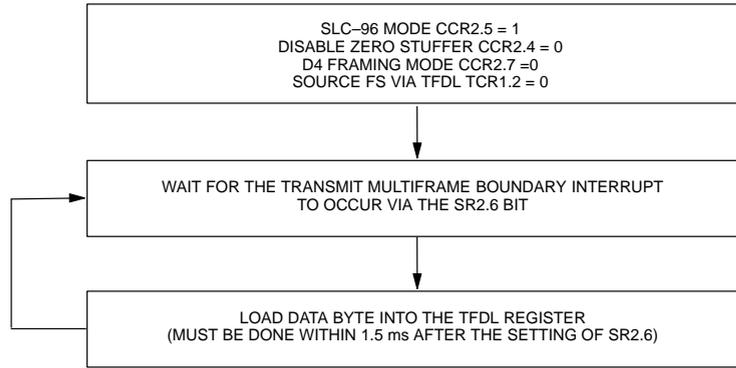
	(MSB)							(LSB)
READ #1	C8	C7	C6	C5	C4	C3	C2	C1
READ #2	M2	M1	S=0	S=1	S=0	C11	C10	C9
READ #3	S=1	S4	S3	S2	S1	A2	A1	M3

Transmit Side SLC-96 Applications

To insert the SLC-96 message fields, the user has the option to either use the external TLINK pin or to use the onboard TFDL register. Usage of the TLINK pin will require some external hardware and to enable this option, the TCR1.2 bit should be set to one. This Application Note concerns itself solely to the use of the TFDL register to insert the SLC-96 message fields.

Figure 3 displays the method to enable the DS2141A, DS2151 or DS2152 to insert the SLC-96 message fields via the TFDL register. On each normal D4 multi-frame boundary, the framer will signal to the user via the SR2.6 bit to write to the TFDL the sequence of bytes shown in Figure 4. The user will write to the TFDL six times in each SLC-96 multiframe.

SLC-96 MESSAGE FIELD INSERTION VIA TFDL Figure 3



STATUS BIT(S) USED:
SR2.6 – TRANSMIT MULTIFRAME BOUNDARY
REGISTER(S) USED:
TFDL – TRANSMIT FDL REGISTER

TFDL REGISTER BYTE SEQUENCE Figure 4

	(MSB)							(LSB)
Write #1	X	X	C1	1	1	1	0	0
Write #2	X	X	C7	C6	C5	C4	C3	C2
Write #3	X	X	S=1	S=0	C11	C10	C9	C8
Write #4	X	X	A2	A1	M3	M2	M1	S=0
Write #5	X	X	0	S=1	S4	S3	S2	S1
Write #6	X	X	0	1	1	1	0	0