DESCRIPTION OF CIRCUITRY AND BLOCK DIAGRAMS

RULE PART NUMBER: 2.1033 (c)(10)

MOBILE DATA PRODUCT

POWER AMPLIFIER (PA) CIRCUIT BOARD

CONNECTIONS

Power and ignition sense are supplied to the radio through J650. Since the power is connected directly to the vehicle battery, the ignition sense line tells the radio when the vehicle ignition is on. The PA board connects to the RF board via J600, a 10-pin socket. This connector supplies power to the RF board through F600 and provides control over the PA board. CR600, a transorb prevents negative voltages and extremely high positive voltages from damaging the radio by conducting and blowing the 12A in-line fuse.

The main antenna is connected to the PA board through J630, a mini-UHF connector. The transmitter output and main receiver input are provided through this 50 Ω connector. The main receiver signal is passed to the RF board through P200, a 50 Ω through-chassis connector. The transmit drive input comes from the RF board through P500, another 50 Ω through-chassis connector.

PA TEMPERATURE SENSE

One control signal provided to the RF board microprocessor is temperature sense. A thermistor (RT680 for 10W models, or RT690 for 40W models) is placed next to the final amplifier on the PA board and its resistance changes with the final amplifier temperature. The thermistor is biased by R405 on the RF board providing a voltage that varies linearly with temperature from 15°C to 125°C, the normal temperature range of the PA during use. If the final amplifier temperature exceeds a preset threshold, the microprocessor will fold back the power to prevent thermal destruction of the final.

PA CURRENT SENSE

Current to the final amplifier passes through R618 creating a proportional voltage across the resistor. U600B, CR614, CR616, R614, R615, R616, and R617 form a differential amplifier that amplifies the voltage across R618 and provide this voltage to the RF board microprocessor. When the final amplifier current exceeds a preset threshold due to high VSWR, the microprocessor will fold back the power to prevent thermal destruction of the final.

PA FORWARD POWER SENSE

The final amplifier output passes through a directional coupler that samples some of the transmit power and rectifies it through CR620 with C674 providing filtering of the RF content. Resistors R636 and R637 drop the voltage down to a suitable level for the microprocessor. The power sense voltage is proportional to the square root of the output power.

PRE-TRANSMIT ENABLE

The pre-transmit enable signal from the RF board prepares the PA board for transmit. The pre-driver, Q670, and driver, Q680, are biased on, and the antenna switch is configured for transmit by turning on CR640 and CR650.

TRANSMIT ENABLE

The transmit enable signal pulls the power control amplifier U600A out of saturation and allows the PA power to reach the programmed output level. When transmit enable is removed, U600A goes into saturation again causing the output power to drop to zero.

POWER CONTROL AND DRIVE BUFFER

The power set voltage from the RF board is applied to the non-inverting input of U600A. The PA forward power sense voltage is fed into the inverting input of U600A through CR605, R601 and R603. The output of U600A is fed into a high current amplifier consisting of Q640, Q650, R606, R607, and R608. This amplifier has a voltage gain of approximately two. The output of the high current amplifier provides bias and collector current for Q665, the drive buffer. When the power set voltage is greater than the forward power voltage, U660A turns the high current amplifier on harder increasing the bias to Q665, and providing more drive level. When the forward power voltage is greater than the power set voltage, U660A cuts the high current amplifier level down decreasing the bias to Q665, and reducing drive level.

The input to Q665 is from the PA buffer on the RF board through an attenuator formed by R619, R620, and R621. C623 and C624 provide the input match, with feedback from C625 and R624 for stability. The output of Q665 goes to the pre-driver Q670 with C626, C629, and C630 providing the interstage match.

3-WATT PRE-DRIVER

Transistor Q670 is a 3-Watt vertical MOSFET that provides pre-drive level for the 40W model and drive level for the 10W model. The output of this stage goes to Q680 with C639, C640, C641, C642, L602, and C643 providing the interstage match.

15-WATT DRIVER / FINAL (10W Model)

Transistor Q680 is a 15-Watt vertical MOSFET that provides drive level for the 40W model and is the final amplifier for the 10W model. The output of this stage goes to Q680 in the 40W model or is matched to 50 Ω in the 10W model. The interstage match consists of C651, C652, C653, L604, C656, C657, and C658. The 10W final match consists of C651, C652, C653, L604, C656, MP690, L608, C666, and C667.

50-WATT FINAL (40W Model Only)

Transistor Q690 is a 50-Watt bipolar transistor that is the final amplifier for the 40W model. The output of this stage is matched to 50 Ω using C664, C665, C666, L608, C667, and C668.

ANTENNA SWITCH

In receive, CR640 and CR650 are biased off and the main receive signal passes from J630, through the low pass filter, forward power detector, L610, C672, and C671 to P200, the RF board main receive input. In transmit, CR640 and CR650 are biased on, shorting the transmit path to the forward power detector and the receive path to ground. When the receive path is grounded, a high impedance is provided from a discrete quarter-wave section formed by C669, L610, and C670 to the transmit path providing rejection between the transmitter and the receiver.

LOW PASS FILTER

To reduce the harmonic content of the final amplifier, the transmit signal passes through a 7-pole low pass filter to the antenna. The low pass filter consists of C678, L612, C679, L614, C680, L616, and C681. R640 bleeds static charge from the antenna to protect the active devices in the power amplifier.

RADIO FREQUENCY (RF) CIRCUIT BOARD

CONNECTIONS

The RF board connects to the PA board via P600, a 10-pin header. This connector supplies power to the RF board and provides control over the PA board. The user or modem interface is provided by J400, a 2x12-pin socket. This connector supplies power to the modem or user interface through F401 and provides control over the RF deck. A secondary interface is provided by J450, a 12-pin male socket, for programming the internal flash or servicing the RF deck while the modem is connected.

The main receiver input comes from the PA board through J200, a 50 Ω through-chassis connector. The transmitter driver output goes to the PA board through J500, another 50 Ω through-chassis connector. The diversity receiver input comes from J300, a panel mount mini-UHF connector that is connected through a length of coax to the RF board.

MICROCONTROLLER

The microcontroller is comprised of microprocessor U420, SCI (Serial Communications Interface) switch Q410 and U410, SPI (Serial Peripheral Interface) switch U430, and PWM (Pulse Width Modulation) filters U450 and U460. Y420 sets the microprocessor reference clock to 4.9152 MHz; the internal bus clock is phase-locked to 7.3728 MHz. The microcontroller has eight 8-bit ADC (Analog to Digital Converter) channels for sensing radio conditions, and five 8-bit PWM outputs with a period of 27.13 µs. One PWM output is used to generate and adjust the internal negative supply for the VCO (Voltage Controlled Oscillator). The other four outputs are amplified and filtered to remove the PWM harmonics. These outputs are then used as 8-bit DACs (Digital to Analog Converters) with an output filter delay of 1ms.

The microcontroller loads the synthesizer, adjusts the Front-end receive filters to track across the RF band according to frequency and also controls the transmitter. The transmitter is calibrated at 4 points for RF output power, deviation and modulation flatness. The microcontroller interpolates for frequencies between the calibrated points to maintain equal power, deviation and modulation flatness across the entire RF band.

The SPI switch is used to change between internal onboard SPI operation and external off-board SPI operation. During internal operation the SPI_BUSY line is low, the BUSY_OUT line is high (if SPI protocol is enabled), and U430 connects the SPI lines to the internal serial devices, synthesizer U850, and digital pot U890. When the internal communications conclude, the SPI_BUSY line is brought high, and the BUSY_OUT line is brought low (if SPI protocol is enabled), and U430 connects the SPI lines to an external device (modem) through J400.

The microprocessor's internal Flash memory is programmed by applying a positive voltage to the AUX FLASH ENABLE (J450 pin3) or XCVR FLASH ENABLE (J400 pin4) and resetting the processor by either cycling power or sending a software reset command serially. The positive voltage turns on Q31 and Q30 applying approximately 10.1V to the microprocessor IRQ (Interrupt ReQuest) pin. Upon reset, all microprocessor ports are configured as inputs and the microprocessor enters Background Debug Mode (BDM). Transistor Q410 is turned off and U410 connects the 5V RS-232 lines to Port A, Pin 0, the BDM Port. Pre-Boot code is sent via the 5V RS-232 lines into RAM through the BDM Port. The Pre-Boot code configures the SCI port for 9600 baud), Port C Pin 5 is brought high turning on Q410 which switches U410 and connects the 5V RS-232 lines to the SCI port to accept the Boot Code. Flash programming resumes through the SCI port at 9600 baud. When programming is finished, the programming voltage must be removed from the AUX FLASH ENABLE (J450 pin3) and XCVR FLASH ENABLE (J400 pin4), and the microprocessor reset for normal operation to continue.

TEMPERATURE SENSE

Integrated circuit U440 provides a voltage to Port B Pin 0 that is proportional to the temperature in the RF cavity. By monitoring the temperature, the microprocessor can compensate for temperature variations in the radio.

+5V LOGIC REGULATOR AND RESET GENERATOR

The input voltage on pin 1 of P600 is regulated by U10 to provide +5V for the logic section. The reset for the microprocessor is provided by U20 on power-up. The shutdown (SD) pin is pulled low when RF_ENABLE is asserted from either the modem or AUX connectors. When the processor powers up, it pulls the SD pin low by asserting the RF_ENABLE_OVERRIDE on Port A Pin 2. When the RF_ENABLE lines are both brought low, the processor removes the RF_ENABLE_OVERRIDE signal and U10 removes power to the logic section. In case of a higher than normal current situation, U10 will go into thermal foldback which will decrease the output voltage to stabilize the internal die temperature preventing destruction of the regulator.

+5.5V AND +9.6V REGULATORS AND +2.5V REFERENCE

When the microprocessor asserts the TRANSCEIVER_ENABLE line, Q20 and Q21 turn on providing power to the +5.5V and +9.6V regulators as well as generating a precision +2.5V reference. C20 and C21 serve two purposes: first, they filter the +2.5V reference, second, they form a capacitive voltage divider that allows the reference to reach +2.5V almost instantly. The +5.5V and +9.6V regulators are regulated off of the +2.5V reference; when U10 goes into thermal shutdown, both supplies as well as the reference voltage follow. Since the microprocessor is unable to control the radio under this condition, this mechanism provides a path to shutdown the RF section.

The +9.6V linear regulator consists of U40B, Q40, Q41 and associated components. This regulator powers the PWM filters, negative voltage generator, VCOs, transmit drivers, LNAs, LO amps, and IF amps. The microprocessor controls the voltage to the transmit drivers through Q94 and Q95. Voltages to the receiver LNAs, LO amps, and IF amps are controlled by Q90 and Q91 for the main receiver and Q92 and Q93 for the diversity receiver. The +5.5V linear regulator consists of U40A, Q50, Q51, Q52 and associated components. This regulator powers the TCXO, synthesizer IC, digital pot, IF ICs, bandwidth switch and data amplifiers.

NEGATIVE VOLTAGE GENERATOR

To minimize switching transients on the supply line, the negative voltage generator uses a constant current source consisting of Q70, Q71, Q72 and R74 in a current mirror configuration. The microprocessor generates the NEG_SWITCH signal as a PWM output that turns Q74 and Q73 off and on. When the Q74 is off, Q71 charges C73 through the lower half of CR70. At the same time, Q73 is off and Q72 charges C70 through both halves of CR70. When Q74 is on, the positive side of C73 is shorted to ground, Q73 is on which shorts the positive side of C70 to the negative side of C73. The negative side of C70 has voltage amplitude that is approximately double the charge voltage of a single capacitor. This voltage is then used to charge C71 and C72 through CR72. By varying the PWM duty cycle, the negative supply voltage can be adjusted.

The output of the negative supply is fed back to the microprocessor through CR78, R78, and R79 to Port B Pin 7. Zener diode CR78 protects the microprocessor from the negative voltage if R79 failed, and protects C72 from reverse voltage when power is removed from the negative supply. The feedback to microprocessor allows it to regulate the negative supply over voltage and temperature variations.

NEGATIVE VOLTAGE SWITCH

The negative voltage switch consists of R81 – R89, C81 – C88, and one-of-eight analog switch, U80. Switch U80 selects one of the taps from the resistive divider formed by R81 through R89. Capacitors C81 through C88 are used to filter each tap point. The purpose of the negative voltage switch is to permit fast switching of the negative voltage to the VCO for large frequency variations.

CAPACITOR MULTIPLIERS

The capacitor multiplier consists of CR805, R805, C805, and Q805 for the Main VCO, and CR139, R139, C139, and Q139 for the 2nd LO VCO. The transistor is configured as an emitter follower with the base voltage being provided by the RC filter. The diode is used to bridge the large resistor voltage on power-up to allow the circuit to turn on quickly.

MAIN VCO (A900)

The main VCO assembly is constructed on a separate PC board that is then placed on the RF Board. Transistor Q900 is the heart of the modified Colpitts oscillator. Capacitors C928 and C930 provide the feedback for oscillation. The tank is coupled to the base of Q900 through C924. The oscillator tank inductance is provided by Z900, a dielectric resonator. CR904, CR906, CR908, and CR910 are varactor diodes that provide capacitive adjustment of the frequency over varying control voltages. The synthesizer control voltage is provided to the cathode of the diodes, and the negative voltage switch output is provided to the anodes. C918 and C908 couple the varactors to the tank. In transmit, CR912 switches in C910, C912, and C914 to move the VCO frequency down and restore VCO gain back to the same level as in receive. When a modulated signal is provided to CR900, the diode's

capacitance varies inversely with the amplitude of the signal. This diode is coupled to the tank by C904 and C906 so that the tank frequency varies proportionally with the signal amplitude.

CASCADE AMPLIFIER (A900)

Transistors Q902 and Q904 form a common emitter cascade amplifier with shared bias to increase signal level and buffer the oscillator. This output is then used for prescaler feedback for the synthesizer. In addition, the output level is then increased by common emitter amplifier Q906 and provided as the main RF output.

VCO RX / TX Splitter

The output of the VCO passes through a two-way resistive splitter formed by R810, R811, R812, and R813 to the Receive LO Buffer Amp and the Transmit Driver.

MAIN VCO PIN SHIFT CIRCUITRY

Transistors Q821 and Q820 provide the voltage for the main VCO pin shift. The outputs of these transistors are inverted from each other so that the pin diodes on A900 are either forward biased when the 9.6 pre-transmit voltage is applied or reverse biased when it is removed.

2^{nd} LO VCO

The second LO VCO is a modified Colpitts oscillator with Q140 as the oscillator transistor. Capacitors C143 and C147 provide the necessary feedback. Capacitor C141 couples the tank to the base of Q140. Inductor L140 provides the oscillator tank inductance. Varactor diode CR140 allows the oscillator frequency to vary proportionally with the control line voltage. Capacitor C146 couples the CR140 into the tank. Transistor Q141 buffers the oscillator output back to the synthesizer prescaler. Transistors Q270 and Q370 buffer the oscillator to the main and diversity receivers respectively.

TCXO

The reference for the synthesizer is provided by TCXO (Temperature Compensated Crystal Oscillator) Y890. This oscillator provides a stable 17.5 MHz output that is compensated to within ± 1.5 PPM over temperature.

FRACTIONAL-N SYNTHESIZER

To maintain stable VCO frequencies, the main and 2^{nd} LO VCOs are phase locked to the standard provided by the TCXO. The TCXO signal enters the reference pin of synthesizer IC U850 where the frequency is divided down to 50 kHz through a programmable R divider. This signal is then provided to one input of both internal phase detectors. The other phase detector input comes from programmable N counters which use the main and 2^{nd} LO VCOs as input. The phase detector generates a current that corresponds to the difference in frequency between the VCO reference and the TCXO reference. The output of the phase detectors pass through loop filters consisting of R840 – R842, and C840 – C843 for the main loop and R141, R143, C145, C146, C148, and C149 for the 2^{nd} LO loop. The loop filters strip off the reference frequency and convert the input current to an output voltage to steer the VCOs on frequency.

The N dividers for the main loop are fractional so channel steps can be made at a fraction (1/8) of the 50kHz reference. This capability allows for narrow 6.25kHz channel steps while maintaining a faster lock time due to the 50kHz reference. Digital Potentiometer U890D adjusts the compensation current to minimize fractional spurious frequencies across the band.

LOCK DETECT

When the phase difference between the two inputs to the phase detector is less than one cycle, the lock detect output goes high to tell the microcontroller that the synthesizer is locked. The lock detect output only goes high when both the main and 2^{nd} LO synthesizer loops are locked.

MODULATION BALANCE AND TX DATA GAIN

The TX data input is switched by U110B, an analog switch, to provide the necessary gain difference between the 12.5kHz and 25kHz versions of the radio. The data is amplified by U880A and the deviation is set by U890A. The signal is amplified further by U880B where the output is coupled to the TCXO modulation pin by R895. The TCXO modulation passes frequencies below the loop frequency of the main synthesizer. The output is also coupled through U890B to the VCO modulation input. The VCO modulation passes frequencies above the loop frequency. The VCO and TCXO inputs are balanced by U890B to provide a flat frequency response.

TRANSMIT DRIVER

The VCO output from R811 of the splitter passes through an attenuator formed by R560, R561, and R562 to Q550, a MMIC (Monolithic Microwave Integrated Circuit) amplifier. Q550 receives bias from R550, R551, and L550 when the 9.6V Pre-transmit voltage is applied. The output from Q550 is coupled through an attenuator formed by R528, R529, and R530 to transmit driver Q520. Q510, R517, R518, R525, and R526 provide bias to Q520. C520, L520, and C523 provide input matching to Q520, with output matching provided by L515, C515, and C516. The transmit driver 50 mW output then passes through to the PA board through J500.

RECEIVE 1st LO BUFFER AMP

The VCO output from R810 of the splitter passes through an attenuator formed by R117 (or C119), R118, and R119 and is coupled through C116 to the receive 1st LO buffer amplifier. The buffer amplifier consists of Q111 in a common emitter configuration with C114 and R115 providing feedback for stability. Q110, R110, R111, R112, R114, and R116 provide active bias for Q111. The input is matched by L111, C117 and C118, and the output is matched by L110, R113, and C115. The output of the 1st LO buffer passes through a resistive splitter formed by R180, R182, R184, and R186 to the 1st LO amplifiers for the main and diversity receivers.

QUARTER-WAVE TRANSMIT/RECEIVE SWITCH

The main receiver input passes through J100 from the PA board. Capacitor C201 provides input matching is needed. The receive signal passes through a quarter-wave microstrip line and is coupled through C204 to the main receiver preselector filter. In transmit, the 9.6PTX voltage biases pin diode CR202 into conduction shorting the end of the quarter-wave microstrip line through C202. The shorted line provides a high impedance to the PA board preventing the transmitter output from passing into the receiver.

MAIN RX 2-POLE AND 3-POLE PRESELECTORS

Receive input spurious rejection is provided by the 2 pole and 3 pole preselector filters. Both filters are varactor tuned to provide optimum spurious rejection and minimum loss across the band. A single tuning voltage is provided by U450A. Capacitors C216, C217, C238, C239, and C240 decouple the RF from the tuning voltage. Resistors R210, R212, R238, R239, and R240 couple the bias voltage to the varactors. Varactors CR211, CR210, CR232, and CR233 are grounded through the tank inductors and are coupled to their individual tanks by C218, C219, C241, and C242 respectively. To improve intermodulation performance, the first tank of the 3-pole filter has four varactors CR230, CR231, CR236, and CR237 in a parallel – series combination that nearly equals the capacitance of a single varactor. The combination reduces the current and voltage across each individual varactor.

Capacitors C214, C215, C235, C236, and C237 provide supplemental tank capacitance. Tank inductance is provided by L216, L218, L240, L242, and L244. Series inductors L212, L214, L234, L236, and L238 add a notch at the image frequency that tracks as the varactor bias is changed. The tanks are coupled by L210, L230, and L232.

Input matching is done through C210 and C211 on the 2 pole and C230 and C233 on the 3-pole filter. Output matching is likewise accomplished with C212 and C213 on the 2 pole and C232 and C234 on the 3-pole filter.

MAIN RX LOW NOISE AMPLIFIER

The low noise amplifier (LNA) consists of Q221 in a common emitter configuration with C225 and R225 providing feedback for stability and R230 and R231 providing emitter degeneration. Q220, R220, R221, R222, R224, and R226 provide active bias for Q221. Switching diode CR220 prevents large signals from damaging the LNA. The input is matched by L222, C228 and C229, and the output is matched by L220, R223, and C227. The output of the LNA passes through an attenuator formed by R233, R234 (or C226), and R235.

MAIN RX 1st LO AMPLIFIER

The VCO output from R180 of the splitter is coupled through C266 to the LO amplifier. The amplifier consists of Q261 in a common emitter configuration with C264 and R265 providing feedback for stability. Q260, R260, R261, R262, R264, and R266 provide active bias for Q261. The input is matched by L262, C267 and C268, and the output is matched by L260, R263, and C265. The output of the amplifier is 50mW.

MAIN RX 1st MIXER AND DISSIPATIVE FILTER

The first mixer is a passive double balanced device that converts the RF input to the 1st IF frequency of 55 MHz. C243 matches the LO input to the mixer. The IF output of the mixer passes through a dissipative filter that is designed to provide a 50 ohm termination to the mixer and 1st IF filter at all frequencies.

MAIN RX 1st IF FILTER

The 1st IF filter is a 55 MHz 4 pole crystal filter, Z250, that provides attenuation of the adjacent channel and close intermodulation frequencies. Capacitors C254 and C255 couple the 2-pole section together. The input is matched by C250, C253, C248, and L248. The output is matched by C249, C256, C252, and L250.

MAIN RX 1st IF AMPLIFIER

The 1st IF signal is amplified by Q250 in a common emitter configuration. Resistors R245, R248, and R249 bias the amplifier. C257 matches the input. C247 and R272 matched the output to the 2nd mixer in U260.

MAIN RX 2nd LO BUFFER

Buffer Q270 is set up in an emitter follower configuration that is biased by R275 and R140. C277 and L272 notch out any 450kHz signals from reaching the buffer. C282 couples the receive 2nd LO to the mixer in U260.

MAIN RX 2nd MIXER AND 2nd IF FILTER

The 2nd mixer is a Gilbert cell configuration located in U260. The mixer converts the 55 MHz 1st IF down to a 450 kHz 2nd IF. The 2nd IF is filtered by Z280 that is a 4-pole constant group delay ceramic filter.

MAIN RX 2nd IF AMPLIFIER AND 2nd IF FILTER

The filtered 2nd IF passes through an IF amplifier in U260. This amplifier generates part of the RSSI current internal to U260. The 2nd IF is filtered again by Z270, another 4-pole constant group delay ceramic filter.

MAIN RX LIMITER AND QUADRATURE DETECTOR

The filtered 2nd IF passes through an IF limiter in U260. The limiter removes variations in signal amplitude and generates the remaining current for RSSI output. The output of the limiter connects directly into one input of the quadrature detector. The other input of the quadrature detector comes from the limiter through C273 and L270, a 450 kHz tank. The capacitively coupled input is shifted 90° in phase from the direct input. When no modulation is present, the quadrature detector has no output. When the IF frequency changes due to modulation, the phase shift changes also causing the baseband signal to be recovered from the quadrature detector.

MAIN RX RSSI BUFFER

The 2nd IF amplifier and limiter generate a current that is proportional to input signal level. The current is passed through a temperature compensated resistor internal to U260 converting the current in to a voltage that is passed to a buffer operational amplifier in U260. Resistors R285, R286, R287, and R288 provide a gain and compensation network for the RSSI voltage. Frequency and temperature variations in RSSI voltage are compensated by the microprocessor and the resulting compensated RSSI is passed to the modem interface.

MAIN RX DATA BUFFER AND GAIN SWITCH

The recovered baseband signal from the quadrature detector is amplified by an internal operational amplifier in U260 using R289 and R290 as gain fixing resistors. The signal then passes through U110A that switches the signal either through R292 for unity gain or R293 for twice the gain depending upon the programming of the gain switch. U120A buffers or amplifies the signal stripping off the 450 kHz components. The signal is then passed to the modem interface and the auxiliary connector.

DIVERSITY RX LOW PASS FILTER

The diversity receiver input passes from J300 through a 7-pole low pass filter (LPF), to the preselector input. The LPF improves the above band rejection and makes the main and diversity receivers as similar as possible. The low pass filter consists of C303, L302, C304, L303, C305, L304, and C306. R302 bleeds static charge from the antenna to protect the active devices in the diversity receiver.

DIVERSITY RX 2-POLE AND 3-POLE PRESELECTORS

Receive input spurious rejection is provided by the 2 pole and 3 pole preselector filters. Both filters are varactor tuned to provide optimum spurious rejection and minimum loss across the band. A single tuning voltage is provided by U460A. Capacitors C316, C317, C338, C339, and C340 decouple the RF from the tuning voltage. Resistors R310, R312, R338, R339, and R340 couple the bias voltage to the varactors. Varactors CR311, CR310, CR332, and CR333 are grounded through the tank inductors and are coupled to their individual tanks by C318, C319, C341, and C342 respectively. To improve intermodulation performance, the first tank of the 3-pole filter has four varactors CR330, CR331, CR336, and CR337 in a parallel – series combination that nearly equals the capacitance of a single varactor. The combination reduces the current and voltage across each individual varactor.

Capacitors C314, C315, C335, C336, and C337 provide supplemental tank capacitance. Tank inductance is provided by L316, L318, L340, L342, and L344. Series inductors L312, L314, L334, L336, and L338 add a notch at the image frequency that tracks as the varactor bias is changed. The tanks are coupled by L310, L330, and L332.

Input matching is done through C310 and C311 on the 2 pole and C330 and C333 on the 3-pole filter. Output matching is likewise accomplished with C312 and C313 on the 2 pole and C332 and C334 on the 3-pole filter.

DIVERSITY RX LOW NOISE AMPLIFIER

The low noise amplifier (LNA) consists of Q321 in a common emitter configuration with C325 and R325 providing feedback for stability and R330 and R331 providing emitter degeneration. Q320, R320, R321, R322, R324, and R326 provide active bias for Q321. Switching diode CR320 prevents large signals from damaging the LNA. The input is matched by L322, C328 and C329, and the output is matched by L320, R323, and C327. The output of the LNA passes through an attenuator formed by R333, R334 (or C326), and R335.

DIVERSITY RX 1st LO AMPLIFIER

The VCO output from R180 of the splitter is coupled through C366 to the LO amplifier. The amplifier consists of Q361 in a common emitter configuration with C364 and R365 providing feedback for stability. Q360, R360, R361, R362, R364, and R366 provide active bias for Q361. The input is matched by L362, C367 and C368, and the output is matched by L360, R363, and C365. The output of the amplifier is 50mW.

DIVERSITY RX 1st MIXER AND DISSIPATIVE FILTER

The first mixer is a passive double balanced device that converts the RF input to the 1st IF frequency of 55 MHz. C343 matches the LO input to the mixer. The IF output of the mixer passes through a dissipative filter that is designed to provide a 50 ohm termination to the mixer and 1st IF filter at all frequencies.

DIVERSITY RX 1st IF FILTER

The 1st IF filter is a 55 MHz 4 pole crystal filter, Z350, that provides attenuation of the adjacent channel and close intermodulation frequencies. Capacitors C354 and C355 couple the 2-pole section together. The input is matched by C350, C353, C348, and L348. The output is matched by C349, C356, C352, and L350.

DIVERSITY RX 1st IF AMPLIFIER

The 1st IF signal is amplified by Q350 in a common emitter configuration. Resistors R345, R348, and R349 bias the amplifier. C357 matches the input. C347 and R372 matched the output to the 2nd mixer in U360.

DIVERSITY RX 2nd LO BUFFER

Buffer Q370 is set up in an emitter follower configuration that is biased by R375 and R140. C377 and L372 notch out any 450kHz signals from reaching the buffer. C382 couples the receive 2nd LO to the mixer in U360.

DIVERSITY RX 2nd MIXER AND 2nd IF FILTER

The 2nd mixer is a Gilbert cell configuration located in U360. The mixer converts the 55 MHz 1st IF down to a 450 kHz 2nd IF. The 2nd IF is filtered by Z380 that is a 4-pole constant group delay ceramic filter.

DIVERSITY RX 2nd IF AMPLIFIER AND 2nd IF FILTER

The filtered 2nd IF passes through an IF amplifier in U360. This amplifier generates part of the RSSI current internal to U360. The 2nd IF is filtered again by Z370, another 4-pole constant group delay ceramic filter.

DIVERSITY RX LIMITER AND QUADRATURE DETECTOR

The filtered 2nd IF passes through an IF limiter in U360. The limiter removes variations in signal amplitude and generates the remaining current for RSSI output. The output of the limiter connects directly into one input of the quadrature detector. The other input of the quadrature detector comes from the limiter through C373 and L370, a 450 kHz tank. The capacitively coupled input is shifted 90° in phase from the direct input. When no modulation is present, the quadrature detector has no output. When the IF frequency changes due to modulation, the phase shift changes also causing the baseband signal to be recovered from the quadrature detector.

DIVERSITY RX RSSI BUFFER

The 2nd IF amplifier and limiter generate a current that is proportional to input signal level. The current is passed through a temperature compensated resistor internal to U360 converting the current in to a voltage that is passed to a buffer operational amplifier in U360. Resistors R385, R386, R387, and R388 provide a gain and compensation network for the RSSI voltage. Frequency and temperature variations in RSSI voltage are compensated by the microprocessor and the resulting compensated RSSI is passed to the modem interface.

DIVERSITY RX DATA BUFFER AND GAIN SWITCH

The recovered baseband signal from the quadrature detector is amplified by an internal operational amplifier in U360 using R389 and R390 as gain fixing resistors. The signal then passes through U110C that switches the signal either through R392 for unity gain or R393 for twice the gain depending upon the programming

of the gain switch. U120B buffers or amplifies the signal stripping off the 450 kHz components. The signal is then passed to the modem interface and the auxiliary connector.

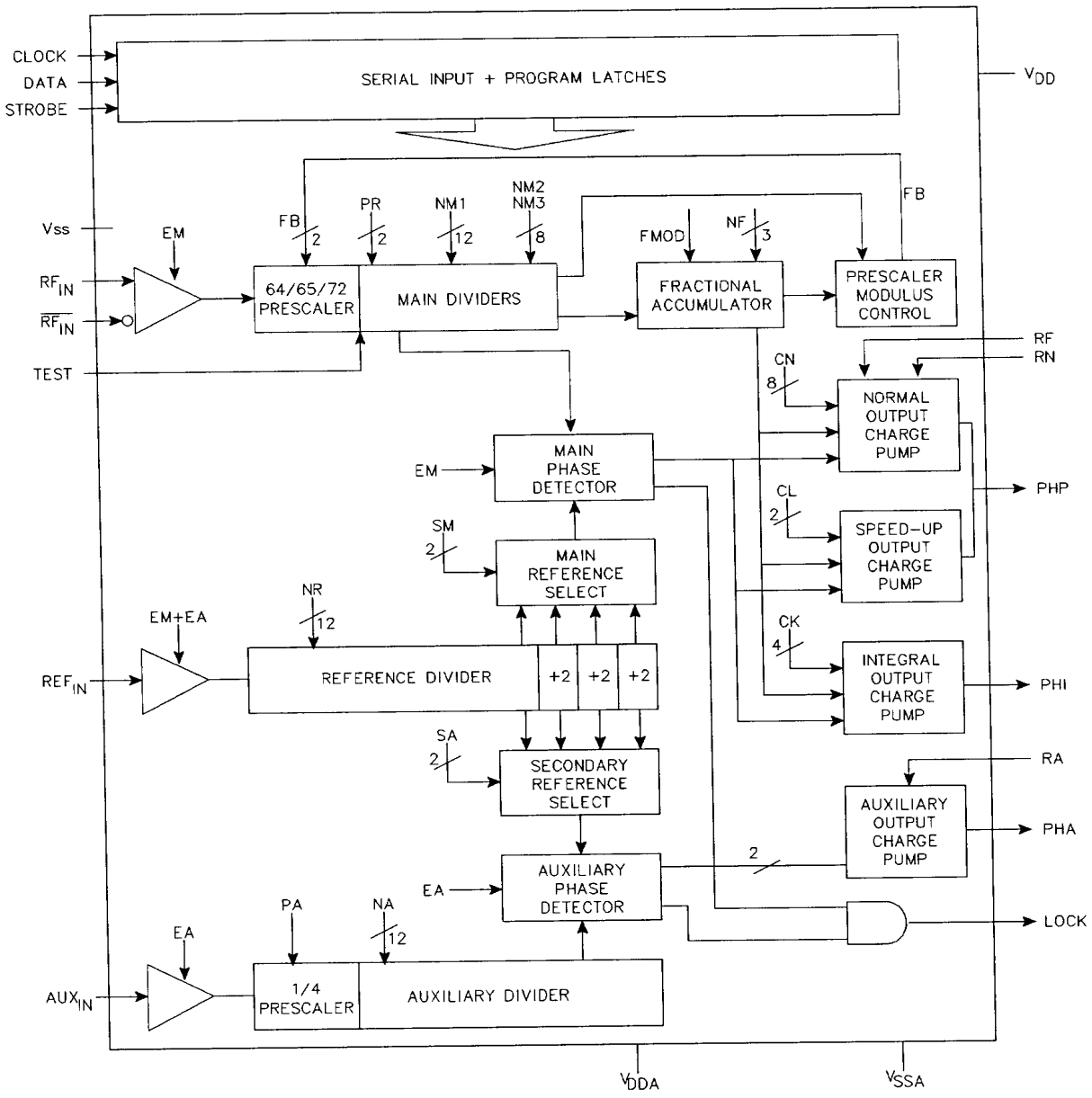

Figure 1: DL-3412 SYNTHESIZER INTEGRATED CIRCUIT (U811)

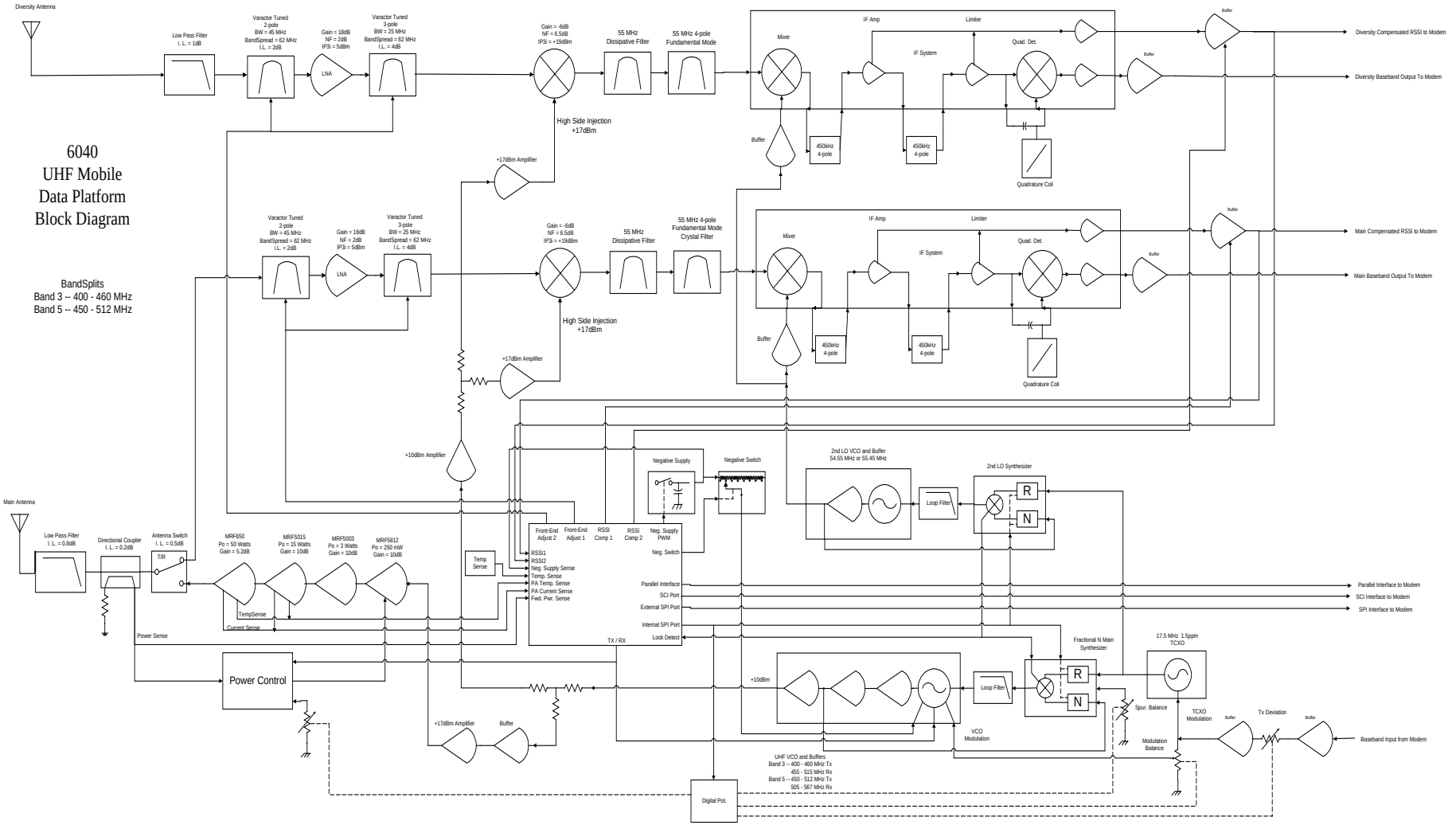

Figure 2: MDP TRANSCEIVER BLOCK DIAGRAM

DESCRIPTION OF CIRCUITRY

RULE PART NUMBER: 2.1033 (c)(10)

Introduction

The Gemini/PD is a mobile radio-modem housed in an aluminum cabinet. It comprises a transceiver with a second diversity receiver, a variable 2-50 Watt power amplifier and a Gemini Control Unit (GCU). The modem used on the GCU is Digital Signal Processor (DSP) driven data modulator and a diversity capable demodulator for operation at up to 9600 b/s in half channels and up to 19.2 Kb/s in full channel radios. Gemini/PD is equipped with an integrated OEM GPS receiver.

The GCU (p/n 050-03322-00x) is described below:

The main functions of the board includes:

- loading the radio frequencies,
- providing the baseband modulating signal for the transmitter,
- demodulating the receive audio signals,
- interfacing the OEM GPS receiver (to get mobile position)

The GCU is divided into 4 sub-sections:

a) CPU block
b) Modem block
c) Power Supply Unit (PSU)
d) OEM GPS receiver board (ASHTECH G8™)

A circuit block diagram of the GCU is located at the end of this section (see Figure 3).

CPU circuit description

a) General:

The CPU block is designed around three 84C015 Intelligent Peripheral Controller (IPCs) designated as U6, U16 and U21. This implementation provides central processing, watchdog, 128-bit CTC channels, 48-bits of I/Os, and a total of 6 serial ports with independent baud rates. These serial ports are configured as: 3 external user ports, 1 sync network port, 1 async radio port, and 1 internal async GPS receiver port.

The CPU block interfaces to:

- The DSPmodem
- RS232 ports (3)
- Transceiver
- GPS receiver port

b) Circuit functions:

The CPU block controls the operation of the whole radio-modem. It uses a “master” IPC processor (U6) and two IPC (U16 and U21) used as “slaves” for interfacing functions.

The CPU clock generator uses a 19.6608 MHz crystal oscillator that provides the master clock rate of 9.8304 MHz for all IPC processors. The timing signal provided for all CTC timer/counters is equal to half the master clock frequency.

The master IPC generates the baud rates for RS 232 ports 2 & 3 using two of its timers. The third timer provides the SYNC signal to the 5V power supply DC-DC converter (U7). Finally, its fourth timer provides the clocking for U21. The master processor also controls the SRAM (U2) and Flash memory (U1).

The second IPC (U21), interfaces to the transceiver and controls RS232 port 1 using one of its internal timers to generate baud rates. The programming and tuning operations for the 16 radio channels can be performed using this async port and only by the manufacturer's loader software.

The third IPC (U16), interfaces to the DSP modem (U13) through a serial buffer (U9) for network data and to the OEM GPS receiver. The serial interface to the DSP modem operates at the nominal network speed (up to 19200 bps). A parallel connection through a parallel buffer (U8) supports future enhancements. The IPC (U16) uses one of its timers to clock the OEM GPS interface, and its three remaining timers are cascaded to provide an internal 24-bit timer.

c) Watchdog circuit:

The watchdog circuit is based on U5 (ADM705AR). This circuit provides a 200msec reset pulse on power-on and manual reset. Its internal watchdog timer has a 1.6 second duration. In addition, it oversees two other reset sources: the master processor's watchdog timer and the DSP watchdog pulse.

DSP modem circuit description

a) General:

The DSP modem is based on a Motorola DSP56303 (U13) operating at an oscillator frequency of 12.228 MHz. The main modem function is to convert the digital data into analog filtered waveforms used to modulate the transceiver with DGFSK (Differential Gaussian Frequency Shift Keying).

The DSP modem interfaces with the master IPC using the serial ports buffered by U9.

The transceiver and the DSP modem interface uses five analog signals:

- XCVR_TXMOD (TXA, outgoing audio signal)
- XCVR_RX1 (RXA_1 incoming audio signal)
- XCVR_RX2 (RXA_2 incoming audio signal)
- CH0 (main receiver' RSSI_1)
- CH1 (diversity receiver' RSSI_2)

The transceiver and the diversity receiver audio incoming channels are processed by U11 (PCM3002 CODEC) using a sampling frequency of 48 KHz. It provides dual filtered audio bi-directional channels, with separate pairs of A/D-D/A converters

The DSP modem circuit processes both Receivers' RSSI signals from the transceiver using U12 (AD7811), a 10-bit serial A/D converter.

b) Operations:

PTT is under master IPC control. The channel selection and the synthesizer frequency are under control of IPC U21.

When transmitting, transmit data from the an RS-232 port are received by RS-232 interface circuits (U15, U17 or U22), TTL level shifted and fed to U6 or U21 to be redirected to U16. Then the digital data are clocked-in from the U16 by the U13 via the sync serial port. The DSP modem will encode the data stream and the resulting baseband DGFSK digital signal is then converted by the CODEC into an analog filtered signal suitable for the RF modulator. The DSP controls deviation level and fine frequency adjust (i.e. warp).

When receiving, both RSSI signals are sampled and A/D converted by U12, then fed to the DSP modem. Both transceiver and secondary receivers' audio signals are read from the CODEC by the DSP. This is transformed to a digital data stream clocked-out via the DSP sync serial port to U16 at the network speed. Further, the received U16 data are redirected to an output port by U6 and RS-232 level shifted by U15, U17 or U22.

Power Supply Unit

The power supply circuit uses U7 (LT1375) DC-DC switching regulator to provide the 5V to the system (including power to the GPS receiver). The linear regulator U14 (LT1129) provides the 3.3V. The GCU is fuse protected from the transceiver DC power input (raw_bat).

G8™ OEM GPS receiver board

The G8™ OEM Global Positioning System (GPS) receiver, by Ashtech, is designed specifically for use as an OEM board. The G8™ supports two TTL serial communication ports; one of which is used to interface to the GCU. The receiver outputs up to one GPS based position information per second serially at 4800 bps.

The G8™ processes signals from the GPS satellite constellation to provide real-time position, velocity, and time measurements. The G8™ receives satellite signals via an external active L-band antenna. The DGPS corrections if used, will be input into to the GPS receiver via the GCU.

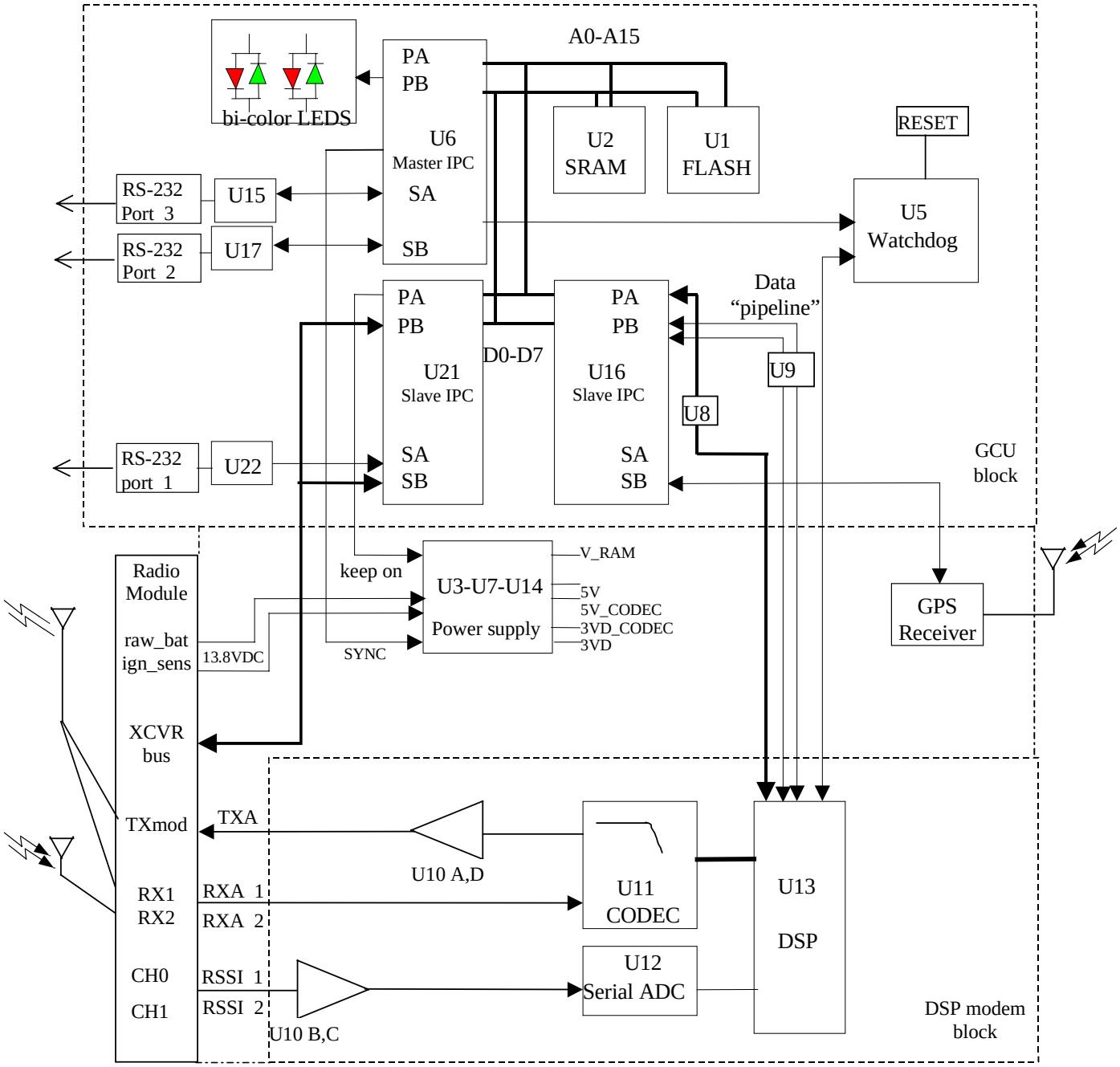

Figure 3: GEMINI(GCU) MODEM BLOCK DIAGRAM