3.5 Output Amplitude Calibration

Output Amplitude Calibration	Model	
	124XXA	125XXA/ 127XXA
3.5.1 - ALC Characterization Instructions	√	√

There are number of steps in this section. These steps provide data that the instrument ALC system needs to properly control the control output amplitude. The steps **must** be performed in the order specified. The entire process is managed by the Calibration Control Program running on the PC. Please read the section which describes the individual test for information on when re-calibration is necessary.

☛ ***NOTE:*** *Do not use Channel B on a 2 Channel Meter.*

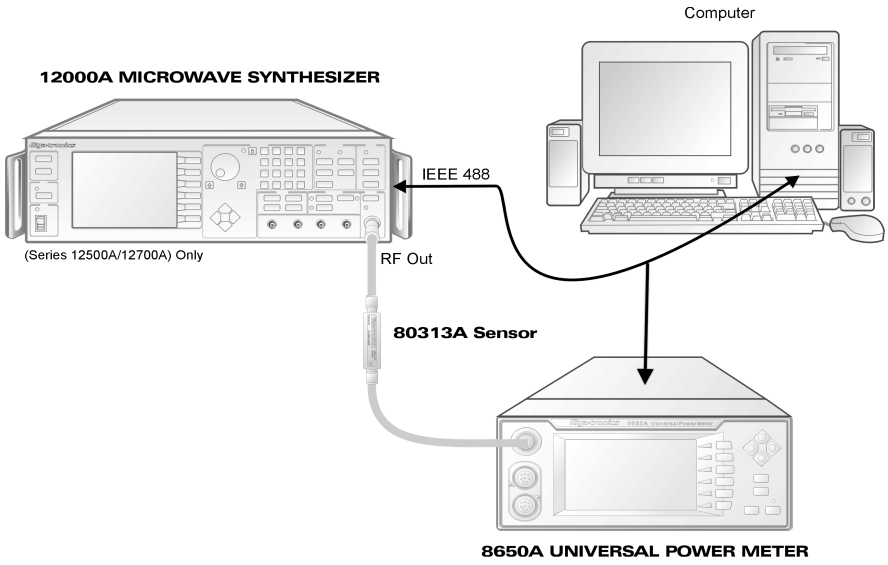


Figure 3-1: Output Amplitude Calibration Connection

1. Connect the sensor to the meter calibrator (use the 'N' to 'K' adapter) and allow at least 15 minutes for the sensor and meter to reach thermal equilibrium. Then perform a sensor calibration.

2. Now connect the equipment as shown above. The 80313A sensor connects to the 12000A RF out connector. If the 12000A has a type 'N' connector, use the 'N' to 'K' adapter. The 12000A should have its IEEE address at 6 (the default). The power meter should be at address 10.

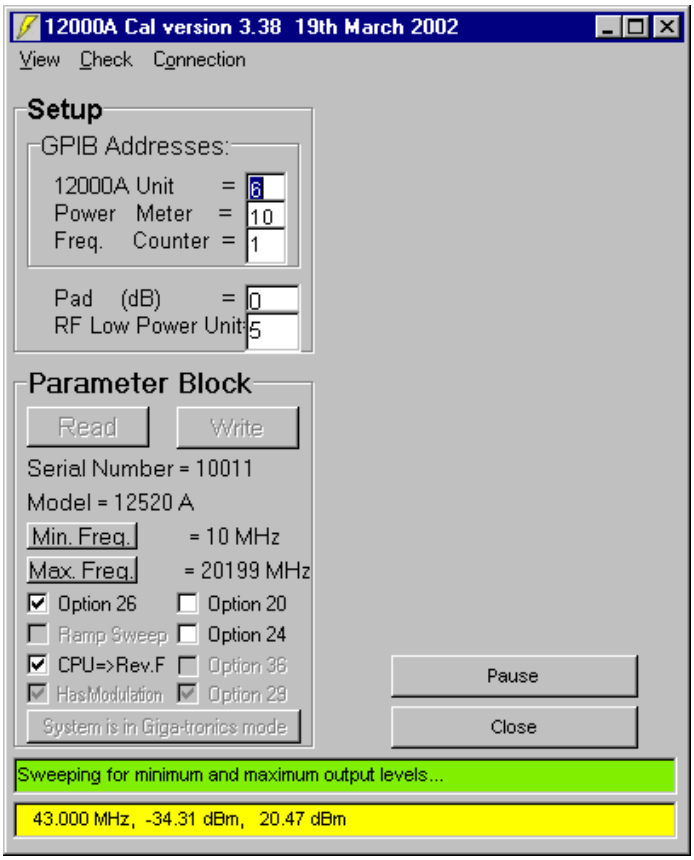
   If the 12000A has not been previously warmed up, allow 15 minutes of warm-up. When the 'Fixed Frequency' screen displays, press the **RF On** button.

3. Click on the 'Modulator (Level Test)' button to begin the process.
   - The 'Modulator' routine generates a curve of attenuation verses control voltage for the modulators at various frequencies. This section must be performed whenever the A3, A6 or A8 assemblies have been changed.

3.5.1 ALC Characterization Instructions

After clicking on the Modulator button, the main window will look like the following picture. The monitor screen will now show the power meter readings (if that mode is selected). In addition, the bottom lines of the main window will show the test being performed and the readings as they are taken. This process will take about 55 minutes for a .01 to 20 GHz instrument.

☛ ***NOTE:*** *When this process is finished, the instrument MUST be powered down to properly store the data (this occurs when it is powered back up) before any other calibrations are done or before the instrument is used.*

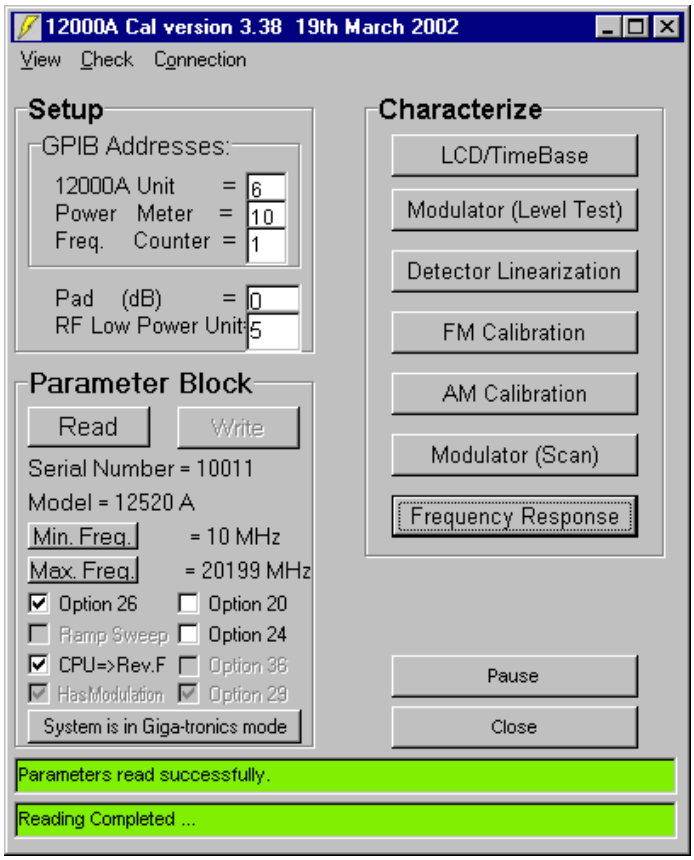


1. After the power is cycled, click the Read button under Parameter Block prior to doing the frequency response to verify the new date and time (for the Modulator) in the Characterization window.

2. Now press the Detector Linearization button. The monitor screen will now show the power meter readings (if that mode is selected). In addition, the bottom lines of the main window will show the test being performed and the readings as they are taken. This process will take about 20 minutes for a .01 to 20 GHz instrument.

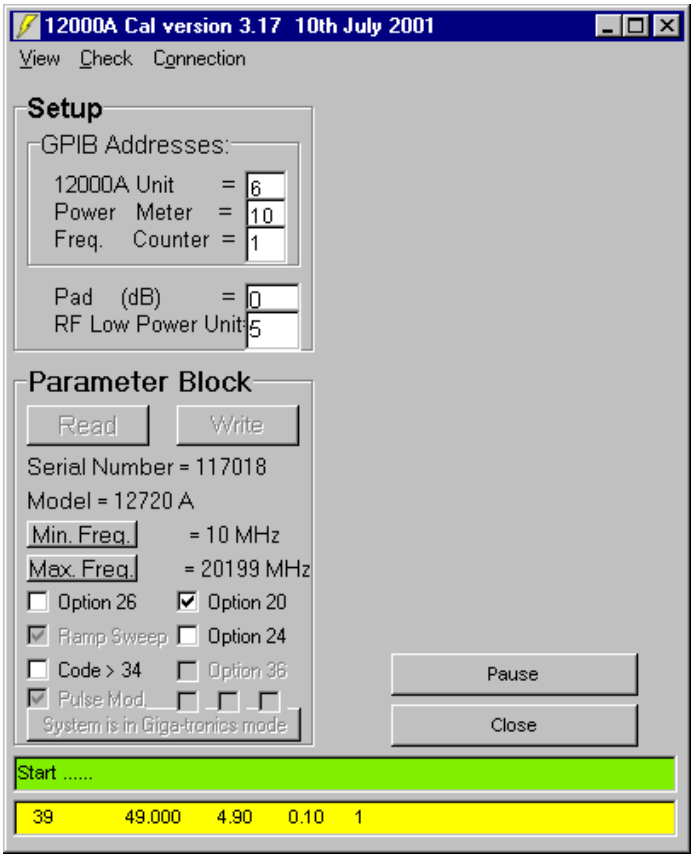
3. After the Detector Linearization is done, the frequency response calibrations may be performed. Instruments with Option 26 (Attenuator) require two calibration runs, one at +5 dBm, the other at –5 dBm. Instruments with Option 20 require an additional run at +16 dBm. The level is selected in the 'Setup' area of the main window. Measurements taken at +5 or –5 are known as "Low Power". The one at +16 is "High Power". For units without Option 26 (i.e. no Attenuator), enter '+1' in the RF Box under setup.

☛ ***NOTE:*** *You must press 'Enter' after changing the RF level parameter.*



4. Now click on 'Frequency Response' button. Frequency Response stores correction factors as a function of output frequency. This calibration will be required if A6, A8, or the optional step attenuator has been changed. It is also recommended that this routine be run if any of the RF cables between A6 and the front/rear output or the output connector itself is changed. Be sure to do the 'Modulator' characterization first, if required.

While the Frequency Response calibration is running the window will look like the following illustration below. The monitor screen will now show the power meter readings (if that mode is selected). In addition, the bottom line of the main window will show the readings as they are taken. This process will take about 25 minutes (for each level) for a .01 to 20 GHz instrument. Repeat process with RF Low Power at -5 dB for units with attenuator (Option 26).



When the process is finished, the window status lines will give a successful completion message.

☛ ***NOTE:*** *The instrument MUST be power cycled after the completion of each Frequency Response. Click the Read button after each power up and change the RF Level box prior to the next Frequency Response calibration.*

3.6 Modulation Calibration

Modulation Calibration	Model	
	124XXA	125XXA/ 127XXA
3.6.1 - Frequency Modulation Calibration	**N/A**	√
3.6.2 - Amplitude Modulation Calibration	**N/A**	√
3.6.3 - Scan Modulation Calibration	**N/A**	√

There are three separate calibration routines for the modulation functions of the 12000A. Each requires a different test setup. See the following sections for a complete description of the test system and sequence. Modulation calibrations may be done in any order. The conditions requiring re-calibration are outlined in this description of the Characterization screen of the Calibration Control Program:

- 'FM Calibration' performs the necessary steps to calibrate the frequency modulation function. Calibrating the Frequency Modulation also calibrates the Phase Modulation. FM calibration must be done if the A1 synthesizer board is replaced.
- 'AM Calibration' performs the necessary steps to calibrate the amplitude modulation function. This calibration of the Scan mode is also performed at this time. This calibration should be performed whenever the A3, A6 or A8 assemblies are replaced. Be sure to do the 'Modulator' characterizations first, if required.
- 'Modulator (Scan)' linearizes the modulators to provide accurate attenuation levels for the open looped 'deep' AM (Scan Modulation). This calibration should be performed whenever the A3, A6 or A8 assemblies are replaced.

3.6.1 Frequency Modulation Calibration

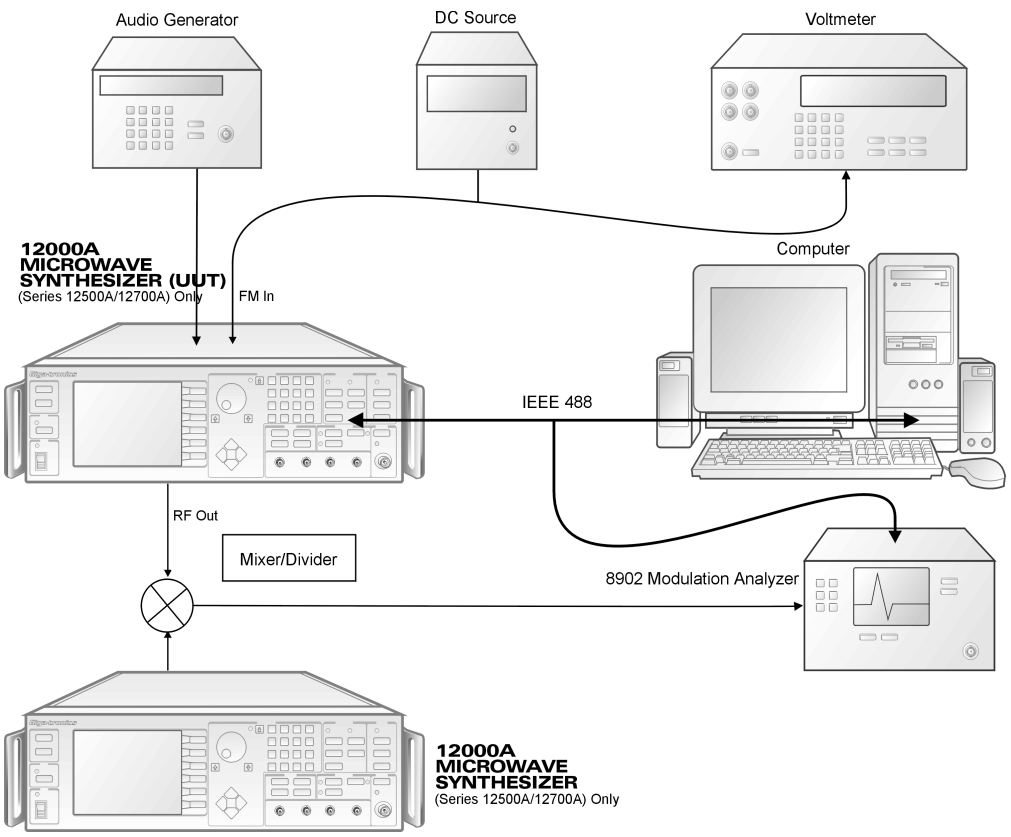


Figure 3-2: Frequency Modulation Calibration Connection

Connect the UUT, computer and Modulation Analyzer to the IEEE 488 bus. The UUT should be at address 6 (the default), the modulation analyzer at 14 and the LO source at 7. Connect the UUT RF output to the mixer RF input and the LO source (shown as a second model 12000A) to the mixer LO input. If the LO source is a Giga-tronics model 12000A or a Giga-tronics model GT9000, the program will set the frequency and power. If the source is some other model, set the LO source to 5450 MHz at +10 dBm, CW mode and press 'Cancel' in the source prompt window. Connect the Mixer/Divider IF divide-by-40 output to the Modulation analyzer input.

☛ ***NOTE:*** *The Mixer/Divider is required since the 8902 is not capable of measuring the required FM deviation. The divider reduces the deviation by a factor of 40 allowing the 8902 to make the measurement. The step-by-step procedure below explains how to use the Audio Source, DC Source and Voltmeter. Operator actions are directed by screen prompts.*

3.6.1.1 Frequency Modulation Instructions

If the 12000A has not been previously warmed up, allow 15 minutes of warm-up.

In the Characterize section, click on the 'FM Calibration' box. Follow the on-screen prompt windows for step-by-step instructions. The steps are outlined below for convenience.

1. The first step requests a zero volts input to the UUT FM connector. Simply leave the input open as there is an internal 50Ω resistor to ground. This test calibrates any zero offset errors. Since FM is DC coupled, any DC component (or zero error) will result in a frequency shift. Press 'OK' when ready.

2. When the prompt requests a 1.0 volt DC input, connect the DC source to the FM input connector and monitor the FM input connector with the voltmeter. Set the DC source to 1.00 volts ±.005 volts. It may be helpful to put a resistor of about 500 ohms in series with the source and the FM input. This will make setting the DC source less critical as it provides a 10:1 divider. Be sure to measure the voltage at the FM input connector with everything connected. This test calibrates the "inside the loop" portion of the FM (approximately DC to 15 kHz). Press 'OK' when ready.

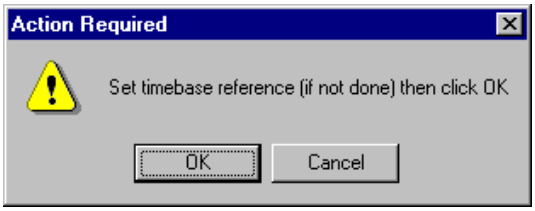
3. The next step requires that the 8902 Modulation analyzer be connected to the 12000A. Since the test is run at a frequency of 5 GHz, it is necessary to use a special downconverter (mixer) that includes a divide-by-40. The LO is set to 5450 MHz at +10 dBm and connected to the mixer LO port.

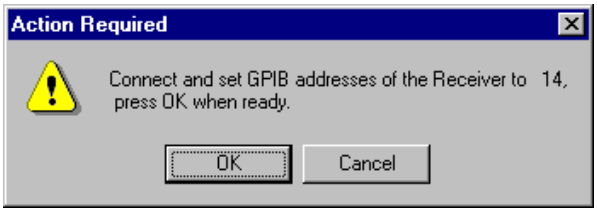
4. Connect the 12000A to the mixer RF port.

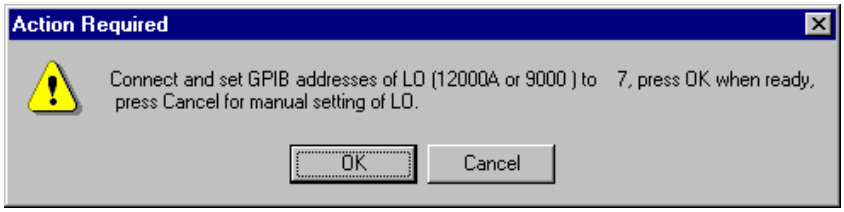
5. Connect the mixer divide-by-40 IF out to the 8902 input.

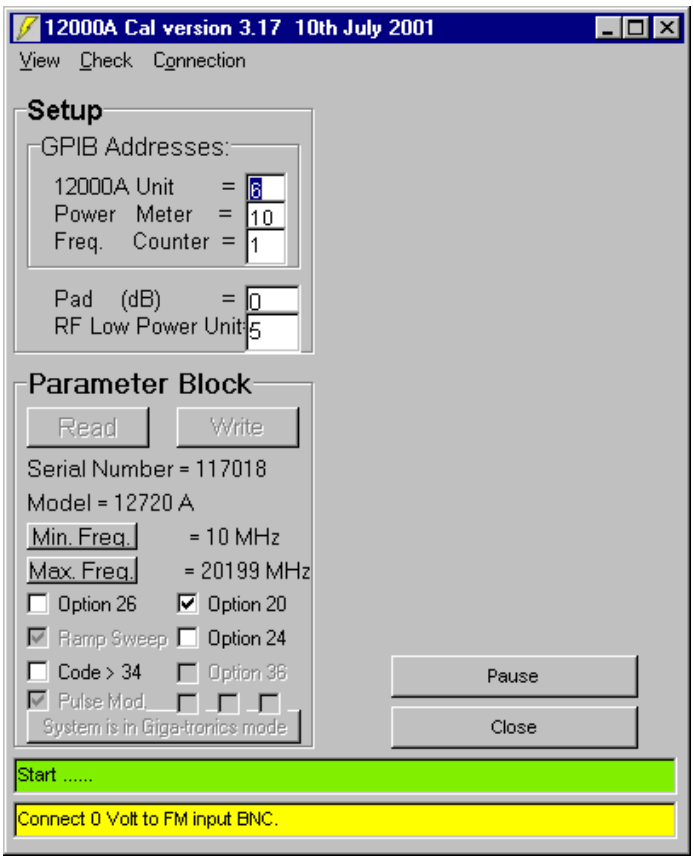
6. Connect the audio source to the 12000A FM input. Set the source to 190 kHz at 2.00 Volts peak-to-peak ± 0.01 volts. An oscilloscope is **NOT** accurate enough to set this level. Use a calibrated source or a digital voltmeter which will accurately measure 150 kHz. Be sure to measure the voltage at the FM input connector with everything connected. This test calibrates the "outside the loop" portion of the FM (approximately 15 kHz to 8 MHz) Press 'OK' when ready.

The following windows will be displayed during the FM calibration process. In addition, prompt windows will appear to provide instructions for each step of the test. The monitor window display the data that is being sent.






Action Required
Connect and set GPIB addresses of LO (12000A or 9000) to 7, press OK when ready, press Cancel for manual setting of LO.
OK
Cancel


12000A Cal version 3.17 10th July 2001
View Check Connection
Setup
GPIB Addresses:
12000A Unit = 6
Power Meter = 10
Freq. Counter = 1
Pad (dB) = 0
RF Low Power Unit 5
Parameter Block
Read
Write
Serial Number = 117018
Model = 12720 A
Min. Freq. = 10 MHz
Max. Freq. = 20199 MHz
Option 26
Option 20
Ramp Sweep
Option 24
Code > 34
Option 36
Pulse Mod
System is in Giga-tronics mode
Pause
Close
Start .....
Connect 0 Volt to FM input BNC.

3.6.2 Amplitude Modulation Calibration

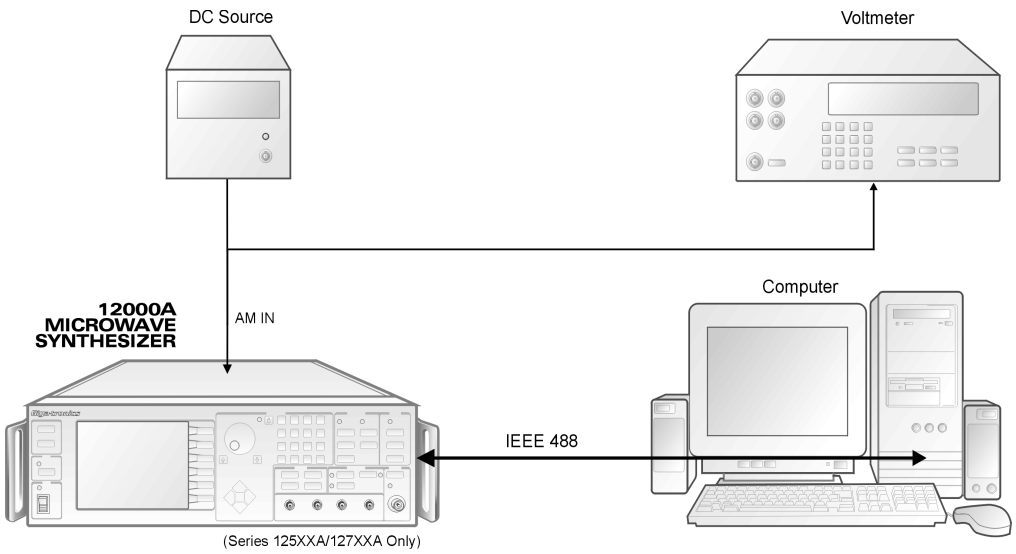


Figure 3-3: Amplitude Modulation Calibration Connection

Connect the UUT and computer to the IEEE 488 bus. If the 12000A has not been previously warmed up, allow 15 minutes of warm-up.

In the Characterize section, click on the 'AM Calibration' box. Follow the on-screen prompt window for step by step instructions. The steps are outlined below for convenience.

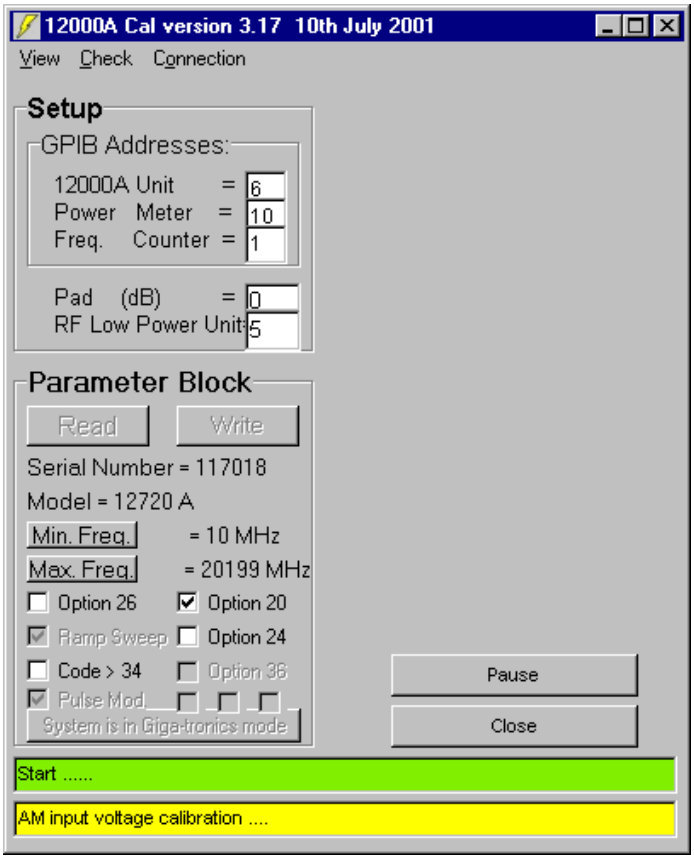
1. The first step requests a zero volts input to the UUT AM connector. Simply leave the input open as there is an internal 600Ω resistor to ground. This test calibrates any zero offset errors. Since AM is DC coupled, any DC component (or zero error) will result in a level shift. Press 'OK' when ready.

2. When the prompt requests a 1.0 volt DC input, connect the DC source to the AM input connector and monitor the AM input connector with the voltmeter. Set the DC source to 1.00 volts ±.005 volts. It may be helpful to put a resistor of about 6000 ohms in series with the source and the AM input. This will make setting the DC source less critical as it provides a 10:1 divider. Be sure to measure the voltage at the AM input connector with everything connected. This test calibrates the 'full scale' of the AM. Press 'OK' when ready.

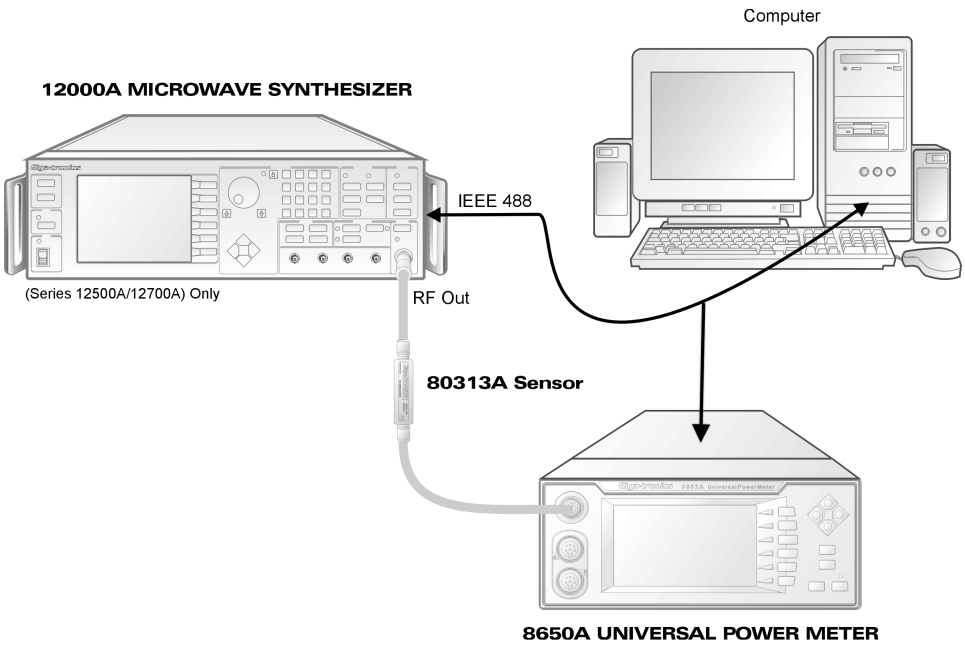
3. The next step will again request a zero volts input to the UUT AM connector. Simply leave the input open as there is an internal 600 Ω resistor to ground. This test calibrates the 'Scan' mode. Press 'OK' when ready.

4. When the prompt requests a 6.0 volt DC input, connect the DC source to the AM input connector and monitor the AM input connector with the voltmeter. Set the DC source to 6.00 volts ±.03 volts. Be sure to measure the voltage at the AM input connector with everything connected. This test calibrates the 'full scale' of the Scan Modulation. Press 'OK' when ready.

The following window will be displayed during the AM calibration process. In addition, prompt windows will appear to provide instructions for each step of the test. The monitor window displays the data that is being sent.



3.6.3 Scan Modulation Calibration



1. Connect the sensor to the meter calibrator (use the 'N' to 'K' adapter) and allow at least 15 minutes for the sensor and meter to reach thermal equilibrium. Then perform a sensor calibration.

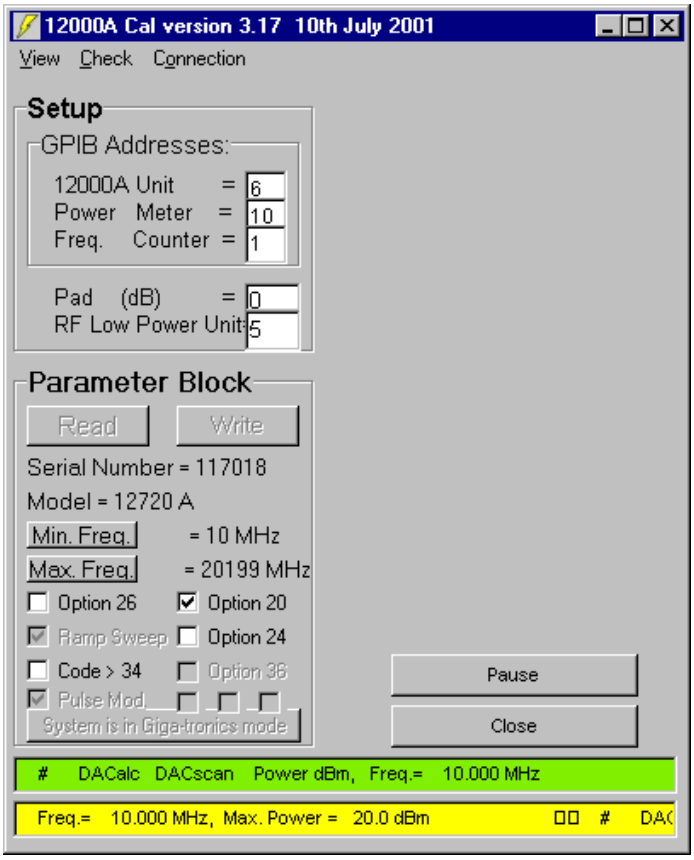
2. Now connect the equipment as shown above. The 80313A sensor connects to the 12000A RF out connector. If the 12000A has a type 'N' connector, use the 'N' to 'K' adapter. The 12000A should have its IEEE address at 6 (the default). The power meter should be at address 10.

3. If the 12000A has not been previously warmed up, allow 15 minutes of warm-up.

4. In the Characterize section, click on the 'Modulator (Scan)' box.

   The purpose of this test is to build a table of correction values. These values, when applied during Scan Modulation operation, create a linear change in the output level (in dB) as the input voltage is varied from 0 to 6 volts. Scan Modulation is run open loop once the selected CW output level has been set. The correction factors are interpolated for frequencies between the calibration points. This routine will take 85 minutes for a .01 to 20 GHz instrument.

The following window will display during the calibration process. In addition, the monitor window may be placed in the 'Power Meter' mode to view the data as it is taken.



3.7 ModGen Pulse Modulation Calibration (Option 24)

3.7.1 Description

Perform calibration of the ModGen Pulse Modulation function in the Series 12000A Microwave Synthesizers.

Due to variation in components on the ModGen board, the delays for the three counters used in pulse modulation can be inaccurate. These inaccuracies can be minimized by the software in the ModGen device driver.

Each counter must be calibrated individually. Calibration is achieved by setting the counter of interest to a known value and allowing it to count down. At the same time, the number of clock cycles from the on-board 10 MHz reference is monitored. When the counter counts down to zero, the number of 10 MHz clock cycles is compared to an expected value. The difference between the original input value and the measured value is used to derive a calibration factor used by the ModGen device driver software.

3.7.2 Equipment Required

UUT

3.7.3 Software

Any version of the Series 12000A Microwave Synthesizer firmware greater than V072-B48-18 is sufficient. Note that the menus for calibrating the ModGen option will not be visible if the board is not installed.

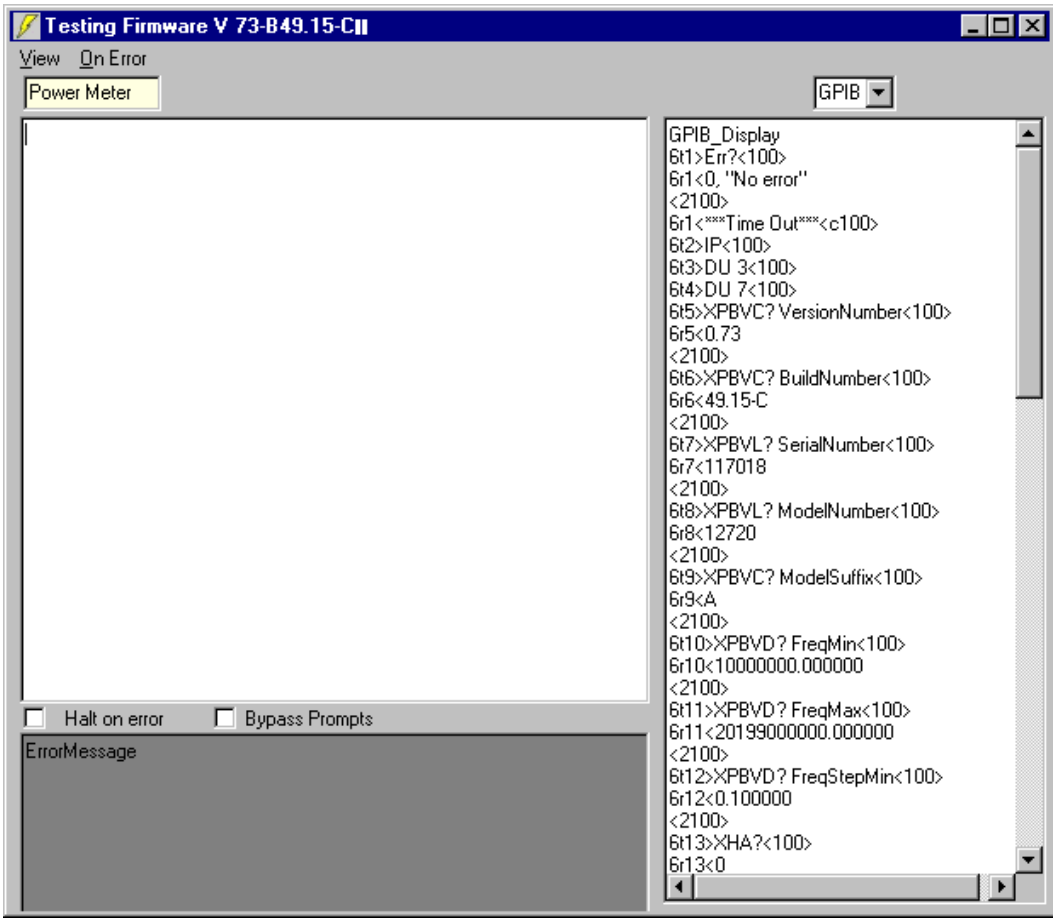
3.7.4 Procedure

1. Turn on the Model 12000A Microwave Synthesizer.
2. Allow the boot process to complete.
3. Press the **[CONFIG]** key in the System group on the front panel.
4. Press the *Service* softkey.
5. Press the *Mod Gen Testing* softkey.
6. Press the *PM* softkey.
7. Using the cursor keys, highlight the delay counter (Start, Pulse, Interval) you wish to calibrate.
8. Press the *Start Cal* softkey. This completes the cal process for the selected delay counter.
9. Repeat 7-8 for each delay counter to be calibrated.

3.8 Monitor Functions

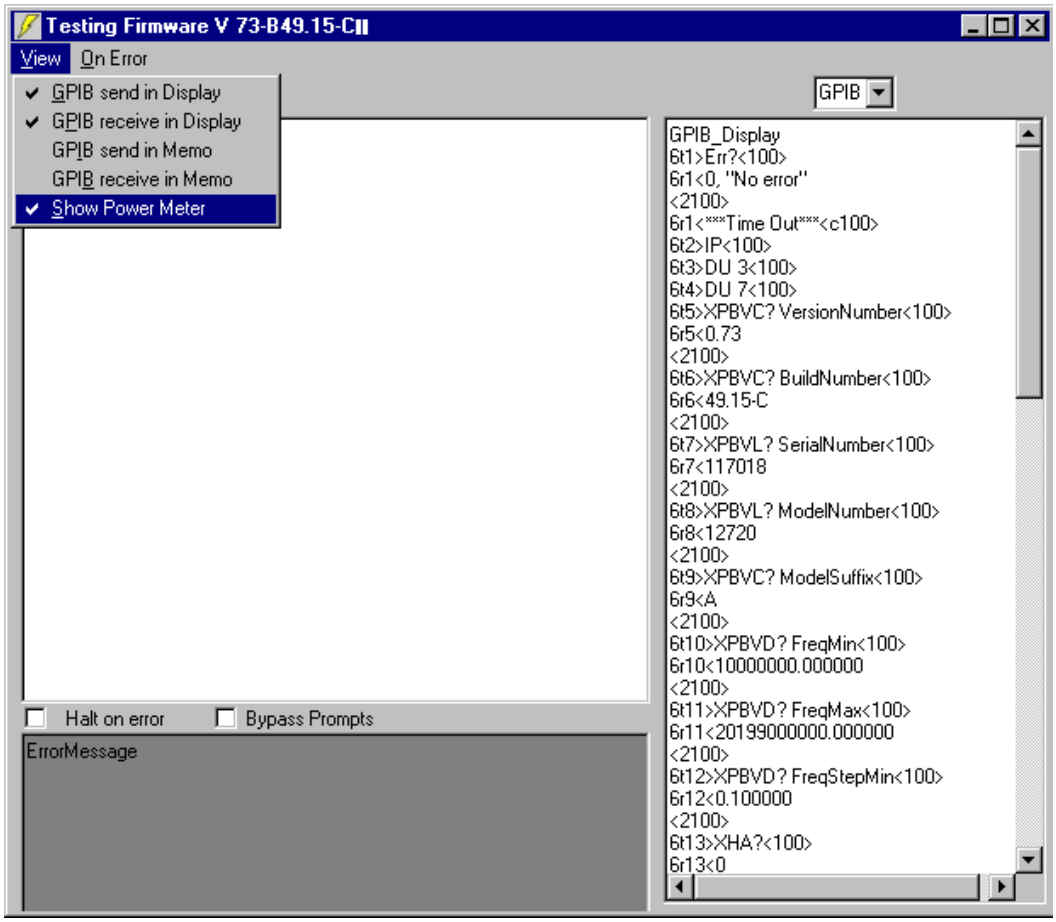
Monitor Functions	Model	
	124XXA	125XXA/ 127XXA
	√	√

The monitor window is provided to allow viewing data or IEEE 488 bus traffic. Since the calibration processes involve significant amounts of data, both the 8650A power meter and the unit under test are operated in modes that do not involve displaying any information on the instruments' displays. The monitor screen allows the user to see the data. The view below is a typical display with the bus traffic monitor turned on (See the following pages for more details).

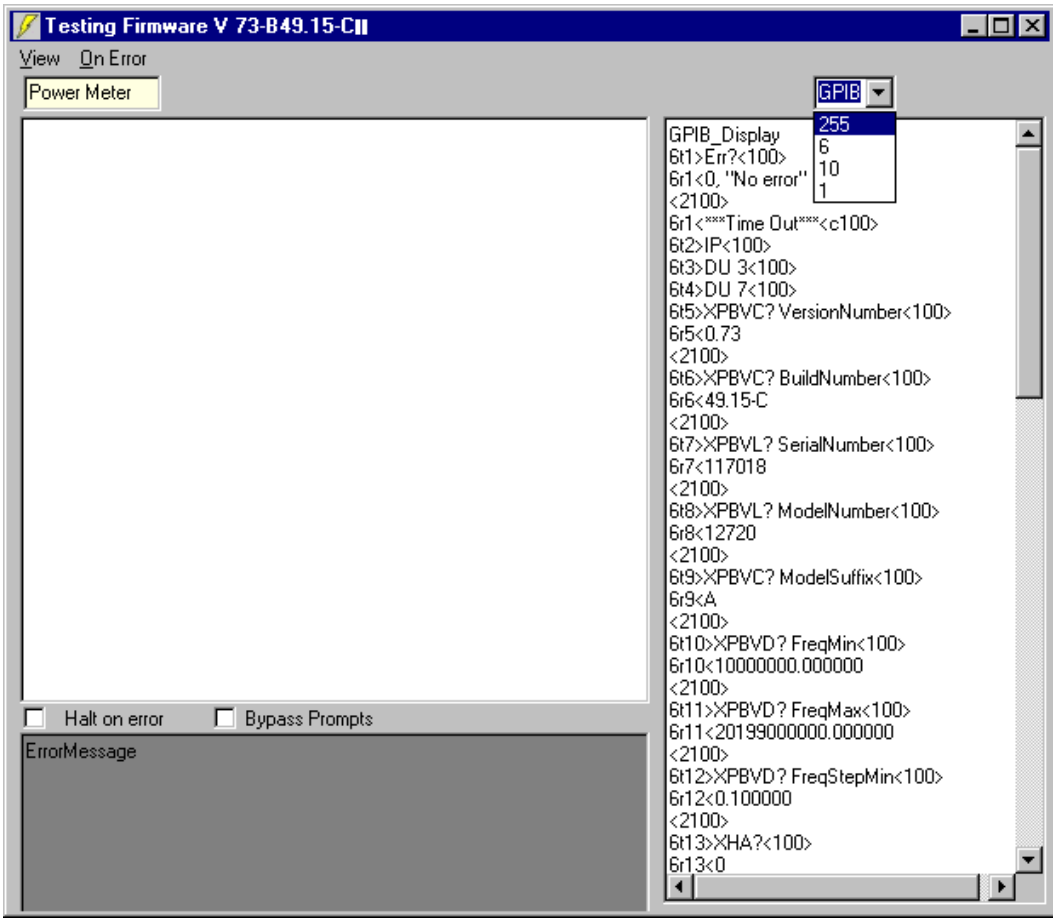


This view shows the choices available for the monitor screen.

- 'GPIB send/receive in display' puts the information in the GPIB Display Window under the GPIB Address box (shown below). The GPIB Address box initially shows 'GPIB' until an address is selected.
- 'GPIB send/receive in memo' puts the information in the same block (the one on the left) as the data. This allows easily seeing what command produced a specific data point.
- 'Show Power Meter' puts the power meter readings in the left block.



This view illustrates the ability to 'filter' the GPIB traffic. A setting of 255 causes the display to show traffic to any GPIB device on the bus. Entering a specific address will show traffic for that device only.



4

Theory of Operation

4.1 Series 12000A Theory of Operation

Theory of Operation	Model	
	124XXA	125XXA/ 127XXA
4.1.1 - Overall System Description	√	√

4.1.1 Overall System description

The Series 12000A is designed using a modular architecture where each basic system functional block is contained on a printed circuit or microwave module. DC power for the instrument is provided by a commercial switching power supply. This supply provides regulated voltages of +6, -6, +12 and –12 volts. The supply is filtered to reduce switching transients and routed to the A4 Distribution PC assembly. This board provides fuse protection, routing and turn-on timing for the supplies to the various other assemblies in the instrument. The A4 board also supplies switching and conditioning for the control lines to the various microwave modules, the step attenuator and Option 20 (High Power). The reference frequency for the instrument, 10 MHz, is supplied by the A15 Time Base PC assembly. The A11 CPU PC assembly supplies all the necessary data processing and control for the instrument. Its inputs include the IEEE 488 bus, the RS232 serial port and the front panel. It controls most of the other instrument PC assemblies via a peripheral data bus. The A11 outputs include many of the rear panel BNC connectors and the display.

Frequency synthesis and frequency modulation are controlled by the A1 Synthesizer PC assembly. This board, in conjunction with the 4-8 GHz YIG oscillator, supplies signals from 1 to 8 GHz. The output from A1 is routed to the A6 and A8 microwave assemblies.

The Frequency Extension Module (A5) accepts input signal from module A7 in the range of 10-20 GHz and creates signals in the range of 20-40 GHz using frequency doublers. The output signals are amplified, modulated (when required), and filtered to remove the undesired harmonics. The module also accepts the input signals from A6 in the range of .01-20 GHz and multiplexes to the main output, providing a full .01-40 GHz out. A wide-band directional detector provides RF level to D.C. voltage output over the combined frequency range of 2-40 GHz.

The A6 assembly contains the amplifiers, amplitude control elements and harmonic filters for the 2-40 GHz frequency range. The A8 assembly contains the same elements for the .01-2 GHz portion of the output range. Microwave module A7 houses the multipliers and filters to produce 8-40 GHz. Its output is routed to A6 for amplification and level control. The output of A6 is optionally routed through the step attenuator. Control of the amplitude functions (leveling and amplitude modulation) is provided by the A3 ALC PC assembly. This board receives level detector signals from A6 and A8 and returns modulator control signals.

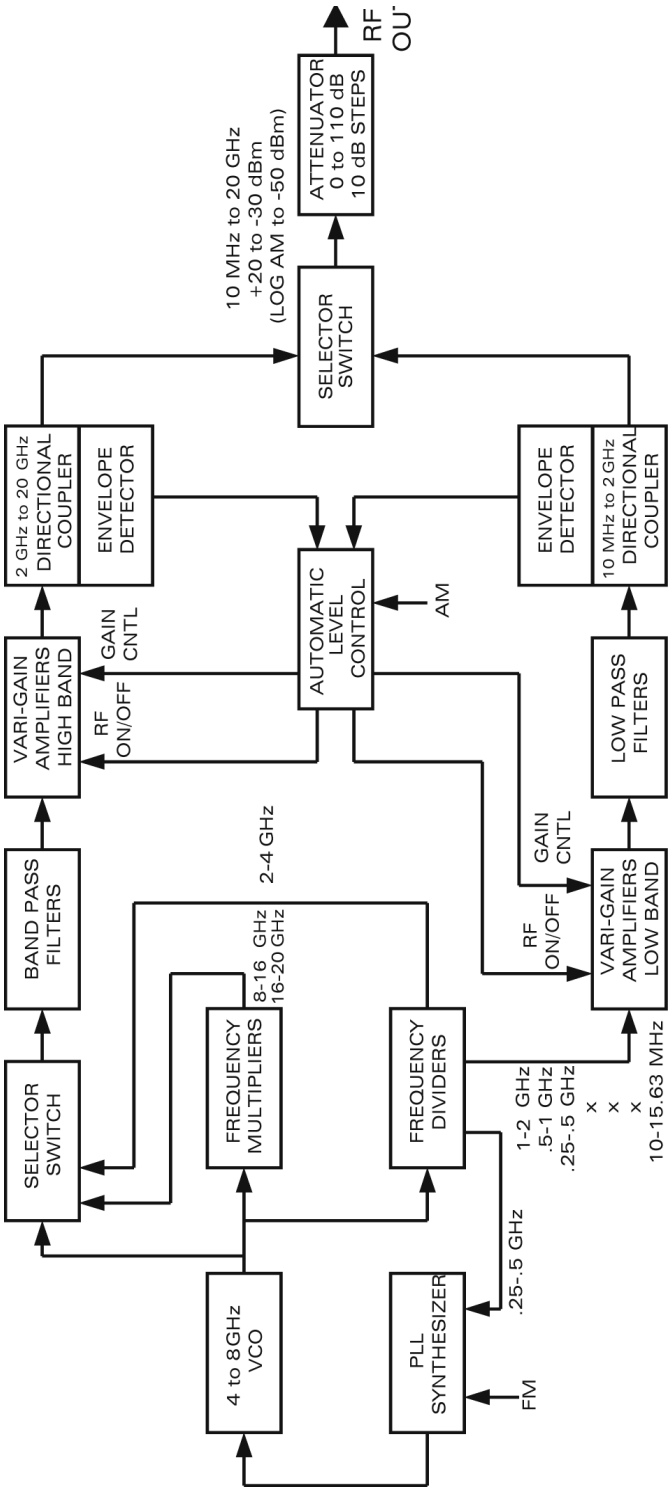


Figure 4-1: Overall Block Diagram

4.2 Power Supply Subsystem (A9)

Power Supply Subsystem (A9)	Model	
	124XXA	125XXA/ 127XXA
	√	√

The Power Supply Assembly consists of two separate power supplies that will accept inputs of 85 to 264 VAC from 47 to 63 Hz:

Standby +12v: Unswitched supply that is operational whenever the AC line cord is plugged in.

Main Supply: Switched Supply that is controlled by the front panel power switch with outputs of +6v, -6v, +12v, and -12v.

The standby power supply is used to provide continuous voltage to the time base oscillator and the YIG heater when the instrument is turned off. When the instrument is turned on, a diode steering network on the A4 assembly switches both the time base and the YIG heater to the main supply. The standby supply is then used to run the cooling fan.

4.3 Power Distribution Subsystem (A4)

Power Distribution Subsystem (A4)	Model	
	124XXA	125XXA/ 127XXA
4.3.1 - Electrical Operation/Circuit Description	√	√

The A4 Distribution assembly is used to condition and distribute the main power supply voltages and various locally generated voltages to the other assemblies. In addition, it provides control for the A5/ A6/A7/A8 modules, the fan, the step attenuator and the high power option.

4.3.1 Electrical Operation/Circuit Description

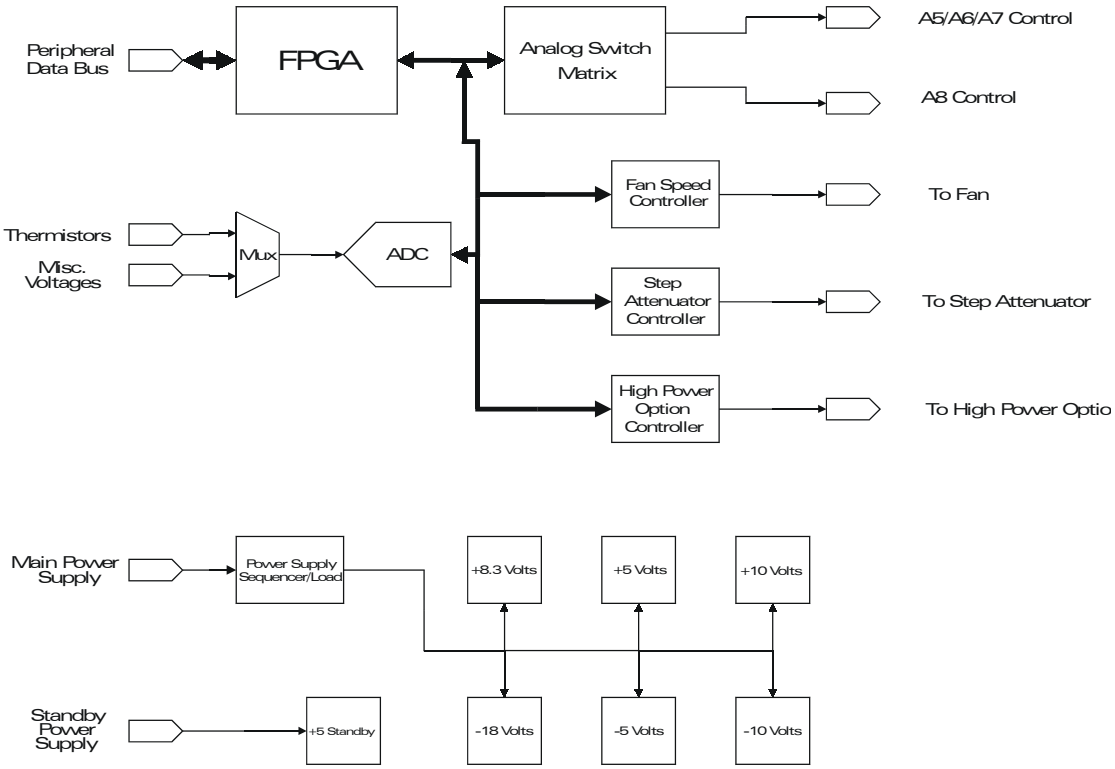


Figure 4-2: A4 Distribution Block Diagram

4.3.1.1 FPGA Interface

The instrument Peripheral Data Bus provides data from the CPU to the on board FPGA, U101. This device has its program code stored in a fuse-programmable memory chip, U102. The code is loaded into the FPGA at power up. The outputs from the FPGA are used to control all the functions represented on this board.

4.3.1.2 A5/A6/A7 Control

Control signals from the FPGA are used to drive a series of analog switches (U210-208). These switches send either a positive or a negative power supply voltage to the module interface connector, P201. The voltages are used to bias the various PIN diode switches in the microwave modules and thus select filters and other operational characteristics.

4.3.1.3 A8 Control

Other outputs from the FPGA are routed directly to the A8 microwave module via connector P102. These logic level signals are translated into appropriate analog signals on the A8 assembly for filter and other switching functions.

4.3.1.4 Fan Speed Control

IC U302 and its associated circuitry are used to provide control of the speed of the main cooling fan. Thermistor RT301 senses the ambient temperature in the instrument and U302 produces a pulse width modulated signal to control FET Q301 and thus the fan itself. The circuit is set up to run the fan at a minimum speed regardless of low temperature. As the temperature increases above the minimum set point, the fan speed rises proportionally.

4.3.1.5 Analog to Digital Converter

A multi-input ADC (U301) is provided on this assembly to monitor various voltages and send the information back to the CPU. Inputs are provided to monitor the temperature of each of the microwave modules that has a leveling detector. This data is then used for temperature compensation of the RF level. The timebase VCXO control voltage is monitored to allow calibration and determine if an external source is connected. Monitor lines from the step attenuator and high power options are used to determine the presence of these items.

4.3.1.6 Step Attenuator Option Control

The optional step attenuator is controlled using driver U304, inverters U303 and transistor Q302. Logic signals from the FPGA are used to control each of the four cells in the attenuator. The cells have values of 10, 20, 40 & 40 dB. Each of the four cells has both an 'on' and an 'off' control line, thus the need for eight drivers. The attenuator has a mechanical device which latches the actuators so the control voltage only supplies current for a few milliseconds at each transition. The attenuator is specially built to have one of the normally unused connector pins tied to ground. This line is monitored to determine the presence of the attenuator.

4.3.1.7 High Power Option Control

The optional high power amplifier assembly is also controlled from the A4 assembly. Q304 and Q303 provide control for the main power to the assembly. U305 and Q305 are used to select either the .01-2 GHz range or the 2-20 GHz range. Two pin diode drive lines (+5 or –18 volts) are also supplied via U305.

4.3.1.8 Standby Power Supply

To be able to keep the heaters on the timebase oscillator and the YIG oscillator operating with the instrument turned off, a separate standby power supply is used. This supply produces +12 volts. The steering diodes, CR418, CR419, and C420, ensure that the YIG heater and timebase are driven off the quieter +12V supply during operation. When the unit is in Standby mode, these diodes provide the +12SB voltage. A voltage regulator composed of U405, U406, Q407, and Q408 is used to produce the +5 volts needed by the timebase oscillator. This supply needs to be very low noise, thus the discrete regulator. R432 is used to reduce dissipation in the regulator pass transistor. A voltage monitor (to the ADC) allows determining when the oven is at operating temperature.

4.3.1.9 Power Supply Sequencing

U401, Q404, Q405 and the other associated circuitry are used to insure that the +12 and +6 power supplies do not come up prior to the negative supplies. A delay is provided by R417 and C402. The power fail signal from the power supply is used to shut off the positive supplies first.

4.3.1.10 System Power Supplies

Although many of the other assemblies in the instrument produce power supply voltages from the four primary supplies, the A4 assembly does produce a number of voltages.

- The +8.3 volt supply is used by the A6 module for amplifier power
- The –18 volt supply is used to switch PIN diodes on A6
- The +5 volt supply is used for logic power and PIN diode switching on A7/A7
- The –5 volt supply is used for PIN diode switching on A7
- The +/-10 volt supplies are used by the CPU board as well as A5/A6/A7/A8

Each of these supplies is produced by a 'three terminal' regulator. The –18 volts is regulated down from a +20 volt switching type boost supply (U410-412). Three devices are used to supply the needed current.

A series of multi-pin connectors distributes the four primary power supply voltages, each of which is fuse protected. A series of green LED indicators signals that each of the primary supplies (and the standby supply) is active. A series of red LED indicators, each connected across one of the fuses, signals that the corresponding fuse has been blown.

4.3.1.11 Source Block

An amplifier provides for gain and input buffering. A Wilkenson power divider samples and returns A7's output signal. Another amplifier provides for more gain. To realize sub-harmonic and harmonic filter rejection, a SP3T switch splits the signal into three bands. The frequency ranges covered by the doublers are as shown on the block diagram. Each of the succeeding circuits in the Source Block is in triplicate due to the band splitting. The doublers are passive and consist of conventional beam lead schottky diode pairs at the intersection of a co-planar waveguide/slotline junction. A 20 to 40 GHz amplifier recaptures some of the loss of the doublers. A dual attenuator approach provides 50 dB dynamic range. 10 dB is used to bring the signal into a linear range (out of saturation). The rest of the dynamic range is utilized for amplitude control and/or AM modulation. A set of three identical broadband, medium power, 20 - 40 GHz MMW amplifiers boosts the signal up to the 100 mW range.

4.3.1.12 Output Combiner

Three band pass filters remove higher order and sub harmonics generated by the doubler and amplifier. A diplexer/low pass filter in conjunction with a PIN diode switch recombine the three bands and the 10MHz to 20 GHz input from module A6. The broadband coupler/detector provides R.F. level to D.C. voltage conversion for 2-40 GHz. Finally, the signal is routed to the module's 10 MHz to 40 GHz output connector.

4.3.2 System Interface

The A5-A1 board interfaces the A5 module to the 12000 system. It distributes all of the power supplies and control lines to A5 via feed-thru and socket connections. The module receives regulated power supply voltages and TTL band-switching commands from the Distribution Module (A4) via a multi-pin connector (see attached Control Logic diagram for more detail). An ALC loop is established between the ALC Module (A3) and the Frequency Extension Module (A5) via the AM drive signals from the former and the sampled output signals from the latter. The Interface Board conditions the signal from the ALC Board to provide the appropriate modulator voltage for both leveling and amplitude modulation. For min attenuation, V1=0V, V2=-10V. For max attenuation, V1=-10V, V2=0V. The input control voltage to J4 on A5-A1 is 0 volts for min attenuation and -3 volts for max attenuation.

4.4 CPU Subsystem (A11)

CPU Subsystem (A11)	Model	
	124XXA	125XXA/ 127XXA
4.4.1 - Memory Resources	√	√
4.4.2 - Reset Circuitry	√	√

The CPU board is the main control element within the instrument. Following is a brief list of the resources and functions that the board provides.

4.4.1 Memory Resources

- 2 M of 0 wait state SRAM
- 1 M of Flash memory
- 1 M of battery backed SRAM, expandable by memory expansion board

4.4.1.1 Next Step Sequencer

Provides high-speed sequencing of signals used to change frequencies or power levels.

4.4.1.2 Peripheral Bus Interface

An 8 bit parallel interface to all other modules in the GT12000A.

4.4.1.3 Video Controller

Provides interface to a 320 x 240 pixel LCD display on the front panel.

4.4.1.4 Front Panel Interface

Provides keyboard, LED, Knob, and Piezo Buzzer interfaces.

4.4.1.5 GPIB

Provides a GPIB interface for the rear panel.

4.4.1.6 Rear Panel I/O

Provides RS232 interface, Blank / Mark BNC, Stop Sweep BNC, Lock/Level BNC, Trigger In, Trigger Out.

4.4.2 Reset Circuitry

The reset signal for the CPU is generated when the +5V supply drops below 4.65 volts. The main power supply generates a power fail signal which provides at least 5mS warning before the output goes out of regulation after AC power is turned off.

4.4.2.1 Serial Bus

The LCD contrast, Front Panel LEDs, calibration Trim-DACs on the Time Base board, and an ADC on the Distribution board are all controlled with a serial data bus. Discrete I/O pins from the CPU and one of the I/O ports are used for this bus. The pins are controlled by software to shift data serially into and out of devices. The serial bus is connected to the Distribution Board via P701. Chip select outputs on the CPU enable the LCD contrast and Front Panel LED serial ports. Chip selects for the calibration Trim-DACs and Distribution Board ADC are controlled over the Peripheral Bus by writing values to registers on the Distribution Board.

4.4.2.2 FLASH Memory

4 – 512 K x 16 word (2 Megabyte) parts provide non-volatile storage for firmware.

Jumper JP201 along with Q203 and associated components allows the FLASH boot block to be programmed. If 12V is provided on the RESET pin, the boot block protection is temporarily disabled and the boot block can be erased and reprogrammed.

4.4.2.3 NVRAM + Expansion

2 - 512 k x 8 Static RAMs (1 Megabyte) are used to hold the instrument configuration data, settings, user data, and list mode settings when power is removed. A memory expansion connector, P202 allows up to 4 more devices to be added for a total of 3 Megabytes of NVRAM storage. A lithium battery provides backup power.

4.4.2.4 FPGA

A Field Programmable Logic Array provides the following functions:

- Next Step Sequencer –Used to coordinate frequency and power level changes.
- Peripheral Bus Sequencer – Controls the transfer of information over the P. Bus.
- Front Panel Interface – Provides an interface to the Keyboard, Knob, and Piezo Buzzer.

4.4.2.5 Peripheral Bus Interface

The Peripheral Bus is used to communicate with other assemblies in the instrument such as the Distribution Board, the Synthesizer, and the ALC. The Address and Data signals are multiplexed onto a single 8-bit bus whose transfer rate is limited to 1 MHz to reduce bus generated EMI. EMI reduction is accomplished by slowing down the signal edges with series resistors and capacitors.

4.4.2.6 Front Panel Interface

Logic for interfacing to the keyboard, optical encoder, and piezoelectric buzzer is contained in the FPGA. Front Panel indicator LEDs are driven serially by the CPU.

4.4.2.7 Video Controller

A Graphics Controller and 32 K x 16 SRAM provides a complete video controller to drive a 320 x 240 pixel LCD display. A clock frequency of 6.25 MHz gives a display refresh rate of about 74 Hz.

4.4.2.8 LCD Bias and Contrast Supply

U507 and associated circuitry provide a –22V bias supply for the LCD panel.

LCD contrast is adjusted by U506. The serial data bus controls U506.

4.4.2.9 GPIB & RS232 Interfaces

A National Instruments NAT9914 provides all of the control logic for the GPIB interface. A 75ALS160 and 75ALS162 function as GPIB bus transceivers. The GPIB controller shares the CPU's second DMA channel with the CPU's serial port and the I/O Expansion Board. The CPU has two integrated serial ports. A MAX213 translates TTL level signals from both ports to RS232 voltage levels. The device contains built in voltage doublers to translate +5V into levels suitable for RS232.

4.4.2.10 External Rear-Panel Connections

There are several BNC connections on the rear panel that are controlled by the CPU :

Trigger In, Trigger Out, Lock /Level Out, Stop Sweep I/O (a bi-directional signal) and Blank / Marker. This output is at +5V when MARK/BLANK_HIGH is at +5V, -5V when MARK/BLANK_LOW is at +5V, or 0V out when both inputs are at 0V.

4.4.2.11 I/O Expansion Connector – P703

This connector provides address, data, and control signals for an additional I/O port

4.4.2.12 Power Supplies

Linear voltage regulators convert +6 volts down to +5 V and +3.3 V.

4.5 Front Panel Subsystem (A10)

Front Panel Subsystem (A10)	Model	
	124XXA	125XXA/ 127XXA
4.5.1 - Memory Resources	√	√
4.5.2 - Piezo Buzzer	√	√
4.5.3 - LEDs	√	√
4.5.4 - Inverter Supply	√	√
4.5.5 - LCD Module	√	√
4.5.6 - Optical Encoder	√	√

The A10 Assembly accepts outputs from the A11 (CPU) Assy. and sends the information to a 320 X 240 dot LCD display, fourteen LEDs, and a piezo buzzer. The contact information from the 50 pushbuttons and the optical encoder is sent to the A11 (CPU) Assembly.

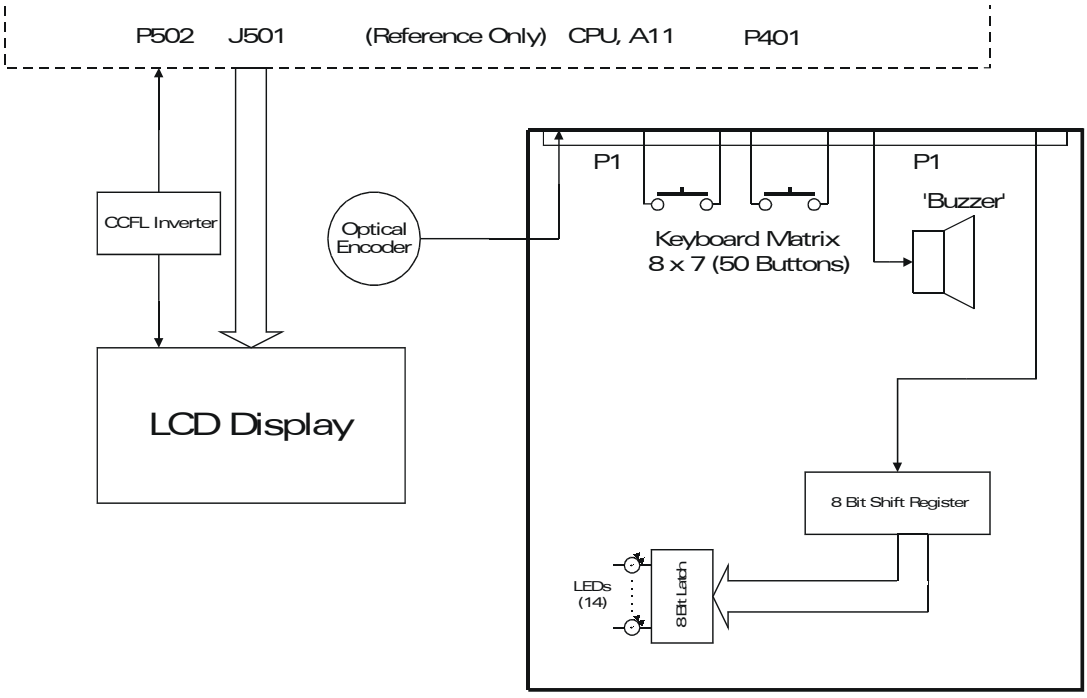


Figure 4-3: A10 Block Diagram

This assembly is functionally divided into six blocks. Three of the blocks are physically on the A10 PCA. The other three blocks are assemblies that are attached to it. Logic for interfacing to the keyboard, optical encoder, and piezoelectric buzzer is contained in the FPGA on A11 (CPU) Assembly.

4.5.1 Keyboard Matrix

There are no active parts on this portion of the assembly, only switch contacts. Debounce and decoding are done in software on A11 (CPU). The row and column information is sent to A11 (CPU) via connector P1. The keyboard is an 8*7 switch matrix of 50 pushbuttons. The row outputs are configured as open collector outputs. Normally, they are all driven low at the same time. When a button is depressed, the low is transferred to one of the column inputs and the FPGA interrupts the CPU. The CPU then scans each keyboard row to determine which button was pressed. Continuous scanning of the keyboard is avoided to reduce EMI.

4.5.2 Piezo Buzzer

The buzzer interfaces with A11 (CPU) via P1. The piezo buzzer interface can produce a continuous 2.5 kHz tone, a 5 kHz tone, or a single click. The CPU controls tone duration by turning the tone on or off. The click is a single 100uS pulse applied to the piezo buzzer. Piezo volume can be set to 8 different levels. Level 0 is off, and level 7 is the highest volume level.

4.5.3 LEDs

Serial data from A11 (CPU) via P1 enters two 8-bit shift registers where it is converted to parallel data that is routed to two 8-bit Latches. The latches store the LED information and also drive the fourteen front panel LEDs.

4.5.4 Inverter Supply

This supply is attached to the A10 Assembly. The supply accepts +5V from the A11 (CPU) Assembly and outputs 230VAC to the LCD assembly for backlight illumination.

4.5.5 LCD Module

The assembly is attached to the A10 Assy. LCD data and contrast signals come from the A11 (CPU) Assembly. The display is mounted to the Signal Generator's front panel, and connected via a ribbon cable to A11 (CPU) J501. The ribbon cable carries all of the signals and power for the display.

4.5.6 Optical Encoder

The encoder mounts to the front panel and is connected to the A10 Assembly with a five-pin cable. The optical encoder is driven by a knob on the front panel and has 64 counts per revolution. Turning the optical encoder knob rapidly, about 3 revolutions per second, produces about 200 counts per second.

4.6 Timebase Module Subsystem (A15)

Timebase Module Subsystem (A15)	Model	
	124XXA	125XXA/ 127XXA
4.6.1 - Synthesizer Subsystem (A1)	√	√

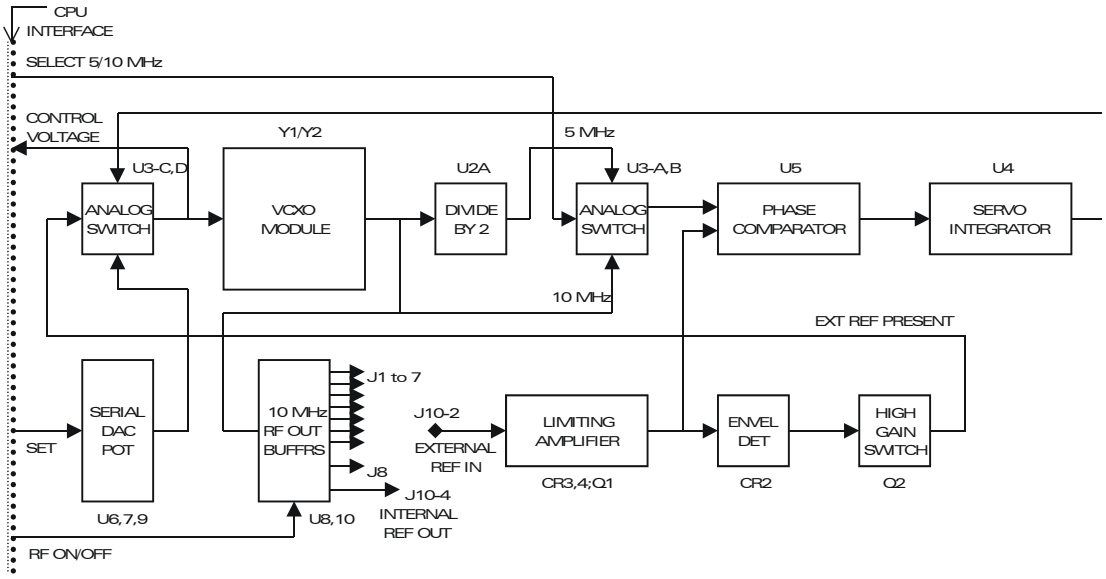


Figure 4-4: A15 Block Diagram

A15 supplies several modules with a 10 MHz frequency standard. There are eight low current-drive outputs and one high-current drive output. One of the low current drive outputs feeds the rear panel BNC connector. The standard is derived from an on-board ovenized 10 MHz voltage controlled crystal oscillator module.

Regardless of whether the operating frequency is derived from the internal crystal oscillator module or an external source, it is the internal module that actually feeds 10 MHz to the A15 outputs. The oscillator feeds three high current buffers. Two outputs of are paralleled and feed J8; the remaining one feeds the inputs of the other eight buffers which feed the remaining coaxial output connectors.

When there is no external frequency reference signal present, the oscillator tuning control voltage is maintained by the CPU at a level determined at the last calibration. The CPU can constantly read the control voltage and adjust it by controlling a digital potentiometer.

Whenever an External Frequency Reference signal is present an envelope detector senses the signal and provides an output to switch control of the VCXO to a phase lock loop. This PLL locks the VCXO to the external source with a very slow loop to filter most of the noise from the external signal. Divider U2A allows the PLL to accept a 5 MHz external source in addition to a 10 MHz one.

4.6.1 Synthesizer Subsystem (A1)

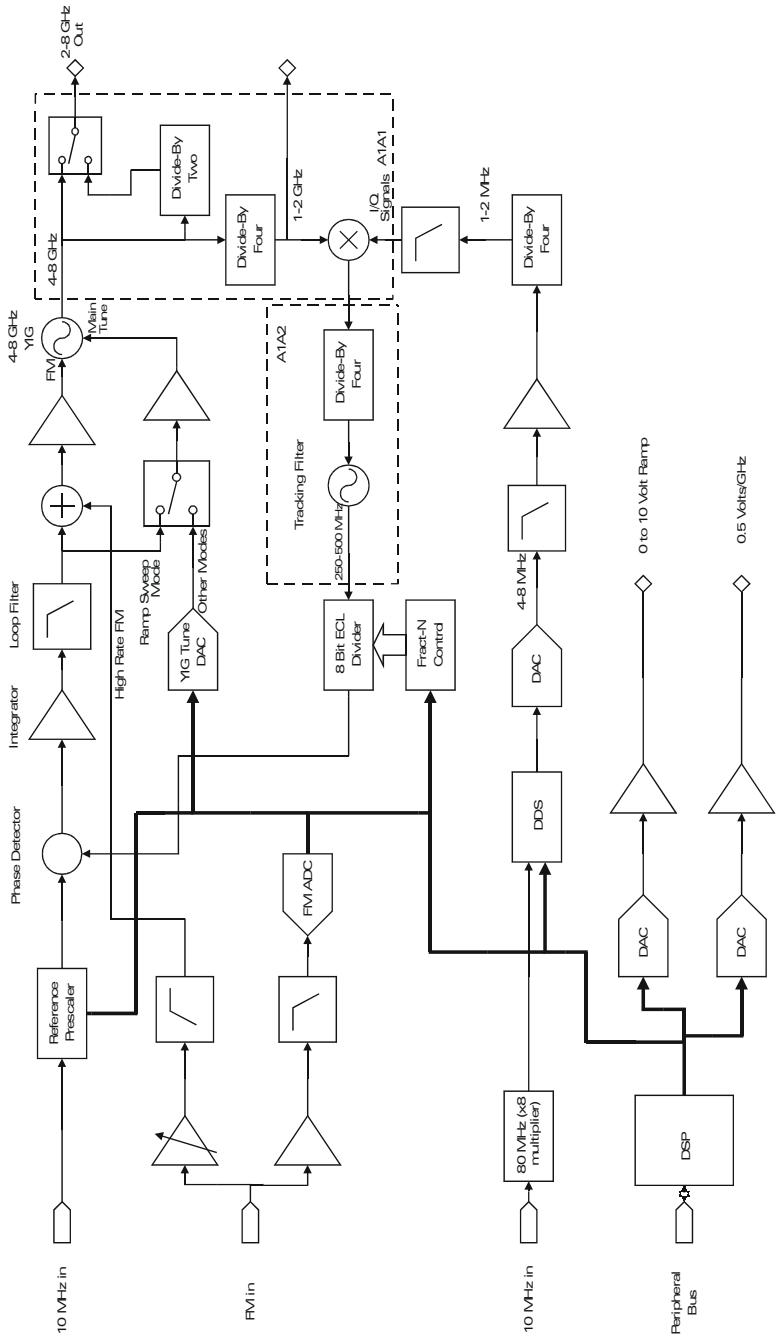


Figure 4-5: A1 Synthesizer Block Diagram

The A1 PC Assembly is used to generate the basic synthesized signal for the instrument. All elements of this function other than the YIG oscillator and the YIG driver FET are contained on the board or on the attached A1A1 and A1A2 assemblies. The assembly provides all the frequencies from 1 to 8 GHz.

The synthesizer may be logically divided into a number of sub-blocks. These are: (1) The primary synthesis loop (2) The high resolution DDS (3) The YIG oscillator main tune coil driver (4) The frequency modulation system and (5) The control system.

4.6.1.1 Primary Synthesis Loop

The primary synthesis loop consists of the Phase Detector, Integrator, Loop Amplifier, YIG Oscillator, A1A1/A1A2, and the Divide-by-N.

The 10 MHz reference input for the phase detector is produced on the A15 Timebase board and is an isolated output to avoid adding any noise to the signal. On the A1 assembly, the 10 MHz is normally routed directly to the phase detector. A divide-by-four pre-scale is used when in the wide FM mode. The other input to the phase detector comes from the output of U510, a programmable 8 bit counter. The preset inputs of this counter are controlled by FPGA U508. The primary purpose for this FPGA is to do the necessary tasks to implement the "Fractional-N" required to obtain 4 MHz resolution in the main loop.

The input to the 8 bit counter comes from the output of the A1A2 tracking filter. This frequency varies from 250 to 500 MHz over the 4-8 GHz range if the YIG oscillator. The counter output drives the 'variable' input of the phase detector (flip-flops U513 and gate U518). Its two outputs go to the integrator.

There are actually three separate integrators used. The first, a 'double integrator' (U601A & U601B) is used in the 'CW' mode (i.e. no FM and not in Ramp Sweep). The extra integrator stage provides additional gain for noise suppression. The second integrator (U602) is used for the wideband FM mode. The remaining integrator (U603) is used for Ramp Sweep. This mode uses the main tuning coil of the YIG oscillator rather than the FM coil. Since the sensitivity and response characteristics are considerably different, a separate integrator is needed.

Amplifier U606 provides a low impedance drive for the loop low pass filter. This filter is included primarily to suppress the 'delete rate' spur of 250 kHz (produced by the Fractional-N). Following the filter is gain control amplifier U608. The gain of the loop will vary as the 'N' number is changed. In this case, a 2:1 change will occur from 4 to 8 GHz. To both maintain stable loop operation and also to allow the FM to work properly, the gain of the loop must be increased as the 'N' number increases.

The final elements of the primary synthesis loop are filter C742, L703, C743 and the FM coil driver U701. The filter provides additional high frequency attenuation. The FM coil driver is a high current device (about 200 ma output) which drives the YIG oscillator FM coil.

4.6.1.2 High Resolution DDS

To enable the synthesizer to have 0.1 Hz resolution, a Direct Digital Synthesizer (DDS) is used in conjunction with a SSB mixer in the A1A1. This DDS is programmed by the DSP and produces steps of 0.025 Hz. Due to the divide-by-four prior to the SSB mixer in the A1A1, the DDS output is effectively multiplied by four at the output of the synthesizer.

4.6.1.3 YIG Oscillator Main Tune Coil Driver

The driver for the YIG main tune coil converts a voltage based 'command' from the control system into a current which tunes the oscillator. The tuning resolution is approximately 60 kHz. The driver also includes the circuitry to switch in the noise reduction capacitor.

A 16 bit DAC (U702), controlled by the DSP, and amplifier U705B provide a voltage proportional to frequency. Amplifier U705A compares the voltage from the DAC to the amplified voltage from the current sense resistor R724. The output of the amplifier is used to control power FET Q703. This FET, in series with the supply voltage to the YIG oscillator main tune coil, effectively sets the current through the coil and thus determines the frequency.

To maintain a fast switching speed, it is necessary to minimize any capacitance across the YIG coil. This, however, results in considerable noise being applied to the oscillator and would degrade the spectral purity of the output signal. To reduce the noise, capacitor C746 is connected across the main tune coil once the instrument has acquired phase lock after a frequency change. The capacitor must be 'pre-charged' to exactly match the voltage across the coil prior to being connected to prevent transients.

NOTE: *There are no adjustments in this circuit. Each time the instrument is powered up a calibration routine is run to determine the proper setting for the DAC to produce a locked condition with the loop control voltage close to zero. Two points are determined, one near 4 GHz and the other near 8 GHz. The computer then uses this information and linearly changes the DAC output proportional to the desired frequency. During instrument operation (in most modes other than sweep) the loop voltage is monitored and the setting of the DAC is changed, one bit at a time to maintain the loop near zero. This change is not noticeable and automatically corrects for any drift or non-linearities.*

4.6.1.4 Frequency Modulation System

External frequency modulation for the instrument is controlled entirely by this assembly. Since the modulation frequency spans DC to 1 MHz, it is necessary to modulate both 'within the loop' and 'outside the loop'. Modulation inside the loop is accomplished using the DDS, modulation outside the loop is summed directly into the YIG FM coil driver.

The signal for the 'Inside the Loop' portion of the FM goes through active filter U312, a fixed low-pass filter and the high speed ADC. The digitized signal is sent to the DSP which uses it to reprogram the frequency setting of the DDS at a 1 MHz rate, thus frequency modulating the DDS output. Since the control is wholly digital and the input is DC coupled, true DCFM is possible with full synthesizer accuracy.

The signal for the 'Outside the Loop' portion of the modulation (effectively everything above 15 kHz) passes through a high pass filter to remove the DC component. The signal for this path has its level adjusted to match the deviation of the inside the loop portion by DAC U302 and analog multiplier U303. Additional gain selection (primarily for input sensitivity setting) is provided by a resistor network, switch U304.and amplifier U305. The output of U305 goes to the YIG FM coil driver.

Due to the phase shift caused by both the primary loop and the tracking filter loop, it is necessary to provide additional compensation to maintain the flatness specification of the deviation. Amplifiers U318 and U320 comprise active filters to produce the required correction. The correction signal amplitude is adjusted using DAC POT U319. During narrow FM operation, switch U604 connects the correction signal directly into the phase detector.

4.6.1.5 Control System

The various functions and operations of the Synthesizer are controlled by various logic devices. Commands from the host CPU are sent to the Synthesizer via the Peripheral Data Bus. A DSP, U104, and a CPLD, U105, decode these commands and route them to the appropriate destinations.

Two analog output signals are generated on the Synthesizer board. These are the 10 volt ramp and the 0.5 volt/GHz output. The 10 volt ramp is a signal used during sweep modes and goes from zero volts at the start of a sweep to 10 volts at the end of the sweep. The 0.5 volt/GHz signal is always present and is proportional to the operating frequency.

A multiple input Analog to Digital converter (U710) is monitored by the control system to provide information on various voltage levels. The include the PLL voltages for both the primary and tracking filter loops, various FM system voltages, and the YIG driver. The readings are used for the calibration and automatic adjustment functions.

Because the synthesizer is sensitive to noise on the power supplies it uses, on board regulators are provided. The majority of these consist of an op-amp and power transistor rather than a packaged regulator. This is done to provide the lowest noise. A precision reference, U807, supplies 5 volts to the regulators. U810 is a switching boost type regulator used to provide 20 volts for the YIG driver and the tracking filter VCO drive.

The Ramp Sweep mode of operation uses a different method to achieve phase lock. Rather than using the YIG driver to coarse tune the YIG and the FM coil to close the loop, the YIG DAC is not used and the loop voltage is fed to the main coil via the remaining driver circuitry. This permits ramp sweep to operate by stepping the frequency in very small (sub-hertz) steps at a high rate of speed.

4.7 Microwave Signal Conditioning Subsystem (A6/A7)

Microwave Signal Conditioning Subsystem (A6/A7)	Model	
	124XXA	125XXA/ 127XXA
4.7.1 - A6 Output Module	√	√
4.7.2 - PIN Diode Pulse Modulator	N/A	√
4.7.3 - Gain Blocks A1-A4	√	√
4.7.4 - Switched-Low Pass Filter	√	√
4.7.5 - Directional Detector	√	√
4.7.6 - A7 Multiplier	√	√

4.7.1 A6 Output Module

The output module (A6) is a wide-band component (2-20 GHz) that provides most of the processing functions of the microwave signal such as: amplification, harmonic filtering, amplitude modulation, and pulse modulation. It can accept the .01-2 GHz signal from the optional Digital Down Converter (A8) to provide .01 to 20+ GHz coverage from a single test port and features a built-in 2-20 GHz directional detector as part of the ALC function.

4.7.2 PIN Diode Pulse Modulator

Located at the input of the module (J1), this component provides high speed amplitude modulation of the 2-8 GHz signal delivered from the synthesizer module. Pulse modulating the 2-8 GHz signal provides the added benefit that subsequently multiplied signals (8-20 GHz through A7, and 20-40 GHz through A5) can also be pulse modulated with no added hardware.

4.7.3 Gain Blocks A1-A4

The gain blocks are GaAs MMIC with dual-gate FET cells. The gain of A1 and A2 are varied together for ALC and AM application, A3s and A4s gain control input provides scan modulation.

4.7.4 Switched-Low Pass Filter

The 2-20 GHz spectrum is redirected into 5 sub-bands (2-3.2, 3.2-5.1, 5.1-8, and 8-20 GHz) with low-pass filters to remove harmonics. An additional switch arm on the output side can also receive the low-band signal (.01-2 GHz) from the optional Digital Down Converter (A8).

4.7.5 Directional Detector

The directional detector consists of a multi-section microstrip coupler with dielectric overlay compensation, built-in termination and a single-diode broadband detector at the coupled port.

4.7.6 A7 Multiplier

The function of module A7 is to produce the 8-20 GHz signal from the 4-8 GHz received from A6, and to remove the spurious products of frequency multiplication by band-pass filtering. The 4-8 GHz signal

is first multiplied by a frequency doubler (ADA1) to produce 8-16 GHz. The output is then split into four bands by a SP4T PIN diode switch; the first three are band-pass filtered to produce the following frequencies: 8-10.1 GHz, 10.1-12.7 GHz, 12.7-16 GHz. The 8-10.1 GHz band is also used to drive the second frequency doubler (ADA2) to produce 16-20.2 GHz. The four frequency bands are filtered to remove the 1/2s and 3/2s spurious signals and combined by a second SP4T switch.

4.8 Interface Assembly (A17)

Interface Assembly (A17)	Model	
	124XXA	125XXA/ 127XXA
	√	√

This printed circuit assembly is used to connect microwave assemblies A6 (2-40 GHZ Output Module) and A7 (Multiplier Module) to the rest of the system. The board provides signal conditioning and routing for both the detector outputs and some of the modulator inputs. Connector P1 delivers power and PIN diode switching signals to both A7 and A6. PIN diode signals (for switch filters) pass through resistors R8-R20 before connecting A6 and A7.

There are two amplifier channels used as detector buffers. One, for CW operation, provides low noise, low drift gain. The other, for pulse operation features fast rise time. The outputs feed the ALC assembly.

4.9 Down Converter (A8)

Down Converter (A8)	Model	
	124XXA	125XXA/ 127XXA
4.9.1 - The Source Block	√	√
4.9.2 - The Amplifier & Modulator Block	N/A	√
4.9.3 - The Switch-Filter Block	√	√
4.9.4 - The Control Logic Block	√	√
4.9.5 - System Interface	√	√

The Digital Down Converter module accepts signals in the range of 1-2 GHz at 4-8 dBm and outputs signals in the range of .01-2.0 GHz at –25 to +18 dBm. The module also provides pulse modulation, amplitude modulation, harmonic filtering, and signal level detection for automatic level control Functional Block Diagram.

The Down Converter is divided functionally into four major circuit blocks:

4.9.1 The Source Block

This is a chain of programmable frequency prescalers and a SP4T switch-combiner. The prescalers perform frequency division (n=2, 4, 8, 16, 32, 64, or 128) on the input signal and the SP4T selects the outputs of the various prescalers which is sent to the Amplifier and Modulator Block. To prevent the generation of the sub-harmonics of the desired signal that are impossible to remove later, unused lower-order prescalers are turned off.

4.9.2 The Amplifier & Modulator Block

This section provides signal amplification, attenuation (modulators), and pulse modulation (ON/OFF) for the full output frequency range of .01 – 2.0 GHz. The amplifiers and modulators are organized in a distributed fashion to minimize the interaction over the frequency range.

4.9.3 The Switch-Filter Block

The incoming signals from the Amplifier/Modulator are directed into fifteen contiguous frequency bands to reduce harmonics. To facilitate signal-blanking and band-switching from the system standpoint, each filter's operating bandwidth is exactly one-half octave wide and a sub-multiple of the original input frequency range (1.0-1.414 GHz, and 1.414-2.0 GHz). The switch-filter matrix is arranged such that the signals that pass through the six lowest-frequency filter bands will be pre-filtered by a filter 3-octaves higher in frequency. The directional coupler and detector located at the output samples and detects the output signal level for ALC and AM purposes.

4.9.4 The Control Logic Block

This portion provides proper drivers to interface between the Down Converter and the Distribution module (PIN diode switch drivers) and between the Down Converter and the ALC module (PM and AM drivers and detector amplifier).

4.9.5 System Interface

R.F. input is supplied by the A1-A1 synthesizer front end and R.F. is output to the A6 output module. The module receives regulated power supply voltages and TTL commands from the Distribution Module (A4) via a multi-pin connector.

4.10 Automatic Level Control (A3)

General Architecture	Model	
	124XXA	125XXA/ 127XXA
4.10.1 - General Architecture	**N/A**	√
4.10.2 - CW Operation	√ (Limitations Apply)	√
4.10.3 - Linear AM Operation	**N/A**	√
4.10.4 - Logarithmic Scan AM Operation	**N/A**	√
4.10.5 - Pulse Modulation PM Operation	**N/A**	√
4.10.6 - Digital Communications, Controls & Calculations	√	√

The Automatic Level Control (ALC) board (A3) contains a feedback control system that maintains the RF output amplitude in accordance with the desired value. It also provides linear Amplitude Modulation (AM), Logarithmic Amplitude Modulation ("Scan"), and Pulse (square wave) Modulation (PM), using whatever arbitrary modulation waveform or timing it receives from the modulation signal sources outside of or within the 12000A chassis for the Series 125XXA/127XXA models.

Closed loop power control of an RF amplifier subsystem can be maintained by the ALC from +20 dBm to –20 dBm. Open loop power control (used for Log AM) can range from +20 dBm to –50 dBm. When the optional 110 dB, automatically controlled 10 dB step attenuator is installed, the range is expanded down to –130 dBm. This electromechanical attenuator permits the RF amplifier subsystem to operate between 0 dBm and +10 dBm for all 12000A output CW levels and AM carrier levels, (except above +10 dBm). Log AM fiduciary levels range between +5 and +15 dBm.

Under normal closed loop critically damped operation, leveling time is about 100 μseconds. By jamming measured, saved, and updated final drive level requirements as a function of 12000A output power into the integrator accumulator just before the leveling loop is closed, leveling time can be reduced to a few microseconds.

The 12000A contains up to three RF amplifier subsystems—for 10 MHz to 2 GHz (A8), for 2 GHz to 20 GHz (A6/A7/A17), and for 20 GHz to 40 GHz (A5). Each of these subsystems contains analog RF gain control elements that the ALC uses as the final drive to control output power level. At the output of each of these subsystems is a directional coupler, diode envelope detector, and a set of video preamplifiers to provide the ALC with a monotonic DC voltage scale of instantaneous RF envelope output power. During the automatic characterization procedure (see Section 5.5), a record of DC voltage vs. RF output power (actually peak RF voltage) at various frequencies is obtained.

The following conceptual block diagram (Figure 4-6) shows the above connections between a typical 12000A RF amplifier subsystem ("microwave module") and the ALC board. Also shown is the ALC board controlling the RF on/off switch, which is also used as the final drive for Pulse Modulation.

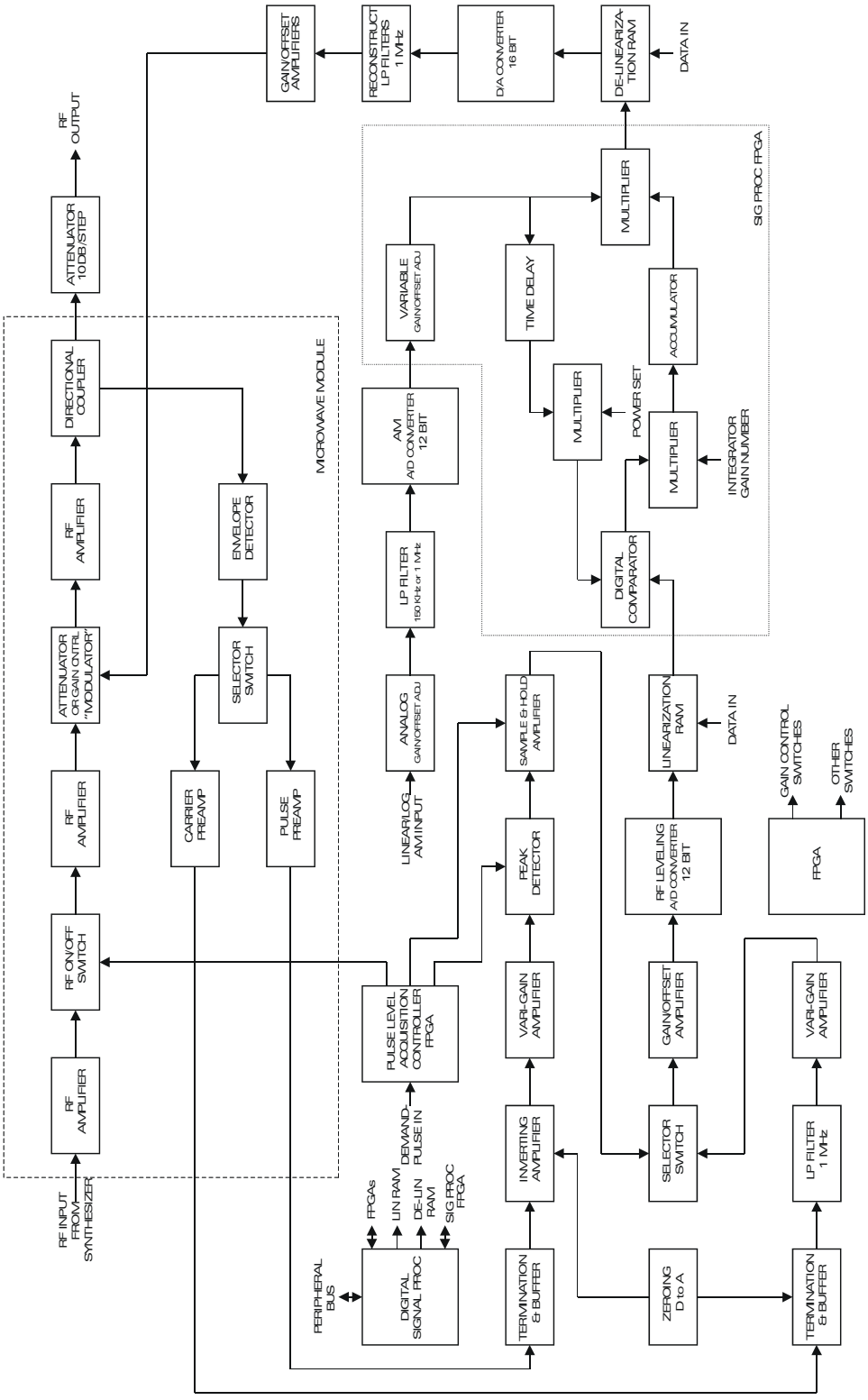


Figure 4-6: A3 Conceptual Block Diagram

4.10.1 General Architecture

Owing to the time it takes for a signal to propagate completely around the control loop (especially including through the gain control elements and RF amplifiers), the servo loop bandwidth is limited to about 10 KHz. However (for reasons explained below), all stages in the main loop are flat from DC up to almost 1 MHz.

The ALC servo element is a high speed, digital hardware-based integrator contained within a Field Programmable Gate Array ("Sig Proc FPGA"). Also contained in this FPGA is gain and offset adjustment of the digitized AM input signal and the means to apply this signal to both the input and output of the integrator. The integrator is broken down into a comparator, multiplier, and accumulator. Multiplying the difference between the desired RF voltage ("Power Set") and instantaneous RF voltage by a selected "integrator gain number" allows the speed of accumulation to be controlled, thus allowing the entire control loop gain to be set for the quickest stable operation.

Preceding the integrator is the 12-bit RF Leveling A/D and lookup table ("Linearization RAM) that allows it to see a linear RF voltage scale, despite the nonlinear transfer characteristics of the diode envelope detectors in the RF amplifier subsystems. Preceding the A/D are two selectable gain controlled amplifier subsystems—one each for CW and Pulse operation. Their principal use is to convert the widely variable detected and pre-amplified signals to the +1 Volt to +4 Volt scale needed by the A/D.

Following the integrator accumulator and feed-forward Linear AM modulator multiplier (inside the Sig Proc FPGA) is another lookup table. This "De-linearization" RAM permits linear changes of the integrator output to result in linear changes of 12000A RF output voltage, despite the grossly nonlinear (mainly logarithmic) transfer characteristics of the gain control elements located in the various RF amplifier subsystems.

The digital control signal is now converted to an analog signal and then gain-and-offset adjusted in separate selectable circuits to accommodate the peculiar gain control curves of each of the three RF amplifier subsystems. The RF output level vs D/A converter count value at various frequencies is measured and stored during the characterization process.

4.10.2 CW Operation

The selector switch in the particular RF amplifier subsystem selects the "carrier" preamplifier. (This preamplifier is also used for Linear AM and calibration of Logarithmic AM.) This preamplifier is optimized for voltage offset stability and low noise. It includes a 20 K-Ohm termination for the detector to maximize its temperature stability and output level. Its DC to 1 MHz bandwidth is needed only for Linear AM; only DC to 30 KHz is needed for CW.

At the ALC Board input is a switch (not shown) that selects one of the three RF amplifier subsystems or an external detector. The RF leveling A/D converter samples its input data at a 10 MHz rate (but only every other sample is used). The 1 MHz low pass filter prevents aliasing of the higher frequency components.

The DC signal level at the ALC Board input varies from several Volts to several millivolts as the 12000A RF output varies from +20 dBm to –20 dBm. In order to maintain an adequate count value per dB set point resolution for small signals without overloading the A/D converter when the signal is large, the gain is adjusted in seven steps over a 250:1 range by the Variable Gain amplifier. The Gain/Offset amplifier is used mainly to shift the voltage scale from 0-3 Volts to 1-4 Volts, needed by the A/D converter input.

The buffer amplifier includes insertion of an offset voltage by the Zeroing D/A converter. During each 12000A boot-up process, the correct D/A converter value is determined for each gain setting; so that the zero-signal A/D count level is consistent over time, regardless of long term offset drift in the diode detector/carrier preamplifier or elsewhere.

Inside the Sig Proc FPGA, the feed-forward Linear AM modulator and power set multipliers are locked to multiply by one. The integrator accumulator counts up or down depending upon whether the "Power" Set input level is higher or lower than the instantaneous signal level delivered by the A/D and Linearization RAM. The speed of counting is directly proportional to the magnitude of this disparity and Integrator Gain Number.

4.10.3 Linear AM Operation

Most of the sophistication present in the ALC result from the requirement to deliver accurate carrier level regulation and low distortion, high modulation index (upward and downward) Linear AM at all modulating frequencies between DC and 150 KHz. Three significant architectural features were employed to meet these requirements:

1. The servo control element sees a linear (voltage) control loop in both the feedback and feedforward directions. This is accomplished despite the nonlinear transfer characteristics of the detector and gain control elements by the two lookup tables. Therefore, the instantaneous open loop RF voltage envelope is proportional to the count value entering the integrator comparator, and any error in the RF voltage is proportional to comparator output and thence the rate of accumulator slew. Finally, the instantaneous open loop RF voltage envelope is also proportional to the accumulator count value. These design measures combine to provide for low distortion closed loop Linear AM at all modulation levels and all RF carrier levels.

   The basic Linear AM process is similar to that found in other closed loop level control systems. The number representing the desired or demanded RF output voltage feeds the comparator reference input through a multiplier, and the other multiplier input receives the modulating signal input. When this modulating signal is at zero level, its multiplier is unity, causing the envelope output voltage to have its unmodulated, carrier level set value. As the modulating voltage varies from its maximum allowable value to its minimum allowable value, the multiplier input value goes from 2 to 0, and the RF voltage goes from twice the carrier level to zero—so demanded by the comparator reference input.

2. Closed loop modulation control is limited, however, to about 10 KHz, commensurate with the highest speed at which the servo loop can apply small phase margin corrections. In order to handle the full spectrum of modulating frequencies, all modulation spectral content that cannot be handled by the loop bandwidth must be injected (fed forward) after the integrator. In the 12000A, the entire modulating spectrum multiplies the carrier level (digital) value, analogous to classical analog high level AM of a Class C amplifier, wherein the voltage that is proportional to RF output power is multiplied by the modulating voltage. There are no crossover elements (except for the servo loop itself) to separate the portion of the spectrum that can and cannot be controlled by the loop. The composite subsystem amplitude and phase response is completely flat up to 150 KHz; there is no indication of where the modulation is inside or outside the loop. The “Time Delay” allows the feedforward modulation information to go around the loop and reach the integrator comparator at the same time as the feedback component.

3. When the RF signal is modulated at a high level with a 150 KHz sine wave, the waveform at the envelope detector output contains the fundamental and several harmonics up to 750 KHz, principally at 300 KHz and 600 KHz. If only the fundamental is considered (harmonics suppressed), the 150 KHz sine wave will have an average value that depends upon the degree of modulation, causing the carrier level adjustment to become increasingly inaccurate as the modulation index is increased. Therefore, a 1 MHz bandpass is maintained in all analog and digital circuitry at least through Linearization RAM lookup table. Similarly, all circuitry between the De-linearization RAM through the gain control elements must have a 1 MHz bandpass to contain the important harmonics commensurate with an exponentiated 150 KHz sine wave.

Before being fed to the Sig Proc FPGA, the AM-intended signal passes through a gain and offset adjustment that maps a –1V-+1V scale to a 0V-5V scale. It then passes through a 150 KHz anti-aliasing filter and the AM (12-bit) A/D converter.

4.10.4 Logarithmic ("Scan") AM Operation

Log AM uses the same 12000A input connector and A/D converter, but the input scale is 0V to 6V (for 0 to 60 dB reduction from the fiduciary CW set point level), and a 1MHz anti-aliasing filter is needed. The 12000A Scan Menu allows other scales than 10 dB/Volt, and these are obtained by the Variable Gain adjustment block in the Sig Proc FPGA.

Log AM operation is carried out totally open loop (unlike its calibration, which is done closed loop by the CW infrastructure). Open loop operation is needed for two reasons:

1. The speed is too high for the 10 KHz feedback control system; a 50 dB change over a μsecond or less is guaranteed.

2. A 60 dB range below the fiduciary level is guaranteed. Owing to the high speed involved, the 10 dB/step electromechanical attenuator is much too slow during operation (but is used to set the fiduciary level). More than 40 dB below the fiduciary level, there is insufficient feedback signal level coming from the detector to operate the servo loop.

Although the Figure shows a single gain control point in the RF amplifier subsystem, there are actually two cascaded gain control points, each controlled separately or in unison by the ALC. Each gain control point has a range of at least 40 dB. Only one of them is used in CW, Linear AM, and Pulse Modulation, while the other is maintained at minimum attenuation. In Log AM, both are needed to obtain the 60 dB or more range.

During factory Log AM (Scan) Characterization (which can be repeated periodically in the field), open loop measurements are made using an external power meter. A D/A converter count vs power output scale is obtained for many frequencies over the 12000A frequency range.

The shape of this scale is stable, but the gain control elements (and other aspects of the RF amplifier subsystem and RF source) offset-drifts with temperature and time. Therefore each time the AM ON switch is actuated, the system first switches briefly to CW, and a closed loop single point calibration is performed at the fiduciary level. This offset calibration is performed each time the 12000A carrier frequency and/or fiduciary power level is changed.

4.10.5 Pulse Modulation (PM) Operation

The RF output level for PM (Square Wave Modulation) is entirely under closed loop control, but there are several differences in the way this control must be effected.

The pulse timing (when the RF output is on or off) is independent of the method used to control the output level. The digital "demand" pulses from the external source or optional internal Modulation Generator directly operate the set of RF on/off switches in the RF amplifier subsystem.

In CW and Linear AM operation, the 12000A is delivering RF at all times; so the feedback signal is automatically always present at the envelope detector, and the RF Leveling A/D converter input. For PM however, a feedback signal is present only while the RF pulse is on, which for very short pulses (such as 50 nSec) can be an extremely short percentage of time. Therefore, special circuitry is needed to capture detected pulse level and hold it a long enough time for the control system to use it and until the next pulse arrives (with its new level information). The PM detected signal also differs from CW and Linear AM in that the narrow pulses and rapid rise time represent a much wider bandwidth than 10 KHz to 1 MHz—at least 20 MHz, which affects both the amplifiers and even the envelope detector itself.

In the respective RF amplifier subsystem, a broadband, higher gain preamplifier is used. Its input terminates the diode detector with only 1 K-Ohm, needed in order for the diode to respond rapidly enough. Such low terminating impedance degrades both the detected signal level and temperature stability.

The ALC board includes a broadband variable gain amplifier and the necessary circuitry to capture the detected pulse amplitude. It is not necessary to determine the detected pulse's presence directly; as its presence is directly correlated with the demand pulse, albeit with a delay. This delay cannot be controlled in Production with sufficient precision to capture the level in a Sample and Hold circuit by itself; so preceding it is a peak detector, which—unlike the Sample and Hold—requires no control signal to capture the level. (The peak detector control line shown in the Figure is used only to reset it.)

The Pulse Level Acquisition Controller FPGA receives the Demand Pulses and passes them immediately to the RF on/off switches. It uses the timing of these Pulses as well as the A/D converter sample clock to operate the sample and hold circuit and peak detector Reset controls. For all pulses longer than several hundred nanoseconds, the pulse height is re-read every 200 nanoseconds.

Each time the Pulse-Modulation-On switch is operated, or the 12000A frequency or RF output level is changed, before the pulse pattern is admitted, the system is switched briefly to CW operation and the D/A converter count noted. Then the system is switched (back) to the Pulse chain, and its zeroing is adjusted until the same D/A converter count is obtained. Thus, the long-term accuracy of CW is obtained for PM.

4.10.6 Digital Communication, Controls & Calculations

In addition to the signal chain components (A/D, D/A, Sig Proc FPGA, and lookup table RAMs) and Detected Pulse Acquisition Timing FPGA, the following major digital components are present on the ALC Board:

The Digital Signal Processor (DSP, U104) receives demanded level data from the Host CPU. It also receives polynomial coefficients from the CPU and expands them to calculate the lookup tables, which it sends to the Linearization and De-linearization RAMs via the Sign Proc FPGA over the lower 16 lines of its 24 line parallel bus. It coordinates all activities on the board with the help of its intra-board serial bus I/O system. This serial bus services the System and I/O CPLDs, the Detected Pulse Acquisition Control FPGA, and the three auxiliary serial DACs.

The system CPLD (U202) operates all the chip selects. It also operates the twelve switches that control the main D/A converter drive to the various RF amplifier subsystem gain control elements and the Load command for the three serial DACs. The data and timing for these functions come from the serial bus. Finally, along with the DSP, this CPLD is connected directly to the Peripheral Bus; so that it can provide its hardware support—including boot support.

The "I/O" CPLD (U203) contains the latches that operate all the analog switches except for those following the D/A converter, including gain setting, detector source selection, modulation type/source selection, CW/PM selection, and filter selection. It also drives the DSP Reset. The control and data come from the serial bus.

In addition to the servo integrator and signal processing functions, the Sig Proc FPGA serves as the distribution device for all parallel data and address lines used by the Linearization and De-linearization RAMs. It does this in order to intersperse loading new tables in one memory segment at the same time (alternate clock cycles) while using a previously loaded segment for leveling.

All communication between the 12000A Host CPU (A11) and ALC Board is provided by the Peripheral Bus. Dedicated inputs include Read, Write, and Reset controls, Sweep Synchronization, Marker, and Sweep Start Timing, Strobe, and RF ON. Dedicated outputs include Ready to Level, Leveling Complete, and Interrupt Request. There is also a bi-directional 8-bit data bus.

5

Replaceable Parts

5.1 Series 12000A Replaceable Parts

Table 5-1: Series 12000A Replaceable Parts List

P/N	Item Description
30572	A1 Synthesizer PCA
31288	A1-A1 Synthesizer Front End assembly
31542	A1-A2 Track Filter assembly
30580	A3 ALC PCA
30584	A4 Distribution PCA
30570	A6/.01-20GHz Output module
30577	A7/8-20GHz Multiplier module
30596	A8 Downconverter assembly
31632	A9 Power Supply assembly
30751	A10 keyboard PCA
30755	A11 Main Processor PCA
30913	A15 Time Base PCA
30771	A16 Modulation Generator PCA
31740	A17 Interface PCA
31891	A18 Power Supply Filter PCA
31807	Upper rear mount feet
31917	Lower rear mount feet
30727	Handle
MPBO-02001	Option 26 Attenuator
IMCO-00002	320 x 240 LCD Module
KGRO-15025	1.50" diameter knob with spinner
FSAC-00200	2A SB Fuse, 3AG
HFBI-00014	Mount bail
HFFL-63202	Left front feet
HFFR-63202	Right front feet
BHGO-05000	Fan finger guard
BHSO-05000	Fan screen
BDOO-05012	12VDC 4-5/8" fan
JRAB-00200	SMA Bulkhead connector
JRDF-00004	BNC panel mount connector

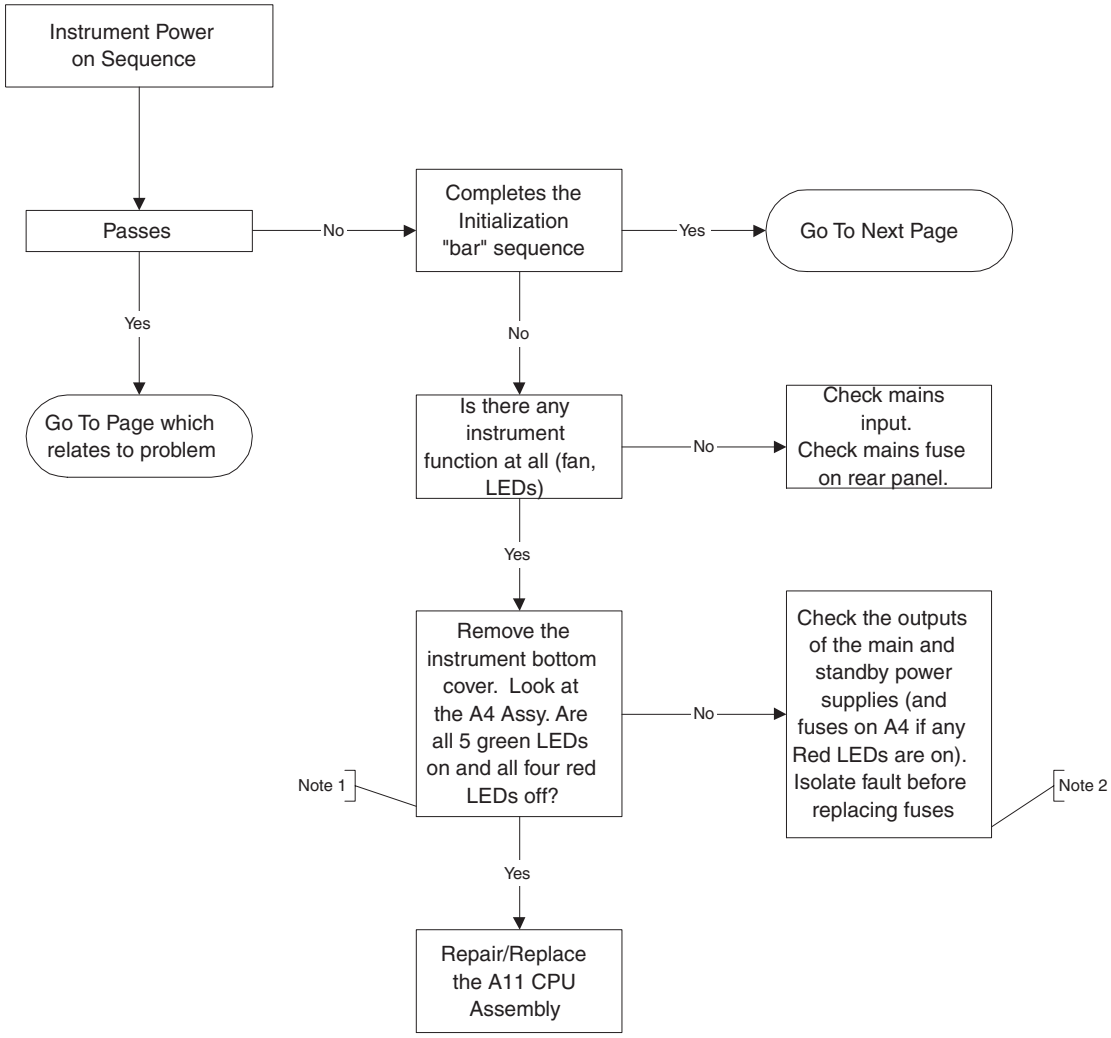
6

Troubleshooting

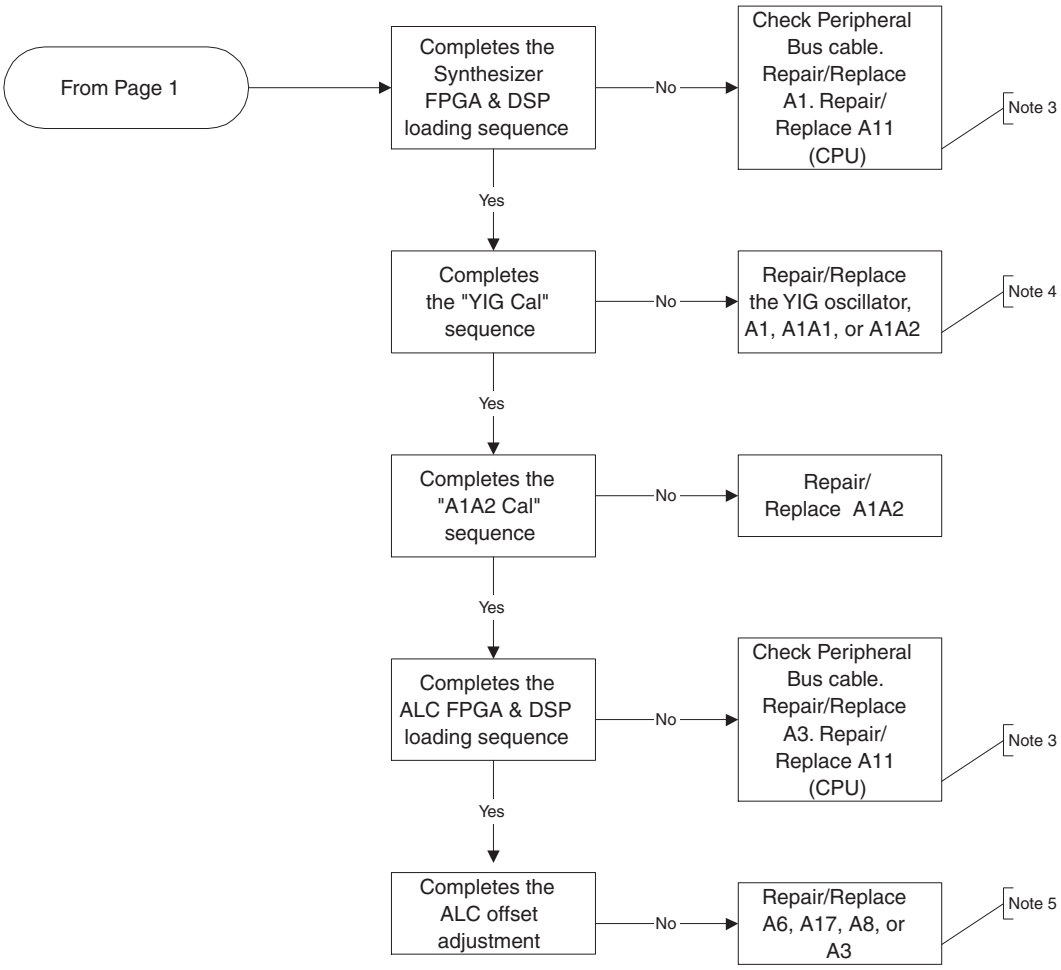
6.1 Series 12000A Fault Isolation Trees

Troubleshooting	Model	
	124XXA	125XXA/ 127XXA
6.1.1 - Power on Sequence Fault Isolation	√	√
6.1.2 - Power on Sequence Fault Isolation Continued	√	√
6.1.3 - CW Operation (Frequency)	√	√
6.1.4 - CW Operation (Frequency) Continued	√	√
6.1.5 - CW Level	√ (Limitations Apply)	√
6.1.5 - Modulation Modes (Series 125XXA/127XXA Only)	**N/A**	√
6.1.6 - Modulation Modes Continued (Series 125XXA/127XXA Only)	**N/A**	√

6.1.1 Power On Sequence Fault Isolation



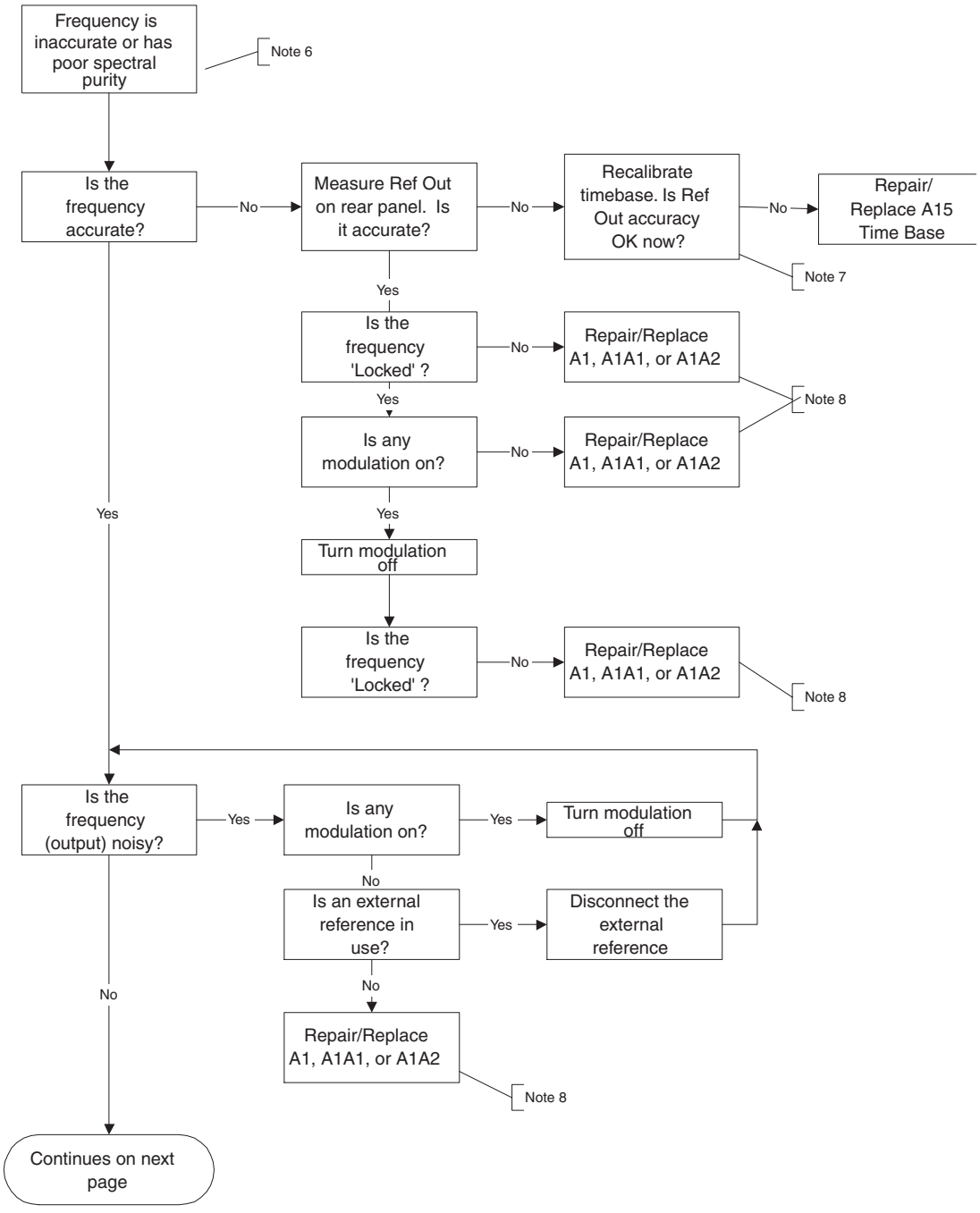
6.1.2 Power On Sequence Fault Isolation Continued



Modulation applies to Series 125XXA/127XXA Models Only

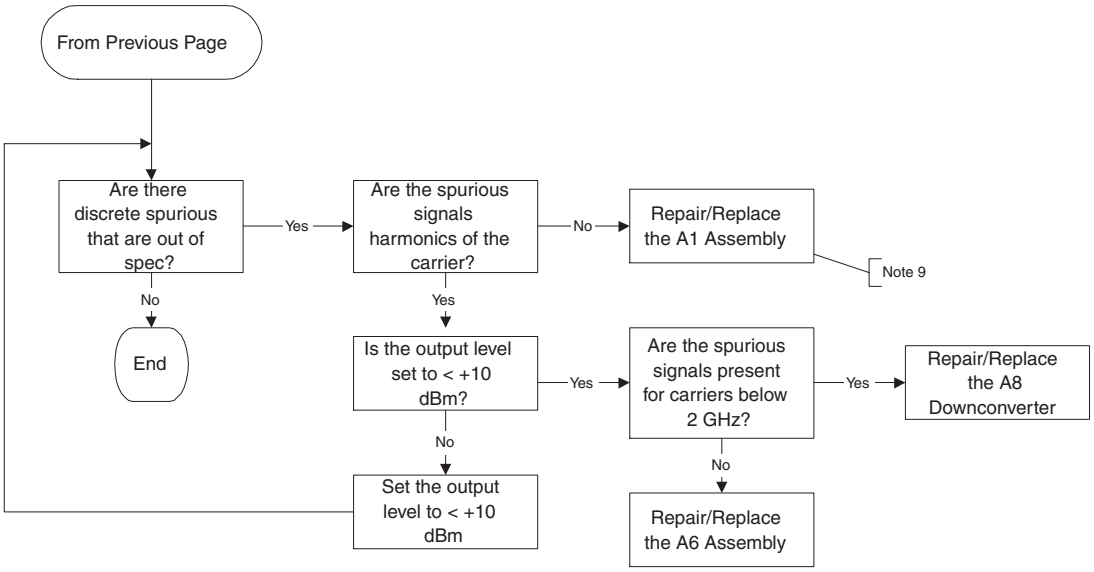
6.1.3 CW Operation (Frequency)

Fault Isolation Tree--CW Operation (Frequency)



6.1.4 CW Operation (Frequency) Continued

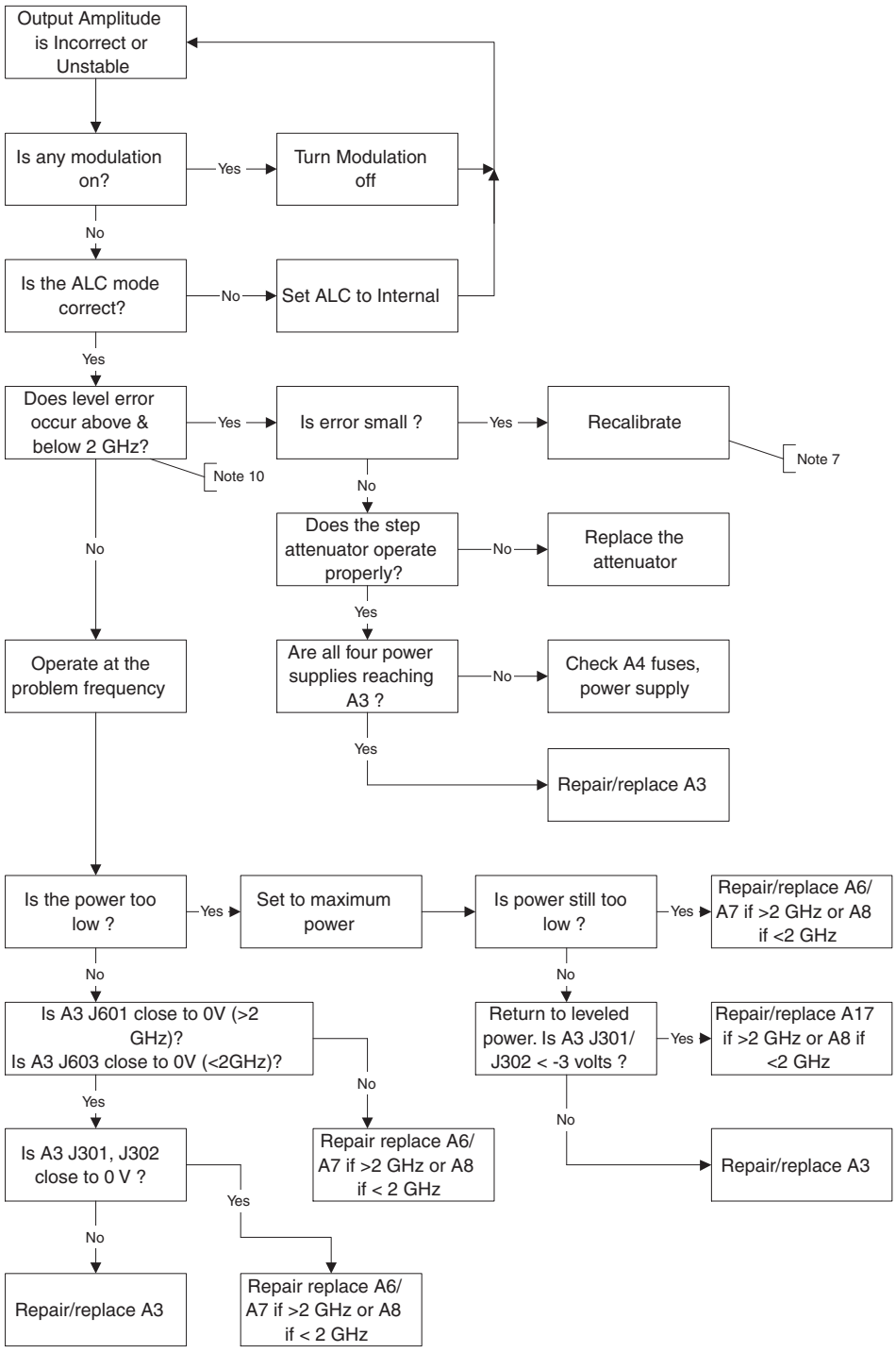
CW Operation (Frequency) Continued



Modulation modes apply to Series 125XXA/127XXA Models Only

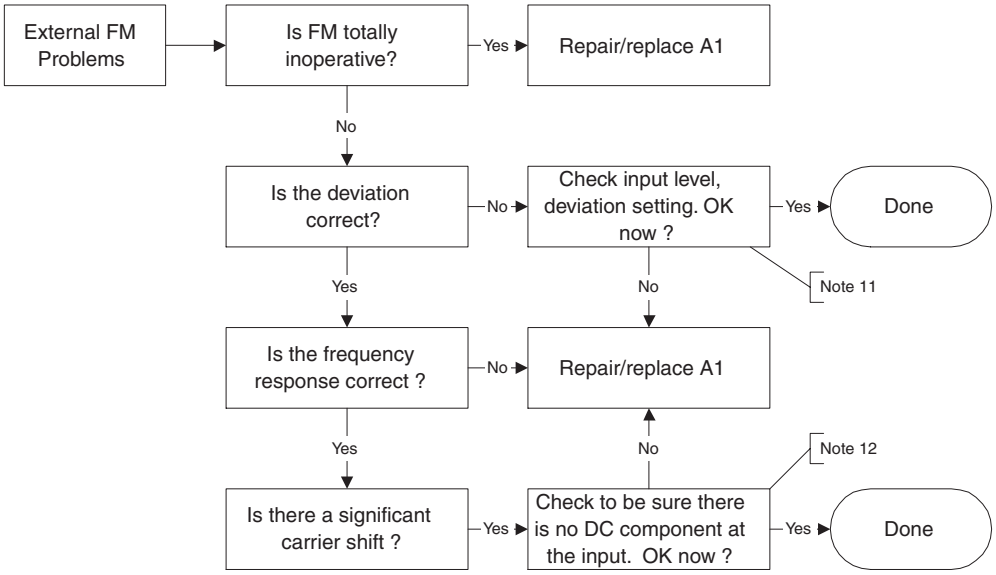
6.1.5 CW Level

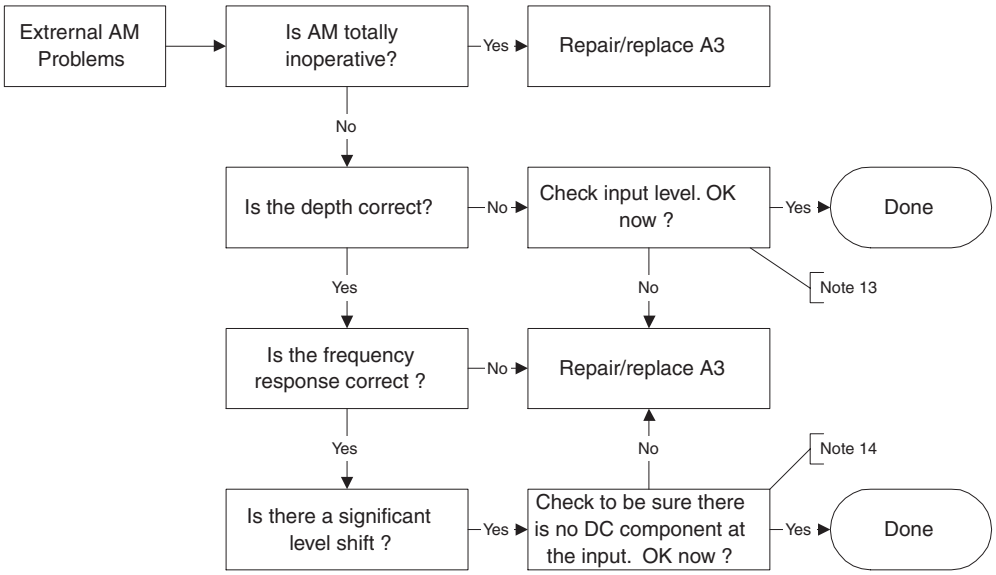
Fault Isolation Tree--CW Operation (Level)



6.1.6 **Modulation Modes** (Series 125XXA/127XXA Only)

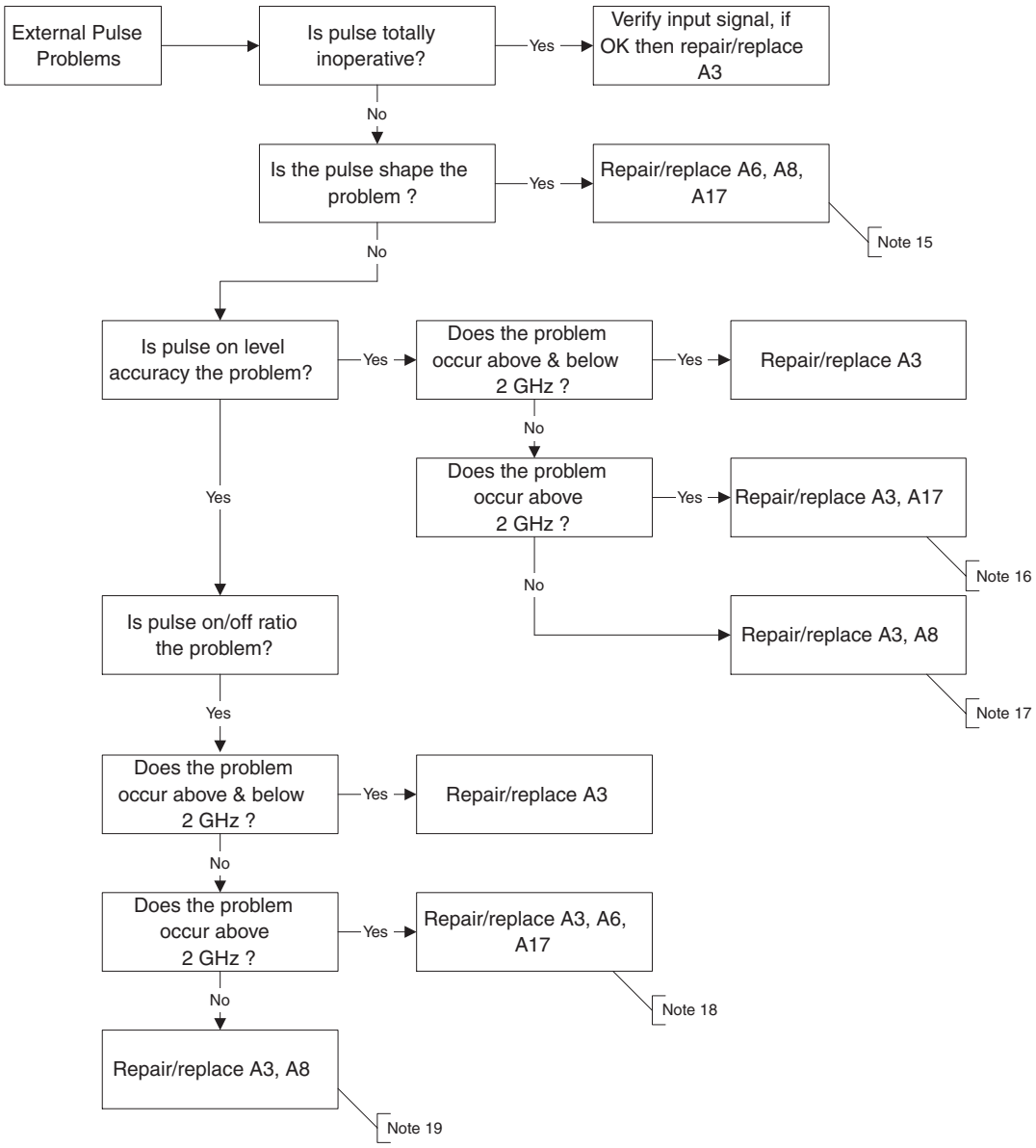
Fault Isolation Tree--Modulation Modes





6.1.7 **Modulation Modes Continued** (Series 125XXA/127XXA Only)

Modulation Modes (Continued)



Notes

Note #	Note Description for Series12000A Fault Isolation Trees	Model	
		124XXA	125XXA/ 127XXA
1	The referenced LEDs are located on the edge of the A4 Distribution PC board away from the power supply assembly. Green LEDs indicate that the monitored power supply is on (they do not indicate that the supply is within tolerance). Monitors are provided for the +12 standby supply and the ± 6 and ± 12 volt main supplies. Red LEDs indicate that the corresponding power supply fuse is open. Monitors are provided for the ± 6 and ± 12 volt main supplies.	√	√
2	To isolate the power supply loads, unplug the 9 pin connectors which connect the power cables from the A4 Distribution board to the other PC assemblies. It will be necessary to remove the A1 Synthesizer assembly to access these connectors.	√	√
3	The Peripheral Bus Cable is a 60 wire ribbon cable that connects the A4, A1, A11, A3 and A16 (if installed). It is recommended that this cable be verified first before replacing any of the PC assemblies.	√	√
4	The "YIG Cal" sequence sets the YIG to 4.5 and 7.5 GHz and adjusts the tuning current to center the PLL. A failure at this point can be further isolated by removing the Instrument bottom cover then removing the coaxial cable from A1A1 J402. *This cable goes to the A6 Microwave Module. It is a .085 Semiflex about 4" long.* Connect a spectrum analyzer to J402. If a signal is present at about +10 dBm, then the YIG is working. If not, measure the voltage on the end of R724 closest to the board edge. It should be *approximately* 0.1 volts/GHz. If the voltage is outside the range of 0.4 to 0.85 volts, the oscillator may not operate and the A1 board should be serviced. A problem in A1A1 or A1A2 can also cause the YIG Cal to fail.	√	√
5	The ALC Offset calibration requires that the detectors in A6 and A8 (if installed) be functioning as well as the circuitry on A17 and A8 that amplifies the detector signals. If possible, verify the signal levels from A17 and/or A8 before replacing assemblies.	√	√
6	This problem includes frequency errors, phase noise problems, and both harmonically and non-harmonically related spurious signals. It is appropriate to determine over what range of carrier frequencies and output amplitude levels the problem exists. This will often provide additional information to help isolate the cause.	√	√
7	See the calibration section of this publication for the procedure.	√	√
8	If available, exchange the A1A1/A1A2 assembly with a known good set and see if this fixes the problem. If so, determine which of the two is at fault. If not, replace the main A1 assembly. No re-calibration is needed if just A1A1 and/or A1A2 is replaced. FM re-calibration is needed if A1 is replaced (Reference to FM re-calibration does not apply to Series 124XXA Models).	√ (Limitations Apply)	√
9	Although the A1 assembly may be the point of entry for the spurious signals, poor connections on ground or power supply leads should be checked. The power supply itself may be producing ripple outside the specified levels. Also check if the spurious signal levels are affected by the amplitude setting. If so, the A3 ALC assembly or one of the RF modules may be at fault. Try looking at the output of A1A1 at J402 with a spectrum analyzer and see if the spur is still present.	√	√
10	A 'Yes' answer here should be used only if the level is neither at minimum nor maximum.	√	√
11	Check the input level at the FM input connector (the front and rear ones are tied together). Instrument calibration assumes that this level is 2 V_{P-P}. Check the setting for the deviation by pressing the FM button. Note that since the instrument uses frequency multiplication and division, the maximum deviation is reduced as the frequency is reduced. If, for example, you set a deviation in narrow mode of 1 MHz at 4 GHz and then change the frequency to 1 GHz, the deviation will automatically change to 250 kHz.	N/A	√
12	The FM Narrow mode is DC coupled. Any DC component on the input signal will shift the carrier at the same scaling as the deviation. If, for example, the deviation is set to 1 MHz and there is 10 mV of offset, there will be 10 kHz of carrier shift.	N/A	√
13	Check the input level at the AM input connector (the front and rear ones are tied together). Instrument calibration assumes that this level is 2 V_{P-P}. Check the setting for the depth by pressing the AM button.	N/A	√
14	The AM mode is DC coupled. Any DC component on the input signal will shift the carrier level as would the peak of an AC component.	N/A	√
15	If the pulse shape (rise/fall time; overshoot, etc) is a problem below 2 GHz, then replace the A8 downconverter (all pulse shape determining circuits are on this assembly). If the problem is above 2 GHz the cause could be on either the A17 board (driver) or the A6 assembly (modulator).	N/A	√
16	Pulse level accuracy (when the RF is on) problems which occur above 2 GHz would most likely be caused by a fault on a the A3 assembly. It is possible, however, that a defect on the A17 assembly could cause a problem since the detector buffer amplifier is located here.	N/A	√
17	Pulse level accuracy (when the RF is on) problems which occur below 2 GHz would most likely be caused by a fault on a the A3 assembly. It is possible, however, that a defect on the A8 assembly could cause a problem since the detector buffer amplifier is located here.	N/A	√
18	Pulse on/of ratio problems could be caused by the amplifiers on the A3 assembly, the driver amplifiers on A17 or by the RF module A6.	N/A	√
19	Pulse on/of ratio problems could be caused by the amplifiers on the A3 assembly or by the driver amplifiers and modulators on A8.	N/A	√

6.2 Series 12000A Disassembly/Assembly Instructions

Series 12000A Disassembly/Assembly Instructions	Model	
	124XXA	125XXA/ 127XXA
6.2.1 - Top & Bottom Covers	√	√
6.2.2 - Side Covers	√	√
6.2.3 - Rear Panel	√	√
6.2.4 - A1 Synthesizer	√	√
6.2.5 - A15 Timebase	√	√
6.2.6 - A4 Distribution Board	√	√
6.2.7 - A3 Automatic Level (ALC) Board	√ (Limitations Apply)	√
6.2.8 - A16 Modulation Generator Board	**N/A**	√
6.2.9 - A11 CPU Board	√	√
6.2.10 - A8 Downconverter	√	√
6.2.11 - A6/A7/A17 Microwave Assembly Board	√	√

The following instructions are provided to assist in the removal and replacement of the various subassemblies in the 12000A.

6.2.1 Top & Bottom Covers

1. Unplug the line cord from the instrument.
2. Remove the eight screws on each cover. Four at the front, four at the rear.
3. Lift the cover off. Note that the cover has a 'lip' on each side. Lift the cover from the front or rear edge.
4. When re-installing the covers, be sure to use the longer #4 screws at the corners.

6.2.2 Side Covers

1. Remove the top and the bottom covers (1).
2. Remove the four #10 flat head screws located at the front and rear edges. The front screws also mount the handles.
3. Remove the four #4 flat head screws located on the top and bottom edges of the cover.
4. Lift the cover off.
5. When replacing the side covers see the following notes:
    a. For instruments without provision for rack slides, the side covers are identical. It is only necessary to be sure that the edge of the cover with the bent lip is at the top of the instrument.
    b. The side covers for instruments that accept rack slides are different. When installed, the ventilation holes go toward the top of the instrument. There are three #10 press nuts to mount the slides. The pair with the closer spacing goes toward the rear of the instrument.

6.2.3 Rear Panel

1. Unplug the instrument line cord.
2. Remove the top and bottom covers (1).
3. Remove the two side covers (2).
4. If the instrument has rear panel RF output, disconnect the coaxial cable from the rear panel output connector.
5. Locate the two coaxial cables running from the rear panel "Ref In" and "Ref Out" connectors to the A15 Time Base Assembly. Release the connector on the A15 by pressing on the lock release while gently pulling on the connector. If necessary, remove the cables from any plastic clips that hold the cables to the chassis.
6. Remove the eight #10 flat head screws located at the four corners of the rear panel casting.
7. Remove the five #6 pan head screws on the rear panel. Four of these are located near the power entry connector, the other one is in the BNC connector area.
8. Carefully pull the panel loose from the four side rails. **Note that the panel will only have sufficient cable slack to move about 2 inches!**
9. To re-install the panel, carefully push the assembly onto the four side rails. Be sure no cables are pinched.
10. Fasten the five #6 pan head screws, then the eight #10 flat head screws. **Be sure to put the #10 screws in the 'outside' holes (closest to the covers).**
11. Re-connect the cable to the A15 board and, if necessary, the RF output.

6.2.4 A1 Synthesizer

This assembly must be removed in a static controlled environment.

1. Remove the bottom cover (1).

2. Disconnect the three coaxial cables from the A1A1 sub-assembly.

3. Disconnect the two power connectors (P401, P801), the YIG (P701) and FET (P702) connectors, and the peripheral buss connector (P101). When removing the peripheral buss connector, press the locking ears outward to release the connector.

4. Disconnect the two blue 10 MHz coax cables (J101, J102). When removing these use the proper removal tool or pull straight up with small tweezers held parallel to the board.

5. Disconnect the twisted pair cable connector at P103. Press the lock release on the cable connector to release.

6. Remove the seven #6 screws around the perimeter of the board. Note that one of these is accessible through the corner hole in the A1A2 assembly.

7. Carefully lift the board out of the instrument.

    a. To remove the A1A1/A1A2 assemblies:

        1). Disconnect the blue cable at J501 on the A1 synthesizer board.

        2). Remove the four #4 screws closest to the four corners of the assembly. These screws are about 1.5 inches long.

        3). **Carefully** lift both assemblies, as a unit. There is a multi-pin connector on the A1A2 which goes through a socket on the A1A1 and then into another socket on the A1 synthesizer board. It may be necessary to 'rock' the assembly slightly to ease removal.

        4). If the A1A1 and A1A2 assemblies need to be separated from each other, carefully pry them apart with a pocket knife blade, or equivalent.

        5). When replacing these assemblies, first plug A1A2 into A1A1, then plug the pair into A1, then fasten with the four #4 screws.

8. To replace the A1 assembly, reverse the above procedure. **Be certain that all connectors are properly aligned!** The 10 MHz (blue) cables are connected by pressing straight down over their sockets.

9. When tightening the three coaxial cables on A1A1, observe proper torque procedures.

6.2.5 A15 Timebase

This assembly must be removed in a static controlled environment.

1. Remove the bottom cover (1).
2. Remove the A1 synthesizer assembly (4).
3. Disconnect the 10 MHz coax cables (blue cables). When removing these use the proper removal tool or pull straight up with small tweezers held parallel to the board.
4. Disconnect the black cable connector. Press the lock release on the cable connector to release.
5. Disconnect the ribbon cable.
6. Using a 'nut driver' or similar tool, unscrew the four mounting fasteners. These are threaded onto studs on the chassis and pass through rubber vibration isolating grommets. They are often quite tight.
7. To replace the A15 assembly, reverse the above procedure. **Be certain that all connectors are properly aligned! Be certain that the 10 MHz cables are connected to the correct sockets!** The 10 MHz (blue) cables are connected by pressing straight down over their sockets.

6.2.6 A4 Distribution Board

This assembly must be removed in a static controlled environment.

1. Remove the bottom cover (1).
2. Remove the A1 Synthesizer assembly (4).
3. Disconnect any power connectors (P403-P410), the main power supply input connector (P401), the fan power connector (P302), and the standby power connector (P402).
4. Disconnect the peripheral buss connector (P101) and the module cables (P102 and P201). When removing these connectors, press the locking ears outward to release the connector.
5. Disconnect the cables to the A15 and A11 boards (P305 and P301).
6. Disconnect the connector on the wire going to the YIG oscillator. This connector is in line with the wire.
7. Disconnect the (optional) step attenuator ribbon cable at P303 and/or the (optional) cable to the high power assembly at P304.
8. Remove the five spacers (that are used to mount the A 1 assembly).
9. Lift the A4 assembly out of the instrument. Note that there is a locating pin on one corner of the board.
10. To re-install the assembly reverse the above procedure.
11. First align the hole in the corner of the board with the locating pin. Press the board onto the pin. Now install the five spacers.
12. Re-connect all the cables. **Be certain that the connectors are properly mated and aligned.**

6.2.7 A3 Automatic Level (ALC) Board

This assembly must be removed in a static controlled environment.

1. Remove the top cover (1).

2. Disconnect the two power connectors (P701, P702) and the peripheral buss connector (P101). When removing the peripheral buss connector, press the locking ear outward to release the connector.

3. Disconnect all of the blue cables. When removing these use the proper removal tool or pull straight up with small tweezers held parallel to the board.

4. Disconnect the twister pair/coaxial cable connector at P301. Press the lock release on the cable connector to release.

5. Remove the nine #6 screws around the perimeter of the board and the one #6 screw in the center.

6. Carefully lift the board out of the instrument.

7. To replace the A3 assembly, reverse the above procedure. **Be certain that all connectors reproperly aligned!** The blue cables are connected by pressing straight down over their sockets.

6.2.8 A16 Modulation Generator Board (Series 125XXA/127XXA Only)

This assembly must be removed in a static controlled environment.

1. Remove the top cover (1).
2. Disconnect the power connector (P400) and the peripheral buss connector (P100). When removing the peripheral buss connector, press the locking ears outward to release the connector.
3. Disconnect the blue 10 MHz cable. When removing this cable use the proper removal tool to pull straight up with small tweezers held parallel to the board.
4. Disconnect the twister pair connector at P101.
5. Disconnect the remaining twisted pair connectors. Press the lock release on the cable connector to release.
6. Remove the six #6 screws around the perimeter of the board and lift out the assembly.
7. To replace the A16 assembly, reverse the above procedure. **Be certain that all connectors are properly aligned!** The blue cable is connected by pressing straight down over its socket.

6.2.9 A11 CPU Board

This assembly must be removed in a static controlled environment.

1. Remove the top cover (1).
2. Remove the A3 ALC assembly (7).
3. Remove the shield plate by removing the nine #6 screws (with their lock and flat washers).
4. Disconnect the main power connector (P702), the backlight power connector (P503), and the peripheral buss connector (P402). When removing the peripheral buss connector, press the locking ears outward to release the connector.
5. Disconnect the blue 10 MHz cable (J101). When removing this cable use the proper removal tool or pull straight up with small tweezers held parallel to the board.
6. Disconnect the LCD flex cable (J501). When removing this cable, pull straight out, parallel to the board.
7. Disconnect the twisted pair connector (J601). Press the lock release on the cable connector to release.
8. Disconnect the remaining four ribbon cables.

9. Disconnect the back-up battery (P201).

WARNING

Disconnecting the battery will clear the non-volatile memory.

If the A11 assembly is to be re-used in this instrument, do not disconnect the battery, unfasten it from the chassis instead.

10. Remove the five #6 screws and lift the assembly out of the instrument.

11. To replace the A11 assembly, reverse the above procedure. **Be certain that all connectors are properly aligned!**

12. The blue cable is connected by pressing straight down over its socket.

    a. When re-connecting the LCD flex cable, grasp the cable near the end and press firmly and carefully into the socket. The cable should have the blue plastic strip toward the PC board (i.e. not visible after the cable is installed).

6.2.10 A8 Downconverter

This assembly must be removed in a static controlled environment.

1. Remove the top cover (1).

2. Remove the A16 Internal Modulation Generator assembly (8), if installed.

3. Remove the two white coaxial cables. One is located at the front edge of the assembly, the other on the inside edge near the peripheral bus cable.

4. Remove the five blue coaxial cables. When removing these use the proper removal tool or pull straight up with small tweezers held parallel to the board.

5. Remove the power/control ribbon cable. When removing this cable, press the locking ears outward to release the connector.

6. Remove the seven #6 screws around the perimeter (If the A16 board was installed, some of the screws are replaced with spacers, remove these) and lift the assembly out of the instrument.

7. To replace the A8 assembly, reverse the above procedure. **Be certain that all connectors are properly aligned!**

    a. The blue cables are connected by pressing straight down over their sockets.

6.2.11 A6/A7/A17 Microwave Assembly

This assembly must be removed in a static controlled environment.

1. Remove the bottom cover (1).
2. Disconnect the RF input on the front of the assembly (Semi-flex) which comes from the A1 synthesizer assembly.
3. Disconnect the RF input on the rear of the assembly (white coax) which comes from the A8 downconverter (if installed).
4. Disconnect the RF output on the rear of the assembly (Semi-flex).
5. Disconnect the ribbon cable from P1. When removing this cable, press the locking ears outward to release the connector.
6. Disconnect the five blue coaxial cables. When removing these use the proper removal tool or pull straight up with small tweezers held parallel to the board.
7. Remove the four slotted head #6 screws from the top module (A7), if it is installed. If not, these screws are phillips head and are on the A17 PC assembly.
8. Remove the two #6 screws from the back end of the A17 PC assembly and lift the entire assembly out of the instrument.
9. To replace the A8 assembly, reverse the above procedure. **Be certain that all connectors are properly aligned!**
    a. The blue cables are connected by pressing straight down over their sockets.
10. When tightening the three coaxial cables observe proper torque procedures.
11. To install the 12000A calibration program simply copy all the files in the 12000A Calibration directory to a directory on your PC.

6.3 Series 12000A CPU Initialization Error Messages

Series 12000A CPU Initialization Error Messages	Model	
	124XXA	125XXA/ 127XXA
	√	√

☛ ***NOTE:*** *The following error messages are listed in the order of (potential) occurrence.*

1. **"Synth boot load timeout"**. Boot code has been transmitted to the Synthesizer, but after 650 microseconds, no response has been received.

2. **"Synth boot load err"**. Boot code has been transmitted to the Synthesizer, and the Synthesizer has responded with an error message. The contents of the Synthesizer DSP HIP status and data registers are displayed.

3. **"ALC boot load timeout"**. Boot code has been transmitted to the ALC board, but after 650 microseconds, no response has been received.

4. **"ALC boot load error"**. Boot code has been transmitted to the ALC board, and the ALC board has responded with an error message. The contents of the ALC board DSP HIP status and data registers are displayed.

5. **"Synth FPGA RdBck timeout"**. A byte of the Synthesizer FPGA program file has been transmitted to the Synthesizer, but after 65 microseconds, no response has been received.

6. **"Synth FPGA RdBck error"**. A byte of the Synthesizer FPGA program file has been transmitted to the Synthesizer, and the Synthesizer has responded with an error message and/or a non-matching data byte rather than an OP COMPLETE message and a matching data byte. The contents of the Synthesizer DSP HIP status and data registers are displayed

7. **"Synth FPGA load opn timeout"**. The entire Synthesizer FPGA program file has been transmitted to the Synthesizer, but after 1300 microseconds, no response has been received.

8. **"Synth FPGA load opn error"**. The entire Synthesizer FPGA program file has been transmitted to the Synthesizer, and the Synthesizer has responded with an error message. The contents of the Synthesizer DSP HIP status and data registers are displayed.

9. **"Synth DSP code rdbck timeout"**. A byte of the Synthesizer DSP operational code file has been transmitted to the Synthesizer, but after 65 microseconds, no response has been received.

10. **"Synth DSP code rdbck err"**. A byte of the Synthesizer DSP operational code file has been transmitted to the Synthesizer, and the Synthesizer has responded with an error message and/or a non-matching data byte rather than an OP COMPLETE message and a matching data byte. The contents of the Synthesizer DSP HIP status and data registers are displayed

11. **"Synth DSP code load opn timeout"**. The entire Synthesizer DSP operational code file has been transmitted to the Synthesizer, but after 65 microseconds, no response has been received.

12. **"Synth DSP code load opn err"**. The entire Synthesizer DSP operational code file has been transmitted to the Synthesizer, and the Synthesizer has responded with an error message. The contents of the Synthesizer DSP HIP status and data registers are displayed.

13. **"YIG Cal xx synth operation timeout"**. Data and strobe have been sent for one of the twelve Synthesizer YIG calibrations, but after 2.5 seconds, no response has been received.

14. **"YIG Cal xx synth operation error"**. Data and strobe have been sent for one of the twelve Synthesizer YIG calibrations, and the Synthesizer has responded with an error message. The contents of the Synthesizer DSP HIP status and data registers are displayed

15. **"YIG Cal xx data readback timeout"**. One of the twelve Synthesizer YIG calibrations has completed successfully, and a request has been sent to retrieve the results, but after .75 seconds, no response has been received.

16. **"YIG Cal xx data readback error"**. One of the twelve Synthesizer YIG calibrations has completed successfully, a request has been sent to retrieve the results, but the Synthesizer has responded with an error message. The contents of the Synthesizer DSP HIP status and data registers are displayed.

17. **"A1A2 Cal xx operation timeout"**. Data and strobe have been sent for one of the 41 A1A2 calibrations, but no response has been received within the time allotted. For cal numbers 0 and 41, this is 5 msec; for the remaining calibrations, this is 640 msec.

18. **"A1A2 Cal xx operation error"**. Data and strobe have been sent for one of 41 A1A2 calibrations, and the Synthesizer has responded with an error message. The contents of the Synthesizer DSP HIP status and data registers are displayed.

19. **"A1A2 Cal xx DSP Word 0 data readback timeout"**. One of the 41 A1A2 calibrations has completed successfully, and a request has been sent to retrieve the results, but after 5 msec, no response has been received.

20. **"A1A2 Cal xx DSP Word 0 data readback error"**. One of the 41 A1A2 calibrations has completed successfully, a request has been sent to retrieve the results, but the Synthesizer has responded with an error message. The contents of the Synthesizer DSP HIP status and data registers are displayed.

21. **"A1A2 Cal xx DSP Word 1 data readback timeout"**. One of A1A2 calibrations 1 - 39 has completed successfully, and a request has been sent to retrieve the second word of results, but after 5 msec, no response has been received.

22. **"A1A2 Cal xx DSP Word 1 data readback error"**. One of A1A2 calibrations 1 - 39 has completed successfully, a request has been sent to retrieve the second word of results, but the Synthesizer has responded with an error message. The contents of the Synthesizer DSP HIP status and data registers are displayed.

23. **"ALC SP FPGA cfg ack timeout"**. The command has been sent to the ALC telling it to get ready for SP FPGA startup program file data, but after 500 msec, no response has been received.

24. **"ALC SP FPGA cfg error"**. The command has been sent to the ALC telling it to get ready for SP FPGA startup program file data, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed.

25. **"ALC SP FPGA load opn timeout"**. The entire ALC SP FPGA startup program file has been transmitted to the ALC, but after 1300 microseconds, no response has been received.

26. **"ALC SP FPGA load opn err"**. The entire ALC SP FPGA startup program file has been transmitted to the ALC, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed.

27. **"ALC PM FPGA cfg ack timeout"**. The command has been sent to the ALC telling it to get ready for PM FPGA program file data, but after 500 msec, no response has been received. **(SERIES 125XXA/127XXA ONLY)**.

28. **"ALC PM FPGA cfg error"**. The command has been sent to the ALC telling it to get ready for SP FPGA program file data, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed. **(SERIES 125XXA/127XXA ONLY)**.

29. **"ALC PM FPGA load opn timeout"**. The entire ALC PM FPGA program file has been transmitted to the ALC, but after 1300 microseconds, no response has been received. **(SERIES 125XXA/127XXA ONLY)**.

30. **"ALC PM FPGA load opn err"**. The entire ALC PM FPGA program file has been transmitted to the ALC, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed. **(SERIES 125XXA/127XXA ONLY)**.

31. **"ALC prog mem test timeout"**. The ALC board has been commanded to test program memory, but hasn't responded after 1 second.

32. **"ALC prog mem test err"**. The ALC board has been commanded to test program memory, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed.

33. **"ALC lin mem test timeout"**. The ALC board has been commanded to test detector linearization memory, but hasn't responded after 1 second.

34. **"ALC lin mem test err"**. The ALC board has been commanded to test detector linearization memory, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed.

35. **"ALC delin mem test timeout"**. The ALC board has been commanded to test modulator delinearization memory, but hasn't responded after 1 second.

36. **"ALC delin mem test err"**. The ALC board has been commanded to test modulator delinearization memory, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed.

37. **"ALC Analog test timeout"**. The ALC board has been commanded to test the analog input circuitry, but hasn't responded after 1 second.

38. **"ALC Analog test err"**. The ALC board has been commanded to test the analog input circuitry, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed.

39. **"ALC DSP code rdbck timeout"**. A byte of the ALC DSP internal memory operational code file has been transmitted to the ALC, but after 65 microseconds, no response has been received.

40. **"ALC DSP code rdbck err"**. A byte of the ALC DSP internal memory operational code file has been transmitted to the ALC, and the ALC has responded with an error message and/or a non-matching data byte rather than an OP COMPLETE message and a matching data byte. The contents of the ALC DSP HIP status and data registers are displayed.

41. **"ALC DSP code load opn timeout"**. The entire ALC DSP internal memory operational code file has been transmitted to the ALC, but after 10 msec, no response has been received.

42. **"ALC DSP code load opn err"**. The entire ALC DSP internal memory operational code file has been transmitted to the ALC, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed.

43. **"ALC DSP ext code rdbck timeout"**. A byte of the ALC DSP external memory operational code file has been transmitted to the ALC, but after 65 microseconds, no response has been received.

44. **"ALC DSP ext code rdbck err"**. A byte of the ALC DSP external memory operational code file has been transmitted to the ALC, and the ALC has responded with an error message and/or a non-matching data byte rather than an OP COMPLETE message and a matching data byte. The contents of the ALC DSP HIP status and data registers are displayed.

45. **"ALC DSP ext code load opn timeout"**. The entire ALC DSP external memory operational code file has been transmitted to the ALC, but after 5 seconds, no response has been received.

46. **"ALC DSP ext code load opn err"**. The entire ALC DSP external memory operational code file has been transmitted to the ALC, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed.

47. **"ALC init timeout"**. The entire ALC DSP operational code file has been transmitted to the ALC, but after .5 seconds, no response has been received.

48. **"ALC init error"**. The entire ALC DSP operational code file has been transmitted to the ALC, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed.

49. **"ALC mod delin table build timeout"**. The ALC modulator delinearization table coefficients have been transmitted to the ALC, but after 10 seconds, no response has been received.

50. **"ALC mod delin table build err"**. The ALC modulator delinearization table coefficients have been transmitted to the ALC, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed.

51. **"ALC A17 det lin table build timeout"**. The ALC A17 CW detector linearization table coefficients have been transmitted to the ALC, but after 10 seconds, no response has been received.

52. **"ALC A17 det lin table build error"**. The ALC A17 CW detector linearization table coefficients have been transmitted to the ALC, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed.

53. **"ALC A8 det lin table build timeout"**. The ALC A8 CW detector linearization table coefficients have been transmitted to the ALC, but after 10 seconds, no response has been received.

54. **"ALC A8 det lin table build error"**. The ALC A8 CW detector linearization table coefficients have been transmitted to the ALC, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed.

55. **"ALC A5 det lin table build timeout"**. The ALC A5 CW detector linearization table coefficients have been transmitted to the ALC, but after 10 seconds, no response has been received.

56. **"ALC A5 det lin table build error"**. The ALC A5 CW detector linearization table coefficients have been transmitted to the ALC, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed.

57. **"ALC A17 det pulse table build timeout"**. The ALC A17 PULSE detector linearization table coefficients have been transmitted to the ALC, but after 10 seconds, no response has been received. **(SERIES 125XXA/127XXA ONLY)**.

58. **"ALC A17 det pulse table build error"**. The ALC A17 PULSE detector linearization table coefficients have been transmitted to the ALC, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed. **(SERIES 125XXA/127XXA ONLY)**.

59. **"ALC A8 det pulse table build timeout"**. The ALC A8 PULSE detector linearization table coefficients have been transmitted to the ALC, but after 10 seconds, no response has been received. **(SERIES 125XXA/127XXA ONLY)**.

60. **"ALC A8 det pulse table build error"**. The ALC A8 PULSE detector linearization table coefficients have been transmitted to the ALC, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed. **(SERIES 125XXA/127XXA ONLY)**.

61. **"ALC A5 det pulse table build timeout"**. The ALC A5 PULSE detector linearization table coefficients have been transmitted to the ALC, but after 10 seconds, no response has been received. **(SERIES 125XXA/127XXA ONLY)**.

62. **"ALC A5 det pulse table build error"**. The ALC A5 PULSE detector linearization table coefficients have been transmitted to the ALC, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed. **(SERIES 125XXA/127XXA ONLY)**.

63. **"ALC A17 CW det zero timeout"**. The ALC has been directed to find A17 CW detector zero, but after 5 seconds, no response has been received.

64. **"ALC A17 CW det zero error"**. The ALC has been directed to find A17 CW detector zero, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed.

65. **"ALC A17 PM det zero timeout"**. The ALC has been directed to find A17 PM detector zero, but after 5 seconds, no response has been received. **(SERIES 125XXA/127XXA ONLY)**.

66. **"ALC A17 PM det zero error"**. The ALC has been directed to find A17 PM detector zero, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed. **(SERIES 125XXA/127XXA ONLY)**.

67. **"ALC A8 CW det zero timeout"**. The ALC has been directed to find A8 CW detector zero, but after 5 seconds, no response has been received.

68. **"ALC A8 CW det zero error"**. The ALC has been directed to find A8 CW detector zero, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed.

69. **"ALC A8 PM det zero timeout"**. The ALC has been directed to find A8 PM detector zero, but after 5 seconds, no response has been received. **(SERIES 125XXA/127XXA ONLY)**.

70. **"ALC A8 PM det zero error"**. The ALC has been directed to find A8 PM detector zero, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed. **(SERIES 125XXA/127XXA ONLY)**.

71. **"ALC A5 CW det zero timeout"**. The ALC has been directed to find A5 CW detector zero, but after 5 seconds, no response has been received.

72. **"ALC A5 CW det zero error"**. The ALC has been directed to find A5 CW detector zero, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed.

73. **"ALC A5 PM det zero timeout"**. The ALC has been directed to find A5 PM detector zero, but after 5 seconds, no response has been received. **(SERIES 125XXA/127XXA ONLY)**.

74. **"ALC A5 PM det zero error"**. The ALC has been directed to find A5 PM detector zero, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed. **(SERIES 125XXA/127XXA ONLY)**.

75. **"ALC AM zero timeout"**. The ALC has been directed to find AM input zero, but after .5 seconds, no response has been received. **(SERIES 125XXA/127XXA ONLY)**.

76. **"ALC AM zero error"**. The ALC has been directed to find AM input zero, and the ALC has responded with an error message. The contents of the ALC DSP HIP status and data registers are displayed. **(SERIES 125XXA/127XXA ONLY)**.

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