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Giga-tronics

Series 50000B
VXIbus Microwave Synthesizer

Operation Manual

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WARRANTY

Giga-tronics instruments are warranted against defective materials and workmanship for one year from date of shipment. Giga-tronics will at its option repair or replace products that are proven defective during the warranty period. This warranty DOES NOT cover damage resulting from improper use, nor workmanship other than Giga-tronics service. There is no implied warranty of fitness for a particular purpose, nor is Giga-tronics liable for any consequential damages. Specification and price change privileges are reserved by Giga-tronics.

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About This Manual

This Operation Manual covers all aspects of Giga-tronics Series 50000B VXIbus syntheized microwave signal generators. Information required to operate, calibrate, and maintain the instrument is included. The manual is divided into the following Chapters:

Preface:

In addition to a comprehensive Table of Contents and general information about the manual, the Preface also contains a record of changes made to the manual since its publication, and a description of Special Configurations. If you have ordered a user-specific manual, please refer to page xiii for a description of the special configuration.

Chapter 1 – Introduction:

This chapter contains a brief introduction to the instrument and its performance parameters.

Chapter 2 – Operation:

A user's guide to the instrument and its programming languages.

Chapter 3 – Theory of Operation:

A description of the instrument's design and its internal functioning, to the block diagram level.

Chapter 4 – Calibration & Testing:

Procedures for calibration and performance testing.

Chapter 5 – Maintenance:

Procedrues for maintenance and troubleshooting.

Appendix A – Options:

Descriptions of the options available for the 50000B Series.

Index:

A word index of the various elements of the 50000B manual.

Changes that occur after publication of the manual, and Special Configuration data will be inserted as loose pages in the manual binder. Please insert and/or replace the indicated pages as detailed in the Technical Publication Change Instructions included with new and replacement pages.

Conventions

The following conventions are used in this product manual. Additional conventions not included here will be defined at the time of usage.

Warning

WARNING

The WARNING statement is enclosed in dashed lines and centered in the page. This calls attention to a situation, or an operating or maintenance procedure, or practice, which if not strictly corrected or observed, could result in injury or death of personnel. An example is the proximity of high voltage.

Caution

CAUTION

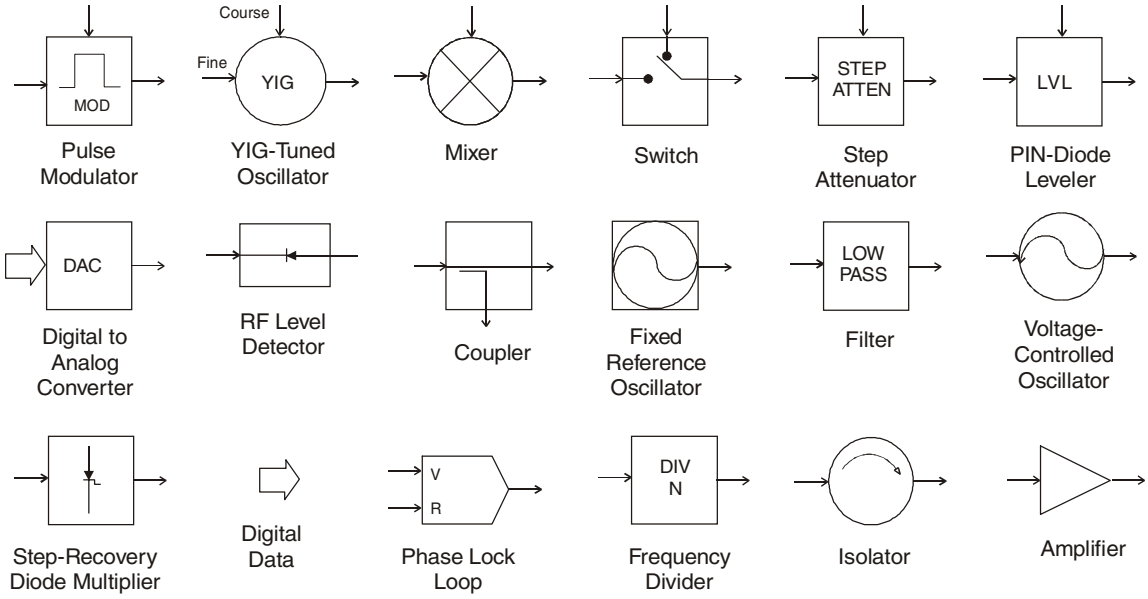
The CAUTION statement is enclosed with single lines and centered in the page. This calls attention to a situation, or an operating or maintenance procedure, or practice, which if not strictly corrected or observed, could result in temporary or permanent damage to the equipment, or loss of effectiveness.

Notes

NOTE: *A NOTE Highlights or amplifies an essential operating or maintenance procedure, practice, condition or statement.*

Symbols

Block diagram symbols frequently used in the manual are illustrated below.



Record of Manual Changes

This table is provided for your convenience to maintain a permanent record of manual change data. Corrected replacement pages will be issued as Technical Publication Change Instructions, and will be inserted at the front of the binder. Remove the corresponding old pages, insert the new pages, and record the changes here.

Change Instruction Number	Change Instruction Date	Date Entered	Comments

Special Configurations

When the accompanying product has been configured for user-specific application(s), supplemental pages will be inserted at the front of the manual binder. Remove the indicated page(s) and replace it (them) with the furnished Special Configuration supplemental page(s).

1

Introduction

1.1 Description

The Giga-tronics VXIbus Microwave Synthesizer produces microwave signals with a high degree of frequency accuracy, frequency resolution and spectral purity. These signals may be controlled in amplitude over a wide range and are capable of being modulated in AM, FM and pulse modes. The product is designed to be installed in a VXI frame and to operate in the VXIbus environment.

The Giga-tronics VXIbus product line is designed to take advantage of the building block characteristics of the VXI system. The synthesizer is divided into discrete, C-size modules. There are two basic modules, which must always be present in any system. The first required module is the Control module (Model 52000B). This single width unit provides an interface to the VXI bus system and generates control signals for all other Giga-tronics modules. These control signals use the 12 local bus lines of the P2 connector. The Control module also provides a number of analog reference signals via front panel connectors.

The other module required for a minimum system is the double-width Synthesizer module (various model numbers in the 50000B/51000B series). Microwave frequencies are synthesized from the signals supplied by the Control module. The Synthesizer module contains all required circuitry and components to generate, modulate, and level the RF output.

Adaptor modules may also be included for optional features to the system.

Complete performance specifications for each module are presented in Section 1.2 in this chapter.

1.1.1 Items Furnished

In addition to options and/or accessories specifically ordered, items furnished with the instrument are as follows:

1 Operation Manual

1 Set of Reference Signal SMB-to-SMB cables (as required by modules)

1 or more RF semi-rigid cables (as required by optional modules)

1.1.2 Items Required

A VXI mainframe which meets the power and cooling requirements of the modules is required. Appropriate output cabling, which is made to fit the female SMA output connector, can be ordered in the form of Accessory A001 (Cable Kit).

1.1.3 Tools and Test Equipment

Special tools are not required in order to operate Series 50000B instruments. Signal sources for external modulation should match the parameters outlined in the specifications in this chapter. Test equipment required for calibration and testing is described in Chapter 4 of the manual.

1.1.4 Storage

Giga-tronics VXIbus modules should be stored in an environment free from excessive dust and dirt and where the temperature remains in the range of -40 °C to +70 °C.

1.1.5 Cooling

The specifications for individual modules define their cooling and airflow requirements. If the module is to be operated outside of a properly ventilated VXI frame, auxiliary air circulation is required, such as a small fan directed at the module.

1.1.6 Receiving Inspection

Use care in removing the instrument from the carton and check immediately for physical damage, such as bent or broken connectors on the front and rear panels, dents or scratches on the panels, broken extractor handles, etc. Check the shipping carton for evidence of physical damage and immediately report any damage to the shipping carrier.

Each Giga-tronics instrument must pass rigorous inspections and tests prior to shipment. Upon receipt, the instrument's performance should be promptly checked to ensure that it's operation has not been impaired during shipment.

Each module is shipped in an operational condition and needs only to be plugged into a VXI frame to be used. A warm-up time of twenty minutes is recommended.

1.1.7 Safety Precautions

When installing modules into the mainframe, be sure that the connectors are properly aligned before pushing the modules into place. Use gentle but firm pressure to insert the modules and make sure they are fully seated for proper operation. In addition, make sure that the modules are installed in the correct positions relative to one another (see Positioning Requirements in Chapter 2).

1.1.8 Returning an Instrument

If you are returning an instrument to Giga-tronics for any reason, including service, first contact Giga-tronics Customer Service at **(800) 444-2878** or Fax at **(925)328-4702** so that a return authorization number can be assigned. You can also contact Customer Service via our e-mail address **repairs@gigatronics.com**.

To protect the instrument during reshipment, use the best packaging materials available. If possible use the original shipping container. If this is not possible, a strong carton or a wooden box should be used. Wrap the instrument in heavy paper or plastic before placing it in the shipping container. Completely fill the areas on all sides of the instrument with packaging material. Take extra precautions to protect the front and rear panels. Seal the package with strong tape or metal bands. Mark the outside of the package **"FRAGILE – DELICATE INSTRUMENT"**.

If corresponding with the factory or local Giga-tronics sales office regarding reshipment, please reference the full model number and serial number. If the instrument is being reshipped for repair, enclose all available pertinent data regarding the problem that has been found.

1.2 Performance Specifications

1.2.1 Control Module (Model 52000B)

VXIbus Characteristics

Compatibility	Fully compatible with VXIbus System Specification, Rev. 1.4
Device Type:	Message based instrument
Module Size:	C-size, one slot wide
Protocol:	Word serial
Languages:	HP compatible syntax subset, CIIL syntax subset, SCPI syntax subset, Giga-tronics syntax subset

Local Bus Characteristics

Control Capacity:	Supports 1 - 8 other synthesizer system modules
Digital Output Signals (Outputs to Controlled Modules):	Output is to the right (as viewed from the front) on the 12 local bus lines on connector P2

Timebase Characteristics

Internal:	10 MHz temperature compensated crystal oscillator; aging rate $\pm 1 \times 10^{-6}$/year after 20 minutes of continuous operation
External (automatically overrides internal time base):	10 MHz $\pm 1 \times 10^{-6}$ or better, >1.5 Vpp
Timebase Related Analog Output Signals (derived from internal or external time base):	10 MHz, ECL levels; 330 MHz, -15 dBm (typical) into 50 Ω; 10 MHz TIMEBASE OUT, ≥2 Vpp into 50 Ω

Front Panel Connectors

10 MHz Output:	Type SMB male
330 MHz Output:	Type SMB male
Timebase Input:	Type BNC female
Timebase Output:	Type BNC female

Power Supply Requirements

Voltage and Current:

Supply (Volts DC)	Max Current (mA)
+24	175
+12	100
+5	2500
+5 standby	not used
-2	not used
-5.2	not used
-12	700
-24	30

Power Rating: 30 W, maximum

Environmental Specifications

Temperature Range:

Operating: 0 °C to 50 °C

Non-operating: -40 °C to 70 °C

Cooling Requirements: For 10 °C temperature rise, air flow must be 2 liters/sec at 0.1 mm H_2O

Relative Humidity: 0 to 95%, non-condensing

EMI: Below 1 GHz, complies with VXIbus Specification Rev 1.4; above 1 GHz, complies with MIL-STD-461C RE02 (part 2)

Warm-Up Time: 20 minutes (typical)

Weight and Dimensions

Weight: 5 lbs.

Dimensions: C-size VXI module, one slot wide

1.2.2 Synthesizer Module (Models 50XXXB, 51XXXB)

VXIbus Characteristics

Compatibility: Compatible with VXIbus System Specification, Rev 1.4

Module Size: C-size, two slots wide

Programming: Local bus from the associated Giga-tronics VXIbus Control Module

Frequency Characteristics

Range (see table):

Model Number	Frequency Range	Drawing Number
50208B	2 - 8 GHz	31175
50212B	2 - 12 GHz	31176
50218B	2 - 18 GHz	31177
50220B	2 - 20 GHz	31178
50612B	5.4 - 12.5 GHz	31179
50618B	6 - 18 GHz	31180
51218B	12 - 18 GHz	31181
50008B	.01 - 8 GHz	31182
50012B	.01 - 12 GHz	31183
50018B	.01 - 18 GHz	31184
50020B	.01 - 20 GHz	31185

Resolution: 1 Hz (throughout the entire frequency range)

Accuracy and Stability: Identical to, and determined by, the timebase oscillator selected in the control module

Spectral Purity

Harmonics (up to maximum frequency of synthesizer): ≤-50 dBc (measured at +0 dBm, 2-20 GHz);
≤-40 dBc (measured at +0 dBm, .01 to 2 GHz)

Subharmonics: (none)

Non-harmonics: (see table below)

Non-harmonic Spurious Frequencies (tested at 0 dBm)

Offset Frequency	Level	Typical
<100 KHz	<-40 dBc	<-50 dBc
100 KHz - <1 MHz	<-50 dBc	<-60 dBc
>1 MHz	<-60 dBc	<-70 dBc

SSB Phase Noise: (see table below)

Single Sideband Phase Noise

Frequency (GHz)	Offset from Carrier						
	100 Hz	1 KHz	10 KHz	100 KHz			
	All Models			50X08B	50X12B 51218B	50618B	50X18B 50X20B
<2	-70	-70	-75	-97	-97		-97
2 - 8	-75	-75	-77	-112	-107	-97	-102
8 - 12	-70	-70	-75		-107	-97	-97
12 - 16	-65	-65	-72		-107	-97	-97
16 - 18	-60	-60	-72		-97	-97	-97
18 - 20	-60	-60	-70				-97

Residual FM (50 Hz - 15 KHz bandwidth): <200 Hz rms, below 8 GHz;
<300 Hz rms, from 8 GHz to 16 GHz;
<400 Hz rms, above 16 GHz

RF Output Power Parameters

Maximum Leveled Output:	≥+8 dBm (.01 - 2 GHz) ≥+12 dBm (2 - 12 GHz) ≥+9 dBm (12 - 20 GHz) (NOTE: Option 26 reduces maximum leveled power by 1 dB from 8-16 GHz and 2 dB above 16 GHz)
Resolution:	0.1 dB
Minimum Leveled Output:	-10 dBm (-15 dBm typical); -90 dBm with Option 26
RF Off:	Typically attenuates a 0 dBm signal to -140 dBm at the output connector
Output Accuracy:	±2 dB (internally leveled)
Flatness:	Included in accuracy
Output Impedance:	50 Ω, nominal
Output SWR:	<2:1

Amplitude Modulation (AM) – General

AM specifications apply for waveforms whose envelope peak is at least 1 dB below maximum specified output power, with FM off and PM off. However, AM may be operated simultaneously with FM and/or PM.

AM Envelope Parameters

(measured at 7 dB below max rated power):

Depth:	0 to ≥82%, 90% typical
Bandwidth :	10 Hz to 10 kHz (50 kHz, typical) (50% depth; 3 dB points referenced to 1 kHz)
Harmonic Distortion:	<10% at 1 kHz rate and 50% depth, 5% typical (relative to externally supplied AM envelope)

Externally Supplied AM Envelope

Waveform:	Any waveform compatible with bandwidth considerations
Rate:	See Bandwidth, above
Sensitivity:	1 Vpp = 50% modulation ±10% (i.e., 40 - 60%), at a 1 kHz rate, measured at 7 dB below maximum rated power
Input Impedance:	600 Ω, nominal, AC coupled

Frequency Modulation (FM) – General

FM specifications apply with AM and PM off. However, FM may be operated simultaneously with AM and/or PM.

FM Envelope Parameters

Deviation:	10 kHz to 5 MHz, peak
Bandwidth:	±3 dB, 10 Hz to 1 MHz
Residual FM:	≤1.5 kHz rms, typical

Externally Supplied FM Envelope

Waveform:	Any waveform compatible with bandwidth considerations
Rate:	See Bandwidth, above
Sensitivity:	2 Vpp is maximum (nominal) deviation
Input Impedance:	50 Ω, nominal

Pulse/Square Wave Modulation (PM) – General

PM specifications apply with AM and FM off. However, PM may be operated simultaneously with AM and/or FM.

PM Envelope Parameters

ON/OFF Ratio:	>80 dB
Rise/Fall Time:	<25 ns
Overshoot, Undershoot, & Ringing:	±2 dB, typical
Pulse Amplitude Accuracy:	Same as RF output level accuracy

Externally Supplied PM Envelope

Repetition Rate:	DC to 1 MHz
Pulse Delay:	100 ns, typical (output envelope leading edge reference to input pulse leading edge)
Input Pulse Required:	TTL level pulse, >50 ns wide (leveled output), positive level = RF on

Inputs Required

Local Bus Input Signals:	Inputs from the left (as viewed from the front), on the 12 local bus lines on connector P2 (from a compatible Giga-tronics VXIbus Module)
Timebase Related Analog Input Signals:	10 MHz, ECL levels; 330 MHz, -15 dBm, typical (from a compatible Giga-tronics VXIbus Module)

Outputs Supplied

RF Output:	RF signal produced by the module; available at the RF OUT connector
Digital Output Signals:	Outputs to the right (as viewed from the front) on the 12 local bus lines on connector P2 (replicates corresponding input signals to control other Giga-tronics VXIbus modules)
Timebase Related Analog Output Signals:	10 MHz, ECL levels; 330 MHz, -15 dBm, typical (available at **REFERENCE OUT** connectors) (buffered from corresponding inputs; drives other Giga-tronics VXIbus modules)

Front Panel Connectors

10 MHz Input and 10 MHz Output:	Type SMB male
330 MHz Input and 330 MHz Output:	Type SMB male
AM In:	Type SMB male
FM In:	Type SMB male
PM In:	Type SMB male
RF Out:	Type SMA female

Front Panel Indicators

Lock:	Green LED
Level:	Green LED
RF On:	Green LED

Power Supply Requirements

Voltage & Current:

Supply (Volts DC)	Max Current (mA)
+24	2500
+12	1200
+5	not used
+5 standby	not used
-2	not used
-5.2	not used
-12	1600
-24	200

Power Rating: 100 W, maximum

Environmental Specifications

Temperature Range: 0 °C to +50 °C (operating); -40 °C to +70 °C (non-operating)

Cooling Requirements: For 10 °C temperature rise, air flow must be 5 liters/sec at 0.2 mm H_2O

Relative Humidity: 0 to 95%, non-condensing

EMI: Below 1 GHz, complies with VXIbus Specification Rev 1.4; above 1 GHz, complies with MIL-STD-461C REO2 (part 2)

Warm-Up Time: 20 minutes (typical)

Weight and Dimensions

Weight: 12 lbs.

Dimensions: C-size VXI module, two slots wide

2

Operation

2.1 Installation

2.1.1 Control Module Address Settings

The Control module requires no pre-installation configuration and can be installed in any slot of the VXI frame (except Slot 0). Its VXI Logical Address is assigned by means of a DIP switch. The switch is accessible through an opening on the left side of the module.

The switch positions represent a binary number pattern from 0 to 255 (more than one bit switch can be set to 1). The bit switch nearest the bottom rail of the module is the least significant bit. The switch position marked **ON** (toward the back of the module) is tied to ground through a resistor and is interpreted as a binary 0. The **OFF** (forward) position is interpreted as a binary 1.

The factory setting for this address is all 1 bits (hex FF, decimal 255). In the VXI environment, this value specifies dynamic configuration, which means that at start-up the Slot 0 controller will first perform a roll call of fixed address devices and then assign free addresses to all dynamic configuration devices. This prevents address conflicts.

The Model 52000B Control module is the only Giga-tronics module recognized directly by the Slot 0 controller. All other Giga-tronics modules must be installed contiguously to the right of the Model 52000B Control module and are recognized via the VXI local bus (12 lines which are forwarded via the backplane and reserved for local purposes).

2.1.2 Address Settings for Other Modules

All of the other Giga-tronics modules require the selection of local addresses to differentiate them from one another. The address of each module is set by a row of switches (accessible from the outside of the module). However, in the case of a local address, these switches are not interpreted as a binary number. Only one of the eight switches should be in the ON (back) position at a time. The switches are labeled 0 - 7 and represent local addresses 0 - 7. Local addresses must be consecutive within a group of modules which work together.

The Synthesizer module should be placed to the immediate right of the Control module and should have the lowest address. The addresses of subsequent modules increase consecutively with the last module in the RF path having the highest address. The recommended arrangement is to set the Synthesizer module address to 0, the next module address to 1, and so on, so that the modules will be easy to identify for programming purposes.

Be sure that modules do not share the same address.

2.1.3 Inserting the Modules

After the module addresses are set, each module can be inserted into the VXI frame. Since the VXI local bus is not strapped across the entire width of the frame but only connects between the outer rows of the

P2 connector in adjacent slots, all Giga-tronics modules must be installed in one contiguous block. Also note that the next slot to the right of the last Giga-tronics module will have data appearing on its local bus lines. This should not cause a problem unless a module placed in that position uses those pins.

It will not cause a conflict if a second Giga-tronics Control module is placed to the right of a block of Giga-tronics modules. The Control module does not connect to the left direction local bus.

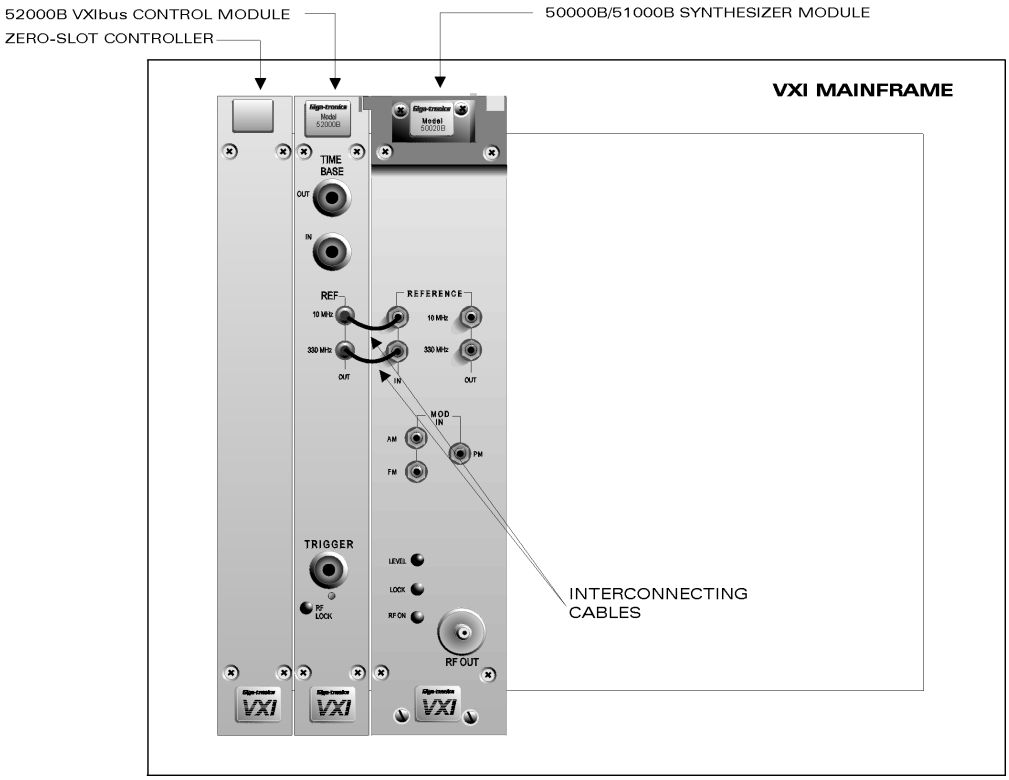


Figure 2-1: Module Mainframe Positions

2.1.4 Interconnection

Once the modules have been inserted in the VXI frame, use the supplied coaxial cables to connect the 10 MHz and 330 MHz signals (these are timebase-derived reference signals). These cables are required for proper interconnection of the Control module and any subsequent Synthesizer modules.

Begin by connecting the Control module 10 MHz output to the 10 MHz input on the first Synthesizer module. Likewise connect the 330 MHz line (see Figure 2-1). All cable assemblies are identical and can be used in any position. If there is more than one Synthesizer module in the system, connect the two signal outputs of the first module to the inputs of the next.

If it is required to place some other Giga-tronics module between two Synthesizer modules, longer cables can be fabricated using SMB female type connectors and a length of appropriate 50 ohm coaxial cable. Cable length should be no greater than is necessary to bridge the gap.

2.1.5 External Inputs

An external 10 MHz timebase can be connected to the Control module to allow the use of an external signal as a common system reference. The internal timebase is automatically disconnected when the external one is connected. The external timebase must have an amplitude of at least 1.5 Vpp and must be accurate to within 1×10^{-6}.

The Synthesizer module has inputs which accept external modulating signals for AM, FM and PM. See the specifications in Chapter 1 for input parameters. The Synthesizer module includes a 10-pin Sweep Input connector, which accepts sweep control signals.

2.1.6 Connections to the VXI Mainframe

All modules connect to the backplane of the VXI mainframe through a pair of 96-pin connectors (P1 and P2). Pin assignments for these connectors are shown below.

Table 2-1: VXI Backplate Pinouts

Pin No.	P1 Connector			P2 Connector		
	Row A	Row B	Row C	Row A	Row B	Row C
1	D00	$\overline{\text{BBSY}}$	D08	ECLTRG0	+5V	CLK10+
2	D01	BCLR	D09	-2V	GND	CLK10-
3	D02	$\overline{\text{ACFAIL}}$	D10	ECLTRG1	RSV1	GND
4	D03	$\overline{\text{BG0IN}}$	D11	GND	A24	-5.2V
5	D04	$\overline{\text{BG0OUT}}$	D12	LBUSA00	A25	LBUSC00
6	D05	$\overline{\text{BG1IN}}$	D13	LBUSA01	A26	LBUSC01
7	D06	$\overline{\text{BG1OUT}}$	D14	-5.2V	A27	GND
8	D07	$\overline{\text{BG2IN}}$	D15	LBUSA02	A28	LBUSC02
9	GND	$\overline{\text{BG2OUT}}$	GND	LBUSA03	A29	LBUSC03
10	SYSCLK	$\overline{\text{BG3IN}}$	$\overline{\text{SYSFAIL}}$	GND	A30	GND
11	GND	$\overline{\text{BG3OUT}}$	$\overline{\text{BERR}}$	LBUSA04	A31	LBUSC04
12	$\overline{\text{DS1}}$	$\overline{\text{BR0}}$	$\overline{\text{SYSRESET}}$	LBUSA05	GND	LBUSC05
13	$\overline{\text{DS0}}$	$\overline{\text{BR1}}$	$\overline{\text{LWORD}}$	-5.2V	+5V	-2V
14	$\overline{\text{WRITE}}$	$\overline{\text{BR2}}$	AM5	LBUSA06	D16	LBUSC06
15	GND	$\overline{\text{BR3}}$	A23	LBUSA07	D17	LBUSC07
16	$\overline{\text{DTACK}}$	AM0	A22	GND	D18	GND
17	GND	AM1	A21	LBUSA08	D19	LBUSC08
18	$\overline{\text{AS}}$	AM2	A20	LBUSA09	D20	LBUSC09
19	GND	AM3	A19	-5.2V	D21	-5.2V
20	$\overline{\text{IACK}}$	GND	A18	LBUSA10	D22	LBUSC10
21	$\overline{\text{IACKIN}}$	SERCLK	A17	LBUSA11	D23	LBUSC11
22	$\overline{\text{IACKOUT}}$	$\overline{\text{SERDAT}}$	A16	GND	GND	GND
23	AM4	GND	A15	$\overline{\text{TTLTRIG0}}$	D24	$\overline{\text{TTLTRIG1}}$
24	A07	$\overline{\text{IRQ7}}$	A14	$\overline{\text{TTLTRIG2}}$	D25	$\overline{\text{TTLTRIG3}}$
25	A06	$\overline{\text{IRQ6}}$	A13	+5V	D26	GND
26	A05	$\overline{\text{IRQ5}}$	A12	$\overline{\text{TTLTRIG4}}$	D27	$\overline{\text{TTLTRIG5}}$
27	A04	$\overline{\text{IRQ4}}$	A11	$\overline{\text{TTLTRIG6}}$	D28	$\overline{\text{TTLTRIG7}}$
28	A03	$\overline{\text{IRQ3}}$	A10	GND	D29	GND
29	A02	$\overline{\text{IRQ2}}$	A09	RSV2	D30	RSV3
30	A01	$\overline{\text{IRQ1}}$	A08	MODID	D31	GND
31	-12V	+5V STDBY	+12V	GND	GND	+24V
32	+5V	+5V	+5V	SUMBUS	+5V	-24V

2.2 Remote Programming

2.2.1 Command Addressing

Two levels of addressing may be required when sending remote control commands to Giga-tronics Series 50000B instruments as described below.

1. Commands in the VXI environment are transmitted to the Slot 0 controller and in turn to the Giga-tronics Control module (commands must specify the VXI Logical Address of the Control module).

2. In addition, certain commands sent to the Control module must be directed towards the Synthesizer module. The means by which the local address of the Synthesizer module is specified will depend upon the remote control command language used. Typically, after the local address is specified it remains in effect until another local address is specified.

2.2.2 Languages Available

All Synthesizer functions are designed to be controlled over the VXIbus. At present, two languages are fully implemented (HP-style and CIIL), and two others (SCPI and GT) are partially implemented. These languages are introduced briefly below, and discussed in more detail under separate headings.

- HP-style syntax is the default language at power-up. It is a set of commands created in the style of Hewlett Packard commands for the 50000B series of instruments. This language has the most varied and detailed command set of the languages available for the Series 50000B.
- Control Interface Intermediate Language (CIIL) is the command syntax used in the MATE program.
- Standard Commands for Programmable Instruments (SCPI) is a language specified by the SCPI Consortium. It is designed to standardize commands and data to and from instruments regardless of the manufacturer. SCPI promotes consistency from the remote programming standpoint between instruments, which are of the same class or have the same functional capability. For a given function such as frequency or power, SCPI specifies the command set that is available for that function.
- Giga-tronics syntax is a set of remote control commands developed for earlier Giga-tronics instruments. A subset of these commands is implemented in the 50000B Series for the convenience of users who are already familiar with them.

2.3 HP-Style Syntax

2.3.1 Synthesizer Local Address

Most commands must be directed towards the synthesizer module, so it is necessary to specify the local address of that module. This is accomplished by sending the command LAx, where x is the appropriate local address. All local commands are directed to this address until another LAx is sent.

If no local address has been selected the Control module directs synthesizer commands to the Synthesizer module having the lowest local address.

Command Format

Commands in the HP-style syntax are represented in the manual by upper case letters. Some commands are followed by one or more lower case letters. These letters are interpreted as follows:

a Indicates that alphanumeric characters are expected.

b Indicates that one or more 8-bit bytes (entered in binary form) are expected.

d Indicates that a decimal number is expected. Decimal numbers may be signed. Exponents are indicated by an E; thus, +4.5E-6 represents 4.5×10^{-6}.

h indicates that a hexadecimal number is expected.

n Indicates that a single digit (0-9) is expected.

t Indicates that a terminator is expected. Usually, codes which specify units are terminators. The codes are HZ (Hz), KZ (kHz), MZ (MHz), GZ (GHz), DB (dB), DM (dBm), SC (sec), MS (msec), and US (μ sec). Alternatively, a comma or line feed can be used as a terminator. This causes the instrument to scale the corresponding function to the fundamental units of Hz, dB, dBm, or seconds.

The absence of lower case letters in a command indicates that the command is complete as shown and requires no variables.

2.3.2 Default Settings

The default settings at power-up, or after a *RST command, are as follows:

- RF is off.
- Frequency is set to minimum.
- All modulation is off.
- Level is set to 0 dBm (this does not take effect until the RF is turned on).

2.3.3 Command Set

The command set for the HP-style syntax is listed in the following tables. The commands are discussed in alphabetical order with some related commands grouped together.

Commands *CLS - *WAI (IEEE-488.2 Common Commands)

See the SCPI section for more information about these commands.

Table 2-2: Commands *CLS - *WAI

Command	Description
*CLS	Clear Status
*ESE	Event Status Enable
*ESE?	Event Status Enable Query
*ESR?	Event Status Register Query
*IDN?	Identify
*OPC	Operation Complete
*OPC?	Operation Complete Query
*RST	Reset
*SRE	Status Register Enable
*SRE?	Status Register Enable Query
*STB?	Status Byte Query
*TST?	Self-Test Query (see the self-test commands, TA etc.).
*WAI	Wait-to-Continue

Commands AM0 through FM1 (Miscellaneous)

Table 2-3: Commands AM0 - FM1

Command	Description
AM0	Deactivate external AM.
AM1	Activate external AM.
AMF0	Deactivate external fast AM.
AMF1	Activate external fast AM.
CIIL	Switch to CIIL language.
CW d t	Select the CW (fixed frequency) mode.
DN	Down step of frequency or power level, depending on whether the last command was CW (Frequency) or PL (Power).
[	Down step of frequency or power level, depending on whether the last command was CW (Frequency) or PL (Power).
FM0	Deactivate external FM.
FM1	Activate external FM.

Commands GA through GR (FSD Commands)

Frequency Sweep Digital (FSD) commands permit the setup then activation of digital frequency sweep. Depending on the sweep triggering method chosen, the sweep can begin immediately upon receipt of the activation command or after the activation command followed by a definable hardware trigger signal. The sweep can be single or continuously repetitive. The next frequency is obtained either by adding the step size increment to the last frequency or by retrieving the next frequency value from a list stored in memory.

Table 2-4: Commands GA - GR

Command	Description
GA d t	Set the sweep start frequency to d GHz. Default: minimum frequency.
GB d t	Set the sweep stop frequency to d GHz. Default: maximum frequency.
GC d t	Set the frequency step size to d GHz. Default: 1 GHz.
GD d t	Set the dwell time to d seconds. Default: 1 s.
GEI	Start the sweep immediately upon receipt of a GG command (this is the default sweep triggering mode).
GEWF	Start the sweep (following receipt of a GG command) when the hardware trigger input goes to the FALSE level (0 V).
GEWT	Start the sweep (following receipt of a GG command) when the hardware trigger input goes to the TRUE level (+5 V).
GFC	Select the continuous sweep mode (the sweep repeats automatically).
GFR	Select the retriggerable single sweep mode (the sweeper will respond to another trigger occurring after completion of the sweep).
GFS	Select the single sweep mode (the sweeper will NOT respond to another trigger occurring after completion of the sweep).
GG	Start the sweep. This command should be entered only after all the setup commands have been entered with the desired values. If the GEI command was sent previously, the GG command will cause the sweep to begin immediately. If the GEWF or GEWT command was sent, the GG command will cause the sweeper to wait for the appropriate hardware trigger input.
GH	Halt the sweep, leaving the frequency at the last stepped value (NOTE: a CW command will also halt the sweep).
GIM	Memory increment mode: increment the frequency by going to the next nonzero frequency stored in an array of up to ten memory locations (see the GJ command). The start frequency, stop frequency, and step size have no effect in this mode, but the dwell time does apply.
GIN	Normal increment mode: increment the frequency by adding the defined step size to the last frequency (see the GC command). The start frequency, stop frequency, step size, and dwell time all apply in this mode.
GJ n d t	Save a sweep frequency (d) at memory location n (the range of values for n is 0 - 9). If the value saved at any memory location is zero, that memory location will have no effect on the sweep.
GK	Clear all saved sweep frequencies from memory (see the GJ command).
GR	Resume a sweep that was halted by a GH command.

Commands GT through LLA (Miscellaneous)

Table 2-5: Commands GT - LLA

Command	Description
GT	Switch to Giga-tronics syntax.
HP	Switch to HP syntax.
LAx	Select local address x for succeeding commands.
LLA	List local addresses.

Commands OI through OV (Output Commands)

Output commands are requests for information. They cause the Series 50000B to transmit data to the controller.

Table 2-6: Commands OI - OV

Command	Description
OI	Send identification.
OPCW	Send the current CW (fixed) frequency.
OPPC	Send the current output coarse level (that is, the setting of the step attenuator).
OPPF	Send the current output fine level (that is, the setting of the level control loop).
OPPL	Send the current power level.
OS	Send the current status (in the form eight ASCII characters, 1 or 0, to indicate lock/ level status).
OV	Send the version of firmware installed.

Commands PC through PL (Power Level Commands)

The output power level may be specified as a single quantity or as separate coarse and fine levels to choose a particular combination of settings for the step attenuator and the leveling loop. Output power always equals the sum of the coarse and fine levels.

When output power is specified as a single quantity, coarse and fine levels are set automatically so as to yield the desired sum. The coarse level changes in 10 dB steps at levels -5 dBm, -15 dBm, and so on. For output levels above -5 dBm the coarse level is set to zero. For a level of -5 dBm, the coarse level is set to -10 and the fine level is set to +5. To avoid the change of attenuator step which normally occurs when the level is set to -5 dBm, specify a coarse level of zero and a fine level of -5.

Table 2-7: Commands PC - PL

Command	Description
PC d t	Set the coarse level in dBm. This specifies the setting of the step attenuator (from 0 dBm to maximum attenuation in 10 dB steps).
PF d t	Set the fine level in dBm. This specifies the setting of the leveling loop, in 0.1 dB increments from -20 dBm to +20 dBm.
PL d t	Set the output power level as a single quantity, in dBm. The coarse and fine levels will be set automatically in order to produce the desired level.

Commands PM0 through SHPL (Miscellaneous)

Table 2-8: Commands PM0 - SHPL

Command	Description
PM0	Deactivate external pulse modulation.
PM1	Activate external pulse modulation.
RF0	Deactivate the RF output.
RF1	Activate the RF output.
RT	Run self-test, a lock-and-level test of the synthesizer's operation across a defined frequency range (see the Self Test commands, TA etc.).
SA0	Disable the step attenuator (the attenuator remains fixed at zero).
SA1	Enable the step attenuator.
SC0	Deactivate scan modulation.
SC1	Activate scan modulation.
SCPI	Select the SCPI syntax.
SHCW d t	Select the frequency step size (for UP and DN commands).
SHPL d t	Select the power level step size (for the UP and DN commands).

Commands TA through TSD (Self Test Commands)

These commands all relate to the instrument's self-test routine.

Table 2-9: Commands TA - TSD

Command	Description
TA	Abort the test.
TFB d t	Set the beginning frequency for the test to d. Default: minimum frequency.
TFE d t	Set the ending frequency for the test to d. Default: maximum frequency.
TFS d t	Set the frequency step size for the test to d. Default: 1 GHz.
TFQ?	Test frequency quit query (at what frequency did the test stop?). The test quits when a failure is detected. Default: 0 (test not yet run).
TPC d t	Set the coarse power level for the test to d dBm. This specifies the setting of the step attenuator (from 0 dBm to maximum attenuation in 10 dB steps) during the test. Default: 0 dBm.
TPF d t	Set the fine power level for the test to d dBm. This specifies the setting of the leveling loop in 0.1 dB increments from -20 dBm - +20 dBm. Default: maximum leveled power.
TSB?	TST Status Binary Query.
TSD?	TST Status Decimal Query.
Related Commands	
*TST?	Self-Test Query
RT	Run self-test is a lock-and-level test of the synthesizer operation across a defined frequency range.

The *TST? command (an IEEE-488.2 Common Command) will preserve (it will save and later restore) these states:

RFx RF On/Off state

CWx CW Frequency value

PCx Power Level (Coarse) value

PFx Power Level (Fine) value

The test will then switch in the maximum step attenuation before doing its own testing to not damage any user circuitry at the RF output connector. The Power Level (fine) value during the test will be the maximum output value for the unit (usually 10 dBm), but the Power Level (coarse) is usually -90 dB. The connector output power is the sum of the two, which is small enough that it presents no risk of damage.

The *TST? command always returns a decimal value result. If the returned value is 0, the test ran without errors. If not, the value is the sum of a series of weights as will be explained later.

The RT command resembles the *TST? command but differs in two respects. The RT command does not reply (separate commands are provided to request results afterward.) The RT command stops at its last frequency, and does not remember the original frequency from before the test was run.

You must separately request the results of the RT command. You might also want to request again the reply of the *TST? command in a different format. Two queries are provided for different style results.

The TSB? (Test Status Binary) query requests the result as a series of ASCII characters; each is either a 1 or a 0. The characters are in order and each one has a specific meaning. For any condition, 1 means the particular condition is satisfactory and 0 means it is not satisfactory. A test that runs without errors will return a TSB? of 11111111.

The TSD? (Test Status Decimal) query requests the same result expressed as a decimal number. If the returned value is 0, the test ran without errors. If not, the value is the sum of a series of weights which depend upon what type of hardware makes up the device. The inclusion of a particular condition's weight in the sum means the condition is not satisfactory.

The bit/weight meanings in the test status reply are the same whether the result is queried by a TSB? or a TSD? command, as illustrated in Table 2-10.

Table 2-10: Bit/Weight Meanings

Bit	Weight	Meaning
7	128	Leveled
6	64	Downconverter Loop Locked
5	32	110 MHz Loop Locked
4	16	Output Loop Locked
3	8	300 MHz Loop Locked
2	4	80 MHz Loop Locked
1	2	(not used)
0	1	(not used)

If you inadvertently enter a very small step size and then start the test running, the abort command (TA) provides a way of stopping it before completion. The test is simply stopped. If you had issued the *TST? command, no reply will occur after abort. You must manage the clearing of your expected reply.

With the *TST? command, you simply wait for the reply. With the RT command, you must be sure the test is done before requesting its status via TSB? or TSD?. The easiest way to do this is by using the *WAI command to wait until the test is done. You might prefer *OPC or *OPC?. Current firmware requires that the coordination command be on its own command line; likewise for the following TSB? or TSD? command.

Commands UL0 through] (Miscellaneous)

Table 2-11: Commands UL0 through]

Command	Description
UL0	Unleveled mode off
UL1	Unleveled mode on
UP	Up step for CW (Frequency) or PL (Power)
]	Up step for CW (Frequency) or PL (Power)

2.4 CIIL Syntax

2.4.1 Command Format

The elements of a CIIL command line are, in sequence, as follows:

```
<command> <noun> <port> <code> <modifier> <value> <code> <modifier> <value>
```

The command is always required. The nature of the command determines which elements must follow it, if any. Some commands, for example, must be followed by a noun. The nature of the command determines the category from which the noun must be chosen. The nature of the noun, in turn, determines the elements which must follow it, and so on.

2.4.2 Commands

STA (status request)

(This command is complete in itself and needs no following information.) For the most recent channel selected:

A series of eight 1 or 0 characters is sent.

1 is TRUE, 0 is FALSE. From left to right, each 1 or 0 means:

Leveled
Locked (Downconverter - if present)
Locked (110 MHz loop)
Locked (Output loop)
Locked (300 MHz loop)
Locked (80 MHz loop)
(not used)
(not used)

FNC (function)

This command requires a following noun to be chosen from this group:

ACS	AC Signal, no modulation
AMS	Amplitude modulated signal
FMS	Frequency modulated signal
PAC	Pulse modulated signal
MDS	Signal with at least one modulation (AM, FM, PM)

All parameters required for setup must be given in a single FNC command. After the noun there must be a channel specification of the format :CHn, where n is 0 through 7, representing a populated module address.

Next come <code, modifier, value> triplets. For the Giga-tronics VXI Synthesizer System, code is always SET. Modifier will be a member of the following group, and will depend upon the preceding noun. A noun will require more than one modifier. Each modifier has its requirement for value as shown in Table 2-12.

Table 2-12: Modifier Requirement Value

Modifier	Significance	Value
FREQ	Frequency (Hz)	Numeric
POWR	Power (dBm)	Numeric
CFRQ	Carrier Frequency (Hz)	Numeric
AMOD	External AM	EXT
FMOD	External FM	EXT
PLMD	External PM	EXT
MDSC	External PM	EXT
PRFR*	Frequency (Hz)	Numeric
POSS*	Positive Slope	[No Value]

Notes:

*PRFR & POSS are no-operations for this device but are allowed for CIIL compatibility.

The noun-modifier relationships are:

ACS requires FREQ and POWR (and optionally MDSC, PRFR or POSS).
AMS requires CFRQ and POWR and AMOD.
FMS requires CFRQ and POWR and FMOD.
PAC requires CFRQ and POWR and PLMD.
MDS requires CFRQ and POWR and one or more of AMOD, FMOD, PLMD.

RST (Reset)

This command requires a noun and a channel but nothing else:

RST noun :CHn

For the specified channel:

Frequency is set to its lowest value.
Power is set to 0 dBm.
All modulation is turned off.

Example Strings

RST ACS :CH0
FNC ACS :CH2 SET FREQ 7E9 SET POWR -9
FNC AMS :CH3 SET CFRQ 6789000000 SET POWR 0 SET AMOD EXT
FNC MDS :CH5 SET CFRQ 8E9 SET POWR -15 SET PLMD EXT SET FMOD EXT
FNC ACS :CH2 SET FREQ 7E9 SET POWER 0 SET MDSC EXT

2.5 SCPI Syntax

The SCPI syntax is now implemented in the 50000B Series. It includes the IEEE 488.2 Common commands, status reporting, error reporting, and table-specified defaults at power-up or *RST.

2.5.1 SCPI Command Format

Details of typography (such as indentation, case, and punctuation) are very significant in SCPI and must be attended to with great care. The typographic conventions employed in the SCPI command tables which follow are summarized here.

Colons indicate changes of level in the SCPI tree structure. If a command is represented in the format ALPHA:BETA:GAMMA, then BETA is one level down from ALPHA, and GAMMA is two levels down from ALPHA. If ALPHA is printed at the left margin, ALPHA is at the root level. In the command tables, indentation indicates relative levels.

Commands can be entered in upper or lowercase. However, only required letters are in upper case in the command table. If you enter more than the required letters, you must enter the entire command (if the command is INITiate, you may use either INIT or INITIATE, but INITI is invalid).

If a command is shown in square brackets, it is an implied command and can be omitted (the brackets are not part of the command and should be omitted even if the command itself is entered). An implied command is the default command among the commands available at its level. For example, in the case of the command INITiate:[IMMediate], the immediate mode is the default mode, so entering INIT has the same effect as entering INIT:IMM.

Because you can query any value that you can set, most commands also exist in a query form (signified by adding a question mark to the end of the keyword). The command tables do not contain separate listings for queries except in the case of commands that exist only in the query form. If there is a command ALPHA, you can assume that there is also an ALPHA? query unless the table entry includes the statement NO QUERY. Some commands are events that cause something to happen at a particular time but do not create a setting or value to be checked afterwards. Consequently, they have no query form.

Some commands require a parameter. The parameter types are:

BOOL:A Boolean (true or false) condition. Enter

ON or 1 for TRUE;
OFF or 0 for FALSE.

VAL:A numeric value or a qualitative term which represents a numeric value. Enter:

sign (optional),
digits,
decimal point (optional),
E xx (optional),
units suffix (optional).
Or enter MIN, or MAX.
Or enter UP, or DOWN (these only change the synthesizer's output frequency or output power level).

NUM:A number (typically represents register bit settings in the form of a decimal integer).

There are also discrete parameters. These are options to be chosen from a limited selection. For example, the TRIGger:SLOPe command has three possible discrete parameters to chose from (POSitive, NEGative, and NONe). The beginning of a parameter must be preceded by a space. The default units suffixes are DBM for power and HZ for frequency (the other suffixes for frequency are GHZ, MHZ, and KHZ).

2.5.2 SCPI Commands

Tables 2-13 through Table 2-17 list the SCPI commands with notes on parameter types, initial values, and whether or not a query form of the command exists. The effect of the command is explained below each command listing. Many of these commands refer to the Status System, which is discussed in detail in Section 2.6. Commands beginning with an asterisk are IEEE-488.2 Common Commands.

Table 2-13: SCPI Commands CLS - TST

Keyword	Parameter Type	Initial Value	Query Form?
*CLS	none	none	no
(Clear Status Command) This command clears the event registers in all status groups. It also clears the Event Status Register and the Error/Event Queue.			
*ESE	NUM	0	yes
(Standard Event Status Enable Command) This command make it possible for specified changes in the Standard Event Status Register to generate service requests. The query form (*ESE?) determines which changes in the Standard Event Status Register have been enabled to generate service requests. The parameter is a decimal number which represents the register's bit settings.			
*ESR?	none	0	query only
(Standard Event Status Register Query) This command causes the event register of the Standard Event Status Register group to be read and transmitted over the bus	It also causes the register to be cleared.		
*IDN?	none	none	query only
(Identification Query) The response takes the form of four ASCII fields separated by commas. The fields are: (1) Manufacturer, (2) Model, (3) Serial Number, and (4) Firmware Level or Equivalent. Fields 1 and 2 are required; fields 3 and 4 are filled by zeros if the data is not available.			
*OPC	none	none	yes
(Operation Complete Command) This command causes the Operation Complete bit (that is, Bit 0 of the Standard Event Status Register) to be set to 1 when all pending selected device operations have been finished. The query form (*OPC?) places an ASCII character 1 into the device's output queue when all pending selected device operations have been finished. Unlike the *OPC command, the *OPC? query does not affect the OPC Event bit in the Standard Event Status Register (ESR).			
*RST	none	none	no
(Reset Command) This command sets the device-specific functions to a known state (the power-on state) that is independent of the past-use history of the device. The command does not reset any part of the status reporting system.			
*SRE	NUM	0	yes
(Service Request Enable Command) This command makes it possible for service requests to be generated by specified bits of the Status Byte Register. The query form (*SRE?) determines which bits of the Status Byte Register have been enabled to generate service requests.			
*STB?	none	none	query only
(Status Byte Query) This command causes the event register of the Status Byte Register group to be read and transmitted over the bus. It also causes the register to be cleared.			
*TST?	none	none	query only
(Self-Test Query) This command causes the synthesizer to perform a self-test routine. See the notes below concerning Self-Test.			

Notes on Self-Test Commands

The Self-Test routine will preserve (save and later restore) these states:

- RF On/Off State
- CW Frequency Value
- Power Level Coarse Value
- Power Level Fine Value

The test routine will then switch in the maximum step attenuation before beginning the test to prevent damage to any user circuitry at the RF output connector. The Power Level (Fine) value during the test will be the maximum output value for the unit (usually +10 dBm), but the Power Level (Coarse) value is set to -90 dB. The output power at the RF connector is the sum of the two, which is still so small that it presents no risk of damage to connected devices.

The synthesizer will go to TEST:FREQuency:BEGin (the default value is the minimum frequency) and check for lock and level. If lock and level are OK, the frequency increment specified by TEST:FREQ:STEP (default: 1 GHz) will be added in order to calculate the next frequency, and the lock and level checks will be made again. If the calculated frequency exceeds TEST:FREQuency:END, the synthesizer will be set to that end frequency instead.

If there are no errors, the test ends when the frequency just tested equals the frequency specified by TEST:FREQuency:END. The saved entry states are restored, and a value of 0 is returned.

If there are errors, the test stops at the frequency where the errors occurred and saves that frequency as TEST:FREQuency:QUIT. The saved entry states are restored and a decimal error code is returned. To determine which bits are ON from the decimal error code, refer to Registers, Bit Numbers and Decimal Weights (Section 2.6.2). The bit meanings are:

Bit 0: (not used)
Bit 1: (not used)
Bit 2: 80 MHz PLL locked/unlocked status
Bit 3: 300 MHz PLL locked/unlocked status
Bit 4: Output PLL locked/unlocked status
Bit 5: 110 MHz PLL locked/unlocked status
Bit 6: Downconverter PLL locked/unlocked status
Bit 7: Level Control leveled/unleveled status

If you inadvertently enter a very small step size and then start the test running, the TEST:ABORt command provides a means of terminating the test before completion. The test is simply stopped. Even though you had issued the *TST? command (a query), no reply will occur after abort. You must manage the clearing of your expected reply.

For any of the above outcomes, a query of TEST:FREQuency:QUIT? will give the value of the last frequency used in the test.

Table 2-14: SCPI Commands WAI - OUTput

Keyword	Parameter Type	Initial Value	Query Form?
*WAI	none	none	no
(Wait-to-Continue Command) This command prevents the instrument from executing any further commands or queries until all pending selected device operations have been finished. The *RST and *CLS commands have no effect on the operation of the *WAI command.			
ABORt	none	none	no
The abort command causes the instrument to abort all current processes (the only applicable process in the Series 50000B would be a frequency sweep).			
INITiate [:IMMediate]	none	none	no
:CONTinuous	BOOL	OFF	no
The initiate command specifies the execute form (the method by which a process is initiated). The applicable process in the Series 50000B is a frequency sweep, and the command should be issued only after all sweep conditions have been set up. If the INITiate[:IMMediate] command is sent, the synthesizer is armed to perform a single sweep, which will occur upon receipt of a hardware trigger or a TRIGger command, but is not retriggerable (this is the default execute form). If the CONTinuous command is sent (with the parameter ON), the synthesizer is set up for a sweep which is retriggerable (that is, when a sweep has been triggered and comes to an end, it can be started again by means of a hardware trigger or a TRIGger command).			
OUTPut [:STATe]	BOOL	OFF	yes
This command activates or deactivates the synthesizer RF output. The query form (OUTPut:STATe?) discovers the ON/OFF status of the RF output.			

2.5.3 SCPI Source Commands

All commands in Table 2-15 begin with [SOURce], but as [SOURce] is the default command at the root level it need not be entered.

Table 2-15: SCPI SOURce Commands

Keyword	Parameter Type	Initial Value	Query Form?
[SOURce] :AM :STATe	BOOL	OFF	yes
This command activates or deactivates the AM mode. The query form (:AM:STATe?) identifies the present ON/OFF status of the AM mode.			
:FM :STATe	BOOL	OFF	yes
This command activates or deactivates the FM mode. The query form (:FM:STATe?) identifies the present ON/OFF status of the FM mode.			
:FREQuency [:CW] or: [:FIXed]	VAL HZ (or choose from: MIN, MAX, UP, or DOWN)	MIN	yes
:STEP [:INCRement]	VAL HZ	1E9	yes
:MODE	Choose from: CW, FIXed, SWEep, or LIST	CW	yes
:STARt	VAL HZ	MIN	yes
:STOP	VAL HZ	MAX	yes
Frequency commands specify frequencies, and operating modes relating to frequency. See the notes below concerning frequency commands.			

Notes on Frequency Commands:

1. The commands :FREQuency[:CW] and :FREQuency[:FIXed] are synonymous; either command specifies a fixed frequency for the synthesizer.
2. The command :FREQuency[:CW]:STEP[:INCRement] specifies a frequency step size for sweeping or for UP/DOWN incrementing.
3. The command :FREQuency:MODE chooses a frequency mode. The choices are CW and FIXed (both of which mean a fixed frequency), SWEep (which means a sequence of frequencies progressing from low to high at a specified rate) and LIST (which means a sequence of frequencies specified by the contents of a series of memory locations).

FREQuency:MODE SWEep

This command sets up the normal increment mode (add the step size to the last frequency). The following commands apply to this mode:

FREQuency:STARt	Start frequency (inclusive)
FREQuency:STOP	Stop frequency (inclusive)
SWEep:STEP	Step size

SWEep:DWELl Dwell time

FREQuency:MODE LIST

This command sets up the memory list increment mode (select the next nonzero frequency in the array). The following commands apply to the list mode:

Table 2-15: SCPI SOURce Commands (Continued)

Keyword	Parameter Type	Initial Value	Query Form?
[SOURce] :LIST :FREQuency	VAL HZ	none	yes
This command sets the value of the next frequency (index numbers 0 - 9) on the list in memory. The default index is 0. When a value is entered, the index automatically increments, up to a ceiling value of 9. The query form (:LIST:FREQuency?) checks the frequency list as follows. First, send the command :LIST:FREQ:POIN 0 to restore the index to 0. Then read the list by sending a series of :LIST:FREQ? queries. Each query causes the index to increment, up to a ceiling value of 9.			
:LIST :FREQuency :POINts	NUM	0	yes
This command changes the current index number (0 - 9) for the frequency list in memory. The query form (:LIST:FREQuency:POINts?) identifies the current index number (that is, the index number of the next frequency to be entered).			
:POWer [:LEVel] [:IMMediate] [:AMPLitude]	VAL dB (or choose from: UP, or DOWN)	0	yes
This command specifies the synthesizer's output power level in dB. The query form (:POWer[:LEVel][:IMMediate][:AMPLitude]?) identifies the present power level.			
:POWer [:LEVel] [:IMMediate] [:AMPLitude] :STEP [:INCRement]	VAL dB	1	yes
This command specifies the power step size (in dB) for UP/DOWN incrementing. The query form (:POWer[:LEVEL][:IMMediate][:AMPLitude]:STEP[:INCRement]?) discovers the present step size.			
:PULM :STATe	BOOL	OFF	yes
This command activates or deactivates the pulse modulation mode. The query form (:PULM:STATe?) identifies the present ON/OFF status of the pulse modulation mode.			
:SWEep :DWELl	VAL SC	1	yes
This command specifies the dwell time for frequency sweeping. The query form (:SWEep:DWELl?) determines the present dwell time.			
:SWEep :STEP	VAL HZ	1E9	yes
This command specifies the step size for frequency sweeping. The query form (:SWEep:STEP?) identifies the present step size.			

2.5.4 SCPI Status Commands

All commands in Table 2-16 relate to the status monitoring system and read from and/or write to the various status group registers.

The event and condition registers are read-only. The enable registers and transition filters are read/write. Each status group's transition filter actually contains two filters, one to detect positive-going transitions (PTR) and one to detect negative-going transitions (NTR).

Data is in the form of a decimal number, which (when decoded to an 8-bit binary number) indicates the On/Off status of individual data bits.

Table 2-16: SCPI Status Commands

Keyword	Parameter Type	Initial Value	Query Form?
STATus :OPERation [:EVENt?]	none	none	query only
:CONDition?	none	none	query only
:ENABle	NUM	255	yes
:PTRansition	NUM	255	yes
:NTRansition	NUM	255	yes
The STATus:OPERation commands relate to the registers of the operational status group.			
STATus :QUEStionable	none	none	yes
[:EVENt?]	none	none	query only
:CONDition?	none	none	query only
:ENABle	NUM	255	yes
:PTRansition	NUM	255	yes
:NTRansition	NUM	255	yes
The STATus:QUEStionable commands relate to the registers of the questionable status group.			
STATus :QUEStionable :POWer	none	none	yes
[:EVENt?]	none	none	query only
:CONDition?	none	none	query only
:ENABle	NUM	255	yes
:PTRansition	NUM	255	yes
:NTRansition	NUM	255	yes
The STATus:QUEStionable:POWer commands relate to the registers of the questionable power status group.			

Table 2-16: SCPI Status Commands (Continued)

Keyword	Parameter Type	Initial Value	Query Form?
STATus :QUEStionable :POWer	none	none	yes
[:EVENt?]	none	none	query only
:CONDition?	none	none	query only
:ENABle	NUM	255	yes
:PTRansition	NUM	255	yes
:NTRansition			
The STATus:QUEStionable:POWer commands relate to the registers of the questionable power status group.			
STATus :QUEStionable :FREQuency	none	none	yes
[:EVENt?]	none	none	query only
:CONDition?	none	none	query only
:ENABle	NUM	255	yes
:PTRansition	NUM	255	yes
:NTRansition	NUM	255	yes
The STATus:QUEStionable:FREQuency commands relate to the registers of the questionable frequency status group.			
STATus :PRESet	none	none	no query
The STATus:PRESet command restores all parts of the status monitoring system to the power-on/reset condition.			

Table 2-17: SCPI Miscellaneous Commands

Keyword	Parameter Type	Initial Value	Query Form?
SYSTem :ERRor?	none	none	query only
:VERSion?	none	none	query only
The SYSTem:ERRor command reads the Error/Event Queue. The SYSTem:VERSion command discovers the release number of the installed firmware.			
:LANGuage	Choose from: CIIL, or HP	none	no query
This command switches from the SCPI syntax to the CIIL or HP syntax. The appropriate commands within those syntaxes must be used to restore the SCPI syntax.			
:LANGuage:HP (command line)	HP-syntax command line	none	no query
This command issues an HP-syntax command line for immediate execution from within SCPI without leaving the SCPI syntax. It is useful primarily for sending an LAx command to change the local address to which the Giga-tronics controller sends subsequent commands. However, any valid HP-syntax command line can be entered including multiple commands separated by semicolons. NOTE: Some HP-syntax commands cause characters to be returned to the controller.			
TEST [:FREQuency] [:QUIT?]	VAL HZ	none	query only
:BEGin	VAL HZ (or choose from: MIN, or MAX)	MIN	yes
:END		MAX	yes
:STEP	VAL HZ	1E9	yes
These commands specify or discover frequency-related factors for the self-test routine (see the *TST? query). The TEST[:FREQuency][:QUIT?] query is used after a test has been run to identify the frequency at which the test concluded. The TEST[:FREQuency]:BEGin command specifies the starting frequency of the test. The query form (TEST[:FREQuency]:BEGin?) discovers the starting frequency. The TEST[:FREQuency]:END command specifies the ending frequency of the test. The query form (TEST[:FREQuency]:END?) discovers the ending frequency. The TEST[:FREQuency]:STEP command specifies the frequency step size for the test. The query form (TEST[:FREQuency]:STEP?) discovers the step size.			
TEST :POWer [:FINe]	VAL dB	+10	yes
:COARse	VAL dB	-90	yes
These commands set up the conditions of the self-test routine (see the *TST? query). The TEST:POWer[:FINe] command specifies the fine power setting for the test in dB. The query form (TEST:POWer[:FINe?) discovers the fine power setting. The TEST:POWer:COARse command specifies the coarse power setting for the test in dB. The query form (TEST:POWer:COARse?) discovers the coarse power setting.			
TEST :ABORt	none	none	yes
This command halts the self-test routine (see the *TST? query).			

Table 2-17: SCPI Miscellaneous Commands (Continued)

Keyword	Parameter Type	Initial Value	Query Form?
TRIGger [:IMMediate]	none	none	no query
:SLOPe	Choose from: POSitive, NEGative, or NONe	NONe	yes
The trigger commands specify the execute mode (the method of triggering a process). The applicable process in the Series 50000B is a frequency sweep. The TRIGger[:IMMediate] command causes a sweep that was awaiting a trigger to commence. The TRIGger:SLOPe command defines the conditions that will trigger a sweep, depending on which of three options is used as a parameter. If the parameter is POSitive, the sweep will be triggered upon receipt of the INITiate command followed either by a hardware trigger level of TRUE (+5 Volts), or by the TRIGger command. If the parameter is NEGative, the sweep will be triggered upon receipt of the INITiate command followed either by a hardware trigger level of FALSE (0 Volts), or by the TRIGger command. If the parameter is NONe, the sweep will be triggered upon receipt of the INITiate command followed by the TRIGger command (no hardware triggering).			

2.5.5 SCPI/HP Equivalent Commands

To get to the SCPI syntax from the HP syntax, type SCPI. To get back, use the SYST:LANG HP command from Table 2-17. Here is a comparison of commands that do the same thing in each language:

Table 2-18: SCPI/HP Equivalent Commands

SCPI Command	Equivalent HP Command
FREQ 6.1 GHz	CW6.1 GZ
POW -9.2	PL-9.2
OUTP ON	RF1
AM:STAT ON	AM1
FM:STAT ON	FM1
PULM:STAT ON	PM1
FREQ?	OPCW
POW?	OPPL

2.5.6 Sample SCPI Commands

Table 2-19 shows some examples of brief SCPI commands:

Table 2-19: Sample SCPI Commands

Command	Meaning
*IDN?	Query instrument identification (response format: maker,model,serial#,firmware version; (sample response: Giga-tronics,50000,048256,75).
*RST	Reset system.
OUTP OFF	Turn off RF output.
AM:STAT OFF	Turn off external amplitude modulation.
AM:STAT?	Query external amplitude modulation (sample response: 0).
POW -9.2	Set output power to -9.2 dBm.
POW?	Query output power (sample response: -9.2).
FM:STAT OFF	Turn off external frequency modulation.
FM:STAT?	Query external frequency modulation (sample response: 0).
FREQ 6.1GHZ	Set output frequency to 6.1 GHz
FREQ?	Query output frequency (sample response: 6100000000).
PULM:STAT OFF	Turn off external pulse modulation.
PULM:STAT?	Query external pulse modulation (sample response: 0).

2.6 SCPI Status System

2.6.1 Introduction

The SCPI standard includes a system for monitoring the status of the instrument. Much of this status system is imported from the IEEE-488.2 standard. Status monitoring is accomplished by means of several registers which can be read from (or in some cases written to). Registers of various kinds are combined into status groups and the status groups are nested: the output bits of a status group are summarized by a logical-OR gate. The summary output becomes one of several inputs to another status group. The various groups and registers are described in detail below.

SCPI terminology is not consistent. The distinction between a register and a group of registers is often ignored. Some status groups are called status registers. This manual does not attempt to correct SCPI's choice of words, but confusions of this kind will be pointed out where they occur.

2.6.2 Registers, Bit Numbers, and Decimal Weights

When a register is read, its bit settings are converted into a single decimal number for transmission over the interface. The decimal weights for the various bits are shown in Table 2-20 below:

Table 2-20: Bit Numbers and Decimal Weights

Bit:	7	6	5	4	3	2	1	0
Weight:	128	64	32	16	8	4	2	1

If Bit 0 (the least significant bit) is ON, its weight is 1. If Bit 7 (the most significant bit) is ON, its weight is 128. If 0 and 7 were the only bits ON, the register would have a decimal value of 129 (the sum of the weights). If all bits were ON, the register would have a decimal value of 255.

NOTE: *Although SCPI defines some registers as having 16 bits, Giga-tronics makes use of only the lowest 8 bits of any register. Therefore, every register can be treated as if it contained only 8 bits.*

To determine which bits are on from the decimal value, find the largest weight that does not exceed the decimal value. Subtract that weight from the value and mark that bit ON. Continue subtracting weights, and marking the associated bits ON until the decimal value is reduced to zero.

EXAMPLE:

The decimal value is 235.
Subtract 128 and mark Bit 7 ON. The decimal value is now 107.
Subtract 64 and mark Bit 6 ON. The decimal value is now 43.
Subtract 32 and mark Bit 5 ON. The decimal value is now 11.
Subtract 8 and mark Bit 3 ON. The decimal value is now 3.
Subtract 2 and mark Bit 1 ON. The decimal value is now 1.
Subtract 1 and mark Bit 0 ON. The decimal value is now 0.
Conclusion: Bits 7, 6, 5, 3, 1, and 0 are ON. Bits 4 and 2 are OFF.

This procedure is done in reverse in order to convert bit settings to a decimal value. Add together the decimal weights (as shown in Table 2-20) for each bit which is ON to find the equivalent decimal value.

EXAMPLE:

Bits 6, 2, and 0 are ON.
Add the decimal weights (64 + 4 + 1) that are associated with those bits.
The decimal value is 69.

2.6.3 Status Group (Generalized Status Register Model)

Figure 2-2 shows how registers are typically combined to form a status group. The group consists of a condition register, a transition filter, an event register, and an enable register. (However, some status groups do not use the condition register or the transition filter.)

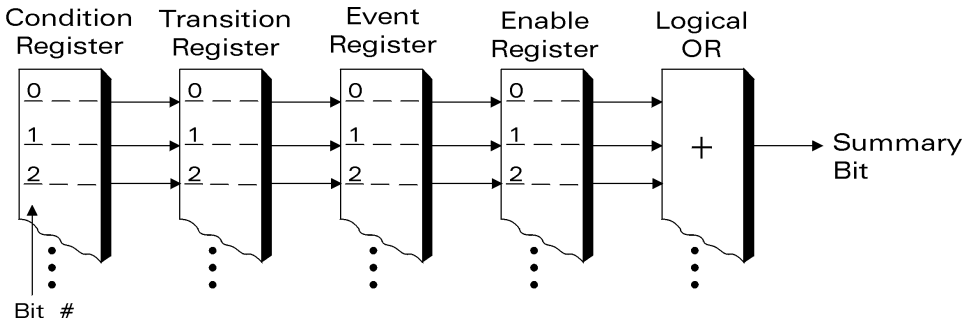


Figure 2-2: Status Group

The condition register continuously monitors the hardware and firmware status of the instrument. There is no latching or buffering for this register. It is updated in real time. The condition register is read-only. A 1 (ON) bit indicates an abnormal state.

The transition filter specifies which types of bit state changes in the condition register will set corresponding bits in the event register. Transition filter bits can be set for positive (0 to 1), negative (1 to 0), or both. Transition filters are read-write and are unaffected by *CLS or queries. They are set to all bits both at power on and after *RST.

The event register latches transition events from the condition register as specified by the transition filter. Bits in the event register are latched and once set, they remain set until cleared by a query or *CLS (clear status). There is no buffering, so while an event bit is set, subsequent events corresponding to that event are ignored. Event registers are read-only.

The enable register specifies which bits in the event register can generate a summary bit. A 1 bit in the same position in both the enable and event registers will cause a summary bit to be set. Summary bits are, in turn, recorded in another status group. Enable registers are read-write. Enable registers are not affected by *CLS (clear status). Querying enable registers does not affect them.

The processor in the Controller module is monopolized by the VXI Zero Slot Controller much of the time. It can process changes in condition registers only when the Series 50000B is executing a command addressed to it. When the processor receives a command, it compares the states of the condition registers at that time to their states as recorded when the last command was received and applies the transition filter to these state changes. To capture changes more frequently, send Read Status Byte queries (*STB?) periodically.

2.6.4 Status Byte Register

Figure 2-3 illustrates the status byte register (which is actually a status group, with no condition register or transition filter):

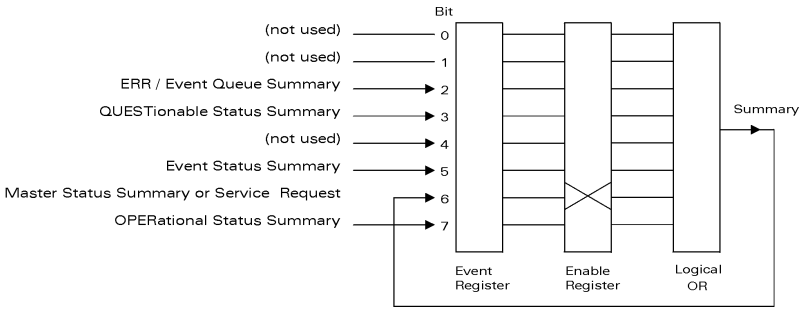


Figure 2-3: Status Byte Register

The individual bits are defined as follows:

Bit 2 (Err/Event Queue Summary)

This bit goes high to indicate that an error message has been stored in the Error/Event Queue.

Bit 3 (QUEStionable Status Summary)

This is the summary bit from the QUEStionable Status Group.

Bit 5 (Event Status Summary)

This is the summary bit from the Standard Event Status Group.

Bit 6 (Master Status Summary, or Service Request)

This is feedback from the summary bit of the Status Byte group itself. Because this is the final or most summarized status group, its summary bit is not furnished to a higher register. Instead, the summary bit is returned to Bit 6 of the Event Register. It is blocked at the Enable Register from affecting the OR-gate summary. The condition of the summary bit must be determined by reading the Status Byte Register and determining whether or not Bit 6 is on (alternatively, the system can be set up so that a Service Request interrupt is issued to the controller whenever the summary bit goes high).

Bit 7 (OPERational Status Summary)

This is the summary bit from the OPERational Status Group. The applicable 488.2 Common Commands are:

*SRE Service Request Enable command
*SRE? Service Request Enable query
*STB? Read Status Byte query

If all service requests are disabled with the command *SRE 0, then the query *SRE? will produce the reply 0. If the Status Byte register had only the Event Status summary bit ON, then the query *STB? would return 32 (because that is the decimal weight of bit 5 alone). If the command *SRE 32 is now sent to enable service requests for the Event Status summary bit, the query *SRE? will confirm by replying 32. The query *STB? would now return 96 because both the Event Status summary bit (weight 32) and the Require Service bit (weight 64) are ON. The Status Byte register is not cleared after it is queried. The primary causes of the bit settings must change in order for the bits to change.

2.6.5 OPERational Status Group

The diagram below illustrates the OPERational Status Group.

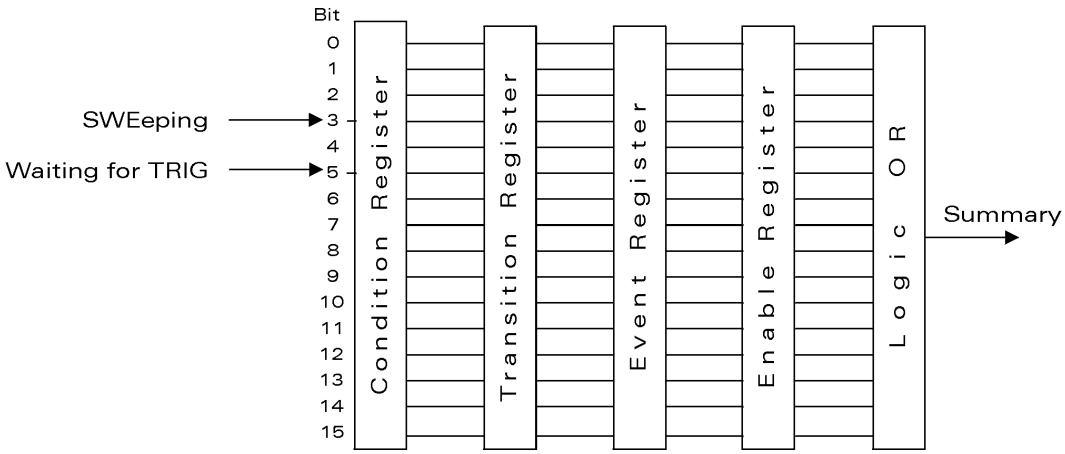


Figure 2-4: OPERational Status Group

Only two of this status group's bits are actually used:

Bit 3 (SWEeping)

This bit goes high when the synthesizer is performing a frequency sweep.

Bit 5 (Waiting for TRIG)

This bit goes high when the synthesizer is in the frequency sweep mode and is awaiting a hardware trigger input.

2.6.6 Standard Event Status Register

This is actually a status group as illustrated below. It includes the event and enable registers but not the condition register or the transition filter:

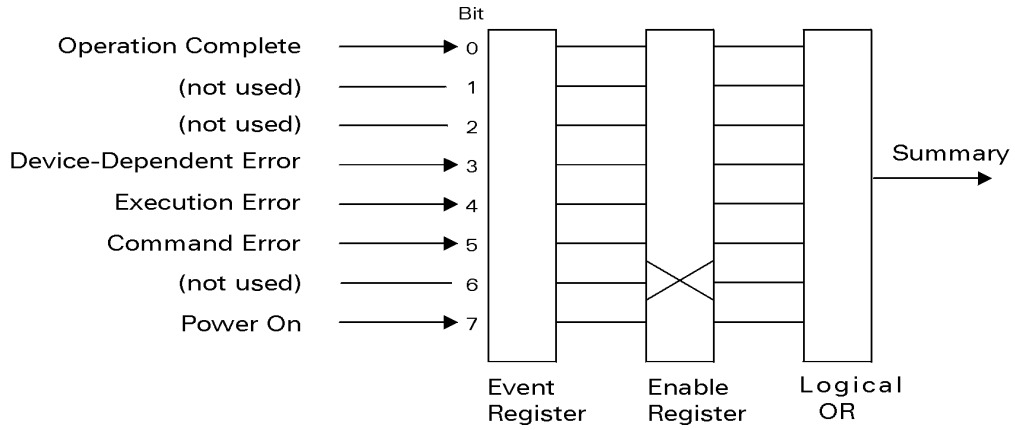


Figure 2-5: Standard Event Status Register

Individual bits of this register are defined as follows:

Bit 7 (Power On)

This event bit indicates that an off-to-on transition has occurred in the device's power supply.

Bit 5 (Command Error)

The parser detected a syntax or semantic error. This is usually caused by an unrecognized header or attempted query of a command-only header.

Bit 4 (Execution Error)

Probably an input data value was out of range or some device condition prevented an otherwise valid command from being executed.

Bit 3 (Device Dependent Error)

The device detected an error which was not one of those already described.

Bit 0 (Operation Complete)

This event bit is generated in response to the *OPC command. It indicates that the device has completed all selected pending operations. (Note that this bit is NOT set as a response to the query form of the command, *OPC?).

The applicable 488.2 Common commands are:

*ESE	Standard Event Status Enable command
*ESE?	Standard Event Status Enable query
*ESR?	Standard Event Status Register query

Reading the Standard Event Status Register with the *ESR? query also clears the register as does power up or the *CLS command.

2.6.7 QUEStionable Status Group

Figure 2-6 shows the entire status group in detail. The raw condition bits for STATus:QUEStionable:POWer and STATus:QUEStionable:FREQuency go through the transition filter to become event bits. These then match their counterparts in the enable register to contribute to the logical OR for the summary bit. The summary bit then becomes a raw bit in the condition register of the next higher level: the STATus:QUEStionable group.

The STATus:QUEStionable:POWer group uses a single bit to represent the leveled/unleveled status of the synthesizer's level control circuit (a 1 or ON bit indicates the unleveled state).

As shown in Figure , the STATus:QUEStionable:FREQuency group uses five bits to represent the locked/unlocked status of five different phase lock loops (a 1 or ON bit indicates an unlocked loop). To query the event register of the STATus:QUEStionable:FREQuency group, use the command line STATus:QUEStionable:FREQuency:EVENt? On receiving the decimal number reply, refer to Registers, Bit Numbers, and Decimal Weights (Section 2.6.2) to determine which bits are ON.

Remember that you must query an event register or issue the general *CLS command to zero the event register's ON bits.

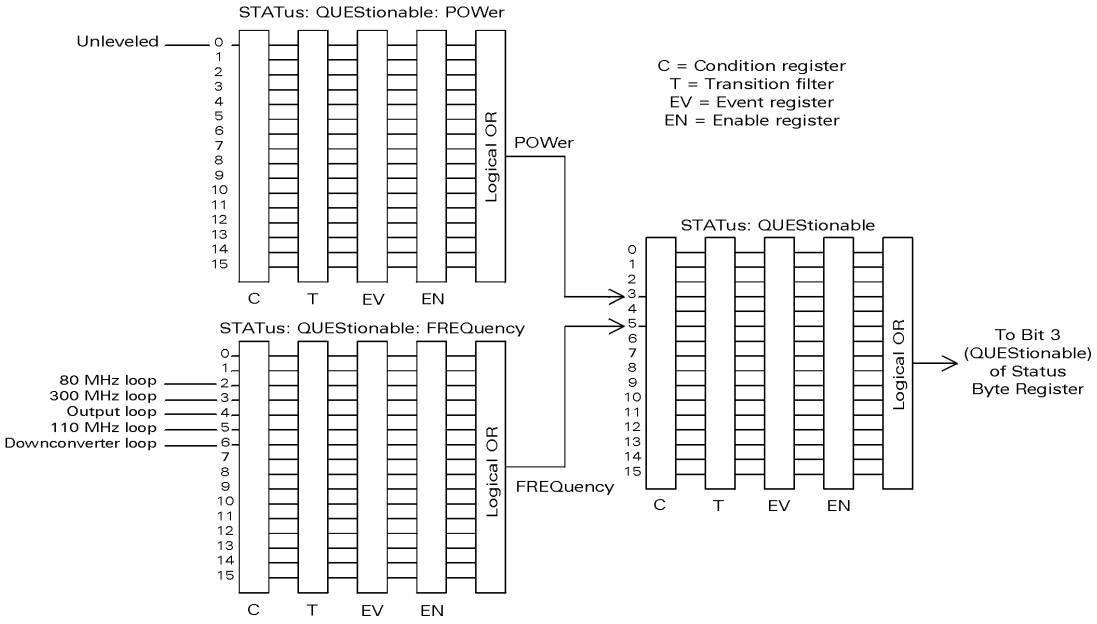


Figure 2-6: Questionable Status Group

2.6.8 Overview of the SCPI Status System

Figure 2-7 provides an overview of the entire status system. You can customize the status reporting (so that only certain conditions of interest are reported) by writing to the enable registers. The broadest stroke would result from the Status Byte Enable Register using the command *SRE. Then only the conditions which set bit 6 (the Master Summary, or Request Service) bit can be seen, using either the *STB? command or a service request mechanism.

The event status enable command *ESE performs the same function for that register. Enable registers within a status group can be set using, for example, STATus:QUEStionable:ENABle.

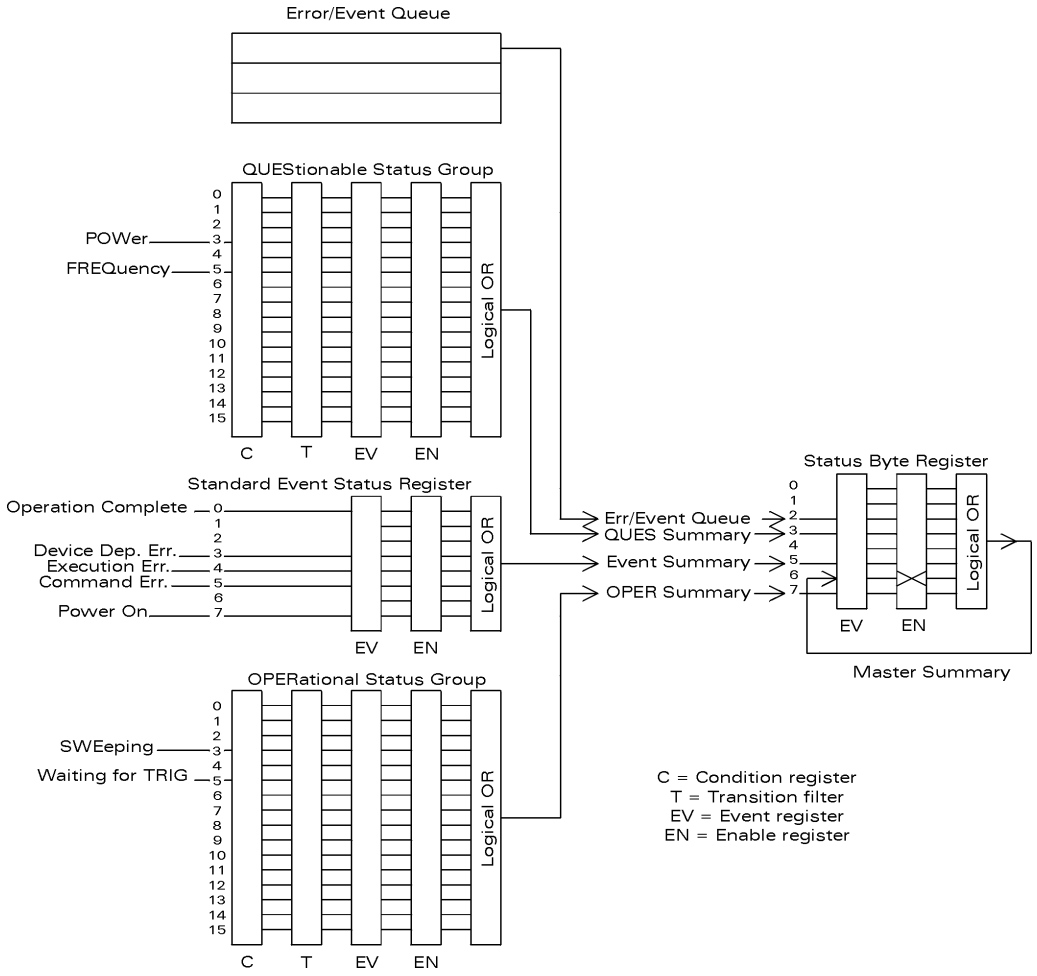


Figure 2-7: Overview of the SCPI Status System

2.7 Giga-tronics Syntax

The Giga-tronics syntax is partially implemented in the 50000B Series. The following commands are supported:

Table 2-21: Giga-tronics Command Syntax

Command	Description
CORRECTIONOFF	Amplitude correction factors disabled
CORRECTIONON	Amplitude correction factors enabled
FA	Set CW Frequency (requires value, in MHz)
GENFIXED	Generate CW frequency
HP	Switch to HP language
LEVEL	Set output power level (requires value, in dBm)
SENDSTATUS	Outputs status of unit
STEPATTENUATOROFF	Step attenuator disabled
STEPATTENUATORON	Step attenuator enabled

3

Theory of Operation

3.1 System Configuration

The Giga-tronics VXI Microwave Synthesizer System includes a VXIbus-compatible Controller module, which runs up to eight functional modules over the VXI local bus. The Slot Zero controller communicates with the Controller module over the VXIbus. The Controller module in turn communicates with the functional modules over the local bus. Functional modules include the Synthesizer module (there can be more than one) and optional modules, which might be installed to perform special functions. Apart from the local bus lines and power supplies, the functional modules do not use the VXI bus.

Giga-tronics configures the twelve lines of the local bus as follows: Bit 0 is the Data Strobe line, Bit 1 is the Data Direction line, Bit 2 is unused, Bit 3 is the Address Strobe line, and the remaining 8 bits are used both as an address byte and a data byte. Since all the Giga-tronics modules are on the same local bus lines, the Controller module must specify the address of a functional module in order to communicate with it. Each functional module may have up to 15 internal registers where commands are stored. In most cases these registers are simply latches. In a few cases they are devices such as Digital/Analog converters, which require multiple bytes of data.

Each command from the controller module to a functional module is preceded by the unique address of the target module and the register in that module. The high half-byte (that is, bits 4 through 7) of the address/data byte selects the appropriate module, while the low half-byte (that is, bits 0 through 3) contains the address of the internal register. Once the register has been addressed, the data byte is sent to and stored in the register. Registers requiring multiple data bytes have their own internal protocol to change the affected parameter only when the data is complete. One of the registers in each module contains status information. This register may be read by the Synthesizer Controller module in response to queries received over the VXIbus. The status register has eight bits and is configured to match the requirements of the individual module.

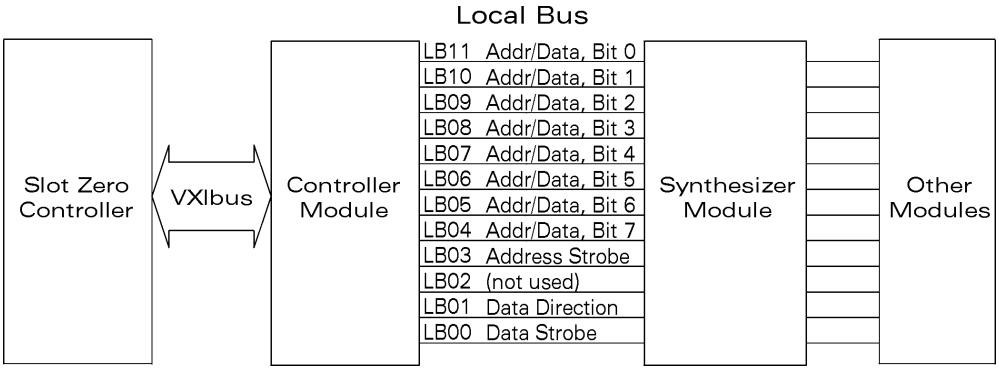


Figure 3-1: The VXIbus and the Local Bus

3.1.1 Control Module

The primary function of the Control module is to serve as an interface between the functional modules and the VXIbus. This module does not have the functions of a slot zero controller. It is a message-based instrument as far as the VXIbus is concerned. Commands sent to it are interpreted by its internal 68000-based computer, and passed on to the various Giga-tronics function modules via the local bus. The computer handles all VXIbus protocol requirements.

A dedicated interface circuit, connected to the 68000 bus structure, adds additional memory and the address decoding required to drive the VXI local bus. Another printed circuit assembly contains the temperature compensated crystal oscillator, which serves as the internal synthesizer timebase.

The remaining circuit in the module produces reference frequencies which are supplied to each of the Synthesizer RF modules. A 110 MHz crystal oscillator is divided by 11 and phase-locked to the 10 MHz timebase. The output of this 110 MHz oscillator is then multiplied by three to produce a 330 MHz reference frequency. The 10 MHz and 330 MHz outputs are buffered and supplied to the front panel connector.

3.1.2 The RF Path

The RF path is those elements from the YIG oscillator to the RF output connector. A variety of operations take place along this path (i.e., coupling, leveling, modulation, filtering and attenuation of the output signal). The clustering of most of those functions into one module greatly reduces the power loss inherent in designs requiring multiple transitions and connectors.

RF Module

The RF module sends (by way of microstrip couplers) samples of the RF output signal that are required by two circuits outside the RF path: the output phase lock loop and the level control circuit.

The leveler circuit, consisting of PIN diodes, functions as a variable attenuator. A signal from the level control circuit regulates current through these diodes in order to adjust output power.

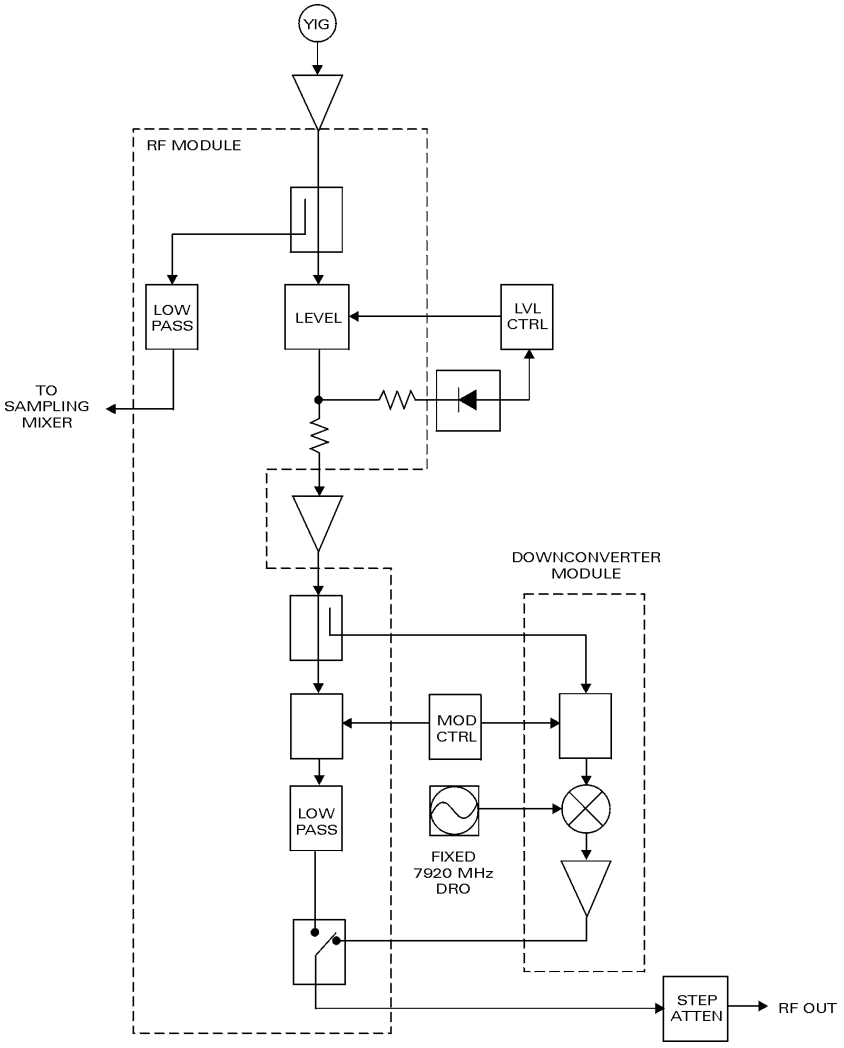


Figure 3-2: The RF Path

RF Module Input

Since the output of a YIG oscillator is not spectrally pure, harmonics of the fundamental frequency are usually present at amplitudes of -12 to -20 dBc. Low-pass filters consisting of shaped microstrip elements are used to reduce these harmonics. The path through the RF module is subdivided into one of five filter lines, depending on the output bandwidth. The switching of these paths is performed by PIN diode circuits, rather than by mechanical switches, for increased reliability.

RF Module Output

Filter switch circuits are also used to pulse-modulate the RF output. (The pulse modulation input is applied to the switch that controls the appropriate filter line).

The output of the RF module is applied to an optional 10 dB step attenuator connected directly to the front panel. Connections between components in the RF path are made through semi-rigid coaxial cable.

3.2 Amplitude Control

Amplitude control of the Synthesizer output is adjusted by a combination of fixed-step attenuation and closed-loop leveling (in the ALC). The fixed-step attenuation is done by a step attenuator providing up to 90 dB of attenuation in 10 dB increments. Closed-loop leveling is accomplished through Automatic Leveling Control (ALC), which provides fine adjustment in 1 dB increments.

3.2.1 The ALC Circuit

The ALC is basically a loop amplifier with multiple inputs. One of the inputs takes fee dBack from the level detector (a circuit that returns a negative voltage proportional to the square of detected power). The RF measured by the detector is coupled from the output path by a circuit in the RF module. The detector signal is amplified and applied to the summing junction of the leveling loop amplifier; it is a variable input in that it changes in response to the loop amplifier output.

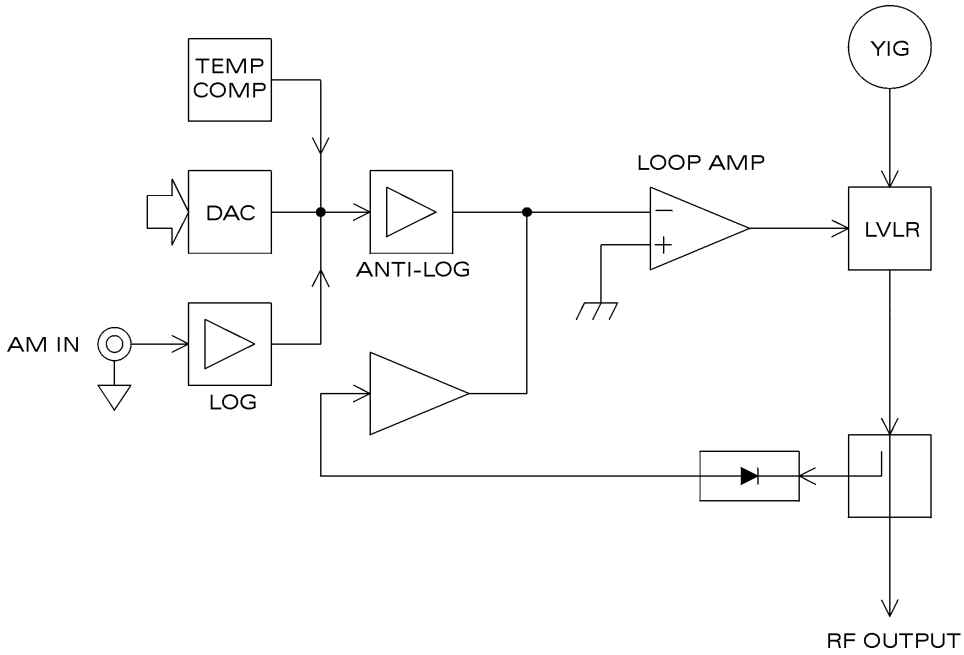


Figure 3-3: Amplitude Control

Another input into the ALC is the reference input. The reference input is a composite of three signals: a correction voltage from the temperature compensation circuit (PC board A3), a fixed leveling input (which the Control module programs by means of a digital to analog converter) and the AM signal from the front panel input. If present, the AM signal is processed by a logarithmic amplifier in order to give it the same logarithmic characteristic as the other two inputs. Then, all three signals can be combined by a summing amplifier; the combined signal is processed by an anti-logarithmic amplifier on its way to the loop amplifier.

The ALC output is sent to an amplifier which drives the PIN diode leveler so as to balance the reference input against an equal and opposite variable fee dBack input. In other words, the leveler adjusts RF power until the detector fee dBack input just cancels the other input to the loop amplifier.

In setting the leveling reference, through the programming of a digital to analog converter, the Control module includes compensation factors from a level-characterization table (stored in a PROM in the Synthesizer module). This data is individual to each synthesizer system and is compiled during production testing.

3.2.2 Amplitude Modulation

The AM input to the level control circuit supplies the leveling loop amplifier with a variable, rather than a fixed leveling reference. The variable reference is processed by a log amplifier in order to match the logarithmic characteristics of the computer leveling reference and the temperature compensation input. The level control circuit furnishes a modulated control voltage to the leveler in the RF module to match the modulation of the reference input. The result is an amplitude modulated RF output with a modulation depth of at least 20 dB.

3.3 Pulse Modulation

Pulse modulation is performed by means of path-switching circuits in the RF module. Depending on output bandwidth, there will be up to five filter paths through the module (only one is active at a given time). PIN diode circuits switch these lines on and off; pulse modulation is accomplished by shutting off the active path intermittently. (A positive voltage at the filter line control pin on the outside of the module shuts the path off.) By this method, an on/off ratio of greater than 80 dB can be achieved.

3.4 Frequency Modulation

Frequency modulation of the RF output is achieved by modifying the fine tuning of the YIG oscillator. The current supply to the YIG's fine tuning coil is controlled by the FM driver (Part of A2), which in turn, is controlled by the output phase lock loop circuit (Part of A2). Normally, the PLL driver output, suitably filtered and amplified, is derived from the outputs of the phase comparator. However, during operation in the FM mode, this phase comparator signal is summed with a modulation signal. The outcome is a modulated drive resulting in a frequency modulated output from the YIG oscillator.

3.5 Frequency Synthesis

The output frequency is produced by a YIG oscillator. Coarse tuning of the YIG is done through the YIG driver (A3). The A3 circuit board supplies a programmable current source which the Control module adjusts by means of a digital to analog converter and amplifier. This current source, connected to the YIG tuning coil, can bring the YIG frequency within 50 MHz of the desired value. Fine tuning of the YIG is accomplished by the output phase lock loop, which supplies a controlled tuning current to the YIG's FM coil. The overall synthesis process can involve up to six phase lock loops, depending on output frequency resolution.

3.5.1 Phase Lock Loop

The purpose of a phase lock loop (PLL) is to control a variable frequency oscillator so that its output frequency has the same accuracy and stability as that of a fixed reference oscillator.

The PLL works by comparing two frequency inputs, one fixed and one variable. After comparison, it supplies a correction signal to the variable oscillator achieving and maintaining a constant phase relationship between the two inputs (see Figure 3-4).

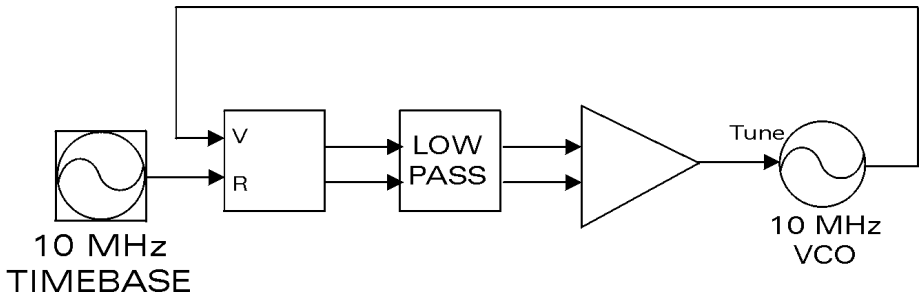


Figure 3-4: Elementary Phase Lock Loop

The stability and accuracy of a reference frequency (for example, the signal produced by a 10 MHz crystal oscillator) can be transferred to a voltage controlled oscillator (VCO) by means of a phase lock loop. The 10 MHz signal is applied to the reference input of the PLL, and the VCO output frequency is fed back to the variable input of the PLL. A phase detector in the PLL circuit compares the two inputs and determines whether the variable input is leading, or lagging, the reference. The phase detector has two outputs. Pulses appear at one output, depending on whether the variable input is leading or lagging. (The width of the pulses is proportional to the degree of phase difference.) The width of the pulses are averaged by a low pass filter and DC amplifier; the result is a correction signal causing the VCO frequency to increase, or decrease, in order to reduce the phase difference between the two input frequencies. When the phase error is eliminated: the frequencies are equal, the loop is said to be locked, and the VCO frequency acquires the accuracy and stability of the reference input.

Although the variable input to the phase detector should equal the frequency of the reference input, it need not equal the frequency of the VCO. If a frequency divider is introduced between the VCO and the variable input, the VCO can be run at a frequency that is a multiple of the reference frequency. For example, if the VCO output is divided by ten before being applied to the phase detector input, the VCO can run at 100 MHz and still be phase locked to a 10 MHz reference. A frequency divider intervening between the VCO and the phase detector variable input is called a prescaler. If the prescaler is programmable (i.e., it can be set to a given divisor), a variety of frequencies can be phase locked to a single reference frequency (see Figure 3-5).

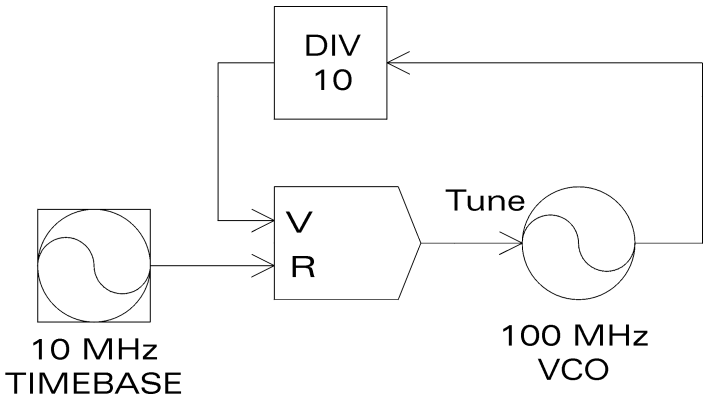


Figure 3-5: Phase Lock Loop, with Prescaler

Since the output frequency must be some multiple of the reference frequency input to the phase detector; the reference frequency limits the resolution of the system. For example: using a 10 MHz timebase, frequencies of 70 MHz, or 80 MHz, can be generated. However, frequencies of 73 MHz cannot be generated, because digital frequency dividers can perform integer divisions only (i.e., the prescaler cannot be programmed to divide by 7.3). Nevertheless, if the reference frequency applied to the phase detector is itself programmable, this difficulty can be overcome. The solution is to use a 1 MHz reference frequency and divide the output by 73, or use a 7.3 MHz reference and divide the output by 10.

3.5.2 Microwave Frequency Synthesis

Digital synthesis of microwave frequencies is impeded by two inherent difficulties. First, these frequencies are well above the operating range of digital logic circuits. Secondly, the bandwidths required tend to be large (several thousand Megahertz). A requirement for fine frequency resolution over so wide of a range further complicates the synthesis process.

Because the Synthesizer output frequency is too high for digital circuits to work with, the Synthesizer uses RF mixers to downconvert microwave signals to a lower and more workable range. Generally, a mixer provides an intermediate frequency equal to the difference between two high-frequency inputs. For example, a step-recovery diode multiplier and an RF mixer (used in a combination known as a sampling mixer) can derive a low frequency I.F. equal to the difference between the output microwave signal and some harmonic of a stable reference frequency. The various reference signals used to synthesize the output are generated at, or mixed down to, frequencies low enough to drive digital circuits.

The problem of bandwidth, insofar as it limits frequency resolution, is overcome through the use of several compounded PLL circuits, which produce reference frequencies programmable in 1 kHz increments over a wide range.

3.5.3 The Synthesis Network

All output frequencies are synthesized by the output PLL, and are ultimately phase locked to the 10 MHz master reference. The Synthesizer can be analyzed as two parallel branches connecting the master reference to the output PLL reference and variable inputs. The variable branch includes fee dBack from the output YIG oscillator. *Unless otherwise noted all circuits are located in the Synthesizer module*.

3.5.4 The Reference Branch

10 MHz master reference (Control module)

110 MHz PLL (Control module)

110 MHz oscillator/multiplier (Control module)

80 MHz PLL (A1)

Output PLL, reference input (A2)

The master reference is the instrument's 10 MHz timebase (either the built-in oscillator or an externally applied reference signal). This reference is located in the Control module.

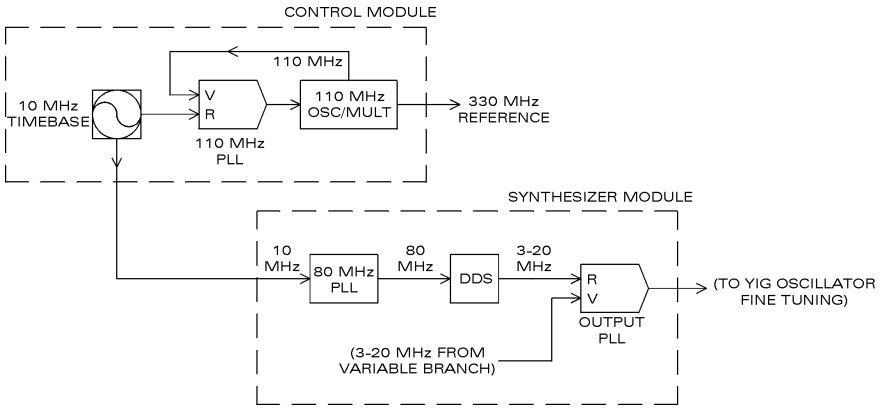


Figure 3-6: The Reference Branch

110 MHz PLL (Control Module)

The 110 MHz PLL phase locks the 110 MHz voltage controlled oscillator to the 10 MHz time-base: a sample of the VCO frequency is divided by 11 and applied to the variable input of a phase comparator (the timebase is the reference input). The phase comparator output is used to generate a tuning voltage for the VCO. The PLL increases or decreases the oscillator frequency, until the phase detector inputs match. The 110 MHz oscillator/multiplier generates a 330 MHz reference signal that is required by other circuits. The 110 MHz oscillator/multiplier incorporates a 110 MHz VCO (tuned by the PLL circuit described above) and a frequency tripler (for the 330 MHz reference). This circuit is located in the Control module.

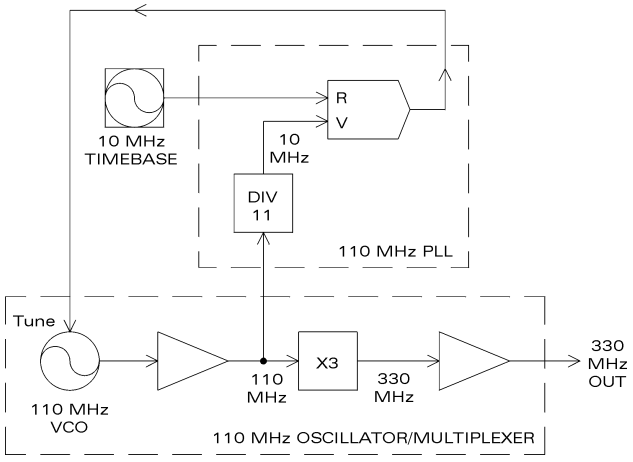


Figure 3-7: 110 MHz Oscillator/Multiplier and PLL

80 MHz PLL (A1)

The 80 MHz PLL is used to generate a fixed 80 MHz output which is phase locked to the timebase. The 80 MHz VCO is tuned by the output of a phase comparator. The VCO output is fed back to the phase comparator's variable input by way of a divide-by-eight circuit (so that the variable input is 10 MHz when the loop is locked). The phase comparator's reference input is the 10 MHz timebase.

The fixed 80 MHz output of the VCO is used as a reference input by the Direct Digital Synthesizer (DDS) chip. The DDS is used in conjunction with a Digital-to-Analog Converter to generate a programmable output frequency in the range of 3 to 20 MHz. The output frequency is programmed digitally by the CPU; the DDS generates a sequence of digital values which is converted into a waveform by the DAC. (The DAC, too, is clocked by the 80 MHz reference input.) The DAC's output is amplified and furnished (through a low-pass filter which removes noise generated by the digital circuits) to the reference input of the Output PLL.

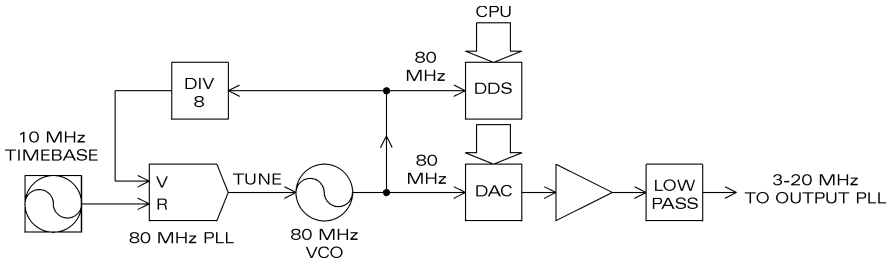


Figure 3-8: 80 MHz PLL and DDS

3.5.5 The Variable Branch

This branch consists of circuits in the following sequence:

10 MHz master reference (Control module)

110 MHz PLL (Control module)

110 MHz oscillator/multiplier (Control module)

300 MHz PLL (A2)

300 MHz VCO/driver (A104)

Sampling mixer/IF amplifier (A104)

Divide-by-N (A2)

Output PLL, variable input (A2)

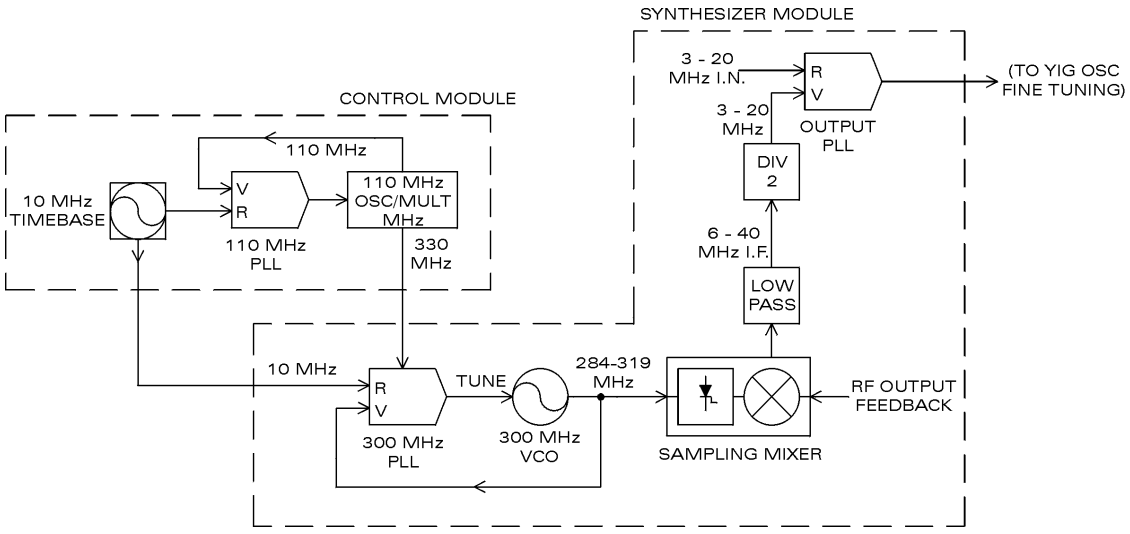


Figure 3-9: The Variable Branch

The 10 MHz master reference and the 110 MHz PLL are the same circuits used in the reference branch.

The 110 MHz oscillator/multiplier supplies a 330 MHz reference input to the 300 MHz PLL.

The 300 MHz PLL and the 300 MHz VCO/driver function together as a programmable source, generating frequencies in 1 MHz steps between 284 and 319 MHz (the 300 MHz PLL/VCO combination is described in more detail on the following page). This 284 to 319 MHz output is amplified and furnished to the multiplier input of the sampling mixer.

The sampling mixer has a step recovery diode multiplier on one of its inputs (the input driven by the 300 MHz VCO): the multiplier produces a series of frequency components that are harmonics of the input. The other input to the mixer is an RF fee dBack signal, coupled from the output of the YIG oscillator. The mixer combines the YIG frequency with the harmonics of the VCO frequency, yielding a great variety of intermediate frequency (IF) components. The IF output is amplified and filtered in order to pass only IFs within an 80 MHz range. In this way the output is limited to a single IF component

derived from the difference between the YIG frequency and one of the VCO's harmonics. The IF (a signal programmable over a range of 6 to 40 MHz) is applied to the divide-by-2 circuit.

The divide-by-2 circuit produces an output frequency in the range of 3 to 20 MHz. The output is applied to the variable input of the output phase lock loop. The amplified and filtered phase detector output of the PLL is further amplified by the FM driver circuit before being applied to the YIG's FM coil. The YIG is tuned in order to adjust the sampling mixer's IF and thus equalize the reference and variable inputs to the PLL.

The various programmable frequencies are set by the Synthesizer Control module, in accordance with a complex algorithm, to produce the requested output frequency.

300 MHz PLL/VCO

The 300 MHz PLL/VCO portion of the variable branch consists of an oscillator, a mixer, two dividers, and a phase comparator (see Figure 3-10). The VCO's frequency output is fed back to the mixer, and mixed with the 330 MHz reference input. The resulting IF equals the difference between the VCO's frequency and 330 MHz; since the VCO has a range of 284 to 319 MHz, the IF has a range of 11 to 46 MHz.

The IF is furnished to a programmable divider. The divider is programmed with whatever divisor is needed to reduce the desired IF to 1 MHz (in other words, if the desired IF is 25 MHz, the divisor is set to 25). The 1 MHz output of the divider is applied to the variable input of the phase comparator (of course, the output of the divider will equal 1 MHz only when the loop is locked).

The reference input to the phase comparator is a fixed 1 MHz signal, produced by dividing the 10 MHz timebase signal by ten. The comparator's output drives the VCO in whatever direction will reduce the difference between the fixed 1 MHz input and the output of the divider.

The frequency of the VCO is determined by the setting of the programmable divider. If the divisor is set to 11, the VCO will be driven by the phase comparator to 319 MHz, resulting in an 11 MHz IF and a 1 MHz input to the phase comparator. If the divisor is set to 46, the VCO will be driven to 284 MHz, resulting in a 46 MHz IF and a 1 MHz input to the phase comparator.

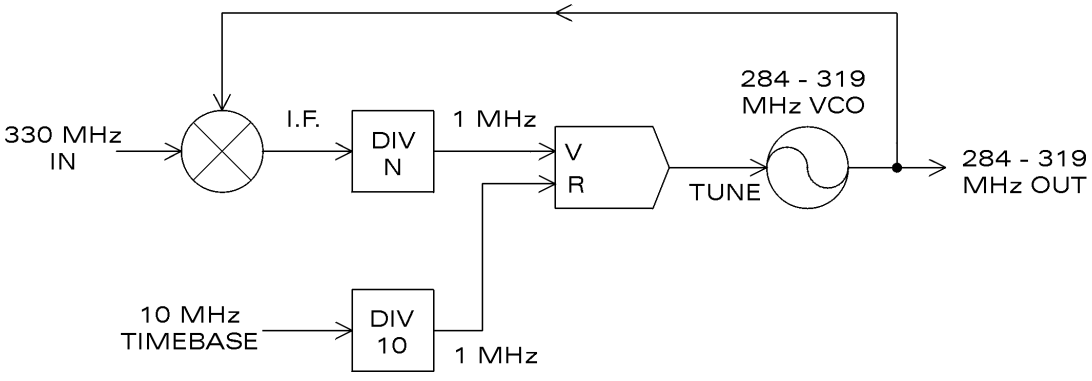


Figure 3-10: 300 MHz PLL/VCO

3.5.6 The Downconverter

The downconverter extends the frequency range of the Synthesizer module downwards, to 10 MHz. The downconverter is needed because its .01 to 2 GHz range is too low to be generated by a YIG oscillator (see Figure 3-11). The downconverter circuit mixes the YIG frequency with the fixed output of a local oscillator, yielding an intermediate frequency output in the range of .01 to 2 GHz.

The downconverter circuit is interposed between the output of the RF module and the input of the 10 dB step attenuator. During operation below 2 GHz, a switch in the output path diverts the RF output from the module to the downconverter; the low frequency signal synthesized by the downconverter is returned to the switch and furnished to the step attenuator.

During operation in the downconverter range, the YIG oscillator is tuned to a frequency in the approximate range of 5.9 to 7.9 GHz. The downconverter switch furnishes this frequency to the downconverter mixer. The other input to the mixer is a fixed 7.920 GHz input from a Dielectric Resonant Oscillator (DRO). The DRO output is phase-locked to the 330 MHz reference signal applied to it; the 330 MHz reference is in turn phase-locked to the instrument's 10 MHz master reference.

The IF output from the mixer is equal to the difference between the YIG frequency and the 7.920 GHz fixed output of the DRO. For example, the IF is 1.000 GHz when the YIG frequency is 6.920 GHz; the IF is .01 GHz when the YIG frequency is 7.910 GHz). The computer tunes and locks the YIG oscillator to the frequency that will yield the desired IF output from the downconverter mixer. The IF is amplified and returned to the downconverter switch.

Instrument functions, including level control and modulation, operate normally in the downconverter range (the leveling and modulation of the RF input to the downconverter mixer from the RF module is reflected in the mixer's IF output). The frequency synthesis process for the YIG frequency is also normal, except that it yields a frequency equal to 7.920 GHz minus the required output frequency.

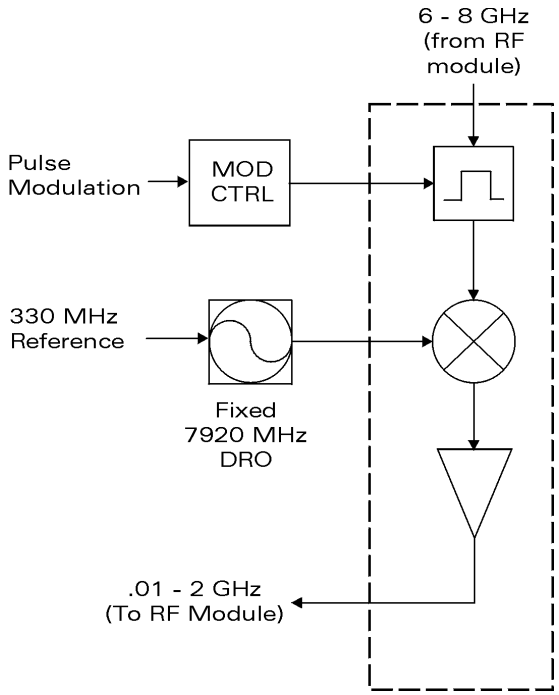


Figure 3-11: Downconverter Circuit

3.6 Circuit Descriptions (Controller)

3.6.1 VXI/Interface Control (A1)

This PC assembly is the only assembly in the Series 50000B that actually talks on the VXI bus. The A1 board holds the DT9150 Interface Technology daughter card, which handles all VXI Bus interface and communication. L1 thru L4 and associated capacitors provide filtering of the +5V supply to this assembly.

In addition to providing VXI bus interface functions, the microprocessor on this board runs the software contained in the U6 and U7 PROMS to control the 50000B modules. This software uses the U13 Peripheral Interface Timer IC 68230 to send and receive data over the VXI Local bus (via U11) to the various 50000B modules in the system. U13 also provides the control signals such as address data strobes and Direction strobe to control the Data bus. U9 supplies address decoding for U13. U10 provides the DTACK signal for the operation of U13.

3.6.2 110 MHz Assembly (A101A1)

110 MHz Phase Lock Loop

The function of this circuit is to phase lock the 110 MHz VCO on the oscillator/multiplier board to the 10 MHz master reference. In addition, this circuit performs important functions related to the master reference itself.

The output frequency of the 110 MHz VCO is received at J8 and U2 divides the input by 11. When the loop is locked, the input is exactly 110 MHz, and the divider output is exactly 10 MHz. One output from U2 is applied to the variable input of the phase comparator at U5-9. The other is buffered by U1C and serves as the 10 MHz reference signal out of the 52000B front panel. The reference input to the phase comparator comes from the 10 MHz input/output circuit.

The reference input to the phase comparator U5-6 comes from a switching circuit, which selects either an internal or external 10 MHz reference. When no external reference is present at J12, the internal 10 MHz reference at J10, buffered by U1B, propagates through U4C and the phase comparator (U5-6). When an external 10 MHz signal is present at J12, it is buffered by U1A and propagates through U4A to the phase comparator. The presence of an external 10 MHz reference is detected when a charge is built up on C24 and the switching circuit (comparator U8) switches to a high state. This causes U6 output to go high and turn off the supply to the internal 10 MHz reference. The switching circuit enables the external reference path at U4A and disables the internal reference at U4C. The selected reference is then available through Q3 and Q4 as the 10 MHz (Timebase) reference output on the 52000B front panel.

When its reference and variable inputs are not in phase, U5 produces wide pulses at one of its outputs, depending on whether the variable input is leading or lagging the reference. The pulsed outputs are filtered and amplified by U3-7 to produce a voltage output (J11) which tunes the 110 MHz VCO.

The lock indicator circuit (U3-1, Q1) responds to the wide pulses that occur on the phase comparator outputs when the loop is unlocked. The lock indicator turns on Q1, pulls the output low and turns on DS1. When the loop is locked, Q1 and DS1 are off.

3.6.3 110 MHZ Oscillator/Multiplier Assembly (A101A2)

This circuit is the source for the 220 MHz and 330 MHz reference signals used by various phase lock loop circuits in the Synthesizer.

The voltage controlled crystal oscillator (Q1, etc.) uses a quartz crystal resonator (Y1). A tuned circuit (L2, etc.) restricts the crystal to an oscillation mode at 110 MHz. The VCXO is fine tuned by a voltage input from the 110 MHz PLL circuit (A12). Its output signal is amplified by AR1 and buffered by line receiver U1. The buffered 110 MHz signal is fed back to the PLL and is also furnished to the frequency tripler.

The frequency tripler takes advantage of the powerful third harmonic component present in any square wave. The U5 line receivers produce a square 110 MHz signal, which is inductively coupled through a band-pass circuit (L4/L5, etc.). C17 and C18 provide peaking adjustment. Two band-stop filters on the output (L3, L6) remove the fundamental and thesecond harmonic of the VCXO frequency. The 330 MHz output is not buffered because the circuit to which it is furnished does not require a high power input.

3.7 Detailed Circuit Descriptions (Synthesizer)

3.7.1 Decode/DDS Assembly (A1)

This assembly contains the decode circuitry, which controls the 80 MHz Phase Lock Loop, and the Direct Digital Synthesis (DDS) circuitry.

Address Decode

This circuitry provides address decoding for the whole Synthesizer module. This module is controlled by the 52000B Control module via the 12 Local Bus lines available on the VXI Bus. Of the 12 available lines, 8 are used for the data bus, one to simulate an Address strobe, one for a Data strobe, and another line for Direction or read/write line.

Bidirectional buffer U5 buffers input from the Local bus and the LDIR line controls direction of the data or address being read or written.

To address a specific chip in a particular module and board, the first set of data written to this board from the control module consists of a module address and a chip address. The chip address bits (0-3) are used by the U6 decoder to decode the specific chip to be read from or written to. The module address bits (4-6) are used by decoder IC U4 to decode the module address. If the decoded module address matches the address selected by the switch at SW1, it enables the LDS and LAS (Local data and address strobes) to propagate thru U1, thus latching the desired chip address at U6 and the selected module address at U4.

Depending if the function is to read or write, the LDir line selects the direction of the U5 buffer. When the LDS or data strobe is received the data is read from the selected chip or written to the selected chip.

U8 is selected when CS0 is activated. This latch allows the module type to be read to identify the module as a synthesizer. The U9 latch allows the status from various PLLs and the leveling loop to be read. U10 decodes the various PLL lock signals to drive the front panel Lock LED. U11 provides control signals for the Reset PROM on A2. Some of the chip selects generated at U6 go directly to circuits on A1; however, many others go to A2 and A3 via the P3 connector.

80 MHz Oscillator and PLL

This circuit generates an 80 MHz reference signal for the DDS chip. The PLL circuitry phase locks the 80 MHz VCO to the 10 MHz reference signal. The main elements of the circuit are the voltage controlled oscillator (VCO), the divider, the phase comparator, and the lock detector.

The VCO (Q2, etc.) oscillates around 80 MHz; its output frequency is determined by the tuning voltage received from U14-1. The VCO output is furnished to the DDS chip after being buffered by Q3 and Q5. The VCO output is also divided by 8 at U13 and applied to the input of the phase comparator (U15-6).

The phase comparator produces pulses at one of its output pins (U15-3 or U15-12) depending on whether its variable input at pin 9 is leading or lagging the reference input at pin 6. The 10 MHz input at pin 9 is from J4, which comes from the front panel of the Synthesizer. The U14-A loop amplifier converts U15 output pulses into a DC control voltage for the VCO. The phase comparator tunes the VCO upward or downward in order to equalize its two input frequencies. When these two frequencies are equal, the loop is locked. The phase comparator output pulses are furnished (via CR3 and CR4) to the lock detector circuit (U14-B). When the loop is unlocked (i.e., when there is a large difference between the phase comparator inputs) the output pulses become very wide, U14-7 goes high to turn on Q4 and fault indicator DS1, and pulls the LOCK output low.

80 MHz DDS

The circuitry in thissection digitally synthesizes a reference frequency for the instrument's output phase locked loop.

The digital information to program the U20 DDS chip is supplied via latch U18. The control signals to strobe the data into the chip and to identify what information is present in the byte loaded at U18, are provided to the chip from latch U19. The 80 MHz reference clock required by the U20 DDS chip and the U16 D/A converter is amplified to CMOS levels via Q6, Q7, and U21-F, and then buffered by the remainingsections of U21 before being supplied to the U20 DDS chip.

Sections A, B and C of U21 can be jumpered to provide different delays of the 80 MHz clock before it is supplied to D/A U16. Coils L11-13, and associated capacitors create a 20 MHz low pass filter to filter harmonics and other spurious signals from the 2 to 20 MHz signal created by the DDS/DA combination. This 2 to 20 MHz signal is buffered by U17 and shifted to ECL levels before being made available to the output PLL at J5.

3.7.2 Level/RF Control (A2)

This assembly contains the Reset ROM, Level Control circuitry, and the Output and 300 MHz PLL. It also provides power, chip selects and data bus lines to the Driver and YIG Driver PC assemblies (A3 and A4) via the P4 ribbon cable.

The chip selects the control lines and data bus lines from the RF/Decode PCA #1 assembly through the ribbon cable at P3. Latches U2 and U6 allow two 8-bit addresses to be latched to create a 16-bit address to address the U5 Reset ROM for the Synthesizer module. The U5 Reset ROM is programmed with information unique to the Synthesizer; including its hardware characteristics, frequency ranges, level and frequency correction data. The controller module must read this information via U50 before it can control the Synthesizer. U1 latches the various logic states for the level and output loops.

Output PLL and Divider

The output PLL circuitry produces a control signal for use in fine-tuning the instrument's YIG oscillator, in order to phase lock the YIG frequency to the master reference. In the FM mode, the control signal is combined with a modulation input.

The U11 phase detector receives two input frequencies, both in the 5 to 10 MHz range. These frequencies are equal when the loop is locked. The reference frequency input comes from the divide-by-8 circuit on the A1 board (J-46) and the variable frequency input (fV) comes from the programmable divider circuit on this board. The phase detector produces outputs at pins 4 and 18 of U11. If the input frequencies are not in phase, wide pulses appear at one of these pins, depending on whether fV is leading or lagging. The outputs are used by the lock detector circuit (see U48-7, Q1) to determine if the loop is locked. They are also used by one of two independent loop amplifier circuits (selected by analog gate U10) to produce the loop control output.

The first loop amplifier circuit is used when the instrument is not in FM mode. The phase detector outputs are amplified by U9-1 and U9-7. Frequency compensation networks (R25/C22, R20/C21, R14/C18) provide the rolloff needed to stabilize the loop. Diodes in the amplifiers fee dBack loops limit the amplifier outputs to prevent saturation during the search mode. The output of U9-7 is applied through the U10 analog gate to the U48-1 amplifier, which drives the U7 YIG driver amplifier. This output tunes the YIG oscillator FM coil; it goes more negative to increase frequency and more positive to decrease.

Thesecond loop amplifier circuit is used when the instrument is in the FM mode. Essentially, it duplicates the first loop amplifier (see U13-1, U13-7) but adds the input FM signal (amplified by U12-1)

to the phase detector output signal. The two signals are combined by U12-7 and applied to analog gate U10.

The variable frequency input to the phase detector is derived from the sampling mixer IF, not directly from the YIG output frequency. The sampler's IF is the product of a harmonic multiplier, and may be derived from the wrong harmonic. In that case the phase lock loop is misdirected, tuning the YIG oscillator in the wrong direction until it reaches its positive or negative rail. To prevent the PLL circuit from becoming stuck in this mode, a search circuit is added, consisting of amplifiers U49-1 and U49-7 to monitor the circuit output and return control voltages to the loop amplifier circuits. When the output becomes too positive (minimum frequency), U49-7 swings to its negative rail, driving the output negative (maximum frequency). When the situation is reversed, U49-1 drives the output positive (minimum frequency).

When the Synthesizer is equipped with analog sweep, the U51 sample and Hold circuit samples the loop voltage when it receives the OP sample signal. The loop is then opened at U10-5 and the sampled loop voltage is substituted at U10-9. This allows a specific start frequency to be programmed for analog sweep.

The programmable divider circuit (U16 and U18) can be set to divide by 2, 4 or 8. It accepts a 10 to 80 MHz sampler IF at J2 from the 300 MHz Oscillator board (A104). A low pass filter (L2, etc.) removes spurious high frequencies from the signal. A series of three flip flops (U18, U16) are used to provide three outputs equal to the input frequency divided by 2 (at U16-4), by 4 (at U16-18) and by 8 (at U18-18). The computer selects the appropriate divisor by means of the A logic and B logic control inputs. Because these inputs are at TTL logic levels, two differential amplifiers (Q4/Q5 and Q2/Q3) are used to convert them to ECL voltages. The differential outputs drive the SET and RESET inputs at U16-17 and U18-15, and also to drive the steering gates at U17-9 and U17-5. Only one of the three flip flops is allowed to contribute its output to the final buffer, U17-12.

The computer selects a divisor which will reduce the 10 to 80 MHz IF input to a 5 to 10 MHz output. The A logic and B logic control bits (see Q4 and Q2) are interpreted as follows:

A logic	B logic	DIVISOR
0	0	2
0	1	4
1	1	8

300 MHz Phase Lock Loop

This circuit tunes the 300 MHz voltage controlled oscillator (A104 module). The VCO can be programmed over a range of 284 to 319 MHz; the PLL circuit enables the computer to select the desired VCO frequency and phase lock the VCO to the instrument's 10 MHz timebase. The input at J7 is fee dBack from the VCO. Because the 284 to 319 MHz input frequency is too high to be counted by the digital circuits used here, the input signal is mixed (see U29) with the 330 MHz reference input (received at J8 and amplified by AR3) yielding an intermediate frequency in the range of 11 to 46 MHz. A low pass filter (L2, etc.) removes the mixer input frequencies. The IF is then amplified (AR2) and applied to the programmable divider.

The purpose of the programmable divider is to divide the 11 to 46 MHz IF down to 1 MHz. The first stage of the divider consists of an 8 bit latch, U20; the computer selects the divisor (in the range of 11 to 46). The outputs of the latch are applied to the comparators of U24 and U21; the comparator outputs translate the eight-bit divisor into ECL levels for use by the high speed ECL down-counters, U25 and U22. The counters are clocked by the amplified IF, and count down from the numbers programmed into them. U22 represents the four least significant bits, U25 the four most significant bits. Flip flop U26, also clocked by the IF, receives a high at its D input (U26-13) at the end of the count and sends a high output pulse (from U26-19) to the phase comparator U28. The counters are reset by U26-18 and the count repeats.

The phase comparator chip, U28, requires reference and variable frequency inputs. The reference input is derived from the instrument's 10 MHz timebase. The 10 MHz input is received at J6, filtered (L3, etc.) and divided by ten at U31. The 1 MHz quotient is applied to the comparator at U28-9. The variable input, received from the programmable divider circuit (see U26-19), is applied to the phase comparator at U28-13. The phase comparator produces wide pulses at one of its outputs (pin 4 or 18) depending on whether the variable input is leading or lagging the reference. The loop amplifier circuit (U27, etc.) converts these pulses into a DC voltage output (J5) with which to tune the VCO. The polarity of tuning is: more positive to increase frequency, more negative to decrease frequency. The PLL circuit tunes the VCO in whatever direction will reduce the phase difference between the reference and variable inputs to the phase comparator. Filter components in the loop amplifier circuit (C50, C57, etc.) remove the phase comparator's output pulses from the tuning signal.

When there is a large phase difference between the reference and variable inputs to the phase comparator (i.e., when the loop is unlocked, wide low-going pulses appear at one of U28's outputs. These pulses are detected by the circuit consisting of U30, etc., and cause the LOCK output to go low and the LED (DS2) to be lit. When the loop is locked, U28's output pulses become extremely narrow and shallow, the LOCK output is high, and the LED is extinguished.

Automatic Level Control (ALC)

The ALC circuit drives the leveler, a variable attenuator circuit in the RF module, in order to make fine adjustments of output power. Fee dBack from a level detector in the RF path is compared with a leveling reference, and the leveler is driven so as to equalize these two inputs. The leveling reference is set by the computer through programming of the digital to analog converter, U34. At U35-6, the reference is combined with a correction voltage from the temperature compensation circuit on A3. During operation in the AM mode, these inputs to U35-6 are also combined with a modulation signal. The AM input is processed by logarithmic amplifier (U39) to match it to the log characteristic of the level reference and temperature compensation inputs) and furnished through U37 to the summing junction at U35-6 (U37 is switched off when AM is off). The combined leveling reference signal is processed by anti-logarithmic amplifier U36 and applied to U47-6, where it is combined with the amplified signal from the level detector (see U40, U42). In the event that the unit has analog power sweep capability, the power sweep ramp signal at J12 will also be summed, via U37, with the other signals at U35 pin 6.

The signal at the inverting input U47-6 is integrated (U47-7) and furnished to the PIN diode leveler circuit in the RF module. The polarity is positive for increased attenuation, negative for reduced attenuation. Following the leveler circuit in the RF path is a level coupler and diode detector. The detector returns a negative voltage proportional to detected RF power. The ALC circuit drives the leveler in such a way that the amplified detector signal and the leveling reference signal cancel for a zero voltage at U47-6.

When the output of U47-7 is within its normal range U46-7 turns off transistor Q6 and the leveled indicator output is pulled high, illuminating the level LED on the unit's front panel. If the ALC circuit has not yet adjusted the RF output to the requested level, a significant voltage will be present at U47-6, turning Q6 on and pulling the indicator output low.

3.7.3 YIG Driver/Temperature Compensation Assembly (A3)

This circuit controls the current source for the tuning coil in the output YIG oscillator. The oscillator tuning coil has a sensitivity of 20 MHz/mA. The computer coarse-tunes the YIG through its programming of this circuit. Note: The components surrounded by a dotted line on the schematic diagram are not located on this circuit board, but are shown for clarity.

U2 is a D/A converter. Its analog output is proportional to the binary number with which it is programmed by the computer. The DAC, together with U1-6 inverting amplifier, furnishes a computer-controlled voltage to the summing junction at U3-2 (by way of the R5 MIN calibration pot). The other inputs to this junction are (1) a negative voltage from reference diode VR1 (by way of the R14 MAX cal pot), (2) a positive voltage fed back from the YIG oscillator tuning coil, and (3) a sweep ramp input from the analog sweep module (during analog sweep operation). The output at U3-6 is furnished by way of Q1 to the base of the transistor which controls the YIG tuning coil current. The computer adjusts the YIG frequency through the programming of the DAC. When the input voltage to amplifier U3-2 changes, its output swings in whatever direction will yield a complementary change in the fee dBack from the YIG coil, thus maintaining virtual ground at the summing junction.

The U5 analog switches select different operating modes. During sweep operation, a ramp input is received at J1 and inverted by U4-6. The YIG ramp input directs the switching of U5-11 to furnish the signal to the summing junction at U3-2.

During repetitive sweeping, it is necessary to retune the YIG oscillator to the start frequency at the beginning of each sweep. Because the filter capacitors in the circuit resist rapid frequency changes, it is necessary to switch them out of the circuit during the transition. When the FAST line goes high, C12 is grounded through U5-15 and, at the same time, C31 is grounded through U5-7.

The Temperature Compensation circuit provides correction signals in response to internal temperature changes in the instrument. U9 is a temperature sensor, producing an output voltage proportional to temperature. The sensor voltage, amplified by U8-1, is furnished to a circuit consisting of U8-7, CR2, CR3, etc., which provides a correction signal to the level control circuit (A2). This correction signal is required because the sensitivity of the level detector changes with temperature, and this would cause a level error if not compensated. Each detector has a unique temperature response. During production testing, R35, R36 and R37 are selected and the ZERO pot (R33) is adjusted to match the response curve of the instrument's particular detector. THESE VALUES SHOULD NOT BE CHANGED.

3.7.4 Attenuator/Pulse Driver Assembly (A4)

The Driver circuitry provides harmonic filter selection and pulse modulation of the output signal. The pulse modulation is applied to the switching diodes of the harmonic filter network. An unmodulated filter system is used for the reference channel of the Synthesizer.

Decoder U1 selects the filter used in the reference channel. The TTL level low true outputs of the decoder are buffered by various amplifiers to provide a bipolar drive of about ±5V to the filter module.

Asecond decoder, U2, selects the output filter ranges. In this case, the pulse modulation signal is applied to the enable pin. Once selected, the external pulse, clamped by CR3 and CR4, is routed to U2 pin 4 via U4A.

Each decoder output has a two-transistor driver to convert the TTL levels of the decoder to the ±5volts required by the filter module. Resistor and capacitor values are chosen to optimize the pulse rise/fall time.

Attenuator Relay Driver

The 10 dB step attenuator is programmed to switch any or all of four fixed-attenuation segments into or out of the device's RF path. The attenuation values of the individual segments are 30 dB, 30 dB, 20 dB and 10 dB. For a setting of 90 dB, all segments are activated. The mechanical switching is enabled by relay drivers, U11 and U12, which respond to TTL-level inputs and provide output levels of zero and approximately +24 volts. By programming the drivers, the computer can select attenuation values between zero and 90 dB, in steps of 10 dB. U14 allows the filter select lines to be controlled from the sweep module during analog sweep.

3.7.5 VXI 10 MHz Buffer Assembly

This circuit receives a 10 MHz input at J5 from the front panel 10 MHz input connector (the source of this signal is the Control module or another Giga-tronics module). The 10 MHz reference signal is buffered by U1 and supplied to several other circuits (via J7, J8, and J9) and to the front panel 10 MHz output connector (via J6).

3.7.6 VXI 330 MHz Buffer Assembly

This circuit receives a 330 MHz input (at J1) from the front panel 330 MHz input connector (the source of this signal is the Control module or another Giga-tronics module). The 330 MHz reference signal is buffered by U3, U4, U5, and U6 and supplied to the 300 MHz PLL (A2) (via J3), and to the front panel 330 MHz output connector (via J2).

3.7.7 300 MHz Oscillator/Driver Assembly (A104)

This circuit board is encased in an aluminum housing and mounted directly beneath the RF module; it is not normally accessible to service in the field.

The tuning output from the 300 MHz PLL circuit on A2 is received at J2. A 1 MHz trap (L3, etc.) reduces the reference-frequency component contributed by the PLL's phase detector. The filtered control signal is applied to the voltage-controlled oscillator (Q4). A sample of the VCO frequency is fed back to the PLL circuit (see AR2) in order to permit phase lock. The VCO operates over a range of 283 to 319 MHz.

The VCO output frequency is taken at L2; this inductor is implemented as a conductive strip in the printed circuit artwork and is tapped very close to ground in order to reduce the load on the oscillator and insure stability. The VCO frequency is amplified by AR1 and AR7 to meet the input level requirement of the sampling mixer (about 4 Vpp).

The sampling mixer is a miniature hybrid RF circuit which combines a mixer with a step-recovery diode multiplier. The multiplier (to which the VCO frequency from the driver is applied) generates numerous harmonic multiples of its input frequency. The harmonics are used as one input to the RF mixer; the other input (see J4) is a sample of the YIG oscillator frequency, obtained from a coupler in the RF module. Because one mixer input is a harmonic series, the intermediate frequency output includes numerous sum and difference frequency components.

The mixer IF must be filtered and amplified in order to isolate one IF component in the range of 10 to 80 MHz. The power level of the IF output is very low; AR3, AR4 and AR5 each provide about +19 dB of gain, and the final amplifier stage (AR6) provides about +33 dB of gain. Three low-pass filters (L6, L8 and L11) roll off sharply above 130 MHz to eliminate harmonics of the IF. The amplitude of the sampling mixer IF is highly variable with frequency; in order to obtain a flat frequency response, an AGC circuit is added (U2-7). Diodes CR4 and CR5 are used by the circuit as signal level detectors; a correction voltage is produced and is applied to attenuator diode CR3 in order to maintain a 1 Vpp IF output at J3.