SHQ x4xx

Precision High Voltage Power Supply SHQ series CAN-Interface

Operators Manual

Attention!

-It is not allowed to use the unit if the covers have been removed.

-We decline all responsibility for damages and injuries caused by an improper use of the module. It is highly recommended to read the operators manual before any kind of operation.

Note

The information in this manual is subject to change without notice. We take no responsibility whatsoever for any error in the document. We reserve the right to make changes in the product design without reservation and without notification to the users.

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1. General information

The SHQ is a high voltage desk top family of instruments which offer output voltages up to 6 kV for use in industry and research.

Main Characteristics:

-High voltage desk top power supplies with either front-panel or remote control via serial interface
-Output voltages with very low ripple and noise
-Compact and ruggedized enclosure with 1 or 2 independent high voltage power supplies
-Polarity manual switchable
-Simultaneous indication of current and voltage in HIGH RESOLUTION format on the 2-line LCD display
-Output short circuit and overload protection

2. Technical Data

TECHNICAL DATA		**HIGH PRECISION**		
Single channel HV Power Supply		SHQ 142M	SHQ 144M	SHQ 146L
Dual channel HV Power Supply		SHQ 242M	SHQ 244M	SHQ 246L
Output voltage $V_{O\ nom}$		2 kV	4 kV	6 kV
Output current $I_{O\ nom}$		6 mA	3 mA	1 mA
Ripple and noise		typ.: < 2 mV_{P-P}		max.: 5 mV_{P-P}
Stability:	$\Delta V_O / \Delta V_{INPUT}$	< $5 * 10^{-5}$ (after a warm-up period from 30 min)		
	ΔV_O (no load/ load)	< $3 * 10^{-5}$ (after a warm-up period from 30 min)		
Temperature coefficient		< $3 * 10^{-5}/_K$		
Voltage measurement	resolution ADC:	100 mV / 6-digit LCD display (Option **VHR**: **10 mV** for SHQ x42M and x44M **only**)		
	accuracy:	± (0,05% V_O + 0,02% $V_{O\ nom}$)		
Voltage settings	manual / DAC:	10-turn potentiometer / digital via serial interface		
	resolution DAC:	100 mV / Option **VHR**: **SHQ x42M** with **30 mV**; **SHQ x44M** with **80 mV**		
Current measurement	resolution ADC:	2 ranges / 6-digit LCD display		
		Range mA: $I_{O\ nom} \geq I_O \geq 100\ \mu A$, Resolution: 100 nA Option **0n1**: $I_{O\ nom} \geq I_O \geq 10\ \mu A$, Resolution: 100 nA Accuracy: ± (0,1% I_O + 0,02% $I_{O\ nom}$)		
		Range µA: 100 µA > I_O > 20 nA, Resolution:: 1 nA Accuracy: ± (0,1% I_O + 20 nA)		
		Option **0n1**: 10 µA > I_O > 2 nA, Resolution: 100 pA Accuracy: ± (0,1% I_O + 2 nA)		
Value scope		all data are guaranteed in the range of (0,2% * $V_{O\ nom}$) < V_O < $V_{O\ nom}$		
Rate of change of output voltage		fixed: 500 $^V/_s$ (at HV-ON/OFF) variable: 2 ... 255 $^V/_s$ (at remote control)		
Protection		-hardware voltage limit (V_{MAX} rotary switch in 10%-steps) -hardware current limit (I_{MAX} rotary switch in 10%-steps, Option **IWP**: setting with 10-turn potentiometer $\mathbf{I_{SET}}$) -INHIBIT (external signal, TTL-level, LOW = active) -programmable current trip (software)		
Interface		CAN-Interface		
Line voltage AC (V_{INPUT})		230 V_{AC} $^{+10\%}/_{-15\%}$ (Option **ACW**)[1]: 95 V_{AC} . . . 265 V_{AC})		
Connectors		HV output: SHV-Connector INHIBIT: 1-pin Lemo-hub CAN: 9-pin male D-Sub connector		

The **built-in options** are signed on the name plate on the rear side!

)1 **Option ACW:** The state-of-readiness of the unit will be achieved ca. 10 s after power up the AC line voltage from 110 V-AC ± 10% !

3. SHQ Description

The functions are described with reference to a block diagram of the SHQ, shown in Appendix A.

High voltage supply

A patented high efficiency resonance converter circuit, which provides a low harmonic sine voltage on the HV-transformer, is used to generate the high voltage. The high voltage is rectified using a high speed HV-rectifier, and the polarity is selected via a high-voltage switch. A consecutive active HV-filter damps the residual ripple and ensures low ripple and noise values as well as the stability of the output voltage. A precision voltage divider is integrated into the HV-filter to provide the set value of the output voltage; an additional voltage divider supplies the measuring signal for the maximum voltage control. A precision measuring and AGC amplifier compares the actual output voltage with the set value given by the DAC (computer control) or the potentiometer (manual control). Signals for the control of the resonance converter and the stabilizer circuit are derived from the result of the comparison. The two-stage layout of the control circuit results in an output voltage, stabilized with very high precision to the set point.

Separate security circuits prevent exceeding the front-panel switch settings for the current I_{max} and voltage V_{max} limits. A monitoring circuit prevents malfunction caused by low supply voltage.

The internal error detection logic evaluates the corresponding error signals and the external INHIBIT signal. It allows the detection of short overcurrent due to single flashovers in addition.

Digital control unit

A micro controller handles the internal control, evaluation and calibration functions of both channels. The actual voltages and currents are read cyclically by an ADC using a multiplexer and processed for display on the 4 digit LCD display. The current and voltage hardware limits are retrieved cyclically several times per second. The reference voltage source provides a precise voltage reference for the ADC and generation of the control signals in the manual operation mode of the unit.

The set values for the corresponding channels are generated by a 18-bit DAC in computer controlled mode.

Filter

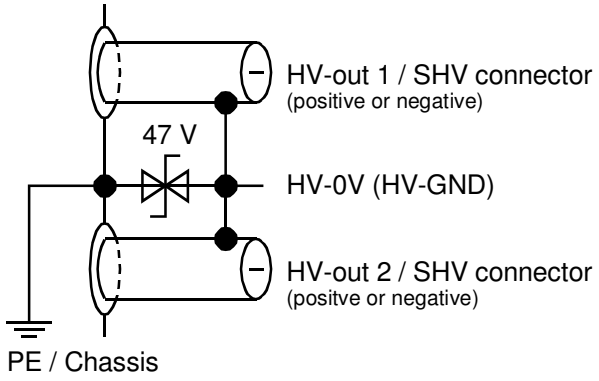
A special property of the unit is a tuned filtering concept, which prevents radiation of electromagnetic interference into the unit, as well as the emittance of interference by the module. A filtering network is located next to the connectors for the supply voltage and the converter circuits of the individual devices are also protected by filters. The high-voltage filters are housed in individual metal enclosures to shield even minimum interference radiation.

Floating HV-outputs

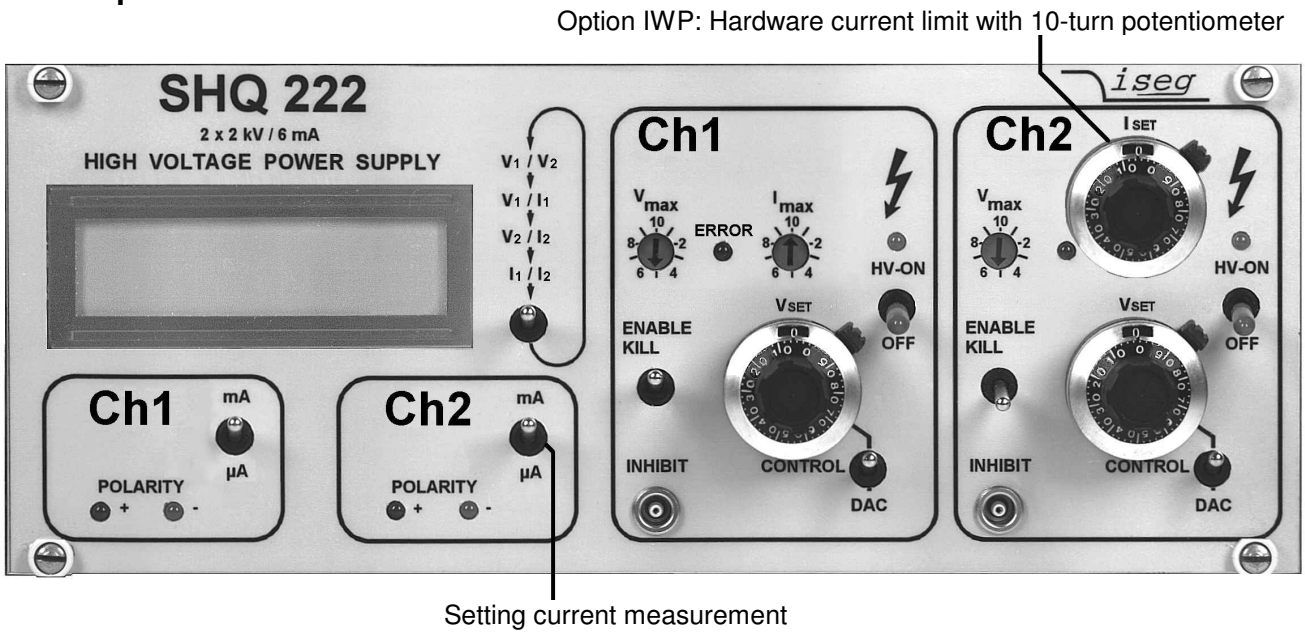
The HV outputs are related to the same ground HV-0V (HV-GND), outer connector (screen of HV cable) of SHV connectors. The channels can be switched independently in polarity and are also independently controlled in output voltage related to HV-0V (HV-GND).

The SHV connectors are mounted isolated to chassis (PE) in order to have a floating HV-0V.

In case of the floating voltage will become more than 47V a suppressor diode connects HV-0V to PE (chassis) and so far avoids that the voltage between HV-0V and PE/chassis will become dangerous.



4. Front panel



Channel 1 shows the panel for the SHQ module without the option IWP. The option IWP ″Hardware current limit setting with 10-turn potentiometer″ is shown on the panel Channel 2, on the right side.

5. Operation

The state-of-readiness of the unit is detected by monitoring the AC line voltage, the 9 pin female D-Sub connector for the serial interface and the HV-output on the rear.

Option ACW: The state-of-readiness of the unit will be achieved ca. 10 s after power up the AC line voltage from 110 V-AC ± 10% !

The Output Polarity is selectable with help of a rotary switch on the rear of the unit. The selected polarity is displayed by a LED on the front panel and a sign on the LCD display.

WARNING! Do not change the polarity under power!

An undefined Output Polarity switch setting (not at one of the end positions) will result in no output voltage.

High voltage output is switched on with HV-ON switch at the front panel. This condition is signalled by the yellow LED over the switch.

WARNING! If the CONTROL switch is in upper position (manual control), high voltage is generated at HV-output on the flip side with a ramp speed from 500 V/s (hardware ramp) to the set voltage chosen via 10-turn potentiometer (V_{SET}).
This is also the case if DAC control is switched over to manual control while operating.

If the CONTROL switch is in lower position (DAC), high voltage will be activated only after receiving corresponding interface commands.

WARNING! During last operation of the unit the user activated the function ″Autostart″, the high voltage will be turned on immediately with the saved parameters!

The type of display can be selected by briefly toggling the switch next to the 2 line LCD display. Voltages and / or currents are indicated with the resolution of voltage- and current measurement of the corresponding SHQ series.

Maximum output voltage can be hardware selected in 10%-steps with the rotary switches V_{max} (switch dialled to 10 corresponds to 100%). The output voltage will be limited to V_{max}.

If working with manual control, output voltage can be set via 10-turn potentiometer in a range from 0 to the set maximal voltage.

If the CONTROL switch is switched over to remote control, the DAC takes over the last set output voltage of manual control. Output voltage can be generated with a programmable ramp speed (software ramp) from 2 to 255 V/s in a range from 0 to the maximal set voltage via the interface.

The maximum output current per channel can be set with a programmable current trip via the interface with the resolution of maximum current measurement range. If the output current exceeds the programmable limit, the output voltage will be shut off permanently by the software. Restoring the voltage is possible only after ″Read status word″ and then ″Start voltage change″ via the serial interface. If ″Auto start″ is active, ″Start voltage change″ is not necessary.

Maximum output current can be hardware selected independently of programmable current trip
- in 10%-steps with the rotary switches I_{max} (switch dialled to 10 corresponds to 100%) or
- optionally with the 10-turn potentiometer I_{SET}.

If the output voltage or current exceeds the limits, is this signalled by the red error LED on the front panel.

The resolution of current measurement can be preset with the switch „Setting current measurement“. There by the setting range of the hardware current limit and maximum output current are defined. 100 % I_{max} or I_{SET} always corresponds to the maximum current measurement data of the chosen sector. The automatic measurement range selection for current measurement and display only functions in the direction of higher resolution and does not influence the setting range of the hardware current limit.

Function of the KILL switch:

Switch to the upper position: (ENABLE KILL)	The output voltage will be shut off permanently without ramp on exceeding I_{max} / I_{SET} or in the presence of an INHIBIT signal (Low=active) at the INHIBIT input. Restoring the output voltage is possible after operating the switches HV-ON or KILL or ″Read status word″ and then ″Start voltage change″ by DAC control. If ″Auto start″ is active, ″Start voltage change″ is not necessary.
Note:	If any capacitance is connected to the HV-output or if the rate of change of the output voltage is high (hardware ramp) at high load, then the KILL function will be released due to the current which is charging this capacitor. In this case a slower rate of output change (software ramp) is recommended or ENABLE KILL should not be selected before the output voltage has arrived the set voltage.
Switch to the lower position: (DISABLE KILL)	The output current will be limited to I_{max} / I_{SET} ; INHIBIT shuts the output voltage off without ramp, the previous voltage setting will be restored with hard- or software ramp on INHIBIT no longer being present.

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6. CAN - Interface

6.1 Device Control Protocol DCP

The communication between the controller and the module works according to the Device Control Protocol DCP, which has been designed for the use of multi-level-hierarchy systems of instruments.

This protocol works according to the master slave principle. Therefore, the controllers which are on higher hierarchy always are masters while devices, which are in lower hierarchy, are working as slaves.

In the event of the control of the HV device through a controller, the controller will have the master function in this system, while the module (as a Front-end device with intelligence) will be the slave.

The data exchange between the controller and the Front-end (FE) device is working with help of data frames. These data frames are assembled of one direction bit DATA_DIR, one identifier bit DATA_ID and further data bytes. The direction bit DATA_DIR defines whether the data frame is a write or read-write access. The DATA_ID carries the information of the type of the data frame and occasionally sub addresses (G0, G1). It has been characterized through the first byte of the data frame with bit 7=1. The function of the module as part of a complex system has been defined through the DATA_ID .

In such systems with many hierarchical levels a single function of a single module can be addressed by using group controllers (GC). Then, for each GC on the way to the module, the data frame is created through nesting of the address fields of the GC-addresses followed by the DATA_ID (not necessary in case of control of a single module).

DATA_DIR	DATA_ID Bit								Access
	7	6	5	4	3	2	1	0	
X	0	x	x	x	x	x	x	x	No DATA_ID
0	1	0	x	x	x	x	x	x	Write access on Front-end device
1	1	0	x	x	x	x	x	x	Read-write access on Front-end device (Request at Write)
0	1	1	x	x	x	x	G1	G0	Write access on group
1	1	1	x	x	x	x	G1	G0	Read-write access on group (Request at Write)
									G0, G1 sub address, only needed if group controller (GC) is used

These data frames correspond to a transfer into layer 3 (Network Layer) respectively layer 4 (Transport Layer) of the OSI model of ISO. The transmission medium is CAN Bus according to the specification 2.0A, related to level1 (Physical Layer) and level 2 (Data Link Layer).

The Device Control Protocol DCP has been matched to the CAN Bus according to specification CAN 2.0A, but it is also possible to be matched to further transmission media (e.g. RS 232). Therefore specials of layer 1 and 2 are only mentioned if absolutely necessary and if misunderstandings of functions between the Transport Layer and functions of the Data Link Layer might be possible. The communication between the controller and a module on the same bus segment will be described as follows.

6.2 Function range

The most important parameters of the high voltage supply can be set and read under computer control via the CAN interface.

CAN-control mode

1st Write function: set voltage; ramp speed; maximal output current (current trip); auto start
2nd Switch function: output voltage = set voltage, output voltage = 0
3rd Read function: set voltage; actual output voltage; ramp speed; actual output current; current trip; auto start ; hardware limits current and voltage; status

Front panel switches have priority over software control.

Manual control mode

While the unit is operating in manual control mode, only CAN Read-write accesses are interpreted. Write accesses are accepted, but do not result into a change of the output voltage.

6.3 Summary of CAN data frames

DATA _DIR	DATA_ID Bit								Access	read/ write/ active	DATA - Bytes
	7	6	5	4	3	2	1	0			
	0	x	x	x	x	x	x	x	no DATA_ID		
	1	**0**	**C2**	**C1**	**C0**	**0**	**N1**	**N0**	Single access CHANNEL: N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B		
1	1	0	0	0	0	0	N1	N0	Actual voltage	r	5
1	1	0	0	1	0	0	N1	N0	Actual current	r	5
1/0	1	0	1	0	0	0	N1	N0	Set voltage	r/w	4
1/0	1	0	1	1	0	0	N1	N0	Ramp speed	r/w	2
0	1	0	0	0	1	0	N1	N0	Start voltage change	w	1
1	1	0	0	1	1	0	N1	N0	Hardware limits	r	4
1/0	1	0	1	0	1	0	N1	N0	Current trip	r/w	4
1/0	1	0	1	1	1	0	N1	N0	Auto start	r/w	2
1/0	1	0	1	1	0	1	N1	N0	Expanded ramp speed	r/w	3
	1	**1**	**C3**	**C2**	**C1**	**C0**	**G1**	**G0**	**Group access MODULE:** **G1 = G0 = 0, only needed if group controller (GC) is used**		
1/0	1	1	0	0	0	0	G1	G0	General status module / Advanced calibration	r/w	2
1	1	1	0	0	0	1	G1	G0	Module status Channel A and B	r	3
1	1	1	0	0	1	0	G1	G0	LAM-status Channel A and B	r	3
1	1	1	0	1	1	0	G1	G0	Log-on Front-end device in superior layer	a	3
0	1	1	0	1	1	0	G1	G0	Log-off superior layer at Front-end device	w	3
0	1	1	0	1	1	1	G1	G0	New bit rate	w	3
1	1	1	1	0	0	0	G1	G0	Serial number, software release and channels	r	7
							C_i		Accesses		
							N_i		Channels A and B		
							G_i		Group 0 to 3 Only needed if group controller (GC) is used		

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6.4 Detailed CAN data frames description

Log-on and Log-off Front-end (FE) device (active/write access)

Log-on frame module (DLC = 3)

Byte		DATA_ID								DATA_1	DATA_0							
Bit		7	6	5	4	3	2	1	0	0	7	6	5	4	3	2	1	0
Designation	DATA_DIR							G1	G0									
Data	1	1	1	0	1	1	0	0	0	x	0	0	0	0	1	1	0	0
Description	active	G1 to G0: Group 0 to 3 Only necessary if group controller (GC) is used								x=1: General status module okay x=0: current limit/trips or voltage limit have been exceeded at least one channel	Module class							

After POWER ON the module will give this group access cyclically on the bus (ca. 2...10 sec).

Bit 0 in DATA_1 describes the general status module (NOR-function of the error bits LAM_REG2ER_, LAM_REG1ER_, LAM_EXTINH_ and LAM_ILIM_ in both channels).

If a controller identifies this access then it is able to register this module as a Front-end device and is able to address it with FE_ADR.
(Module address, see also item 6.5, description 11bit-Identifier and item 6.6)

Remote-frame Log-on controller (DLC = 3)

Byte		DATA_ID								DATA_1	DATA_0							
Bit		7	6	5	4	3	2	1	0	0	7	6	5	4	3	2	1	0
Designation	DATA_DIR							G1	G0									
Data	0	1	1	0	1	1	0	0	0	1	0	0	0	0	1	1	0	0
Description	write	G1 to G0: Group 0 to 3 Only necessary if group controller (GC) is used								Module is log-on	Module class							

The module will not send further ‘Log-on controller” accesses after the successful registration as long as it receives accesses from the external CAN Bus in periods shorter than one minute and until the controller will send a ‘Log-off controller” access to the Front-end device, respectively.

Remote-frame Log-off controller (DLC = 3)

Byte		DATA_ID								DATA_1	DATA_0							
Bit		7	6	5	4	3	2	1	0	0	7	6	5	4	3	2	1	0
Designation	DATA_DIR							G1	G0									
Data	0	1	1	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0
Description	write	G1 to G0: Group 0 to 3 Only needed if group controller (GC) is used								Module is log-off	Module class							

Single access CHANNEL: Actual voltage (Read-write access)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR							N1	N0
assignment	1	1	0	0	0	0	0	x	x
Description	read	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Controller (DLC = 1):
Read actual voltage at the corresponding channel

⇓ Response module (DLC = 5)

Byte		DATA_ID								DATA_3			DATA_2			DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0		...	0	7	...	0	7	...	0
Designation	DATA_DIR							N1	N0									LSB			LSB
assignment	0	1	0	0	0	0	0	x	x	x									x		
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								Actual voltage [V]: exponential representation mantissa in 24-bit binary notation in DATA_3, DATA_2 und Data_1, exponent with sign in DATA_0											

Single access CHANNEL: Actual current (Read-write access)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR							N1	N0
Data	1	1	0	0	1	0	0	x	x
Description	read	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Controller (DLC = 1):
Read actual current at the corresponding channel

⇓ Response module (DLC = 5)

Byte		DATA_ID								DATA_3			DATA_2			DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0		...	0	7	...	0	7	...	0
Designation	DATA_DIR							N1	N0									LSB			LSB
Data	0	1	0	0	1	0	0	x	x	x									x		
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								Actual current [A]: exponential representation mantissa in 24-bit binary notation in DATA_3, DATA_2 und Data_1, exponent with sign in DATA_0											

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Single access CHANNEL: Set voltage (Read-write/Write access)

Read-write

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR							N1	N0
Data	1	1	0	1	0	0	0	x	x
Description	read	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Controller (DLC = 1):
Read set voltage at the corresponding channel

⇓ Response module (DLC = 4)

Byte		DATA_ID								DATA_2			DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7	...	0	7	...	0
Designation	DATA_DIR							N1	N0									LSB
Data	0	1	0	1	0	0	0	x	x	X								
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								Set voltage in [0,1V] in DATA_2, DATA_1 and DATA_0								

Write [Controller (DLC = 4): Write set voltage at corresponding channel]

Byte		DATA_ID								DATA_2			DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7	...	0	7	...	0
Designation	DATA_DIR							N1	N0									LSB
Data	0	1	0	1	0	0	0	x	x	X								
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								Set voltage in [0,1V] in DATA_2, DATA_1 and DATA_0								

Set voltages which are higher than the maximum channel voltage (nominal module voltage or V_{max}) will be set to nominal module voltage or V_{max} under software control.

Single access CHANNEL: Ramp speed (Read-write/Write access)

Read-write

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR							N1	N0
Data	1	1	0	1	1	0	0	x	x
Description	read	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Controller (DLC = 1):
Read actual ramp speed at the corresponding channel

⇓ Response module (DLC = 2)

Byte		DATA_ID								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA_DIR							N1	N0								LSB
Data	0	1	0	1	1	0	0	x	x	x7	x6	x5	x4	x3	x2	x1	x0
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								x7 ... x0: Ramp speed (1 to 255 V/s)							

Write [Controller (DLC = 2): Write ramp speed at the corresponding channel]

Byte		DATA_ID								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA_DIR							N1	N0								LSB
Data	0	1	0	1	1	0	0	x	x	x7	x6	x5	x4	x3	x2	x1	x0
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								x7 ... x0: Ramp speed (1 to 255 V/s)							

Ramp speed lower than 1 V/s will be set on 1 V/s with help of the firmware.

This value will be pre selected also after connecting to the supply voltages if - during the last use - the function „Auto start“ did not store a different voltage ramp.

If – during the process of change of the output voltage – a new voltage ramp will be initialized by firmware then this change will be taken immediately and the set voltage will be made with the new software ramp.

Specials if using the Single access CHANNEL: Expanded ramp speed (see page 13)

If you use the command “Expanded ramp speed” to write a ramp speed with

1st the value is not integer and

2nd the value is not in the range from 1 V/s to 255 V/s,

the response of the module will be with value 0 in DATA_0.

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Single access CHANNEL: Expanded ramp speed (Read-write/Write access)

Read-write

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR							N1	N0
Data	1	1	0	1	1	0	1	x	x
Description	read	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Controller (DLC = 1):
Read actual ramp speed at the corresponding channel in expanded resolution

⇓ Response module (DLC = 3)

Byte		DATA_ID								DATA_1								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA_DIR							N1	N0																LSB
Data	0	1	0	1	1	0	1	x	x	x15							x8	x7							x0
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								x15 ... x0: Ramp speed with resolution 0,1 V/s (up 0,1 V/s to 2500 V/s)															

Write [Controller (DLC = 3): Write expanded ramp speed at the corresponding channel]

Byte		DATA_ID								DATA_1								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA_DIR							N1	N0																LSB
Data	0	1	0	1	1	0	1	x	x	x15							x8	x7							x0
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								x15 ... x0: Ramp speed with resolution 0,1 V/s (up 0,1 V/s to 2500 V/s)															

If these command will be use with ramp speeds > 255 V/s the unit must have a higher hardware ramp speed too (e.g. 2600 V/s)!

Ramp speed lower than 0,1 V/s will be set on 0,1 V/s with help of the firmware.

The value 1 V/s will be pre selected after connecting to the supply voltages if - during the last use - the function „Auto start“ did not store a different voltage ramp.

If – during the process of change of the output voltage – a new voltage ramp will be initialized by firmware then this change will be taken immediately and the set voltage will be made with the new software ramp.

Please note the connection with the **Single access CHANNEL: Ramp speed** (see page 12)!

Single access CHANNEL: Start (Write access)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR							N1	N0
Data	0	1	0	0	0	1	0	x	x
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Controller (DLC = 1):

Start voltage change in the corresponding CHANNEL.

If the output voltage has been switched off permanently through the exceeding of I_{max} respectively through INHIBIT in case of ENABLE KILL or the programmable current trips , it is necessary to READ the LAM-Status of the register LAM_REG1ER, LAM_EXTINH or LAM_ILIM to set them back, before it is possible to reset an output voltage again.

If the output voltage has been limited through the exceeding of V_{max} or I_{max} in case of DISABLE KILL (ERROR-LED flashes and LAM_REG2ER_= 1),it is possible to decrease the output voltage through the writing of a lower set voltage and following „Start“ (Error-LED flashes no more!!). But before the voltage can be set higher afterwards the register LAM_REG2ER must be reset through READ of register LAM-status.

Single access CHANNEL: Limit (Read-write access)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR							N1	N0
Data	1	1	0	0	1	1	0	x	x
Description	read	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Controller (DLC = 1):

check Hardware limit settings of the corresponding CHANNEL

⇓ Response module (DLC = 4)

Byte		DATA_ID								DATA_2			DATA_1						DATA_0					
Bit		7	6	5	4	3	2	1	0	7	...	0	7	..	4	3	..	0	7	..	4	3	..	0
Designation	DATA_DIR							N1	N0			LSB		..			..			..	LSB		..	
Data	0	1	0	0	1	1	0	x	x	x			x			x			x			x		
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								mantissa V_{max} (8 bit)			Exp.V_{max}			mantissa I_{max} (8 bit)			exp I_{max}					
													exp. (4 bit), for exp. > 7 results in: negative exponent in 2´er complement											

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Single access CHANNEL: Current trip (Read-write//Write access)

Read-write access

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR							N1	N0
Data	1	1	0	1	0	1	0	x	x
Description	read	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Controller (DLC = 1):
Read maximum output current (current trip) of the corresponding CHANNEL .

⇓ Response module (DLC = 4)

Byte		DATA_ID								DATA_2			DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7	...	0	7	...	0
Designation	DATA_DIR							N1	N0									LSB
Data	0	1	0	1	0	1	0	x	x	x								
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								Current trip [A]: exponential representation mantissa in 24-bit binary notation in DATA_3, DATA_2 und Data_1, without exponent. Exponent is according to the value in the max. current measurement range								

Write access [Controller (DLC = 4): set max. output current (current trip) of corresponding CHANNEL]

Byte		DATA_ID								DATA_2			DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7	...	0	7	...	0
Designation	DATA_DIR							N1	N0									LSB
Data	0	1	0	1	0	1	0	x	x	x								
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								Current trip [A]: exponential representation mantissa in 24-bit binary notation in DATA_3, DATA_2 und Data_1, without exponent. Exponent is according to the value in the max. current measurement range								

If the output current exceeds the programmed current value then the output voltage will be switched off via the software (current trip). The highest resolution of the current measuring determines the possible resolution of maximum current limit. For the max. current limit = 0 A no current trip is programmable.
If the output voltage has been switched off through the exceeding of the max. current then the LAM–status must be read again in order to reset the output voltage with „Start“ or active „Auto start“ again.

Single access CHANNEL: Auto start (Read-write//Write access)

Read-write access

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR							N1	N0
Data	1	1	0	1	1	1	0	x	x
Description	read	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Controller (DLC = 1):
Check if „Auto start“ of corresponding CHANNEL is active.

⇓ Response module (DLC = 2)

Byte		DATA_ID								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA_DIR							N1	N0								LSB
Data	0	1	0	1	1	1	0	x	x					x3			
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								x3 = 1: Auto start is active x3 = 0: Auto start not active							

Auto start active means:

- if the ‘Auto start’ conditions (module-status ON_OFF_+ IN_EX_= 0 and LAM-Status _REG2ER_+_REG1ER_+_EXTINH_+_ILIM_= 0) are made, then the output voltage of the CHANNEL will be ramped to the actual set voltage, i.e. „Start“ is not necessary after ‘Write set voltage’ **,** Power-ON and Power OFF⇒ ON.
- if the output voltage of the CHANNEL has been switched off permanently through the exceeding of I_{max} respectively through INHIBIT (in case of ENABLE KILL or Current Trip) then it will be reset with software ramp after READ of LAM-status.
- if the output voltage will be limited through exceeding of V_{max} or I_{max} in case of DISABLE KILL (ERROR-LED flashed and LAM_REG2ER_= 1), then it is possible to ramp to a lower voltage (write a lower set voltage, Error-LED does not flash any more). But only Read LAM status of LAM_REG2ER reset the register and allows to increase the voltage.

Write access [Controller (DLC = 2): activate Auto start for corresponding CHANNEL]

Byte		DATA_ID								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA_DIR							N1	N0								LSB
Data	0	1	0	1	1	1	0	x	x					x3	x2	x1	x0
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								x3 = 1: Auto start activate							

x2 = 1: actual current trip ⎫
x1 = 1: actual set voltage ⎬ store in EEPROM one time
x0 = 1: actual voltage ramp ⎭

Values will be restored in corresponding register after supply voltages will have been connected!

(for EEPROM 1 Million write cycles guaranteed)

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Group access: General status module / Advanced calibration (Read-write access)

Read-write access

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR								
Data	1	1	1	0	0	0	0	0	0
Description	read								

Controller (DLC = 1):
Read general status module

⇓ Response module (DLC = 2)

Byte		DATA_ID								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA_DIR																LSB
Data	0	1	1	0	0	0	0	0	0	1	1	1	b4	1	1	b1	b0
Description	write									b4: advanced calibration b1: ramp status b0: sum status							

Write access [Controller (DLC = 2): Advanced calibration shut off or on]

Byte		DATA_ID								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA_DIR																LSB
Data	0	1	1	0	0	0	0	0	0	X	X	X	b4	X	X	X	X
Description	write									B4: advanced calibration X: any							

Bit	Name	Description	0	1
b4	ADVANCED STATUS	Advanced calibration	off	on
b1	RAMP STATUS	V_{OUT} in change with ramp	yes	no
b0	SUM STATUS	General status of module is okay	no	yes

The advanced calibration will be compensate long time and temperature drifts of the DACs. If the advanced calibration is on, these drifts will be compensated recurrent with help of averaging resp. approximation from the actual voltage.
The ADVANCED STATUS (bit 4) will be set on factory, the advanced calibration is on. If the advanced calibration will not use bit 4 = 0 must write with this group access.

The RAMP STATUS (bit 1) will be set, if V_{OUT} is stable in both channels (no changing with ramp).

The SUM STATUS (bit 0) will be built with the NOR-function of the error bits LAM_REG2ER_, LAM_REG1ER_, LAM_EXTINH_ and LAM_ILIM_ in both channels. Bit 0 will be set if the module is without these errors, the general status of module is okay.

Group access: module status CHANNEL A and B (Read-write access)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR								
Data	1	1	1	0	0	0	1	0	0
Description	read								

Controller (DLC = 1):
READ module - status of channels

⇓ Response module (DLC = 3)

Byte		DATA_ID								DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7	...	0
Designation	DATA_DIR									CHANNEL B			CHANNEL A		
Data	0	1	1	0	0	0	1	0	0	x					
Description	write									see list					

Description				Module-status CHANNEL A and B (read)		
CHANNEL	DATA	Bit	Name	Description	0	1
B	**_1**	b7	ERROR_2	error in CHANNEL B	channel ok	error
		b6	STATV_2	status V_{out}	V_{out} stable	V_{out} in change
		b5	TRENDV_2	Moving direction of V_{out}	V_{out} falling	V_{out} rising
		b4	KILL_2	switch position KILL	disabled	enabled
		b3	ON_OFF_2	Switch position HV-ON/OFF	on	off
		b2	POL_2	Polarity of output voltage V_{out}	negative	positive
		b1	IN_EX_2	Switch position CONTROL	DAC	manual
		b0	VZ_2	Output voltage V_{out} CHANNEL B	V_{out}<>0	V_{out}=0
A	**_0**	b7	ERROR_1	Error in CHANNEL A	channel ok	error
		b6	STATV_1	status V_{out}	V_{out} stable	V_{out} in change
		b5	TRENDV_1	Moving direction of V_{out}	V_{out} falling	V_{out} rising
		b4	KILL_1	switch position KILL	disabled	enabled
		b3	ON_OFF_1	Switch position HV-ON/OFF	on	off
		b2	POL_1	Polarity of output voltage V_{out}	negative	positive
		b1	IN_EX_1	Switch position CONTROL	DAC	manual
		b0	VZ_1	Output voltage V_{out} CHANNEL B	V_{out}<>0	V_{out}=0

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Group access: LAM-status CHANNEL A and B (Read-write access)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR								
Data	1	1	1	0	0	1	0	0	0
Description	read								

Controller (DLC = 1):
READ module - Status of channels

⇓ Response module (DLC = 3)

Byte		DATA_ID								DATA_1		DATA_0	
Bit		7	6	5	4	3	2	1	0	7 ... 0		7 ... 0	
Designation	DATA_DIR									CHANNEL B		CHANNEL A	
Data	0	1	1	0	0	1	0	0	0	x			
Description	write									See list			

Description				LAM-Status CHANNEL A and B (read)	
CHANNEL	DATA	Bit	Name	Description for Bit = 1	remarks
B	_1	b7	LAM_REG2ER_2	Quality of output voltage of CHANNEL B is not guaranteed at time	
		b6	LAM_REG1ER_2	exceeding of V_{max} or I_{max} was/is present	
		b5	LAM_EXTINH_2	external Inhibit-signal was / is active	
		b4	LAM_RANGE_2	relation V_{nom} to V_{max} > 1	Set voltage > V_{max}
		b3	LAM_KEY_CHANGED	A front panel switch of CHANNEL B has been activated	ON_OFF_2, IN_EXT_2, KILL_2
		b2	LAM_EOP_2	V_{out} CHANNEL B arrived at set voltage	end of process_2
		b1	LAM_ILIM_2	I_{out} has been higher than programmed I_{max} (current trip CHANNEL B)	
		b0			
A	_0	b7	LAM_REG2ER_1	Quality of output voltage of CHANNEL A is not guaranteed at this moment.	
		b6	LAM_REG1ER_1	Exceeding of V_{max} or I_{max} was/is present.	
		b5	LAM_EXTINH_1	external Inhibit-signal was/ is active	
		b4	LAM_RANGE_1	Relation V_{nom} to V_{max} > 1	Set voltage > V_{max}
		b3	LAM_KEY_CHANGED	A front panel switch of CHANNEL A has been activated	ON_OFF_1, IN_EXT_1, KILL_1
		b2	LAM_EOP_1	V_{out} CHANNEL A arrived at set voltage	end of process_1
		b1	LAM_ILIM_1	I_{out} has been higher than programmed I_{max} (current trip CHANNEL A)	
		b0			

Status bits will be set if a corresponding event happens and reset if LAM-status will be read afterwards. If the event is still existing or if it happens again the corresponding bits will be set again.

Group access: New bit rate (Write access)

Controller (DLC = 3): „ write new bit rate“ into EEPROM.

Byte		DATA_ID								DATA_1								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA_DIR																								LSB
Data	0	1	1	0	1	1	1	0	0								x8	x7	x6	x5	x4	x3	x2	x1	x0
Description	write									x8 ... x0: -7 bit rates are possible 1) 20 kBit/s 2) 50 kBit/s 3) 100 kBit/s 4) 125 kBit/s 5) 250 kBit/s 6) 500 kBit/s only on request 7) 1000 kBit/s only on request -the new bit rate is active after RESET or POWER OFF/ON and - it has to be sure, that - before a RESET or POWER OFF/ON – all modules of one segment have been set to the same bit rate. - the factory fixed bit rate is labeled on the rear side.														

Group access: Serial number and Software release (Read-write access)

Read-write

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR								
Data	1	1	1	1	0	0	0	0	0
Description	read								

Controller (DLC = 1):
Read serial number and software release module

⇓ Response module (DLC = 7)

Byte		DATA_ID								DATA_5		DATA_4		DATA_3		DATA_2		DATA_1		DATA_0	
Bit		7	6	5	4	3	2	1	0	BCD	BCD	BCD	BCD	BCD	BCD	BCD	BCD	BCD	BCD	BCD	BCD
Designation	DATA_DIR																				
Data	0	1	1	1	0	0	0	0	0	z6	z5	z4	z3	z2	z1	0	y3	y2	y1	0	x1
Description	write									z_n : 6 BCD Serial number						y_n : 3 BCD software release				x1: 1 BCD existing channels	

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6.5 Implementation in CAN-Bus

The data frame structure is matched to the message frame of the standard-format according to CAN specification 2.0A, whereas looking from the point of view of the CAN protocol a pure data transmission will be done, which is not applying to the protocol.

The data frame of the DCP will be transferred as data-word with n bytes length in the data field of the CAN frames according to the specific demands of the respective access. Therefore this results into a Data Length Code (DLC) of the CAN-protocol of n.
It is possible to transfer 8 data bytes that apply to the DLC field with falling values.

The RTR Bit is always set to zero.

The information for the direction of the data transfer (DATA_DIR) is written into the lowest bit ID0 of the 11 Bit CAN-Identifier. The controller therefore will start a read-write access for data with DATA_DIR = 1 and will send with DATA_DIR = 0.The Front-end device responds to the data request by sending the corresponding data with DATA_DIR = 0.Only if the Front-end device is not registered at the controller respectively if it does not receive valid data during a longer time period (ca. 1 min), then it will actively send the registration frame with DATA_DIR = 1 (see also item 4.3)

Therefore it follows that all even CAN-ports (Identifier) are interpreted as 'Write ports' all odd CAN ports as ' Read ports'.

The addressing of the Front-end device is also made with the 11 bit identifier of the CAN protocol. In order to keep the CAN segment open also for other protocols, the addressing room was limited to 64 nodes.

ID9 to ID10 are 0,
ID3 to ID8 allows the addressing of 64 Front-end devices (ID3: A0 = 2^0 ;...; ID8: A5 = 2^5),
ID1 and ID2 are not used.

Within one CAN segment only modules are allowed with different identifiers and identical bit rates.
The factory fixed bit rate is written on the sticker of the connector.

Following data frame is valid for the control of the Front-end device in this lowest CAN segment.

S	Identifier		R			DLC	n – data bytes						CRC	Ack
O			T	0	0	(n = 1 - 8)	DATA_ID		DATA_(n-2) ≥ 0		DATA_(n-3) ≥ 0		DATA_ ...			F.
F	b11	b0	R	reserve		b3	b0	**b7=**	b0	b7	b0	b7	b0	b7	b0	15 bit	

ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0	0	A5	A4	A3	A2	A1	A0			DATA _DIR

Acceptance-Filter of the used CAN-Controller is set to Front-end-address

The Front-end device must do:

- Processing of the single commands with direct channel values.
- Processing of group information of the channels.
- Self registration in the higher level through sending the module address.
- Building of status information.

The electrical transmission is floating and works with signal CAN_L and CAN_H, with reference to CAN_GND. The pin assignment of connector D-Sub 9 is shown in this list. Please note: the CANbus must be terminated with 120 Ohm between CAN_L and CAN_H on both ends.

PIN	Signal	description
2	CAN_L	
3	CAN_GND	GND
5	CAN_SHLD	shield
7	CAN_H	

6.6 Store the module address (identifier) in EEPROM

1. Pre-settings of both channels before AC line voltage (internal ± 24V; ± 6V) switch ON :
   ⇨ switch CONTROL [10] on MANUAL; ⇨ switch HV-ON [9] on OFF;
   ⇨ switch KILL [12] on ENABLE.
2. Switch ON of supply voltages.
3. The LCD-display [1] shows on left hand side an 'A' and on right hand side the actual address in HEX, e.g. 00. In between flash a hyphen.
4. Switching of measuring switch [3] the address will increase address step by step up to 3F , then the address jumps back to 00.
5. If there is no change during 10s or if switch CONTROL, KILL or HV-ON will be set, then the chosen address will be taken into EEPROM and the module is ready to operate.

6.7 Resetting module

The module will be reset to the factory settings with follows:

1. Setting module address unequal 00 (see point 6.6)
2. Setting module address to 00.

The module is set to the factory settings.

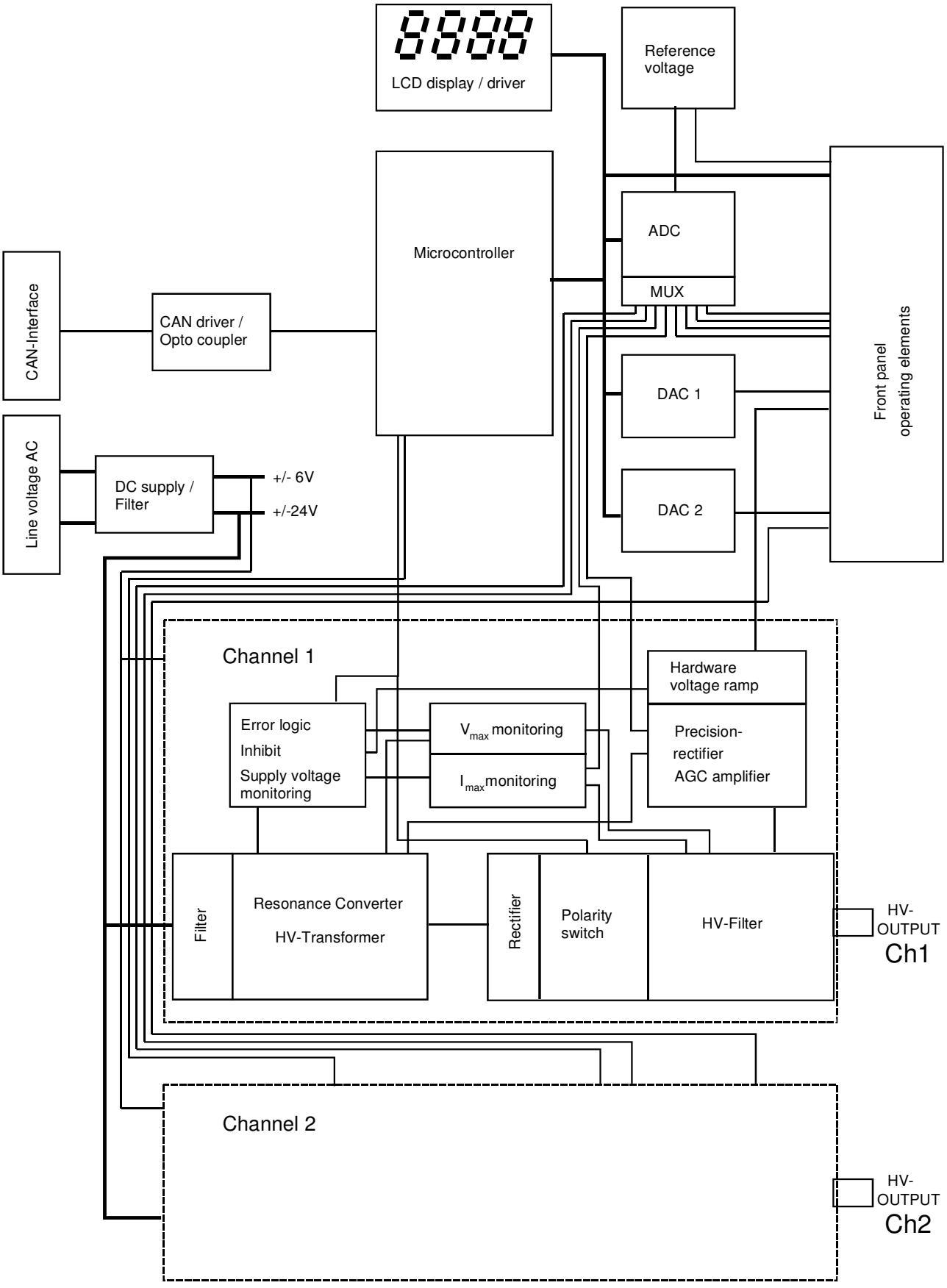
6.8 Software

Have a look also to our comfortable control and test software.

6.9 Programme example

Controller													Explanation
Transmission memory						Receiver memory							
Identi-fier	DLC	DATA_n _ID				Identi-fier	DLC	DATA_n _ID					Scheme of identifier look at 6.5
						031h	3h	D8h	01h	0Ch			Module no. 6 wants to lock on with general status o.k. at controller
030h	3h	D8h	01h	0Ch									Module is locked on as no. 6
031h	1h	99h				030h	4h	99h	14h	23h	CCh		Limits channel A ⇒ 2000 V / 6 mA (e.g. each limit 100% for SHQ 242M)
031h	1h	9Ah				030h	4h	9Ah	0Ah	21h	ECh		Limits channel B ⇒ 1000 V / 3 mA (e.g. each limit 50 % for SHQ 242M)
031h	1h	C4h				030h	3h	C4h	11h	05h			Module - Status ⇒ Channel B: ok, KILL enabled, ON V_{out} neg., DAC, V_{out} = 0 Channel A: ok, KILL disabled, ON V_{out} pos., DAC, V_{out} = 0
030h	2h	B1h	14h										Write Voltage ramp channel A with 20 V/s
030h	2h	B2h	C8h										Write voltage ramp channel B with 200 V/s
030h	4h	A1h	00h	0Bh	B8h								Set voltage channel A: 300 V ; 000BB8h = 3000 * 0,1 V
030h	4h	A2h	00h	23h	28h								Set voltage channel B: 900 V ; 002328h = 9000 * 0,1 V
030h	1h	89h											Start change voltage channel A
030h	1h	8Ah											Start change voltage channel B
031h	1h	C4h				030h	3h	C4h	70h	64h			Module - status ⇒ Channel B: ok, V_{out} in change V_{out} rising, V_{out} <> 0 Channel A: ok, V_{out} in change V_{out} rising, V_{out} <> 0
031h	1h	C8h				030h	3h	C8h	40h	04h			LAM - status ⇒ Channel B: V_{max} or I_{max} exceeded Channel A: V_{out} arrives at set voltage
031h	1h	81h				030h	5h	81h	00h	0Bh	B8h	FFh	Actual voltage channel A ⇒ 300 V 000BB8h * 10E-1 V
031h	1h	82h				030h	5h	82h	00h	00h	00h	FFh	Actual voltage channel B ⇒ 0 V 000000h * 10E-1 V
030h	4h	A2h	00h	1fh	40h								Set voltage channel B: 800 V, 001f40h = 8000*0,1 V
030	1h	8Ah											Start change voltage channel B
031h	1h	C4h				030h	3h	C4h	70h	04h			Module - Status ⇒ Channel B: ok, V_{out} in change V_{out} rising, V_{out} <> 0 Channel A: ok, V_{out} stable, V_{out} <> 0
031h	1h	C8h				030h	3h	C8h	04h	04h			LAM - Status ⇒ Channel B: V_{out} arrives at set voltage Channel A: V_{out} arrives at set voltage
031h	1h	91h				030h	5h	91h	00h	00h	21h	F9h	Actual current channel A ⇒ 3,3 µA 000021h * 10E-7 A
031h	1h	92h				030h	5h	92h	00h	2Ch	6Ch	F9h	Actual current channel B ⇒ 1,1372 mA 002C6Ch * 10E-7 A
030h	3h	A1h	00h	00h									Set voltage channel A: 0 V
030h	3h	A2h	00h	00h									Set voltage channel B: 0 V

Controller													Explanation
Transmission memory						Receiver memory							
Identi-fier	DLC	DATA_n _ID				Identi-fier	DLC	DATA_n _ID					Scheme of identifier look at 6.5
030h	1h	89h											Start change voltage channel A
030h	1h	8Ah											Start change voltage channel B
031h	1h	C8h				030h	3h	C8h	04h	04h			LAM - Status ⇒ Channel B: V_{out} arrives at set voltage Channel A: V_{out} arrives at set voltage
030h	3h	D8h	00h	0Ch									Module is locked off
						031h	3h	D8h	01h	0Ch			Module no. 6 wants to lock on with general status o.k. at controller



Appendix A: Block diagram SHQ