

## Technical information

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# VME Interface Programmers Guide

## for VHQ High Precision and Standard Modules

### Document history

Version	Date	Major changes
1.0	06.10.2011	Initial version
2.0	11.05.2016	Relayouted documentation

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# 1 VME Interface High Precision

## 1.1 VME Addressing Modes

The following VME addressing modes are available (AM = Address Modifier):

- Short supervisory access (AM = 0x2D)
- Short non-privileged access (AM = 0x29)

## 1.2 VME Interface Control

- Write function: set voltage; ramp speed; maximal output current (current trip); auto start
- Switch function: output voltage = set voltage, output voltage = 0
- Read function: set voltage; measured output voltage; ramp speed; measured output current; current trip; auto start ; voltage and current hardware limits; status

Front panel switches have priority over software control.

## 1.3 Manual Control

While the unit is operated in manual control mode, only VME read cycles are interpreted. Commands are accepted, but do not result in an output voltage change.

## 1.4 VME Command Execution Time

The VME command execution time is 2  $\mu$ s typically.

## 1.5 VME Base Address

The base address BA is permanently saved in an EEPROM.

Setting the BA:

1. Before the module is powered on by switching on the supply voltages ( $\pm 24V$ ;  $\pm 6V$ ), the following front panel switch configuration must be set for both channels:
  - switch CONTROL to MANUAL
  - switch HV to OFF
  - switch KILL to ENABLE
2. Power-on the VME to switch on the supply voltages
3. LCD shows an "A" on the left side and the high byte of the base address in HEX (e.g. "dd") on the right side, with flashing separator in between
4. The High-order nibble can be set with Channel switch, the low-order nibble with Measuring switch
5. If no changes were made within 10 s, or any other switch is changed, the selected base address is saved in EEPROM and the module is ready to operate
6. Factory setting: BA = 0xDD00

## 1.6 Register Addresses

Address Offset	Read		Write	
BA + 0x00	Status register 1			
BA + 0x04	Set voltage Channel A	(V)	Set voltage Channel A ( $0 \leq V_{\text{Set}} \leq V_{\text{Max}}$ )	(V)
BA + 0x06	Set voltage Channel A	(0.1 V)	Set voltage Channel A ( $0 \leq V_{\text{Set}} \leq V_{\text{Max}}$ )	(0.1 V)
BA + 0x08	Set voltage Channel B	(V)	Set voltage Channel B ( $0 \leq V_{\text{Set}} \leq V_{\text{Max}}$ )	(V)
BA + 0x0A	Set voltage Channel B	(0.1 V)	Set voltage Channel B ( $0 \leq V_{\text{Set}} \leq V_{\text{Max}}$ )	(0.1 V)
BA + 0x0C	Ramp speed Channel A	(V/s)	Ramp speed Channel A ( $2 \leq V_{\text{Ramp}} \leq 255$ )	(V/s)
BA + 0x10	Ramp speed Channel B	(V/s)	Ramp speed Channel B ( $2 \leq V_{\text{Ramp}} \leq 255$ )	(V/s)
BA + 0x14	Measured voltage Channel A	(V)		
BA + 0x16	Measured voltage Channel A	(0.1 V)		
BA + 0x18	Measured voltage Channel B	(V)		
BA + 0x1A	Measured voltage Channel B	(0.1 V)		
BA + 0x1C	Measured current Channel A	(0.1 $\mu$ A)		
BA + 0x1E	Measured current Channel A	<sup>*)</sup> 2MA		
BA + 0x20	Measured current Channel B	(0.1 $\mu$ A)		
BA + 0x22	Measured current Channel B	<sup>*)</sup> 2MA		
BA + 0x24	Hardware limits Channel A ( $V_{\text{Max}}, I_{\text{Max}}$ )	(%)		
BA + 0x26	Measured current Channel A	<sup>*)</sup> 2MA0n1		
BA + 0x28	Hardware limits Channel B ( $V_{\text{Max}}, I_{\text{Max}}$ )	(%)		
BA + 0x2A	Measured current Channel B	<sup>*)</sup> 2MA0n1		
BA + 0x2C	Data ready			
BA + 0x30	Status register 2			
BA + 0x34	Start voltage ramp Channel A	(V)	Start voltage ramp Channel A with data: Set voltage Channel A	(V)
BA + 0x36	Start voltage ramp Channel A	(0.1 V)	Start voltage ramp Channel A with data: Set voltage Channel A	(0.1 V)
BA + 0x38	Start voltage ramp Channel B	(V)	Start voltage ramp Channel B with data: Set voltage Channel B	(V)
BA + 0x3A	Start voltage ramp Channel B	(0.1 V)	Start voltage ramp Channel B with data: Set voltage Channel B	(0.1 V)
BA + 0x3C	Module Identifier			
BA + 0x44	Software Current Limit Channel A <sup>***)</sup>	<sup>**) (</sup> $\mu$ A)	Software current limit Channel A with data <sup>***)</sup>	<sup>**) (</sup> $\mu$ A)
BA + 0x46	Software Current Limit Channel A <sup>***)</sup>	<sup>*)</sup>	Software current limit Channel A with data <sup>***)</sup>	<sup>*)</sup>
BA + 0x48	Software Current Limit Channel B <sup>***)</sup>	<sup>**) (</sup> $\mu$ A)	Software current limit Channel B with data <sup>***)</sup>	<sup>**) (</sup> $\mu$ A)
BA + 0x4A	Software Current Limit Channel B <sup>***)</sup>	<sup>*)</sup>	Software current limit Channel B with data <sup>***)</sup>	<sup>*)</sup>

<sup>\*)</sup> Corresponding resolution in the second current measurement range:

- Option 2MA:  $I_{\text{Nom}2} = 65 \mu\text{A}$ , Resolution = 0.1  $\mu\text{A}$ , max. value = 6553.4  $\mu\text{A}$
- Option 2MA0n1:  $I_{\text{Nom}2} = 6.5 \mu\text{A}$ , Resolution = 0.1 nA, max. value = 6553.4 nA

\*\*\*) Corresponding to resolution in the first current measurement range

\*\*\*) A value of 0 disables the software current limit

## 1.7 Status Register 1 (BA + 0x00)

Channel	Bit	Name	Description	0	1
B	D15	ERROR_B	Error in Channel B	Channel ok	Error
B	D14	STATV_B	Status $V_{out}$	$V_{out}$ stable	$V_{out}$ changing
B	D13	TRENDV_B	Ramp up / down	$V_{out}$ falling	$V_{out}$ rising
B	D12	KILL_B	KILL switch setting	Disabled	Enabled
B	D11	ON_OFF_B	HV-ON/OFF switch setting	On	Off
B	D10	POL_B	Polarity $V_{out}$	Negative	Positive
B	D9	DAC_MAN_B	CONTROL switch setting	DAC	Manual
B	D8	ZEROV_B	$V_{out} = 0$	$V_{out} <> 0$	$V_{out} = 0$
A	D7	ERROR_A	Error in Channel A	Channel ok	Error
A	D6	STATV_A	Status $V_O$	$V_{out}$ stable	$V_{out}$ changing
A	D5	TRENDV_A	Ramp up / down	$V_{out}$ falling	$V_{out}$ rising
A	D4	KILL_A	KILL switch setting	Disabled	Enabled
A	D3	ON_OFF_A	HV-ON/OFF switch setting	On	Off
A	D2	POL_A	Polarity $V_{out}$	Negative	Positive
A	D1	DAC_MAN_A	CONTROL switch setting	DAC	Manual
A	D0	ZEROV_A	$V_{out} = 0$	$V_{out} <> 0$	$V_{out} = 0$

This register represents the general status of the VHQ.

ERROR\_x is generated by a logical OR of REG2ER\_x, REG1ER\_x, EXTINH\_x, RANGE\_x and ILIM\_x from "Status register 2".

ZEROV\_x is generated by a logical AND of DAC output = 0 and measured voltage < 5 V.

## 1.8 Set Voltage Channel A/B in resolution 1 V (BA + 0x04 / BA + 0x08)

Set voltage  $V_{set}$  from 0 to  $V_{nom}$  in Volt. If  $V_{set}$  is greater than  $V_{max}$  (BA + 0x24 / BA + 0x28),  $V_{set}$  is not changed.

**With option VHR:** Set Voltage Channel A/B with 0.1 V resolution (BA + 0x06 / BA + 0x0A)

Set voltage  $V_{set}$  from 0 to  $V_{nom}$  in 0.1 Volt. If  $V_{set}$  greater than  $V_{max}$  (BA + 0x24 / BA + 0x28),  $V_{set}$  is not changed.

## 1.9 Ramp Speed Channel A/B (BA + 0x0C / BA + 0x10)

Voltage ramp speed from 2 V/s to 255 V/s. All processor controlled output voltage changes are performed at this ramp speed.

## 1.10 Measured Voltage Channel A/B (BA + 0x14 / BA + 0x18)

Measured output voltage  $V_{out}$  of the channel in Volt.

**With option VHR:** Measured Voltage Channel A/B with 0.1 V resolution (BA + 0x16 / BA + 0x1A)

Measured output voltage  $V_{out}$  of the channel with 0.1 Volt resolution.

## 1.11 Measured Current Channel A/B (BA + 0x1C / BA + 0x20)

Measured output current  $I_{out}$  of the channel with 100 nA resolution, corresponding to first current measurement range  $I_{nom}$ .

**With option 2MA:** Measured Current Channel A/B with 1 nA resolution (BA + 0x1E / BA + 0x22)

Measured output current  $I_{out}$  of the channel with 1 nA resolution, corresponding to second current measurement range 65  $\mu$ A.

**With option 2MA0n1:** Measured Current Channel A/B with 100 pA resolution (BA + 0x26 / BA + 0x2A)

Measured output current  $I_{out}$  of the channel with 100 pA resolution, corresponding to second current measurement range 6.5  $\mu$ A.

## 1.12 Hardware Limits (BA + 0x24 / BA + 0x28)

D0 .. D3	Maximum output current ( $I_{max}$ ) in 10 %, hardware setting on the front panel switches
D4 .. D7	Maximum output voltage ( $V_{max}$ ) in 10 %, hardware setting on the front panel switches
D8 .. D15	0

## 1.13 Data Ready (BA + 0x2C)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	Current B	Voltage B	Current A	Voltage A

The individual bits are set once new measured data is available. The bits are deleted after the corresponding reading command.

## 1.14 Status Register 2 (BA + 0x30)

Channel	Bit	Name	Description	Remark
B	D15	REG2ER_B	Quality of output voltage currently not guaranteed	
B	D14	REG1ER_B	$I_{max}$ is or was exceeded	
B	D13	EXT_INH_B	External inhibit is or was active	
B	D12	RANGE_B	$V_{set} > V_{max}$	
B	D11	KEY_B	A frontpanel switch position was changed	ON_OFF_B, DAC_MAN_B, KILL_B
B	D10	EOP_B	$V_{out}$ has reached set value	End of process B
B	D9	ILIM_B	$I_{out}$ was greater programmed $I_{max}$	Current trip
	D8	-	-	
A	D7	REG2ER_A	Quality of output voltage currently not guaranteed	
A	D6	REG1ER_A	$I_{max}$ is or was exceeded	
A	D5	EXT_INH_A	External inhibit is or was active	
A	D4	RANGE_A	$V_{set} > V_{max}$	
A	D3	KEY_A	A front panel switch position was changed	ON_OFF_A, DAC_MAN_A, KILL_A
A	D2	EOP_A	$V_{out}$ has reached set value	End of process A
A	D1	ILIM_A	$I_{out}$ was greater programmed $I_{max}$	Current trip
	D0	TOT	Timeout error	New initialisation

The individual bits are set on the occurrence of the event. A general clear is performed after readout.

If the Output voltage was permanently switched off by exceeding  $I_{max}$  (KILL-ENABLE resp. Current trip), or EXTERNAL INHIBIT, the error bits (REG1ER\_x, EXTINH\_x, ILIM\_x) must be reset by reading "Status register 2" before an output voltage can be set again.

## 1.15 Start Voltage Ramp Channel A/B (BA + 0x34 / BA + 0x38)

Reading these registers will start the output voltage ramp to the set voltage (BA + 0x04 / BA + 0x08) with the given software ramp (BA + 0x0C / BA + 0x10). Writing a set voltage to these registers will store the data as a new set voltage (BA + 0x04 / BA + 0x08;  $V_{\text{set}} \leq V_{\text{max}}$ ) and directly start the voltage ramp.

The output voltage will not change, if some of the error conditions described below are active.

If the hardware limits  $V_{\text{max}}$  and  $I_{\text{max}}$  have been exceeded with KILL-DISABLE (limitation of the voltage/current, Error-LED on), the voltage can be lowered a single time before resetting REG1ER\_x by reading status register 2 (BA + 0x30).

The command execution can be monitored by reading status register 1 (BA + 0x00). The bits D14 (channel B), D6 (channel A) respectively are set on start of voltage change. Once the set voltage is reached the bits D10, D2 of status register 2 (BA + 0x30) are set. An interruption of the voltage change (e.g. with an external INHIBIT) can be observed from these bits (Status register 1: D14 / D6 = 0; Status register 2: D10 / D2 = 0).

### **With option VHR:** Start Voltage Ramp Channel A/B with 0.1 V resolution (BA + 0x36 / BA + 0x3A)

Writing a set voltage to these registers will store the data as a new set voltage with 0.1 Volt resolution (BA + 0x06 / BA + 0x0A;  $V_{\text{set}} \leq V_{\text{max}}$ ) and directly start the voltage ramp.

## 1.16 Module Serial Number (BA + 0x3C)

D15 .. D0      Four digit serial number, BCD coded

## 1.17 Current Trip Channel A/B (BA + 0x44 / BA + 0x48)

Reading these registers will return the programmed maximum output current in the corresponding current resolution. If the measured output current exceeds the programmed limit, the output voltage will be shut down permanently (Current Trip). The response time for this is between 20 and 60 ms.

A current trip is set by writing a current value in the corresponding current resolution. A current trip value of 0 deactivates the current trip function.

The hardware current limit ( $I_{\max}$ ) limits the current independently of the software trip.

### **With option 2MA or 2MA0n1: Software Current Limit (BA + 0x46 / BA + 0x4A)**

The maximum output current corresponding to the resolution of the second current measurement range. If the output current exceeds the programmed limit, the output voltage will be shut down permanently (Current Trip). The response time for this is between 20 and 60 ms.

A current trip is set by writing a current value in the corresponding current resolution of the second current measurement range.

A current trip value of 0 deactivates the current trip function.

## 2 VME Interface Standard

### 2.1 VME Addressing Modes

The following VME addressing modes are available (AM = Address Modifier):

- Short supervisory access (AM = 0x2D)
- Short non-privileged access (AM = 0x29)

### 2.2 VME Interface Control

- Write function: set voltage; ramp speed; maximal output current (current trip); auto start
- Switch function: output voltage = set voltage, output voltage = 0
- Read function: set voltage; measured output voltage; ramp speed; measured output current; current trip; auto start; hardware limits current and voltage; status

Front panel switches have priority over software control.

### 2.3 Manual control

While the unit is operated in manual control mode, only VME read cycles are interpreted. Commands are accepted, but do not result in an output voltage change.

### 2.4 Command Execution Time

The command execution time is 2  $\mu$ s typically.

### 2.5 VME Base Address

The base address BA is permanently saved in an EEPROM.

Setting the BA:

1. Before the module is powered on by switching on the supply voltages ( $\pm 24V$ ;  $\pm 6V$ ), the following front panel switch configuration must be set for both channels:
  - switch CONTROL to MANUAL
  - switch HV to OFF
  - switch KILL to ENABLE
2. Power-on the VME to switch on the supply voltages
3. LCD shows an "A" on the left side and the high byte of the base address in HEX (e.g. "dd") on the right side, with flashing separator in between
4. The High-order nibble can be set with Channel switch, the low-order nibble with Measuring switch
5. If no changes were made within 10 s, or any other switch is changed, the selected base address is saved in EEPROM and the module is ready to operate
6. Factory setting: BA = 0xDD00

## 2.6 Register Addresses

Address Offset	Read		Write	
BA + 0x00	Status register 1			
BA + 0x04	Set voltage Channel A	(V)	Set voltage Channel A ( $0 \leq V_{Set} \leq V_{Max}$ )	(V)
BA + 0x08	Set voltage Channel B	(V)	Set voltage Channel B ( $0 \leq V_{Set} \leq V_{Max}$ )	(V)
BA + 0x0C	Ramp speed Channel A	(V/s)	Ramp speed Channel A ( $2 \leq V_{Ramp} \leq 255$ )	(V/s)
BA + 0x10	Ramp speed Channel B	(V/s)	Ramp speed Channel B ( $2 \leq V_{Ramp} \leq 255$ )	(V/s)
BA + 0x14	Measured Voltage Channel A	(V)		
BA + 0x18	Measured Voltage Channel B	(V)		
BA + 0x1C	Measured current Channel A	*)		
BA + 0x20	Measured current Channel B	*)		
BA + 0x24	Hardware limits Channel A ( $V_{Max}, I_{Max}$ )			
BA + 0x28	Hardware limits Channel B ( $V_{Max}, I_{Max}$ )			
BA + 0x2C	Data ready			
BA + 0x30	Status register 2			
BA + 0x34	Start voltage ramp Channel A		Start voltage ramp Channel A with data: Set voltage Channel A	(V)
BA + 0x38	Start voltage ramp Channel B		Start voltage ramp Channel B with data: Set voltage Channel B	(V)
BA + 0x3C	Module identifier			
BA + 0x44	Software current limit Channel A **)	*)	Software current limit Channel A with data **)	*)
BA + 0x48	Software current limit Channel B **)	*)	Software current limit Channel B with data **)	*)

\*) Corresponding to current resolution

\*\*) A value of 0 disables the software current limit

## 2.7 Status Register 1 (BA + 0x00)

Channel	Bit	Name	Description	0	1
B	D15	ERROR_B	Error on Channel B	Channel ok	Error
B	D14	STATV_B	Status $V_{out}$	$V_{out}$ stable	$V_{out}$ changing
B	D13	TRENDV_B	Ramp up / down	$V_{out}$ falling	$V_{out}$ rising
B	D12	KILL_B	KILL switch setting	Disabled	Enabled
B	D11	ON_OFF_B	HV-ON/OFF switch setting	On	Off
B	D10	POL_B	Polarity $V_{out}$	Negative	Positive
B	D9	DAC_MAN_B	CONTROL switch setting	DAC	Manual
B	D8	ZEROV_B	$V_{out} = 0$	$V_{out} <> 0$	$V_{out} = 0$
A	D7	ERROR_A	Error on Channel A	Channel ok	Error
A	D6	STATV_A	Status $V_{out}$	$V_{out}$ stable	$V_{out}$ changing
A	D5	TRENDV_A	Ramp up / down	$V_{out}$ falling	$V_{out}$ rising
A	D4	KILL_A	KILL switch setting	Disabled	Enabled
A	D3	ON_OFF_A	HV-ON/OFF switch setting	On	Off
A	D2	POL_A	Polarity $V_{out}$	Negative	Positive
A	D1	DAC_MAN_A	CONTROL switch setting	DAC	Manual
A	D0	ZEROV_A	$V_{out} = 0$	$V_{out} <> 0$	$V_{out} = 0$

This register represents the general status of the VHQ.

ERROR\_x is generated by a logical OR of REG2ER\_x, REG1ER\_x, EXTINH\_x, RANGE\_x and ILIM\_x from "Status register 2".

ZEROV\_x is generated by a logical AND of DAC output = 0 and measured voltage < 5 V.

## 2.8 Set Voltage Channel A/B (BA + 0x04 / BA + 0x08)

Set voltage  $V_{set}$  from 0 to  $V_{max}$  in Volt. If  $V_{set}$  is greater than  $V_{max}$  (BA + 0x24 / BA + 0x28),  $V_{set}$  is not changed.

## 2.9 Ramp Speed Channel A/B (BA + 0x0C / BA + 0x10)

Voltage ramp speed from 2 V/s to 255 V/s. All processor controlled output voltage changes are performed at this ramp speed.

## 2.10 Measured Voltage Channel A/B (BA + 0x14 / BA + 0x18)

Measured output voltage  $V_{out}$  of the channel in Volt.

## 2.11 Measured Current Channel A/B (BA + 0x1C / BA + 0x20)

Measured output current  $I_{out}$  of the channel in the corresponding current resolution.

## 2.12 Hardware Limits (BA + 0x24 / BA + 0x28)

D0 .. D3 Maximum output current ( $I_{max}$ ) in 10 %, hardware setting on the front panel switches

D4 .. D7 Maximum output voltage ( $V_{max}$ ) in 10 %, hardware setting on the front panel switches

D8 .. D15 0

## 2.13 Data Ready (BA + 0x2C)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	Current B	Voltage B	Current A	Voltage A

The individual bits are set once new measured data is available. The bits are deleted after the corresponding reading command.

## 2.14 Status Register 2 (BA + 0x30)

Channel	Bit	Name	Description	Remark
B	D15	REG2ER_B	Quality of output voltage currently not guaranteed	
B	D14	REG1ER_B	$V_{max}$ or $I_{max}$ is or was exceeded	
B	D13	EXT_INH_B	External inhibit is or was active	
B	D12	RANGE_B	$V_{set} > V_{max}$	
B	D11	KEY_B	A front panel switch position was changed	ON_OFF_B, DAC_MAN_B, KILL_B
B	D10	EOP_B	$V_{out}$ has reached set value	End of process B
B	D9	ILIM_B	$I_{out}$ was greater programmed $I_{max}$	Current trip
B	D8	-	-	
A	D7	REG2ER_A	Quality of output voltage currently not guaranteed	
A	D6	REG1ER_A	$V_{max}$ or $I_{max}$ is or was exceeded	
A	D5	EXT_INH_A	External inhibit is or was active	
A	D4	RANGE_A	$V_{set} > V_{max}$	
A	D3	KEY_A	A front panel switch position was changed	ON_OFF_A, DAC_MAN_A, KILL_A
A	D2	EOP_A	$V_{out}$ has reached set value	End of process A
A	D1	ILIM_A	$I_{out}$ was greater programmed $I_{max}$	Current trip
A	D0	TOT	Timeout error	New initialization

The individual bits are set on the occurrence of the event. A general clear is performed after readout.

If the Output voltage was permanently switched off by exceeding  $V_{max}$  or  $I_{max}$  (KILL-ENABLE resp. Current trip), or INHIBIT respectively, the error bits (REG1ER\_x, EXTINH\_x, ILIM\_x) have to be reset by reading " Status register 2" before an output voltage can be set again.

## 2.15 Start Voltage Ramp in Channel A/B (BA + 0x34 / BA + 0x38)

Reading these registers will start the output voltage ramp to the set voltage (BA + 0x04 / BA + 0x08) with the given software ramp (BA + 0x0C / BA + 0x10). Writing a set voltage to these registers will store the data as a new set voltage (BA + 0x04 / BA + 0x08;  $V_{set} \leq V_{max}$ ) and directly start the voltage ramp.

The output voltage will not change, if some of the error conditions described below are active.

If the hardware limits  $V_{max}$  and  $I_{max}$  have been exceeded with KILL-DISABLE (limitation of the voltage/current, Error-LED on), the voltage can be lowered a single time before resetting REG1ER\_x by reading status register 2 (BA + 0x30).

The command execution can be monitored by reading status register 1 (BA + 0x00). The bits D14 (channel B), D6 (channel A) respectively are set on start of voltage change. Once the set voltage is reached the bits D10, D2 of status register 2 (BA + 0x30) are set. An interruption of the voltage change (e.g. with an external INHIBIT) can be observed from these bits (status register 1: D14 / D6 = 0; status register 2: D10 / D2 = 0).

## 2.16 Module Identifier (BA + 0x3C)

D15 .. D0 Four digit serial number, BCD-coded

## 2.17 Current Trip Channel A/B (BA + 0x44 / BA + 0x48)

Reading these registers will return the programmed maximum output current in the corresponding current resolution. If the output current exceeds the programmed limit, the output voltage will be shut down permanently (Current trip). The response time for this is between 20 and 60 ms.

A current trip is set by writing a current value in the corresponding current resolution. A current trip value of 0 deactivates the current trip function.

The hardware current limit ( $I_{\max}$ ) limits the current independently of the software trip.

### 3 Manufacturers Contact

**iseq Spezialelektronik GmbH**

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