

RED BOX DETECTION CIRCUIT

A PRACTICAL USE FOR A "TOLL FRAUD" DEVICE

KINGPIN
LOPHT HEAVY INDUSTRIES

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OVERVIEW

In light of Bernie S.'s misfortune, I doubt it would do any good to tell police that your Red Box (a.k.a. A "Toll Fraud" Device) was really being used to turn on your TV, start your car, or shut off your lights (clap on, clap off). Despite this disappointing fact, this circuit can be used in a multitude of applications and truly does give you a legitimate reason to possess this type of multi-frequency generator.

The Red Box Detection Circuit can be used for practical everyday use or for security purposes. Using this circuit, you could trigger household appliances (turn on the disco ball, vibrating bed, etc.) using a nickel, dime, or quarter tone, which all are generated with 1700Hz and 2200Hz. Essentially, the Detection Circuit behaves like "The Clapper", which turns the lights on with one clap, leaving them on until another clap is detected. The device is timing-independent, so any coin type will be detected and produce the same result. From a security standpoint, telephone companies can use this as a cheap method to detect the Red Box tones, and police officers can have a portable unit to test "Toll Fraud" devices in the field (which will hopefully never happen, but it is a very real possibility as Red Boxes become more and more widespread into the mainstream).

The heart of this circuit is the MX-COM MX105A. This chip is a tone detector for use in single and multitone signalling systems. Key reasons for using this part is that it requires minimal external components and recognizes tones in the presence of high noise levels. An LM386 Low Voltage Audio Power Amplifier is used to bring the audio signal from the microphone to a proper input level for the MX105A. The data sheets provided with the MX105A are very descript and make design fairly straightforward. A 7474 D-Type Positive Edge Flip-Flop takes the "Detect Out" signal from the MX105A and acts as a switch, leaving the final detect state high (or low) until another Red Box tone is detected, which will then complement the logic state.

CIRCUIT THEORY

I will explain the basic design of this circuit from input to output, starting with the audio amplification, into the tone detector, and through the logic of the flip-flop. The power to the circuit is supplied by a standard 9V battery, connected to a 7805 voltage regulator (U4). This gives us a clean 5V to power the tone detector and flip-flop, and a not-so-clean 9V (approximately) to power the audio amp and microphone. The microphone (a common electret, X1) needs to be supplied a voltage in order for it to function correctly, so we drive 9V through a 510K resistor (R1) into the positive wire. The resistor will limit the current of the 9V supply to protect the microphone. The LM386 amplifier (U1) has a gain internally set to 20 (26dB increase), which is too small for our application. By adding a 10uF capacitor (C1) across pins 1 and 8, we can increase the gain to 200 (46dB increase). The audio amplifier section of the Red Box Detection circuit is very simple, and uses only three external components. R2, the 10k potentiometer, will limit the input voltage to the audio amp. This will be adjusted, upon testing of the module, to give us a clean, unsaturated, amplified signal. The output of the amp goes through a coupling capacitor (C2) and feeds into pin 1 (Tone In) of the MX105A Tone Decoder.

Calculating the values of external components for the MX105A (U2) is done in a series of simple mathematical equations, all described in the data sheet. The first step is to define the MX105A to respond to a center frequency, f_o , of either 1700Hz or 2200Hz, both of which make up the “Red Box” tone. I chose to have the circuit detect 1700Hz, leading to an operating bandwidth of 8.25%, giving us a 140Hz cushion to allow for small variances in frequency production from your particular flavor of “Red Box”. We also need to define the maximum allowed response time of the circuit, which is the maximum amount of time the circuit has to detect the tone. Using common, off-the-shelf component values, we can get a maximum response time of 31.1ms. This yields a lock time of 10.7ms and a detection time of 20.4ms. There are also formulas included in the data sheet to calculate signal-to-noise performance and to modify the de-response time of the circuit. The latter is the time the MX105A will take to turn off after a valid in-band signal has been removed from the input. This may be helpful, depending on what you are interfacing your circuit to. In the schematic provided, you need not worry about de-response time, since it is taken care of by the flip-flop circuitry. All of the component values can be approximated to a close off-the-shelf equivalent, with the exception of R5. This potentiometer is a major component in setting the free running frequency of the VCO and plays a direct role in setting f_o . R5 was calculated to be 636.6k, but the actual value you need may be slightly different, because of tolerances in component values. Setting R5 is the last step to testing the circuit, since you can “tune” it to only respond to 1700Hz. The construction of the tone detector module of the circuit is simple as well, but requires a few more external components.

The final module of the unit is the flip-flop circuitry. This will use the Detect Out pin of the MX105A as input to the clock of the 7474 (U3) and respond accordingly. The power connections to the flip-flop are not included in the schematic, so be sure to connect +5V to pin 14 and GND to pin 7 (standard power connection for a digital logic device). The MX105A only raises the logic of Detect Out for a brief moment, but we need to have the

final detect state remain on or off until another valid frequency is detected. The D-type flip-flop detects a positive-edge of the clock, which is a low-to-high transition, and complements the state of the output pin. The low-to-high transition of the Detect Out pin only occurs once per valid tone detection, so each time a red box tone is detected, the output of the flip-flop will either turn on or turn off. We now have a “Clapper”-compatible circuit.

TESTING AND TROUBLESHOOTING

It is a good idea to test each of the “modules” (defined by dotted boxes on the schematic) before building the whole circuit. Using the provided schematic, construction is very easy. I would suggest using a prototype board for your first draft of the circuit, which makes it easy to exchange components and fine-tune your project for your particular needs. Common mistakes in constructing the amplifier circuit include not driving the input of the microphone with a voltage, or doing so incorrectly. Also remember to connect all ground references together. Double check all your connections and make sure the components are receiving the correct supply voltages.

To test the functionality of the tone detection circuit, connect a 1k resistor (R8) in series with an LED (D1) to pin 9 (Detect Out), or hook to an oscilloscope or logic analyzer to monitor the state of this pin. Drive the microphone with a Red Box or audio tone generator. If everything is working correctly, the Detect Out pin will go high briefly, upon detection of a correct tone (1700Hz), thus lighting the LED. The only crucial component in the tone detection module is R5, which, as mentioned before, sets the center frequency of the circuit.

There is not much that can go wrong with the circuit, so when troubleshooting, remember to Keep It Simple, Stupid. The problem is most likely a result of a shorted, improper, or loose connection.

CONCLUSION AND OTHER IDEAS

Much more could be said about the Red Box Detection Circuit, and those interested in modifying it for other uses should feel free. Take a look at the data sheets for more technical data than you will ever need. A useful idea for this circuit would be to connect an NPN transistor (2N2222) to the output of the flip-flop and drive a 120VAC relay to operate standard outlet-powered equipment and appliances. Another useful idea would be to interface the unit with a telephone line, and use it as an access device for your voice mail or answering machine, or turning appliances on and off remotely. You could also modify the circuit to detect both the 1700Hz and 2200Hz frequencies generated by the Red Box for greater accuracy. A more complicated idea would be to make the circuit timing-dependent, detecting the timing differences between the nickel, dime, and quarter tones, and perform a different function for each. A previous letter to the editor asked about "Red Boxing" a video game to get free credits. As stupid as that question sounds, it can now be done (with your own modified arcade game, of course), and it is sure to impress your friends.

This article is just a brief glimpse of what can be done and I hope it has brought into the light the possibilities of electronics. Although this circuit is silly, it could be used for practical or security purposes, and if you disagree, you can still learn quite a bit by experimenting with it.

MX-COM, INC.	http://www.mxcom.com	800-638-5577
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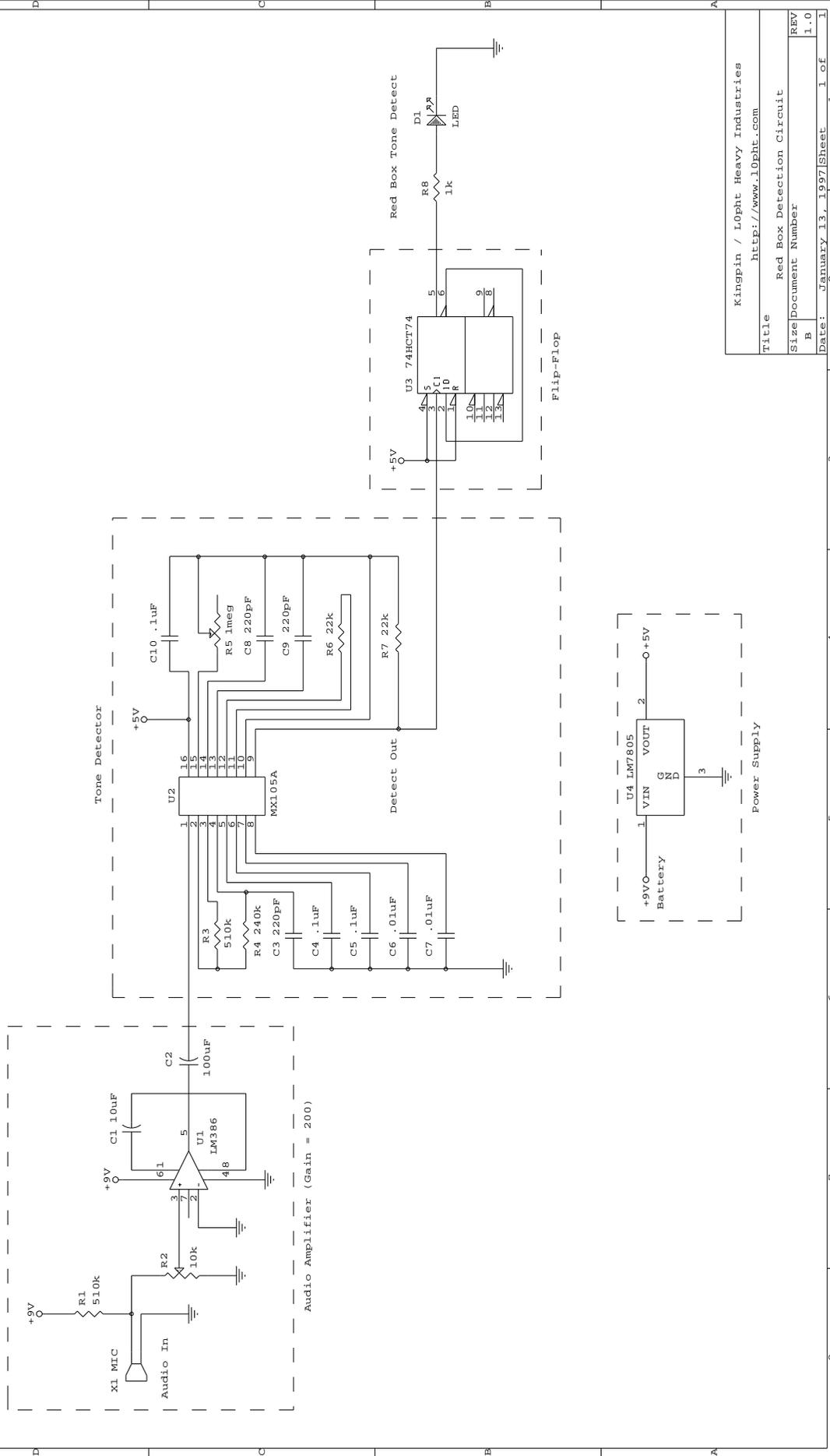
PDF formatted data sheets can be found at the above locations for the MX105A, LM386, and 7474.

Questions and comments can be directed to kingpin@2600.com or kingpin@l0pht.com. A re-print of this article, along with data sheets and schematics, can be found at <http://www.l0pht.com/~kingpin>

END OF TRANSMISSION

BILL OF MATERIALS

Item	Quantity	Reference	Part
1	1	C1	10uF
2	1	C2	100uF
3	3	C3,C8,C9	220pF
4	3	C4,C5,C10	.1uF
5	2	C6,C7	.01uF
6	1	D1	LED
7	2	R1,R3	510k
8	1	R2	10k
9	1	R4	240k
10	1	R5	1meg
11	2	R6,R7	22k
12	1	R8	1k
13	1	U1	LM386
14	1	U2	MX105A
15	1	U3	74HCT74
16	1	U4	LM7805
17	1	X1	MIC



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Red Box Detection Circuit	
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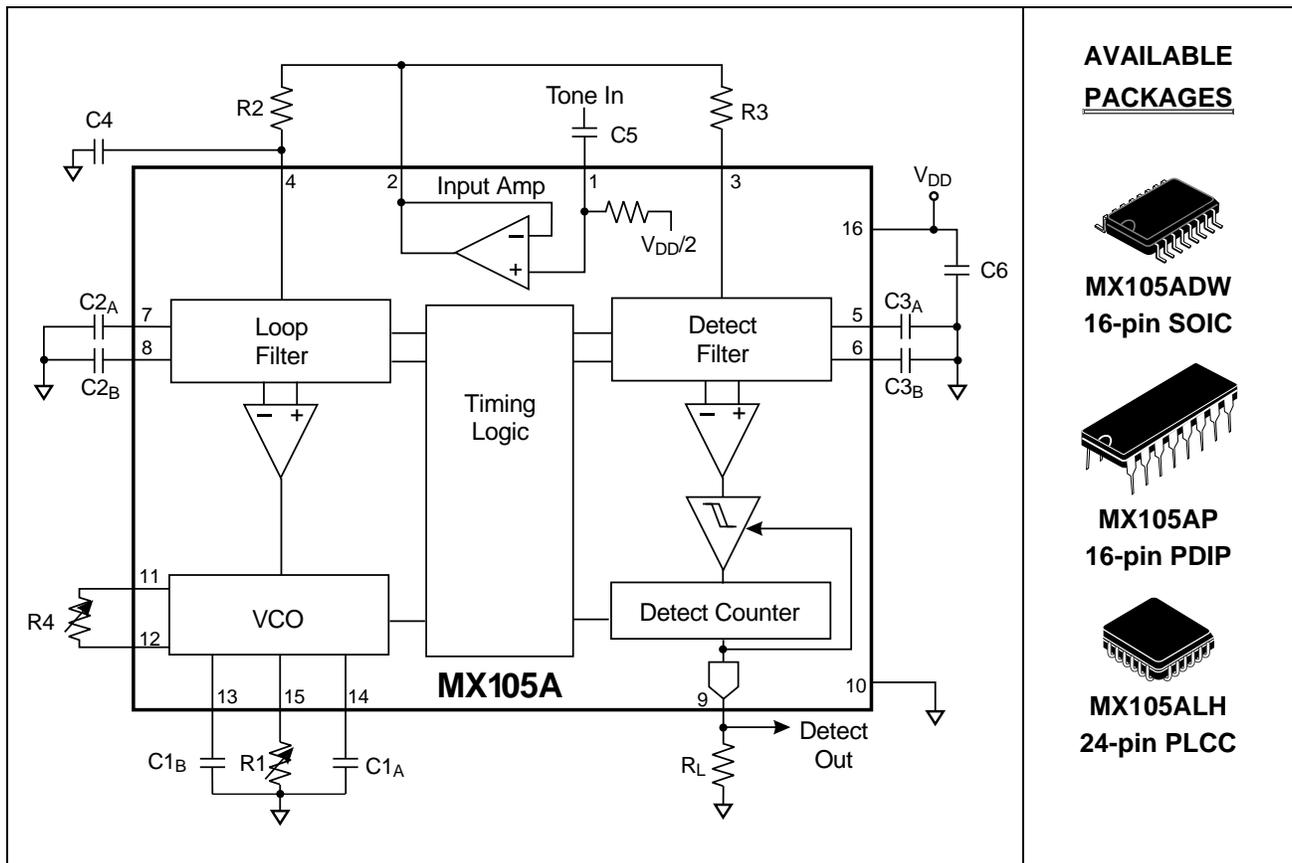
MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX105A Tone Detector

PRELIMINARY INFORMATION

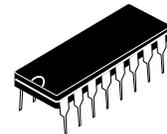
- Operates in High Noise Conditions
- ≥ 36 dB Signal Input Range
- High Sensitivity
- Low Power
- Adjustable Bandwidth
- Adjustable Frequency
- Wide Voltage Range (2.7 V to 5.5 V)
- Single and Multitone System Applications



AVAILABLE PACKAGES



MX105ADW
16-pin SOIC



MX105AP
16-pin PDIP



MX105ALH
24-pin PLCC

The MX105A is a monolithic CMOS tone detector for tone decoding in single and multitone signaling systems. Using phase locked loop (PLL) decoding techniques, the MX105A recognizes tones in the presence of high noise levels and strong adjacent channel tones. Detection frequency and bandwidth can each be independently adjusted. The design is immune to high levels of harmonic and sub-harmonic noise. It also maintains excellent noise immunity and constant bandwidth over a wide range of input signal levels.

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1. Block Diagram

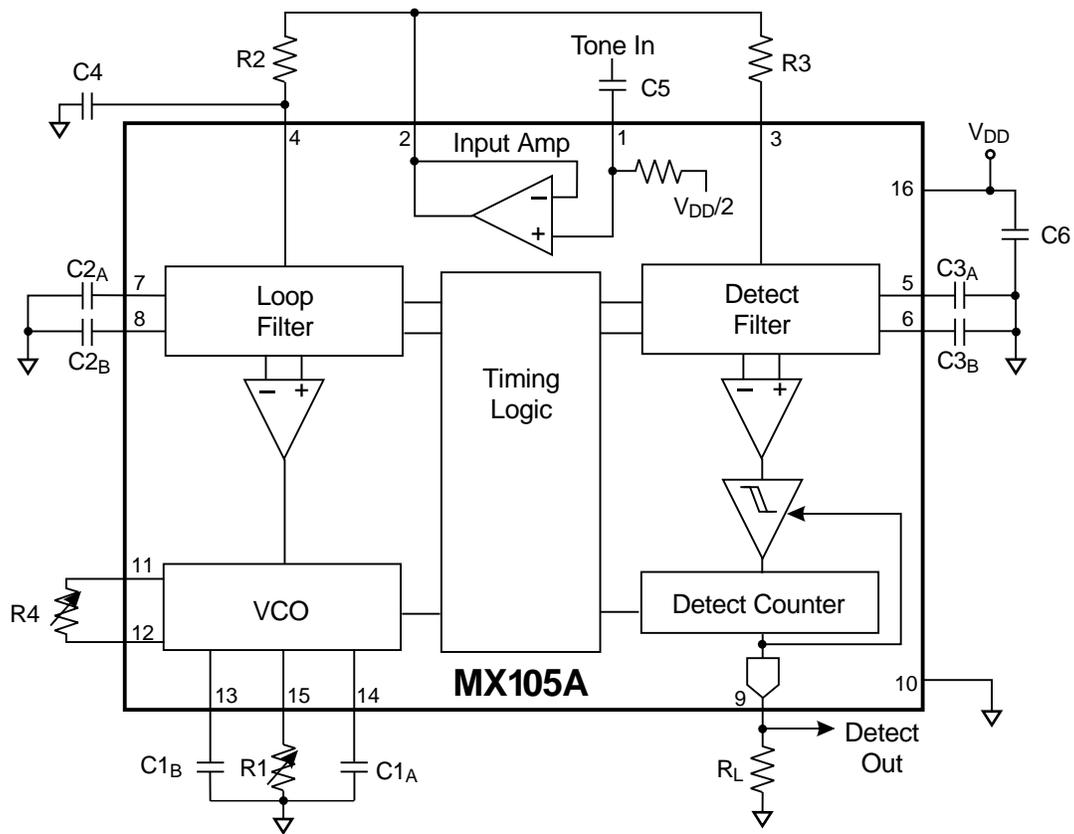


Figure 1: Block Diagram

2. Signal List

Pin No.	Pin No.	Name	Type	Description
DW/P	LH			
1	1	INPUT AMP IN	input	AC couple to this input. Nominal input impedance is 200 k Ω .
2	3	INPUT AMP OUT	output	Nominal output impedance is 1 k Ω .
3	5	R3	input	Detect filter resistor pin.
4	6	R2	input	PLL loop filter resistor pin. For improved performance C4 may be chosen to provide 30° of phase shift at the loop filter input.
5	7	C3 _A	output	Detect filter capacitor pin A
6	8	C3 _B	output	Detect filter capacitor pin B
7	10	C2 _A	output	Loop filter capacitor pin A
8	11	C2 _B	output	Loop filter capacitor pin B
9	13	DETECT OUT	output	PMOS open drain output - active on detect.
10	14	V _{SS}	power	Ground.
11	16	R4 _A	input	Bandwidth control resistor pin A
12	17	R4 _B	input	Bandwidth control resistor pin B
13	19	C1 _B	output	VCO capacitor B
14	20	C1 _A	output	VCO capacitor A
15	22	R1	input	VCO discharge resistor. When potentiometer tuning is required, a series resistor is recommend to prevent possible shorting to ground.
16	24	V _{DD}	power	Power supply.

3. General Description

The MX105A implements a frequency detector with a phase locked loop (PLL) and a lock detector. The voltage controlled oscillator (VCO) center frequency, detection bandwidth, loop filter, and detect filter are all independently controlled by external components.

The MX105A provides a pair of pseudo-sinewave multipliers for splitting the input signal into approximately orthogonal components. These multipliers are implemented with commutating filters (cyclically sampling filters) which translate an in band AC input signal to DC. The commutating loop filter is used as the phase detector of the PLL while the commutating detect filter provides for lock detection. Each pseudo-sinewave has a cyclic form (1 1 0 -1 -1 0) to eliminate low order harmonic responses. The loop filter produces an error signal, which when applied to the VCO input allows frequency locking. A limiter between the loop filter output and the VCO input provides tunable control of the detection bandwidth (BW). Once lock is achieved the detect filter produces a DC value proportional to the input tone amplitude. An internally generated reference is compared to the detect filter output to determine whether the PLL is locked to an input tone. Once lock is determined the internal reference is reduced by 50% to minimize output chatter with marginal input signals.

The sampling clocks of the detect filter lag those of the loop filter by 60°. To improve performance, a capacitor (C4) can be used to phase shift the input to the loop filter by 30°. This shifts all sampling clocks an additional 30° relative to the input tone to phase align the detect filter sampling clocks with the amplitude peaks of the input tone.

Figure 2 shows the sampling clocks relative to an in band input tone; this figure represents the steady state 'locked' condition without C4.

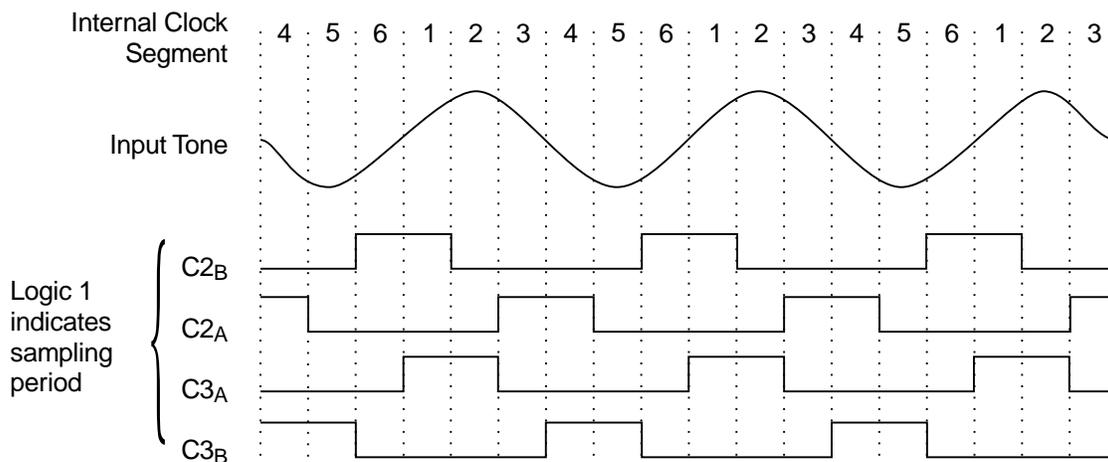


Figure 2: Sampling Clocks of Commutating Filters

4. External Components

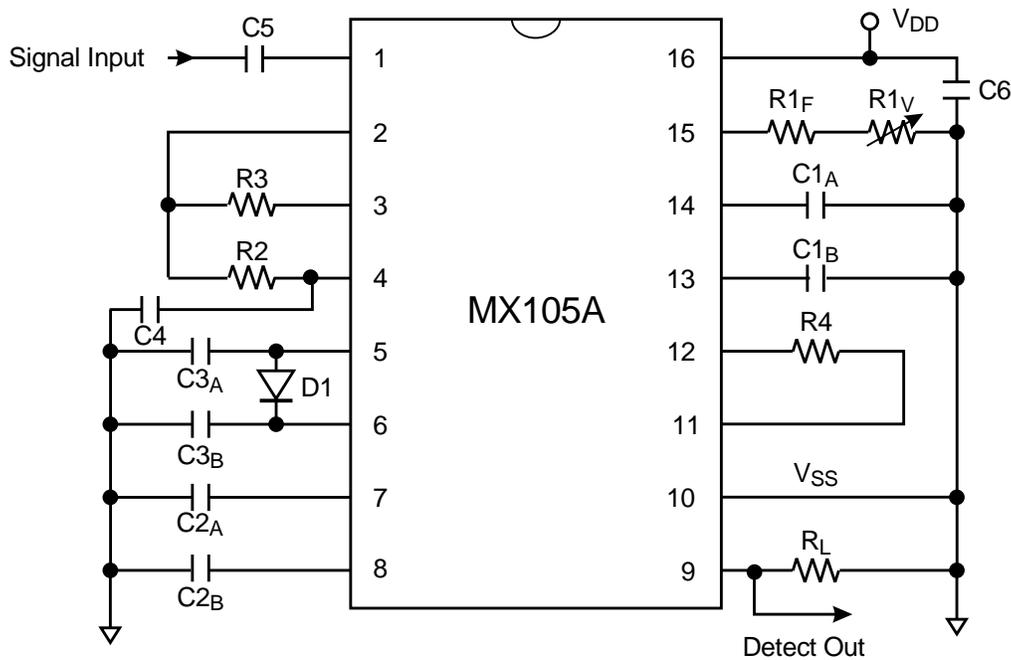


Figure 3: Recommended External Components

R _{1F}	See Section 5.1	300kΩ	
R _{1V}	See Section 5.1	100kΩ	
R ₂	See Section 5.5		
R ₃	See Section 5.7		
R ₄	See Section 5.4		
R _L	Note 4	20kΩ	±20%
C _{1A}	See Section 5.1 Note 2		
C _{1B}	See Section 5.1 Note 2		

C _{2A}	See section 5.5 Note 2		
C _{2B}	See Section 5.5 Note 2		
C _{3A}	See Section 5.7 Note 2		
C _{3B}	See Section 5.7 Note 2		
C ₄	See Section 5.10 Note 1, 2		
C ₅		0.27μF	±20%
C ₆		0.1μF	±20%
D ₁	See Section 5.8 Note 3	small signal diode (1N914)	

External Components Notes:

- For improved performance, C₄ may be chosen to provide 30° phase shift at the VCO loop filter input.
- For compatibility with the MX105; capacitors (C₁ - C₄) may be connected to V_{DD} instead of V_{SS}.
- For improved de-response time, a diode (D₁) may be added.
- Any value load resistance (R_L) may be used, providing the maximum load current does not exceed the value given in 'Maximum Ratings Specifications'.

The external components shown in Figure 3 are used to adjust the various performance parameters of the MX105A. The signal-to-noise performance, response time and signal bandwidth are all interrelated factors which should be optimized to meet the requirements of the application.

By selecting component values in accordance with the following formulas, optimum circuit performance is obtained for any given application.

First define the following application parameters:

- A. The center frequency to be detected (f_0).
- B. The MX105A Minimum Usable Bandwidth (MUBW). This is obtained by taking into account the worst case tolerances on the input tone frequency and variations in the MX105A f_0 due to supply voltage and any temperature effect of the MX105A and its supporting components.
- C. The maximum permissible MX105A response time.
- D. The minimum input signal amplitude.

Note: Using this information the appropriate component values can be calculated, and the signal-to-noise performance can be read from a chart. Do not add large safety margins for response time and minimum signal amplitude; reasonable margins are already included in the formulas. Excessive margins may result in reduced noise immunity.

5. Method for Calculating External Component Values

The examples on the following pages demonstrate the calculation of component values for any given application. For the purpose of the examples, the values below are used:

- A. $f_0 = 2800$ Hz
- B. $\Delta\text{TEMP} = 100$ °C, $\Delta V_{DD} = 1$ V, $\Delta f_{IN} = 0.5\%$
- C. Maximum allowed response time = 50ms
- D. Minimum input signal amplitude = 200 mV_{RMS}.

5.1 Define f_0

The components R_1 , C_{1A} and C_{1B} set the free running frequency of the VCO and therefore the f_0 of the MX105A. As shown below, the frequency of 2800 Hz corresponds to a capacitor value of 220pF and a resistor value of 385 k Ω . This resistance can be achieved with a 300 k Ω fixed resistor for R_{1F} and for R_{1V} a 100 k Ω potentiometer. The capacitance of C_{1A} and C_{1B} should include 10-20pF parasitic capacitance due to the device and its package plus any board parasitic capacitance.

$$f_0 = \frac{1}{K \cdot R_1(C_{1A} + C_{1B})} \Rightarrow R_1 \times C_{1A} = \frac{1}{2Kf_0}$$

$$\begin{aligned} \text{where : } K &= 2.1 \pm 5\% \\ R_1 &= (R_{1F} + R_{1V}) \end{aligned}$$

5.2 Calculate Minimum Usable Bandwidth

Minimum Usable Bandwidth (MUBW) is the TOTAL bandwidth required for the following:

- A. Input signal frequency tolerance
- B. MX105A f_0 temperature coefficient ($T_C = 100$ ppm/°C)
- C. MX105A f_0 supply voltage coefficient ($V_C = 5000$ ppm/V)

Note: Add A, B and C and express as TOTAL bandwidth, not as a \pm percentage (%) value.

$$\begin{aligned} \text{MUBW} &= \Delta f_0 + T_C \Delta\text{TEMP} + V_C \Delta V \\ \text{MUBW} &= 0.5 + 0.01 \times 100 + 0.5 \times 1 = 2\% \end{aligned}$$

5.3 Calculate The Recommended Operating Bandwidth

$$\text{BW} = \frac{10 + \text{MUBW}}{2} = \frac{10 + 2}{2} = 6\%$$

5.4 Select R4 for Operating BW

$$R4 = \frac{4.8 \times BW}{10.35 - BW} = \frac{4.8 \times 6}{10.35 - 6} \approx 6.8k\Omega$$

The exact bandwidth given by any value of R4 will vary slightly. In applications where an exact bandwidth is required, R4 should be a variable resistor to permit adjustment.

5.5 Calculate R2×C2_A

$$R2 \times C2_A \approx \frac{100}{3 \times f_0 \times BW}$$

For a frequency of 2800 Hz, a bandwidth of 6%, and a choice of C2_A = 0.01μF ⇒ R_V = 200kΩ.

Note: Use nearest preferred values.

5.6 Define Maximum Allowed Response Time

The maximum response time (T_{ON}) is the sum of the VCO lock time (T_{LOCK}) and the DETECT integration time (T_{DETECT}). The MX105A's T_{ON} must not exceed the maximum time allowed for the application, but a value lying near the maximum gives the best S/N performance.

A. Calculate T_{LOCK}

$$T_{LOCK} = \frac{150}{f_0 \times BW}$$

Using the formula above, for a frequency of 2800 Hz and a bandwidth of 6% the approximate Lock time (T_{LOCK}) will be 9 ms. Since the maximum response time is 50 ms, a DETECT time of 41 ms is allowed.

Note: T_{LOCK} may vary from near zero to the value given, causing corresponding variations in actual T_{ON}.

B. Calculate Maximum Allowable T_{DETECT}

$$T_{DETECT} = T_{ONMAX} - T_{LOCK}$$

C. Define Minimum Expected Signal Amplitude (V_{INMIN})

This is used in calculating T_{DETECT} components.

5.7 Calculate R3×C3_A

$$R3 \times C3_A \approx \frac{T_{DETECT}}{-3 \times \ln \left(1 - \frac{V_{TH}}{V_{INMIN}} \right)}$$

where: V_{TH} is the detect filter sensitivity.

Note:

1. For a signal amplitude of 200 mV_{RMS}, a resistor value R3 of 510 kΩ with a 0.1mF capacitor for C3_A and C3_B will yield a T_{DETECT} time of 20ms. This in turn yields a response time of 9ms + 20 ms = 29ms.
2. Use nearest preferred values.

5.8 Calculate Maximum De-response Time

$$T_{\text{OFF}} \approx -3 \times \ln\left(\frac{V_{\text{TH}}}{V_{\text{INMAX}}}\right) \cdot R3 \times C3_A$$

where: V_{TH} is the detect filter sensitivity.

For improved de-response time, a diode (1N914 or similar) can be placed between pins 5 and 6, as shown in Figure 3. The formula and figure below show the approximate time the MX105A will take to turn off after an in-band signal has been removed. The effect of this diode is to greatly reduce the turn-off time with signal input amplitudes greater than 300 mV_{RMS}. This graph is for $V_{\text{DD}} = 5\text{V}$; for lower V_{DD} KDT increases.

$$T_{\text{OFF}} \approx K_{\text{DT}} \times R3 \times C3_A$$

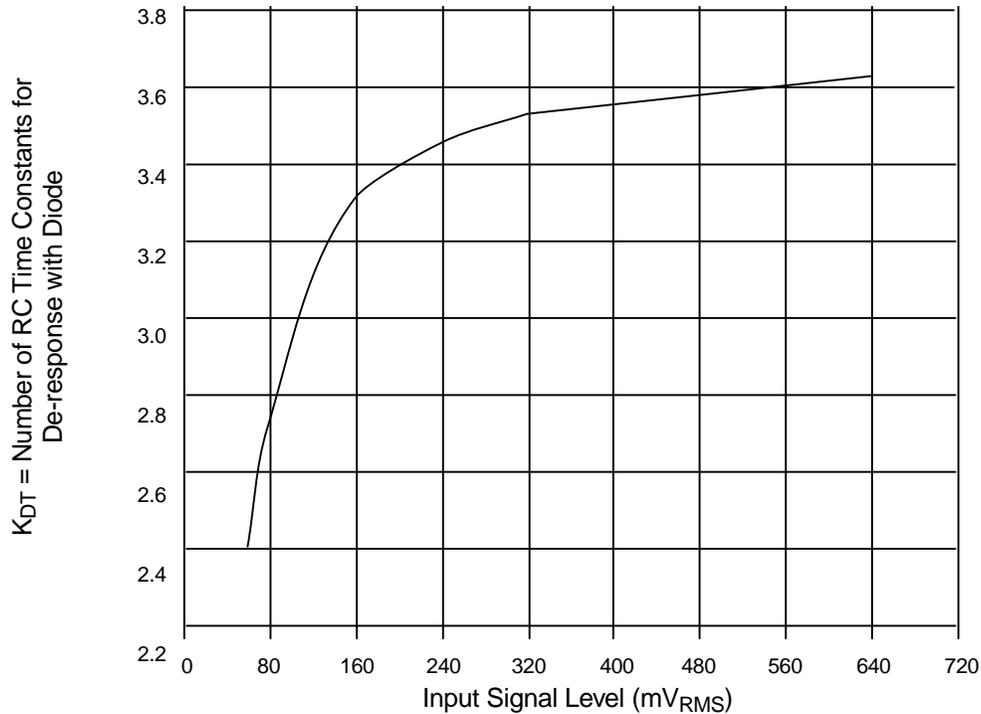


Figure 4: KDT Factor for TOFF vs. Signal Input Amplitude

5.9 Calculate Signal to Noise Performance

Worst-case S/N calculations depend on calculation of a value “M” using the formula shown below:

$$M = \frac{R3 \times C3_A}{3 \times R2 \times C2_A}$$

substituting example values,

$$M = \frac{510 \times 0.1}{3 \times 200 \times 0.01} = 8.5$$

By substituting this value for M in Figure 5, the minimum required S/N of an in band tone with respect to an adjacent interfering tone can be found. This then has to be increased depending on the input tone amplitude.

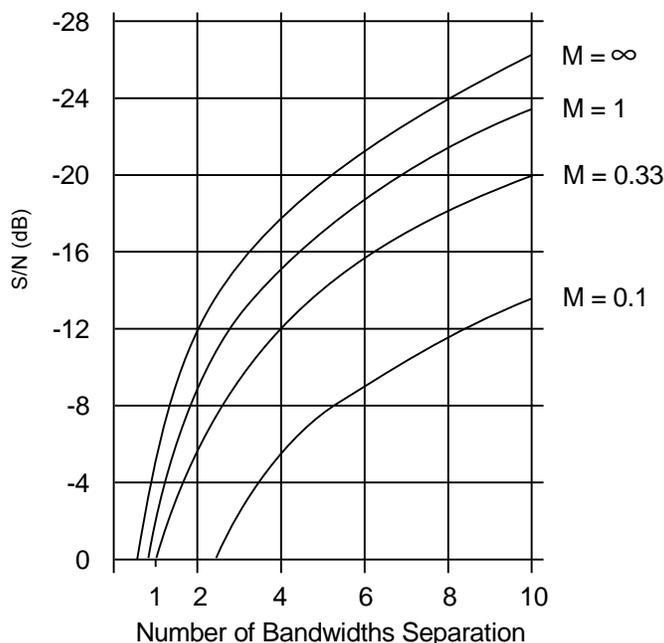


Figure 5: S/N vs. BW Separation

The following formula expresses the reduction in noise immunity as the input signal approaches the detect filter sensitivity V_{TH} .

$$\text{required } \frac{S}{N} = 20 \log \left(\frac{V_{IN}}{V_{IN} - V_{TH}} \right) + \frac{S}{N_{\text{Figure 5}}}$$

If this S/N is better than required for the application, $R3 \times C3_A$ can be reduced, or the operating bandwidth can be increased to obtain a faster tone detection time.

If the S/N performance is not adequate, the operating bandwidth can be reduced toward the MUBW, or $R3 \times C3_A$ can be increased to improve S/N performance at the expense of slower response time.

5.10 Calculate C4 for 30° Phase Shift

Capacitor C4 is used to phase shift the input to the VCO commutating filter by 30°, thereby shifting the sampling clocks by the same amount. This enables the Detect sampling filter to sample and integrate at the maximum and minimum of the input tone.

$$C4 = \frac{\tan(30^\circ)}{2\pi \times f_0 \times R_V} \approx \frac{0.092}{f_0 \times R_V} \approx 164 \text{pF}$$

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply ($V_{DD} - V_{SS}$)	-0.3	7.0	V
Voltage on any pin (wrt V_{SS})	-0.3	$V_{DD} + 0.3$	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pins	-20	20	mA
Max. Output Switch Load Current		10	mA
P/LH/DW Package			
Storage Temperature	-40	85	°C
Operating Temperature	-30	85	°C
Device Dissipation at $T_{AMB} = 25^{\circ}\text{C}$		800	mW
Derating above 25°C		13	mW/°C above 25°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply ($V_{DD} - V_{SS}$)		2.7	5.5	V
Operating Temperature		-30	85	°C

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

$$V_{DD} = 5.0 \text{ V @ } T_{AMB} = 25^{\circ}\text{C}$$

Load resistance on decoder output = 20k Ω .

	Notes	Min.	Typ.	Max.	Units
Static Parameters					
I _{DD}			1.0		mA
Amplifier Input Impedance		160	200		k Ω
Digital Output Impedance			500	1000	Ω
Analog Output Impedance			1000	1200	Ω
Dynamic Parameters					
Input Signal					
Frequency		40		20,000	Hz
Lowest Must Detect Level	1		30		mV _{RMS}
Highest Will Not Detect Level	1		20		mV _{RMS}
Highest Will Not Detect f ₀ /2	1, 2		30		dB
			790		mV _{RMS}
Highest Will Not Detect 5(f ₀)	1, 2		20		dB
			250		mV _{RMS}
VCO					
Frequency	3	120		120,000	Hz
Frequency Stability			100		ppm/ $^{\circ}$ C
			5000		ppm/V
BW Limiter					
BW Range		2		10	%f ₀
Amplifier					
Open Loop Gain			60		dB
GBWP			1.0		MHz
Closed Loop Gain			0		dB
Detect Commutating Filter					
Sensitivity (V _{TH})	1		25		mV _{RMS}

Operating Characteristics Notes:

1. Multiply by V_{DD} /5V for other supply values.
2. The reference level is V_{TH}. The following formula converts dB to mV_{RMS}.

$$\text{mV}_{\text{RMS}} = 10^{(\text{dB}/20)} \times V_{\text{TH}}$$

3. Observing pins 13, 14, or 15 (DW/J package) will cause a frequency shift due to additional loading. If tuning center frequency by observing oscillator, design in a buffer amplifier between pin 15 and probe/calibration point and tune with no input signal. Otherwise, tune by observing detect output band edges while sweeping input signal. VCO center frequency is 6(f₀) at pin 15 while it is 3(f₀) at pins 13 and 14.

6.2 Packaging

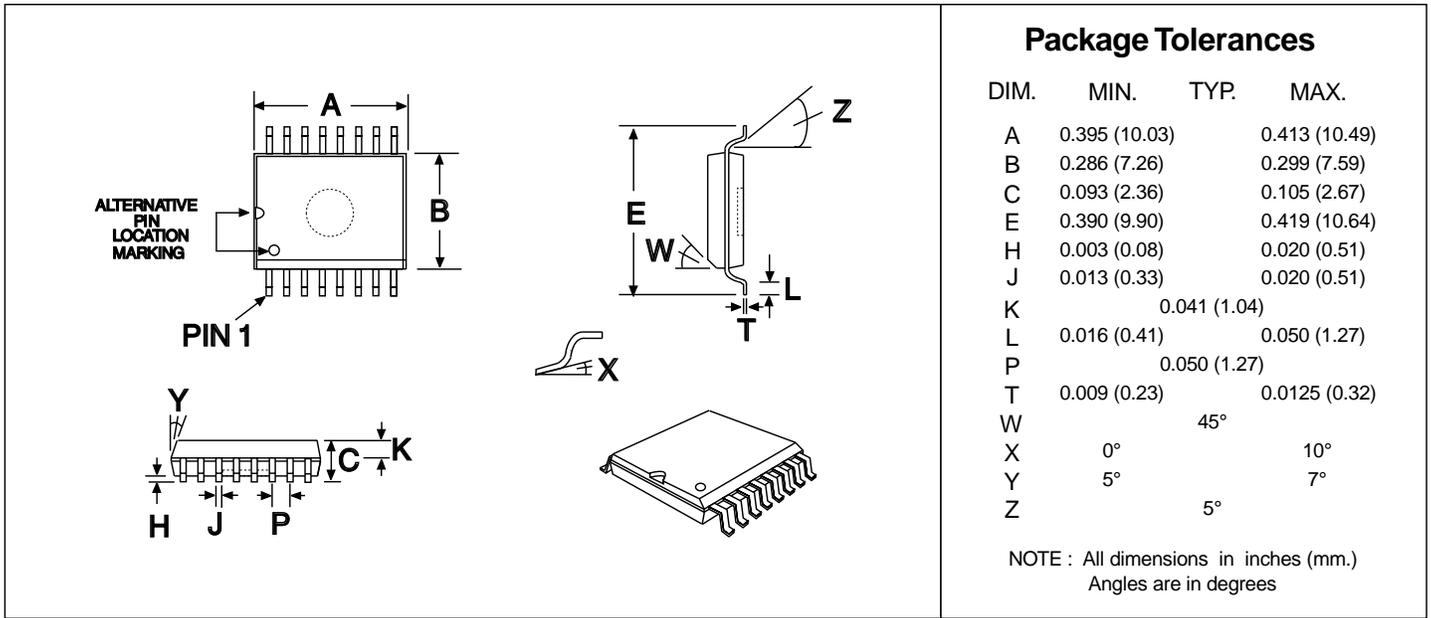


Figure 6: 16-pin SOIC Mechanical Outline: *Order as part no. MX105ADW*

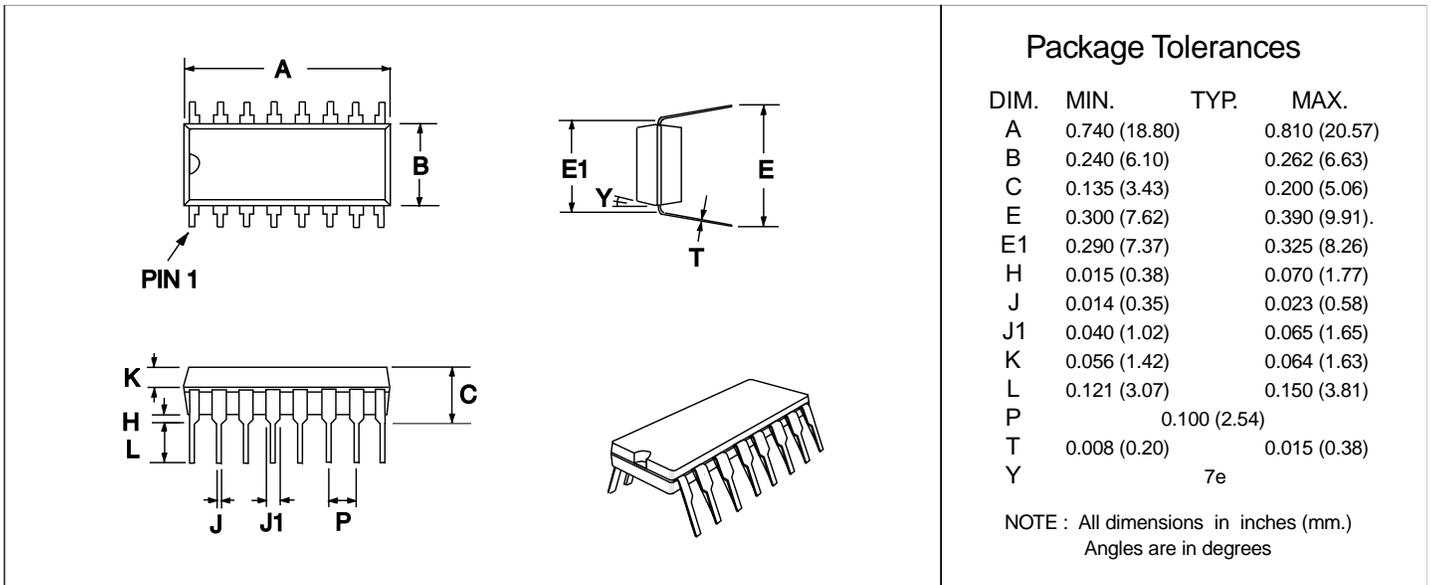


Figure 7: 16-pin PDIP Mechanical Outline: *Order as part no. MX105AP*

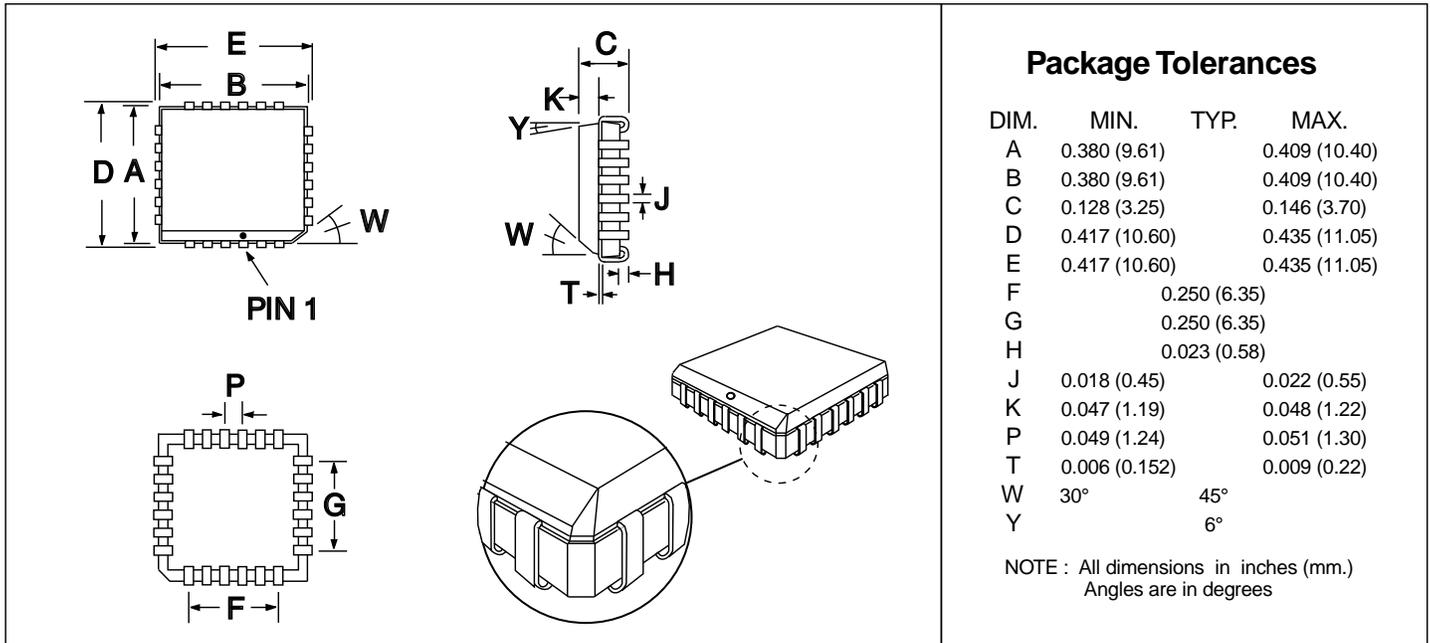


Figure 8: 24-pin PLCC Mechanical Outline: Order as part no. MX105ALH

LM386 Low Voltage Audio Power Amplifier

General Description

The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.

- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion
- Eight pin dual-in-line package

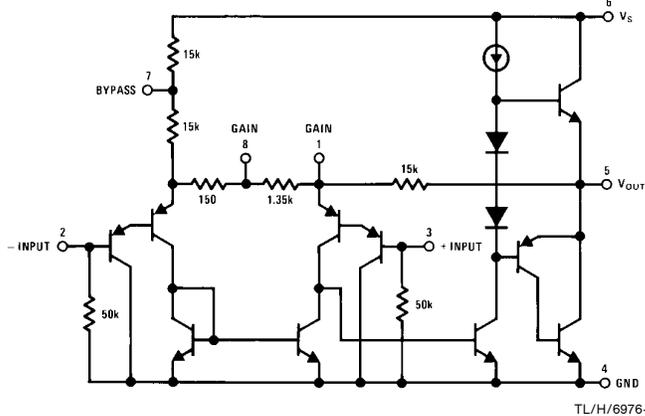
Features

- Battery operation
- Minimum external parts
- Wide supply voltage range 4V–12V or 5V–18V
- Low quiescent current drain 4 mA

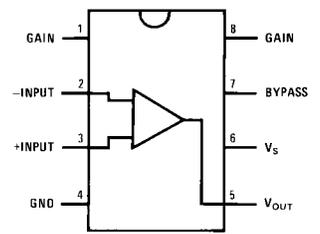
Applications

- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



Dual-In-Line and Small Outline Packages

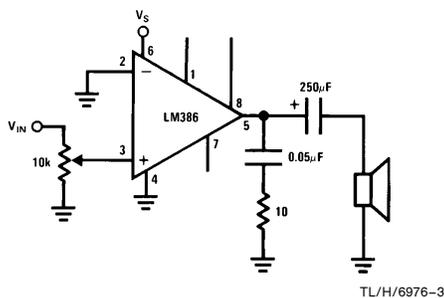


Top View

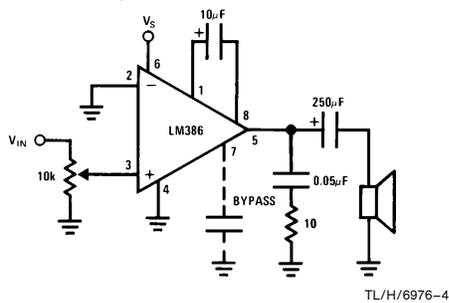
Order Number LM386M-1,
LM386N-1, LM386N-3 or LM386N-4
See NS Package Number
M08A or N08E

Typical Applications

Amplifier with Gain = 20 Minimum Parts



Amplifier with Gain = 200



Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (LM386N-1, -3, LM386M-1)	15V
Supply Voltage (LM386N-4)	22V
Package Dissipation (Note 1) (LM386N)	1.25W
(LM386M)	0.73W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	+150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 sec)	+260°C
Small Outline Package	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Thermal Resistance

θ_{JC} (DIP)	37°C/W
θ_{JA} (DIP)	107°C/W
θ_{JC} (SO Package)	35°C/W
θ_{JA} (SO Package)	172°C/W

Electrical Characteristics $T_A = 25^\circ\text{C}$

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage (V_S) LM386N-1, -3, LM386M-1 LM386N-4		4 5		12 18	V V
Quiescent Current (I_Q)	$V_S = 6V, V_{IN} = 0$		4	8	mA
Output Power (P_{OUT}) LM386N-1, LM386M-1 LM386N-3 LM386N-4	$V_S = 6V, R_L = 8\Omega, THD = 10\%$ $V_S = 9V, R_L = 8\Omega, THD = 10\%$ $V_S = 16V, R_L = 32\Omega, THD = 10\%$	250 500 700	325 700 1000		mW mW mW
Voltage Gain (A_V)	$V_S = 6V, f = 1\text{ kHz}$ 10 μF from Pin 1 to 8		26 46		dB dB
Bandwidth (BW)	$V_S = 6V$, Pins 1 and 8 Open		300		kHz
Total Harmonic Distortion (THD)	$V_S = 6V, R_L = 8\Omega, P_{OUT} = 125\text{ mW}$ $f = 1\text{ kHz}$, Pins 1 and 8 Open		0.2		%
Power Supply Rejection Ratio (PSRR)	$V_S = 6V, f = 1\text{ kHz}, C_{BYPASS} = 10\ \mu\text{F}$ Pins 1 and 8 Open, Referred to Output		50		dB
Input Resistance (R_{IN}) Input Bias Current (I_{BIAS})	$V_S = 6V$, Pins 2 and 3 Open		50 250		k Ω nA

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and 1) a thermal resistance of 80°C/W junction to ambient for the dual-in-line package and 2) a thermal resistance of 170°C/W for the small outline package.

Application Hints

GAIN CONTROL

To make the LM386 a more versatile amplifier, two pins (1 and 8) are provided for gain control. With pins 1 and 8 open the 1.35 k Ω resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35 k Ω resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 1 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 5 (paralleling the internal 15 k Ω resistor). For 6 dB effective bass boost: $R \approx 15\text{ k}\Omega$, the lowest value for good stable operation is $R = 10\text{ k}\Omega$ if pin 8 is open. If pins 1 and 8 are bypassed then R as low as 2 k Ω can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9.

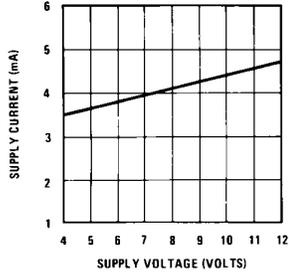
INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 k Ω resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM386 is higher than 250 k Ω it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 k Ω , then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

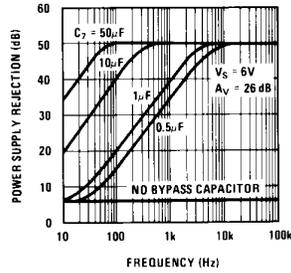
When using the LM386 with higher gains (bypassing the 1.35 k Ω resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 μF capacitor or a short to ground depending on the dc source resistance on the driven input.

Typical Performance Characteristics

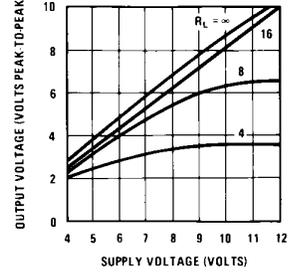
Quiescent Supply Current vs Supply Voltage



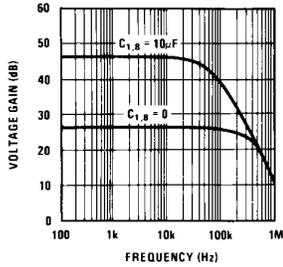
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



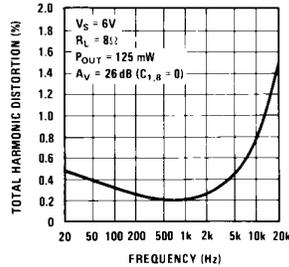
Peak-to-Peak Output Voltage Swing vs Supply Voltage



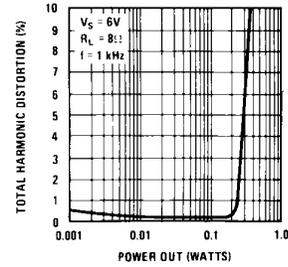
Voltage Gain vs Frequency



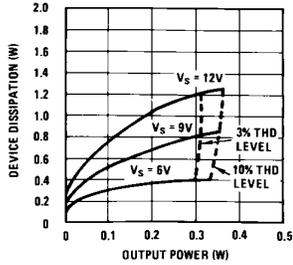
Distortion vs Frequency



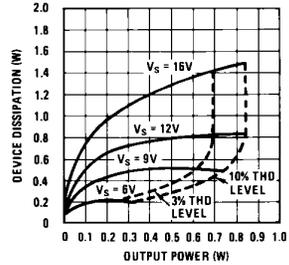
Distortion vs Output Power



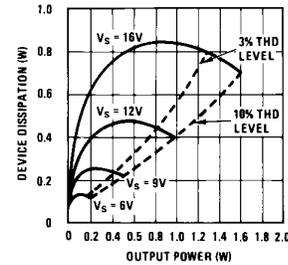
Device Dissipation vs Output Power—4Ω Load



Device Dissipation vs Output Power—8Ω Load



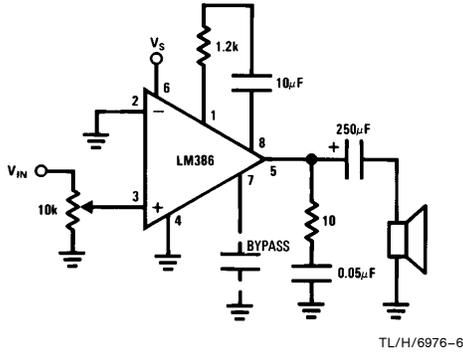
Device Dissipation vs Output Power—16Ω Load



TL/H/6976-5

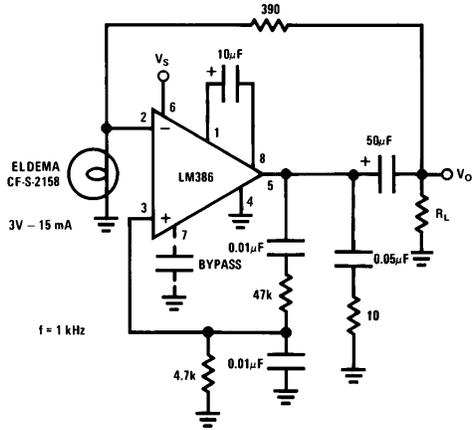
Typical Applications (Continued)

Amplifier with Gain = 50



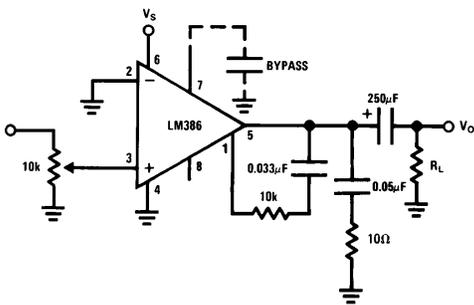
TL/H/6976-6

Low Distortion Power Wienbridge Oscillator



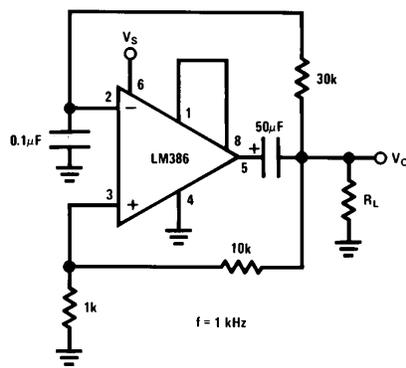
TL/H/6976-7

Amplifier with Bass Boost



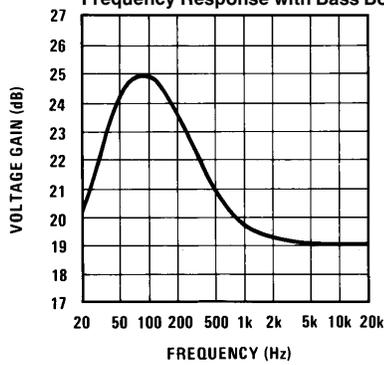
TL/H/6976-8

Square Wave Oscillator



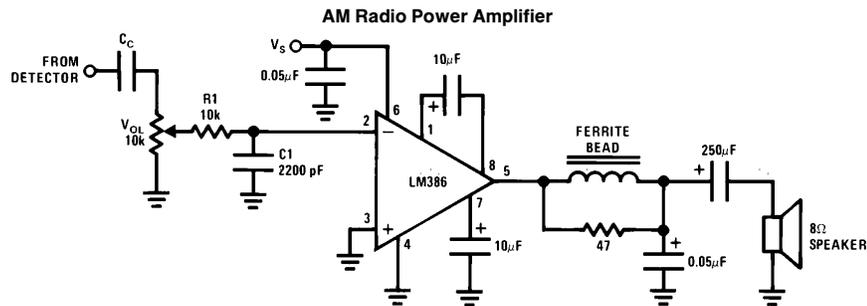
TL/H/6976-9

Frequency Response with Bass Boost



TL/H/6976-10

Typical Applications (Continued)



Note 1: Twist supply lead and supply ground very tightly.

Note 2: Twist speaker lead and ground very tightly.

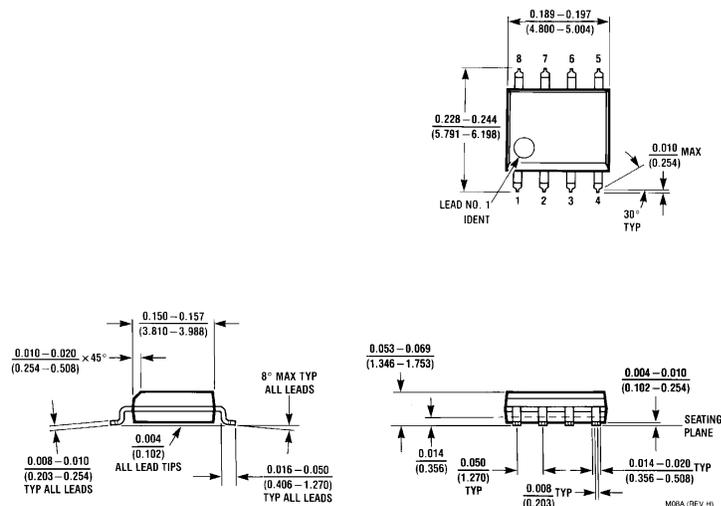
Note 3: Ferrite bead is Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 4: R1C1 band limits input signals.

Note 5: All components must be spaced very close to IC.

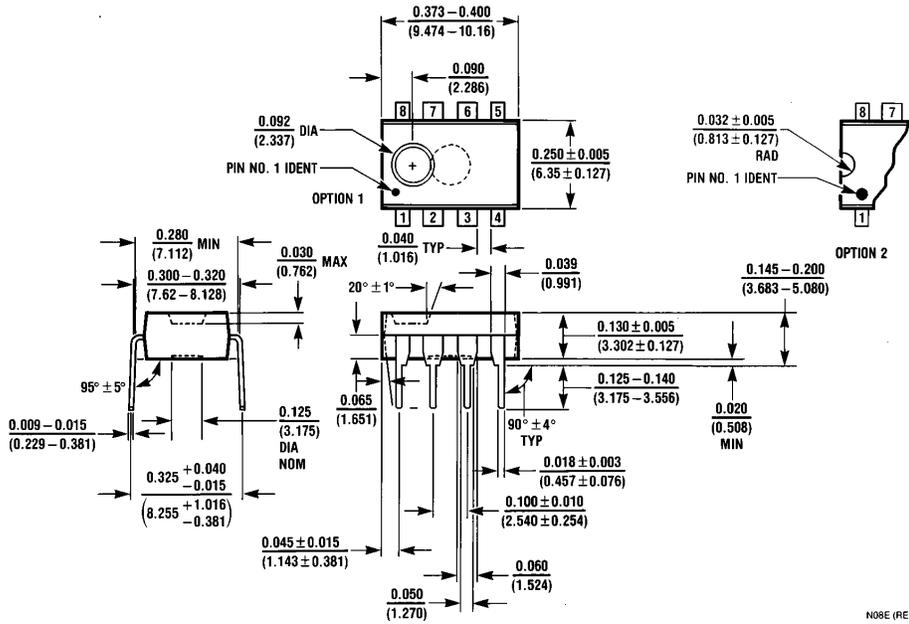
TL/H/6976-11

Physical Dimensions inches (millimeters)



SO Package (M)
Order Number LM386M-1
NS Package Number M08A

Physical Dimensions inches (millimeters) (Continued)



Dual-In-Line Package (N)
Order Number LM386N-1, LM386N-3 or LM386N-4
NS Package Number N08E

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5474/DM5474/DM7474 Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

General Description

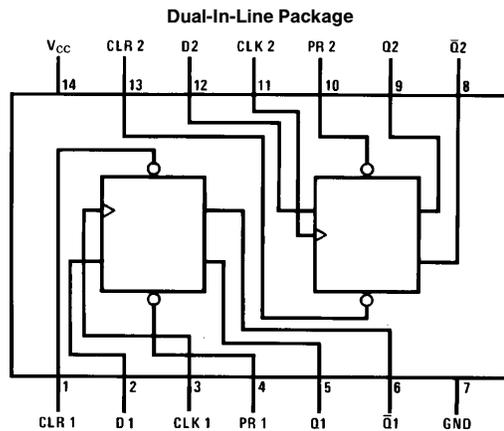
This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not

violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

- Alternate Military/Aerospace device (5474) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram



TL/F/6526-1

Order Number 5474DMQB, 5474FMQB, DM5474J, DM5474W, DM7474M or DM7474N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	\bar{Q} ₀

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↑ = Positive-going transition of the clock.

* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (high) level.

Q₀ = The output logic level of Q before the indicated input conditions were established.

5474/DM5474/DM7474 Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	-55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM5474			DM7474			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.8			0.8	V
I _{OH}	High Level Output Current			-0.4			-0.4	mA
I _{OL}	Low Level Output Current			16			16	mA
f _{CLK}	Clock Frequency (Note 2)	0		15	0		15	MHz
t _w	Pulse Width (Note 2)	Clock High	30		30			ns
		Clock Low	37		37			
		Clear Low	30		30			
		Preset Low	30		30			
t _{SU}	Input Setup Time (Notes 1 & 2)	20 ↑			20 ↑			ns
t _H	Input Hold Time (Notes 1 & 2)	5 ↑			5 ↑			ns
T _A	Free Air Operating Temperature	-55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 3)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -12 mA			-1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max, V _{IH} = Min	2.4	3.4		V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IH} = Min, V _{IL} = Max		0.2	0.4	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 5.5V			1	mA
I _{IH}	High Level Input Current	V _{CC} = Max V _I = 2.4V	D		40	μA
			Clock		80	
			Clear		120	
			Preset		40	
I _{IL}	Low Level Input Current	V _{CC} = Max V _I = 0.4V (Note 6)	D		-1.6	mA
			Clock		-3.2	
			Clear		-3.2	
			Preset		-1.6	
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 4)	DM54	-20	-55	mA
			DM74	-18	-55	
I _{CC}	Supply Current	V _{CC} = Max (Note 5)		17	30	mA

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time.

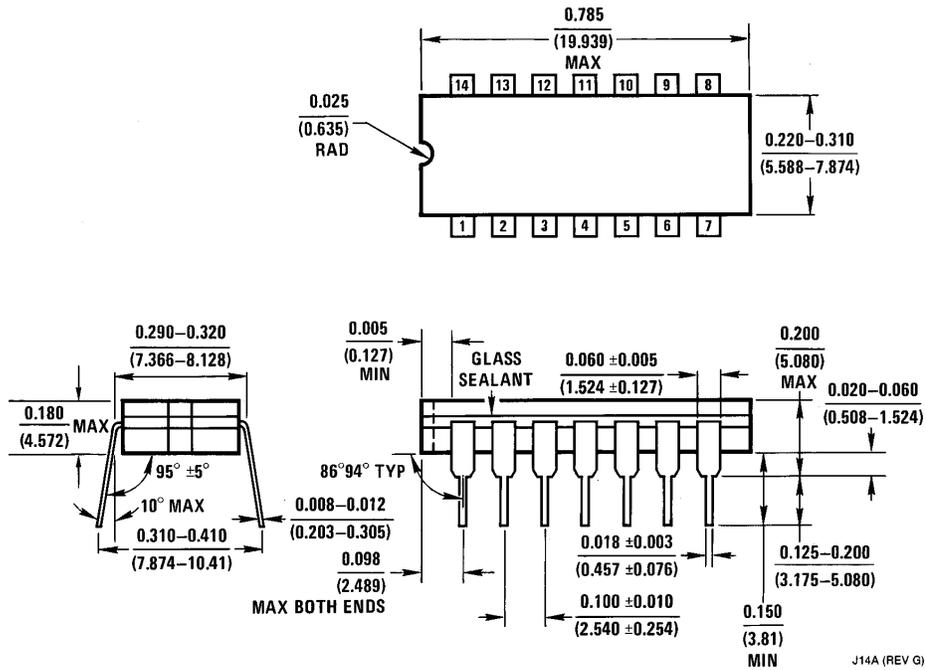
Note 5: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement the clock is grounded.

Note 6: Clear is tested with preset high and preset is tested with clear high.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$ $C_L = 15\text{ pF}$		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to \bar{Q}		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to \bar{Q}		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or \bar{Q}		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or \bar{Q}		25	ns

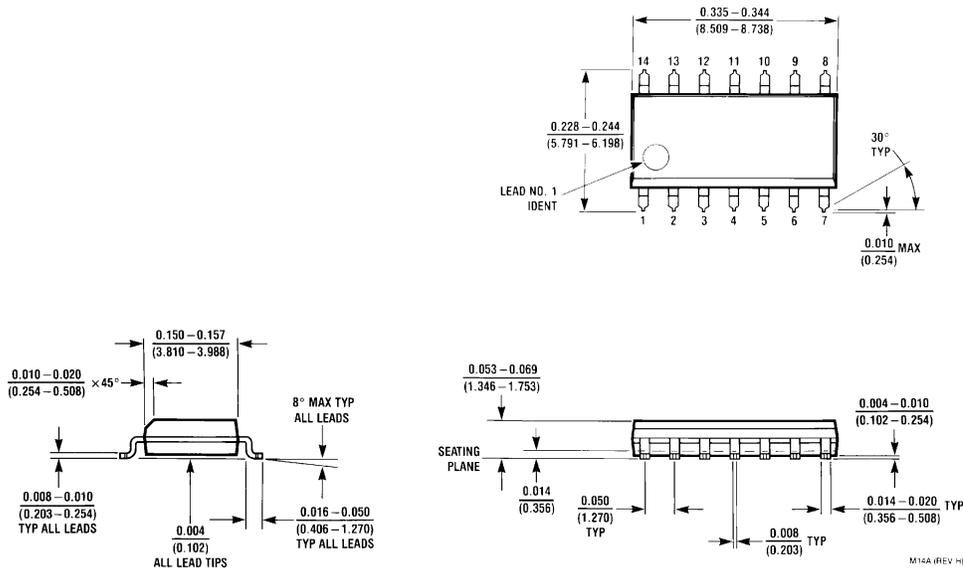
Physical Dimensions inches (millimeters)



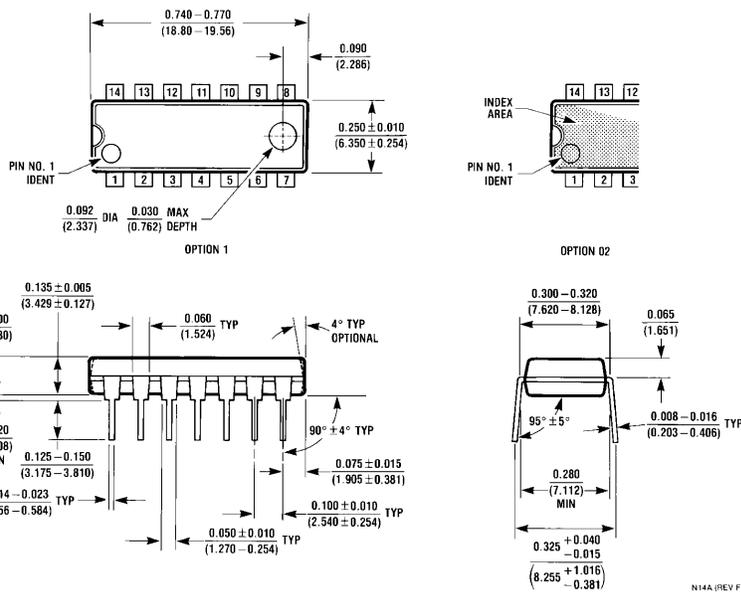
14-Lead Ceramic Dual-In-Line Package (J)
 Order Number 5474DMQB or DM5474J
 NS Package Number J14A

J14A (REV G)

Physical Dimensions inches (millimeters) (Continued)



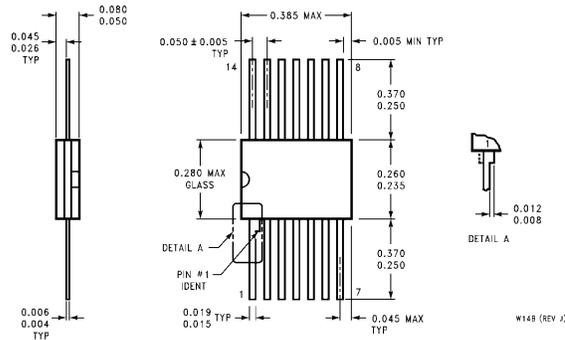
14-Lead Small Outline Molded Package (M)
Order Number DM7474M
NS Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM7474N
NS Package Number N14A

5474/DM5474/DM7474 Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 5474FMQB or DM5474W
NS Package Number W14B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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