

# High Efficiency Synchronous Step-Down Switching Regulator

## FEATURES

- Synchronizable/Programmable Fixed Frequency
- OPTI-LOOP™ Compensation Minimizes C<sub>OUT</sub>
- ±1% Output Voltage Accuracy
- Dual N-Channel MOSFET Synchronous Drive
- Wide V<sub>IN</sub> Range: 3.5V to 36V Operation
- V<sub>OUT</sub> Range: 0.8V to 6V
- Internal Current Foldback
- Output Overvoltage Crowbar Protection
- Latched Short-Circuit Shutdown Timer with Defeat Option
- Very Low Dropout Operation: 99% Duty Cycle
- Forced Continuous Control Pin
- Optional Programmable Soft-Start
- Remote Output Voltage Sense
- Power Good Output (LTC1735F Only)
- Logic Controlled Micropower Shutdown: I<sub>Q</sub> < 25μA
- LTC1435 Pin Compatible with Minor Component Changes
- Available in 16-Lead Narrow SSOP, SO Packages and 20-Lead TSSOP Package (LTC1735F Only)

## APPLICATIONS

- Notebook and Palmtop Computers, PDAs
- Cellular Telephones and Wireless Modems
- DC Power Distribution Systems

## DESCRIPTION

The LTC<sup>®</sup>1735 is a synchronous step-down switching regulator controller that drives external N-channel power MOSFETs using a fixed frequency architecture. Burst Mode™ operation provides high efficiency at low load currents. The precision 0.8V reference is compatible with future microprocessor generations. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values.

The operating frequency (synchronizable up to 500kHz) is set by an external capacitor allowing maximum flexibility in optimizing efficiency. A forced continuous control pin reduces noise and RF interference and can assist secondary winding regulation by disabling Burst Mode operation when the main output is lightly loaded.

Protection features include internal foldback current limiting, output overvoltage crowbar and optional short-circuit shutdown. Soft-start is provided by an external capacitor that can be used to properly sequence supplies. The operating current level is user-programmable via an external current sense resistor. Wide input supply range allows operation from 3.5V to 30V (36V maximum).

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## TYPICAL APPLICATION

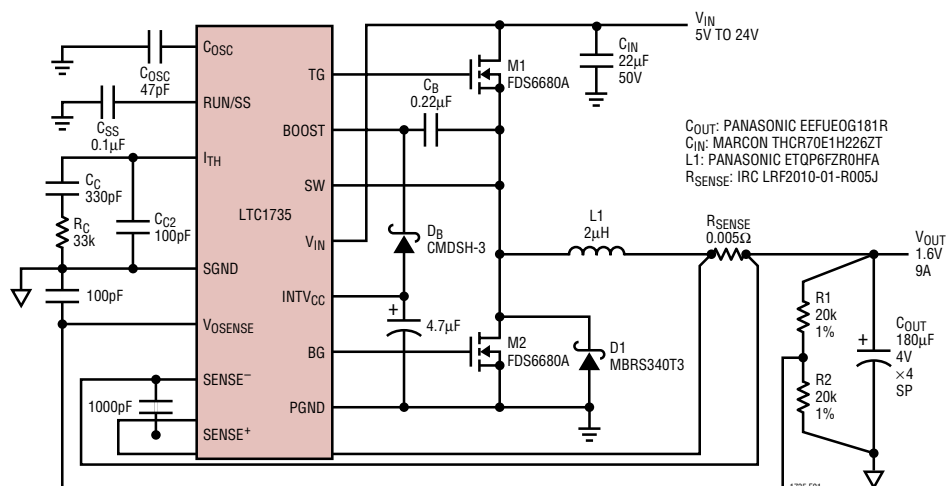


Figure 1. High Efficiency Step-Down Converter

# LTC1735

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage ( $V_{IN}$ )	36V to -0.3V	Peak Driver Output Current <math><10\mu\text{s}</math> (TG, BG)	3A
Topside Driver Supply Voltage (BOOST)	42V to -0.3V	INTV <sub>CC</sub> Output Current	50mA
Switch Voltage (SW)	36V to -5V	Operating Ambient Temperature Range	
EXTV <sub>CC</sub> Voltage	7V to -0.3V	LTC1735C	0°C to 85°C
Boosted Driver Voltage (BOOST - SW)	7V to -0.3V	LTC1735I	-40°C to 85°C
SENSE <sup>+</sup> , SENSE <sup>-</sup> Voltages	1.1 (INTV <sub>CC</sub> ) to -0.3V	Junction Temperature (Note 2)	125°C
FCB Voltage	(INTV <sub>CC</sub> + 0.3V) to -0.3V	Storage Temperature Range	-65°C to 150°C
$I_{TH}$ , $V_{OSENSE}$ Voltages	2.7V to -0.3V	Lead Temperature (Soldering, 10 sec)	300°C
RUN/SS, PGOOD (LTC1735F Only)			
Voltages	7V to -0.3V		

## PACKAGE/ORDER INFORMATION

<p>GN PACKAGE 16-LEAD NARROW PLASTIC SSOP</p> <p><math>T_{JMAX} = 125^{\circ}\text{C}</math>, <math>\theta_{JA} = 130^{\circ}\text{C/W}</math> (GN) <math>T_{JMAX} = 125^{\circ}\text{C}</math>, <math>\theta_{JA} = 110^{\circ}\text{C/W}</math> (S)</p>	<p>ORDER PART NUMBER</p> <p>LTC1735CGN LTC1735CS LTC1735IGN LTC1735IS</p> <p>GN PART MARKING</p> <p>1735 1735I</p>	<p>F PACKAGE 20-LEAD PLASTIC TSSOP</p> <p><math>T_{JMAX} = 125^{\circ}\text{C}</math>, <math>\theta_{JA} = 110^{\circ}\text{C/W}</math></p>	<p>ORDER PART NUMBER</p> <p>LTC1735CF LTC1735IF</p>
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Consult LTC marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}\text{C}$ .  $V_{IN} = 15\text{V}$ ,  $V_{RUN/SS} = 5\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Main Control Loop</b>						
$I_{VOSENSE}$	Feedback Current	(Note 3)		-4	-25	nA
$V_{OSENSE}$	Feedback Voltage	(Note 3)	● 0.792	0.8	0.808	V
$\Delta V_{LINEREG}$	Reference Voltage Line Regulation	$V_{IN} = 3.6\text{V}$ to 30V (Note 3)		0.001	0.02	%/V
$\Delta V_{LOADREG}$	Output Voltage Load Regulation	(Note 3)				
		Measured in Servo Loop; $V_{ITH} = 0.7\text{V}$	●	0.1	0.3	%
		Measured in Servo Loop; $V_{ITH} = 2\text{V}$	●	-0.1	-0.3	%
DF Max	Maximum Duty Factor	In Dropout		98	99.4	%
$g_m$	Transconductance Amplifier $g_m$			1.3		mmho
$V_{FCB}$	Forced Continuous Threshold		● 0.76	0.8	0.84	V
$I_{FCB}$	Forced Continuous Current	$V_{FCB} = 0.85\text{V}$		-0.17	-0.3	$\mu\text{A}$

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## ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 15\text{V}$ ,  $V_{RUN/SS} = 5\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{OVL}$	Feedback Overvoltage Lockout		● 0.84	0.86	0.88	V
$I_Q$	Input DC Supply Current	(Note 4)		450		$\mu\text{A}$
	Normal Mode			15	25	$\mu\text{A}$
	Shutdown	$V_{RUN/SS} = 0\text{V}$				
$V_{RUN/SS}$	Run Pin Start Threshold	$V_{RUN/SS}$ , Ramping Positive	1.0	1.5	1.9	V
$V_{RUN/SS}$	Run Pin Begin Latchoff Threshold	$V_{RUN/SS}$ , Ramping Positive		4.1	4.5	V
$I_{RUN/SS}$	Soft-Start Charge Current	$V_{RUN/SS} = 0\text{V}$	-0.7	-1.2		$\mu\text{A}$
$I_{SCL}$	RUN/SS Discharge Current	Soft Short Condition, $V_{OSENSE} = 0.5\text{V}$ , $V_{RUN/SS} = 4.5\text{V}$	0.5	2	4	$\mu\text{A}$
UVLO	Undervoltage Lockout	Measured at $V_{IN}$ Pin ( $V_{IN}$ Ramping Down)	●	3.5	3.9	V
$\Delta V_{SENSE(MAX)}$	Maximum Current Sense Threshold	$V_{OSENSE} = 0.7\text{V}$	● 60	75	85	mV
$I_{SENSE}$	Sense Pins Total Source Current	$V_{SENSE}^- = V_{SENSE}^+ = 0\text{V}$		60	80	$\mu\text{A}$
$t_{ON(MIN)}$	Minimum On-Time	Tested with a Square Wave (Note 6)		160	200	ns
TG $t_r$	TG Transition Time: Rise Time	(Note 7) $C_{LOAD} = 3300\text{pF}$		50	90	ns
TG $t_f$	TG Transition Time: Fall Time	$C_{LOAD} = 3300\text{pF}$		50	90	ns
BG $t_r$	BG Transition Time: Rise Time	(Note 7) $C_{LOAD} = 3300\text{pF}$		50	90	ns
BG $t_f$	BG Transition Time: Fall Time	$C_{LOAD} = 3300\text{pF}$		40	80	ns
TG/BG $t_{1D}$	Top Gate Off to Synchronous Gate On Delay Time	$C_{LOAD} = 3300\text{pF}$ Each Driver		100		ns
TG/BG $t_{2D}$	Synchronous Gate Off to Top Gate On Delay Time	$C_{LOAD} = 3300\text{pF}$ Each Driver		70		ns

### Internal $V_{CC}$ Regulator

$V_{INTVCC}$	Internal $V_{CC}$ Voltage	$6\text{V} < V_{IN} < 30\text{V}$ , $V_{EXTVCC} = 4\text{V}$		5.0	5.2	5.4	V
$V_{LDO(INT)}$	Internal $V_{CC}$ Load Regulation	$I_{CC} = 0$ to $20\text{mA}$ , $V_{EXTVCC} = 4\text{V}$		0.2	1		%
$V_{LDO(EXT)}$	EXTV <sub>CC</sub> Drop Voltage	$I_{CC} = 20\text{mA}$ , $V_{EXTVCC} = 5\text{V}$		130	200		mV
$V_{EXTVCC}$	EXTV <sub>CC</sub> Switchover Voltage	$I_{CC} = 20\text{mA}$ , EXTV <sub>CC</sub> Ramping Positive	● 4.5	4.7			V
$V_{EXTVCC(HYS)}$	EXTV <sub>CC</sub> Hysteresis			0.2			V

### Oscillator

$f_{OSC}$	Oscillator Frequency	$C_{OSC} = 43\text{pF}$ (Note 5)		265	300	335	kHz
$f_H/f_{OSC}$	Maximum Sync Frequency Ratio			1.3			
$f_{FCB(SYNC)}$	FCB Pin Threshold For Sync	Ramping Negative		0.9	1.2		V

### PGOOD Output (LTC1735F Only)

$V_{PGL}$	PGOOD Voltage Low	$I_{PGOOD} = 2\text{mA}$		110	200		mV
$I_{PGOOD}$	PGOOD Leakage Current	$V_{PGOOD} = 5\text{V}$			$\pm 1$		$\mu\text{A}$
$V_{PG}$	PGOOD Trip Level	$V_{OSENSE}$ with Respect to Set Output Voltage		-6.0	-7.5	-9.5	%
		$V_{OSENSE}$ Ramping Negative		6.0	7.5	9.5	%
		$V_{OSENSE}$ Ramping Positive					

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:**  $T_J$  is calculated from the ambient temperature  $T_A$  and power dissipation  $P_D$  according to the following formulas:

$$\text{LTC1735CS, LTC1735IS: } T_J = T_A + (P_D \cdot 110^\circ\text{C/W})$$

$$\text{LTC1735CGN, LTC1735IGN: } T_J = T_A + (P_D \cdot 130^\circ\text{C/W})$$

$$\text{LTC1735CF, LTC1735IF: } T_J = T_A + (P_D \cdot 110^\circ\text{C/W})$$

## ELECTRICAL CHARACTERISTICS

**Note 3:** The LTC1735 is tested in a feedback loop that servos  $V_{OSENSE}$  to the balance point for the error amplifier ( $V_{ITH} = 1.2V$ ).

**Note 4:** Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

**Note 5:** Oscillator frequency is tested by measuring the  $C_{OSC}$  charge current ( $I_{OSC}$ ) and applying the formula:

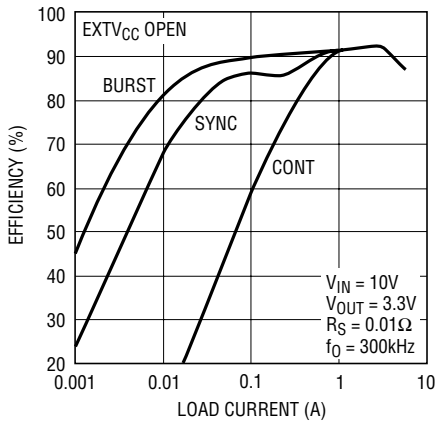
$$f_{OSC} = \left( \frac{8.477(10^{11})}{C_{OSC}(\text{pF}) + 11} \right) \left( \frac{1}{I_{CHG}} + \frac{1}{I_{DIS}} \right)^{-1}$$

**Note 6:** The minimum on-time condition corresponds to an inductor peak-to-peak ripple current  $\geq 40\%$  of  $I_{MAX}$  (see Minimum On-Time Considerations in the Applications Information section).

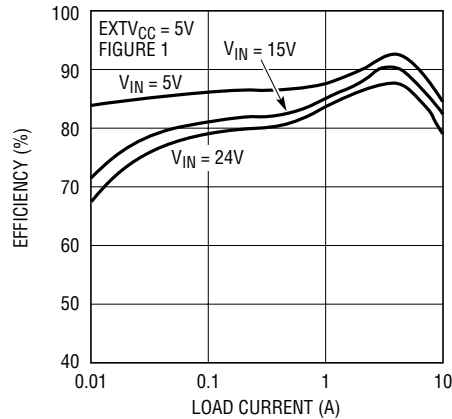
**Note 7:** Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

## TYPICAL PERFORMANCE CHARACTERISTICS

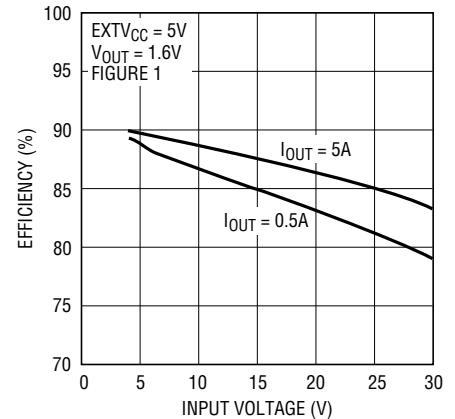
**Efficiency vs Load Current (3 Operating Modes)**



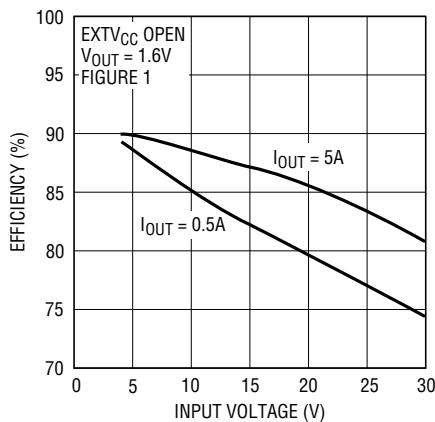
**Efficiency vs Load Current**



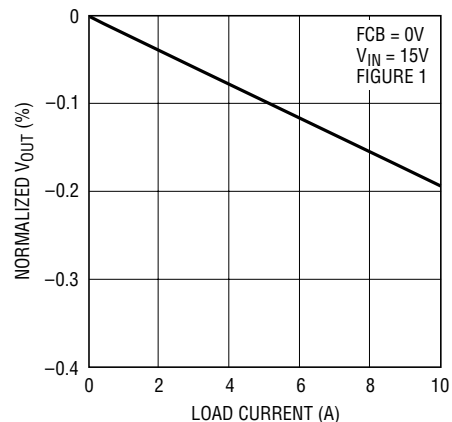
**Efficiency vs Input Voltage**



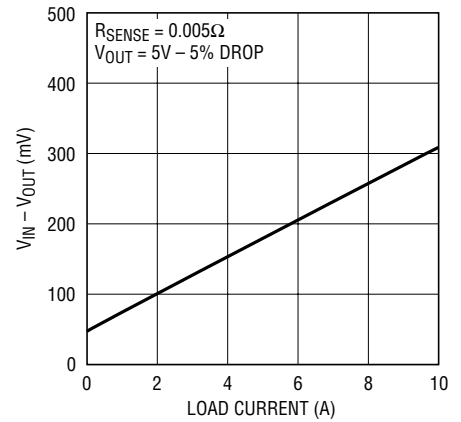
**Efficiency vs Input Voltage**



**Load Regulation**

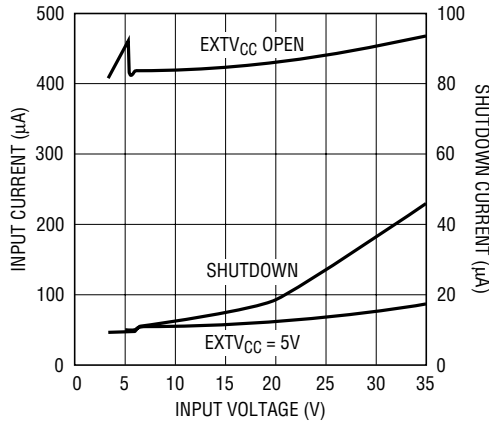


**$V_{IN} - V_{OUT}$  Dropout Voltage vs Load Current**



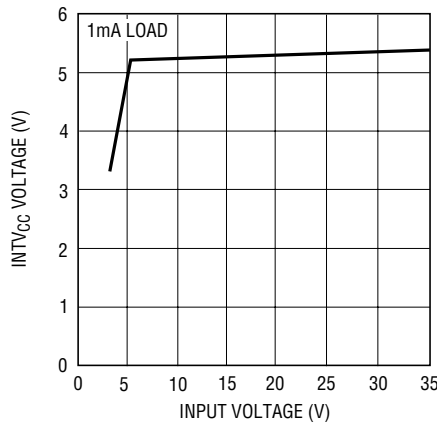
# TYPICAL PERFORMANCE CHARACTERISTICS

**Input and Shutdown Currents vs Input Voltage**



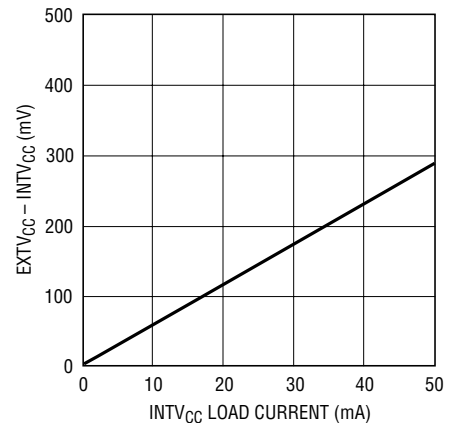
1735 G07

**INTV<sub>CC</sub> Line Regulation**



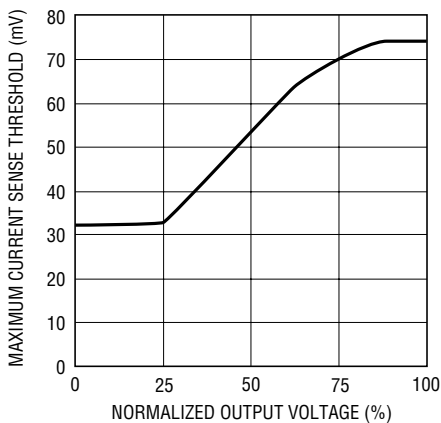
1735 G08

**EXTV<sub>CC</sub> Switch Drop vs INTV<sub>CC</sub> Load Current**



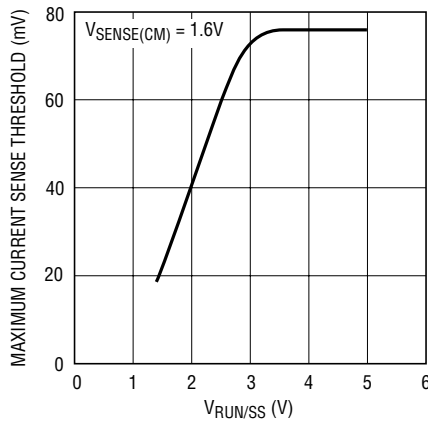
1735 G09

**Maximum Current Sense Threshold vs Normalized Output Voltage (Foldback)**



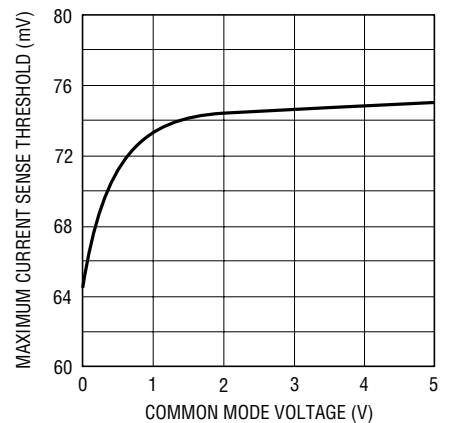
1735 G10

**Maximum Current Sense Threshold vs V<sub>RUN/SS</sub>**



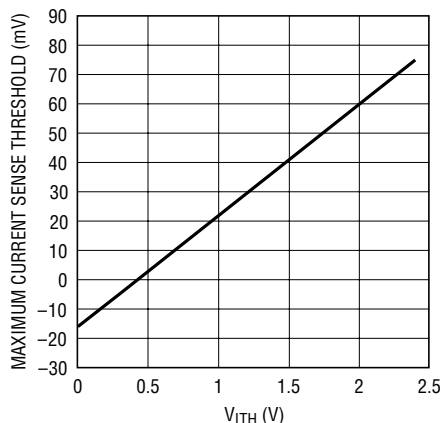
1735 G11

**Maximum Current Sense Threshold vs Sense Common Mode Voltage**



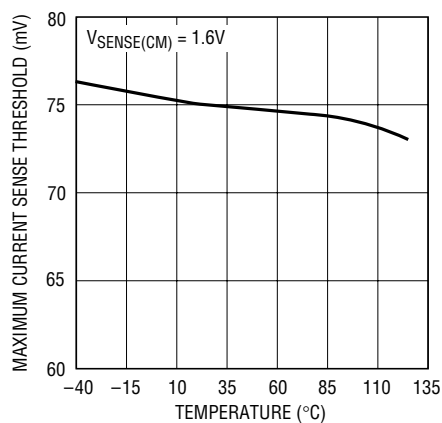
1735 G12

**Maximum Current Sense Threshold vs I<sub>TH</sub> Voltage**



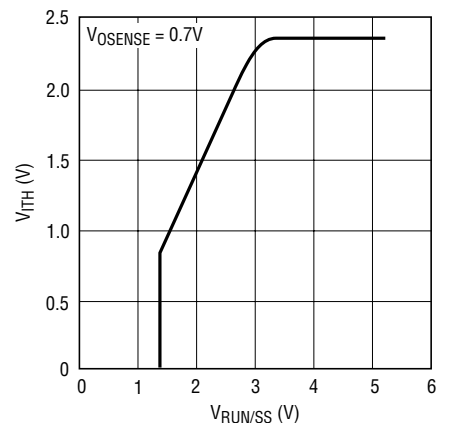
1735 G13

**Maximum Current Sense Threshold vs Temperature**



1735 G18

**V<sub>I TH</sub> vs V<sub>RUN/SS</sub>**

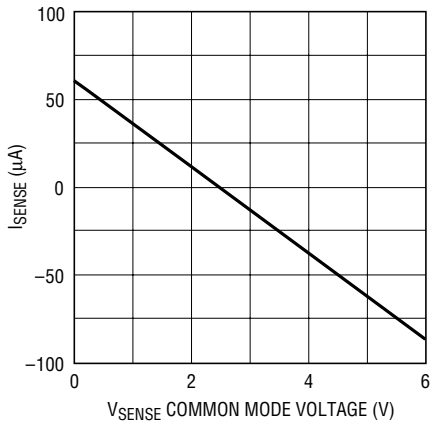


1735 G15

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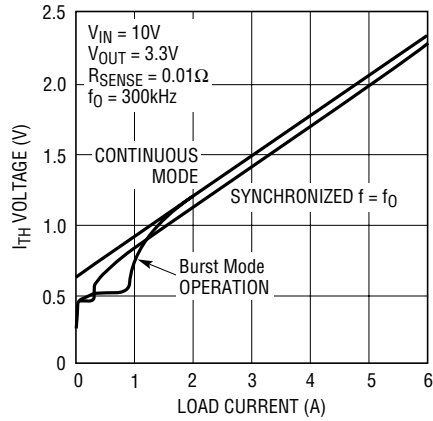
# TYPICAL PERFORMANCE CHARACTERISTICS

**SENSE Pins Total Source Current**



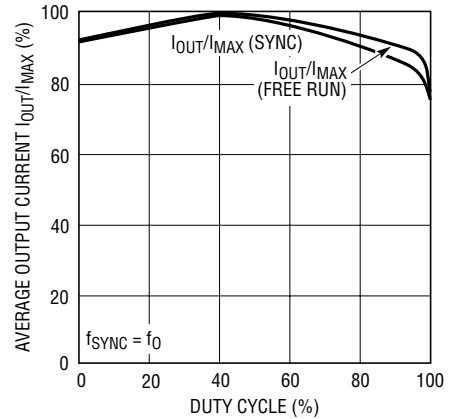
1735 G16

**$I_{TH}$  Voltage vs Load Current**



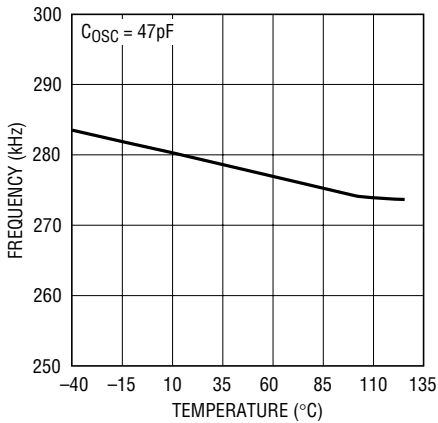
1735 G17

**Output Current vs Duty Cycle**



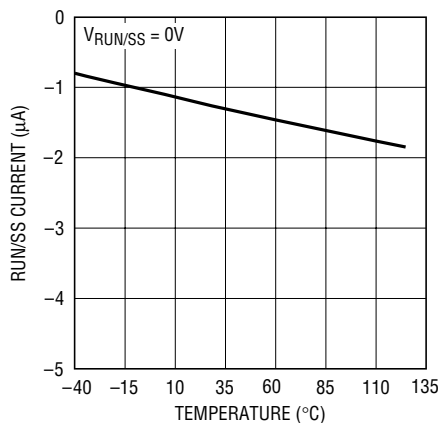
1735 G14

**Oscillator Frequency vs Temperature**



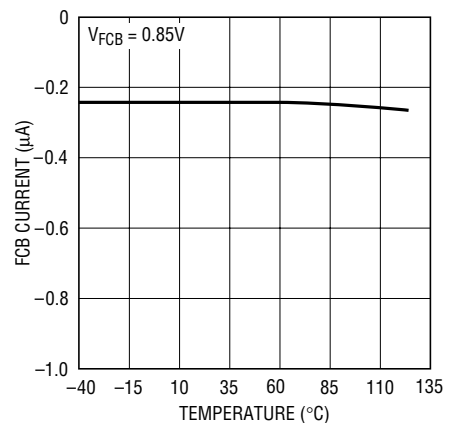
1735 G19

**RUN/SS Pin Current vs Temperature**



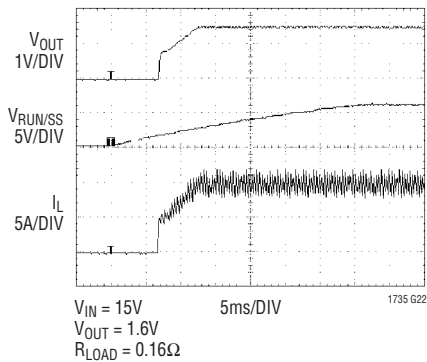
1735 G20

**FCB Pin Current vs Temperature**



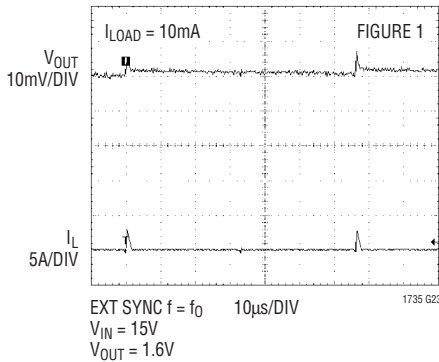
1735 G21

**Start-Up**



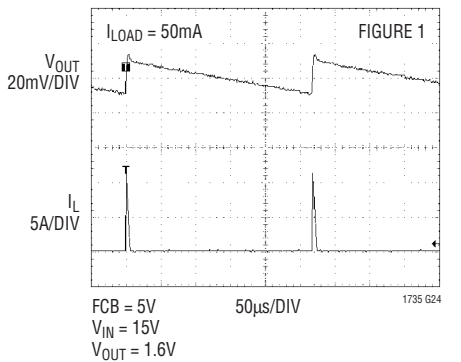
1735 G22

**$V_{OUT}$ (RIPPLE) (Synchronized)**



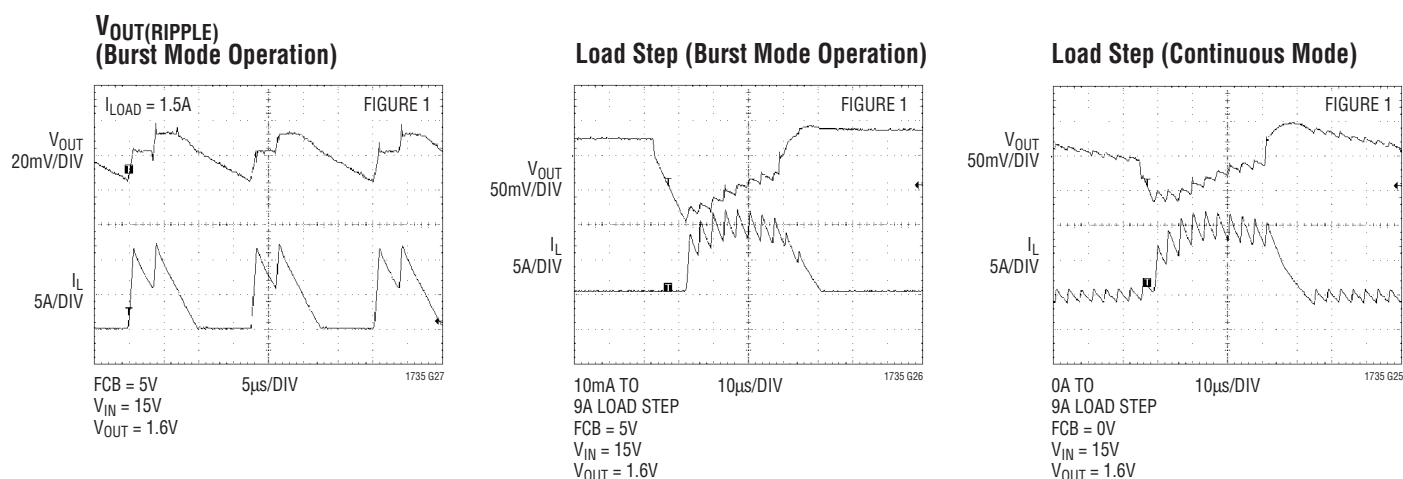
1735 G23

**$V_{OUT}$ (RIPPLE) (Burst Mode Operation)**



1735 G24

## TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS

**C<sub>OSSC</sub>:** External capacitor C<sub>OSSC</sub> from this pin to ground sets the operating frequency.

**RUN/SS:** Combination of Soft-Start and Run Control Inputs. A capacitor to ground at this pin sets the ramp time to full output current. The time is approximately 1.25s/μF. Forcing this pin below 1.5V causes the device to be shutdown. In shutdown all functions are disabled. Latchoff overcurrent protection is also invoked via this pin as described in the Applications Information section.

**I<sub>TH</sub>:** Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 2.4V.

**FCB:** Forced Continuous/Synchronization Input. Tie this pin to ground for continuous synchronous operation, to a resistive divider from the secondary output when using a secondary winding or to INTV<sub>CC</sub> to enable Burst Mode operation at low load currents. Clocking this pin with a signal above 1.5V<sub>P-P</sub> disables Burst Mode operation but allows cycle-skipping at low load currents and synchronizes the internal oscillator with the external clock.

**SGND:** Small-Signal Ground. All small-signal components such as C<sub>OSSC</sub>, C<sub>SS</sub>, the feedback divider plus the loop compensation resistors and capacitor(s) should single-point tie to this pin. This pin should, in turn, connect to PGND.

**V<sub>OSENSE</sub>:** Receives the feedback voltage from an external resistive divider across the output.

**SENSE<sup>-</sup>:** The (-) Input to the Current Comparator.

**SENSE<sup>+</sup>:** The (+) Input to the Current Comparator. Built-in offsets between SENSE<sup>-</sup> and SENSE<sup>+</sup> pins in conjunction with R<sub>SENSE</sub> set the current trip threshold.

**PGOOD (LTC1735F Only):** Open-Drain Logic Output. PGOOD is pulled to ground when the voltage on the V<sub>OSENSE</sub> pin is not within ±7.5% of its set point.

**EXTV<sub>CC</sub>:** Input to the Internal Switch Connected to INTV<sub>CC</sub>. This switch closes and supplies V<sub>CC</sub> power whenever EXTV<sub>CC</sub> is higher than 4.7V. See EXTV<sub>CC</sub> connection in the Applications Information section. Do not exceed 7V on this pin and ensure EXTV<sub>CC</sub> ≤ V<sub>IN</sub>.

**PGND:** Driver Power Ground. Connects to the source of bottom N-channel MOSFET, the anode of the Schottky diode, and the (-) terminal of C<sub>IN</sub>.

**BG:** High Current Gate Drive for Bottom N-Channel MOSFET. Voltage swing at this pin is from ground to INTV<sub>CC</sub>.

**INTV<sub>CC</sub>:** Output of the Internal 5.2V Regulator and EXTV<sub>CC</sub> Switch. The driver and control circuits are powered from this voltage. Decouple to power ground with a 1μF ceramic capacitor placed directly adjacent to the IC together with a minimum of 4.7μF tantalum or other low ESR capacitor.

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## OPERATION (Refer to Functional Diagram)

ence, which in turn causes the  $I_{TH}$  voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by current comparator  $I_2$ , or the beginning of the next cycle.

The top MOSFET driver is powered from a floating bootstrap capacitor  $C_B$ . This capacitor is normally recharged from  $INTV_{CC}$  through an external diode when the top MOSFET is turned off. As  $V_{IN}$  decreases towards  $V_{OUT}$ , the converter will attempt to turn on the top MOSFET continuously (“dropout”). A dropout counter detects this condition and forces the top MOSFET to turn off for about 500ns every tenth cycle to recharge the bootstrap capacitor.

The main control loop is shut down by pulling Pin 2 (RUN/SS) low. Releasing RUN/SS allows an internal 1.2 $\mu$ A current source to charge soft-start capacitor  $C_{SS}$ . When  $C_{SS}$  reaches 1.5V, the main control loop is enabled with the  $I_{TH}$  voltage clamped at approximately 30% of its maximum value. As  $C_{SS}$  continues to charge,  $I_{TH}$  is gradually released allowing normal operation to resume. If  $V_{OUT}$  has not reached 70% of its final value when  $C_{SS}$  has charged to 4.1V, latching can be invoked as described in the Applications Information section.

The internal oscillator can be synchronized to an external clock applied to the FCB pin and can lock to a frequency between 90% and 130% of its nominal rate set by capacitor  $C_{OSC}$ .

An overvoltage comparator,  $OV$ , guards against transient overshoots (>7.5%) as well as other more serious conditions that may overvoltage the output. In this case, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Foldback current limiting for an output shorted to ground is provided by amplifier A. As  $V_{OSENSE}$  drops below 0.6V, the buffered  $I_{TH}$  input to the current comparator is gradually pulled down to a 0.86V clamp. This reduces peak inductor current to about 1/4 of its maximum value.

### Low Current Operation

The LTC1735 has three low current modes controlled by the FCB pin. Burst Mode operation is selected when the

FCB pin is above 0.8V (typically tied to  $INTV_{CC}$ ). In Burst Mode operation, if the error amplifier drives the  $I_{TH}$  voltage below 0.86V, the buffered  $I_{TH}$  input to the current comparator will be clamped at 0.86V. The inductor current peak is then held at approximately  $20mV/R_{SENSE}$  (about 1/4 of maximum output current). If  $I_{TH}$  then drops below 0.5V, the Burst Mode comparator B will turn off both MOSFETs to maximize efficiency. The load current will be supplied solely by the output capacitor until  $I_{TH}$  rises above the 60mV hysteresis of the comparator and switching is resumed. Burst Mode operation is disabled by comparator F when the FCB pin is brought below 0.8V. This forces continuous operation and can assist secondary winding regulation.

When the FCB pin is driven by an external oscillator, a low noise cycle-skipping mode is invoked and the internal oscillator is synchronized to the external clock by comparator C. In this mode the 25% minimum inductor current clamp is removed, providing constant frequency discontinuous operation over the widest possible output current range. This constant frequency operation is not quite as efficient as Burst Mode operation, but provides a lower noise, constant frequency spectrum.

The FCB pin is tied to ground when forced continuous operation is desired. This is the least efficient mode, but is desirable in certain applications. The output can source or sink current in this mode. When sinking current while in forced continuous operation, current will be forced back into the main power supply potentially boosting the input supply to dangerous voltage levels—BEWARE.

### Foldback Current, Short-Circuit Detection and Short-Circuit Latchoff

The RUN/SS capacitor,  $C_{SS}$ , is used initially to limit the inrush current of the switching regulator. After the controller has been started and been given adequate time to charge up the output capacitors and provide full load current,  $C_{SS}$  is used as a short-circuit time-out circuit. If the output voltage falls to less than 70% of its nominal output voltage,  $C_{SS}$  begins discharging on the assumption that the output is in an overcurrent and/or short-circuit condition. If the condition lasts for a long enough period as determined by the size of  $C_{SS}$ , the controller will be shut

## OPERATION (Refer to Functional Diagram)

down until the RUN/SS pin voltage is recycled. This built-in latching can be overridden by providing a current  $>5\mu\text{A}$  at a compliance of 5V to the RUN/SS pin. This current shortens the soft-start period but also prevents net discharge of  $C_{SS}$  during an overcurrent and/or short-circuit condition. Foldback current limiting is activated when the output voltage falls below 70% of its nominal level whether or not the short-circuit latching circuit is enabled.

### INTV<sub>CC</sub>/EXTV<sub>CC</sub> POWER

Power for the top and bottom MOSFET drivers and most of the internal circuitry of the LTC1735 is derived from the INTV<sub>CC</sub> pin. When the EXTV<sub>CC</sub> pin is left open, an internal 5.2V low dropout regulator supplies the INTV<sub>CC</sub> power from V<sub>IN</sub>. If EXTV<sub>CC</sub> is raised above 4.7V, the internal

regulator is turned off and an internal switch connects EXTV<sub>CC</sub> to INTV<sub>CC</sub>. This allows a high efficiency source, such as the primary or a secondary output of the converter itself, to provide the INTV<sub>CC</sub> power. Voltages up to 7V can be applied to EXTV<sub>CC</sub> for additional gate drive capability.

To provide clean start-up and to protect the MOSFETs, undervoltage lockout is used to keep both MOSFETs off until the input voltage is above 3.5V.

### PGOOD (LTC1735F Only)

A window comparator monitors the output voltage and its open-drain output is pulled low when the divided down output voltage is not within  $\pm 7.5\%$  of the reference voltage of 0.8V.

## APPLICATIONS INFORMATION

The basic LTC1735 application circuit is shown in Figure 1 on the first page. External component selection is driven by the load requirement and begins with the selection of R<sub>SENSE</sub>. Once R<sub>SENSE</sub> is known, C<sub>O<sub>SC</sub></sub> and L can be chosen. Next, the power MOSFETs and D1 are selected. The operating frequency and the inductor are chosen based largely on the desired amount of ripple current. Finally, C<sub>IN</sub> is selected for its ability to handle the large RMS current into the converter and C<sub>OUT</sub> is chosen with low enough ESR to meet the output voltage ripple and transient specifications. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 28V (limited by the external MOSFETs).

### R<sub>SENSE</sub> Selection for Output Current

R<sub>SENSE</sub> is chosen based on the required output current. The LTC1735 current comparator has a maximum threshold of  $75\text{mV}/R_{\text{SENSE}}$  and an input common mode range of SGND to 1.1(INTV<sub>CC</sub>). The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I<sub>MAX</sub> equal to the peak value less half the peak-to-peak ripple current,  $\Delta I_L$ .

Allowing a margin for variations in the LTC1735 and external component values yields:

$$R_{\text{SENSE}} = \frac{50\text{mV}}{I_{\text{MAX}}}$$

### C<sub>O<sub>SC</sub></sub> Selection for Operating Frequency and Synchronization

The choice of operating frequency and inductor value is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, both gate charge loss and transition loss. However, lower frequency operation requires more inductance for a given amount of ripple current.

The LTC1735 uses a constant frequency architecture with the frequency determined by an external oscillator capacitor C<sub>O<sub>SC</sub></sub>. Each time the topside MOSFET turns on, the voltage on C<sub>O<sub>SC</sub></sub> is reset to ground. During the on-time, C<sub>O<sub>SC</sub></sub> is charged by a fixed current. When the voltage on the capacitor reaches 1.19V, C<sub>O<sub>SC</sub></sub> is reset to ground. The process then repeats.

## APPLICATIONS INFORMATION

The value of  $C_{OSC}$  is calculated from the desired operating frequency assuming no external clock input on the FCB pin:

$$C_{OSC}(\text{pF}) = \left[ \frac{1.61(10^7)}{\text{Frequency}} \right] - 11$$

A graph for selecting  $C_{OSC}$  versus frequency is shown in Figure 2. The maximum recommended switching frequency is 550kHz.

The internal oscillator runs at its nominal frequency ( $f_0$ ) when the FCB pin is pulled high to  $INTV_{CC}$  or connected to ground. Clocking the FCB pin above and below 0.8V will cause the internal oscillator to injection lock to an external clock signal applied to the FCB pin with a frequency between  $0.9f_0$  and  $1.3f_0$ . The clock high level must exceed 1.3V for at least  $0.3\mu\text{s}$  and the clock low level must be less than 0.3V for at least  $0.3\mu\text{s}$ . The top MOSFET turn-on will synchronize with the rising edge of the clock.

Attempting to synchronize to too high an external frequency (above  $1.3f_0$ ) can result in inadequate slope compensation and possible loop instability. If this condition exists simply lower the value of  $C_{OSC}$  so  $f_{EXT} = f_0$  according to Figure 2.

When synchronized to an external clock, Burst Mode operation is disabled but the inductor current is not allowed to reverse. The 25% minimum inductor current clamp present in Burst Mode operation is removed,

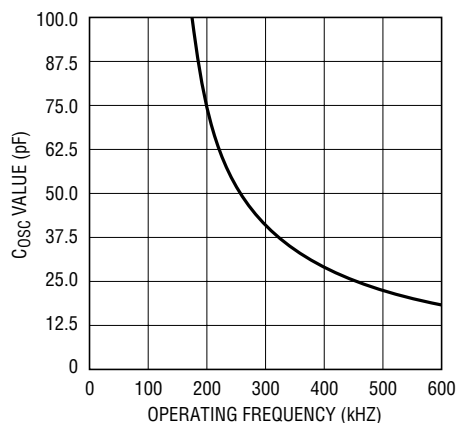


Figure 2. Timing Capacitor Value

providing constant frequency discontinuous operation over the widest possible output current range. In this mode the synchronous MOSFET is forced on once every 10 clock cycles to recharge the bootstrap capacitor. This minimizes audible noise while maintaining reasonably high efficiency.

### Inductor Value Calculation

The operating frequency and inductor selection are inter-related in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current  $\Delta I_L$  decreases with higher inductance or frequency and increases with higher  $V_{IN}$  or  $V_{OUT}$ :

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT} \left[ 1 - \frac{V_{OUT}}{V_{IN}} \right]$$

Accepting larger values of  $\Delta I_L$  allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is  $\Delta I_L = 0.3$  to  $0.4(I_{MAX})$ . Remember, the maximum  $\Delta I_L$  occurs at the maximum input voltage.

The inductor value also has an effect on low current operation. The transition to low current operation begins when the inductor current reaches zero while the bottom MOSFET is on. Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by  $R_{SENSE}$ . Lower inductor values (higher  $\Delta I_L$ ) will cause this to occur at higher load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

## APPLICATIONS INFORMATION

### Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool M $\mu$ <sup>®</sup> cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool M $\mu$ . Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, designs for surface mount are available that do not increase the height significantly.

### Power MOSFET and D1 Selection

Two external power MOSFETs must be selected for use with the LTC1735: An N-channel MOSFET for the top (main) switch and an N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak gate drive levels are set by the INTV<sub>CC</sub> voltage. This voltage is typically 5.2V during start-up (see EXTV<sub>CC</sub> pin connection). Consequently, logic-level threshold MOSFETs must be used in most LTC1735 applications. The only exception is when low input voltage is expected ( $V_{IN} < 5V$ ); then, sub-logic level threshold MOSFETs ( $V_{GS(TH)} < 3V$ ) should be used. Pay close attention to the BV<sub>DSS</sub> specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the “ON” resistance  $R_{DS(ON)}$ , reverse transfer capacitance  $C_{RSS}$ , input voltage and maximum output current. When the LTC1735 is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \delta) R_{DS(ON)} + k (V_{IN})^2 (I_{MAX}) (C_{RSS}) (f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \delta) R_{DS(ON)}$$

where  $\delta$  is the temperature dependency of  $R_{DS(ON)}$  and k is a constant inversely related to the gate drive current.

Both MOSFETs have  $I^2R$  losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For  $V_{IN} < 20V$  the high current efficiency generally improves with larger MOSFETs, while for  $V_{IN} > 20V$  the transition losses rapidly increase to the point that the use of a higher  $R_{DS(ON)}$  device with lower  $C_{RSS}$  actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage or during a short-circuit when the duty cycle in this switch is nearly 100%.

The term  $(1 + \delta)$  is generally given for a MOSFET in the form of a normalized  $R_{DS(ON)}$  vs Temperature curve, but  $\delta = 0.005/^\circ C$  can be used as an approximation for low voltage MOSFETs.  $C_{RSS}$  is usually specified in the MOSFET characteristics. The constant  $k = 1.7$  can be used to estimate the contributions of the two terms in the main switch dissipation equation.

Kool M $\mu$  is a registered trademark of Magnetics, Inc.

## APPLICATIONS INFORMATION

The Schottky diode D1 shown in Figure 1 conducts during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency. A 3A Schottky is generally a good size for 10A to 12A regulators due to the relatively small average current. Larger diodes can result in additional transition losses due to their larger junction capacitance. The diode may be omitted if the efficiency loss can be tolerated.

### C<sub>IN</sub> Selection

In continuous mode, the source current of the top N-channel MOSFET is a square wave of duty cycle  $V_{OUT}/V_{IN}$ . To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \cong I_{O(MAX)} \frac{V_{OUT}}{V_{IN}} \left( \frac{V_{IN}}{V_{OUT}} - 1 \right)^{1/2}$$

This formula has a maximum at  $V_{IN} = 2V_{OUT}$ , where  $I_{RMS} = I_{O(MAX)}/2$ . This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

### C<sub>OUT</sub> Selection

The selection of  $C_{OUT}$  is primarily determined by the effective series resistance (ESR) to minimize voltage ripple. The output ripple ( $\Delta V_{OUT}$ ) in continuous mode is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left( ESR + \frac{1}{8fC_{OUT}} \right)$$

Where  $f$  = operating frequency,  $C_{OUT}$  = output capacitance and  $\Delta I_L$  = ripple current in the inductor. The output ripple is highest at maximum input voltage since  $\Delta I_L$

increases with input voltage. Typically, once the ESR requirement for  $C_{OUT}$  has been met, the RMS current rating generally far exceeds the  $I_{RIPPLE(P-P)}$  requirement. With  $\Delta I_L = 0.3I_{OUT(MAX)}$  and allowing 2/3 of the ripple due to ESR the output ripple will be less than 50mV at max  $V_{IN}$  assuming:

$$C_{OUT} \text{ required ESR} < 2.2 R_{SENSE}$$

$$C_{OUT} > 1/(8fR_{SENSE})$$

The first condition relates to the ripple current into the ESR of the output capacitance while the second term guarantees that the output capacitance does not significantly discharge during the operating frequency period due to ripple current. The choice of using smaller output capacitance increases the ripple voltage due to the discharging term but can be compensated for by using capacitors of very low ESR to maintain the ripple voltage at or below 50mV. The  $I_{TH}$  pin OPTI-LOOP compensation components can be optimized to provide stable, high performance transient response regardless of the output capacitors selected.

The selection of output capacitors for CPU or other applications with large load current transients is primarily determined by the voltage tolerance specifications of the load. The resistive component of the capacitor, ESR, multiplied by the load current change plus any output voltage ripple must be within the voltage tolerance of the load (CPU).

The required ESR due to a load current step is:

$$R_{ESR} < \Delta V / \Delta I$$

where  $\Delta I$  is the change in current from full load to zero load (or minimum load) and  $\Delta V$  is the allowed voltage deviation (not including any droop due to finite capacitance).

The amount of capacitance needed is determined by the maximum energy stored in the inductor. The capacitance must be sufficient to absorb the change in inductor current when a high current to low current transition occurs. The opposite load current transition is generally determined by the control loop OPTI-LOOP components, so make sure not to over compensate and slow down the response. The minimum capacitance to assure the inductors' energy is adequately absorbed is:

## APPLICATIONS INFORMATION

$$C_{OUT} > \frac{L(\Delta I)^2}{2(\Delta V)V_{OUT}}$$

where  $\Delta I$  is the change in load current.

Manufacturers such as Nichicon, United Chemicon and Sanyo can be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest (ESR)(size) product of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON capacitors is recommended to reduce the inductance effects.

In surface mount applications multiple capacitors may need to be used in parallel to meet the ESR, RMS current handling and load step requirements of the application. Aluminum electrolytic, dry tantalum and special polymer capacitors are available in surface mount packages. Special polymer surface mount capacitors offer very low ESR but have much lower capacitive density per unit volume than other capacitor types. These capacitors offer a very cost-effective output capacitor solution and are an ideal choice when combined with a controller having high loop bandwidth. Tantalum capacitors offer the highest capacitance density and are often used as output capacitors for switching regulators having controlled soft-start. Several excellent surge-tested choices are the AVX TPS, AVX TPSV or the KEMET T510 series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Aluminum electrolytic capacitors can be used in cost-driven applications providing that consideration is given to ripple current ratings, temperature and long-term reliability. A typical application will require several to many aluminum electrolytic capacitors in parallel. A combination of the above mentioned capacitors will often result in maximizing performance and minimizing overall cost. Other capacitor types include Nichicon PL series, NEC Neocap, Panasonic SP and Sprague 595D series. Consult manufacturers for other specific recommendations.

Like all components, capacitors are not ideal. Each capacitor has its own benefits and limitations. Combinations of different capacitor types have proven to be a very cost effective solution. Remember also to include high frequency decoupling capacitors. They should be placed

as close as possible to the power pins of the load. Any inductance present in the circuit board traces negates their usefulness.

### INTV<sub>CC</sub> Regulator

An internal P-channel low dropout regulator produces the 5.2V supply that powers the drivers and internal circuitry within the LTC1735. The INTV<sub>CC</sub> pin can supply a maximum RMS current of 50mA and must be bypassed to ground with a minimum of 4.7 $\mu$ F tantalum, 10 $\mu$ F special polymer or low ESR type electrolytic capacitor. A 1 $\mu$ F ceramic capacitor placed directly adjacent to the INTV<sub>CC</sub> and PGND IC pins is highly recommended. Good bypassing is required to supply the high transient currents required by the MOSFET gate drivers.

Higher input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC1735 to be exceeded. The system supply current is normally dominated by the gate charge current. Additional loading of INTV<sub>CC</sub> also needs to be taken into account for the power dissipation calculations. The total INTV<sub>CC</sub> current can be supplied by either the 5.2V internal linear regulator or by the EXTV<sub>CC</sub> input pin. When the voltage applied to the EXTV<sub>CC</sub> pin is less than 4.7V, all of the INTV<sub>CC</sub> current is supplied by the internal 5.2V linear regulator. Power dissipation for the IC in this case is highest:  $(V_{IN})(I_{INTVCC})$  and overall efficiency is lowered. The gate charge is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, the LTC1735CS is limited to less than 17mA from a 30V supply when not using the EXTV<sub>CC</sub> pin as follows:

$$T_J = 70^\circ\text{C} + (17\text{mA})(30\text{V})(110^\circ\text{C}/\text{W}) = 126^\circ\text{C}$$

Use of the EXTV<sub>CC</sub> input pin reduces the junction temperature to:

$$T_J = 70^\circ\text{C} + (17\text{mA})(5\text{V})(110^\circ\text{C}/\text{W}) = 79^\circ\text{C}$$

To prevent maximum junction temperature from being exceeded, the input supply current must be checked operating in continuous mode at maximum  $V_{IN}$ .

## APPLICATIONS INFORMATION

### EXTV<sub>CC</sub> Connection

The LTC1735 contains an internal P-channel MOSFET switch connected between the EXTV<sub>CC</sub> and INTV<sub>CC</sub> pins. Whenever the EXTV<sub>CC</sub> pin is above 4.7V the internal 5.2V regulator shuts off, the switch closes and INTV<sub>CC</sub> power is supplied via EXTV<sub>CC</sub> until EXTV<sub>CC</sub> drops below 4.5V. This allows the MOSFET gate drive and control power to be derived from the output or other external source during normal operation. When the output is out of regulation (start-up, short circuit) power is supplied from the internal regulator. Do not apply greater than 7V to the EXTV<sub>CC</sub> pin and ensure that  $EXTV_{CC} \leq V_{IN}$ .

Significant efficiency gains can be realized by powering INTV<sub>CC</sub> from the output, since the  $V_{IN}$  current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Efficiency). For 5V regulators this simply means connecting the EXTV<sub>CC</sub> pin directly to  $V_{OUT}$ . However, for 3.3V and other lower voltage regulators, additional circuitry is required to derive INTV<sub>CC</sub> power from the output.

The following list summarizes the four possible connections for EXTV<sub>CC</sub>:

1. EXTV<sub>CC</sub> left open (or grounded). This will cause INTV<sub>CC</sub> to be powered from the internal 5.2V regulator resulting in an efficiency penalty of up to 10% at high input voltages.
2. EXTV<sub>CC</sub> connected directly to  $V_{OUT}$ . This is the normal connection for a 5V output regulator and provides the highest efficiency. For output voltages higher than 5V, EXTV<sub>CC</sub> is required to connect to  $V_{OUT}$  so the SENSE pins' absolute maximum ratings are not exceeded.
3. EXTV<sub>CC</sub> connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting EXTV<sub>CC</sub> to an output-derived voltage that has been boosted to greater than 4.7V. This can be done with either the inductive boost winding as shown in Figure 3a or the capacitive charge pump shown in Figure 3b. The charge pump has the advantage of simple magnetics.
4. EXTV<sub>CC</sub> connected to an external supply. If an external supply is available in the 5V to 7V range ( $EXTV_{CC} \leq V_{IN}$ ), such as notebook main 5V system power, it may be used to power EXTV<sub>CC</sub> providing it is compatible with the

MOSFET gate drive requirements. This is the typical case as the 5V power is almost always present and is derived by another high efficiency regulator.

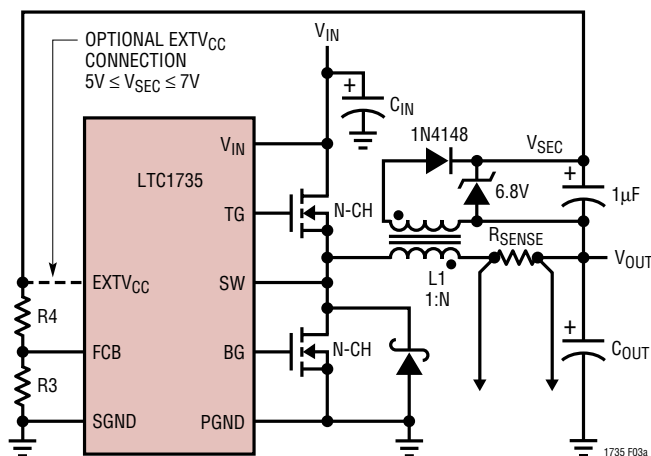


Figure 3a. Secondary Output Loop and EXTV<sub>CC</sub> Connection

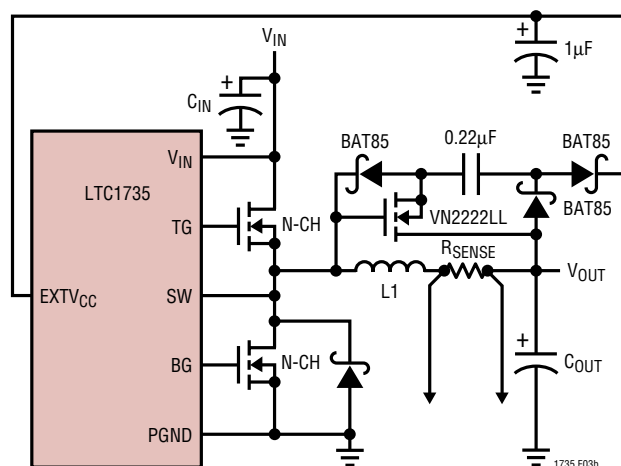


Figure 3b. Capacitive Charge Pump for EXTV<sub>CC</sub>

### Output Voltage Programming

The output voltage is set by an external resistive divider according to the following formula:

$$V_{OUT} = 0.8V \left( 1 + \frac{R2}{R1} \right)$$

The resistive divider is connected to the output as shown in Figure 4 allowing remote voltage sensing.

sn1735 1735fas

## APPLICATIONS INFORMATION

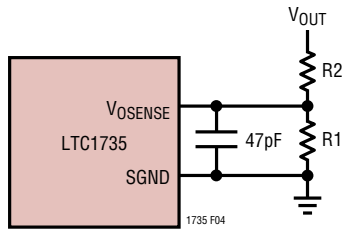


Figure 4. Setting the LTC1735 Output Voltage

Topside MOSFET Driver Supply ( $C_B$ ,  $D_B$ )

An external bootstrap capacitor  $C_B$  connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. Capacitor  $C_B$  in the Functional Diagram is charged through external diode  $D_B$  from  $INTV_{CC}$  when the SW pin is low. Note that the voltage across  $C_B$  is about a diode drop below  $INTV_{CC}$ . When the topside MOSFET is to be turned on, the driver places the  $C_B$  voltage across the gate-source of the MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage SW rises to  $V_{IN}$  and the BOOST pin rises to  $V_{IN} + INTV_{CC}$ . The value of the boost capacitor  $C_B$  needs to be 100 times greater than the total input capacitance of the topside MOSFET. In most applications 0.1 $\mu$ F to 0.33 $\mu$ F is adequate. The reverse breakdown on  $D_B$  must be greater than  $V_{IN(MAX)}$ .

*When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If you make a change and the input current decreases, then you improved the efficiency. If there is no change in input current, then there is no change in efficiency.*

SENSE<sup>+</sup>/SENSE<sup>-</sup> Pins

The common mode input range of the current comparator is from 0V to 1.1( $INTV_{CC}$ ). Continuous linear operation in step-down applications is guaranteed throughout this range allowing output voltages anywhere from 0.8V to 7V. A differential NPN input stage is used and is biased with internal resistors from an internal 2.4V source as shown in the Functional Diagram. This causes current to either be sourced or sunk by the sense pins depending on the output voltage. If the output voltage is below 2.4V current will flow out of both sense pins to the main output. This forces a minimum load current that can be fulfilled by the

$V_{OUT}$  resistive divider. The maximum current flowing out of the sense pins is:

$$I_{SENSE^+} + I_{SENSE^-} = (2.4V - V_{OUT})/24k$$

Since  $V_{OSENSE}$  is servoed to the 0.8V reference voltage, we can choose R1 in Figure 4 to have a maximum value to absorb this current:

$$R1_{(MAX)} = 24k \left( \frac{0.8V}{2.4V - V_{OUT}} \right)$$

Regulating an output voltage of 1.8V, the maximum value of R1 should be 32k. Note that at output voltages above 2.4V no maximum value of R1 is necessary to absorb the sense pin currents; however, R1 is still bounded by the  $V_{OSENSE}$  feedback current.

## Soft-Start/Run Function

The RUN/SS pin is a multipurpose pin that provides a soft-start function and a means to shut down the LTC1735. Soft-start reduces surge currents from  $V_{IN}$  by gradually increasing the controller's current limit  $I_{TH(MAX)}$ . This pin can also be used for power supply sequencing.

Pulling the RUN/SS pin below 1.5V puts the LTC1735 into a low quiescent current shutdown ( $I_Q < 25\mu A$ ). This pin can be driven directly from logic as shown in Figure 5. Releasing the RUN/SS pin allows an internal 1.2 $\mu A$  current source to charge up the external soft-start capacitor  $C_{SS}$ . If RUN/SS has been pulled all the way to ground there is a delay before starting of approximately:

$$t_{DELAY} = \frac{1.5V}{1.2\mu A} C_{SS} = (1.25s/\mu F) C_{SS}$$

When the voltage on RUN/SS reaches 1.5V the LTC1735 begins operating with a current limit at approximately 25mV/ $R_{SENSE}$ . As the voltage on the RUN/SS pin increases from 1.5V to 3.0V, the internal current limit is increased from 25mV/ $R_{SENSE}$  to 75mV/ $R_{SENSE}$ . The output current limit ramps up slowly, taking an additional 1.25s/ $\mu F$  to reach full current. The output current thus ramps up slowly, reducing the starting surge current required from the input power supply.

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Diode D1 in Figure 5 reduces the start delay while allowing  $C_{SS}$  to charge up slowly for the soft-start function. This diode and  $C_{SS}$  can be deleted if soft-start is not needed. The RUN/SS pin has an internal 6V zener clamp (See Functional Diagram).

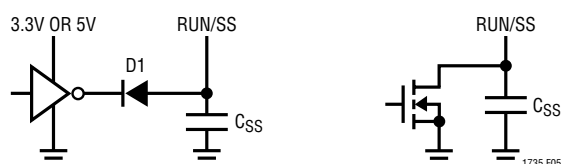


Figure 5. RUN/SS Pin Interfacing

### Fault Conditions: Overcurrent Latchoff

The RUN/SS pin also provides the ability to shut off the controller and latch off when an overcurrent condition is detected. The RUN/SS capacitor,  $C_{SS}$ , is used initially to turn on and limit the inrush current of the controller. After the controller has been started and given adequate time to charge up the output capacitor and provide full load current,  $C_{SS}$  is used as a short-circuit timer. If the output voltage falls to less than 70% of its nominal output voltage *after*  $C_{SS}$  reaches 4.1V, the assumption is made that the output is in a severe overcurrent and/or short-circuit condition and  $C_{SS}$  begins discharging. If the condition lasts for a long enough period as determined by the size of  $C_{SS}$ , the controller will be shut down until the RUN/SS pin voltage is recycled.

This built-in latchoff can be overridden by providing a current  $>5\mu\text{A}$  at a compliance of 5V to the RUN/SS pin as shown in Figure 6. This current shortens the soft-start period but also prevents net discharge of the RUN/SS

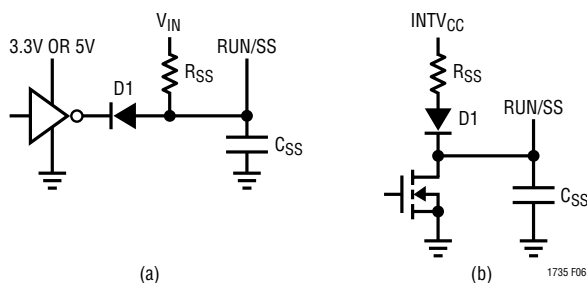


Figure 6. RUN/SS Pin Interfacing with Latchoff Defeated

capacitor during a severe overcurrent and/or short-circuit condition. When deriving the  $5\mu\text{A}$  current from  $V_{IN}$  as in Figure 6a, current latchoff is always defeated. Diode connecting this pull-up resistor to  $\text{INTV}_{CC}$ , as in Figure 6b, eliminates any extra supply current during controller shutdown while eliminating the  $\text{INTV}_{CC}$  loading from preventing controller start-up. If the voltage on  $C_{SS}$  does not exceed 4.1V the overcurrent latch is not armed and the function is disabled.

Why should you defeat overcurrent latchoff? During the prototyping stage of a design, there may be a problem with noise pickup or poor layout causing the protection circuit to latch off. Defeating this feature will easily allow troubleshooting of the circuit and PC layout. The internal short-circuit and foldback current limiting still remains active, thereby protecting the power supply system from failure. After the design is complete, a decision can be made whether to enable the latchoff feature.

The value of the soft-start capacitor  $C_{SS}$  will need to be scaled with output current, output capacitance and load current characteristics. The minimum soft-start capacitance is given by:

$$C_{SS} > (C_{OUT})(V_{OUT})(10^{-4})(R_{SENSE})$$

The minimum recommended soft-start capacitor of  $C_{SS} = 0.1\mu\text{F}$  will be sufficient for most applications.

### Fault Conditions: Current Limit and Current Foldback

The LTC1735 current comparator has a maximum sense voltage of 75mV resulting in a maximum MOSFET current of  $75\text{mV}/R_{SENSE}$ .

The LTC1735 includes current foldback to help further limit load current when the output is shorted to ground. The foldback circuit is active even when the overload shutdown latch described above is defeated. If the output falls by more than half, then the maximum sense voltage is progressively lowered from 75mV to 30mV. Under short-circuit conditions with very low duty cycle, the LTC1735 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be conducting the peak current. The short-circuit ripple current is determined by the minimum on-time

## APPLICATIONS INFORMATION

$t_{ON(MIN)}$  of the LTC1735 (approximately 200ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} V_{IN}/L$$

The resulting short-circuit current is:

$$I_{SC} = \frac{30mV}{R_{SENSE}} + \frac{1}{2} \Delta I_{L(SC)}$$

The current foldback function is always active and is not effected by the current latchoff function.

### Fault Conditions: Output Overvoltage Protection (Crowbar)

The output overvoltage crowbar is designed to blow a system fuse in the input lead when the output of the regulator rises much higher than nominal levels. This condition causes huge currents to flow, much greater than in normal operation. This feature is designed to protect against a shorted top MOSFET; it does not protect against a failure of the controller itself.

The comparator (OV in the Functional Diagram) detects overvoltage faults greater than 7.5% above the nominal output voltage. When this condition is sensed the top MOSFET is turned off and the bottom MOSFET is forced on. The bottom MOSFET remains on continuously for as long as the OV condition persists; if  $V_{OUT}$  returns to a safe level, normal operation automatically resumes.

Note that dynamically changing the output voltage may cause overvoltage protection to be momentarily activated during programmed output voltage decreases. This will not cause permanent latchoff nor will it disrupt the desired voltage change. With soft-latch overvoltage protection, dynamically changing the output voltage is allowed and the overvoltage protection tracks the newly programmed output voltage, always protecting the load.

### Minimum On-Time Considerations

Minimum on-time  $t_{ON(MIN)}$  is the smallest amount of time that the LTC1735 is capable of turning the top MOSFET on and off again. It is determined by internal timing delays and

the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC1735 will begin to skip cycles. The output voltage will continue to be regulated, but the ripple current and voltage will increase.

The minimum on-time for the LTC1735 in a properly configured application is generally less than 200ns. However, as the peak sense voltage decreases, the minimum on-time gradually increases as shown in Figure 7. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

If an application can operate close to the minimum on-time limit, an inductor must be chosen that is low enough to provide sufficient ripple amplitude to meet the minimum on-time requirement. *As a general rule keep the inductor ripple current equal or greater than 30% of  $I_{OUT(MAX)}$  at  $V_{IN(MAX)}$ .*

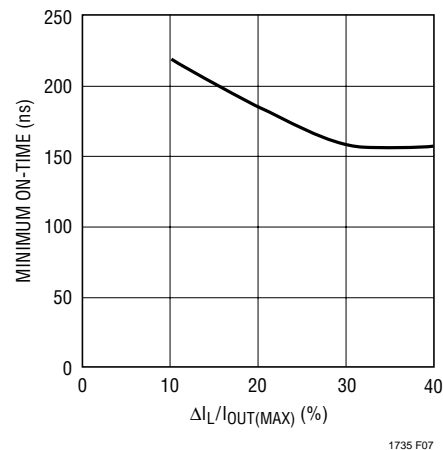


Figure 7. Minimum On-Time vs  $\Delta I_L$

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### FCB Pin Operation

When the FCB pin drops below its 0.8V threshold, continuous mode operation is forced. In this case, the top and bottom MOSFETs continue to be driven synchronously regardless of the load on the main output. Burst Mode operation is disabled and current reversal is allowed in the inductor.

In addition to providing a logic input to force continuous synchronous operation and external synchronization, the FCB pin provides a means to regulate a flyback winding output. During continuous mode, current flows continuously in the transformer primary. The secondary winding(s) draw current only when the bottom, synchronous switch is on. When primary load currents are low and/or the  $V_{IN}/V_{OUT}$  ratio is low, the synchronous switch may not be on for a sufficient amount of time to transfer power from the output capacitor to the secondary load. Forced continuous operation will support secondary windings providing there is sufficient synchronous switch duty factor. Thus, the FCB input pin removes the requirement that power must be drawn from the inductor primary in order to extract power from the auxiliary windings. With the loop in continuous mode, the auxiliary outputs may nominally be loaded without regard to the primary output load.

The secondary output voltage  $V_{SEC}$  is normally set as shown in Figure 3a by the turns ratio  $N$  of the transformer:

$$V_{SEC} \cong (N + 1)V_{OUT}$$

However, if the controller goes into Burst Mode operation and halts switching due to a light primary load current, then  $V_{SEC}$  will droop. An external resistive divider from  $V_{SEC}$  to the FCB pin sets a minimum voltage  $V_{SEC(MIN)}$ :

$$V_{SEC(MIN)} \approx 0.8V \left( 1 + \frac{R4}{R3} \right)$$

If  $V_{SEC}$  drops below this level, the FCB voltage forces continuous switching operation until  $V_{SEC}$  is again above its minimum.

In order to prevent erratic operation if no external connections are made to the FCB pin, the FCB pin has a 0.17 $\mu$ A

internal current source pulling the pin high. Remember to include this current when choosing resistor values  $R3$  and  $R4$ .

The internal LTC1735 oscillator can be synchronized to an external oscillator by applying and clocking the FCB pin with a signal above 1.5V<sub>P-P</sub>. When synchronized to an external frequency, Burst Mode operation is disabled but cycle skipping is allowed at low load currents since current reversal is inhibited. The bottom gate will come on every 10 clock cycles to assure the bootstrap cap is kept refreshed. The rising edge of an external clock applied to the FCB pin starts a new cycle.

The range of synchronization is from  $0.9f_0$  to  $1.3f_0$ , with  $f_0$  set by  $C_{OSC}$ . Attempting to synchronize to a higher frequency than  $1.3f_0$  can result in inadequate slope compensation and cause loop instability with high duty cycles (duty cycle > 50%). If loop instability is observed while synchronized, additional slope compensation can be obtained by simply decreasing  $C_{OSC}$ .

The following table summarizes the possible states available on the FCB pin:

**Table 1**

FCB Pin	Condition
DC Voltage: 0V to 0.7V	Burst Disabled/Forced Continuous Current Reversal Enabled
DC Voltage: $\geq 0.9V$	Burst Mode Operation, No Current Reversal
Feedback Resistors	Regulating a Secondary Winding
Ext Clock: (0V to $V_{FCBSYNC}$ ) ( $V_{FCBSYNC} > 1.5V$ )	Burst Mode Operation Disabled No Current Reversal

### Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{Efficiency} = 100\% - (L1 + L2 + L3 + \dots)$$

where  $L1$ ,  $L2$ , etc. are the individual losses as a percentage of input power.

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Although all dissipative elements in the circuit produce losses, 4 main sources usually account for most of the losses in LTC1735 circuits: 1) LTC1735  $V_{IN}$  current, 2)  $INTV_{CC}$  current, 3)  $I^2R$  losses, 4) Topside MOSFET transition losses.

1) The  $V_{IN}$  current is the DC supply current given in the electrical characteristics which excludes MOSFET driver and control currents.  $V_{IN}$  current results in a small (<0.1%) loss that increases with  $V_{IN}$ .

2)  $INTV_{CC}$  current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge  $dQ$  moves from  $INTV_{CC}$  to ground. The resulting  $dQ/dt$  is a current out of  $INTV_{CC}$  that is typically much larger than the control circuit current. In continuous mode,  $I_{GATECHG} = f(Q_T + Q_B)$ , where  $Q_T$  and  $Q_B$  are the gate charges of the topside and bottom-side MOSFETs.

Supplying  $INTV_{CC}$  power through the  $EXTV_{CC}$  switch input from an output-derived or other high efficiency source will scale the  $V_{IN}$  current required for the driver and control circuits by a factor of (Duty Cycle)/(Efficiency). For example, in a 20V to 5V application, 10mA of  $INTV_{CC}$  current results in approximately 3mA of  $V_{IN}$  current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from  $V_{IN}$ ) to only a few percent.

3)  $I^2R$  losses are predicted from the DC resistances of the MOSFET, inductor and current shunt. In continuous mode the average output current flows through L and  $R_{SENSE}$ , but is “chopped” between the topside main MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same  $R_{DS(ON)}$ , then the resistance of one MOSFET can simply be summed with the resistances of L and  $R_{SENSE}$  to obtain  $I^2R$  losses. For example, if each  $R_{DS(ON)} = 0.03\Omega$ ,  $R_L = 0.05\Omega$  and  $R_{SENSE} = 0.01\Omega$ , then the total resistance is  $0.09\Omega$ . This results in losses ranging from 2% to 9% as the output current increases from 1A to 5A for a 5V output, or a 3% to 14% loss for a 3.3V output. Efficiency varies as the inverse square of  $V_{OUT}$  for the same external components and output power level.  $I^2R$  losses cause the efficiency to drop at high output currents.

4) Transition losses apply only to the topside MOSFET(s) and only become significant when operating at high input voltages (typically 12V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} = (1.7) V_{IN}^2 I_{O(MAX)} C_{RSS} f$$

Other “hidden” losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these “system” level losses in the design of a system. The internal battery and fuse resistance losses can be minimized by making sure that  $C_{IN}$  has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20 $\mu$ F to 40 $\mu$ F of capacitance having a maximum of 0.01 $\Omega$  to 0.02 $\Omega$  of ESR. Other losses including Schottky conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

### Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs,  $V_{OUT}$  shifts by an amount equal to  $\Delta I_{LOAD}$  (ESR), where ESR is the effective series resistance of  $C_{OUT}$ .  $\Delta I_{LOAD}$  also begins to charge or discharge  $C_{OUT}$  generating the feedback error signal that forces the regulator to adapt to the current change and return  $V_{OUT}$  to its steady-state value. During this recovery time  $V_{OUT}$  can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the  $I_{TH}$  pin not only allows optimization of control loop behavior but also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time and settling at this test point truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The  $I_{TH}$  external components shown in the Figure 1 circuit will provide an adequate starting point for most applications.

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The  $I_{TH}$  series  $R_C$ - $C_C$  filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of  $1\mu\text{s}$  to  $10\mu\text{s}$  will produce output voltage and  $I_{TH}$  pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second-order overshoot/DC ratio cannot be used to determine phase margin. The gain of the loop will be increased by increasing  $R_C$  and the bandwidth of the loop will be increased by decreasing  $C_C$ . If  $R_C$  is increased by the same factor that  $C_C$  is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

A second, more severe transient is caused by switching in loads with large ( $>1\mu\text{F}$ ) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with  $C_{OUT}$ , causing a rapid drop in  $V_{OUT}$ . No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of  $C_{LOAD}$  to  $C_{OUT}$  is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately  $(25)(C_{LOAD})$ . Thus a  $10\mu\text{F}$  capacitor would require a  $250\mu\text{s}$  rise time, limiting the charging current to about 200mA.

### Improve Transient Response and Reduce Output Capacitance with Active Voltage Positioning

Fast load transient response, limited board space and low cost are requirements of microprocessor power supplies.

Active voltage positioning improves transient response and reduces the output capacitance required to power a microprocessor where a typical load step can be from 0.2A to 15A in 100ns or 15A to 0.2A in 100ns. The voltage at the microprocessor must be held to about  $\pm 0.1\text{V}$  of nominal in spite of these load current steps. Since the control loop cannot respond this fast, the output capacitors must supply the load current until the control loop can respond. Capacitor ESR and ESL primarily determine the amount of droop or overshoot in the output voltage. Normally, several capacitors in parallel are required to meet microprocessor transient requirements.

Active voltage positioning is a form of deregulation. It sets the output voltage high for light loads and low for heavy loads. When load current suddenly increases, the output voltage starts from a level higher than nominal so the output voltage can droop more and stay within the specified voltage range. When load current suddenly decreases the output voltage starts at a level lower than nominal so the output voltage can have more overshoot and stay within the specified voltage range. Less output capacitance is required when voltage positioning is used because more voltage variation is allowed on the output capacitors.

Active voltage positioning can be implemented using the OPTI-LOOP architecture of the LTC1735 and two resistors connected to the  $I_{TH}$  pin. An input voltage offset is introduced when the error amplifier has to drive a resistive load. This offset is limited to  $\pm 30\text{mV}$  at the input of the error amplifier. The resulting change in output voltage is the product of input offset and the feedback voltage divider ratio.

Figure 8 shows a CPU-core-voltage regulator with active voltage positioning. Resistors R1 and R4 force the input voltage offset that adjusts the output voltage according to the load current level. To select values for R1 and R4, first determine the amount of output deregulation allowed. The actual specification for a typical microprocessor allows the output to vary  $\pm 0.112\text{V}$ . The LTC1735 reference accuracy is  $\pm 1\%$ . Using 1% tolerance resistors, the total feedback divider accuracy is about 1% because both feedback resistors are close to the same value. The resulting setpoint accuracy is  $\pm 2\%$  so the output transient

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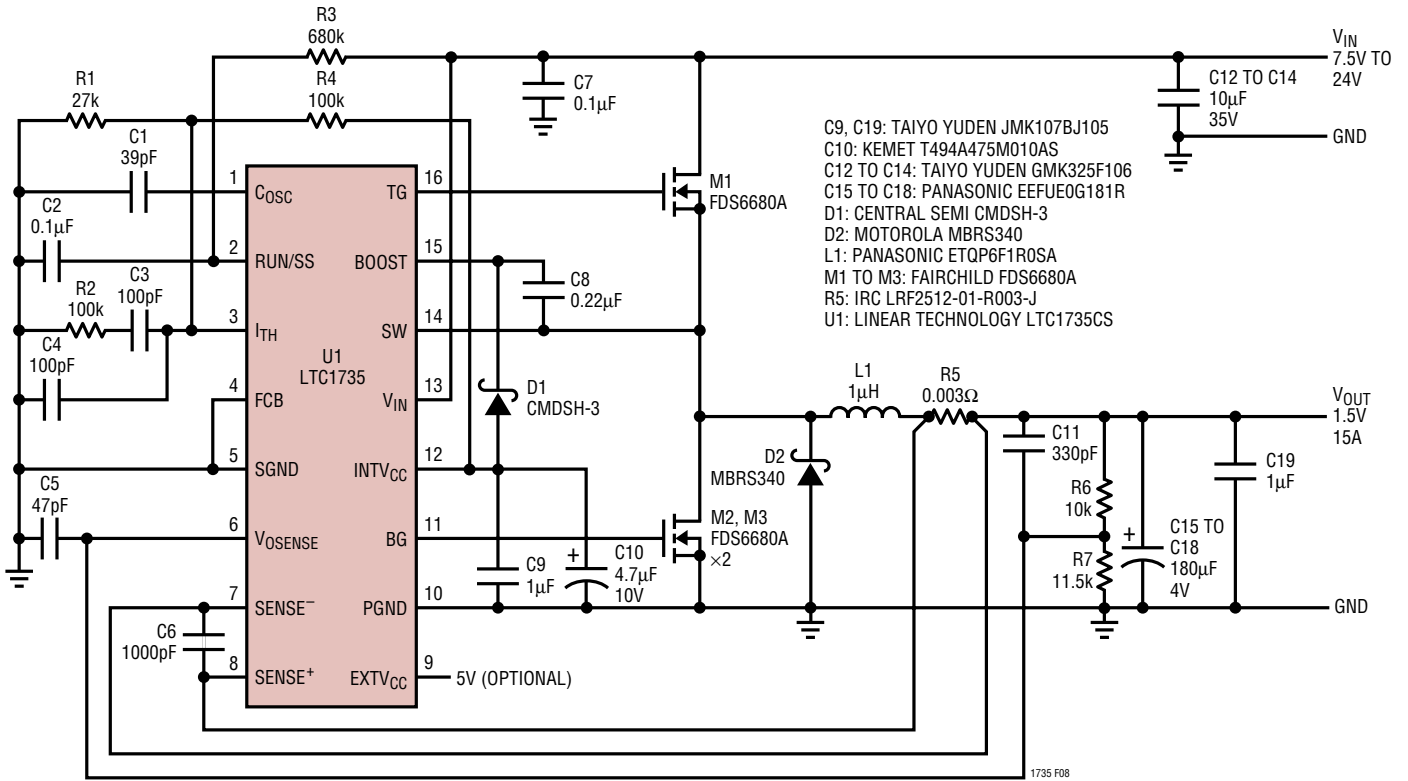


Figure 8. CPU-Core-Voltage Regulator with Active Voltage Positioning

voltage cannot exceed  $\pm 0.082V$ . At  $V_{OUT} = 1.5V$ , the maximum output voltage change controlled by the  $I_{TH}$  pin would be:

$$\begin{aligned} \Delta V_{OSENSE} &= \frac{\text{Input Offset} \cdot V_{OUT}}{V_{REF}} \\ &= \frac{\pm 0.03V \cdot 1.5}{0.8V} = \pm 56mV \end{aligned}$$

With the optimum resistor values at the  $I_{TH}$  pin, the output voltage will swing from 1.55V at minimum load to 1.44V at full load. At this output voltage, active voltage positioning provides an additional  $\pm 56mV$  to the allowable transient voltage on the output capacitors, a 68% improvement over the  $\pm 82mV$  allowed without active voltage positioning.

The next step is to calculate the  $I_{TH}$  pin voltage,  $V_{ITH}$ , scale factor. The  $V_{ITH}$  scale factor reflects the  $I_{TH}$  pin voltage

required for a given load current.  $V_{ITH}$  controls the peak sense resistor voltage, which represents the DC output current plus one half of the peak-to-peak inductor current. The no load to full load  $V_{ITH}$  range is from 0.3V to 2.4V, which controls the sense resistor voltage from 0V to the  $\Delta V_{SENSE(MAX)}$  voltage of 75mV. The calculated  $V_{ITH}$  scale factor with a 0.003Ω sense resistor is:

$$\begin{aligned} V_{ITH} \text{ Scale Factor} &= \frac{V_{ITH} \text{ Range} \cdot \text{Sense Resistor Value}}{\Delta V_{SENSE(MAX)}} \\ &= \frac{(2.4V - 0.3V) \cdot 0.003}{0.075V} = 0.084V/A \end{aligned}$$

$V_{ITH}$  at any load current is:

$$V_{ITH} = \left[ \left( I_{OUTDC} + \frac{\Delta I_L}{2} \right) \cdot V_{ITH} \text{ Scale Factor} \right] + V_{ITH} \text{ Offset}$$

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At full load current:

$$V_{I_{TH}(MAX)} = \left[ \left( 15A + \frac{5A_{P-P}}{2} \right) \cdot 0.084V/A \right] + 0.3V$$

$$= 1.77V$$

At minimum load current:

$$V_{I_{TH}(MIN)} = \left[ \left( 0.2A + \frac{2A_{P-P}}{2} \right) \cdot 0.084V/A \right] + 0.3V$$

$$= 0.40V$$

In this circuit,  $V_{I_{TH}}$  changes from 0.40V at light load to 1.77V at full load, a 1.37V change. Notice that  $\Delta I_L$ , the peak-to-peak inductor current, changes from light load to full load. Increasing the DC inductor current decreases the permeability of the inductor core material, which decreases the inductance and increases  $\Delta I_L$ . The amount of inductance change is a function of the inductor design.

To create the  $\pm 30mV$  input offset, the gain of the error amplifier must be limited. The desired gain is:

$$A_V = \frac{\Delta V_{I_{TH}}}{\text{Input Offset Error}} = \frac{1.37V}{2(0.03V)} = 22.8$$

Connecting a resistor to the output of the transconductance error amplifier will limit the voltage gain. The value of this resistor is:

$$R_{I_{TH}} = \frac{A_V}{\text{Error Amplifier } g_m} = \frac{22.8}{1.3ms} = 17.54k$$

To center the output voltage variation,  $V_{I_{TH}}$  must be centered so that no  $I_{TH}$  pin current flows when the output voltage is nominal.  $V_{I_{TH}(NOM)}$  is the average voltage between  $V_{I_{TH}}$  at maximum output current and minimum output current:

$$V_{I_{TH}(NOM)} = \frac{V_{I_{TH}(MAX)} - V_{I_{TH}(MIN)}}{2} + V_{I_{TH}(MIN)}$$

$$= \frac{1.77V - 0.40V}{2} + 0.40V = 1.085V$$

The Thevenin equivalent of the gain limiting resistance value of 17.54k is made up of a resistor R4 that sources current into the  $I_{TH}$  pin and resistor R1 that sinks current to SGND.

To calculate the resistor values, first determine the ratio between them:

$$k = \frac{V_{INTVCC} - V_{I_{TH}(NOM)}}{V_{I_{TH}(NOM)}} = \frac{5.2V - 1.085V}{1.085V} = 3.79$$

$V_{INTVCC}$  is equal to  $V_{EXTVCC}$  or 5.2V if  $EXTVCC$  is not used. Resistor R4 is:

$$R4 = (k + 1) \cdot R_{I_{TH}} = (3.79 + 1) \cdot 17.54 = 84.0k$$

Resistor R1 is:

$$R1 = \frac{(k + 1) \cdot R_{I_{TH}}}{k} = \frac{(3.79 + 1) \cdot 17.54k}{3.79} = 22.17k$$

Unfortunately, PCB noise can add to the voltage developed across the sense resistor, R5, causing the  $I_{TH}$  pin voltage to be slightly higher than calculated for a given output current. The amount of noise is proportional to the output current level. This PCB noise does not present a serious problem but it does change the effective value of R5 so the calculated values of R1 and R4 may need to be adjusted to achieve the required results. Since PCB noise is a function of the layout, it will be the same on all boards with the same layout.

Figures 9 and 10 show the transient response before and after active voltage positioning is implemented. Notice that active voltage positioning reduced the transient response from almost 200mV<sub>P-P</sub> to a little over 100mV<sub>P-P</sub>.

Refer to Design Solutions 10 for more information about active voltage positioning.

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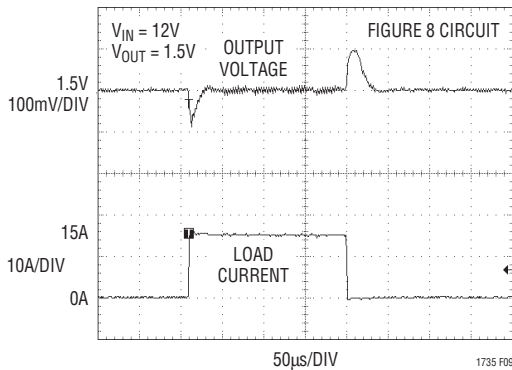


Figure 9. Normal Transient Response (Without R1, R4)

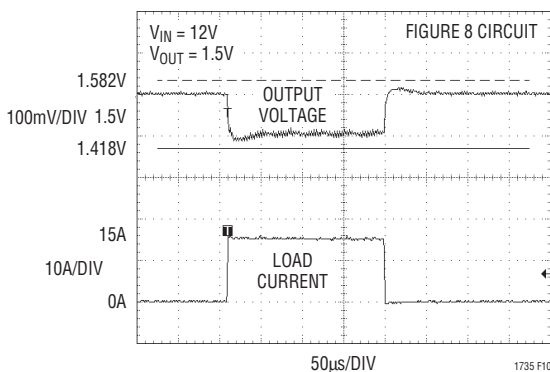


Figure 10. Transient Response with Active Voltage Positioning

## Automotive Considerations: Plugging into the Cigarette Lighter

As battery-powered devices go mobile, there is a natural interest in plugging into the cigarette lighter in order to conserve or even recharge battery packs during operation. But before you connect, be advised: you are plugging into the supply from hell. The main power line in an automobile is the source of a number of nasty potential transients, including load-dump, reverse-battery and double-battery.

Load-dump is the result of a loose battery cable. When the cable breaks connection, the field collapse in the alternator can cause a positive spike as high as 60V which takes several hundred milliseconds to decay. Reverse-battery is just what it says, while double-battery is a consequence of tow-truck operators finding that a 24V jump start cranks cold engines faster than 12V.

The network shown in Figure 11 is the most straightforward approach to protect a DC/DC converter from the ravages of an automotive power line. The series diode prevents current from flowing during reverse-battery, while the transient suppressor clamps the input voltage during load-dump. Note that the transient suppressor should not conduct during double-battery operation, but must still clamp the input voltage below breakdown of the converter. Although the LTC1735 has a maximum input voltage of 36V, most applications will be limited to 30V by the MOSFET  $BV_{DSS}$ .

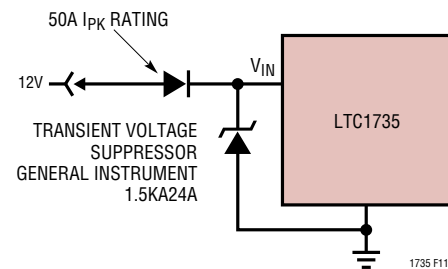


Figure 11. Plugging into the Cigarette Lighter

## Design Example

As a design example, assume  $V_{IN} = 12V$  (nominal),  $V_{IN} = 22V$  (max),  $V_{OUT} = 1.8V$ ,  $I_{MAX} = 5A$  and  $f = 300kHz$ .  $R_{SENSE}$  and  $C_{OSC}$  can immediately be calculated:

$$R_{SENSE} = 50mV/5A = 0.01\Omega$$

$$C_{OSC} = 1.61(10^7)/(300kHz) - 11pF = 43pF$$

Assume a  $3.3\mu H$  inductor and check the actual value of the ripple current. The following equation is used:

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

The highest value of the ripple current occurs at the maximum input voltage:

$$\Delta I_L = \frac{1.8V}{300kHz(3.3\mu H)} \left( 1 - \frac{1.8V}{22V} \right) = 2.3A$$

The maximum ripple current is 33% of maximum output current, which is about right.

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Next verify the minimum on-time of 200ns is not violated. The minimum on-time occurs at maximum  $V_{IN}$ :

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}f} = \frac{1.8V}{22V(300kHz)} = 273ns$$

Since the output voltage is below 2.4V the output resistive divider will need to be sized to not only set the output voltage but also to absorb the sense pin current.

$$\begin{aligned} R1_{(MAX)} &= 24k \left( \frac{0.8V}{2.4V - V_{OUT}} \right) \\ &= 24k \left( \frac{0.8V}{2.4V - 1.8V} \right) = 32k \end{aligned}$$

Choosing 1% resistors;  $R1 = 25.5k$  and  $R2 = 32.4k$  yields an output voltage of 1.816V.

The power dissipation on the topline MOSFET can be easily estimated. Choosing a Siliconix Si4412DY results in  $R_{DS(ON)} = 0.042\Omega$ ,  $C_{RSS} = 100pF$ . At maximum input voltage with  $T$ (estimated) = 50°C:

$$\begin{aligned} P_{MAIN} &= \frac{1.8V}{22V} (5)^2 \left[ 1 + (0.005)(50^\circ C - 25^\circ C) \right] (0.042\Omega) \\ &\quad + 1.7(22V)^2 (5A)(100pF)(300kHz) \\ &= 220mW \end{aligned}$$

Because the duty cycle of the bottom MOSFET is much greater than the top, a larger MOSFET, Siliconix Si4410DY, ( $R_{DS(ON)} = 0.02\Omega$ ) is chosen. The power dissipation in the bottom MOSFET, again assuming  $T_A = 50^\circ C$ , is:

$$\begin{aligned} P_{SYNC} &= \frac{22V - 1.8V}{22V} (5A)^2 (1.1)(0.02\Omega) \\ &= 500mW \end{aligned}$$

Thanks to current foldback, the bottom MOSFET dissipation in short-circuit will be less than under full load conditions.

$C_{IN}$  is chosen for an RMS current rating of at least 2.5A at temperature.  $C_{OUT}$  is chosen with an ESR of  $0.02\Omega$  for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The worst-case output voltage ripple due to ESR is approximately:

$$V_{ORIPPLE} = R_{ESR}(\Delta I_L) = 0.02\Omega(2.3A) = 46mV_{P-P}$$

### PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1735. These items are also illustrated graphically in the layout diagram of Figure 12. Check the following in your layout:

1) Are the signal and power grounds segregated? The LTC1735 PGND pin should tie to the ground plane close to the input capacitor(s). The SGND pin should then connect to PGND and all components that connect to SGND should make a single point tie to the SGND pin. The synchronous MOSFET source pins should connect to the input capacitor(s) ground.

2) Does the  $V_{OSENSE}$  pin connect directly to the feedback resistors? The resistive divider  $R1$ ,  $R2$  must be connected between the (+) plate of  $C_{OUT}$  and signal ground. The 47pF to 100pF capacitor should be as close as possible to the LTC1735. Be careful locating the feedback resistors too far away from the LTC1735. The  $V_{OSENSE}$  line should not be routed close to any other nodes with high slew rates.

3) Are the  $SENSE^-$  and  $SENSE^+$  leads routed together with minimum PC trace spacing? The filter capacitor between  $SENSE^+$  and  $SENSE^-$  should be as close as possible to the LTC1735. Ensure accurate current sensing with Kelvin connections as shown in Figure 13. Series resistance can be added to the  $SENSE$  lines to increase noise rejection.

4) Does the (+) terminal of  $C_{IN}$  connect to the drain of the topline MOSFET(s) as closely as possible? This capacitor provides the AC current to the MOSFET(s).

5) Is the  $INTV_{CC}$  decoupling capacitor connected closely between  $INTV_{CC}$  and the power ground pin? This capacitor carries the MOSFET driver peak currents. An additional 1 $\mu$ F ceramic capacitor placed immediately next to

## APPLICATIONS INFORMATION

the  $INTV_{CC}$  and  $PGND$  pins can help improve noise performance.

6) Keep the switching node (SW), top gate node (TG) and boost node (BOOST) away from sensitive small-signal nodes, especially from the voltage and current sensing

feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the “output side” (Pin 9 to Pin 16) of the LTC1735 and occupy minimum PC trace area.

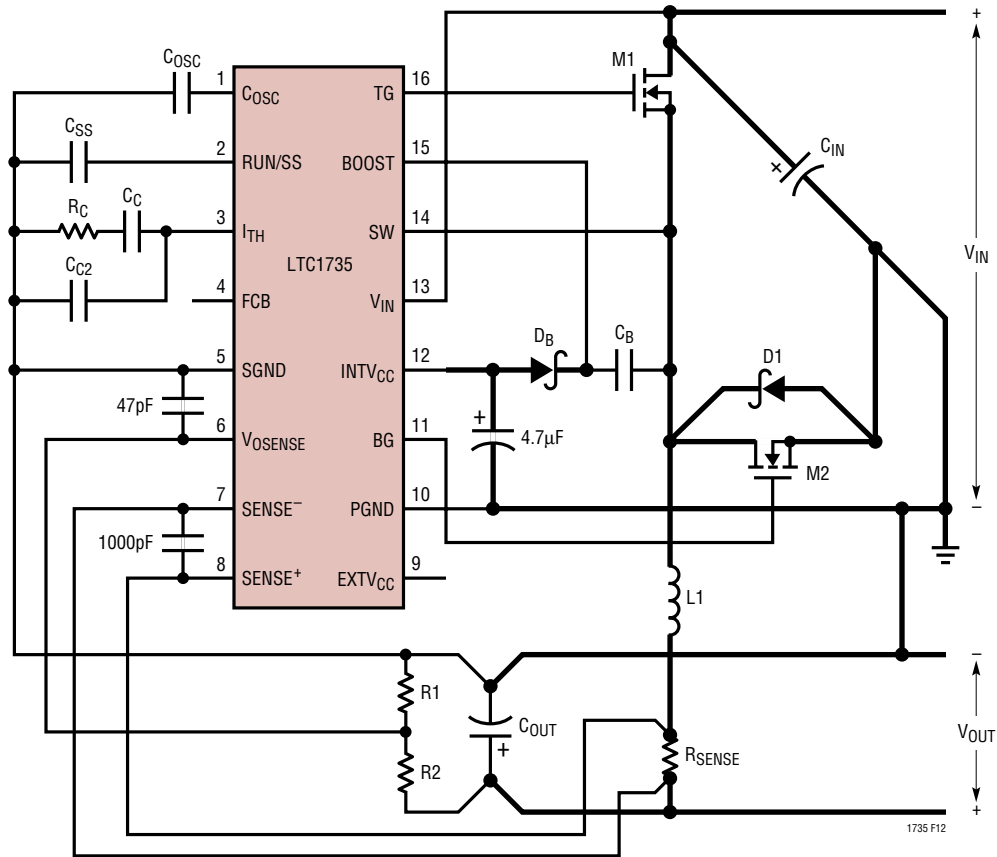


Figure 12. LTC1735 Layout Diagram

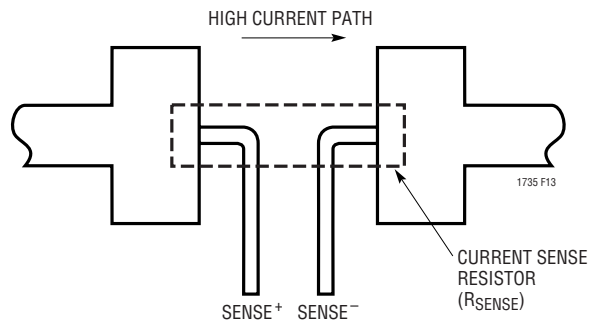
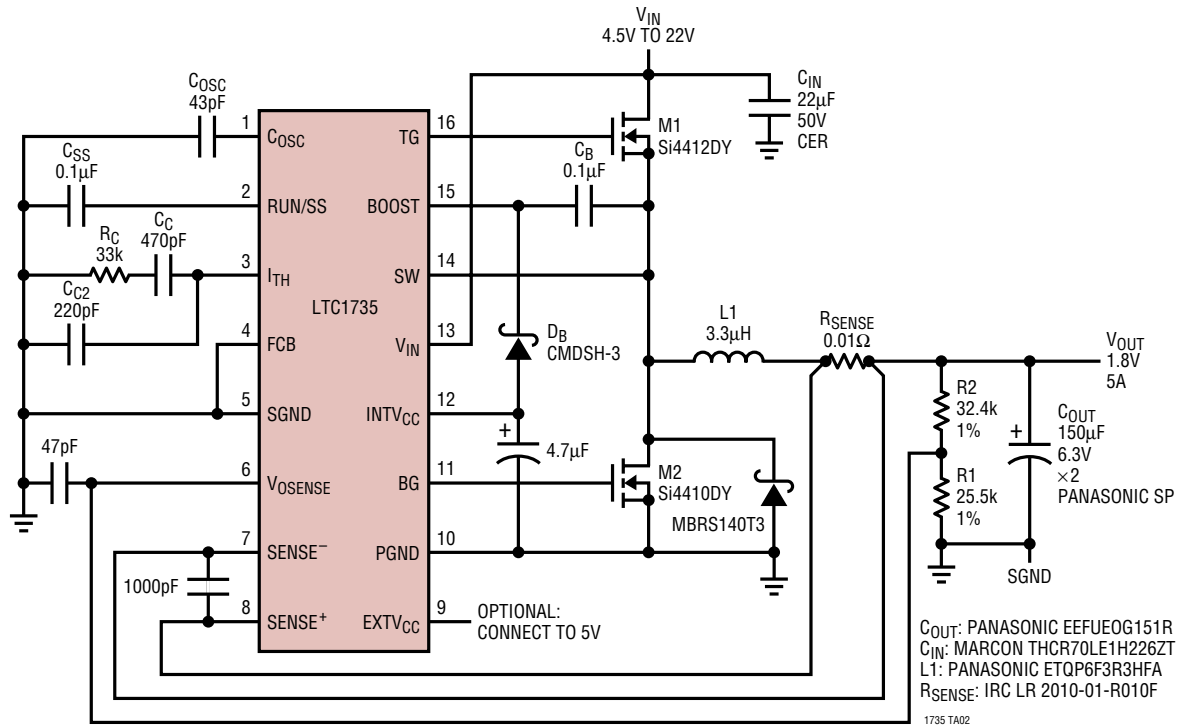


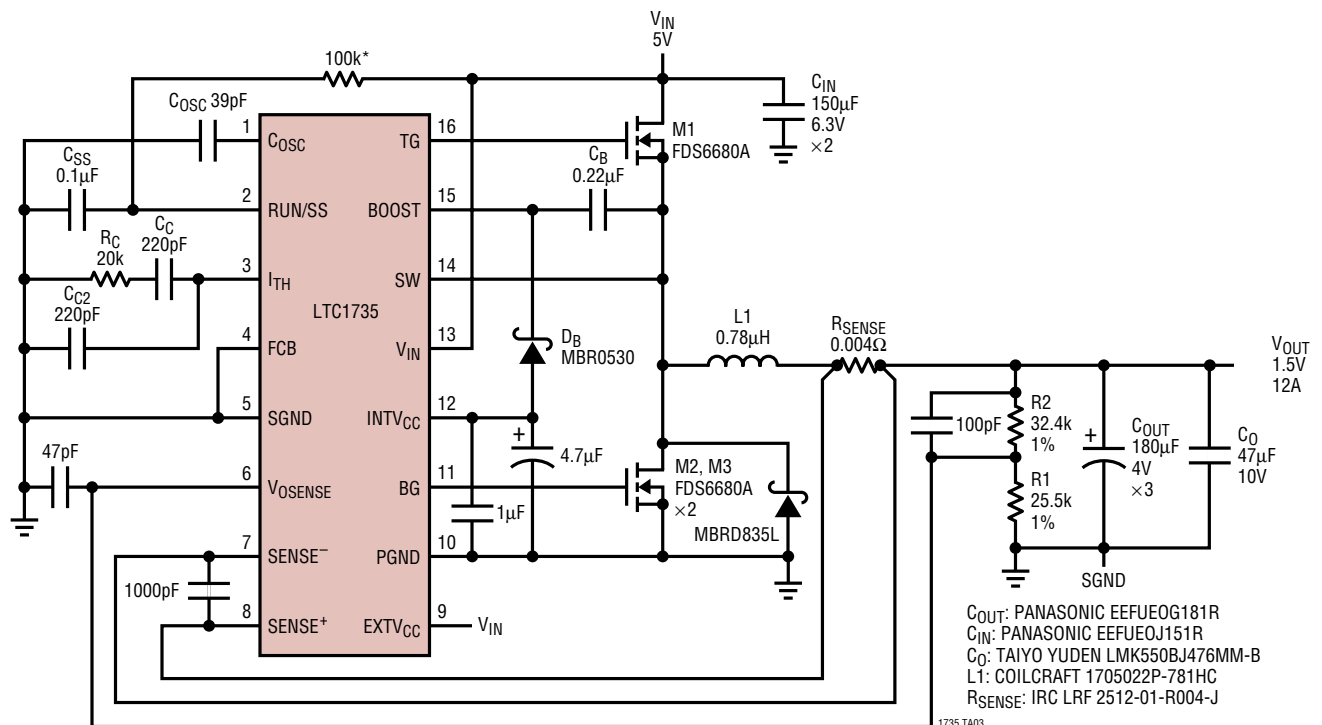
Figure 13. Kelvin Sensing  $R_{SENSE}$

# TYPICAL APPLICATIONS

1.8V/5A Converter from Design Example with Burst Mode Operation Disabled



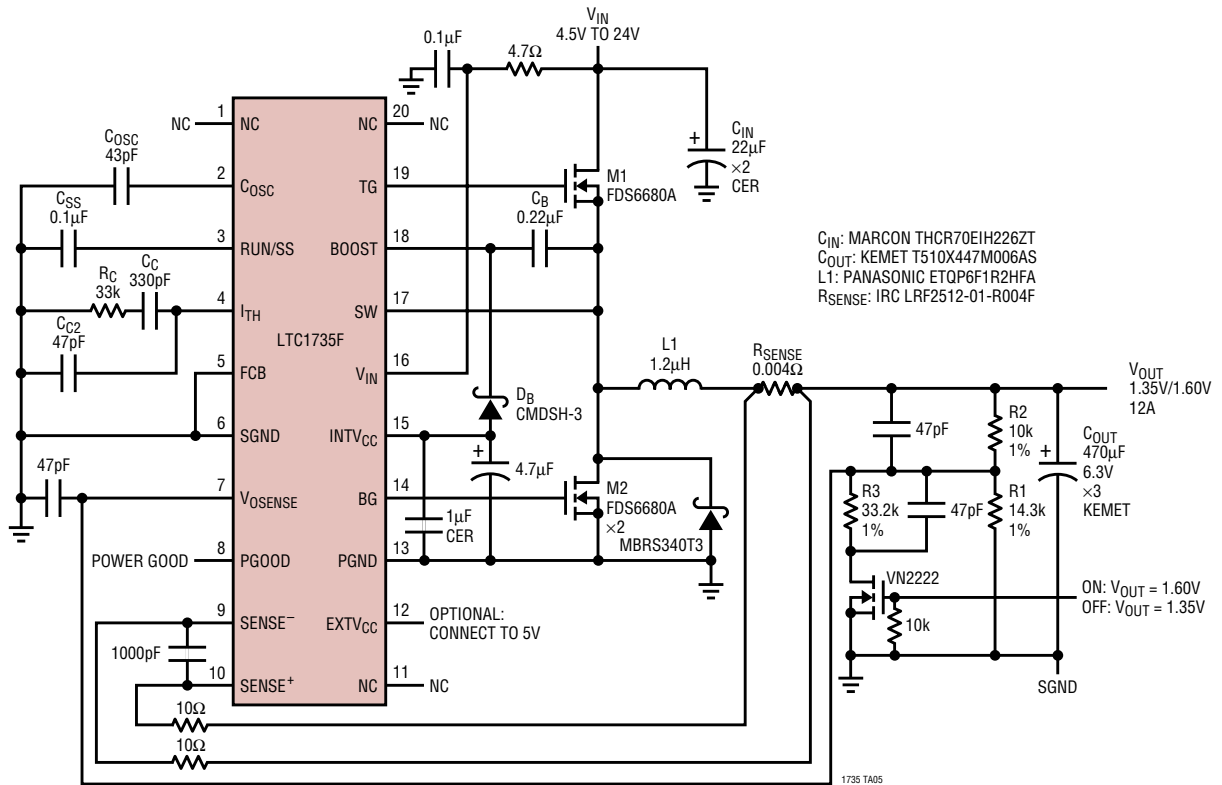
CPU Core Voltage Regulator for 2-Step Applications (V<sub>IN</sub> = 5V)



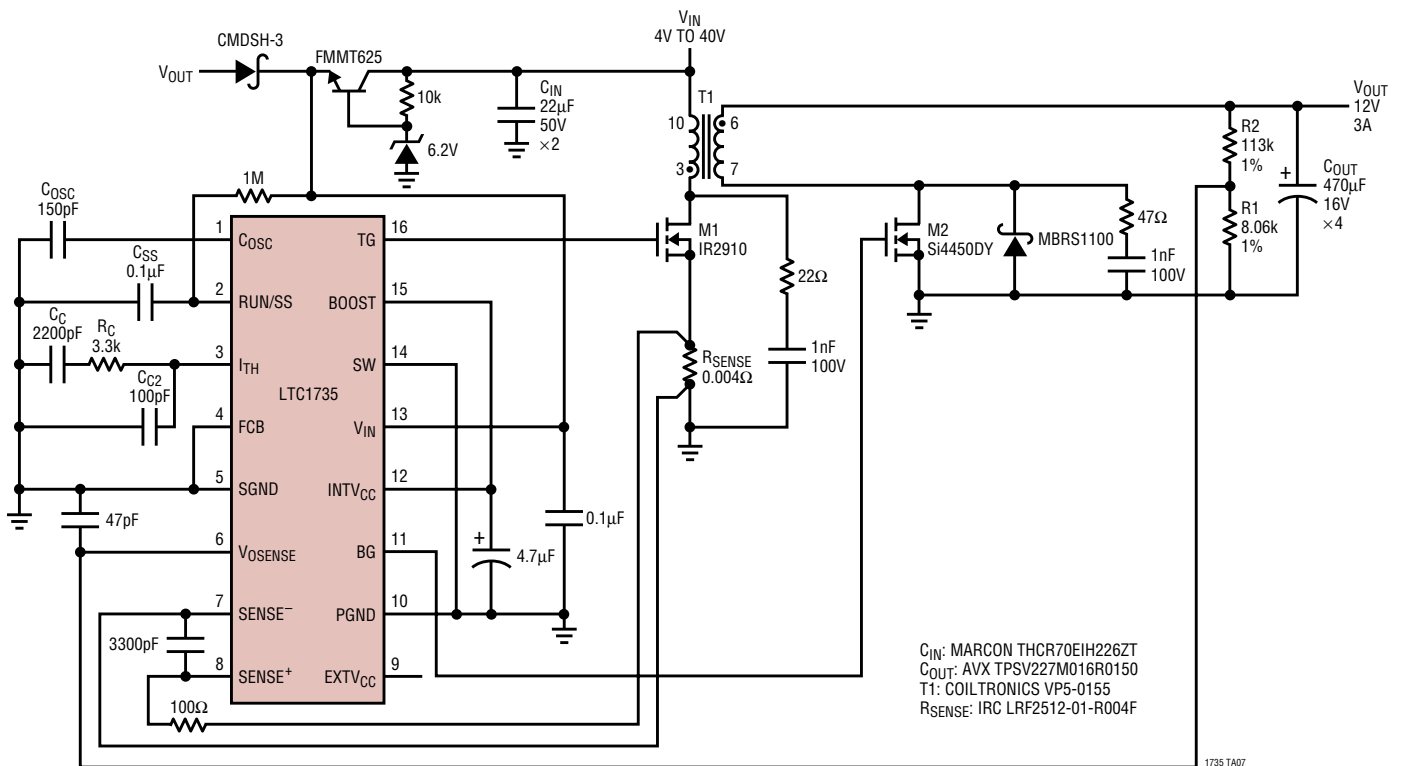
\*OPTIONAL TO DEFEAT OVERCURRENT LATCHOFF

TYPICAL APPLICATIONS

Selectable Output Voltage Converter with Burst Mode Operation Disabled for CPU Power

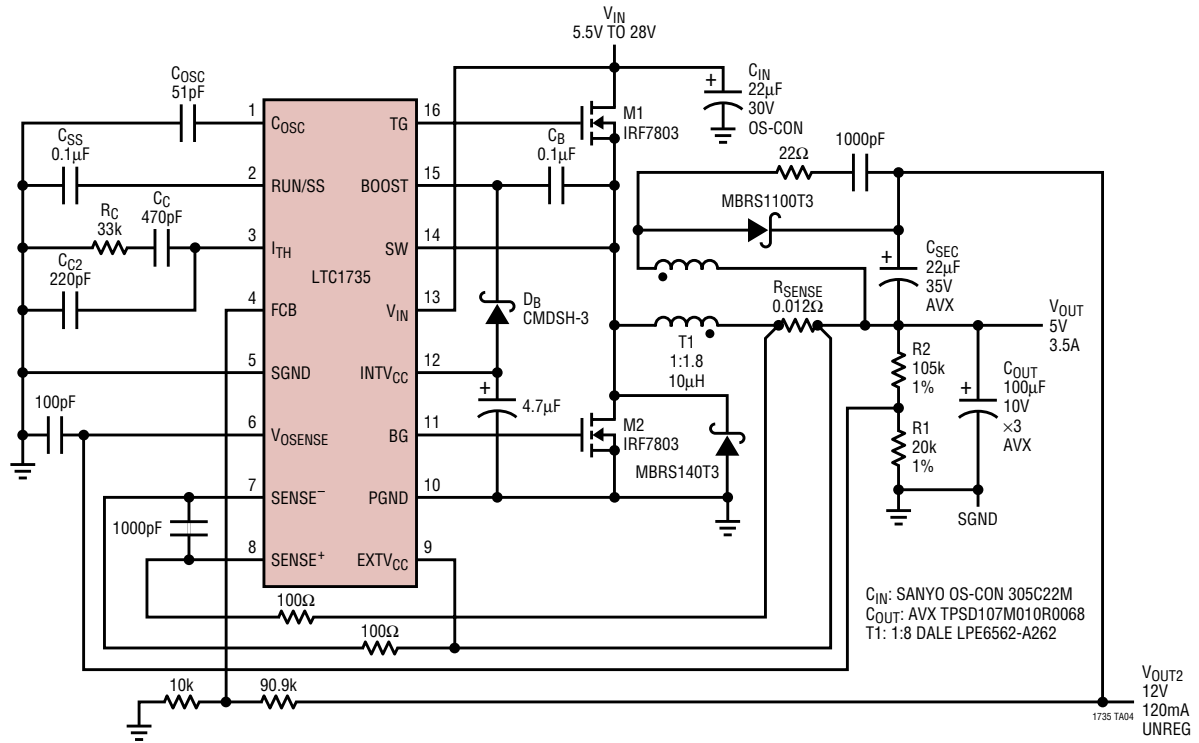


4V to 40V Input to 12V Flyback Converter

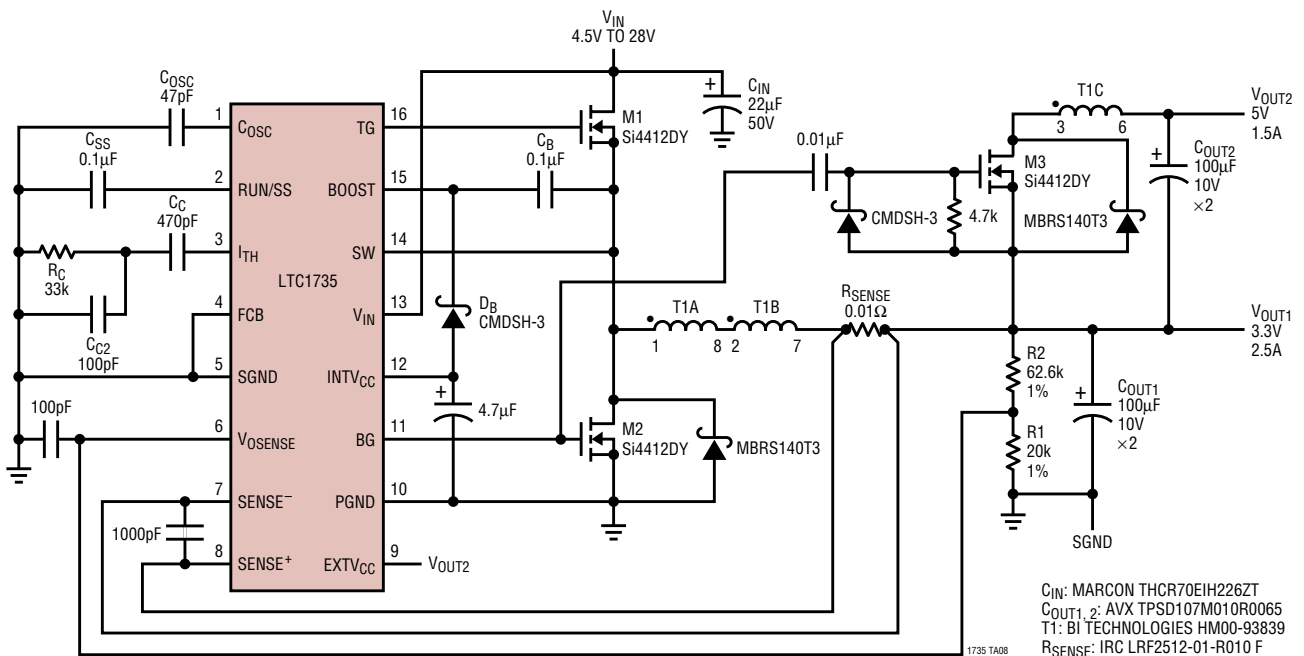


# TYPICAL APPLICATIONS

## 5V/3.5A Converter with 12V/200mA Auxiliary Output

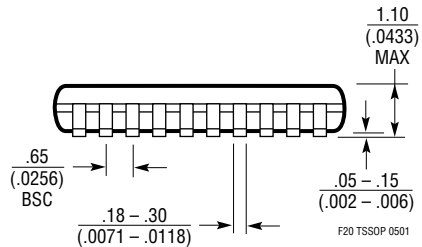
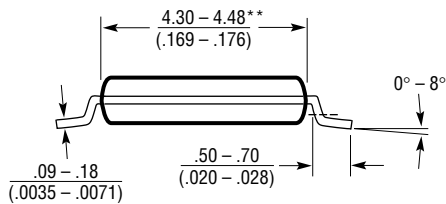
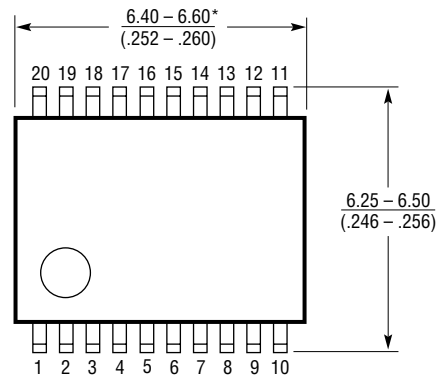


## Dual Output 15W 3.3V/5V Power Supply



**PACKAGE DESCRIPTION**

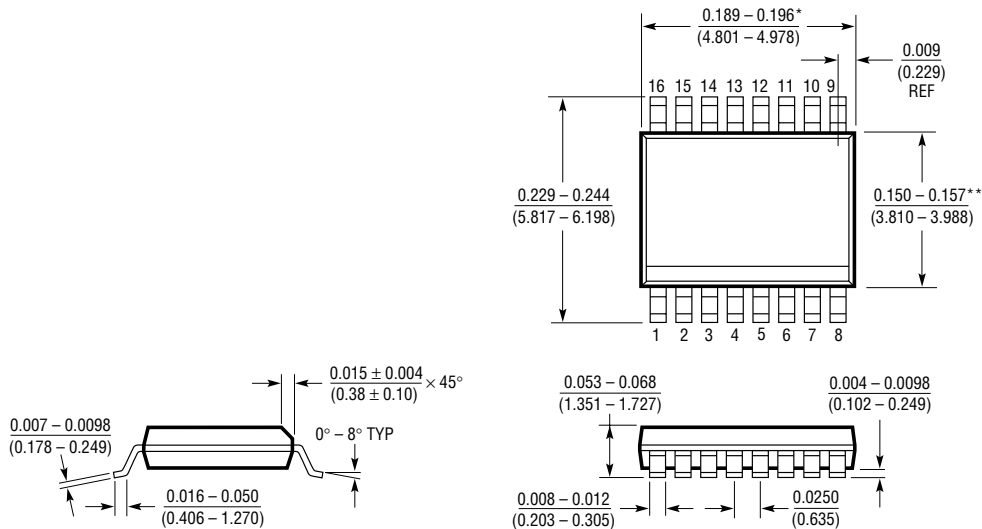
**F Package**  
**20-Lead Plastic TSSOP (4.4mm)**  
 (Reference LTC DWG # 05-08-1650)



- NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
  2. DIMENSIONS ARE IN  $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
  3. DRAWING NOT TO SCALE
- \*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
- \*\*DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

# PACKAGE DESCRIPTION

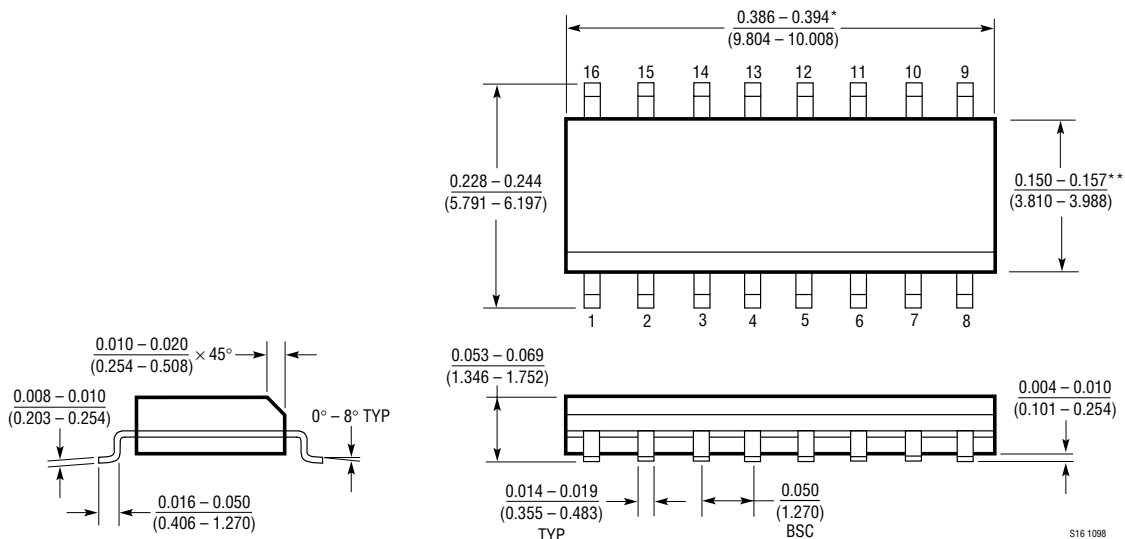
## GN Package 16-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641)



\* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE  
 \*\* DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 1098

## S Package 16-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)

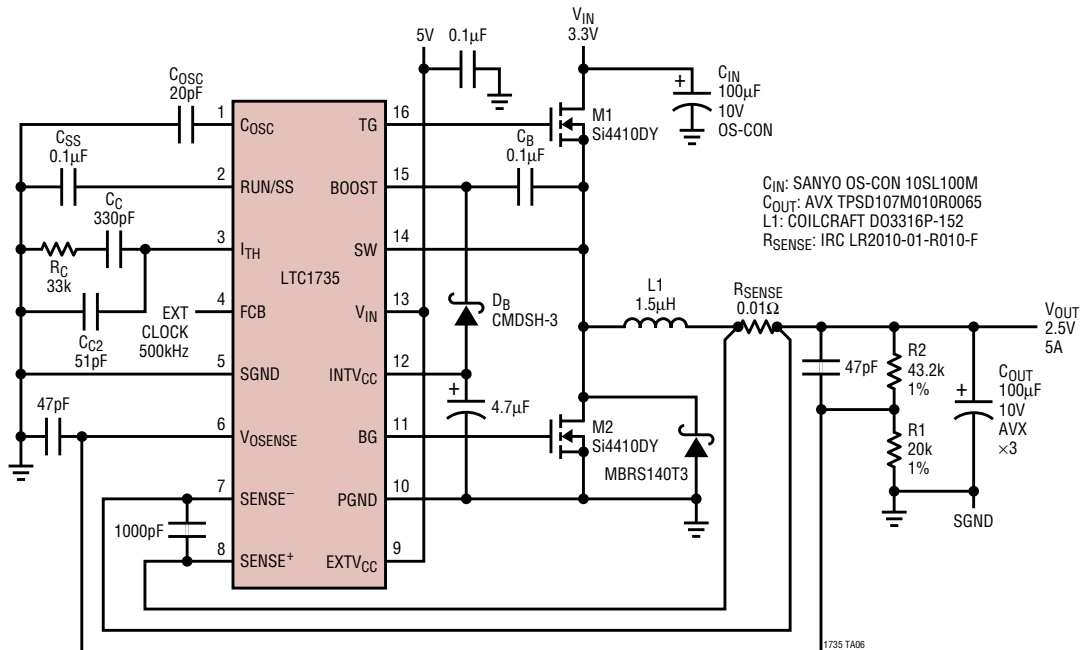


\* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE  
 \*\* DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S16 1098

## TYPICAL APPLICATION

## 3.3V to 2.5V/5A Converter with External Clock Synchronization Operating at 500kHz



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1148HV/LTC1148	High Efficiency Synchronous Step-Down Controller	100% DC*, Burst Mode Operation, $V_{IN} < 20V$
LTC1159	High Efficiency Synchronous Step-Down Controller	100% DC*, Logic Level MOSFETs, $V_{IN} < 40V$
LT1375/LT1376	1.5A 500kHz Step-Down Switching Regulator	High Efficiency, Monolithic, SO-8
LTC1435A	High Efficiency Synchronous Step-Down Controller, N-Ch Drive	Burst Mode Operation, 16-Pin Narrow SO
LTC1436/LTC1436-PLL	High Efficiency Low Noise Synchronous Step-Down Converter, N-Ch Drive	Adaptive Power Mode, 24-Pin SSOP
LTC1624	High Efficiency SO-8 N-Channel Switching Regulator Controller	95% DC*, 3.5V to 36V $V_{IN}$
LTC1625/LTC1775	No $R_{SENSE}$ ™ Current Mode Synchronous Step-Down Controller	Burst Mode Operation, 16-Pin SSOP
LTC1628	Dual High Efficiency 2-Phase Step-Down Controller	Antiphase Drive for Reduced Input Capacitance
LTC1702	550kHz Dual Output Synchronous Step-Down Controller	Antiphase Drive, 24-Pin SSOP
LTC1735-1	High Efficiency Step-Down Controller with Power Good	Output Fault Protection, 16-Pin SO/SSOP
LTC1736	High Efficiency Step-Down Controller with VID Control	Output Fault Protection, 24-Pin SSOP
LTC1771	Ultralow Quiescent Current DC/DC Controller	10µA Standby Current, $2.8V \leq V_{IN} \leq 20V$
LTC1772	SOT-23 Step-Down Controller	100% DC*, Up to 4A, 2.2V to 9.8V $V_{IN}$
LTC1773	Synchronous Step-Down Controller	550kHz Operation, $2.65V \leq V_{IN} \leq 8.5V$ , MS10
LTC1778	No $R_{SENSE}$ Synchronous Step-Down Controller	$4V \leq V_{IN} \leq 36V$ , True Current Mode, Up to 36V Input
LTC1876	Triple Output DC/DC Controller	Dual 2-Phase Synchronous Operation with Step-Up DC/DC Converter
LTC1878	Synchronous Monolithic 0.6A Step-Down Regulator	100% DC*, 2.6V to 6V $V_{IN}$ , 8-Pin MSOP

No  $R_{SENSE}$  is trademark of Linear Technology Corporation. \*DC = Duty Cycle

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