LTC1860L

µPower, 3V, 12-Bit, 150ksps ADC in MSOP

September 2002

FEATURES

- **12-Bit 150ksps ADC in MSOP Package**
- Single 3V Supply
- Low Supply Current: 450µA (Typ)
- Auto Shutdown Reduces Supply Current to 10µA at 1ksps
- True Differential Inputs
- SPI/MICROWIRE™ Compatible Serial I/O
- High Speed Upgrade to LTC1285
- Pin Compatible with 16-Bit LTC1864L

APPLICATIONS

- High Speed Data Acquisition
- Portable or Compact Instrumentation
- Low Power Battery-Operated Instrumentation
- Isolated and/or Remote Data Acquisition

DESCRIPTION

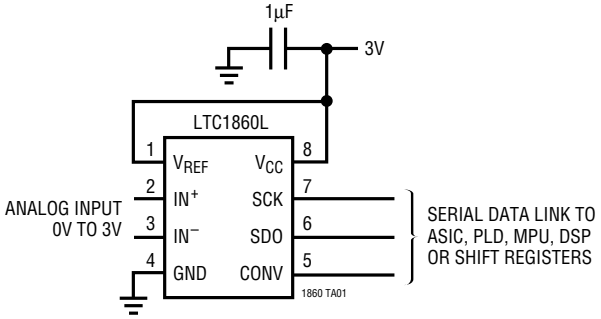
The LTC®1860L is a12-bit A/D converter that is offered in MSOP and SO-8 packages and operates on a single 3V supply. At 150ksps, the supply current is only 450µA. The supply current drops at lower speeds because the LTC1860L automatically powers down between conversions. This 12-bit switched capacitor successive approximation ADC includes a sample-and-hold. The LTC1860L has a differential analog input with an adjustable reference pin.

The 3-wire, serial I/O, small MSOP or SO-8 package and extremely high sample rate-to-power ratio make this ADC an ideal choice for compact, low power, high speed systems.

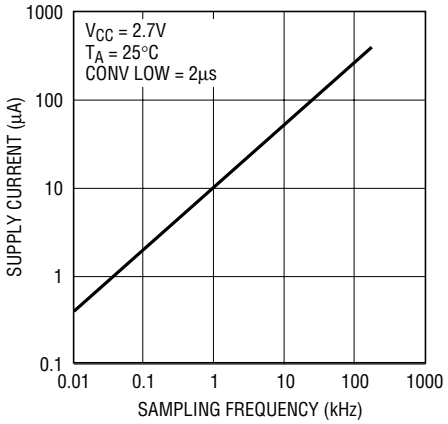
This ADC can be used in ratiometric applications or with external references. The high impedance analog inputs and the ability to operate with reduced spans down to 1V full scale, allow direct connection to signal sources in many applications, eliminating the need for external gain stages.

TYPICAL APPLICATION

Single 3V Supply, 150ksps, 12-Bit Sampling ADC



Supply Current vs Sampling Frequency

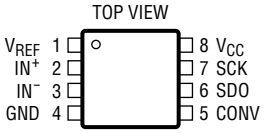


ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage (V_{CC}) 7V
Analog Input ..... (GND – 0.3V) to (V_{CC} + 0.3V)
Digital Input ..... (GND – 0.3V) to 7V
Digital Output ..... (GND – 0.3V) to (V_{CC} + 0.3V)
Power Dissipation 400mW

Operating Temperature Range
LTC1860LC ..... 0°C to 70°C
LTC1860LI ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

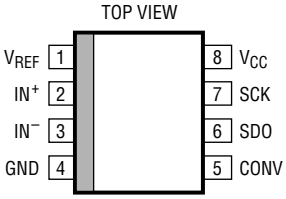
PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 210°C/W

ORDER PART NUMBER
LTC1860LCMS8 LTC1860LIMS8
MS8 PART MARKING
LTD2 LTD3



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 175°C/W

ORDER PART NUMBER
LTC1860LCS8 LTC1860LIS8
MS PART MARKING
1860L 1860LI

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 2.7V, V_{REF} = 2.5V, f_{SCK} = $f_{SCK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution		●	12			Bits
No Missing Codes Resolution		●	12			Bits
INL	(Note 3)	●			±1	LSB
Transition Noise				0.13		LSB_{RMS}
Gain Error		●			±20	mV
Offset Error		●		±2	±5	mV
Analog Input Range	$IN^+ – IN^–$	●	0		V_{REF}	V
Absolute Input Range	IN^+ Input $IN^–$ Input		–0.05 –0.05		V_{CC} + 0.05 V_{CC}/2	V V
V_{REF} Input Range			1		V_{CC}	V
Analog Input Leakage Current	(Note 4)	●			±1	µA
C_{IN} Input Capacitance	In Sample Mode During Conversion			12 5		pF pF

DYNAMIC ACCURACY

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 3V, V_{REF} = 3V, f_{SAMPLE} = 150kHz, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio				72		dB
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	1kHz Input Signal			72		dB
THD	Total Hamonic Distortion Up to 5th Harmonic	1kHz Input Signal			86		dB
	Full Power Bandwidth				10		MHz
	Full Linear Bandwidth	S/(N + D) ≥ 68dB			30		kHz

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 2.7V, V_{REF} = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.3V	●	1.9			V
V_{IL}	Low Level Input Voltage	V_{CC} = 2.7V	●			0.45	V
I_{IH}	High Level Input Current	V_{IN} = V_{CC}	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 2.7V, I_O = 10µA V_{CC} = 2.7V, I_O = 360µA	● ●	2.3 2.1	2.60 2.45		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 2.7V, I_O = 400µA	●			0.3	V
I_{OZ}	Hi-Z Output Leakage	CONV = V_{CC}	●			±3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–6.5		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			6.5		mA
I_{REF}	Reference Current	CONV = V_{CC} f_{SMPL} = $f_{SMPL(MAX)}$	● ●		0.001 0.01	3 0.1	µA mA
I_{CC}	Supply Current	CONV = V_{CC} After Conversion f_{SMPL} = $f_{SMPL(MAX)}$	● ●		0.5 0.45	10 1.0	µA mA
P_D	Power Dissipation	f_{SMPL} = $f_{SMPL(MAX)}$			1.22		mW

RECOMMENDED OPERATING CONDITIONS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage			2.7		3.6	V
f_{SCK}	Clock Frequency		●	DC		8	MHz
t_{CYC}	Total Cycle Time			12 • SCK + t_{CONV}			µs
t_{SMPL}	Analog Input Sampling Time			12			SCK
t_{suCONV}	Setup Time CONV↓ Before First SCK↑, (See Figure 1)			60			ns
t_{WHCLK}	SCK High Time	f_{SCK} = $f_{SCK(MAX)}$		45%			$1/f_{SCK}$
t_{WLCLK}	SCK Low Time	f_{SCK} = $f_{SCK(MAX)}$		45%			$1/f_{SCK}$
t_{WHCONV}	CONV High Time Between Data Transfer Cycles			t_{CONV}			µs
t_{WLCONV}	CONV Low Time During Data Transfer			12			SCK
t_{hCONV}	Hold Time CONV Low After Last SCK↑			26			ns

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 2.7V, V_{REF} = 2.5V, f_{SCK} = $f_{SCK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{CONV}	Conversion Time (See Figure 1)		●		3.7	4.66	µs
$f_{SMPL(MAX)}$	Maximum Sampling Frequency		●	150			kHz
t_{dDO}	Delay Time, SCK↓ to SDO Data Valid	C_{LOAD} = 20pF	 ●		45	55 60	ns ns
t_{dis}	Delay Time, CONV↑ to SDO Hi-Z		●		55	120	ns
t_{en}	Delay Time, CONV↓to SDO Enabled	C_{LOAD} = 20pF	●		35	120	ns
t_{hDO}	Time Output Data Remains Valid After SCK↓	C_{LOAD} = 20pF	●	5	15		ns
t_r	SDO Rise Time	C_{LOAD} = 20pF			25		ns
t_f	SDO Fall Time	C_{LOAD} = 20pF			12		ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: Integral nonlinearity is defined as deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 4: Channel leakage current is measured while the part is in sample mode.

PIN FUNCTIONS

V_{REF} (Pin 1): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.

IN^+, IN^- (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

CONV (Pin 5): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

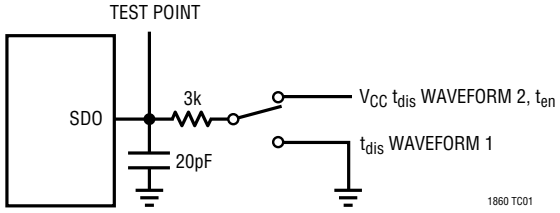
SDO (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this pin.

SCK (Pin 7): Shift Clock Input. This clock synchronizes the serial data transfer.

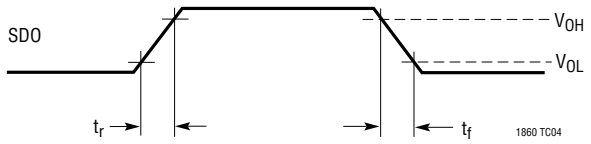
V_{CC} (Pin 8): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

TEST CIRCUITS

Load Circuit for t_{dDO}, t_r, t_f, t_{dis} and t_{en}

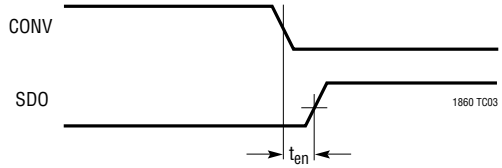


Voltage Waveforms for SDO Rise and Fall Times, t_r, t_f

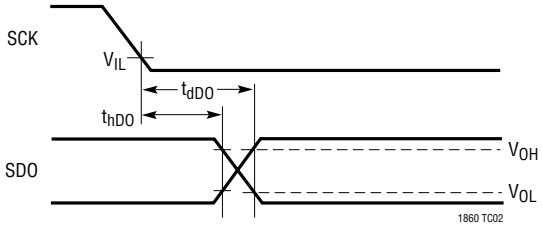


TEST CIRCUITS

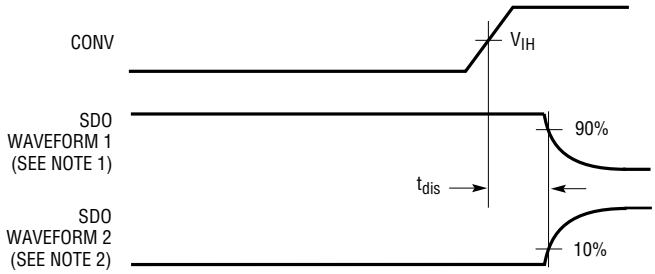
Voltage Waveforms for t_{en}



Voltage Waveforms for SDO Delay Time, t_{dDO}, t_{hDO}



Voltage Waveforms for t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL

1860 TC05

APPLICATIONS INFORMATION

Operating Sequence

The LTC1860L conversion cycle begins with the rising edge of CONV. After a period equal to t_{CONV}, the conversion is finished. If CONV is left high after this time, the LTC1860L goes into sleep mode drawing only leakage current. On the falling edge of CONV, the LTC1860L goes into sample mode and SDO is enabled. SCK synchronizes the data transfer with each bit being transmitted from SDO on the falling SCK edge. The receiving system should capture the data from SDO on the rising edge of SCK. After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely. See Figure 1.

Analog Inputs

The LTC1860L has a unipolar differential analog input. The converter will measure the voltage between the "IN^+" and "IN^-" inputs. A zero code will occur when IN^+ minus IN^- equals zero. Full scale occurs when IN^+ minus IN^- equals V_{REF} minus 1LSB. See Figure 2. Both the "IN^+" and "IN^-" inputs are sampled at the same time, so common mode noise on the inputs is rejected by the ADC. If "IN^-" is grounded and V_{REF} is tied to V_{CC}, a rail-to-rail input span will result on "IN^+" as shown in Figure 3.

Reference Input

The voltage on the reference input of the LTC1860L defines the full-scale range of the A/D converter. This ADC can operate with reference voltages from V_{CC} to 1V.

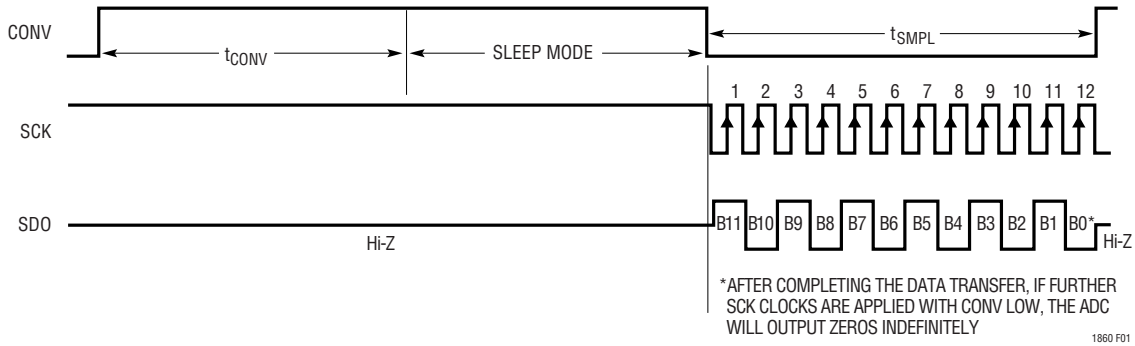


Figure 1. LTC1860L Operating Sequence

APPLICATIONS INFORMATION

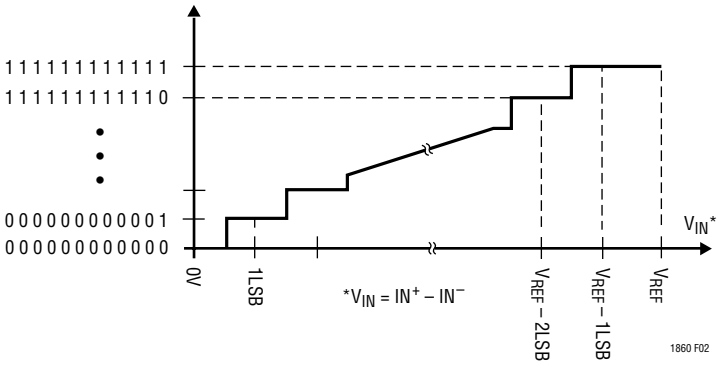


Figure 2. LTC1860L Transfer Curve

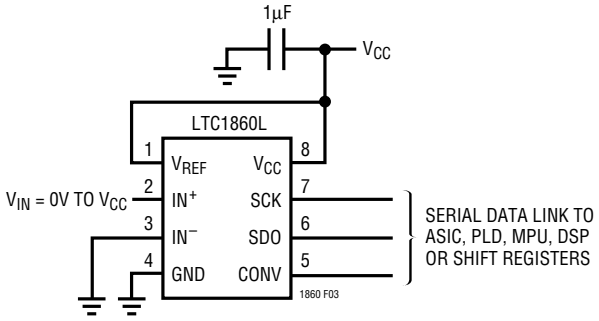


Figure 3. LTC1860L with Rail-to-Rail Input Span

GENERAL ANALOG CONSIDERATIONS

Grounding

The LTC1860L should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance, use a printed circuit board. The ground pin should be tied directly to the analog ground plane with minimum lead length.

Bypassing

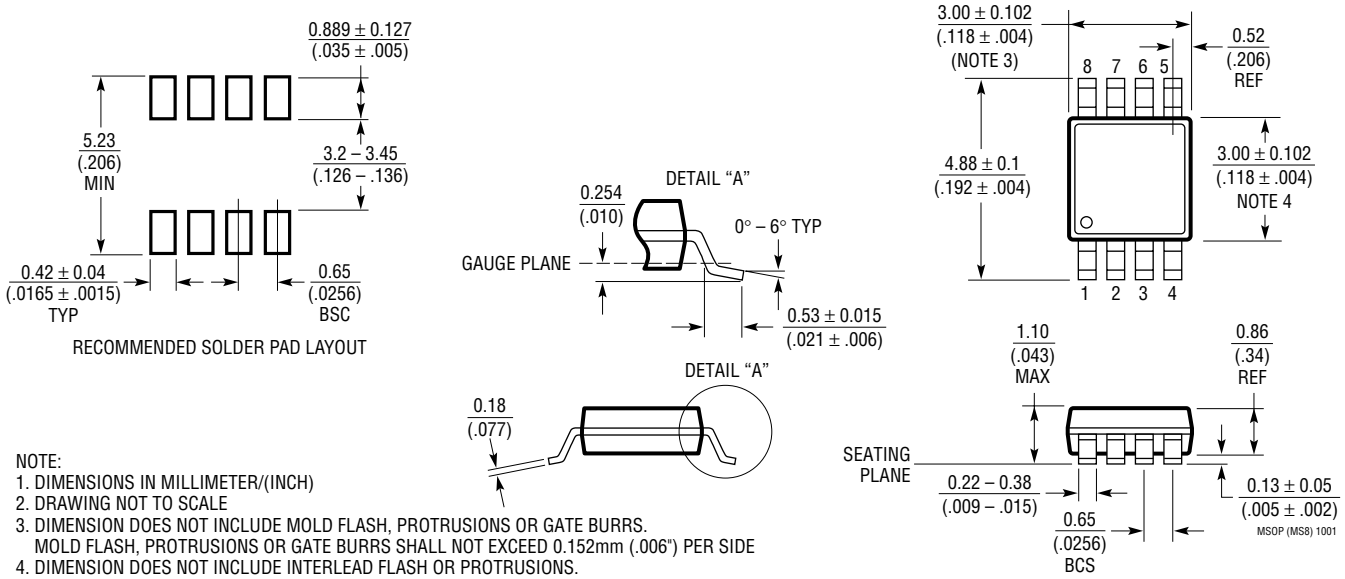
For good performance, the V_{CC} and V_{REF} pins must be free of noise and ripple. Any changes in the V_{CC}/V_{REF} voltage with respect to ground during the conversion cycle can induce errors or noise in the output code. Bypass the V_{CC} and V_{REF} pins directly to the analog ground plane with a minimum of 1µF tantalum. Keep the bypass capacitor leads as short as possible.

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1860L have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem if source resistances are less than 200Ω or high speed op amps are used (e.g., the LT®1211, LT1469, LT1807, LT1810, LT1630, LT1226 or LT1215). But if large source resistances are used, or if slow settling op amps drive the inputs, take care to ensure the transients caused by the current spikes settle completely before the conversion begins.

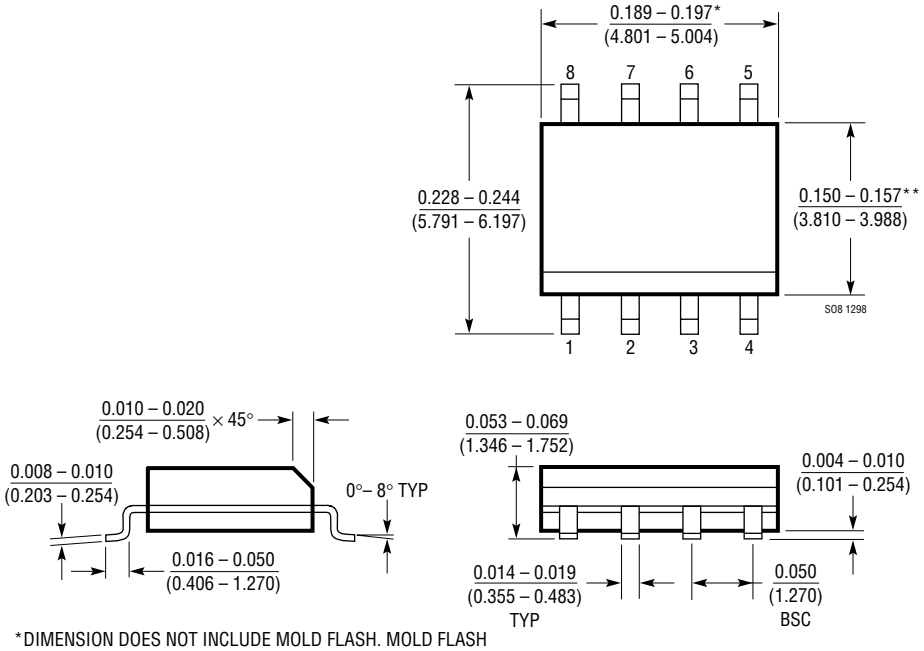
PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	SAMPLE RATE	POWER DISSIPATION	DESCRIPTION
8-Bit Serial I/O ADCs			
LTC1096/LTC1096L	15ksps	0.9mW	1-Channel, Unipolar Operation, 5V/3V
LTC1098/LTC1098L	15ksps	0.6mW	2-Channel, Unipolar Operation, 5V/3V
LTC1196	1Msps	20mW	1-Channel, Unipolar Operation with Reference Input, 5V/3V
LTC1198	750ksps	20mW	2-Channel, Unipolar Operation, 5V/3V
10-Bit Serial I/O ADCs			
LTC1197/LTC1197L	500ksps/250ksps	22.5mW	SO-8, MS8, 1-Channel, 5V/3V
LTC1199/LTC1199L	450ksps/210ksps	25mW	SO-8, MS8, 2-Channel, 5V/3V
12-Bit Serial I/O ADCs			
LTC1286/LTC1298	12.5ksps/11.1ksps	1.3mW/1.7mW	1-Channel with Ref. Input (LTC1286), 2-Channel (LTC1298), 5V
LTC1400	400ksps	75mW	1-Channel, Bipolar or Unipolar Operation, Internal Reference, 5V
LTC1401	200ksps	15mW	SO-8 with Internal Reference, 3V
LTC1402	2.2Msps	90mW	Serial I/O, Bipolar or Unipolar, Internal Reference
LTC1404	600ksps	25mW	SO-8 with Internal Reference, Bipolar or Unipolar, 5V
LTC1860/LTC1861	250ksps	4.25mW	SO-8, MS8, 1-Channel, 5V/SO-8, MS10, 2-Channel, 5V
14-Bit Serial I/O ADCs			
LTC1417	400ksps	20mW	16-Pin SSOP, Unipolar or Bipolar, Reference, 5V
LTC1418	200ksps	15mW	Serial/Parallel I/O, Internal Reference, 5V
16-Bit Serial I/O ADCs			
LTC1609	200ksps	65mW	Configurable Bipolar or Unipolar Input Ranges, 5V
LTC1864/LTC1865	250ksps	4.25mW	SO-8, MS8, 1-Channel, 5V/SO-8, MS10, 2-Channel, 5V
LTC1864L	150ksps	1.22mW	SO-8, MS8, 1-Channel, 3V

PART NUMBER	DESCRIPTION	COMMENTS
References		
LT1460	Micropower Precision Series Reference	Bandgap, 130µA Supply Current, 10ppm/°C, Available in SOT-23
LT1790	Micropower Low Dropout Reference	60µA Supply Current, 10ppm/°C, SOT-23
Op Amps		
LT1468/LT1469	Single/Dual 90MHz, 16-Bit Accurate Op Amps	22V/µs Slew Rate, 75µV/125µV Offset
LT1806/LT1807	Single/Dual 325MHz Low Noise Op Amps	140V/µs Slew Rate, 3.5nV/$\sqrt{Hz}$ Noise, –80dBc Distortion
LT1809/LT1810	Single/Dual 180MHz Low Distortion Op Amps	350V/µs Slew Rate, –90dBc Distortion at 5MHz

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