

Product of the Month

2-Phase DC/DC Converter Powers Mobile Pentium® III Processors and Fits Tightest Space—LTC3716

The LTC3716 is the first 2-phase CPU CORE power supply for Intel's PC Pentium® III Tualatin and Coppermine-T notebook processors. The LTC3716's 2-phase solution occupies the smallest space, has the lowest profile, uses the fewest input and output capacitors and generates minimum heat. The LTC3716 is also compliant with the new Intel Mobile Voltage Positioning specifications (IMVP2). With CPU CORE requirements of 23A and above, single-phase DC/DC converters suffer from poor efficiency. The LTC3716 is the most effective solution in the market, which can easily meet or exceed the power demands of the new high speed processors.

The LTC3716 simplifies the design of the power supply by converting a battery voltage directly to the processor's core voltage, thus eliminating the need for an intermediate voltage (Figure 1). The IC can easily exceed the requirements of all mobile Pentium III processors by handling currents as high as 40A, at output voltages ranging from 0.6V to 1.75V. By comparison, single-phase DC/DC converters can only safely deliver up to 19A. Above this 19A level, value, single-phase DC/DC converters suffer from hot-spot effect and degraded component reliability.

The LTC3716 operates over an input range of 4V to 36V with an output accuracy of ±1%. It is housed in a narrow body 36-lead SSOP package.

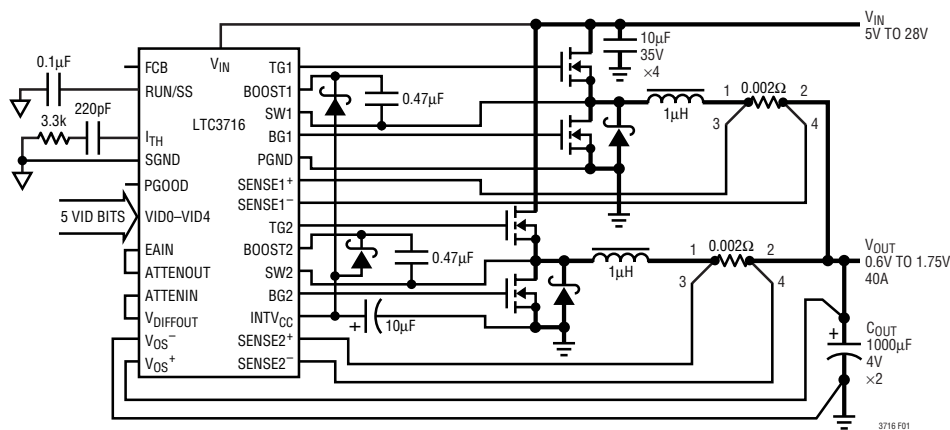


Figure 1. High Current Dual Phase Step-Down Converter

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4.5ns Rail-to-Rail Input and Output Comparator Operates from 2.4V to 12V—LT1711

The LT1711 is the first single comparator that features 4.5ns propagation delay, rail-to-rail inputs, complimentary rail-to-rail CMOS/TTL compatible outputs, with internal data latch and an operating supply range of 2.4V to 12V. The LT1711 is more than just a fast response comparator. Its 2.4V operation, combined with rail-to-rail inputs and CMOS compatible outputs, make it ideal for use in a wide variety of low voltage digital applications, such as clock recovery, or as a line receiver in broadband communications systems. The LT1711's 12V operational capability, high speed and tiny MSOP package makes it equally well-suited for use in automatic test equipment.

With rail-to-rail complimentary outputs that can sink and source 10mA and an output latch with built-in hysteresis, the LT1711 simplifies the design of discrete PWM circuits, current sensing circuits for switching power supplies, bang-bang controllers and a host of other applications.

The LT1711 is available in an 8-pin MSOP package in both commercial and industrial temperature ranges.

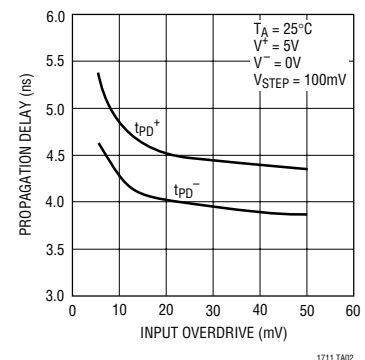


Figure 1. LT1711 Propagation Delay vs Input Overdrive

Single Chip WCDMA Base Station Continuous Time Filter Requires No External Components—LTC1566-1

The LTC1566-1 is a fully differential, 2.3MHz, 7th order (40dB attenuation at 1.5 times the cutoff frequency), linear phase lowpass filter. Designed specifically for WCDMA base station applications, this low noise (62µV in a 2MHz bandwidth), low distortion (SFDR is -71dB for 2.5V_{P-P} differential output) IC, both filters and amplifies (12dB of gain) the receive signal prior to the analog-to-digital conversion.

Housed in an 8-pin SO, this completely self-contained solution requires no external components or clock signal, which

significantly reduces the component count and board area when compared to both filter modules and “roll your own” discrete filter designs.

Unlike discrete solutions that require fists full of components, LTC1566-1 is fully tested and guaranteed prior to placement on

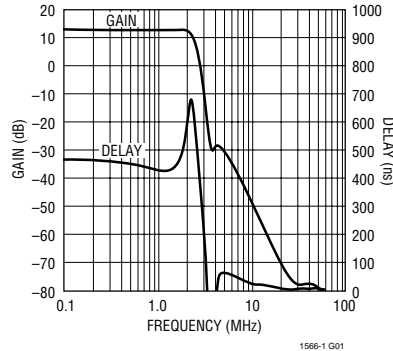


Figure 1. LTC1566-1 Frequency Response

the expensive multilayer PC board. This results in less scrap, less rework and faster throughput at the assembly facility. The 12dB of gain eliminates the need for an external differential high speed amplifier typically required to overcome the insertion loss associated with all high order LC filters. Note that lower than 12dB differential gain can be obtained via three external resistors.

The LTC1566-1 is the only single-chip receive filter capable of meeting the requirements of WCDMA base stations. The unique ability to introduce a programmable differential offset at the output facilitates simple sideband signal suppression and allows easy calibration of the A/D converters. This fully self-contained, WCDMA, surface mount, receive filter solution is available with specifications guaranteed over -40°C to 85°C or 0°C to 70°C temperature ranges.

Program DC/DC Converter Output Voltage via SMBus or I²C Interface—LTC1699

The LTC1699 is a variable resistor divider with ±0.35% accuracy, which is software programmed through a 2-wire SMBus or I²C interface. The LTC1699 provides the flexibility to digitally set the output voltage of a DC/DC converter without modifying the circuit board (Figure 1). The IC simplifies

the implementation of a voltage regulator module (VRM), voltage margining and power supply sequencing for use with CPUs, DSPs, FPGA and ASICs in applications such as portable computers, servers and telecom systems.

Two digital codes may be written and stored into the LTC1699 registers via an SMBus or I²C interface. A code is chosen to set the output voltage of a 0.8V referenced DC/D/C converter using the digital SEL pin. The LTC1699 incorporates special write-protect safeguards that prevent

misprogramming of the output voltage due to bus conflicts or errors. A power good output is provided.

The LTC1699 is offered in three versions and in two package options. The LTC1699-80 is fully compliant to mobile CPU voltage codes, the LTC1699-81 is for desktop CPU and the LTC1699-82 is for the new Intel VRM9.0. The 16-lead SSOP can turn on/off a total of three DC/DC converters compared to the 8-lead MSOP version, which controls only one DC/DC converter.

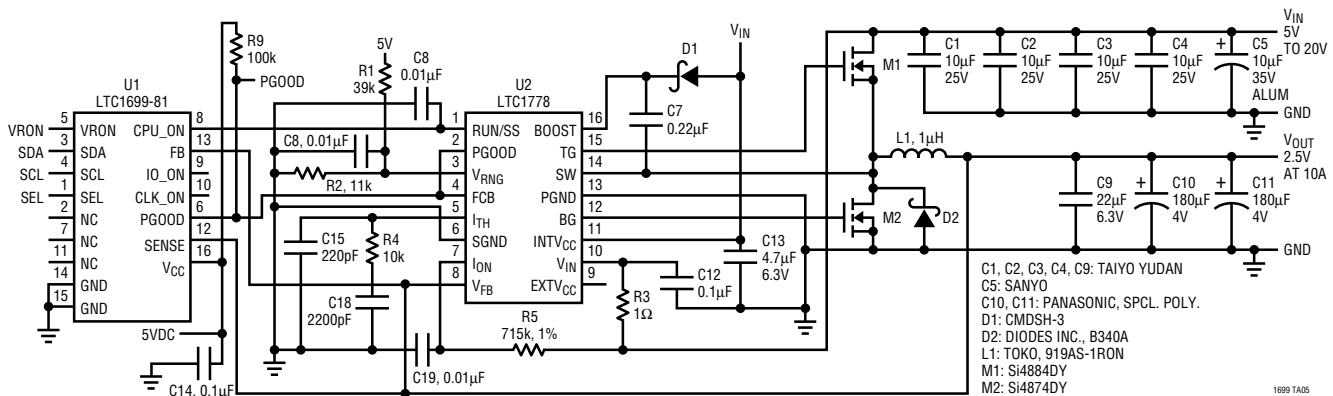


Figure 1. SMBus Controlled High Efficiency DC/DC Converter

Application of the Month

Infinite Sample-and-Hold Based on LTC1417 Outperforms Many Legacy Sample-and-Hold Amplifiers

Few sample-and-hold amplifiers are available today. An ADC followed by a DAC can provide this function while producing characteristics not possible with a conventional sample-and-hold. The circuit shown in Figure 1 is a simple and compact implementation of a topology referred to as an "infinite sample-and-hold." It will hold until the power is turned off or until a new sample is required. Formed from an ADC feeding a DAC, the sample is held as a digital code in the registers of the DAC. The overall accuracy is better in most aspects than many of the integrated sample-and-hold amplifiers.


The sample-and-hold in Figure 1 uses an **LTC1417** serial 14-bit ADC with an **LTC1658** serial 14-bit DAC. The short acquisition time of the ADC, coupled with

external trigger circuitry, can produce a variety of useful functions, such as peak detection, phase measurement schemes, capacitance measurement or time division multiplexing, all without processor intervention. The advantages of a scheme that does not require a processor are low power, cost and possibly a higher sample rate.

The serial output from the **LTC1417** is passed directly to the **LTC1658**. The **LT1077** buffers the 2.5V output and provides a gain of 1.634 to produce the appropriate 4.096V reference for the **LTC1658**. If the output section is located at a distance or across a potential barrier, it needs a separate 4.096V reference at the **LTC1658**.

The **LTC1417** is used in "internal conversion clock mode," where conversion and

data transfer occur simultaneously. Thus there is a one-conversion delay between the data sampled and the data output. If the waveform is sampled infrequently and an update is required as soon as possible, a first conversion must be performed at the time of the required sample, followed by a dummy conversion to transfer the data.

The use of a field-programmable gate array (FPGA) between the ADC and DAC allows the digital data to be modified prior to sending it to the DAC. If parallel I/O converters are used, some simple and useful operations, such as conversion of signed to absolute valued data, are possible even with a programmable-array device. (Linear Technology magazine, November 2000.) 

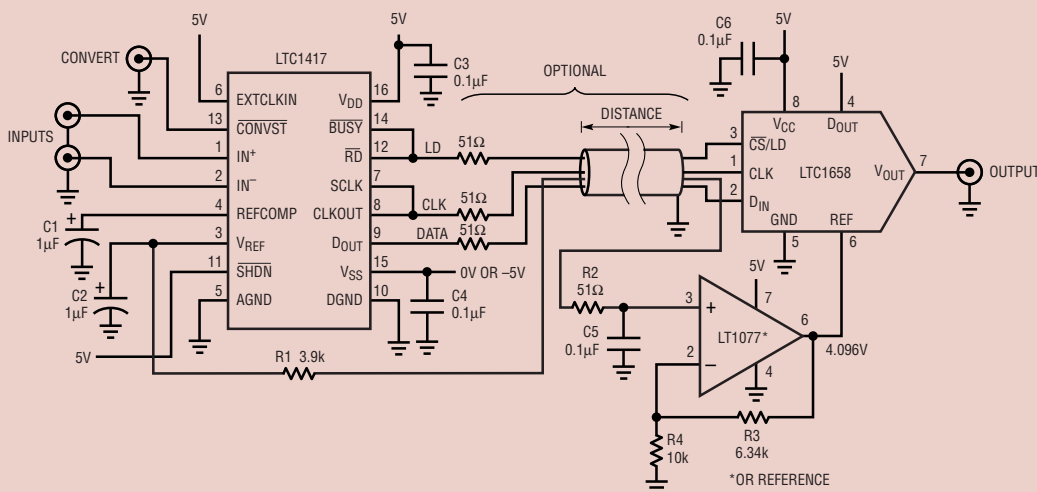


Figure 1. ADC Plus DAC Create an Infinite Sample-and-Hold Circuit

Precision RF Power Controllers for Dual Band GSM Cellular Phones Minimize Test Time—LTC1758/LTC1957

The **LTC1758/LTC1957** are precision RF power controllers for single- and dual-band GSM/PCS cellular phones. With excellent temperature stability and offset error cancellation, these ICs minimize a cell phone's production test time by allowing a single calibration at room temperature. This means cost savings on test time and expenses associated with testing and

calibrating phones. Both parts operate directly from single-cell Li-Ion battery and support a wide range of RF power amplifiers from various manufacturers. Applications include single- and dual-band GSM phones, PCS devices, wireless data modems and TDMA cellular phones.

The **LTC1758/LTC1957** feature an autozero loop, which cancels initial offsets

and temperature dependent offset errors, allowing accurate low power programming of the RF power amplifier. It minimizes production test time by allowing fewer calibration points. It also provides excellent temperature stability across a broad range of output power, which is difficult to achieve with a more conventional approach. Both

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