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COVER ARTICLE

DESIGN FEATURES

DESIGN IDEAS

12-Bit, 1.25Msps ADC with 8-Channel Programmable MUX Offers Incredible Versatility

by Dave Thomas

Close Your Eyes, Make a Wish

Think about everything you have ever wanted from a multiplexed ADC: plenty of channels with a fast per-channel throughput rate; single-ended or differential inputs, or both; unipolar and bipolar input spans; multiple input ranges. Take all of that, throw in the ability to reconfigure on the fly, automatically scan through all of the channels or program and run a sequence of up to sixteen addresses and configurations and you are only beginning to understand the power of the new LTC1851. If you are tired of adapting your inputs to fit your ADC, Linear Technology offers an ADC that can adapt to your inputs.

The LTC1851 has an 8-channel input multiplexer, a programmable sample-and-hold and an internal

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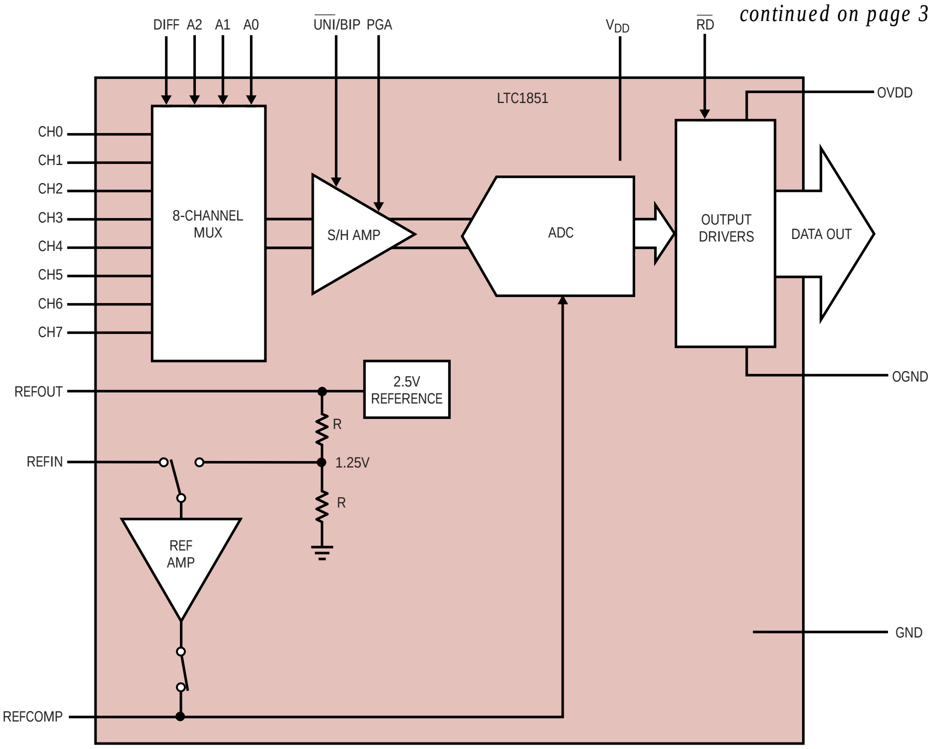


Figure 1. Simplified block diagram shows programmable MUX, sample-and-hold and 3-pin reference interface.

Issue Highlights

Our cover article in this issue introduces the new LTC1851, which features everything you have ever wanted from a multiplexed ADC: plenty of channels with a fast per-channel throughput rate; single-ended or differential inputs, or both; unipolar and bipolar input spans; multiple input ranges. Take all of that, throw in the ability to reconfigure on the fly, automatically scan through all of the channels or program and run a sequence of up to sixteen addresses and configurations and you are only beginning to understand the power of the new LTC1851.

Several other exciting products debut in this issue, including one of the most versatile amplifiers on the market today. The 80 MHz LT1800 amplifier consumes a mere 2mA max supply current and still provides both the speed and DC accuracy required by low voltage signal conditioning and data acquisition systems. Usually, one cannot have both high bandwidth and low supply-current in an amplifier, but the LT1800 optimizes both through a 6GHz f_T process and by running the transistors at reduced quiescent currents. It can operate from supplies as low as 2.5V, and the entire supply range is available because of the device's rail-to-rail inputs and outputs. The DC performance is exceptional, with a maximum offset voltage of 350µV. This comes from trimming the input offset voltage, and canceling the input bias currents, where the maximum input bias current is 250nA. The device is available in commercial and industrial temperature grades, in both SOIC and SOT-23 packages, making for a tiny and versatile amplifier.

Several new power products are also featured in this issue. The LTC1960 Dual Battery Power Manager solves many of the design problems inherent in parallel battery systems by including many desired features within a monolithic device and greatly simplifying the control interface. The results are a simple way to increase battery run time and significantly decrease charge time for dual battery systems.

The LTC1644 and LTC1646 Hot Swap™ controllers safely limit the currents drawn by bypass capacitors when a circuit board is inserted into a hot backplane. They also offer several features specifically tailored for CompactPCI™ (CPCI) Hot Swap applications:

The LT1964 negative low dropout regulator is capable of providing 200mA of output current at 340mV of dropout, while drawing only 30µA of quiescent current, dropping to 3µA in shutdown. Its small size and ability to work with small, low cost components facilitate portable power supply design. A bidirectional logic shutdown pin allows easy interfacing with existing positive regulators without adding extra external components.

The new LTC1911 Step-Down DC/DC converter helps designers produce tiny conversion circuits while maintaining the high efficiencies needed to extend battery life. The LTC1911 saves space by operating at high frequency, allowing the use of tiny low cost ceramic capacitors—no inductors required. The LTC1911 also comes in a low profile (1.1mm) MSOP-8 package. A complete converter can take less than 0.08in^2 of board space. Its small size and efficiency make it well suited for single cell Li-Ion as well as 3-cell NiMH/NiCd battery powered applications.

Our Design Ideas section features five simple circuit ideas, including: an efficient circuit for a triple voltage supply geared towards small TFT LCDs, a circuit that satisfies the low noise bias supply needs of avalanche photo diodes (APDs), a way to reduce the power consumption of DSL modems using the LT1969 line driver, a 2-step voltage converter that reduces power supply size and heat dissipation—perfect for notebook computers, and finally, an I^{2}C dual fan speed controller that increases fan efficiency and lifetime and reduces noise—important in rack based servers and telecom systems.

At the back are four New Device Cameos. Visit www.linear.com for complete device specifications.

LTC in the News...

On October 16, Linear Technology Corporation announced its financial results for the 1st quarter of fiscal year 2002. Robert H. Swanson, Chairman of the Board and CEO stated, "These have been difficult times for technology companies. As we had forecasted, sales declined from the previous quarter by 40%. Although our bookings improved, they were still less than our billings and, consequently, we further reduced backlog. However, we continue to be strongly profitable, even with reduced sales, as demonstrated by our 38% return on sales. We incurred charges for severance costs associated with a modest reduction in workforce of approximately $900,000 and we donated $500,000 to assist those people in New York impacted by the September 11 attack. Although we had a reduction in workforce, we are still staffed and building product in anticipation of improved demand. However, much of the incremental inventory our current workforce has produced has been expensed.

Looking forward, we have recently seen some modest improvement in our booking activity across all of our major end markets. However, our backlog is low and global economic conditions are tenuous given the ongoing political events. Therefore, confidently and accurately forecasting future results is more difficult. Consequently, while we anticipate improved bookings, we expect sales and profits in the December quarter to be similar to those just achieved."

The Company reported net sales of $120,104,000 and net income of $45,150,000 for the quarter ended September 30, 2001. Diluted earnings were $0.14 per share.

CompactPCI is a trademark of the PCI Industrial Computer Manufacturers Group.

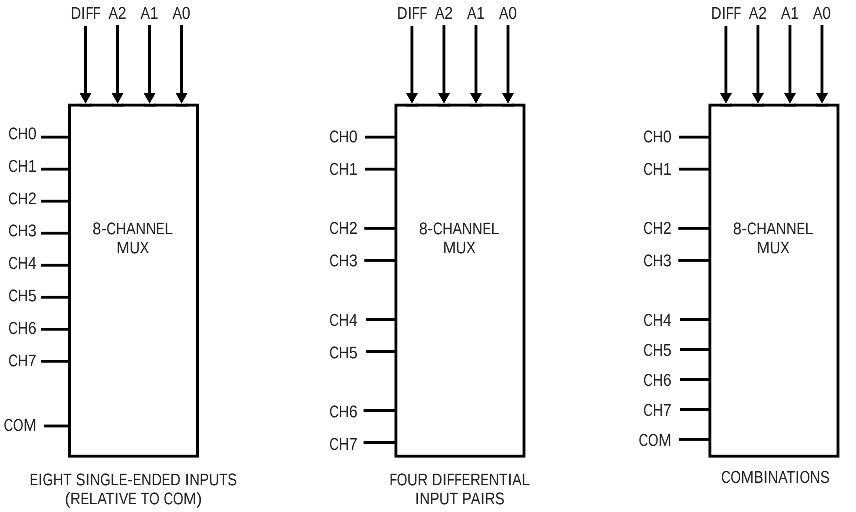


Figure 2. Input multiplexer handles single-ended or differential inputs or combinations.

LTC1851, continued from page 1

reference. The 12-bit, 1.25Msps ADC runs off of a single 5V supply, drawing only 25mW. The part has NAP and SLEEP shutdown modes and good DC and AC specs. Figure 1 is a simplified diagram of the signal path of the LTC1851, showing the individual blocks and control signals. The LTC1851 uses six configuration control bits (DIFF, A2, A1, A0, $\overline{\text{UNI}}$/BIP and PGA) and three operational modes to provide unprecedented flexibility to fit your application.

Input Multiplexer Handles Single-Ended or Differential Inputs

What kind of signals do you need to convert—single-ended? No problem. The LTC1851 can be configured for eight single-ended inputs, each relative to a common pin (COM). The COM pin can be connected to ground or used to offset the negative input. Differential? Again, no problem. The eight channels of the LTC1851 can be configured as four differential pairs (Channel 0 and Channel 1, Channel 2 and Channel 3 and so on). Choosing between the two modes is as easy as connecting the DIFF pin to ground or to the supply. In addition, the DIFF bit can be changed between conversions, even when the LTC1851 is running at the full conversion rate, effectively reconfiguring the MUX with every conversion. Figure 2 illustrates the possibilities. With DIFF tied low you get eight single-ended inputs. With DIFF tied high you get four differential pairs. Changing the DIFF bit with the MUX Address for each conversion can provide any desired combination of single-ended and differential inputs.

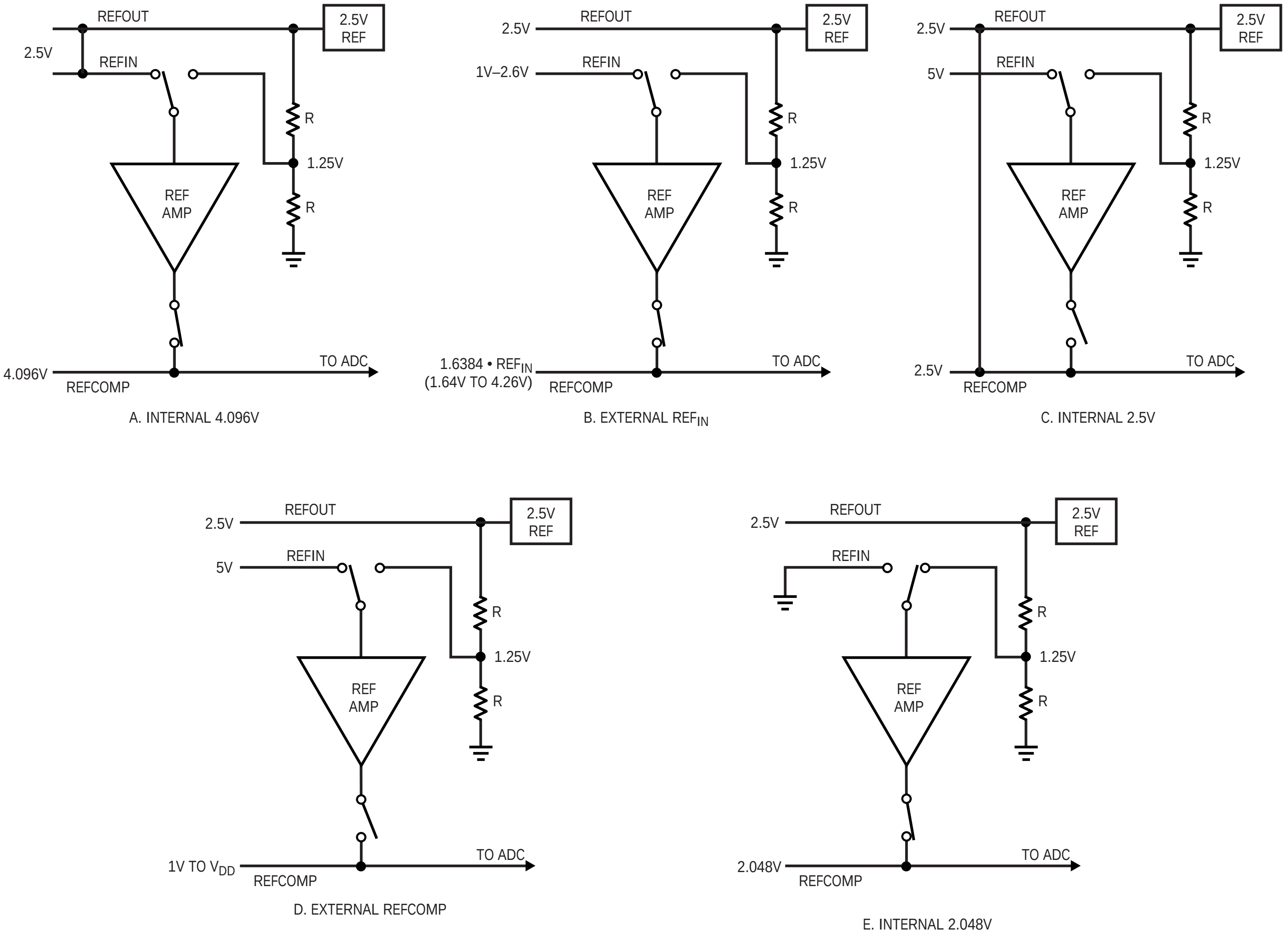
The MUX Address Inputs (A2, A1, A0) select the “positive” input. In the single-ended case, the COM pin will always be the “negative” input. In the differential case, the “negative” input will be the other input of the pair. Note that this method allows either input of a differential pair to be the “positive” input, allowing the user to choose the polarity. Table 1 summarizes the MUX Address Input selection. Regardless of the configuration of the Input MUX, the inputs to the ADC are always truly differential, meaning that both inputs are sampled simultaneously. Any noise or signal that is common to both inputs will be rejected.

Programmable Sample-and-Hold and Reference Provide Multiple Input Ranges

The flexibility of the LTC1851 is also apparent in its wide selection of input ranges. The sample-and-hold gives you the option of unipolar or bipolar inputs and a choice of two gains, and is completely programmable. The reference, although not programmable in the strictest sense, offers three pin-strappable options using the internal reference and two options for using an external reference. Together, the sample-and-hold and reference provide a choice of ten different input ranges using the internal reference (unipolar ranges of 0V–1.024V,

Table 1. Input MUX address selection

MUX Address				Single-Ended Channel Selection								
DIFF	A2	A1	A0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	0	+								–
0	0	0	1		+							–
0	0	1	0			+						–
0	0	1	1				+					–
0	1	0	0					+				–
0	1	0	1						+			–
0	1	1	0							+		–
0	1	1	1								+	–
MUX Address				**Differential Channel Selection**								
DIFF	**A2**	**A1**	**A0**	**CH0**	**CH1**	**CH2**	**CH3**	**CH4**	**CH5**	**CH6**	**CH7**	**COM**
1	0	0	0	+	–							
1	0	0	1	–	+							
1	0	1	0			+	–					
1	0	1	1			–	+					
1	1	0	0					+	–			
1	1	0	1					–	+			
1	1	1	0							+	–	
1	1	1	1							–	+	



A. INTERNAL 4.096V

B. EXTERNAL REF$_{IN}$

C. INTERNAL 2.5V

D. EXTERNAL REFCOMP

E. INTERNAL 2.048V

Figure 3. Reference options: A. internal reference using reference amplifier; B. external reference using reference amplifier; C. internal reference bypassing reference amplifier; D. external reference bypassing reference amplifier; E. one-half of internal reference using reference amplifier

0V–1.25V, 0V–2.048V, 0V–2.5V and 0V–4.096V, and bipolar ranges of ±0.512V, ±0.625V, ±1.024V, ±1.25V and ±2.048V) and virtually unlimited ranges using an external reference. The input range is set by programming the sample-and-hold to determine the input span relative to the full-scale reference (REFCOMP) and then configuring the reference to determine REFCOMP.

Programming the Sample-and-Hold for Unipolar/Bipolar Mode and Gain

The sample-and-hold of the LTC1851 lets you choose either a unipolar or bipolar input and a gain of one or two. When $\overline{\text{UNI}}$/BIP is low, a unipolar input range of 0 – SPAN is selected. When $\overline{\text{UNI}}$/BIP is high, a bipolar input range of ±SPAN/2 is selected. It should be noted that in bipolar mode the inputs must always be between the supply rails and are not allowed to be above V_{DD} or below ground. The “negative” input should be connected to a common mode voltage (typically mid-supply or midreference) and the “positive” input swings ±SPAN/2 around the common mode voltage. The PGA bit selects the gain of the sample-and-hold and determines how the input SPAN relates to REFCOMP. If PGA is held high, the SPAN will be equal to REFCOMP (gain of one). If PGA is held low, the SPAN will be equal to REFCOMP/2 (gain of two). With two bits of control the user can select one of four input ranges relative to REFCOMP: 0–REFCOMP, ± REFCOMP/2, 0–REFCOMP/2, and ±REFCOMP/4. Table 2 illustrates the input range options of the LTC1851. It is important to remember that, just like the input MUX, the state of the sample-and-hold can be changed between conversions while the LTC1851 is running at the full conversion rate of 1.25Msps.

Table 2. Input range selection

			REFCOMP = 4.096V	
	PGA = 0	**PGA = 1**	**PGA = 0**	**PGA =1**
$\overline{\text{UNI}}$/BIP = 0	0V–REFCOMP/2	0V–REFCOMP	0V–2.048V	0V–4.096V
$\overline{\text{UNI}}$/BIP = 1	±REFCOMP/4	±REFCOMP/2	±1.024V	±2.048V

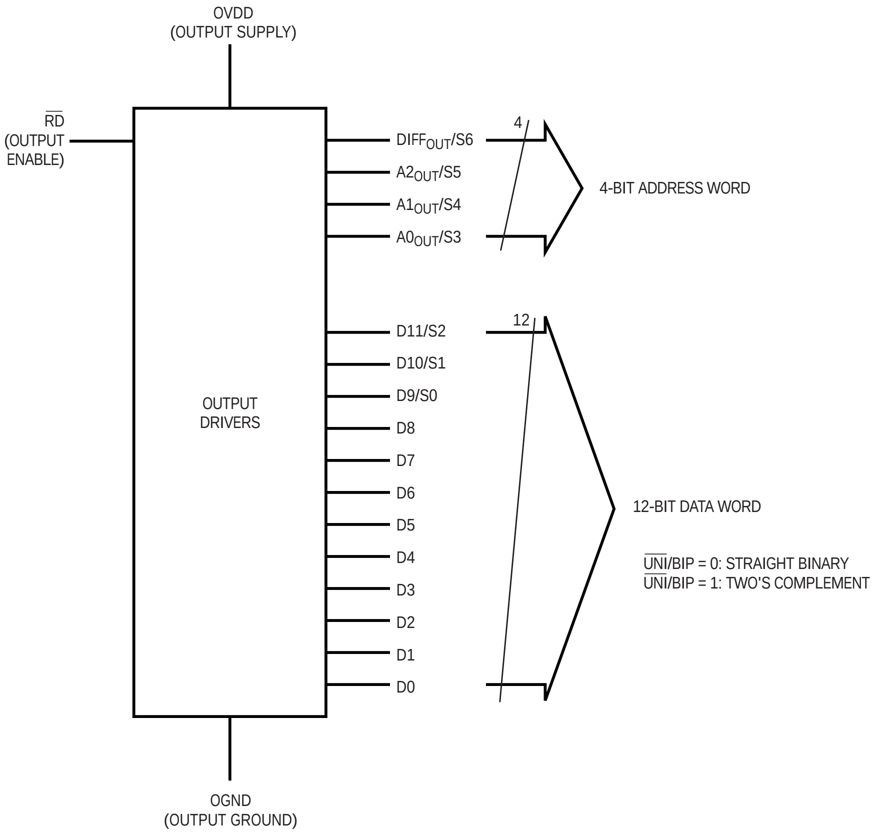


Figure 4. Output word automatically includes address and data-format switches.

Setting the Full-Scale Reference

The last piece of the puzzle concerning the input range is to set the full-scale reference, which is set by the voltage that appears on the REFCOMP pin. Again, the LTC1851 gives the user a number of choices. The LTC1851 offers three pin-strappable options for REFCOMP as well as two additional options for using an external reference or DAC. The onboard reference of the LTC1851 consists of a 2.5V reference and a reference buffer with an accurately trimmed gain of 1.6384 (see Figure 1). The REFOUT pin is the output of the 2.5V reference, the REFIN pin is the input to the reference buffer and also acts as a control pin to select the reference buffer mode and the REFCOMP pin is the output of the reference buffer.

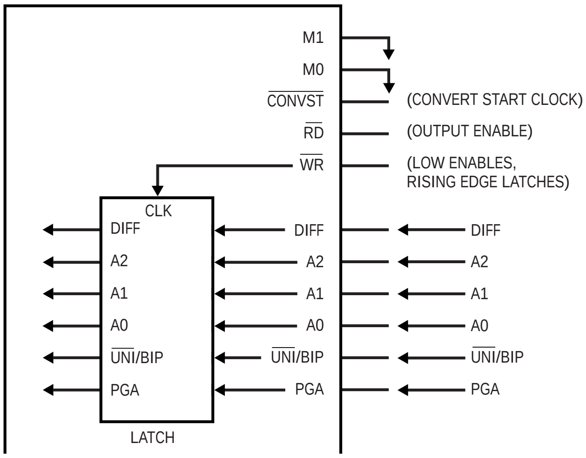


Figure 5. Direct address mode

If REFIN is driven with a voltage of 1V to 2.6V, the reference buffer will produce a voltage of 1.6384 • REFIN on the REFCOMP pin. REFIN can be connected to REFOUT to produce a REFCOMP voltage of 4.096V using the internal reference or REFIN can be driven by an external reference or DAC. If REFIN is held high, the reference buffer will be disabled and REFCOMP can be driven directly. In this mode, REFCOMP can be connected to REFOUT to produce a 2.5V range using the internal reference or REFCOMP can be driven by an external reference or DAC. Finally, if REFIN is held low, the input to the reference buffer is switched to a voltage representing REFOUT/2. This produces a voltage on REFCOMP of 2.048V using the internal reference. Figure 3 summarizes the five reference modes.

The LTC1851's internal reference, reference buffer and the gain and full scale of the input are all trimmed independently. This method ensures accuracy regardless of the reference configuration.

Output Word Automatically Includes Address and Data Format Switches

At the end of every conversion, the LTC1851 outputs a 16-bit parallel word that includes the 12-bit data word (D11–D0) and the 4-bit MUX Address (DIFF out, A2 out, A1 out, A0 out). This provides the user with the conversion result as well as the configuration (single-ended or differential) and address of the inputs that were sampled to obtain it (see Figure 4). The 12-bit data word automatically changes format depending on the status of the $\overline{\text{UNI}}$/BIP bit when the conversion starts. If the $\overline{\text{UNI}}$/BIP bit was low at the start of the conversion, indicating a unipolar input, the format of the 12-bit data word will be straight binary. If the $\overline{\text{UNI}}$/BIP bit was high, indicating a bipolar input, the format of the 12-bit data word will be two's complement. During a normal conversion cycle $\overline{\text{RD}}$ acts as an output enable control. The sixteen outputs are enabled when $\overline{\text{RD}}$ is low and are high impedance when $\overline{\text{RD}}$ is

Table 3. Output data format

Unipolar Mode ($\overline{\text{UNI}}$/BIP = 0)			
Output Code	Input Voltage		
		REFCOMP = 4.096V	
		PGA = 0 V_{FS} = 2.048V	PGA = 1 V_{FS} = 4.096V
1111 1111 1111	V_{FS} – 1LSB	2.0475V	4.095V
1111 1111 1110	V_{FS} – 2LSB	2.047V	4.094V
1000 0000 0001	(V_{FS}/2) + 1LSB	1.0245V	2.049V
1000 0000 0000	V_{FS}/2	1.024V	2.048V
0111 1111 1111	(V_{FS}/2) – 1LSB	1.0235V	2.047V
0111 1111 1110	(V_{FS}/2) – 2LSB	1.023V	2.046V
0000 0000 0001	1LSB	0.0005V	0.001V
0000 0000 0000	0	0V	0V

Bipolar Mode ($\overline{\text{UNI}}$/BIP = 1)			
Output Code	Input Voltage		
		REFCOMP = 4.096V	
		PGA = 0 V_{FS} = 1.024V	PGA = 1 V_{FS} = 2.048V
0111 1111 1111	V_{FS} – 1LSB	1.0235V	2.047V
0111 1111 1110	V_{FS} – 2LSB	1.023V	2.046V
0000 0000 0001	1LSB	0.0005V	0.001V
0000 0000 0000	0	0V	0V
1111 1111 1111	–1LSB	–0.0005V	–0.001V
1111 1111 1110	–2LSB	–0.001V	–0.002V
1000 0000 0001	–V_{FS} + 1LSB	–1.0235V	–2.047V
1000 0000 0000	–V_{FS}	–1.024V	–2.048V

high. All sixteen outputs and $\overline{\text{BUSY}}$ run off of the separate OV_{DD} and OGND supplies to make it easy to interface to 3V logic. Table 3 summarizes the output data format.

Manual, Semiautomatic and Fully Automatic Operation

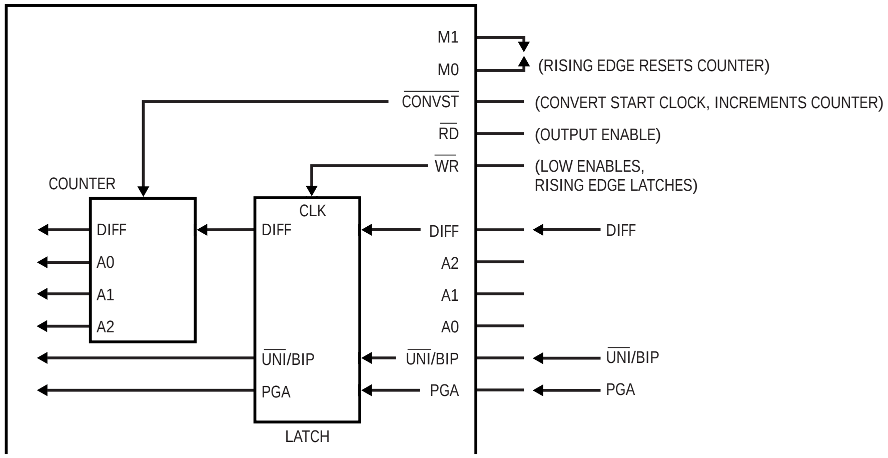
The best thing about the flexibility of the LTC1851 is that you can choose how much of it you want to use. It is easy to use in the simplest applications but has enough power to handle almost anything you can throw at it. The LTC1851 accomplishes this by offering three distinct operating modes that correspond roughly to manual, semiautomatic and automatic.

Manually Set It and Forget It, or Reconfigure It for Every Conversion

Sometimes a MUX doesn't need to be fancy and superprogrammable, it just needs to be a MUX. In Direct Address Mode (see Figure 5) it is very easy to set the LTC1851 up as an 8 × 1 or 4 × 2 MUX with a single input range for all channels. The DIFF, $\overline{\text{UNI}}$/BIP and PGA pins can be tied high or low so all that is needed is to send an address on the A2, A1, and A0 input pins to select the channel to convert. The rising edge of $\overline{\text{WR}}$ can be used to latch the data on these six pins or $\overline{\text{WR}}$ can be tied low to leave the pins always enabled (in which case the falling edge of $\overline{\text{CONVST}}$ will latch the data until the end of the conversion). If your application is a little more demanding, you can still take advantage of the programmability of the LTC1851 in Direct Address Mode by driving the DIFF, $\overline{\text{UNI}}$/BIP and PGA pins in addition to the Address Input pins. In fact, you can change all six Configuration Control bits (DIFF, A2, A1, A0, $\overline{\text{UNI}}$/BIP and PGA) between conversions at the full conversion rate of 1.25Msps. Again, $\overline{\text{WR}}$ functions as an input enable pin, enabling the six configuration control pins when low and latching on the rising edge.

Scan All Channels Semiautomatically

It is very common to have several sensors connected to a MUX and an ADC that repeatedly converts each channel in succession. The MUX address must be updated for each conversion normally requiring a processor or an external counter to keep track of and increment the address. The LTC1851 Scan Mode (see Figure 6) solves this problem by handling the addressing so that all that is needed is a stream of $\overline{\text{CONVST}}$ pulses. The DIFF, $\overline{\text{UNI}}$/BIP and PGA pins function the same way they do in the Direct Address mode (enabled when $\overline{\text{WR}}$ is low and latched on the rising edge of $\overline{\text{WR}}$) but the Address pins are ignored. Instead, the LTC1851 uses an internal counter to provide the MUX Address. It starts at address 000 (reset to 000 on either edge of M0) and steps through each channel. The counter is smart enough to adjust the step size depending on the state of the DIFF pin. If the DIFF pin is low, it will step the address by one through eight single-ended channels (CH0–COM, CH1–COM, CH2–COM, CH3–COM, … CH7–COM, repeat). The throughput rate for each channel is 1.25Msps/8 or 156.25kHz. If the DIFF pin is high, it will step the address by two to scan through the four differential pairs (CH0–CH1, CH2–CH3, CH4–CH5, CH6–CH7, repeat). In this case, the throughput rate for each differential pair is 1.25Msps/4 or 312.5kHz. It is also possible to vary the internal counter step size by changing the



DIFF = 0: CH0, CH1, CH2, CH3, CH4, CH5, CH6, CH7 8 SINGLE-ENDED PAIRS RELATIVE TO COM
DIFF = 1: CH0–CH1, CH2–CH3, CH4–CH5, CH6–CH7 4 DIFFERENTIAL PAIRS
DIFF = A0$_{\text{OUT}}$: CH0, CH1, CH2–CH3, CH4, CH5, CH6–CH7 4 SINGLE-ENDED, 2 DIFFERENTIAL PAIRS

Figure 6. Scan mode

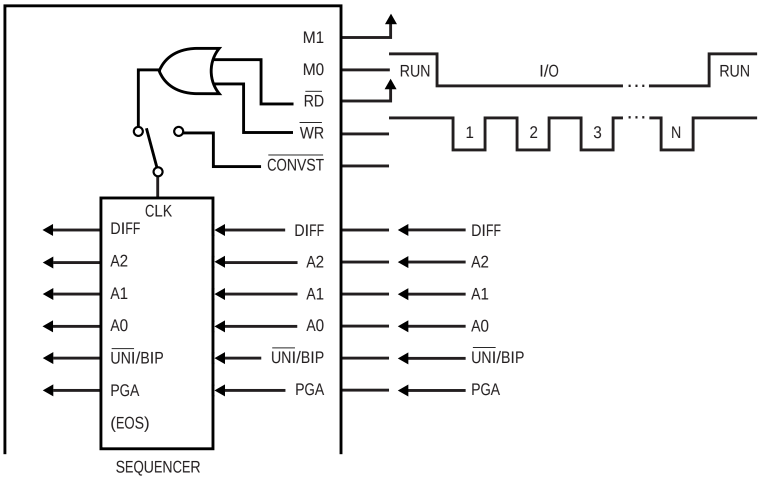
state of the DIFF pin between conversions. For example, if the A0 output is connected to DIFF, the LTC1851 will sequentially convert the following pattern of four single-ended inputs and two differential pairs: CH0–COM, CH1–COM, CH2–CH3, CH4–COM, CH5–COM, CH6–CH7, repeat. Remember that $\overline{\text{WR}}$ must be held or clocked low for changes on the DIFF pin to be recognized. An added bonus is that the 4-bit MUX address is available with each conversion result as part of the 16-bit data output word. This provides a foolproof way to synchronize a conversion result with the input channel (or channels) it represents.

Fully Automatic Programmable Sequencer Solves the Toughest Problems

Now let's look at two problems where the power of the LTC1851 really begins to shine. First, let's imagine the following set of inputs that we would like to scan continuously: Input A has a range of 0V–4.096V, input B has a range of 0V–2.048V, input C has a range of ±2.048V that swings around 2.5V, input D has a range of ±1.024V and is truly differential with a common mode of 2V (each input swings between 1.488V and 2.512V) and input E has a range of 1V–3.048V. We could use the Direct Address Mode but it's going to require that we send an address and configuration for each conversion, over and over again. We could use the Scan Mode to handle the addressing but it doesn't fit any of the obvious scan patterns and we're still going to have to use processing power to drive the $\overline{\text{UNI}}$/BIP and PGA pins to switch the sample-and-hold.

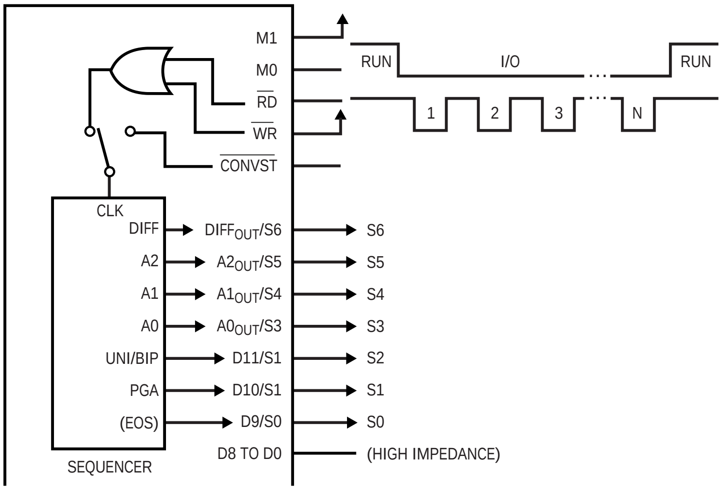
The second problem is extremely common. Let's say we have eight single-ended channels to convert but one of the channels needs to be sampled much faster (for example, 500kHz) than the other seven (for example, 50kHz). Again, we could use the Direct Address Mode but we have to send the same pattern of addresses over and over again, or we could use the Scan Mode but that divides the throughput evenly among the eight channels, limiting each channel to 156.25kHz—not fast enough for the fast channel.

The answer to both of these problems is the LTC1851 Sequencer Mode. In this mode, all control of the six configuration control bits is relinquished to a programmable sequencer. The sequencer has a memory of sixteen locations that allows the user to program a repeating pattern of up to sixteen steps, where each step is an independent MUX address and configuration. This is useful for configuring the MUX for any combination of single-ended and/or differential inputs, unipolar and/or bipolar inputs and two gains. In the first problem, the LTC1851 can be easily programmed to run a five-step sequence to read all five of these sensors sequentially and automatically. The first step reads Channel 0, single-ended, unipolar, with a gain of one to get a 0V–4.096V range for input A. The second step switches to Channel 1 and a gain of two to get a 0V–2.048V range for input B. The third step switches back to a gain of one, switches the MUX to differential, switches the sample-and-hold to bipolar and converts Channel 2–Channel 3 with the input C connected to Channel 2 and Channel 3 connected to 2.5V. The fourth step switches to a gain of two using Channels 4 and 5 as a differential pair (input D). The fifth and last step uses Channels 6 and 7 differential, unipolar, gain of two with the input E



RISING EDGE OF $\overline{\text{WR}}$ LATCHES DATA INTO THE SEQUENCER AND INCREMENTS THE POINTER

Figure 7. Writing to the sequencer



FALLING EDGE OF $\overline{\text{RD}}$ ENABLES DATA OUTPUTS; RISING EDGE DISABLES OUTPUTS AND INCREMENTS THE POINTER

Figure 8. Reading the sequencer

connected to Channel 6 and Channel 7 connected to 1V. The LTC1851 then cycles through these addresses and configurations, each with a throughput of 1.25Msps/5 or 250kHz, with nothing more than a series of $\overline{\text{CONVST}}$ pulses.

The second problem is just as easily solved by the sequencer's ability to program an arbitrary pattern of addresses, allowing the user to allocate the throughput per channel as needed. A throughput of 625kHz on Channel 0 and throughputs of 89.28kHz on Channels 1–7 can easily be achieved by programming a pattern of CH0, CH1, CH0, CH2, CH0, CH3, CH0, CH4, CH0, CH5, CH0, CH6, CH0, CH7, repeat. Again, the LTC1851 will run this pattern with just a series of $\overline{\text{CONVST}}$ pulses and will provide channel identity with each conversion result.

Writing to the Sequencer

How is the sequencer used? First, it is necessary to store the sequence of conversions the LTC1851 is to perform. To write to the sequencer, the $\overline{\text{RD}}$ pin must be held high, the M0 pin taken low and $\overline{\text{WR}}$ taken low (see Figure 7). The first falling edge of $\overline{\text{WR}}$ enables the Configuration Control inputs (DIFF, A2, A1, A0, UNI/$\overline{\text{BIP}}$ and PGA). The rising edge of $\overline{\text{WR}}$ latches the current state of those pins into the sequencer location 0000 and advances the pointer to the next location. Subsequent $\overline{\text{WR}}$ low pulses will continue to write up to sixteen locations. After the last desired location is written, M0 should be taken high and the sequence is ready to run beginning at location 0000.

Reading the Sequencer

In many applications, it is important to confirm the integrity of the programmed sequence before beginning conversions or before resuming conversions after a potentially disruptive event. The LTC1851 allows the user to read back the entire contents of the sequencer to confirm the program before running. $\overline{\text{WR}}$ must be held high, M0 taken low and $\overline{\text{RD}}$ taken low (see Figure 8). The first falling edge of $\overline{\text{RD}}$ will output the contents of the first sequencer location and enable the seven Status Word output pins (S6–S0). The next rising edge of $\overline{\text{RD}}$ will return the output pins to a high impedance state and increment the pointer to the next sequencer location. Subsequent $\overline{\text{RD}}$ low pulses will read through all sixteen locations and then return to location 0000. The last location in the current sequence will be indicated by a logic 1 on the S0 pin.

Running the Sequencer

Now the program is stored and checked and ready to run. The M0 pin must be returned high, which will reset the pointer to location 0000 (see Figure 9). The LTC1851 will then begin acquiring the input signal using the configuration stored in the first sequencer memory location. The first falling edge of $\overline{\text{CONVST}}$ will sample the inputs, begin a conversion and increment the pointer so that when the conversion is finished, the LTC1851 will begin acquiring the next input using the configuration stored in sequencer memory location 0001. This continues until the last programmed location is reached, after which the sequencer will return to location 0000. The program stored in the sequencer memory is retained as long as power is continuously applied to the part. This allows the user to jump between any of the three modes (Direct Address, Scan or Sequencer) or into and out of the NAP or SLEEP

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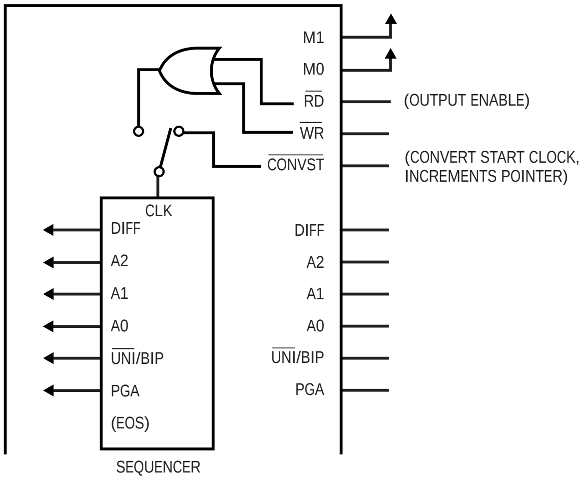


ANY EDGE OF M1 OR M0 RESETS THE SEQUENCER POINTER

Figure 9. Running the sequencer

Accurate and Fast 80MHz Amplifier Draws only 2mA

by William Jett, Danh Tran and Glen Brisebois

Introduction

The 80MHz LT1800 amplifier consumes a mere 2mA max supply current and still provides both the speed and DC accuracy required by low voltage signal conditioning and data acquisition systems. Usually, one cannot have both high bandwidth and low supply-current in an amplifier, but the LT1800 optimizes both through a 6GHz f_T process and by running the transistors at reduced quiescent currents. It can operate from supplies as low as 2.5V, and the entire supply range is available because of the device's rail-to-rail inputs and outputs. The DC performance is exceptional, with a maximum offset voltage of 350µV. This comes from trimming the input offset voltage, and canceling the input bias currents, where the maximum input bias current is 250nA. The device is available in commercial and industrial temperature grades, in both SOIC and SOT-23 packages, making for a tiny and versatile amplifier.

Performance

Table 1 summarizes the performance of the LT1800. The input offset voltage and input bias current are specified and guaranteed with the common mode voltage at each rail. Both input offset voltage and input bias current are trimmed for maximum accuracy with the inputs near the negative rail.

The LT1800 is well behaved with capacitive loading, making it easier to use than most other 80MHz amplifiers. Figures 1 and 2 show the small

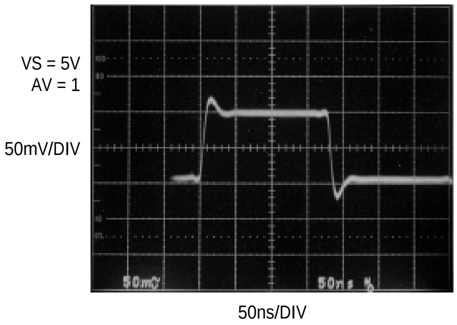


Figure 1: Small signal response
R_L = 1k

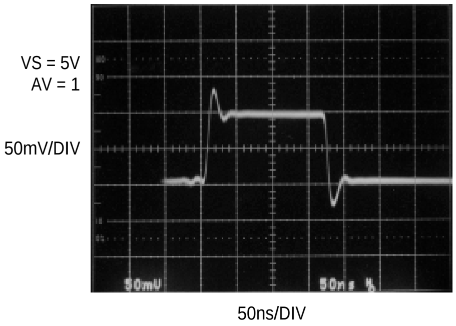


Figure 2: Small signal response
R_L = 1k, C_L = 50pF

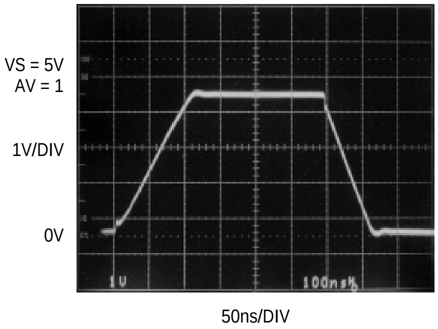


Figure 3: Large signal response
R_L = 1k, C_L = 50pF

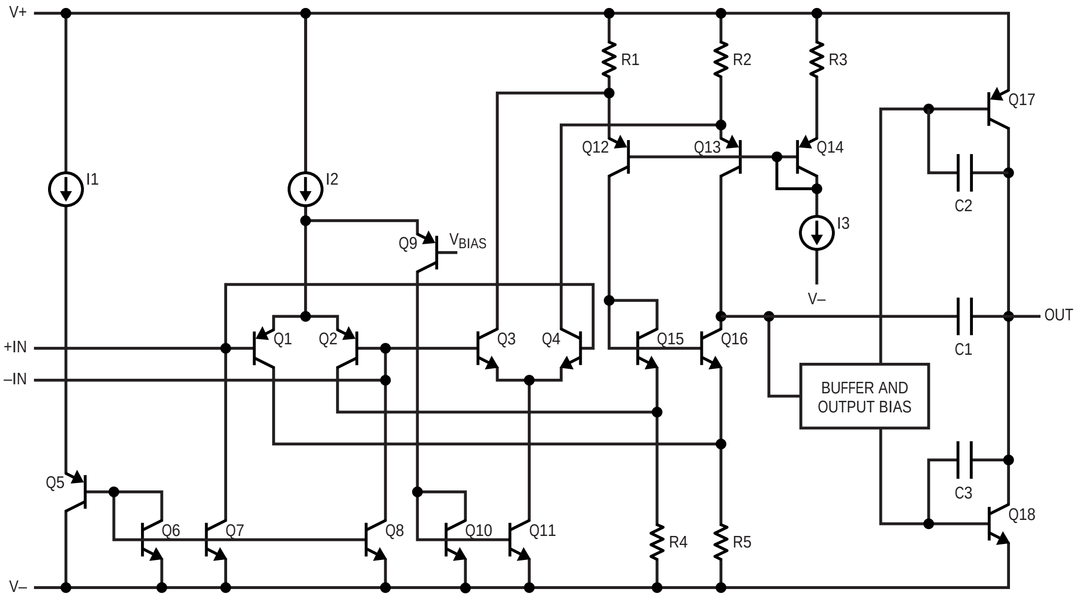


Figure 4: Simplified schematic

signal behavior of the device with a 1k load, and with 1k in parallel with 50pF. The large signal response is also well behaved, as can be seen in Figure 3.

Table 1: Specifications

Parameter	Conditions	Value	Units
–3dB Bandwidth	A_V =1	80	MHz
Gain-Bandwidth Product		80	MHz
Slew Rate		25	V/µs
Supply Current		2.0 Max	mA
Operating Supply Range		2.5 to 12	V
Input Offset Voltage	V_{CM} = 0V, SO-8	350 Max	µV
	V_{CM} = 0V, SOT-23	750 Max	
	V_{CM} = V^+, SO-8	3000 Max	
	V_{CM} = V^+, SOT-23	3500 Max	
Input Bias Current	V_{CM} = 1V	250 Max	nA
	V_{CM} = V^+	1500 Max	
CMRR	V_S = 5V, V_{CM} = 0V to 3.5V	85 Min	dB
PSRR	V_S = 2.5V to 10V, V_{CM}=0V	80 Min	dB
Input Voltage Noise	f = 10kHz	8	nV/√Hz
Harmonic Distortion	f_C = 1MHz, V_S = 5V, A_V =1, V_O = $2V_{P–P}$	–75	dBc
A_{VOL}	V_S = 5V, V_O = 0.5V to 4.5V, R_L =1k	35 Min	k
Output Voltage Swing HIGH	I_L = 5mA	V^+ – 250 Max	mV
	I_L = 20mA	V^+ – 750 Max	
Output Voltage Swing LOW	I_L = 5mA	160 Max	
	I_L = 20mA	450 Max	

Circuit Description

Figure 4 shows a simplified schematic of the amplifier. The circuit is composed of three distinct stages: an input stage, an intermediate stage, and an output stage. The input stage consists of two differential amplifiers, a PNP stage (Q1-Q2) and an NPN stage (Q3-Q4), that are active over different portions of the input common mode range. The intermediate stage is a folded cascode configuration formed by Q12-Q16, which provides most of the voltage gain. A pair of complementary common emitter devices, Q17-18, creates an output stage which can swing from rail to rail.

Looking at the input stage, devices Q5-8 act to cancel the bias current of the PNP input pair. When Q1-Q2 are active, the current in Q5 is controlled to be the same as the current in Q1-Q2, thus the base current of Q5 is nominally equal to the base current of the input devices. The base current of Q5 is mirrored by devices Q6-Q8 to each input. The cancellation is effective for common mode voltages greater than the saturation voltage of Q7 and Q8, about $V^– + 0.2V$, up to the voltage that the PNP devices switch off, about $V^+ – 1.2V$. Figure 5 shows input bias current versus common mode input voltage for a typical part.

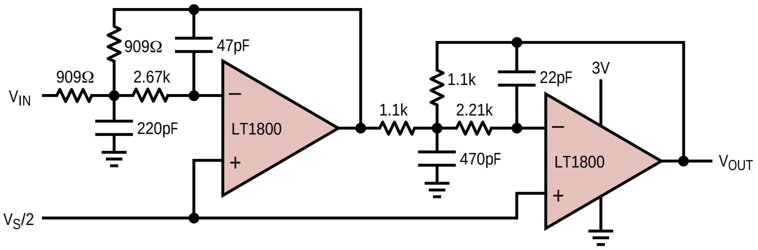


Figure 6: 3V, 1MHz, 4th order Butterworth filter

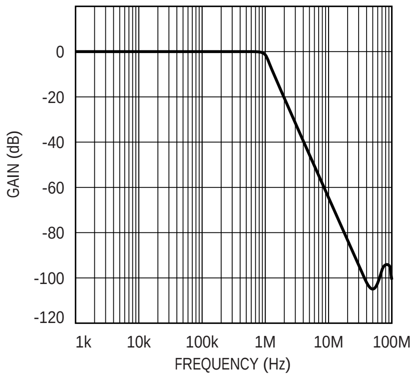


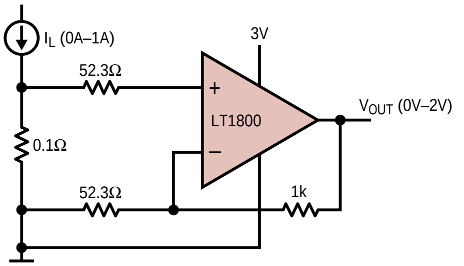
Figure 7: 1MHz filter frequency response

1MHz 4th Order Butterworth Filter for 3V Operation

The circuit shown in Figure 6 makes use of the low voltage operation and the wide bandwidth of the LT1800 to create a DC accurate 1MHz 4th order lowpass filter powered from a 3V supply. The amplifiers are configured in the inverting mode for the lowest distortion and the output can swing rail-to-rail for maximum dynamic range. Figure 7 displays the frequency response of the filter. Stopband attenuation is greater than 100dB at 50MHz. With a $2.25V_{P–P}$, 250kHz input signal, the filter has harmonic distortion products of less than –85dBc. Worst-case output offset is less than 6mV.

Fast 1A Current Sense

Figure 8A shows a simple, fast current sense suitable for quickly responding to out of range currents. The configuration amplifies the voltage across the 0.1Ω sense resistor by a gain of 20, resulting in a conversion gain of 2V/A. The –3dB bandwidth of



$V_{OUT} = 2 \cdot I_L$
$f_{-3dB} = 4MHz$
UNCERTAINTY DUE TO V_{OS}, $I_B < 4mA$

Figure 8: Fast 1A current sense

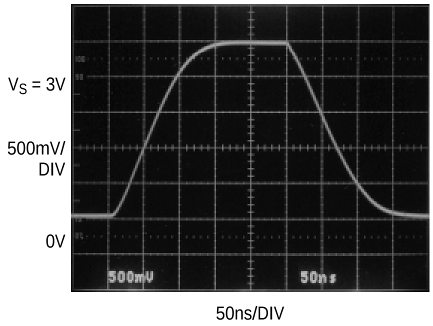


Figure 9: Current sense amplifier large signal response

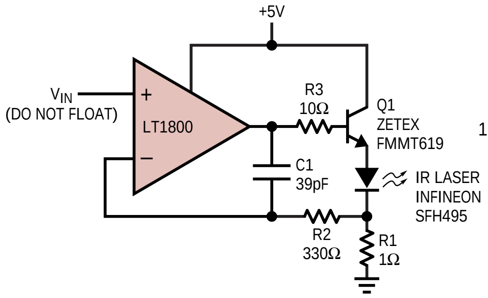


Figure 10: Small 1A low duty cycle laser driver

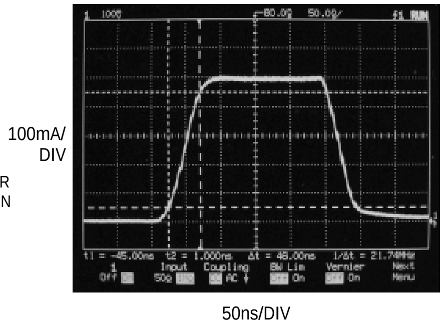


Figure 11: Pulse response of 1A laser driver circuit shows better than 50ns rise time on 500mA pulse.

the circuit is 4MHz, and the uncertainty due to V_{OS} and I_B is less than 4mA. The minimum output voltage is 60mV maximum, corresponding to 30mA. Figure 9 shows the large signal response of the circuit.

Single Supply 1A Laser Driver

Figure 10 shows the LT1800 used in a 1A laser driver application. One of the reasons the LT1800 is well suited to this control task is that its 2.4V operation ensures that it will be awake upon power-up and in control before the circuit can otherwise cause significant current to flow in the 2.1V threshold laser. Driving the noninverting input of the LT1800 to some voltage V_{IN} causes its output to rise, turning on the FMMT619 high current NPN transistor and the SFH495 IR laser. The transistor and laser will turn on until the input voltage appears back at the LT1800 inverting input, and therefore also appears across the 1Ω resistor R1. In order for this to occur, a current equal to V_{IN}/R1 must exist, and the only place it can come from is through the laser. The overall circuit is therefore a V-to-I converter with a 1 ampere per volt characteristic.

Lower values for R1 may be selected, but the designer is reminded to keep series loop traces very short: for example, even 10nH of lead inductance will cause a 16MHz pole into 1Ω, and a 1.6MHz pole into 0.1Ω! Also, when decreasing the value of R1, consider the total of the dynamic impedances of the transistor V_{BE} and the laser. They divide the feedback voltage by R1 thus increasing circuit noise gain. This has the effect of degrading the DC precision and reducing the achievable bandwidth.

Frequency compensation components R2 and C1 were selected for fast but zero-overshoot time domain response, to avoid overcurrent conditions in the laser. They may vary from design to design depending on desired response characteristics, circuit layout, the value of R1, and the actual

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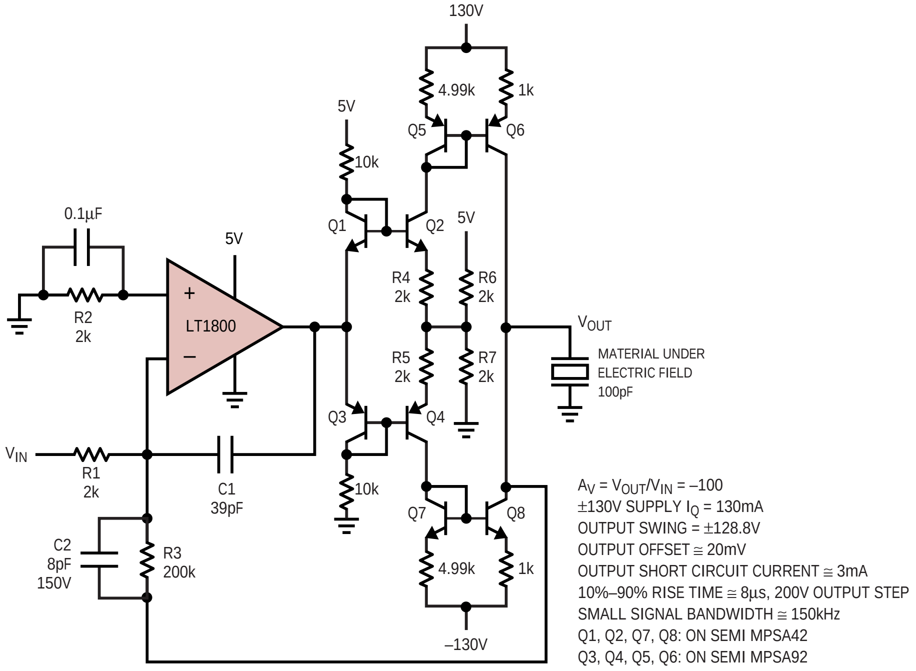


$A_V = V_{OUT}/V_{IN} = –100$
±130V SUPPLY I_Q = 130mA
OUTPUT SWING = ±128.8V
OUTPUT OFFSET ≅ 20mV
OUTPUT SHORT CIRCUIT CURRENT ≅ 3mA
10%–90% RISE TIME ≅ 8µs, 200V OUTPUT STEP
SMALL SIGNAL BANDWIDTH ≅ 150kHz
Q1, Q2, Q7, Q8: ON SEMI MPSA42
Q3, Q4, Q5, Q6: ON SEMI MPSA92

Figure 12: Low power high voltage amplifier

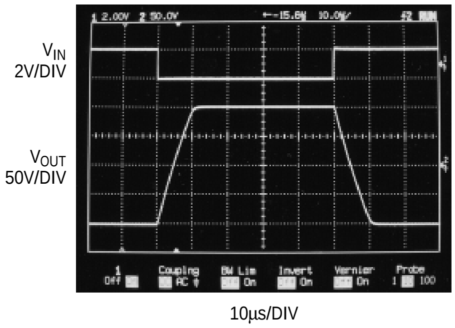


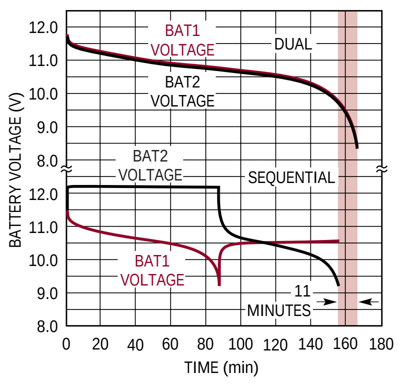
Figure 13: Large signal time domain response of the material bias amplifier

Monolithic Dual Battery Power Manager Increases Run Time and Decreases Charge Time

by Mark Gurries

Introduction

Many portable computers and other modern electronics use two (or more) rechargeable batteries to increase device run time. Two batteries discharged in sequence can double the run time over a single battery, but the downfall of a sequential system is that charging the batteries in sequence also doubles the charge time. A much more efficient method is to charge and discharge in parallel, which can *more than double* run time over a single battery and cut charge time in half relative to a sequential system. Although it has long been possible to parallel the charge and discharge of multiple batteries, it was difficult to design a circuit to do so, until now. The LTC1960 Dual Battery Power Manager solves many of the design problems inherent in parallel battery systems by including many desired features within a monolithic device and greatly simplifying the control interface. The results are a simple way to increase battery run time and significantly decrease charge time for dual battery systems.



BATTERY TYPE: 10.8V Li-Ion(MOLTECH NI2020)
LOAD CURRENT = 3A

Figure 1. Comparison of battery discharge times for a dual (simultaneous) system and for a sequential system

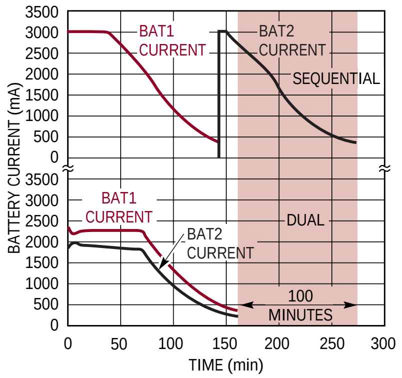
Attractive Features but Tough to Implement

How does it work? Figure 1 shows how in high current drain applications, paralleling two batteries can extend battery discharge time to more than twice that of a single battery. When two batteries share the load current equally, internal battery I^2R power losses are reduced by one fourth in each battery. This leads to longer run times, with increases of 12% possible. In terms of time, 12% represents over 21 minutes of runtime beyond a baseline of 3 hours. Popular battery chemistries with high internal resistance values benefit the most from parallel operation.

Figure 2 shows how charge times benefit. Batteries that use a Constant Voltage (CV) mode during charge termination take a long time to reach their full capacity relative to batteries that use a Constant Current (CC) mode during charge termination. Specifically, Li-Ion is one of the most popular portable computer battery chemistries in use today. The Li-Ion battery has two phases of charge: a current limited phase where most of the energy is put into the battery, and a CV phase where the current falls off quickly at first but slows down as it asymptotically approaches zero current. The problem is that the battery fills to only about 85% of its capacity in the first half of the total charge cycle time, while taking just as much time for the remaining 15%. From a user perspective, the charge time with two batteries becomes excessive. By charging the batteries in parallel, the charge time is cut almost in half relative to sequentially charging them, for three reasons:

- ❑ The lower current in each battery results in a smaller internal battery voltage drop, allowing a longer current limit phase, and therefore achieving a higher charge capacity point (90%) before entering the CV phase.
- ❑ When both batteries charged at the same time in CV phase, the time spent in CV phase is half of what it is using the sequential charging.
- ❑ Since the shared current in dual charge mode results in a given battery receiving less than its maximum allowed rate, the total current can be raised, reducing the total charge time even further.

Until now, implementing a system to do all the features listed above was prohibitively complex. Simultaneously discharging two batteries with different terminal voltages in direct electrical parallel with each other can lead to dangerous uncontrolled cur-



BATTERY TYPE: 10.8V Li-Ion (MOLTECH NI2020)
REQUESTED CURRENT = 3A
REQUESTED VOLTAGE = 12.3V
MAX CHARGER CURRENT = 4.1A

Figure 2. Comparison of battery charge times for a dual (simultaneous) system and for a sequential system

rent flow between the two batteries. Traditional circuits for paralleling batteries, which also had to provide isolation, often consumed any extra battery energy, offering little or no net gain in run time.

Then there is the issue of charging two Li-Ion batteries in parallel to proper charge termination while maintaining a precision voltage that is independent of the current. All is even more complicated if the batteries used are not the same chemistry or voltage (cell count) configuration.

Another problem is implementing power crisis management when a selected power source loses power or was inadvertently removed. Adding bulk capacitance to prop up the system while the system tries to switch over to another power source is not an option in today's products, given space and cost constraints. There are also safety issues, such as preventing accidental overcharge of the batteries when the host crashes, and safely handling a catastrophic short circuit condition with the loss of control.

Designers have long known that creating a circuit that does all of these tricks *and* fits into the limited space on modern circuit boards is just about impossible, until now...

Introducing the LTC1960

The LTC1960 is the first single chip dual battery PowerPath™ and charge controller that allows dual parallel charge and discharge of batteries. The IC is a complete analog building block that, when under the control of a host microcontroller, can safely implement all of the features mentioned above, with minimal parts count. In addition to the charge and discharge PowerPath control, the LTC1960 integrates two precision DACs for charge control, a watchdog timer, full status reporting bits, input current limiting, short circuit overload protection and automatic power crises management in a single IC that can operate up to 32V. Figure 3 shows the system architecture.

The LTC1960 can be broken down into two major parts: A PowerPath controller and a charger controller.

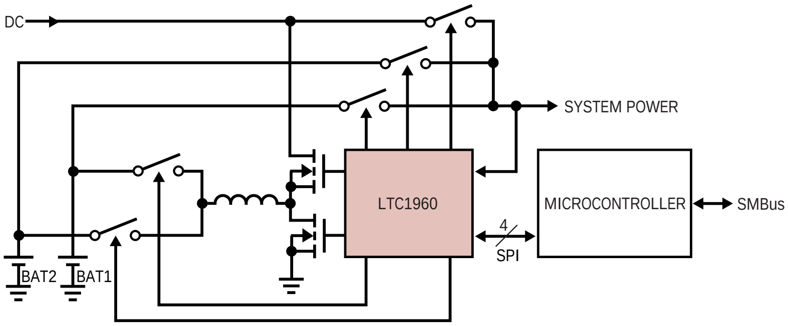


Figure 3. The LTC1960 system architecture

The PowerPath controller is designed to manage two batteries and a DC input supply. The heart of the PowerPath controller is the ideal diode circuit that allows precise voltage tracking between batteries. The ideal diode circuit uses the same MOSFET transistors that turn power on and off, and makes them act like diodes, but without the power loss issues or variation in voltage drop as a function of current. High-speed comparators monitor reverse current conditions and shutoff the MOSFETs in microseconds. An undervoltage detector watches for sudden loss of voltage at the load and turns on all the power sources in microseconds, with no host intervention required. A high-speed emergency shutdown input is provided in case of CPU overvoltage conditions or other system-level crises. Finally, there is a combined time and current based short circuit protection system that protects the PowerPath MOSFETs from destruction in the event of a short.

The charger controller uses synchronous rectification for both high efficiency and high current capability with a 0.5V low dropout capability and a 99% max duty cycle. An 11-bit voltage DAC with a worse case SYSTEM level accuracy of ±0.8% is provided along with a 5% accurate 10-bit current DAC. The ability to program from milliamps to amps makes maintaining good current accuracy at low current a challenge. Often such low currents are needed during battery recovery from excessive discharge. The LTC1960 charger solves this problem by pulse charging in the low current mode. By using time averaging, accuracy can be maintained down to milliamp levels. A patented 5% accurate input current limit threshold allows all the power of the wall adapter to be used to charge the batteries as quickly as possible. An overvoltage comparator detects a sudden battery disconnect and shuts off the charger until the overvoltage condition is cleared. Figure 4 shows a schematic for a complete charger.

Ideal Diodes

Figure 5 shows a circuit that safely parallels batteries for discharge. The solution is unique in that it that drives two back-to-back series MOSFETs used in the power path of the battery, which act as a virtual ideal diode. The IC actively drives the gate of a P-Channel MOSFET, Q7, such that when current is flowing out of the battery, the voltage drop across both MOSFETs is regulated to 25mV. This is at least a factor of 20 improvement over the best Schottky diode, where a factor of 30 improvement is more typical.

The upper limit of regulation is reached when the load current multiplied by the $R_{DS(ON)}$ of the Q7 exceeds 25mV. If the voltage drop decreases below 25mV, then Q7 turns off slowly, preventing current flow. If the voltage across the MOSFETs is reversed at any time with a magnitude exceeding 20mV, the MOSFET will turn off instantly. The power loss of this circuit is less than any other solution, short of an electromechanical switch. A similar circuit is employed in the battery charge path as well, using

N-Channel MOSFETs as shown in Figure 6.

Automatic Current Sharing

In a dual parallel charge configuration, the LTC1960 does not actually control the current flowing into each individual battery. This job is handled by the batteries themselves. The capacity or Amp-Hour rating of each battery determines how the charger current is shared. This automatic steering of current is what allows both batteries to reach their full capacity points at the same time. In other words, given all other things are equal, charge termination will happen simultaneously.

A charging battery can be modeled as a huge capacitor and hence governed by the same laws.

$$I = C \bullet (dV/dt)$$

Where:

I = Current flowing though the capacitor.

C = Capacity rating of battery (using Amp-Hour values instead of capacitance)

dV= Change in voltage

dt = Change in time

The equivalent model of a set or parallel batteries is a set of parallel capacitors. Since they are in parallel the change in voltage over time is the same at each battery.

$$(dV/dt)_{BAT1} = (dV/dt)_{BAT2}$$

From here we can simplify.

$$I/C_{BAT1} = dV/dt = I/C_{BAT2}$$

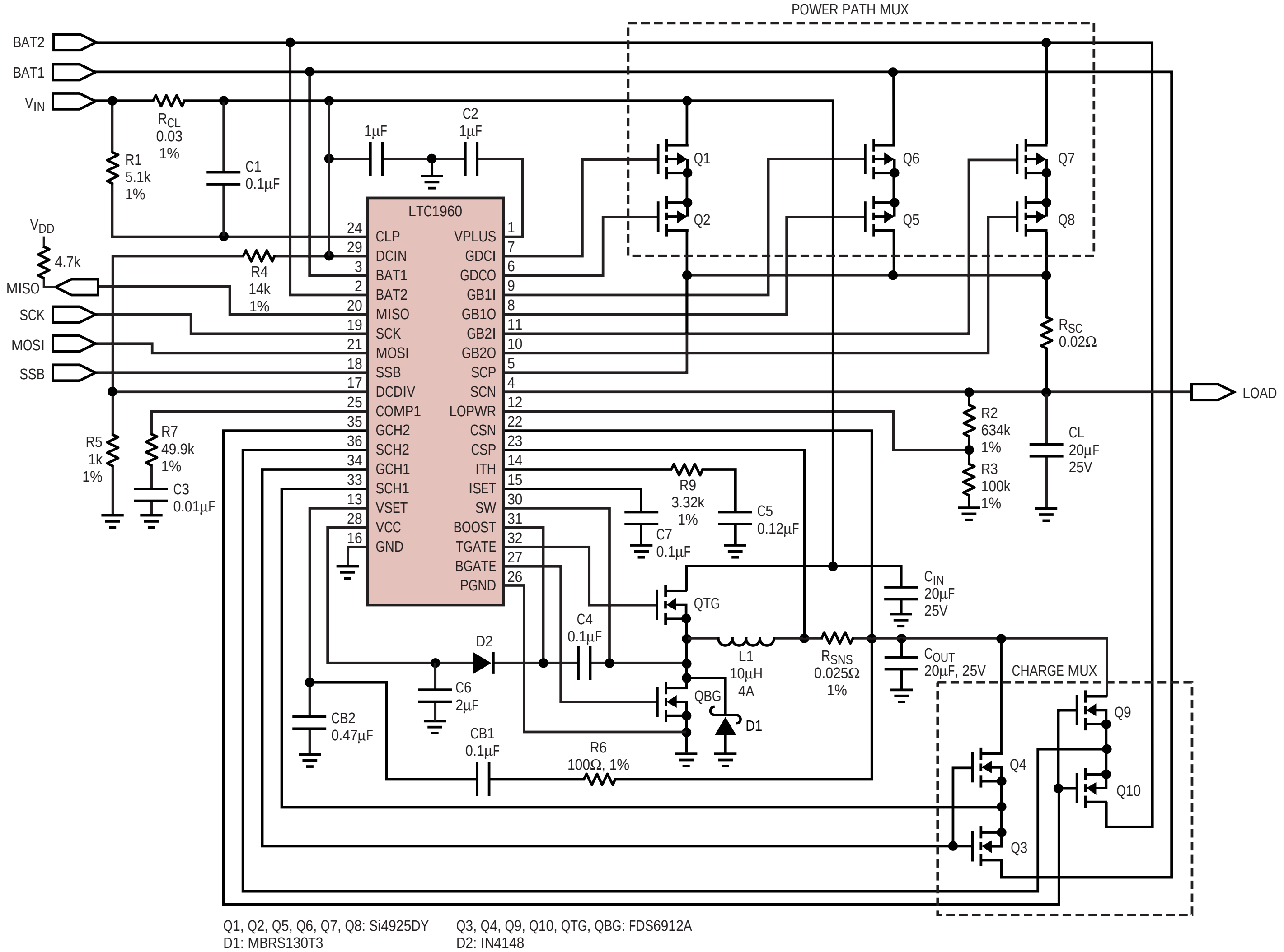
$$I_{BAT2}/I_{BAT1} = C_{BAT2}/C_{BAT1}$$

The current divides as the ratio of the batteries' capacity ratings. The sum of the current into both batteries is the same as the current being supplied by the charger. This is independent of the mode of the charger (CC or CV).

$$I_{CHRG} = I_{BAT1} + I_{BAT2}$$

$$I_{BAT1} = I_{CHRG} \bullet C_{BAT1}/(C_{BAT1} + C_{BAT2})$$

$$I_{BAT2} = I_{CHRG} \bullet C_{BAT2}/(C_{BAT1} + C_{BAT2})$$



Q1, Q2, Q5, Q6, Q7, Q8: Si4925DY
D1: MBRS130T3

Q3, Q4, Q9, Q10, QTG, QBG: FDS6912A
D2: IN4148

Figure 4. Complete charger schematic

Please note that the actual observed current sharing value will vary from manufacturers' specified capacity ratings since it is based on real physical capacity at the time of charge.

Dual Battery Discharging

The rules for charge also apply to discharge when dealing with like batteries. The amount of current sharing is a direct function of the state of charge between the two batteries. Discharging two batteries of identical configuration, characteristics and charge states will allow them to maintain whatever current sharing levels they establish until both batteries run out of energy at the same time. Parallel batteries of slightly mismatched characteristics will run out of energy at slightly different times since they have different real world capacities.

Dual Battery Charging

Batteries that need constant voltage (CV) charge termination can benefit from parallel charge. Under ideal conditions, a CV battery would become full the moment the cell voltage equals the termination voltage specified for the cell. In reality the series (ESR) resistance will make the cell voltage appear higher than it really is because the voltage drop across the internal series resistance is added to the actual cell voltage. As a result, instead of instant charge termination, there is a gradual reduction in current until the resistive voltage drop goes to zero.

Unfortunately, you never reach charge termination because the charge current asymptotically approaches zero. This necessitates a cutoff current threshold that corresponds to a capacity that is close to 100%. Since the voltage drop is proportional to the charge current, by reducing the current though current sharing between two battery packs, both batteries will charge faster than if each battery was charged in a serial (sequential) fashion. In other words, the same properties of that allow longer run times for parallel battery discharge also work to reduce total charge time. The LTC1960's low 25mV ideal diode voltage drop will ensure that both batteries will terminate at nearly the same time. The Schottky diode approach would create a much greater discrepancy in charge states between the two batteries when one of the two batteries decides it is full.

Turbo Charging

There is another advantage when charging Li-Ion batteries in parallel in the CC phase of charging. If the wall adapter and battery charger are capable of supplying more than a 1C charge rate to a single battery pack, the charger can programmed at a higher charge rate, up to 2C, since the charge current will be shared between the two batteries.

Charging to the Max with Input Current Limiting

The LTC1960 features Linear Technology's patented wall adapter current limiting. The circuit monitors the current draw from the wall adapter and allows the battery, or batteries, to be charged at the highest possible current without exceeding the adapter's current rating. In terms of pure current operation, the sum of charger input current and the system load current are never allowed to exceed the maximum current rating of the wall adapter. The circuit works by constantly adjusting the charger output current automatically in time of potential adapter overload such that a constant current is drawn from the adapter without exceeding its ratings. When the system load frees up adapter current, the charger is restored to its original charge current limit setting. This allows the use of reserve AC adapter power to charge faster without needing a bigger wall adapter.

Charge Safely

In addition to the ideal diode reverse current protection, a watchdog timer is included in the LTC1960 to prevent accidental overcharge if the host computer is shutdown by accident or crashes. Simply writing to the charger control register every second is all that is needed to keep the charger going. If the charger times out, resumption of charge will occur as soon as a new write to the charge control register occurs. There is no loss of voltage and current charge values. The LTC1960 features bit-for-bit readback when setting charger voltage and current values, which allows for error free programming without the need for any specialized error checking code or software.

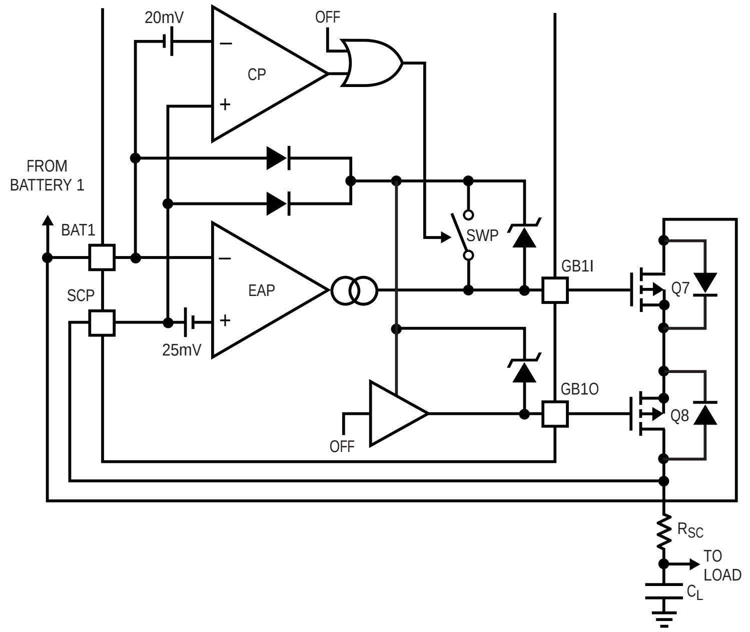


Figure 5. Single battery path discharge controller

More than Two Batteries? No Problem

For situations where two batteries are not enough, such as in backup power situations, it is possible to configure the LTC1960 to work with more than two batteries. The IC is designed to allow the use of multiple LTC1960s in parallel with only one additional connection required from the host microcontroller for each LTC1960 added to the system.

Automatic Crisis Power Management

Another aspect of PowerPath control is the ability to handle sudden loss of power to the load. The LTC1960 allows for the selection of a single power source—from the three options: AC power adapter and the two batteries—to act as the sole source for the system. The LTC1960 manages power by monitoring the voltage at the summing point of all three sources (the load voltage) at the SCN pin (refer to Figure 4). A programmable voltage comparator called LOW_PWR detects a loss of power and activates the 3-diode mode (3DM) to restore power to the system *before* it fails regardless of the original power source chosen. 3DM mode refers to the state where all three power sources are connected to the load. The three MOSFETs, Q2, Q5 and Q8, are turned on in 10µs when LOW_PWR detects a voltage drop; putting all three power sources in parallel though the diode functions of Q1, Q6 and Q7. The power source with the highest voltage will pick up the load, with multisource current sharing possible. The ideal diode MOSFETs are active in preventing energy transfer from any power source to any other power source. Only discharge is permitted. The battery charger MOSFETs and the charger itself are not affected by 3DM mode.

Three Strikes and You're Out

The LTC1960 can be programmed to use any power configuration of the dual batteries and wall power, but it will not force the issue with a configuration that simply can't supply enough voltage (unless the host system demands it). Whenever LOW_PWR is tripped, the LTC1960 assumes the worst and automatically goes into 3DM mode. It waits 1 second and then turns off 3DM mode while reconnecting the original, pre-LOW_PWR, power source configuration. The LTC1960 increments the Power Fail counter each time LOW_PWR is tripped, and at three consecutive strikes for any particular configuration, it goes into 3DM and stays there. It also sets the PF bit in the LTC1960 Status Register. Up to this point, nothing outside of the LTC1960 circuit needs to intervene—though once the PF bit is set, the system software is responsible for determining if the current power source configuration is still viable as a power source, or if it isn't, whether it should be replaced by another configuration.

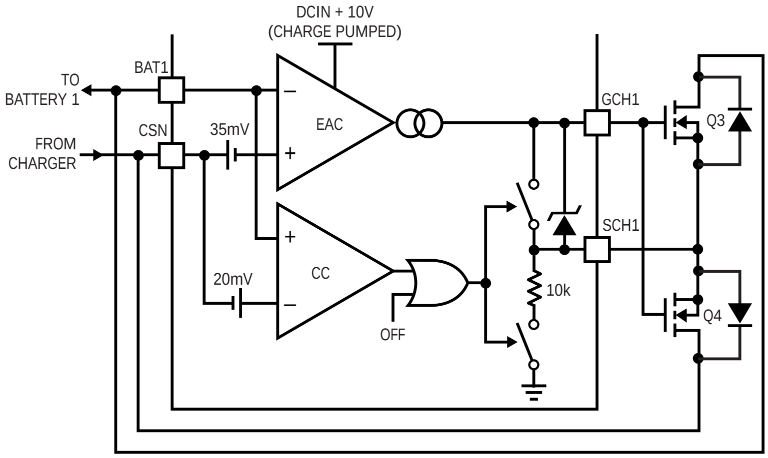


Figure 6. Single battery path charge controller

Ultraflexible Discharge PowerPath Management

Each discharge PowerPath can be individually selected or selected in *any* combination without regard to invalid or unsafe configurations. The host system can choose to leave all three PowerPaths on (3DM mode) at the same time without concerning itself with the power configuration. At startup, the LTC1960 defaults to 3DM mode until a specific path is selected through via the serial interface. If none is selected, it remains in 3DM mode. This greatly simplifies integration of the LTC1960. No software required: Just plug it in and go!

Realistic Short Circuit Protection

The LTC1960 provides short circuit protection against excessive current flow. When the voltage across RSC exceeds 100mV nominal, a 15ms timer is started. If at the end of the timer period the load current does not decrease below the trip point, the LTC1960 shuts down. The 15ms timer prevents premature shutdown by allowing transient currents to pass though.

Emergency System Shutdown

LTC1960 will shut down for either of two events. The first is excessive current due to a system short, as described above. The other is that it is told to shut down by the host system by driving the DCDIV pin above 7V. The DCDIV input allows the system designer to kill power in an emergency, perhaps to protect the CPU from an overvoltage condition. The shutdown mode is a latching mode that forces all charge and discharge FETs to the off state regardless of the PowerPath register settings. The LTC1960 is reset by cycling power off, then on again.

Precision Wall Adapter (Input) Voltage Trip Point

To minimize power dissipation at high power levels, battery chargers are often required to operate in low dropout

continued on page 36

CompactPCI Hot Swap Controllers with Bus Precharge, On-Chip Intercept of PCI Reset Signal and Much More

by Andrew Gardner

Introduction

When a circuit board is inserted into a "hot" (powered) backplane, its supply bypass capacitors can draw large currents from the backplane power bus as they charge. These currents can cause glitches on the backplane supply voltage, resetting other boards in the system, and can even damage edge connectors. The LTC1644 and LTC1646 Hot Swap™ controllers safely limit these charging currents during board insertion into a hot backplane. They also offer several features specifically tailored for CompactPCI™ (CPCI) Hot Swap applications:

- Precharge output for biasing I/O connector pins during board insertion and extraction to minimize bus glitches
- On-chip intercept of the global PCI reset signal
- Dual-level circuit breakers for the 5V and 3.3V supplies with slow and fast response times for overcurrent and short-circuit fault conditions, respectively
- The ability to power-up all supplies over a wide range of capacitive loads using foldback current limit without causing spurious overcurrent faults

The LTC1644 provides a Hot Swap solution for CPCI applications requiring all four rails available from a CPCI connector: 5V, 3.3V, 12V and –12V. The LTC1646 is intended for use in CPCI applications where only the 5V and 3.3V rails are used. The LTC1644 is available in a 20-pin SSOP package, whereas the LTC1646 is available in a space-saving 16-pin SSOP package.

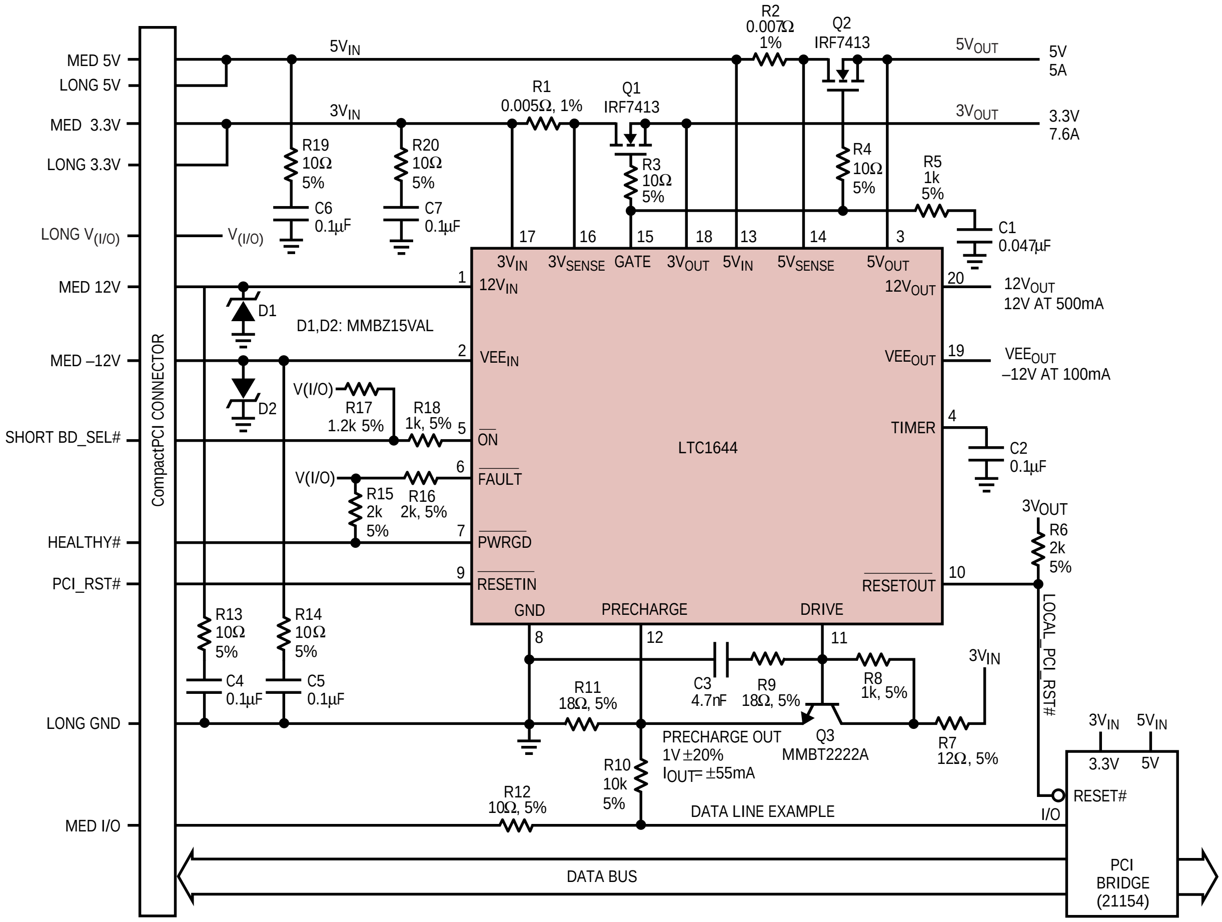


Figure 1. LTC1644 typical application

Typical CPCI Hot Swap Applications

Figures 1 and 2 show the LTC1644 and LTC1646, respectively, in typical CPCI Hot Swap applications. In both applications, transistors Q1 and Q2 limit the 3.3V and 5V supply currents when a board is inserted into a hot backplane. The currents through Q1 and Q2 are sensed across resistors R1 and R2. Resistors R3 and R4 prevent high frequency oscillations in Q1 and Q2. By ramping the gates of Q1 and Q2 up at a controlled rate, the transient surge current (I = C • dv/dt) drawn from the main backplane supply is limited to a safe value when the board is inserted. In addition, the LTC1644 contains internal pass transistors for both the 12V and –12V supplies that have fixed current limits. A current foldback limit feature also protects all of the supplies. If an output voltage is shorted to ground, the current limit drops in order to keep power dissipation and supply glitches to a minimum.

Transistor Q3 and its associated components form the precharge circuit in both applications. The voltage at the DRIVE pin is varied in order to maintain a constant 1V at the PRECHARGE pin. Resistor R10 biases the example I/O line to 1V during hot insertion and extraction, thus minimizing glitches on the backplane I/O line as the connector pin makes/breaks its connection.

The LTC1644 and LTC1646 are designed to fully support the CPCI backplane-to-daughtercard signaling environment. The BD_SEL# signal is connected to the ON pin while the HEALTHY# signal is connected to the PWRGD pin. In the event that any of the output voltages fall below their power-good thresholds, the PWRGD pin is pulled up to $V_{(I/O)}$, causing the HEALTHY# signal to deassert. The global PCI_RST# signal is combined on-chip with the HEALTHY# signal in order to generate the LOCAL_PCI_RST# signal at the RESETOUT pin. The LOCAL_PCI_RST# signal is pulled low whenever the HEALTHY# signal is high; it can also be pulled low when the PCI_RST# input signal is low.

When a board is inserted into a CPCI connector, the long $V_{(I/O)}$, 5V, 3V and GND pins make contact first and power up the $V_{(I/O)}$ pull-up resistors, bus precharge circuitry inside the LTC1644 and LTC1646 and the PCI bridge chip. During the next stage of insertion, the medium length 5V, 3.3V, 12V, –12V and I/O pins make contact. At the final stage of insertion, the short connector BD_SEL# pin makes contact, pulling the ON pin voltage to GND, and a power-up sequence begins.

Power-Up Sequence

The timing for a typical power-up cycle for the LTC1644 is shown in Figure 3 (the LTC1646 waveforms are similar except for the absence of the 12V and –12V input and output voltages). The gates of the FETs (GATE pin) are pulled up by an internal

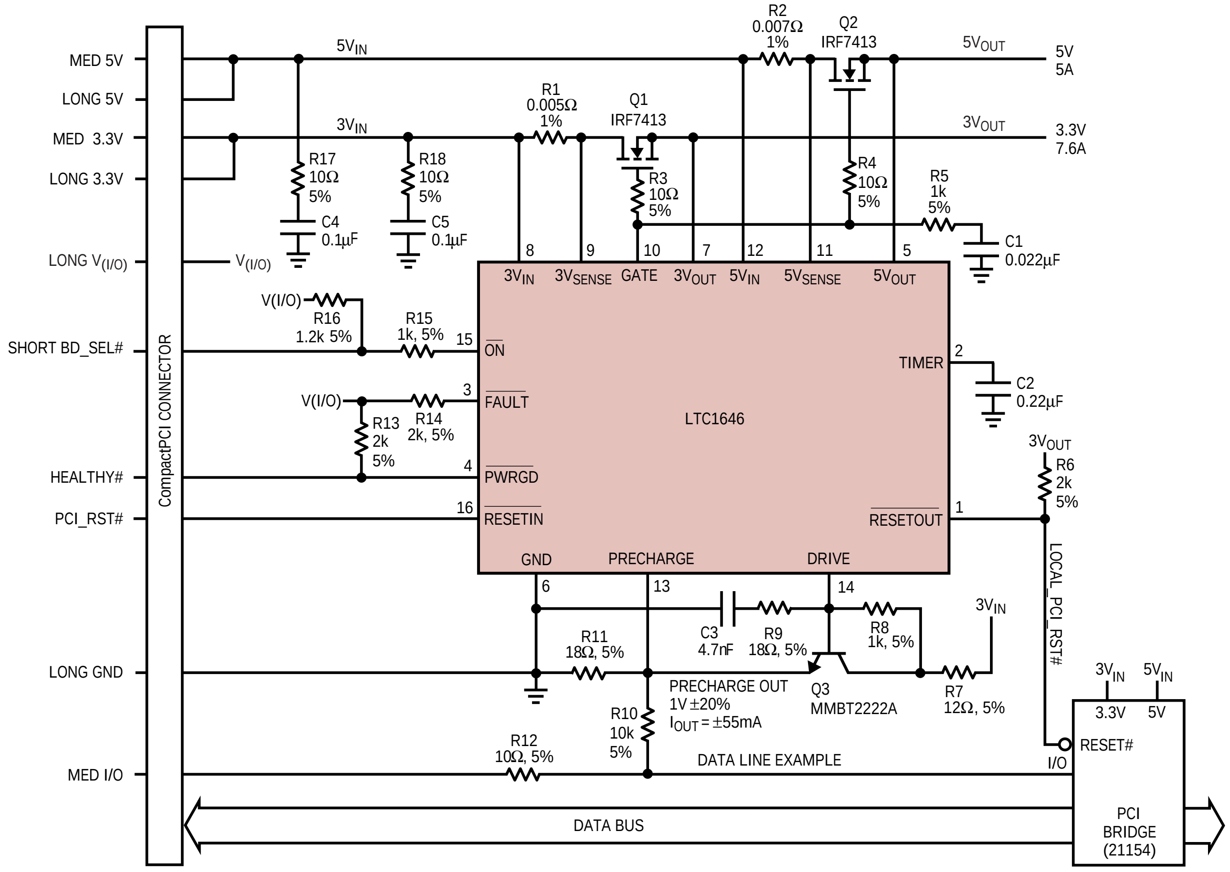


Figure 2. LTC1646 typical application

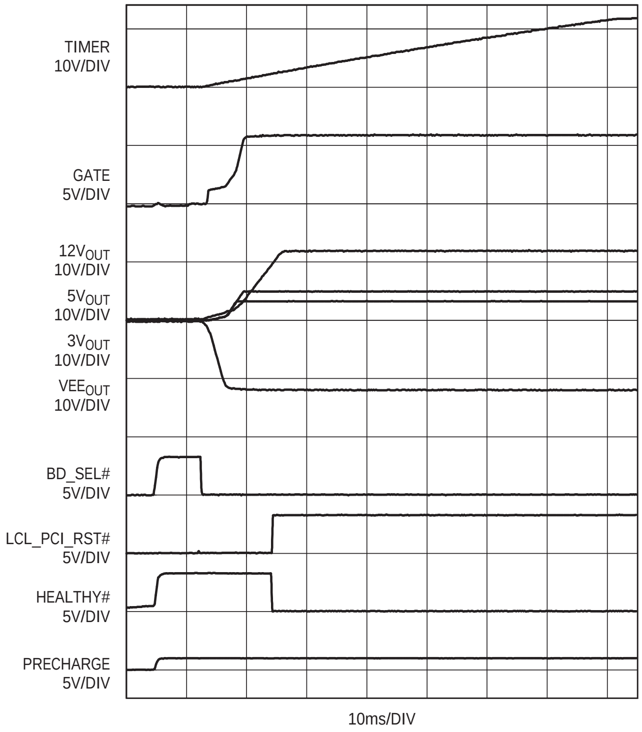


Figure 3. Typical power-up sequence

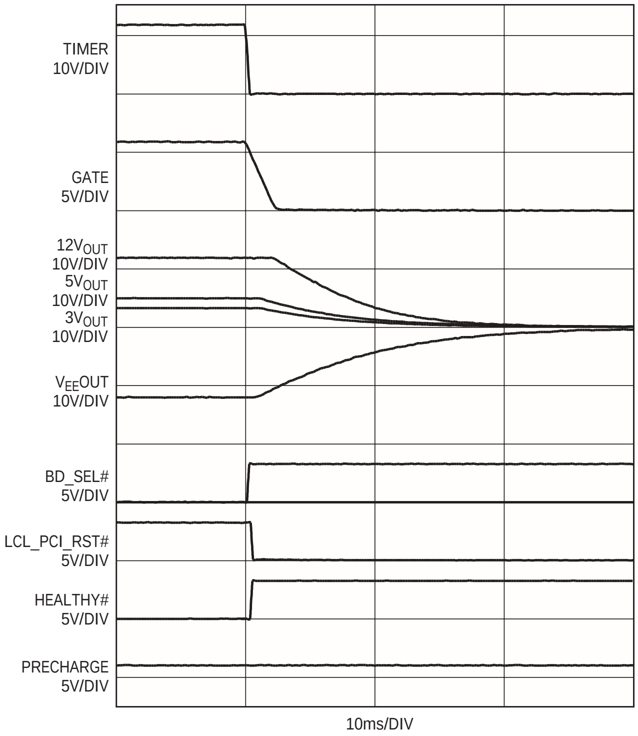


Figure 4. Typical power-down sequence

current source. Simultaneously, the capacitor connected to the TIMER pin is also charged by an internal current source (5µA for the LTC1646, 20µA for the LTC1644). Each supply is allowed to power-up at the rate dv/dt = I/C1 (where I is 20µA for the LTC1646 and 50µ for the LTC1644) or as determined by the current limit and the load capacitance, whichever is slower. Current limit faults are ignored while the TIMER pin voltage is ramping up and is less than the timer threshold voltage. Once all the output supply voltages have crossed their power-good thresholds, the HEALTHY# signal is pulled low and LOCAL_PCI_RST# can follow PCI_RST#. The power cycle is complete after the TIMER pin voltage exceeds the timer threshold voltage (1.2V for the LTC1646, V_{12VIN} – 1V for the LTC1644).

Power-Down Sequence

When the $\overline{\text{ON}}$ pin is pulled high, a power-down sequence begins (see Figure 4). Internal pull-down switches are connected to each of the output supply voltage pins to discharge the bypass capacitors to ground. The TIMER pin is immediately pulled low and the voltage on the GATE pin is discharged by a 200µA current source to prevent the load currents on the 3.3V and 5V supplies from going to zero instantaneously and causing glitches on the power supplies. When any of the output voltages dips below its power-good threshold, the HEALTHY# signal is pulled high. The PRECHARGE pin voltage is held at 1V by the LTC1644 and LTC1646 independent of the state of the $\overline{\text{ON}}$ pin voltage.

Timer

During a power-up sequence, a current source (5µA for the LTC1646, 20µ for the LTC1644) is connected to the TIMER pin and current limit faults are ignored until the voltage on this pin exceeds the timer threshold voltage (1.20V for the LTC1646 and $12V_{IN}$ – 1V for the LTC1644). This feature allows the chip to power-up CPCI cards with widely varying capacitive loads on the supplies. The timer period should be set longer than the maximum supply turn-on time but short enough not to exceed the maximum safe operating area of the pass transistors in the event of a short circuit. The TIMER pin voltage is immediately pulled low when the $\overline{\text{ON}}$ pin voltage is pulled high.

Short-Circuit Protection

During a power-up cycle, the LTC1644 and LTC1646 rely on analog current limit to protect the supplies against short-circuit faults. To prevent excessive power dissipation in the pass transistors and prevent voltage spikes on the supplies during short-circuit conditions, the current limit on each supply is designed to be a function of the output voltage. As the output voltage drops, the current limit decreases. Unlike a traditional circuit breaker function, where huge currents can flow before the breaker trips, the current foldback feature guarantees that the supply current will be kept at a safe level and prevent voltage glitches while applying power into a short.

Contemporary hot swap controllers also rely on analog current limit as a means of protecting against short-circuit faults once a board has powered-up. In addition, these controllers tend to delay opening the

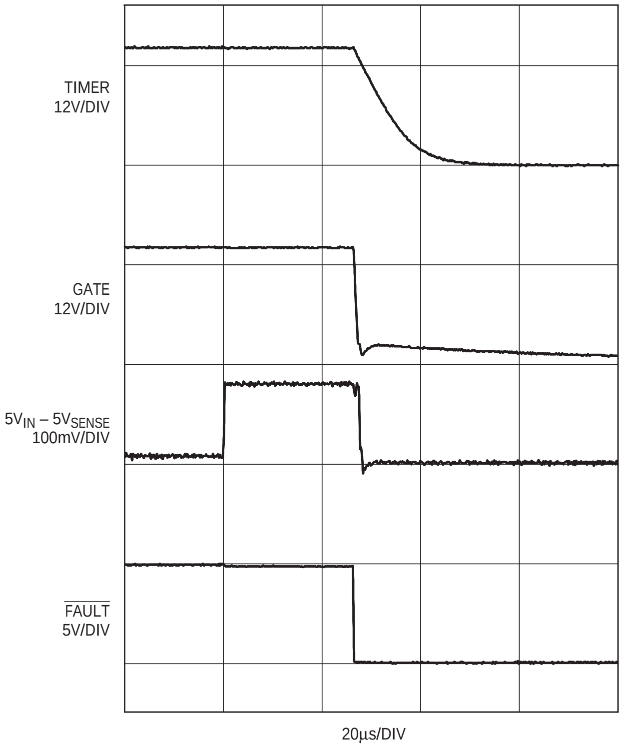


Figure 5. Overcurrent fault on 5V

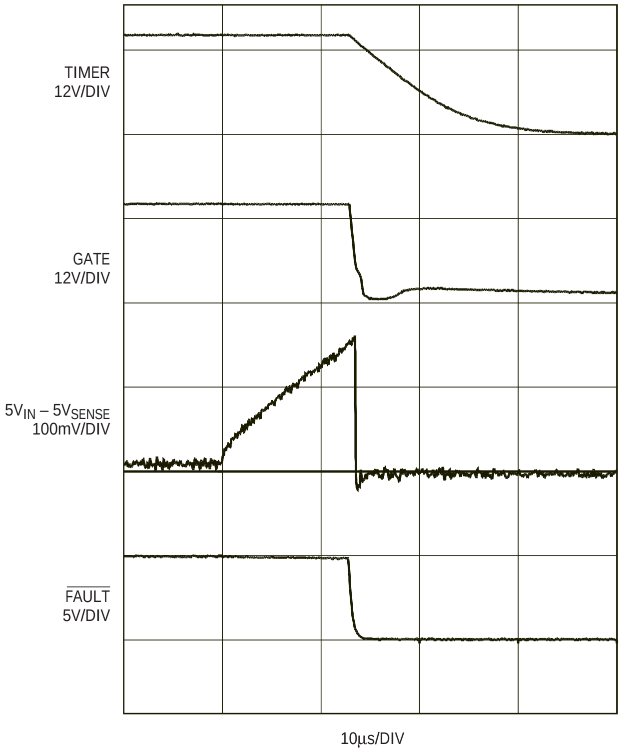


Figure 6. Short-circuit fault on 5V

circuit breaker for a period of time in order to prevent brief overcurrent conditions from triggering a fault. Although this approach guarantees that the supply current will not exceed the design limit, it has an inherent flaw: the hot swap controller deliberately compromises output voltage compliance in order to regulate supply current during an overcurrent glitch. As a result the output voltage may drop out of tolerance causing a variety of potential problems on the CPCI board, among them being the potential for asserting the LOCAL_PCI_RST# signal.

The LTC1644 and LTC1646 provide a simple solution to this problem. Both the 5V and 3.3V supplies use dual-level circuit breakers to guard against overcurrent and short-circuit faults once the power-up cycle is completed. Overcurrent faults are defined here as the condition where the voltage across the terminals of an external sense resistor exceeds 50mV but is less that 150mV. A sense resistor voltage differential greater than 150mV qualifies as short-circuit fault. During an overcurrent event, an internal timer is started, but no attempt is made to limit current by reducing the gate voltage of the external 3.3V and 5V pass FETs. If the overcurrent condition remains after 20µs, the circuit breaker is tripped, the GATE pin is pulled down to ground and the chip latches-off (Figure 5). In the event of a short-circuit fault, however, the circuit-breaker trips without delay causing the GATE pin to be pulled to ground, and the chip latches-off (Figure 6). Toggling the /ON pin voltage low-high-low causes another power cycle to begin and resets the circuit breakers.

Power-Good and Resetout Outputs

Both the LTC1644 and the LTC1646 monitor the status of the output voltages using the /PWRGD pin. For CPCI applications, the HEALTHY# backplane signal should be connected to the $\overline{\text{PWRGD}}$ pin and the PCI_RST# backplane signal should be tied to the $\overline{\text{RESETIN}}$ pin. The HEALTHY# and PCI_RST# signals are combined on chip to yield the LOCAL_PCI_RST# signal (see Table 1), which is available at the $\overline{\text{RESETOUT}}$ pin. In the event that any of the output voltages drop below their power-good thresholds for more than 20µs, the HEALTHY# signal is pulled high, and the LOCAL_PCI_RESET# signal is pulled low. The delay feature prevents a system reset from occurring as a result of brief glitch on the output supply voltage.

Table 1. LOCAL_PCI_RST# truth table

PCI_RST#	HEALTHY#	LOCAL_PCI_RST#
Low	Low	Low
Low	High	Low
High	Low	High
High	High	Low

Precharge

During hot insertion and extraction, the bus I/O connector pins will bounce before a solid connection is made or broken. The charging and discharging of these three-stated pin capacitances result in glitches that can potentially interfere with bus transactions that are occurring while a CPCI board is being inserted into or removed from the system. In order to minimize these glitches, these bus I/O pins should be precharged to 1V before the medium length CPCI connector pins make or break contact with the backplane connector. The LTC1644 and the LTC1646 offer a solution to the precharge requirement for CPCI applications. Both parts provide a PRECHARGE pin and a DRIVE pin that are intended for use with the precharge application circuit, as shown in Figures 1 and 2. The precharge application circuit is capable of sourcing and sinking up to 55mA of current and can bias up to 128 I/O connector pins operating from $V_{(I/O)}$ voltages as high as 5V while still maintaining 1V ±20% at the PRECHARGE pin. Power for this circuit should be derived from the long $5V_{IN}$ or $3V_{IN}$ connector pins in order to guarantee that the 1V precharge output is available to bias the medium length connector pins during CPCI board insertion and extraction.

Conclusion

The LTC1644 and LTC1646 provide comprehensive solutions for CPCI Hot Swap applications. These devices incorporate several features that are tailored for CPCI, such as bus precharge and on-chip intercept of the global PCI_RST# signal. They are capable of powering up CPCI boards with wide ranges of load capacitance in foldback current limit. Once the power-up cycle is completed, dual-level circuit breakers for the 5V and 3.3V supplies offer fast, effective current limiting in the event of a short circuit without compromising output voltage compliance during brief overcurrent conditions, thus offering CPCI board designers a level of short-circuit protection that is unique to LTC's Hot Swap family.

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LT1800, continued from page 11

laser and transistor devices selected. Although not found to be absolutely necessary, R3 is included to ensure a minimum linear load for the op amp. Figure 11 shows the time domain response of this circuit, measured at R1, and given a 500mV 230ns input pulse. While the circuit shown is capable of 1A operation, the laser and the transistor are thermally limited and so must be operated at low duty cycles.

Low Power High Voltage Amplifier

Certain recently developed materials have optical characteristics that depend on the presence and strength of a DC electric field. Many applications for these materials require a bias voltage applied across the materials, sometimes as high as 100s of volts, precisely in order to achieve and maintain desired properties in the material. The materials are not conductive, and present an almost purely capacitive load.

Figure 12 shows the LT1800 used in an amplifier intended for capacitive loads and capable of 250V output swing. When no input signal is present, the op amp output sits at about mid-supply. Transistors Q1 and Q3 create bias voltages for Q2 and Q4, which are forced into a low quiescent current by degeneration resistors R4 and R5. When a transient signal arrives at V_{IN}, the op amp output jumps away from mid-supply and causes current through Q2 or Q4 depending on the signal polarity. The current, limited by the clipping of the LT1800 output and the 3kΩ of total emitter degeneration, is level shifted to the high voltage supplies and mirrored into the capacitive load. This causes a voltage slew at V_{OUT} until the feedback loop (through R3) is satisfied. The LT1800 output then returns back to near mid supply, providing just enough DC output current to maintain the output voltage across R3. The circuit thus alternates between a low current hold state and a higher transient but limited current slew state.

Careful attention to current levels minimizes power dissipation allowing for a dense component layout, and also provides inherent output short circuit protection. To further save power, the LT1800 is operated single supply with its inputs at ground. Because the inputs are at ground, the LT1800 turns off its internal bias current cancellation, and adding R2 externally restores input precision.

Figure 13 shows the time domain response of the amplifier providing a 200V output swing into a 100pF load.

Conclusion

The LT1800 provides a low power solution to high speed, low voltage signal conditioning. The rail-to-rail inputs and output of the device maximize dynamic range, and can simplify designs by eliminating the negative supply. Circuits that require source impedances of 1k or more, such as filters, will benefit from the low input bias currents and low input offset voltage. The combination of speed, DC accuracy, and low power in a SOT-23 package makes the LT1800 a top choice for low voltage signal conditioning.

Micropower Negative LDO Provides a Quiet Output in SOT-23

by Todd Owen

Introduction

With the myriad of new portable and wireless devices in design today, a multitude of power supply requirements surface. Portable devices run from batteries, requiring low dropout voltage and low quiescent current to maximize battery life. Low noise operation is a key parameter for RF applications, where power supply noise creates unwanted sidebands on RF amplifiers, degrading performance. Another factor is low voltage operation, both on the input and output. Finally, portability requirements dictate strict size constraints on both active devices and passive components. These requirements have been met for many designs with families of low noise, low dropout regulators, but one hole had yet to be filled.

Taking the Flip Side

A wide choice of regulators is available for providing a low noise positive supply voltage. Now, it is possible to provide a similar level of performance for a negative supply. Figure 1 shows a typical application for the LT1964, a new negative low dropout regulator in a 5-lead SOT-23 package. The LT1964 provides the lowest noise available from any negative LDO and it is a micropower device. The LT1964 incorporates features that make it useful for a variety of applications. It is stable with a wide range of output capacitors with an ESR in the range of only a few milliohms up to 3Ω. Small ceramic capacitors can be used without the addition of ESR as is common with other regulators. The output capacitor can be as low as 1µF to maintain a stable output. For low noise operation, the addition of a small bypass capacitor from the output to the BYP pin can reduce output voltage noise to $30\mu V_{RMS}$ over the 10Hz to 100kHz range. However, when using a noise bypass capacitor, we recommend using a minimum of 3.3µF of output capacitance.

The LT1964 delivers 200mA of output current at a dropout voltage of 340mV, making it suitable for many portable designs. The input voltage can range from –2V to –20V, allowing for a wide range of input supplies. The low 30µA operating quiescent current is ideal for battery-powered applications. Quiescent current is well controlled; it does not rise excessively in dropout as happens with many competing regulators. The LT1964 also provides a low power shutdown state: with the shutdown pin pulled to ground, the output is turned off and quiescent operating current is reduced to 3µA. The shutdown pin is bidirectional. Pulling the shutdown pin below –2.1V or above +1.6V will turn the LT1964 on, providing a regulated output. This bidirectional shutdown logic permits easy interfacing to either positive or negative logic, allowing the shutdown pins of both positive and negative supplies to be driven together for easy system management. Figure 2 shows the operational status of the LT1964 based on the shutdown pin voltage. If the shutdown pin is unused, it should be tied to the input to ensure normal operation.

The LT1964 provides many protection features that ease design headaches. The output of the LT1964 can be pulled above ground by several volts without damage; it can be pulled 20V above the input and still allow the device to start and operate. With the input open circuit or grounded, the output of a fixed voltage LT1964 acts like a large resistor, typically 500kΩ or higher, while adjustable LT1964 devices act like an open circuit, with no current flow into the pin. When the input is powered by a voltage source, the output will sink up to the short-circuit current of the device and protect itself by thermal limiting. Like other IC power regulators, the LT1964 provides safe operating area protection. This protection activates at input-to-output differentials greater than –7V, decreasing current limit as the differential increases and keeping the power transistor inside a safe operating region.

The LT1964 is available as a fixed –5V regulator and as two different adjustable versions with a reference voltage of –1.22V. The LT1964-5 brings out all functions, while the addition of the adjust pin on the other versions necessitates sacrificing one of the two functions. For the LT1964-SD, the BYPASS pin is not connected, while the SHUTDOWN pin is brought out. This allows the regulator to be operated normally, with the exception that lowest noise operation cannot be achieved. For the LT1964-BYP, the SHUTDOWN pin has been tied inter-

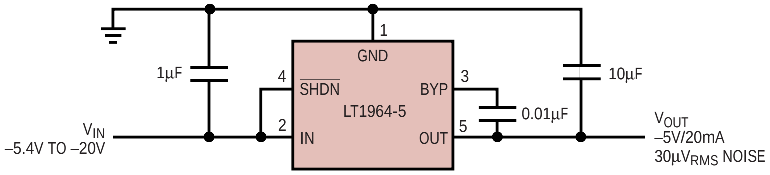

Figure 1. Low noise negative regulator—typical application

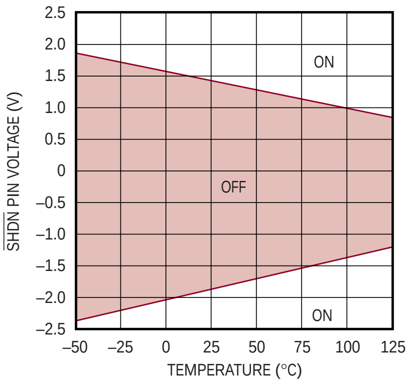

Figure 2. $\overline{SHDN}$ pin thresholds

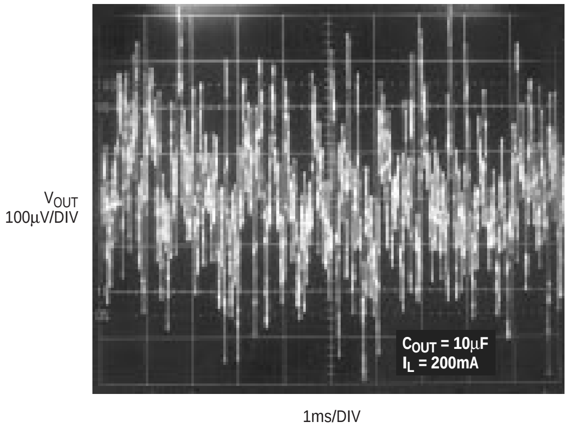

Figure 3. LT1964-5, 10Hz to 100kHz output noise, C_{BYP} = 0

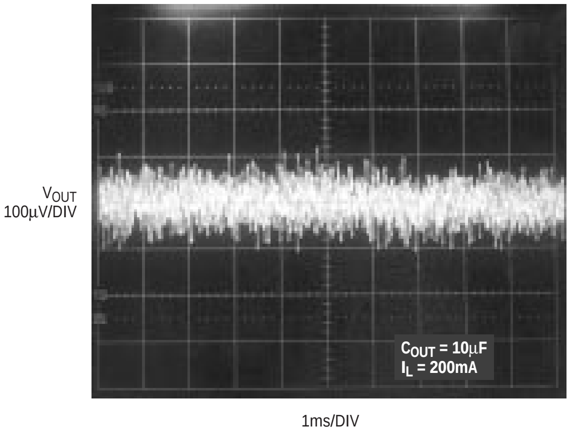

Figure 4. LT1964-5, 10Hz to 100kHz output noise, C_{BYP} = 0.01µF

nally to the input while the BYPASS pin is brought out to allow for low noise operation with the addition of a small reference bypass capacitor.

Measuring Performance

Determining LDO performance is often quite straightforward. Most characteristics are simple to define, with easily obtainable measurements that can be made with DC testing, or pulsed testing to limit power dissipation. Establishing and verifying low noise performance can be quite tricky, particularly when dealing with ultra-low noise outputs. Linear Technology strives to provide accurate, relevant data to customers regarding noise performance. For detailed information on measuring output voltage noise, see Linear Technology Application Note 83, “Performance Verification of Low Noise, Low Dropout Regulators.”

When low noise operation is critical, the small reference bypass capacitor provides a significant reduction in output noise. Figures 3 and 4 show the output of the LT1964-5 both with and without the low noise reference bypass capacitor. The LT1964 was tested with 10µF X5R ceramic capacitors on both the input and output, with a 0.01µF used for the reference bypass. Figure 5 shows noise spectral density of the LT1964-BYP and LT1964-5 as varying amounts of reference bypassing is added. Tests were done using a full 200mA load to provide worst-case operating conditions. Four D-cell batteries provided the input voltage to avoid issues with input supply noise feeding through to the output and corrupting noise measurements. This caveat is one that must be considered whenever designing in any low noise linear regulator; devices do not have infinite power supply rejection and will pass through some portion of input ripple to the output. Additionally, care must be exercised with layout and shielding considerations. Proximity to noisy signal traces can induce unwanted crosstalk that can masquerade as increased output voltage noise.

When specifying a regulator for a power supply design, the LT1964 can provide obvious advantages over the competition. The LT1964 can provide lower dropout, lower quiescent current, lower noise, and many other qualities that other regulators lack. All of these characteristics may not be critical to a design, but when any one or two are, the LT1964 becomes an obvious choice.

Applying the LT1964

One of the best uses for the LT1964 is to pair it with the LT1761. Both devices are micropower (LT1761: 20µA I_Q, LT1964: 30µA I_Q), low dropout (LT1761: 300mV at 100mA, LT1964: 340mV at 200mA), low noise (LT1761: $20\mu V_{RMS}$, LT1964: $30\mu V_{RMS}$) regulators in 5-lead SOT-23 packages. Figure 6 shows a ±5V low noise supply designed with both devices. Input,

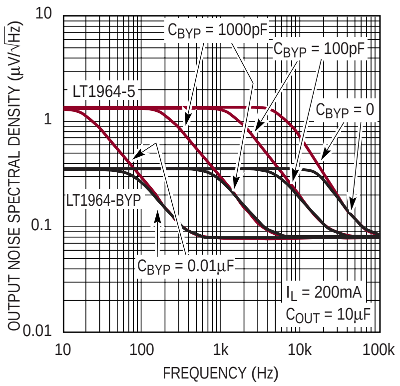

Figure 5. Output noise spectral density

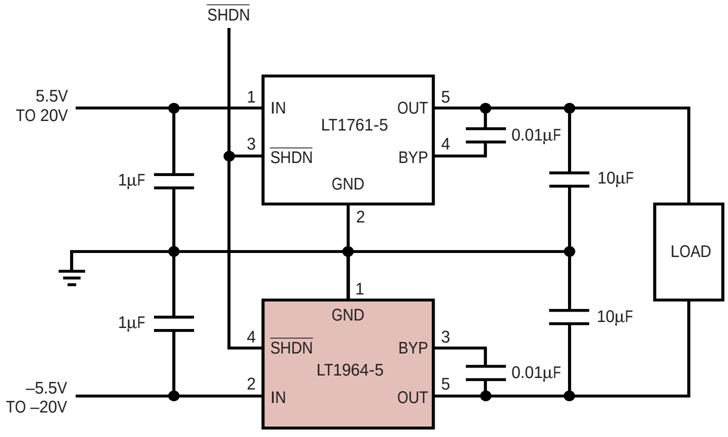

Figure 6. Logic-controlled ±5V low noise supply

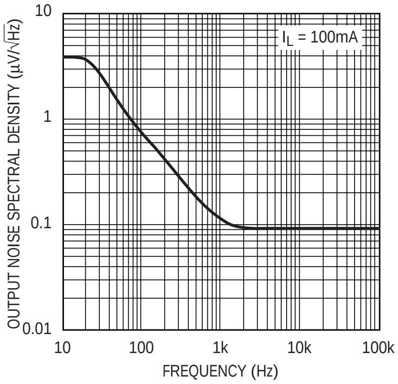

Figure 7. Low noise supply, output noise spectral density

output and reference bypass capacitors are similar on both sides of ground, making for a small bill-of-materials when building a board. Logic control for shutdown of both regulators allows for the shutdown pins of both regulators to be tied together. Pulling the shutdown to ground shuts off both devices and limits total quiescent current to only a few microamperes. With the shutdown pin pulled above 2V, both devices turn on and begin supplying power to the load.

This low noise supply has a good deal of functionality, while leaving little out. One item that is left out is protection diodes, particularly on the outputs of the devices. Many older regulators require reverse protection diodes on the output to prevent the output of the positive regulator from being dragged negative, or vice-versa. Both the LT1761 and LT1964 are designed to allow their respective outputs to be pulled to the wrong side of ground and still allow the parts to start and operate. This is quite useful with a common mode load, such as is shown in Figure 6. The circuit operates with only $40\mu V_{RMS}$ (in the 10Hz to 100kHz bandwidth) of noise, sufficiently quiet for noise-sensitive instrumentation, such as high bit-count A/D and D/A circuits. RF amplifiers will find a minimum amount of power in unwanted sidebands, improving circuit performance.

The performance of this supply is detailed in Figures 7 and 8. Figure 7 shows the spectral noise density seen across the common mode load, whereas Figure 8 shows the peak-to-peak noise on the common mode load. The levels of noise correspond with what would be expected for the sum of the noise from the outputs of the two regulators. Total RMS noise is about $40\mu V_{RMS}$, which is approximately equal to the RMS sum of the output noise of both regulators. Maximum load from the positive side is 100mA, and maximum from the negative is 200mA. Both inputs enter dropout at approximately 300mV above the regulated output voltage at maximum load current, maximizing battery lifetime. Dropout voltage is lower at lighter load currents. Quiescent current is well controlled in dropout, not rising as is common with many other linear regulators. Usually one characteristic of a regulator is not enough to satisfy design requirements. The LT1761 and LT1964 both try to meet any and all needs.

Conclusion

Capable of providing 200mA of output current at 340mV of dropout, the LT1964 draws only 30µA of quiescent current, dropping to 3µA in shutdown. Its small size and ability to work with small, low cost components facilitate portable power supply design. A bidirectional logic shutdown pin allows easy interfacing with existing positive regulators without adding extra external components.

The LT1964 rounds out the offering of low noise regulators from Linear Technology. These regulator families provide a wide range of output currents with low dropout voltage and ultralow output voltage noise. The quiet output is the result of a carefully designed circuit that works with a wide range of external passive components, allowing for a low cost, tightly spaced design. Designing a low noise supply for a new design is no longer a headache.

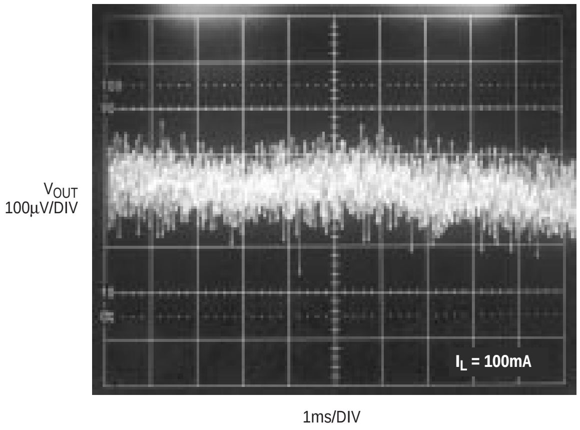

Figure 8. Low noise supply 10Hz to 100kHz output noise

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No Space? No Problem for these Tiny, Inductorless, Efficient, Low Noise, 1.8V and 1.5V, Step-Down DC/DC Converters

by Bill Walter

Introduction

The proliferation of portable devices with ever increasing functionality has imposed a higher demand on power conversion circuitry, with a continued emphasis on maximizing battery life while reducing board real estate. The new LTC1911 Step-Down DC/DC converter helps designers make extremely small conversion circuits while maintaining the high efficiencies needed to extend battery life. The LTC1911 saves space by operating at high frequency, allowing the use of tiny low cost ceramic capacitors—no inductors required. The LTC1911 also comes in a low profile (1.1mm) MSOP-8 package. Figure 1 shows just how small the conversion circuit can be—a complete converter takes less than 0.08in^2 of board space. Its small size and efficiency make it well suited for single cell Li-Ion as well as 3-cell NiMH/NiCd battery powered applications.

The LTC1911-1.8 and LTC1911-1.5 are switched capacitor step-down DC/DC converters that provide 250mA of output current at 1.8V and 1.5V, respectively, with a tolerance of ±4%, from a single 2.7V to 5.5V supply. To achieve high efficiency over the entire input range, the LTC1911 uses three possible switched capacitor fractional conversion modes: 2-to-1, 3-to-2 or 1-to-1 step-down mode. Internal circuitry selects the step-down conversion mode to optimize efficiency and ensure output regulation as the input supply voltage and output load conditions vary. A single input and output capacitor, as well as two external flying capacitors are all that is needed to operate in all three modes. The typical LTC1911 efficiency is over 25% higher than that of a linear regulator.

The LTC1911 also has a Burst Mode function that delivers a minimum amount of charge for one cycle then goes into a low current state until the output drops enough to require another burst of charge. Burst Mode® operation allows the LTC1911 to achieve high efficiency even at light loads. An output current sense circuit is used to detect when the required output current drops below about 30mA. When this occurs, the oscillator shuts down and the part goes into a low current operating state. The LTC1911 will remain in the low current operating state until the output has dropped enough to require another burst of current..

In the case of traditional charge pumps the amount of current delivered during a burst cycle is a function of many factors such as supply voltage, switch strength and capacitor selection. For this reason the output ripple voltage of a traditional charge pump can vary widely under light loads and it is not uncommon to have a couple hundred millivolts of output ripple under worst case conditions. In contrast, the amount of current delivered during the burst cycle of the LTC1911 is a function of burst threshold, which is essentially constant over all conditions. Therefore the peak-to-peak output ripple voltage of the LTC1911 will also remain essentially constant, and is only about 5mV$_{P-P}$ for a 10µF output capacitor.

Low Noise

The LTC1911's constant frequency architecture (patent pending) not only provides a low noise regulated output, but also has lower input noise than conventional switched capacitor charge pump regulators. Regulation is achieved by sensing the output voltage and regulating the amount of charge transferred per cycle. This method of regulation provides much lower input and output ripple than that of conventional switched capacitor charge pumps. Charge transfer in the LTC1911 is at a constant, high frequency making it easy to filter input and output noise. Conventional switched capacitor charge pumps, like those used in most other regulators with burst operation, are much more difficult to filter because they operate over a range of frequencies that covers several orders of magnitude. Figure 2 shows the ripple voltage of the LTC1911 output for all 3 switching

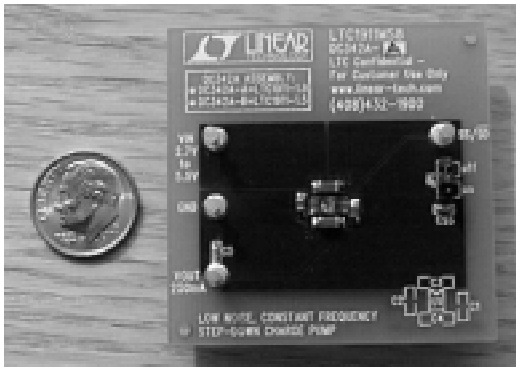

Figure 1: Space is no problem for this complete DC/DC coverter.

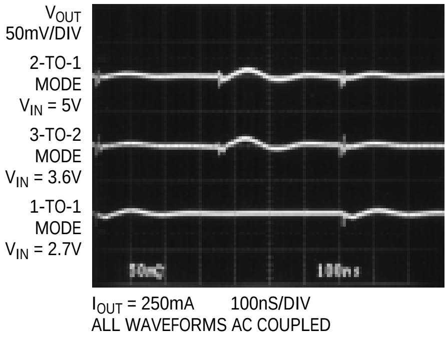

Figure 2. Output voltage ripple

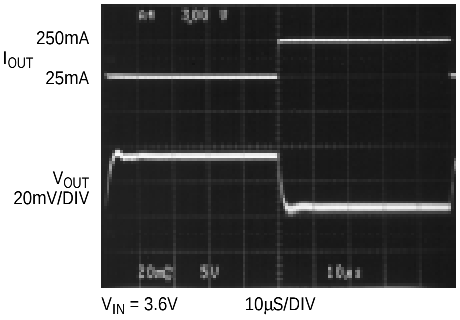

Figure 3. Output current transient response

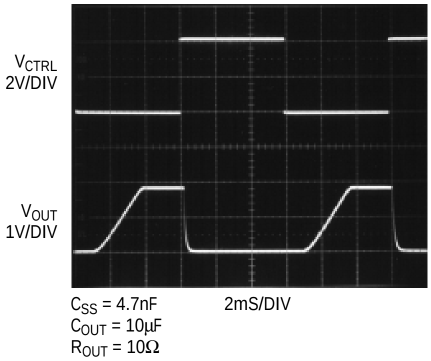

Figure 4. Soft-start operation

modes of operation with a 250mA output load.

Fast Transient Response

In addition to low output noise, the LTC1911 provides exceptional transient recovery. Figure 3 shows the LTC1911 recovery from a fast (<1µs) near full-scale (25mA to 250mA) load transient. The LTC1911 recovers in only 5µs, with very little overshoot, or undershoot.

Short-Circuit and Thermal Protection

The LTC1911 has built-in short-circuit current limiting as well as over temperature protection. During a short-circuit condition the part automatically limits the output current to approximately 600mA. The LTC1911 shuts down and stops all charge transfer when the IC temperature exceeds approximately 160°C. Under normal operating conditions, the part should not go into thermal shutdown but the function is included to protect the IC in cases of excessively high ambient temperatures, or in cases of excessive power dissipation inside the IC (i.e., overcurrent or short circuit). The charge transfer will reactivate once the junction temperature drops back to approximately 150°C. The LTC1911 can cycle in and out of thermal shutdown indefinitely without latch-up or damage until the fault condition is removed. To keep the LTC1911 running cool, the IC is housed in a thermally enhanced MSOP-8 package, with the lead frame of the IC connected to ground (pin 4).

Soft-Start and Shutdown Operation

The SS/$\overline{\text{SHDN}}$ pin is used to implement both low current shutdown and soft-start. Forcing a voltage lower than 0.6V on the SS/$\overline{\text{SHDN}}$ pin will put the LTC1911 into shutdown mode. Shutdown mode disables all control circuitry and forces the output into a high impedance state. A 2µA pull-up current on the SS/$\overline{\text{SHDN}}$ pin will force the part into active mode if the pin is left floating or is driven with an open-drain output that is in a high impedance state. If the pin is not driven with an open-drain device or floating, it must be forced to a logic high voltage of 2.2V (min) to ensure proper output regulation.

A known issue with conventional charge pumps is that the initial inrush of current required to charge the output capacitor to regulation can cause undesirable transients on the input supply during power on. The soft-start feature limits inrush currents required to charge the output capacitor, thereby minimizing input supply transients caused by the power on phase of the IC. To implement soft-start, a capacitor is connected to the SS/$\overline{\text{SHDN}}$ pin. An open-drain device can also be connected from the SS/$\overline{\text{SHDN}}$ pin to GND to implement shutdown. Once the open-drain device is turned off, the 2µA pull-up current will begin charging the external soft-start capacitor and force the voltage on the pin to ramp towards V_{IN}. As soon as the shutdown threshold is reached (0.6V typical), the internal reference voltage that controls the output regulation point will follow the ramp voltage on the SS/$\overline{\text{SHDN}}$ pin until the reference reaches its final band gap voltage. This occurs when the voltage on the SS/$\overline{\text{SHDN}}$ pin reaches approximately 1.9V. Since the ramp rate on the SS/$\overline{\text{SHDN}}$ pin controls the ramp rate on the output, the average inrush current can be controlled through the selection of soft-start capacitor (C_{SS}) and the output capacitor. For example, a 4.7nF capacitor on SS/$\overline{\text{SHDN}}$ results in a 3ms ramp time from 0.6V to 1.9V on the pin. If the output capacitor is 10µF, the 3ms output ramp time results in an average output capacitor current of only 6mA which translates directly into 6mA of input current. Figure 4 shows a scope photo of the output ramping up following an open drain device going into high impedance.

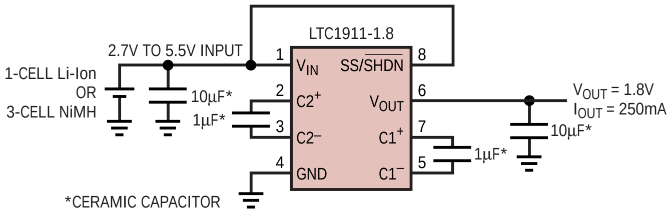

Figure 5. Single cell Li-Ion to 1.8V DC/DC converter

continued on page 29

Simple and Efficient Way to Provide Three Supply Voltages for Small TFT LCDs

by Bryan Legates

TFT LCDs used in portable devices today typically need three different supply voltages: 5V, 15V, and –10V. One way to generate these three voltages is to use a single DC/DC converter and a large number of external components, but this results in mediocre line and load regulation. The LT1944-1 dual micropower DC/DC converter simplifies LCD power supply design by generating three well-regulated output voltages using a small number of external components. Both DC/DC converters in the LT1944-1 use a constant-off-time Burst Mode® control scheme to ensure high efficiency at very light load currents. The two converters are independently optimized for high and low step-up ratios: the first converter generates –10V and 15V using a switch current limited at 100mA with a 400ns off-time, while the second converter generates 5V using a switch current limited to 175mA with a 1.5µs off-time. The longer off-time of the second converter ensures a well-controlled inductor current for applications where the step-up ratio is low (i.e. in a Li-Ion to 5V converter or a 2-cell alkaline to 3.3V converter).

The circuit shown in Figure 1 generates three output voltages from a single Li-Ion battery. This power supply can provide 5V at 30mA, 15V at 2.5mA, and –10V at 1mA, making it ideal for the small LCDs found in cellular phones and handheld computers. If needed, the –10V output can be easily changed to a –15V output by connecting the cathode of diode D3 to ground instead of to the 5V output. The LT1944-1 operates from an input voltage of 1.2V to 15V and is capable of producing output voltages up to ±35V, making it a good choice for a wide variety of applications needing multiple output voltages.

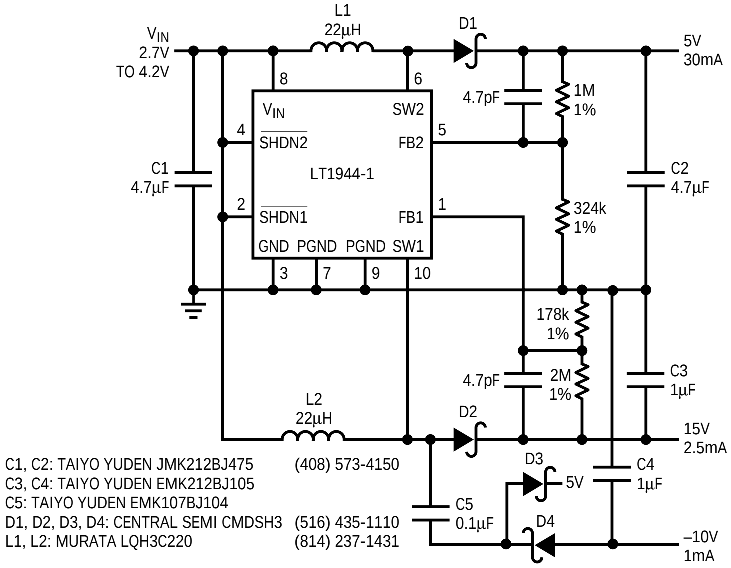

Figure 1. Triple output power supply for LCDs

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Fiber Optic Communication Systems Benefit from Tiny, Low Noise Avalanche Photodiode Bias Supply

by Michael Negrete

Avalanche photodiodes (APDs) are the photo detector of choice for long-haul fiber optic communication systems because of their high sensitivity and high internal gain. An important characteristic of APDs is that their internal gain is optimal when there is a high voltage reverse bias (30V to 90V) across the APD. Nevertheless, the high gain is all for naught if the sensitivity of the APD is compromised by a noisy bias supply.

Traditionally, such low noise bias supplies required custom circuits that brought with them another problem: large space requirements. Linear Technology's LT1930A 2.2MHz step-up DC/DC converter in a 5-lead SOT-23 package solves these APD bias voltage problems and does so in a compact package suitable for most fiber optic applications.

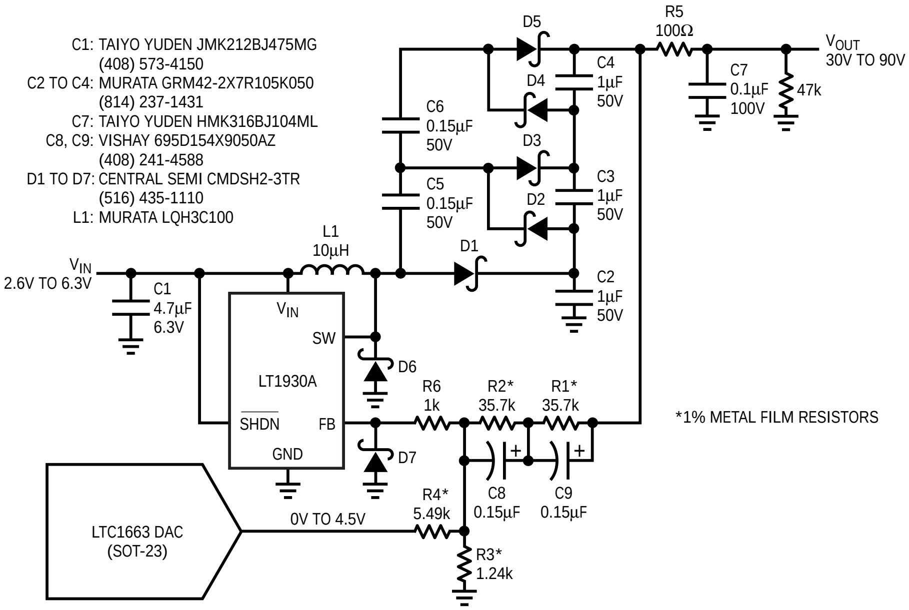

Figure 1. LT1930A-based boost regulator produces 30V to 90V for avalanche photodiode bias supplies with only 200µV_{P-P} noise.

The LT1930A, a capacitor-diode tripler and an external DAC provide a bias voltage of up to 90V, allowing easy temperature compensation (via the DAC) to optimize internal gain. By running the IC at a switching frequency of 2.2MHz, one can use tiny, low cost capacitors and inductors to keep the circuit footprint under 0.5in^2. The LT1930A's constant frequency PWM operation keeps output noise low and easy to filter.

Figure 1 shows a high voltage, low noise APD bias supply that works from an input range of 2.6V to 6.3V. The DAC, driven from a processor, adjusts the output from 30V to 90V to compensate for temperature dependent APD gain fluctuations. The LT1930A includes a 35V switch making it capable of producing 105V output through a capacitor-diode tripler.

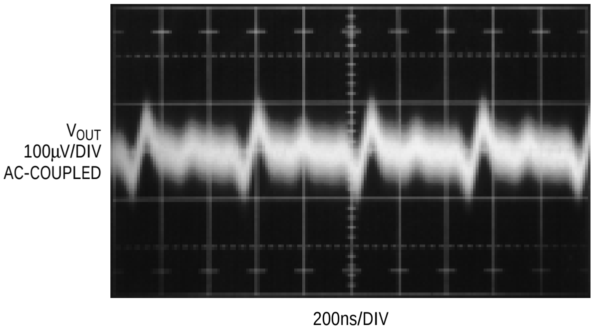

Figure 2. 50V Avalanche photodiode bias shows 200µV_{P-P} ripple and noise, improving fiber optic receiver sensitivity.

To eliminate noise from the internal reference and error amplifier, two 0.15µF tantalum feedback capacitors are used in series. A series connection ensures a sufficient voltage rating of the feedback capacitance. Ceramic feedback capacitors have a piezoelectric response to temperature and low frequency vibrations under 1kHz, which is amplified by the LT1930A internal error amplifier. These should not be used unless noise in that bandwidth is acceptable. To protect the switch pin from negative voltage swings, a clamping diode is tied to ground. An identical diode is placed at the feedback (FB) pin, along with a 1k resistor to protect the part from a sudden short in the load, which would force the feedback capacitor's negative side to the negative value of the output voltage. All other capacitors can be ceramic, which are small and capable of handling the high voltages of the regulator.

Figure 2 shows the AC coupled noise of a 50V output with a 5V input. The switching noise is less than $200\mu V_{P-P}$, allowing greater sensitivity and dynamic range than most APD bias solutions. Oscilloscope measurement bandwidth is 100Hz to 10MHz, all probe cables are coaxial and special attention is given to grounding.[1]

Conclusion

The LT1930A exceeds all of the stringent demands of an APD reverse-bias voltage, eliminating the need for custom APD bias supplies. The LT1930A solution not only provides the cleanest output in the industry for APDs, but also achieves this in a fraction of the space required by other solutions.

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[1] Discussion of low noise measurement issues is available in "A Monolithic Switching Regulator with 100µV Output Noise," Linear Technology Corporation, Application Note 70 by Jim Williams.

LTC1911, continued from page 26

Applications

Figure 5 shows an application for the LTC1911-1.8V. Here the SS/$\overline{\text{SHDN}}$ pin has been connected to the input supply, thus disabling the soft-start function. In this application the output will come up immediately when the supply is applied. This application is good for users who are not worried about slight transients on the input supply caused by the IC turning on, and don't need the shutdown feature. Here, shutdown is effectively achieved by removing the input supply.

Figure 6 shows an application for the LTC1911-1.5V. Here the SS/$\overline{\text{SHDN}}$ pin is connected to a soft-start capacitor and an open drain device. This application allows the user full access to the shutdown function as well as soft-start to limit the inrush current at power on or coming out of shutdown. The open drain device can be omitted for users who only wish to limit the inrush current, but do not need the shutdown feature of the part.

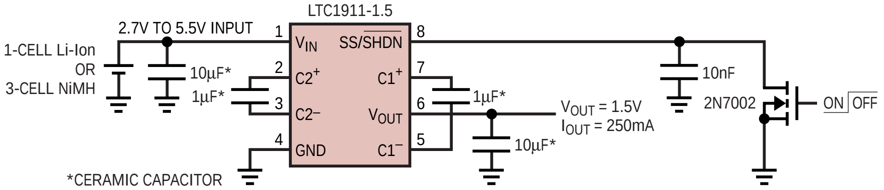

Figure 6. DC/DC converter with shutdown and soft-start

Conclusion

The LTC1911-1.8 and LTC1911-1.5 are well suited for medium to low power step-down applications with tight board space requirements. These low noise step-down DC/DC converters can deliver 250mA of output current and provide efficient operation over the input voltage range of 2.7V to 5.5V. Both parts come in the thermally enhanced MSOP-8 packages. The LTC1911 keeps external components to a minimum, requiring only four or five inexpensive external capacitors, helping designers meet the tightest space requirements. LTC1911 is a good match for single cell Li-Ion as well as 3-cell NiMH/NiCd battery powered applications.

LTC1851, continued from page 8

shutdown modes and retain the stored program. The user can run a programmed sequence, interrupt and take direct control of the MUX or shut the converter down and then return to the programmed sequence. Any edge of M1 or M0 will reset the counter and/or pointer so that Scan Mode always starts at MUX address 000 and the sequencer always starts at location 0000.

Conclusion

The LTC1851 has everything you've ever wanted from a Multiplexed ADC. It has a programmable input MUX and sample-and-hold that can handle single-ended, differential, unipolar or bipolar inputs. It has a flexible reference that offers three internal ranges and two options for using an external reference. The ADC is a low power, high performance 12-bit, 1.25Msps converter. The three operational modes make it easy to use in the simplest applications but powerful enough to solve your toughest problems. Stop adapting your inputs to the ADC and start using an ADC designed to adapt itself to your inputs and your application.

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Reduce Power Consumption of DSL Modems with the LT1969 Line Driver

by Tim Regan

Introduction

The LT1969 is an ADSL line driver ideally suited for CPE modem designs, with the added feature of programmable operating current. With a minimum output current capability of ±200mA and a wide 700MHz gain-bandwidth product, the LT1969 is suitable for placing any standard ADSL signal with up to 13dBm of RMS power onto a 100Ω phone line. The part is housed in a very small MS-10 package; the two additional package pins are employed to program the operating current of the driver stage.

One of the biggest headaches in the implementation of DSL modems is the total power consumption of the system. Although the DSP and analog front end (AFE) ASICs use much of the power, a significant amount is also dissipated by the line-driver stage. The driver stage must have large enough power supply rails to prevent clipping of the peaks of the DMT signal in ADSL or the PAM signals of HDSL2. These peaks can be four to six times the normally transmitted RMS signal. The quiescent biasing current of the amplifiers times the increased power supply voltage level sets the minimum power consumption of the driver stage, even when no signal is being transmitted.

This issue becomes a major concern in central office DSL designs where multiport cards are required. It is less of a problem on the CPE end of the connection where the power dissipation of just a single modem or port can be tolerated. However, as the deployment of DSL into the office environment expands, multiport CPE boxes face the same cumulative power consumption issue. Any techniques that reduce power consumption and power dissipation are most welcome by the power supply and thermal management engineers producing multiport DSL line cards.

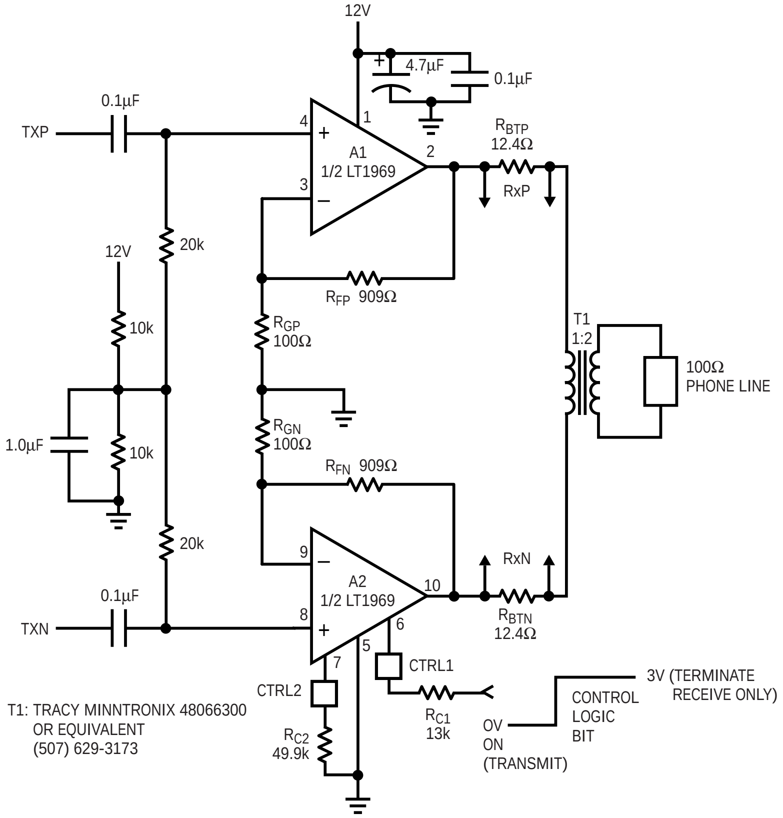

Figure 1. CPE ADSL line driver with operating current control

Adjust Transmit Driver Quiescent Current and Receiver Line-Terminate Bias Current

Two control pins (pins 6 and 7) are available on the LT1969 to set the operating current of the driver (Figure 1). Both of these pins are biased internally to approximately 1VDC above the V^- supply rail (pin 5). Resistors connected between these two pins and V^- set the driver stage operating current. The intended operation of the LT1969 is to fix the minimum operating current with one of the resistors in order to maintain low driver output impedance when not transmitting signals. This maintains termination of the transformer back-termination resistors so that signals received from the telephone line can still be developed across these resistors and detected by the receiver circuitry. Fixed resistor R_{C2}, connected from CTRL2 to V^-, sets the minimum operating current. The total supply current of the driver amplifiers is approximately 150 times the total current flowing out of the two control pins. An R_{C2} value of 49.9k sets 20µA of control current resulting in a minimum total driver supply current of 3mA (1.5mA per amplifier). Figure 2 illustrates the output impedance of each driver amplifier vs the programmed supply current. At 1.5mA per amplifier of supply current, the output impedance is less than 1Ω, which allows received signals

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LTC1705: 2-Step Voltage Conversion Reduces Size and Heat in Notebook Computer Supply

by Haresh Patel

Linear Technology's LTC1705 is the most integrated CPU core, I/O and clock supply solution for Intel's mobile Pentium® III microprocessor. This chip is a part of a "2-step" conversion architecture. 2-step conversion uses a primary regulator to convert the input power source (Li-Ion batteries) to 5V. This 5V supply is down-converted to provide a lower processor core voltage, I/O and clock supply by the LTC1705. Each regulator in a 2-step system maintains a relatively low step-down ratio (5:1 or less), running at high efficiency while maintaining a reasonable duty cycle (V_O/V_{IN}). In contrast, a single-step conversion from a high input voltage to a 1.xV output must operate at a very narrow duty cycle, mandating trade-offs in external component values while compromising efficiency and transient response.

2-step regulation can also buy advantages in thermal management. In a typical microprocessor core supply regulator, the DC/DC controller is

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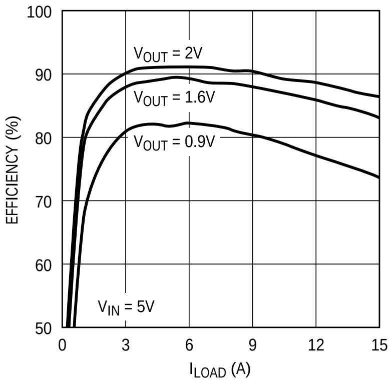
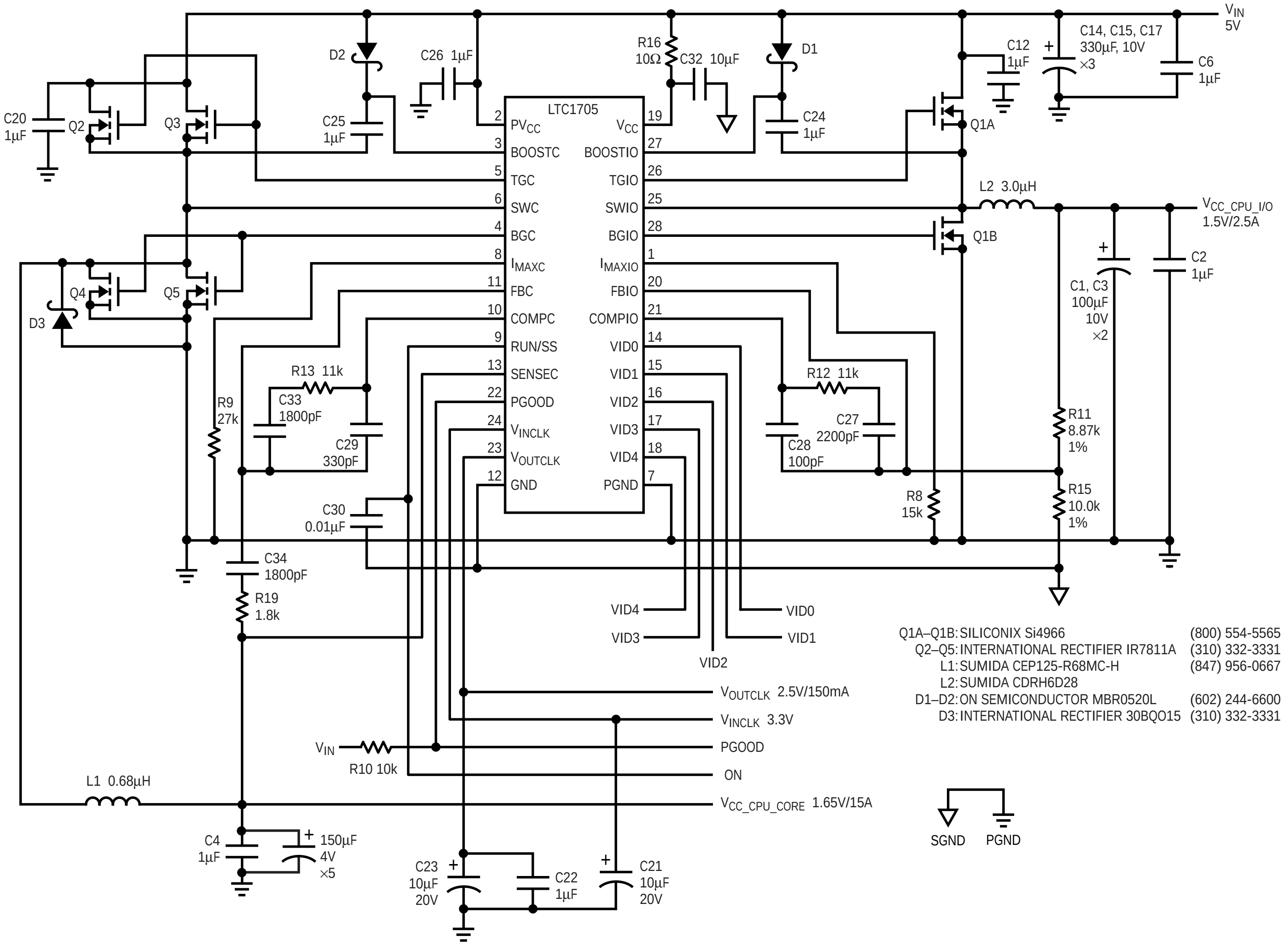


Figure 2. LTC1705 typical efficiency for various output voltages



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Q2–Q5:	INTERNATIONAL RECTIFIER IR7811A	(310) 332-3331
L1:	SUMIDA CEP125-R68MC-H	(847) 956-0667
L2:	SUMIDA CDRH6D28	
D1–D2:	ON SEMICONDUCTOR MBR0520L	(602) 244-6600
D3:	INTERNATIONAL RECTIFIER 30BQ015	(310) 332-3331

Figure 1. LTC1705 typical application for mobile Pentium III processor

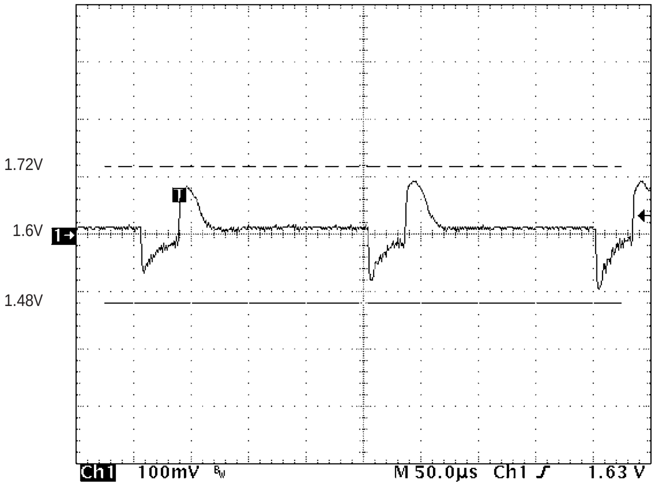


Figure 3. Transient response of Figure 1's circuit for a 0A to 14A load step

located next to the CPU. In a 1-step design, all of the power dissipated by the core regulator is located next to the already hot CPU, making thermal management a nightmare. In a 2-step LTC1705 design, a significant percentage of the power lost in the core regulation system occurs in the 5V supply, which is usually located away from the CPU. The power lost to heat in the LTC1705 section of the system is relatively low, minimizing the added heat near the CPU. 2-step solutions using the LTC1705 usually match or exceed the total system efficiency of single-step solutions and provide the additional benefits of improved transient response, reduced PCB area and simplified power trace routing.

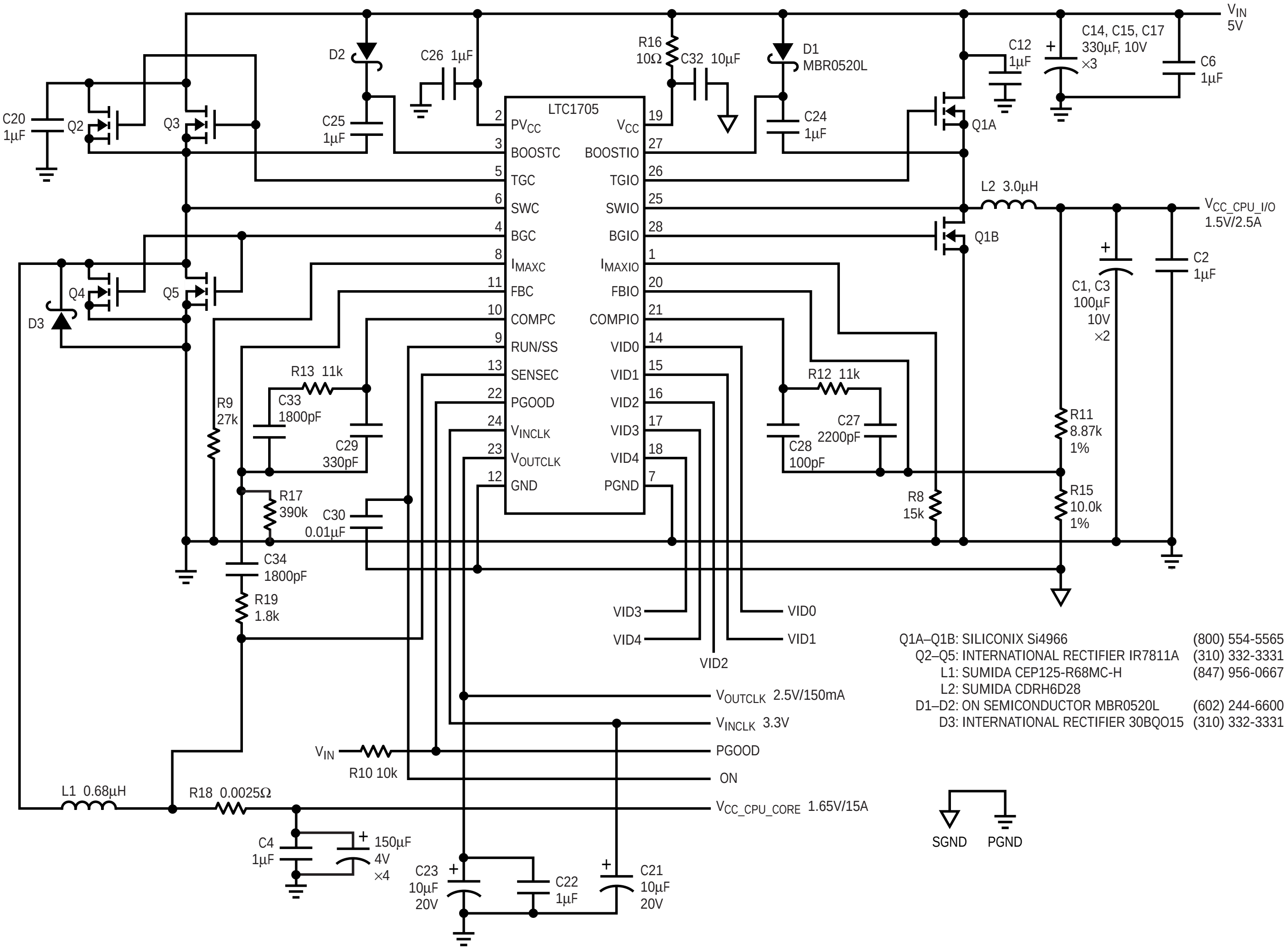


Figure 4. LTC1705 application with an external sense resistor for active voltage positioning

The LTC1705 uses a constant 550kHz switching frequency that allows the use of physically small inductors. The LTC1705 includes two switching regulator controllers, one for the CPU core and one for the I/O, each designed to drive a pair of N-channel MOSFETs in a voltage-mode feedback, synchronous buck configuration. An onboard 5-bit DAC sets the core output voltage according to the Intel mobile VID specification. The IC also includes a low dropout linear regulator (LDO) that delivers more than 150mA of output current for the CLK supply. The LTC1705 also has an open-drain PGOOD pin that indicates when all three outputs are within ±10% of their regulated values.

The circuit in Figure 1 is a typical Intel mobile Pentium III application for the core, I/O and clock supplies. The core voltage is VID controlled and can vary from 0.9V to 2.0V at 18A. The I/O voltage is set for 1.5V at 3A and is programmed by two resistors. The clock voltage is set internally for 2.5V at 150mA. Figure 2 shows the typical core efficiency for various output voltages and Figure 3 shows the core output transient response for a 14A load step.

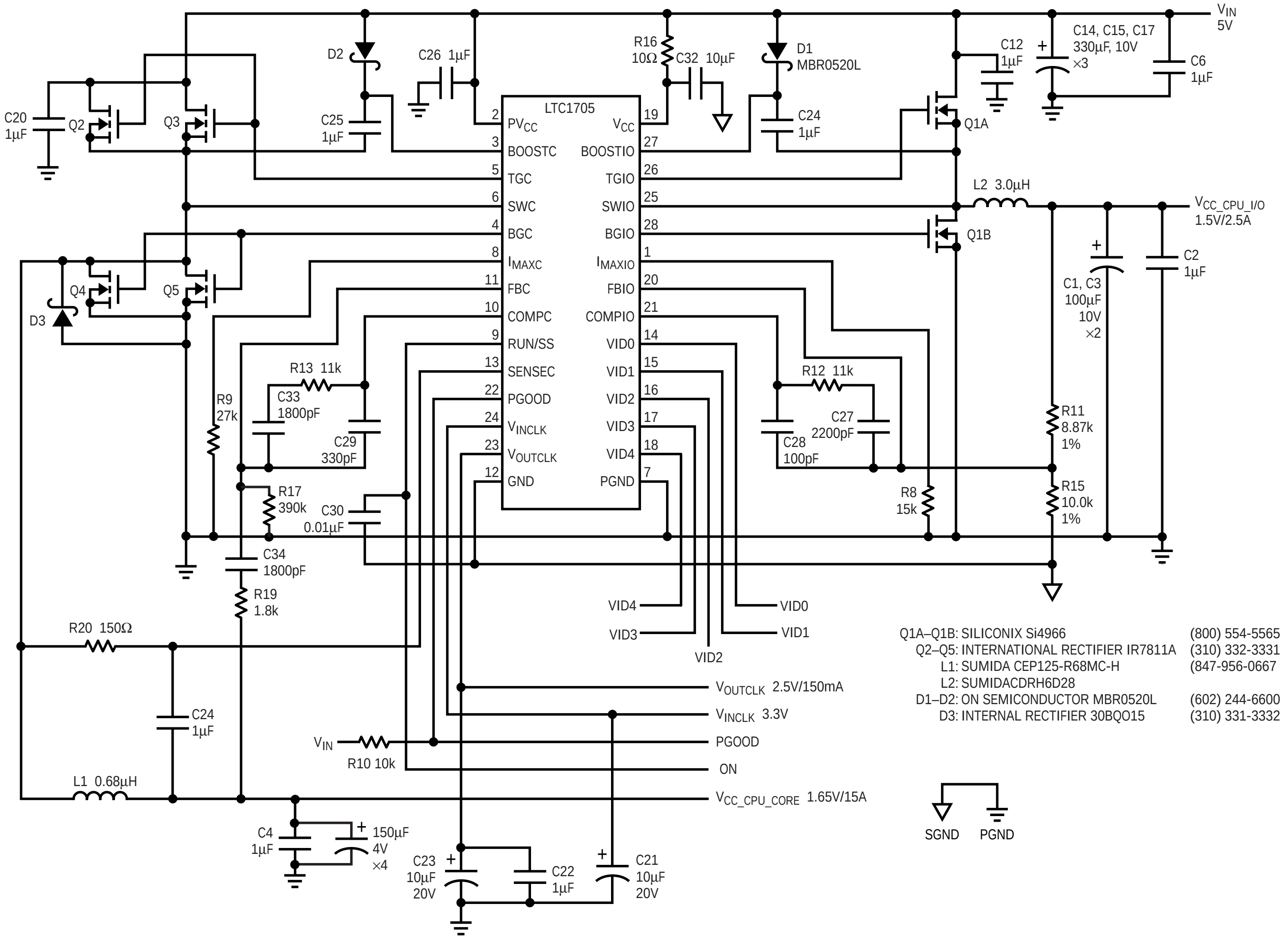
LTC1705 Circuit with Active Voltage Positioning (AVP)

Figures 4 and 5 show two methods of implementing active voltage positioning on an LTC1705 circuit. In Figure 4, the voltage deregulation is set by adding a 2.5mΩ resistor (R18) in the power path. At full load, the output voltage will be less than nominal by $I_{FULL\ LOAD} \cdot 0.0025$. In order to program the output voltage higher than nominal at zero load, a 390k resistor (R17) is added between FB1 and ground. The DC value by which the output voltage increases over nominal can be calculated by the following formula:

$$V_{HIGHER} = (0.8/390k) \cdot 10k \cong 20mV$$

where 0.8 is the feedback voltage and 10k is the top feedback resistor for the LT1705's internal DAC.

In Figure 5, the voltage deregulation is set by the DC resistance of the power inductor L1, which is approximately 2.5mΩ. The SENSE pin of the LTC1705 is connected between R20 (150Ω) and C24 (1µF). R20 and C24, which are connected across the inductor L2, act as a lowpass filter with a time constant of 150µs. Likewise, a 390k resistor is added between



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Q2–Q5:	INTERNATIONAL RECTIFIER IR7811A	(310) 332-3331
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L2:	SUMIDACDRH6D28	
D1–D2:	ON SEMICONDUCTOR MBR0520L	(602) 244-6600
D3:	INTERNAL RECTIFIER 30BQO15	(310) 331-3332

Figure 5. LTC1705 application that uses the resistance of the power inductor for active voltage positioning

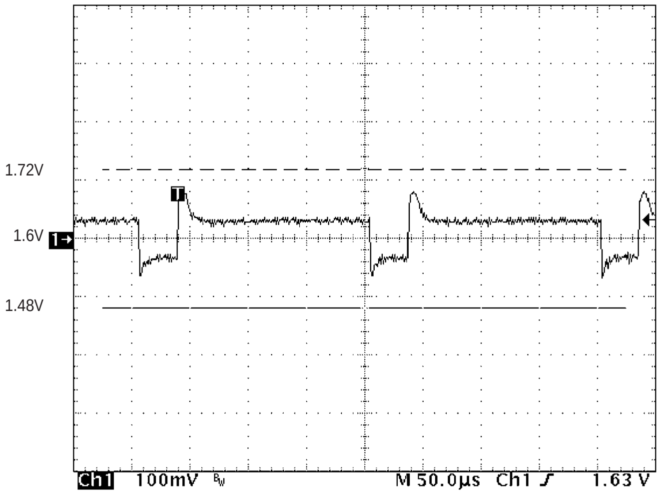

Figure 6. Transient response for Figure 4's circuit with a 0A to 14A load step

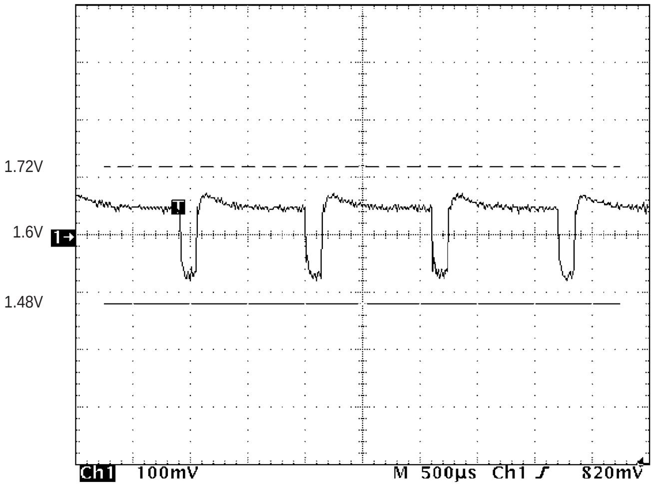

Figure 7. Transient response for Figure 5's circuit with a 0A to 14A load step

FB1 pin and ground. Figures 6 and 7 show the transient response of the LTC1705 circuits in Figures 4 and 5, respectively, for a 0A to 14A transient load step with four 150µF Sanyo POSCAP capacitors.

Conclusion

The LTC1705 minimizes expensive bulk output capacitors by using active voltage positioning (AVP). It also takes advantage of 2-step conversion and the produces the most efficient and highly integrated CPU Core, I/O and clock supply currently available for Intel's mobile Pentium III microprocessor.

LT1969, continued from page 30

to be developed across the 12.4Ω back-termination resistors. This is the line-terminate mode of operation, in which the line drivers consume only 36mW of power from a single 12V power supply.

During "Show Time," when the modem is communicating with the central office, the line driver needs more biasing current to provide sufficient bandwidth, slew rate and output current for distortion-free placement of the transmitted signal on to the phone line. This is where the second controlling pin is used. Referring again to Figure 1, the CTRL1 input pin is connected to a second resistor, R_{C1}, which is driven by a 0V to 3V logic input signal. This logic signal sets the driver into transmit mode or terminate mode. When taken high (greater than 1.2V more positive than V^- of the driver), no current flows out of the CTRL1 pin, leaving the supply current to be set only by the CTRL2 pin. When taken low, to a potential equal to V^- of the driver (which, in this case, is ground), resistor R_{C1} (13k) effectively parallels R_{C2} (49.9k), producing a total control resistance of 10.3k.

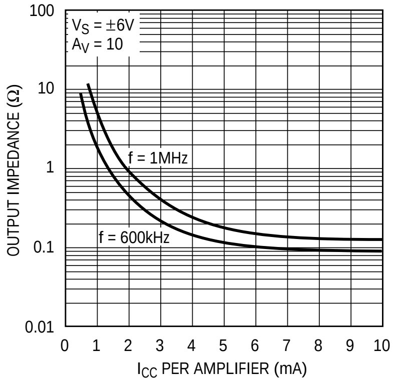

Figure 2. The LT1969 output impedance remains low at reduced operating current.

This increases the total current flowing out of the control pins, thereby increasing the driver supply current for signal transmission duty. A total supply current of 12mA is normally sufficient for distortion-free transmissions of ADSL upstream data.

Conclusion

At this operating level, the quiescent power consumption of the line driver is 144mW when not transmitting. Using the LT1969 and adding simple logic control of the operating current provides 75% power savings in an idle channel. This can really add up in multiport designs. Additionally, the tiny footprint, MS-10 package used for the LT1969 occupies only 50% of the board area of a standard 8-pin surface mount device (S8 package), another benefit for compact multiport designs.

I²C Dual Fan Speed Controller Increases Efficiency and Reduces Noise

by Dilian Reyes

Busy servers and rack-based network and telecom equipment rely on hard-working cooling systems to keep from melting down. The simplest cooling system is a bank of fans running at full tilt, all of the time. This approach ensures a cool environment, but overcompensation is neither efficient, nor is it good for the fans. High output fans that work full time do not last very long (their bearings wear out), are not very efficient (they use power also), and are noisy (especially when their bearings wear out). The LTC1840 dual fan speed controller reduces the wear on bearings, and noise, by continuously adjusting fan speed to match the instantaneous cooling requirements of the system.

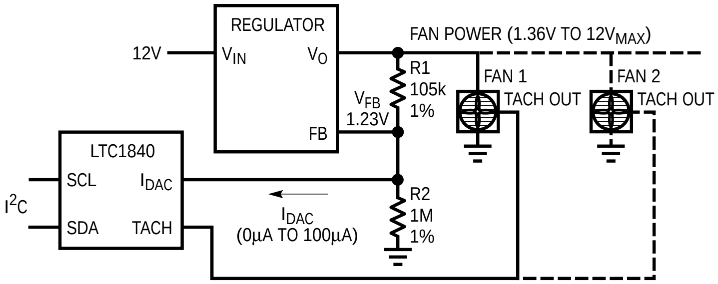

Figure 1. LTC1840 fan speed control block diagram

The LTC1840 monitors and controls multiple fans via an I²C and SMBus compatible 2-wire serial interface. It provides two fan speed control channels, features fan tachometer and fault monitoring, nine slave addresses and four general-purpose programmable I/O pins, all in a convenient 16-pin SSOP package.

Figure 1 shows a block diagram for a fan speed control system using the LTC1840. The LTC1840 contains two current output DACs that control fan speed. The scaled currents individu-

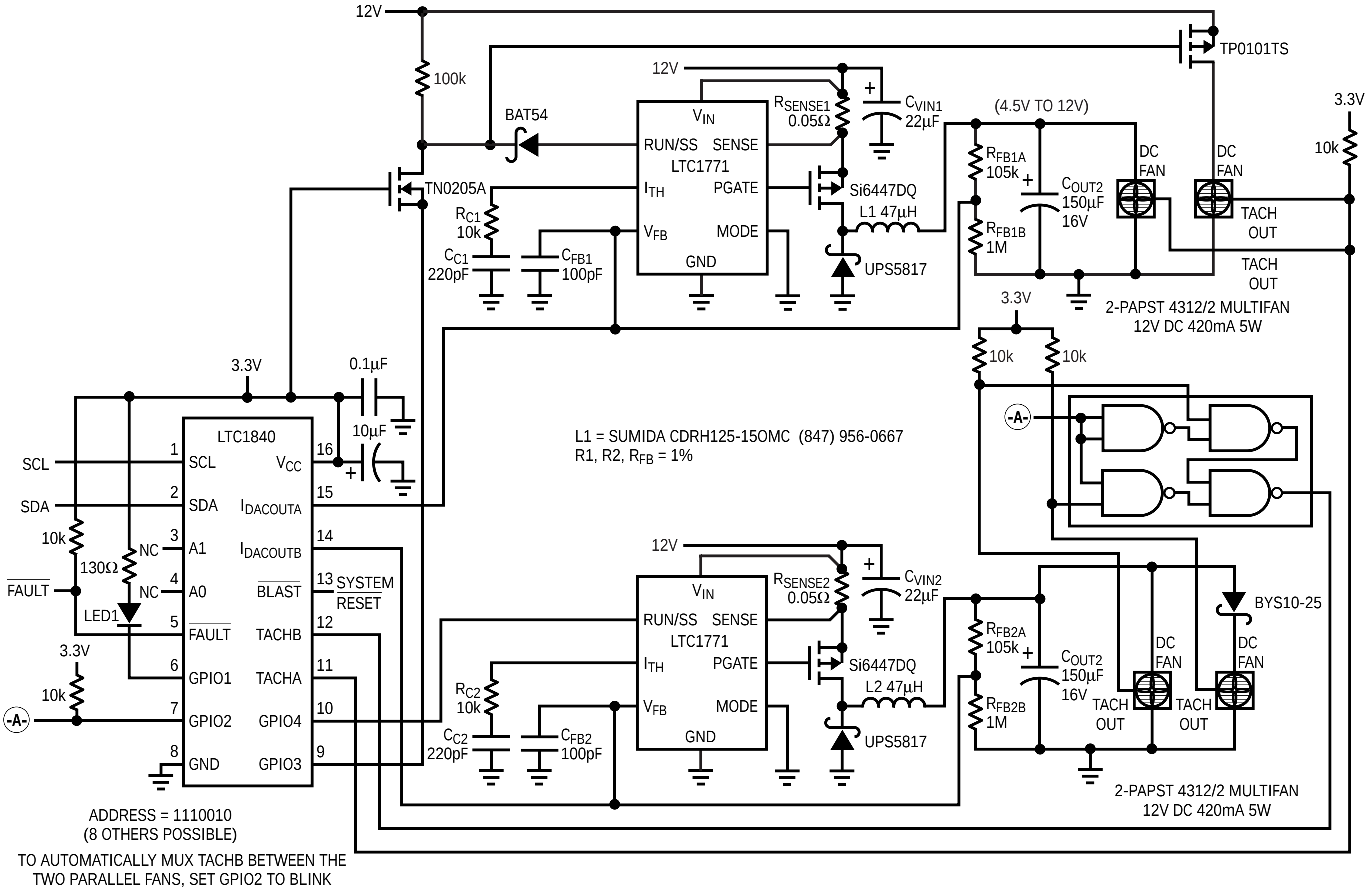

Figure 2. Controlling four fans with the LTC1840

ally adjust the fan-driving output voltage of a switching regulator. V_O increases as the current I_{DAC} is increased under command of the serial interface. The number of fans controlled by one DAC is limited only by the switching regulator output power.

The TACH pin of the LTC1840 monitors the speed of fans that include a tachometer output. Internal logic accumulates a maximum of 255 counts between the fan tachometer's rising edges. The rate of the counter is determined by a divisor (2, 4, 8 or 16 chosen via the serial interface) from the 50kHz internal oscillator. Fans slowing down due to worn bearings or halted from a jam will cause an overflow in the internal counter and a corresponding bit is set low in the fault register. The system controller can then take action, shutting down the faulty fan and summoning maintenance.

The chip contains four general-purpose input/output (GPIO) pins, which are configured independently. As open-drain outputs, they can be set high, low or to pulse at a 1.5Hz rate. The outputs are rated at 10mA sink current so they can drive LEDs. When the GPIO pins are configured as inputs, they can monitor thermal switches, push buttons and the fault or power good outputs of switching regulators and Hot Swap™ controllers. A fault register detects and flags state changes.

Internal data registers are read and programmed via I^2C by specifying device address and register address. DACA and DACB registers control the 100µA current outputs on a 255-step scale. The STATUS register allows the user to enable the TACHA and TACHB fault data and set the divisor for the internal counter frequency. The internal count, which is inversely proportional to tachometer speed, is stored in the TACHA and TACHB registers. Unmasked faults set the FAULT pin high as an instant hardware alert. The GPIO setup and GPIO data registers configure the GPIO pins, assign output and fault status, and read input state.

Continuous System Cooling and Tachometer Monitoring

The circuit in Figure 2 demonstrates the capabilities of the LTC1840. Each of the two LTC1771 high efficiency step-down regulators can supply power for up to four 12V, 420mA fans. As shown, the upper LTC1771 drives a single fan backed up by an idle, redundant fan. In the event the primary fan fails, GPIO3 turns off the LTC1771 and simultaneously activates the backup fan at full speed. These two fans operate one at a time so their tachometer outputs are wired OR, and only one input (TACHA) is required to monitor their speed.

The other two fans are driven in parallel by the second LTC1771 and alternately monitored by TACHB. These fans operate concurrently, so their tachometer outputs are muxed by a quad NAND gate. GPIO2 operates in pulsing mode and serves to clock the mux.

Additional Features

For applications requiring multiple fan controllers, the LTC1840's three-state (high, low, no connect) address programming inputs support nine user-selectable slave addresses. The $\overline{\text{FAULT}}$ output bypasses the serial interface and brings immediate attention to fault conditions detected by the LTC1840, including slowdowns in the tachometer and changes in GPIO logic state.

If the $\overline{\text{BLAST}}$ pin is high at startup or presented with a high to low transition at anytime, the DAC output currents are immediately forced to full scale and the chip awaits commands from the serial bus. In addition, when $\overline{\text{BLAST}}$ is set high the LTC1840 guards against system controller crashes with an internal watchdog timer. If the device is not accessed for a period of more than 1.5 minutes, both DAC outputs go to full scale to guarantee adequate cooling.

LTC1960, continued from page 16

situations. Accurate wall adapter voltage detection can be critical. The LTC1960 has a user adjustable wall adapter input voltage trip point setting with less than a 2% error. For example, you can have valid AC present detection with a wall adapter rated as low as 13.2V and still charge a 12.6V 3-cell Li-Ion battery.

Simple Serial Interface

The serial connections are based on the Serial Peripheral Interface (SPI) protocol, a communications system that allows a host CPU to communicate with many peripheral devices. SPI is a very simple TTL level interface that does not require any special interface requirements from the host microprocessor. A simple bit-banging method using standard logic outputs makes the part compatible with any microprocessor. Given the high level of LTC1960 functional integration, the serial interface dramatically reduces the number of required signals between the host and the IC, freeing up host pins for other functions.

Conclusion

The LTC1960 represents the first complete dual battery discharge-charge system solution on a chip. It reduces solution cost, development time, PCB space and part count while at the same time providing more control, safety, and automatic crisis management relative to any other solution available today. Combined with a host microcontroller, it has the flexibility to work in both user proprietary and Smart Battery based applications. The limits of what can be accomplished with LTC1960 are solely dependent on the software controlling the IC. Although the primary LTC1960 market is notebooks and portable battery applications, its expandability also makes it a good solution for many battery backup applications, such as those in small servers.

New Device Cameos

DAC Circuit Design Just Got Easier: Ultraprecise 16-Bit SoftSpan DAC with Software Programmable Output Range

The LTC1592 is the only 16-Bit current output DAC that has a software programmable output range. The SoftSpan™ DAC is easily programmed via a 3-wire serial interface to operate in any one of six possible output ranges (0V to 5V, 0V to 10V, ±10V, ±5V, ±2.5V and -2.5V to 7.5V). All output spans have ultraprecise specifications of ±1LSB INL, ±1LSB DNL and excellent gain specifications over the industrial temperature range.

Gone are the precision resistors, switches and external amplifiers required for range switching. Fewer components means easier and faster design, which translates into your products making it to market sooner. A single board design can serve several applications, like instrumentation and data acquisition, without the need for jumpers to obtain different versions of the board. The only external components needed to get your SoftSpan DAC up and running are a precision 5V reference, a dual op-amp and a feedback capacitor.

For fast settling 16-bit precision industrial applications, choose the LTC1592 and the LT1468 (LT1469 dual) op amp to achieve 2µs settling times to 0.0015% for a 10V step. The LTC1592 has an ultralow 2nV-sec glitch impulse, which helps achieve low distortion in digital waveform generation and reduces overshoot in industrial and process control and optical switches and filters for communications applications. An asynchronous clear input always resets the LTC1592 to zero volts output regardless of the output range selected.

The LTC1592 has a 24- or 32-bit 3-wire serial interface with double-buffered internal 16-bit data registers. The part is available in a 16-lead SSOP package. It is ideally suited for 16-bit precision application in process control, industrial automation, optical switching in communications, digital waveform generation, instrumentation, data acquisition and ATE.

LT1766, LT1766-SYNC: 60V, 200kHz Monolithic Buck Regulators Offer High Efficiency and Maintain 1.5A Peak Switch Current over Full Duty Cycle Range

The LT1766 and LT1766-SYNC are 200kHz Monolithic buck regulators with peak switch currents of 1.5A. Capable of operation with input voltages of up to 60V, the parts achieve high efficiency over a wide range of input voltages and output currents. Power dissipation is minimized by using very fast output switch rates and by using a supply boost capacitor to fully saturate the 200mΩ power switch. In addition, a bias pin allows the control circuitry to be supplied from the output. The boost supply can be provided by outputs as low as 3V. Supply current is reduced to 25µA in shutdown for the LT1766.

The LT1766 and LT1766-SYNC incorporate a patented anti-slope-compensation circuit to maintain peak switch current over the entire duty cycle range. This circuitry allows optimum slope compensation without the usual penalty of reduced peak switch current at higher duty cycles. The LT1766-SYNC can be externally synchronized to frequencies as high as 700kHz.

Both regulators are available in fixed output voltages of 5Vand 3.3V or as an adjustable device with an output voltage range of 1.25V to 40V. The regulators are packaged in the fused lead 8-pin SO and are pin compatible with the LT1576 1.5A monolithic buck converter (see *Linear Technology*, IX:2, June 1999).

LTC3440 Synchronous Buck-Boost Converter Implements Lithium-Ion to 3.3V Conversion with a Single Inductor

In Lithium-Ion (Li-Ion) battery-powered applications, where a regulated voltage between 2.5V and 4.2V is required, SEPIC converters are typically used. The drawbacks of the SEPIC converter include the coupled inductor, additional high current capacitor and mediocre efficiency; however, until now, there have been few other options. The LTC3440 is the industry's first constant frequency, single inductor, buck-boost converter. It incorporates a patent pending control technique to efficiently regulate an output voltage above, below or equal to the input source voltage. Efficiencies of up to 95% are achieved with a single surface mount inductor and all ceramic capacitors. The small component count and the tiny, thermally enhanced MS-10 package make this product ideal for portable power applications requiring less than 2W of output power.

The LTC3440 input and output voltage ranges are both 2.5V to 5.5V, making it suitable for single Li-Ion or 3-cell alkaline/NiMH applications. The low $R_{DS(ON)}$ (0.2Ω NMOS, 0.25Ω PMOS), low gate charge synchronous switches, along with 15ns break-before-make times, provide high frequency, low noise operation with high efficiency. At light loads the bat-

For further information on any of the devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number:

1-800-4-LINEAR

Ask for the pertinent data sheets and Application Notes.

tery life is maximized with the low 25µA quiescent current (using Burst Mode® operation). Burst Mode operation is user controlled and can be enabled by driving the MODE/SYNC pin high. If the MODE/SYNC pin is either clocked or is driven low, fixed frequency switching is enabled. The operating frequency can be programmed from 300kHz to 2MHz with a resistor from the R_T pin to ground.

The part can also be commanded to shut down by pulling the $\overline{\text{SHDN}}$/SS pin low; in shutdown, the part draws less than 1µA of quiescent current. To limit inrush current at startup, an external RC is connected to the $\overline{\text{SHDN}}$/SS pin. Because operating frequency, soft-start, output voltage and Burst Mode operation are all user programmable, the product is suitable for a variety of applications. Other features include oscillator synchronization, current limit, thermal shutdown, antiringing control and input voltage feedforward for improved line regulation.

220MHz, 1500V/ms Dual/Quad Op Amps Save Space and Power

The LT1816 and LT1817 are low power, low distortion dual and quad op amps with a 220MHz gain bandwidth product and a 1500V/µs slew rate. The parts operate with supplies from ±2V to ±6V and draw a typical supply current of only 6.5mA per amplifier. In addition, the LT1816A features a current programming pin, which allows the user to lower the supply current by means of a single resistor.

The amplifiers can drive 100Ω loads with a low distortion of –67dBc relative to a 5MHz, $2V_{P\text{-}P}$ signal. The output swings to 0.9V from either supply rail with a 500Ω load, and to 1.2V with a 100Ω load. With the outputs at ±3V, the amplifier can sink or source a current of ±80mA.

The LT1816 dual op amp is available in space saving 8-lead MSOP and SO-8 packages. The LT1817 fits four amplifiers in an equally tiny 16-lead SSOP package, with a 14-lead SO also available. The LT1816A features two op amps with a current programming pin, in a 10-lead MSOP package. A single resistor can reduce each amplifier's supply current to as low as 1mA, retaining a 55MHz bandwidth. This way, performance and power consumption can be traded off on-the-fly for maximum efficiency in portable applications.

The low distortion, good output drive capability, combined with the $6\text{nV}/\sqrt{\text{Hz}}$ input voltage noise, make the LT1816/LT1817 ideal choices for receivers, filters, cable drivers and ADCs in high-speed communication, video or data acquisition systems. All parts are fully specified at ±5V and single 5V supplies, and are available in commercial and industrial temperature grades.

DESIGN TOOLS

Data Books and Applications Handbooks

1990 Linear Databook, Vol I —This 1440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices. $10.00

1992 Linear Databook, Vol II — This 1248 page supplement to the 1990 Linear Databook includes all products introduced in 1991 and 1992. $10.00

1994 Linear Databook, Vol III —This 1826 page supplement to the 1990 and 1992 Linear Databooks includes all products introduced since 1992. $10.00

1995 Linear Databook, Vol IV —This 1152 page supplement to the 1990, 1992 and 1994 Linear Databooks includes all products introduced since 1994. $10.00

1996 Linear Databook, Vol V —This 1152 page supplement to the 1990, 1992, 1994 and 1995 Linear Databooks includes all products introduced since 1995. $10.00

1997 Linear Databook, Vol VI —This 1360 page supplement to the 1990, 1992, 1994, 1995 and 1996 Linear Databooks includes all products introduced since 1996. $10.00

1999 Linear Data Book, Vol VII — This 1968 page supplement to the 1990, 1992, 1994, 1995, 1996 and 1997 Linear Databooks includes all products introduced since 1997. $10.00

1990 Linear Applications Handbook, Volume I — 928 pages full of application ideas covered in depth by 40 Application Notes and 33 Design Notes. This catalog covers a broad range of "real world" linear circuitry. In addition to detailed, systems-oriented circuits, this handbook contains broad tutorial content together with liberal use of schematics and scope photography. A special feature in this edition includes a 22-page section on SPICE macromodels. $20.00

1993 Linear Applications Handbook, Volume II — Continues the stream of "real world" linear circuitry initiated by the 1990 Handbook. Similar in scope to the 1990 edition, the new book covers Application Notes 40 through 54 and Design Notes 33 through 69. References and articles from non-LTC publications that we have found useful are also included. $20.00

1997 Linear Applications Handbook, Volume III — This 976 page handbook includes Application Notes 55 through 69 and Design Notes 70 through 144. Subjects include switching regulators, measurement and control circuits, filters, video designs, interface, data converters, power products, battery chargers and CCFL inverters. An extensive subject index references circuits in LTC data sheets, design notes, application notes and *Linear Technology* magazines. $20.00

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Brochures and Software

Power Management Solutions Brochure — This 96 page collection of circuits contains real-life solutions for common power supply design problems. There are over 70 circuits, including descriptions, graphs and performance specifications. Topics covered include battery chargers, desktop PC power supplies, notebook PC power supplies, portable electronics power supplies, distributed power supplies, telecommunications and isolated power supplies, off-line power supplies and power management circuits. Selection guides are provided for each section and a variety of helpful design tools are also listed for quick reference. Available at no charge.

Data Conversion Solutions Brochure — This 88 page collection of data conversion circuits, products and selection guides serves as excellent reference for the data acquisition system designer. Over 40 products are showcased, solving problems in low power, small size and high performance data conversion applications—with performance graphs and specifications. Topics covered include delta-sigma ADCs, low power and high speed ADCs and low power and high speed DACs. A complete glossary defines data conversion specifications; a list of selected application and design notes is also included. Available at no charge

Telecommunications Solutions Brochure —This 76 page collection of application circuits and selection guides covers a wide variety of products targeted for telecommunications. Circuits solve real life problems for central office switching, cellular phones, high speed modems, basestation, plus special sections covering –48V and Hot Swap^{TM} applications. Many applications highlight new products such as Hot Swap controllers, power products, high speed amplifiers, A/D converters, interface transceivers and filters. Includes a telecommunications glossary, serial interface standards, protocol information and a complete list of key application notes and design notes. Available at no charge.

SwitcherCAD™ III — LTC SwitcherCAD III is a fully functional SPICE simulator with enhancements and models to ease the simulation of switching regulators. This SPICE is a high performance circuit simulator and integrated waveform viewer, and also includes schematic capture. Our enhancements to SPICE result in much faster simulation of switching regulators than is possible with normal SPICE simulators. SwitcherCAD III includes SPICE, macromodels for 80% of LTC's switching regulators and over 200 op amp models. It also includes models of resistors, transistors and MOSFETs. With this SPICE simulator, most switching regulator waveforms can be viewed in a few minutes on a high performance PC. Circuits using op amps and transistors can also be easily simulated. Download at www.linear.com

FilterCAD™ 3.0 — FilterCAD 3.0 is a computer aided design program for creating filters with Linear Technology's filter ICs. Filter CAD is designed to help users without special expertise in filter design to design good filters with a minimum of effort. It can also help experienced filter designers achieve better results by playing "what if" with the configuration and values of various components and observing the results. With FCAD, you can design lowpass, highpass, bandpass or notch filters with a variety of responses, including Butterworth, Bessel, Chebychev, elliptic and minimum Q elliptic, plus custom responses. Download at www.linear.com

SPICE Macromodel Disk — This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models and a demonstration copy of PSPICE™ by MicroSim. Available at no charge

Noise Disk — This IBM-PC (or compatible) program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise and calculate noise using specs for any op amp. Available at no charge

World Wide Web and CD-ROM

LTC Web Site — Customers can quickly and conveniently find and retrieve the latest technical information covering the company's products on LTC's web site. Located at www.linear.com, the site allows searching of data sheets, application notes, design notes, *Linear Technology* magazine issues and other LTC publications. The LTC web site simplifies searches by providing three separate search engines. The first is a quick search function that provides a complete list of all documentation for a particular word or part number. There is also a product function tree that lists all products in a given product family. The most powerful, though, is the parametric search engine. It allows engineers to specify key parameters and specifications that satisfy their design requirements. Other areas within the site include a sales office directory, press releases, financial information, quality assurance documentation, and general corporate information.

Linear Direct E-Commerce — As of January 2001 the LTC web site has been empowered to allow direct credit card sales for quantities up to 100 units. All customers with sample, prototype, and small production run needs can now order directly from Linear Technology. Once a customer selects a part, they simply enter Linear Direct by clicking the "buy" button located in the upper left hand corner of the data sheet. Linear Direct will ship customer orders worldwide.

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