LINEAR TECHNOLOGY

MARCH 2003 VOLUME XIII NUMBER 1

IN THIS ISSUE...

24-Bit ADC Challenges ΔΣ Conventions

by Mike Mayes

Introduction

Using a delta sigma ADC for precision instrumentation can be a simple proposition, despite conventional wisdom to the contrary. Conventional wisdom suggests that measuring low level signals, such as strain gauge bridges or thermocouples, requires amplification to match the ADC input range. Conventional wisdom also suggests that achieving a high level of accuracy and rejection requires a fast output rate and accompanying post-processing, and that a low impedance source cannot be measured directly, but requires buffering. The natural conclusion of conventional wisdom is that high resolution, delta sigma ADCs make for complex designs. Conventional wisdom may be conventional, but in this case it is not necessarily wise.

Over the past 5 years, Linear Technology has produced an extensive family of ultrahigh precision delta sigma analog-to-digital converters. This family differentiates itself from other high resolution converters by offering extreme accuracy without the added complexities usually associated with delta sigma converters. Calibration sequences, configuration registers, filter settling time, and external oscillators are eliminated. Transparent offset and full-scale auto calibration are performed every conversion cycle to ensure absolute accuracy independent of time, temperature, and supply voltage. The No Latency Delta-Sigma™ architecture simplifies multiplexing applications.

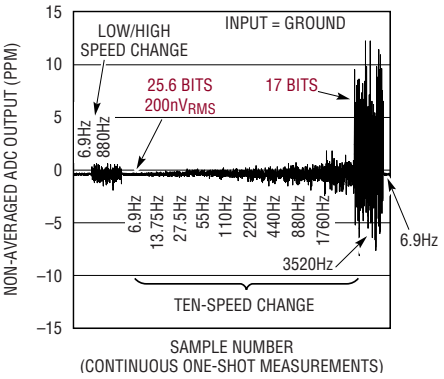


Figure 1. Shifting gears on the LTC2440 has little to no affect on accuracy. This graph shows continuous single-shot measurements of a grounded input as the speed is changed on the fly. The speed change from 6.9Hz to 880Hz is implemented by simply driving the SDI pin from low to high. Alternatively, the speed can be increased in nine steps (5-bit input to SDI) from 6.9Hz to 3.5kHz.

An internal oscillator enables accurate line frequency rejection while eliminating the need for high frequency external oscillators and the coupling problems that can result.

Figure 2 shows a block diagram of the new LTC2440, which uses a new delta sigma converter architecture but remains pin and timing compatible with the existing delta sigma converter product line. A programmable over sample ratio (OSR) allows users to tune the speed and resolution for a variety of applications (see Figure 1). Figure 3 shows the ten speed/resolution combinations from 6.9Hz/24.6 bits to 3.5kHz/17 bits which are selectable through a

continued on page 3

Issue Highlights

Our cover article introduces the LTC2440 delta sigma ADC. Over the past 5 years, Linear Technology has produced an extensive family of ultrahigh precision delta sigma analog-to-digital converters. This family differentiates itself from other high resolution converters by offering extreme accuracy without the added complexities usually associated with delta sigma converters. Calibration sequences, configuration registers, filter settling time, and external oscillators are eliminated. Transparent offset and full-scale auto calibration are performed every conversion cycle to ensure absolute accuracy independent of time, temperature, and supply voltage. The No Latency Delta-Sigma™ architecture simplifies multiplexing applications. An internal oscillator enables accurate line frequency rejection while eliminating the need for high frequency external oscillators and the coupling problems that can result.

This issue also features a host of new products, including the LT1934, a micropower buck regulator with an internal 400mA power switch. The LT1934 provides up to 300mA output current, while consuming just 12µA of quiescent current. This is an important feature for always-on battery-powered applications such as laptop computer standby supplies or remote instrumentation that must operate for years from primary batteries. Its wide input voltage range of 3.4V to 34V makes it applicable to a variety of power sources including 24V industrial supplies, automotive batteries and unregulated wall transformers.

The next article presents the LTC3730, LTC3731 and LTC3732 family of PolyPhase® controllers. These controllers are efficient at both heavy and light CPU loads, making them a good match for high performance notebook computer applications.

The LT6550 and LT6551 3.3V triple and quad high speed amplifiers make it possible to create compact solutions for driving RGB and component video cables. These voltage feedback amplifiers drive either 50Ω or 75Ω double terminated cables and are preconfigured for a fixed gain of two, thus eliminating six or eight external gain setting resistors.

The LT1716 is a micropower, precision rail-to-rail comparator that operates on single or split supply voltages that total anywhere between 2.7V and 44V. The part is unique in that the input voltage range is from V_{EE} up to 44V above V_{EE}, regardless of the V_{CC} voltage being used.

The LTC1955 dual smart card interface provides a complete and compact solution for multicard applications. The LTC1955 and five small capacitors are all that are needed to interface two card sockets to a host microcontroller. Designed to comply with all smart card standards, the LTC1955 can be used for full sized card sockets, smaller vendor card (simlock) sockets, or any combination of smart card and vendor card sockets.

The LT3150 controller drives an external N-channel MOSFET as a source follower to create an extremely low dropout, ultra-fast transient response linear regulator. The LT3150's precision-trimmed reference provides ±0.6% initial accuracy, ±1% tolerance over temperature and accommodates low-voltage outputs. Transient response performance is optimized around low cost, low ESR, readily available ceramic capacitors.

The LTC4006, LTC4007 and LTC4008 series of battery chargers pack all of the most desirable battery charger and protection features into a single IC. These devices also offer novel features that save board space, and modern I/O features for communication with host systems

The LTC4251, LTC4252 and LTC4253 Hot Swap controllers offer comprehensive circuit protection for –48V applications (and higher) through three stages of current control. They protect the system bus from hot swapped power modules and they protect the power modules from glitches on the system bus. These devices are available in a variety of configurations to fill almost any application need.

Starting on page 37 are three new Design Ideas covering a variety of applications, from a simple way to charge batteries using USB power, to using a positive buck regulator to make a negative boost DC/DC converter.

At the back are five New Device Cameos. See www.linear.com for complete device specifications and more applications information.

LTC in the News...

On January 15, Linear Technology Corporation announced its financial results for the 2nd quarter of fiscal year 2003. According to Robert H. Swanson, Chairman of the Board and CEO, "We grew this quarter slightly over the previous quarter and significantly over the similar quarter in the prior year. We continue to be strongly profitable as demonstrated by our 39% return on sales and also strongly cash flow positive. We have turned in these good results during difficult economic times. Lead times and backlog are low and customers continue to order only to near term demand. Therefore, confidently and accurately forecasting short-term future results continues to be difficult. However, the March quarter is customarily stronger for us and we expect some improvement in demand. Consequently, we estimate that sales and profits will grow in mid single digits, 3% to 7%, from the December quarter."

The Company reported net sales of $145,045,000 and net income of $56,163,000 for the quarter ended December 29, 2002. Diluted earnings were $0.18 per share. A cash dividend of $.05 per share will be paid on February 12, 2003 to stockholders of record on January 24, 2003.

LTC2440, continued from page 1

simple serial interface, where resolution = log(RMS noise/5)/log 2. The digital filter has no latency, allowing the converter to respond to speed selections or external input channel changes between conversions without settling errors.

The ultra low noise of the ADC eliminates the system-level complexities related to using PGAs by offering 25 million counts over a ±2.5V input range ($200nV_{RMSNOISE}$) or 500,000 counts over a ±50mV input range independent of sensor offset/tare voltages. The absolute accuracy (5ppm INL, 1ppm offset, 10ppm full-scale, all independent of output rate), and flexible input range (common mode input from GND to V_{CC} independent of V_{REF}) greatly simplify analog front end circuitry.

Measuring Low Level Signals without a PGA

Programmable gain amplifiers (PGAs) are commonly used in systems where a small input signal (RTD, thermocouple, strain gauge) needs to be applied to a wide input range analog-to-digital converter. The convention is to amplify the sensor output voltage range so that it matches the ADC input range. The input referred noise due to the ADC is reduced by the PGA gain. However, the system performance is dominated by the noise performance of the PGA as well as its offset, full-scale, and linearity performance. PGAs degrade the system performance by introducing added error sources, drift, cost and complexity. In addition, sensor offset/tare voltages need to be adjusted out to prevent saturating the amplifier output or over-ranging the ADC input. Because PGAs are used to reduce the noise contributed by the analog-to-digital converter, if the ADC noise is low enough, these PGA tradeoffs can be eliminated.

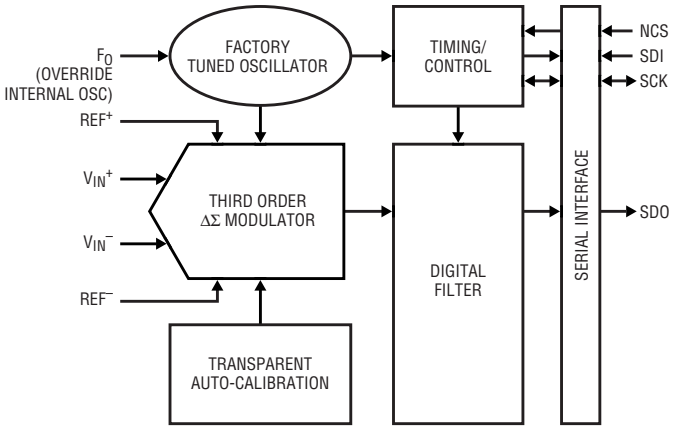


Figure 2. High performance variable speed/resolution ΔΣ architecture

Eliminating the PGA (and tare adjust) requires a converter with exceptional offset, linearity, full-scale accuracy, drift, and noise performance. The converter requires enough resolution over its full input range to maintain high resolution within a significantly reduced portion of its input span. This allows system designers to directly interface sensors to the ADC while using a small portion of the overall converter input range; thus, significantly simplifying the analog front end. The number of counts produced over the full output range typically determines performance. The resolution is determined by dividing the sensor's full-scale output voltage by the RMS noise of the analog front end.

The LTC2440 running at 6.9Hz has an RMS noise level of 200nV over a ±2.5V input range equivalent to 25,000,000 counts. The exceptional noise performance of this device allows the user to make one conversion (no averaging) with 500,000 counts and no DC errors for any ±50mV range (Figure 4). Because it doesn't need a PGA, the LTC2440 maintains a wide input range and easily handles sensor offset and tare voltages. The offset error is less than 5µV independent of temperature and the full-scale is within 0.003% with less than 0.2ppm/C drift.

The exceptional DC performance of the LTC2440 does not require extra system calibration. The programmable OSR enables the system to seamlessly change the conversion rate without degrading this exceptional DC performance. While running at 880Hz, the LTC2440 maintains approximately 50,000 counts over the same ±50mV range. Then the OSR can be changed to 6.9Hz on the next conversion with full accuracy, as shown in Figure 1. The OSR is programmed either by tying a single pin LOW or HIGH (880Hz or 6.9Hz) or with a 5-bit serial word applied to that same pin (10 speed selections).

The offset, full-scale, integral linearity and power dissipation are all independent of the speed selected. Speed independent accuracy coupled with no latency enables users to gear

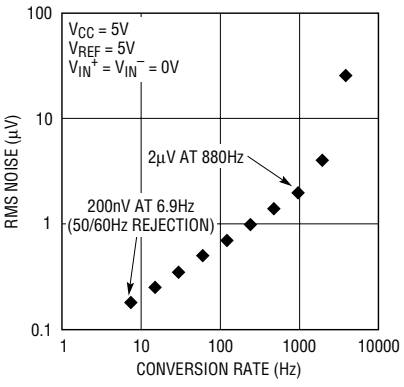


Figure 3. The variety of easy-to-select speed/resolution combinations allows the LTC2440 to be tailored to many applications

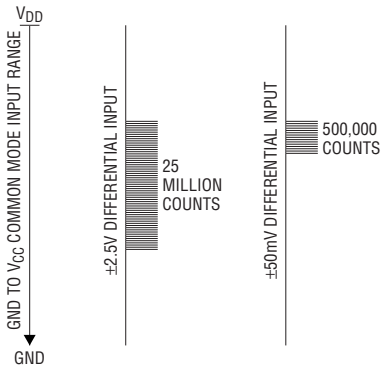


Figure 4. High resolution mode directly digitizes low level signals even while monitoring a wide input range.

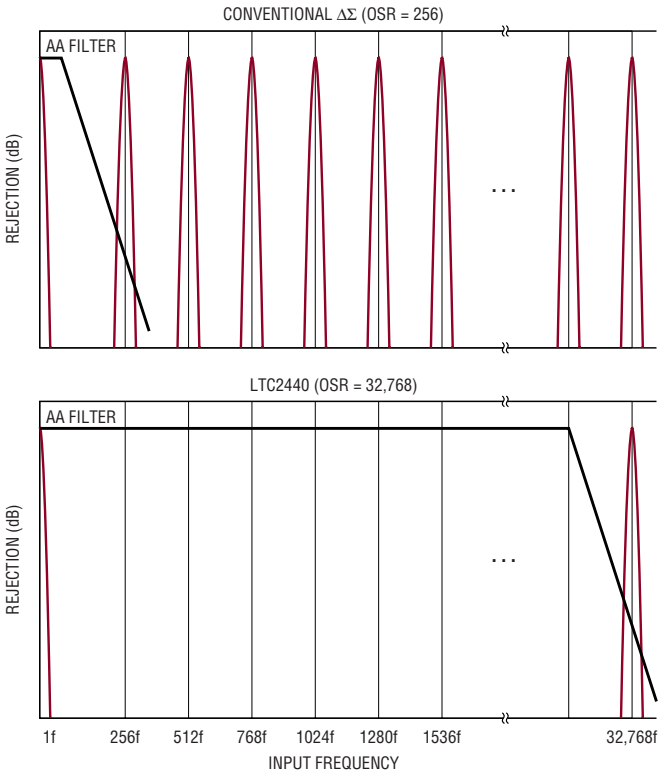


Figure 5. Large OSR eases front end filtering requirements

shift between conversions. For example, the LTC2440 may monitor a fast moving signal at 3.5kHz output rate, and then switch to a slower output rate in order to obtain a lower noise reading. This is useful in systems monitoring input perturbations as they settle, auto-ranging circuits, or general data acquisition.

Achieving High Input Rejection without High Output Rates

One property common to all high resolution delta sigma ADCs is an on chip digital lowpass filter. These filters offer excellent rejection up to the internal modulator sampling rate. At multiples of the internal modulator sample rate, unwanted input perturbations are folded back to DC with little attenuation (aliasing). Delta sigma converters sample the input at a multiple, commonly referred to as the over sample ratio (OSR), of the output rate. Since the OSR is typically large (≥64), the digital filter offers excellent rejection of input noise sources and simple antialiasing requirements.

Conventional high resolution delta sigma ADCs operate at a fixed OSR typically between 64 and 256. In order for these devices to reject 50Hz and 60Hz line frequencies the modulator sample rate, f_{SAMPLE}, is only 64 to 256 times the line frequency (3.8kHz to 15.3kHz). Noise applied to the input with frequency content at f_{SAMPLE} is aliased back to DC resulting in unwanted errors. As the OSR is increased for a given rejection frequency, f_{SAMPLE} is increased and the antialiasing requirements are reduced.

The LTC2440 internal sampling clock (f_{SAMPLE}) is fixed at 1.8MHz independent of the output rate. In order to change the output rate, the internal OSR is changed. While the LTC2440 is operating at 6.9Hz, the digital filter simultaneously rejects 50Hz and 60Hz and the OSR is very high (32,768). With its sample rate of 1.8MHz, the LTC2440 offers much more rejection and simple antialiasing compared to conventional converters running at lower OSRs, as shown in Figure 5.

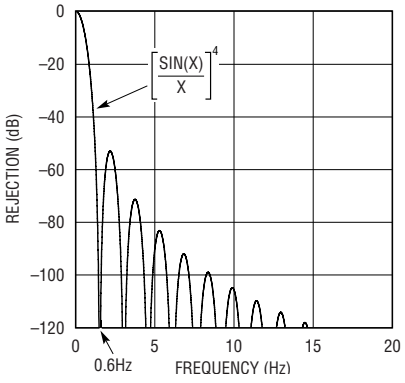


Figure 6. Input rejection with an external 100kHz oscillator reduces noise down to 0.6Hz

Direct Digitization of Low Level Signals without Buffers

A commonly overlooked and/or misunderstood issue related to analog-to-digital converters is the effect of the switched-capacitor sampling network on performance. Looking into the input terminal of a delta-sigma converter is a high frequency switched capacitor array switching at a frequency, f_{SAMPLE}. If the external network tied to the converter input settles within the sampling period ($1/f_{SAMPLE}$), no error results. The source impedance of the sensor, external capacitance at the input terminal, the ADC sample rate, and the size of the internal sampling capacitor determine the settling time.

Some manufacturers of high resolution delta-sigma converters have invented various clever ways to improve the *apparent* input settling, but the tradeoffs in system performance render these methods impractical for many applications. Some include on-chip buffers in the signal path to isolate the switched capacitor array from the external circuit. The problem with this approach is the input signal range is limited to several hundred millivolts above ground and 1.5V below V_{DD}. Since many sensors' output ranges are outside of this range, these buffers cannot be used. Other manufacturers attempt to solve this problem by partially sampling the output of the buffer through a coarse cycle, then sampling the residual through a fine sample. While this allows input signals near ground, it introduces settling errors as a function of the amplifier's offset and common mode rejection. This results in signal dependent errors that vary over time and temperature.

For these reasons, most system designers choose to disable the input buffer circuitry and handle the input settling externally. Some designers have discovered when they remove the bypassing capacitor at the input to the ADC and apply the sensor directly to the converter the input settling errors are gone. In this case, the input settling errors are no longer a function of the large external capacitor, but become a function of the external source resistance and the internal sampling capacitor (typically on the order of a few pF).

The LTC2440 can directly digitize sensors with output impedances up to 500Ω with no errors due to the input settling current. This allows direct digitization of thermocouples, RTDs, and 350Ω bridges. In the case of remote sensing, the LTC2440 can be directly connected to the sensor. The excellent common mode and normal mode input rejection enables direct connection without the need for external amplifiers, level shifters, and capacitors. Since the programmable OSR technology adjusts the output rate without changing the internal sampling rate, the input settling characteristics are independent of conversion rate. Thus, a 500Ω source impedance signal can be measured at any output rate from 6.9Hz to 3.5kHz while the output level and input settling characteristics do not change.

Running with a Slow External Oscillator

f_{SAMPLE} is set to 1.8MHz by a factory-tuned on-chip oscillator running at 9MHz. This oscillator may be overridden by attaching an external oscillator to the device. If the external oscillator is set to 100kHz, for example, the internal sample rate is reduced to 20kHz. While this internal sample rate is on the order of conventional delta sigma converters offering great input rejection at 60Hz, the LTC2440 rejects frequencies above 0.6Hz (see Figure 6). This is equivalent to an impractical lowpass filter with external resistances on the order of MΩ or capacitances on the order of Farads. In addition to rejection above 0.6Hz, the LTC2440 front end analog circuitry incorporates a chopper which removes the very low frequency 1/f noise and offset drift. Under these conditions, the LTC2440 can be used to precisely measure DC voltages in excessively noisy environments.

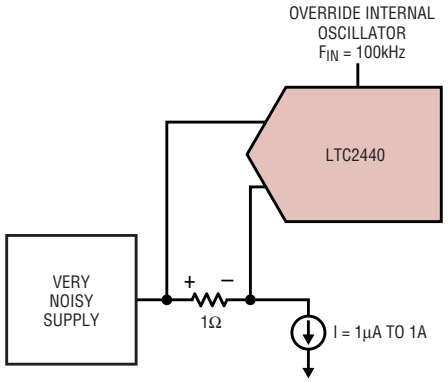


Figure 7. Very low frequency rejection and wide common mode input range enable precise current sensing over a wide current range

One such application is measuring the DC current through a shunt resistor (see Figure 7). Any noise above 0.6Hz is rejected by more than 120dB up to the sample rate. Since the OSR is large (32,768), the antialiasing requirements are simple. Other delta-sigma converters using low OSRs for their digital filter sample the input at rates below 150Hz making antialiasing extremely difficult.

Running with an external oscillator of 100kHz and the highest resolution (OSR = 32,768), the RMS noise of the LTC2440 is 200nV over a full ±2.5V input range. Six decades of current, in either direction, can be measured accurately through a 1Ω resistor independent of low frequency system noise. The flexible common mode input range enables the LTC2440 to digitize these signals near V_{DD}.

Reduced Power Operation

In addition to adjusting the speed/resolution of the LTC2440, the average power dissipation may also be adjusted using the automatic sleep mode. During the conversion cycle, the LTC2440 draws 8mA independent of the conversion output rate. Once the conversion is completed, the device automatically enters a low power sleep state drawing 8µA. The device remains in this state until the conversion result is read. The user may reduce the DC power dissipation by extending the duration of the low power sleep state.

For example, if the OSR (OSR = 64) is programmed for minimum conversion rate (T_{CONV} = 0.285ms) and the sleep state is extended to 10ms, the effective output rate is 100Hz while the power dissipation is below 1.3mW. By further extending the duration of the sleep state to 100ms, the effective output rate is 10Hz and the power dissipation is 150µW. Noise, power, and speed can be adjusted by setting the OSR and sleep mode duration.

Summary

The LTC2440 offers accuracy, stability, and ease of use that are common to the LTC2400 product family. It combines a programmable OSR digital filter with a high speed analog modulator in order to achieve high speed and accuracy independent of output rate. The LTC2440's wide range of user programmable speed and resolution combinations makes it flexible enough to fit in a wide variety of applications.

For more information on parts featured in this issue, see http://www.linear.com/go/ltmag

Micropower SOT-23 Buck Regulator Accepts Inputs to 34V

by Jeff Witt

Introduction

The LT1934 is a micropower buck regulator with an internal 400mA power switch. It provides up to 300mA output current, while consuming just 12µA of quiescent current, an important feature for always-on battery-powered applications such as laptop computer standby supplies or remote instrumentation that must operate for years from primary batteries. Its wide input voltage range of 3.4V to 34V makes it applicable to a variety of power sources including 24V industrial supplies, automotive batteries and unregulated wall transformers.

3.3V 250mA Supply from 24V Input Consumes Just 15µA

Figure 1 shows a 3.3V/250mA supply that accepts inputs from 4.5V to 34V. With the output in regulation and with no load, the input current with V_{IN} = 24V is less than 15µA. Input current falls to less than 1µA when the LT1934 is placed in shutdown mode by pulling $\overline{SHDN}$ to ground. The $\overline{SHDN}$ pin can be tied to V_{IN} if the shutdown mode is not used. The capacitor and diode tied to the BOOST pin provide a bias voltage above V_{IN} in order to fully saturate the internal NPN power switch, thereby maintaining high efficiency over the entire input voltage range.

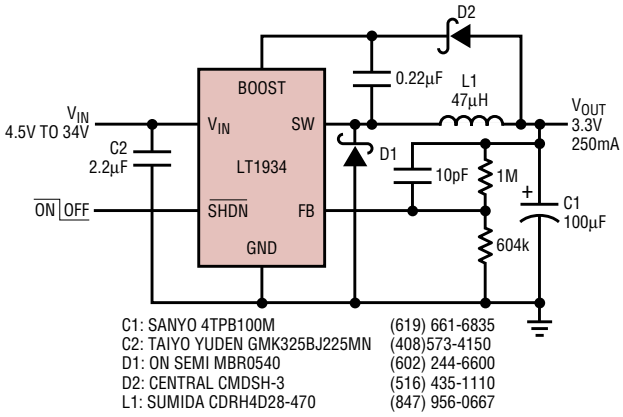


Figure 1a. This buck regulator supplies 250mA at 3.3V from an input voltage as high as 34V. Input current with no load applied is less than 15µA.

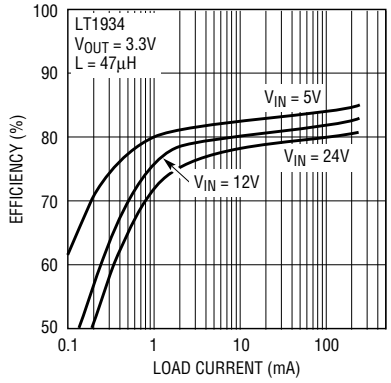


Figure 1b. Efficiency of Figure 1's ciruit

The LT1934 uses Burst Mode® operation, with low quiescent current, to achieve high efficiency across a wide range of load currents, as shown in Figure 1b. An internal comparator monitors the voltage at the FB pin. When the voltage at this pin is above 1.25V, the LT1934 is in its sleep mode with only its reference and feedback comparator biased. In this state the V_{IN} pin current is 12µA. As the load current discharges the output capacitor, the FB pin voltage falls below 1.25V and the comparator enables the internal oscillator and drive circuits. The LT1934 switches with a fixed off time of 1.8µs, limiting the peak inductor current to 400mA as it delivers power to the output. Figure 2 shows the operating waveforms of the circuit in Figure 1a. Output voltage ripple is less than $50mV_{P-P}$. Figure 3a shows a circuit that generates 5V from a 6.5V–34V input. Figure 3b shows the efficiency of this circuit.

The accurate, fast, cycle-by-cycle current limit of the LT1934 keeps the switch and inductor currents under control at all times. In addition, the 1.8µs switch off time is extended during fault conditions when the output voltage is pulled below the programmed output voltage. This ensures that the LT1934 can handle a shorted output.

The LT1934-1 for Low Current Supplies

The LT1934-1 is identical to the LT1934 except that the current limit is 120mA. The LT1934-1 can be used in applications with a maximum load current of 60mA. This lower current limit allows a better match between the power components (the inductor and the input and output capacitors) and the application, resulting in a smaller circuit size. Input ripple is also lower, reducing noise and simplifying input filtering. The LT1934-1 may be a better choice when the power source has a high output impedance, such as 4mA-20mA loops, long-life primary batteries with high internal resistance

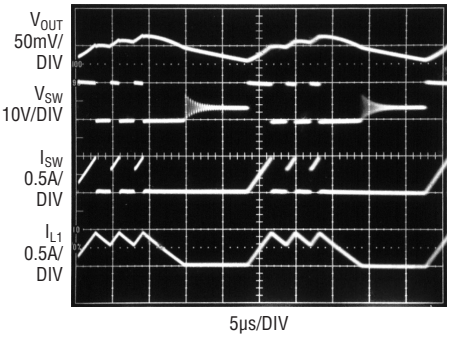


Figure 2. The operating waveforms of the circuit in Figure 1 as it delivers 180mA from a 10V input. The fast, accurate, cycle-by-cycle current limit results in a robust circuit that can withstand a shorted output.

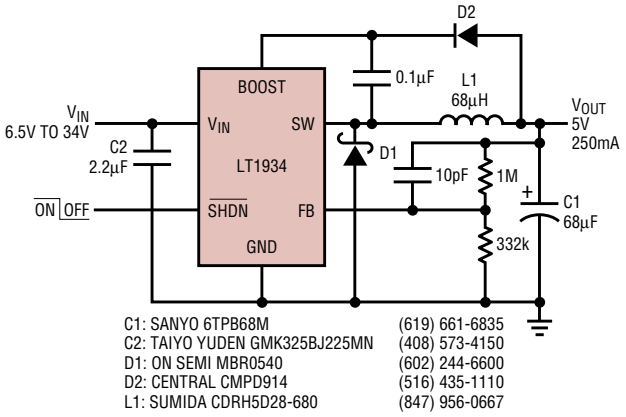


Figure 3a. The LT1934 provides 250mA at 5V.

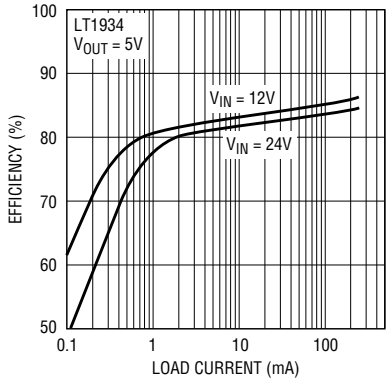


Figure 3b. Efficiency of Figure 3's circuit

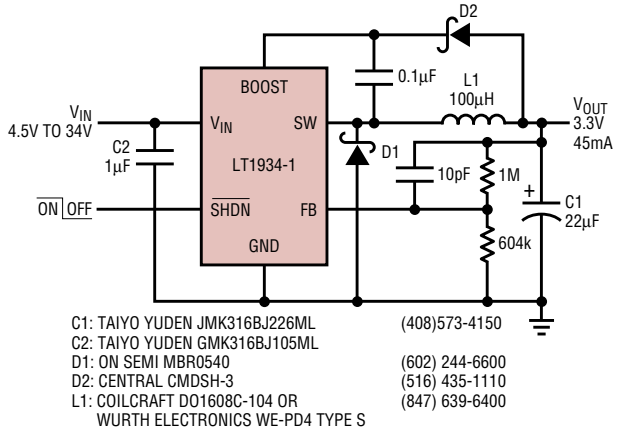


Figure 4. Smaller components can be used with the lower current LT1934-1.

or remote supplies with long cables. Low maximum switch current is also helpful in designing intrinsically safe systems, which have limits on stored energy and require current limiting resistors in series with external connections. Figure 4 shows a 3.3V supply implemented with the LT1934-1.

Li-Ion Battery Charger with Industrial Input Range

The circuit in Figure 5 is a complete, single-cell Li-Ion battery charger that operates from an input of 7V to 28V and provides a charge current of 350mA. This charger requires no microcontroller. A charge cycle is initiated when power is applied to the circuit, and end-of-charge is indicated when the battery voltage reaches 4.2V and charge current has fallen to one tenth of the nominal charge current.

The LT1934 acts as a current-limited 5V pre-regulator for the LTC4052-4.2 pulse charger. The LTC4052 monitors the battery voltage and pulls the $\overline{\text{CHRG}}$ pin low to indicate that the battery is being charged.

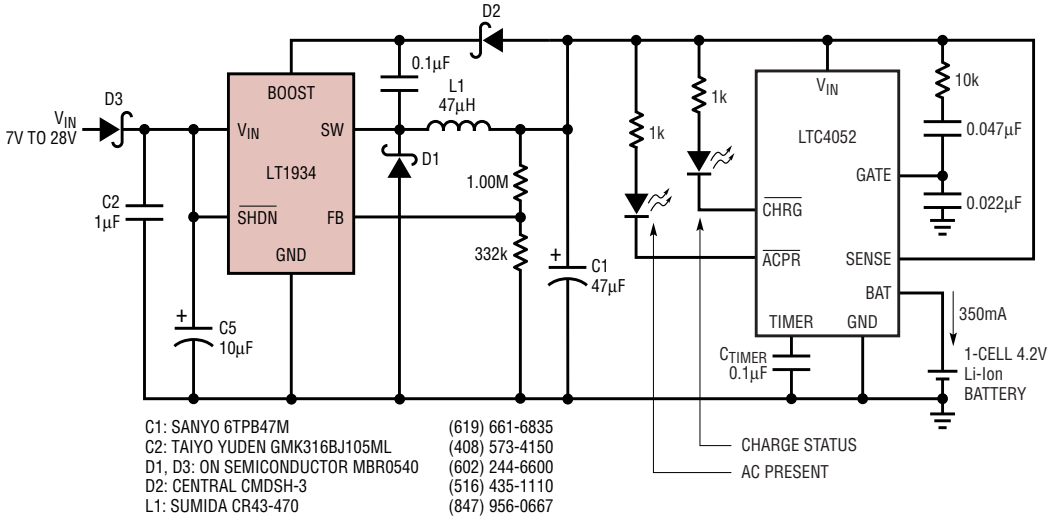


Figure 5. This standalone 350mA Li-Ion battery charger accepts inputs to 28V and requires no heat sinks.

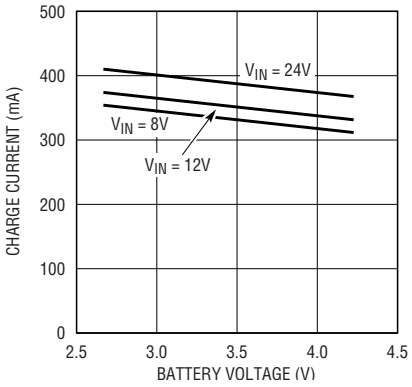


Figure 6. Charging current as a function of battery voltage and input voltage

If this voltage is less than 2.5V, the LTC4052 applies a 24mA trickle charge, with the LT1934 maintaining 5V across C1.

When the battery voltage rises above 2.5V, the LTC4052 enters its fast charge mode, turning on an internal N-channel FET switch between its SENSE and BAT pins. This connects the LT1934's output to the battery. As the voltage across C1 falls to the battery voltage, the LT1934 limits its output current, charging the battery at 350mA. Because the FET is fully on, very little power is dissipated, and the charging circuit maintains high efficiency during the entire charge cycle.

When the battery voltage reaches 4.2V, the LTC4052 turns off the switch for 100ms. If the battery voltage falls below 4.2V during this period, the switch is turned back on for at least 400ms. In this manner, the LTC4052 modulates the duty cycle of the 350mA current source. When this duty cycle falls to 10%, the LTC4052 indicates that the battery is nearly charged by switching the $\overline{CHRG}$ pin to a weak 40µA pull down. Pulse charging continues until a timer in the LTC4052 stops the charge cycle after three hours, when the $\overline{CHRG}$ pin goes to a high impedance state. If the battery voltage is pulled below 4.05V due to a load current, the LTC4052 reenters its fast charge mode.

If input power is removed, the LTC4052 isolates the LT1934's circuitry and reduces battery load to less than 1µA. Diode D3 provides reverse input protection.

The LT1934 regulates its output current by limiting the peak current in L1 to 400mA. The charge current equals the average current in L1, and depends on the input and output voltages, as shown in Figure 6. In addition to these variations, expect approximately ±15% variation in the nominal charge current due to variations in the current limit and switch off time of the LT1934 and the value of L1.

In addition to indicating charge status, the LTC4052 also provides an AC-present flag that indicates that power has been applied to the charger. A similar device, the LTC1730, can be used to provide additional features, including a thermistor interface for monitoring the temperature of the battery and a shutdown pin that can be used to reinitialize the charge cycle timer.

This Li-Ion charger uses only surface mount devices, requires no heat sinks, and its wide input voltage range accepts a variety of power sources including unregulated wall transformers, car batteries and 24V industrial supplies. The charger is completely standalone, requiring no

continued on page 27

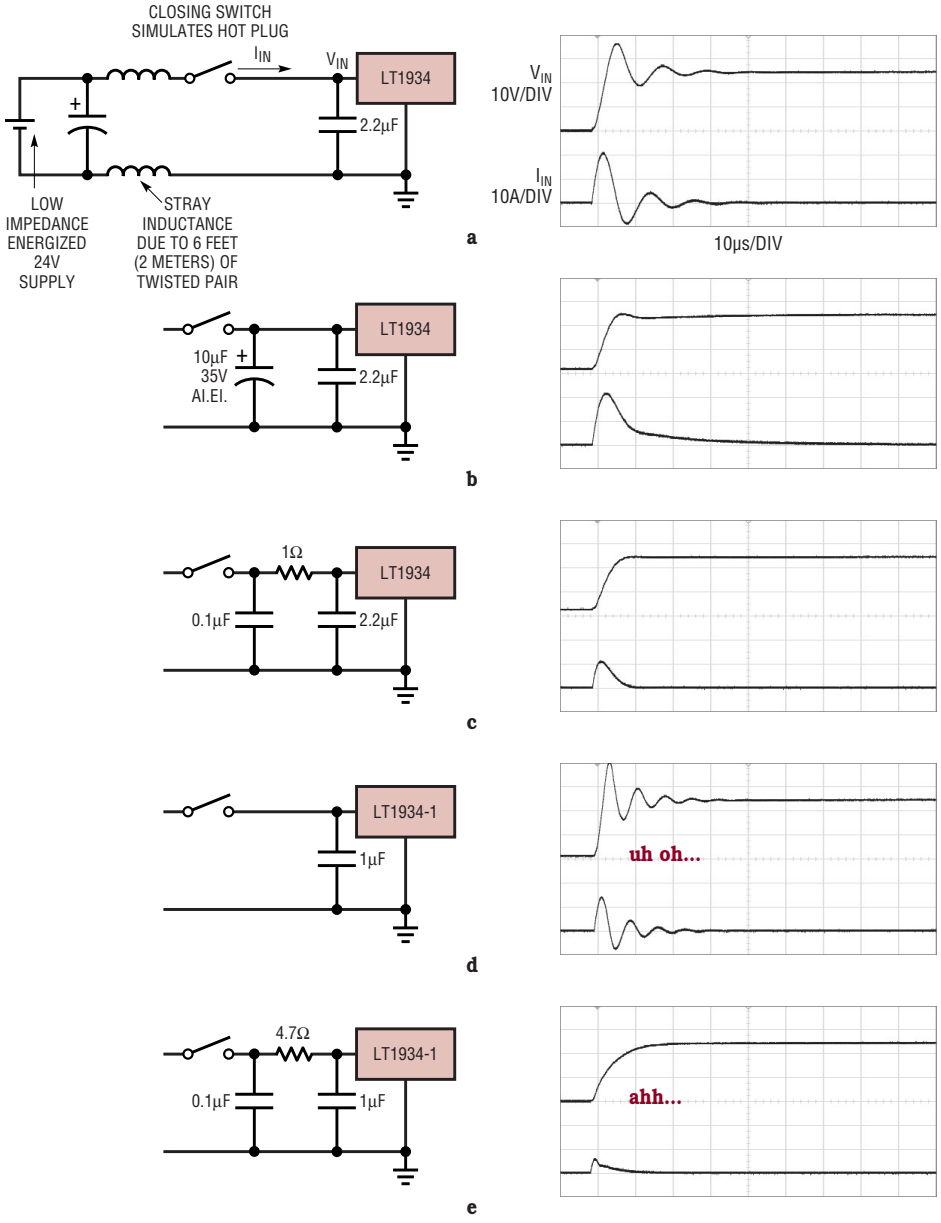


Figure 7. A well chosen input network prevents input voltage overshoot and ensures reliable operation when the LT1934 is connected to a live supply.

High Performance 3-Phase Power Supplies Yields High Efficiency over the Entire CPU Load Range

by Wei Chen and Steve Hobrecht

Introduction

Thermal stress is a major concern for enterprise CPUs that frequently draw up to 100A of load current. PolyPhase® switching DC/DC converters reduce thermal stress by providing high efficiency at heavy loads, and thus have become the standard power supply solution for high powered CPUs. PolyPhase switchers are also finding their way into mobile applications where CPUs are drawing currents greater than 30A, and will draw 65A in the near future. Mobile CPUs pose an additional problem, though. They spend much of the time in sleep or standby modes, meaning that *light load* efficiency is important to maximize battery run-time. Traditional PolyPhase converters, despite their exceptional performance at heavy load, are not as efficient at light load.

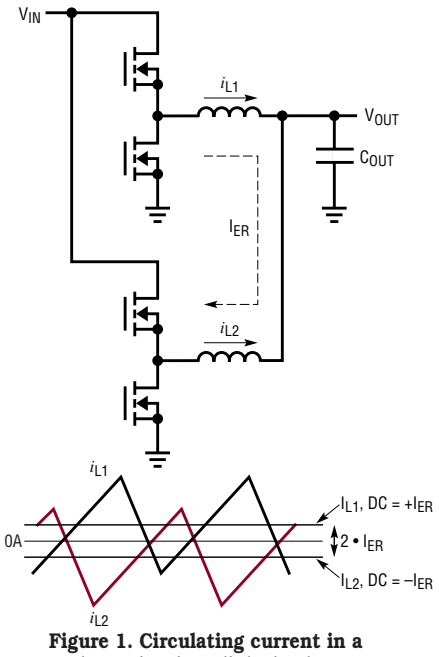


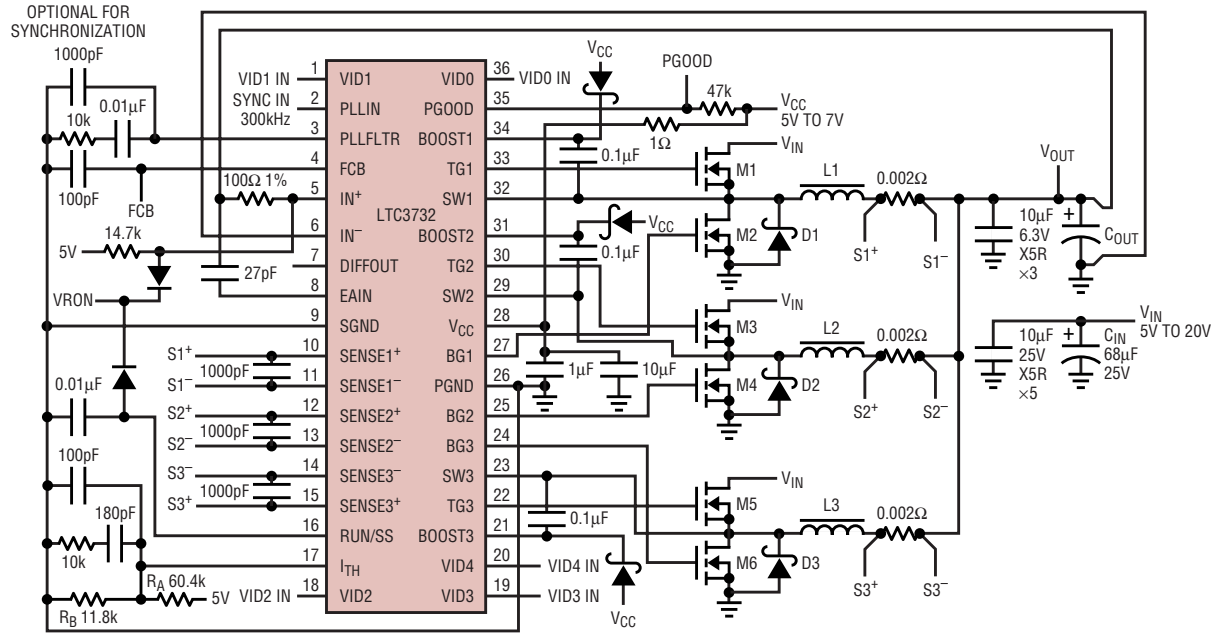
Figure 1. Circulating current in a 2-phase circuit at light load

The LTC3730, LTC3731 and LTC3732 family of PolyPhase controllers are efficient at both heavy and light CPU loads, making these new controllers a good match for high performance notebook computer applications.

This high efficiency at light loads is a result of a new Stage Shedding™ feature, which significantly reduces conduction switching losses.

These new controllers have other important features that make them a good choice for mobile CPU applications:

- ❑ True remote sensing on both the positive and negative output rails to ensure tight output regulation at high output currents;
- ❑ Kelvin sensing (positive and negative) on the pads of each current sense resistor to achieve accurate



VIN: 3.3V TO 20V
VOUT: 1.1V TO 1.85V, 60A
fSW: 300kHz
CIN: SANYO OS-CON 25SP68M (619) 661-6835
COUT: 330µF/2.5V ×10 SANYO POSCAP 2RSTPE330MC
D1 TO D3: B340A

L1 TO L3: 0.8µH SUMIDA CEP125-0R8 (847) 956-0667
M1, M3, M5: IR IRF7811W (310) 322-3331
OR FAIRCHILD FDS6688 (408) 822-2126
OR SILICONIX Si7860DP (800) 554-5565
M2, M4, M6: IR IRF7822 ×2
OR SILICONIX Si7856DP ×2

Figure 2. Schematic diagram of a 3-phase 65A VRM9.x power supply

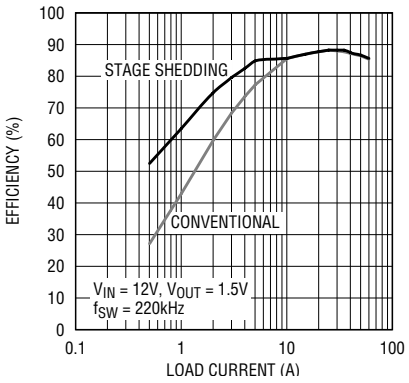


Figure 3. Measured efficiencies of Stage Shedding operation and conventional operation for the VRM9 design

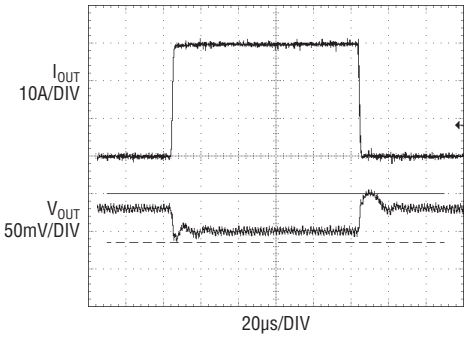


Figure 4. Load transient waveforms for the VRM9.1 design

current sharing, even if the layout of parallel power stages is not symmetrical;

- ❑ All controllers feature integrated high current MOSFET drivers for up to 600kHz switching frequency, thus minimizing the overall power supply size and component count.

LTC3731 is a versatile 3-phase controller that generates a 30 or 60 degree clock output based on the voltage level of the PHASMD pin. This feature allows several LTC3731s to be paralleled for up to 12-phase operation. The 0.6V to 6V output voltage is programmed by an external resistor divider. The LTC3730 is a dedicated 3-phase controller with 5-bit VID output programming that is compatible with IMVP2 and IMVP3 requirements. The internal op amp can be used to program voltage offsets for different CPU operation modes. This controller is suitable for powering Intel mobile Northwood CPUs. The LTC3732 is another 3-phase controller with a 5-bit VID output programming that is compatible with VRM9.x specs. This controller is suitable for powering Intel desktop Pentium 4 (P4) CPUs in a so called DeskNote PC or Transportable PC design. A DeskNote PC uses the desktop CPU in a notebook computer design to simultaneously achieve high performance and low cost. All three controllers are available in space saving SSOP36 packages, while the LTC3731 is also available in the much smaller, and thermally enhanced, 5mm × 5mm QFN package.

Stage Shedding Operation Improves Efficiency at Light Loads

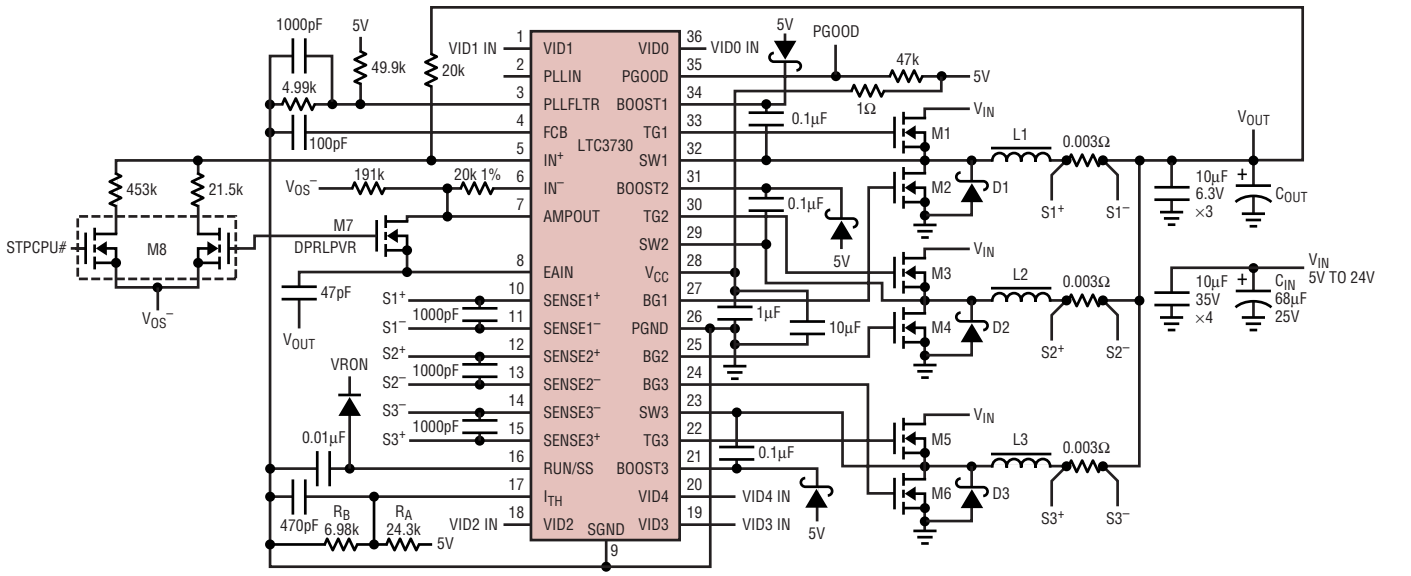
There are three main obstacles to obtaining high efficiency at light loads with a PolyPhase converter:

- ❑ Switching related losses
- ❑ Extra conduction losses induced by circulating currents
- ❑ IC bias losses

The first two obstacles, described below, are reduced by the Stage Shedding feature. The IC bias losses can be reduced by enabling Burst Mode® operation.

Light Load Efficiency Obstacle 1: Switching-Related Power Losses

In high current applications, low $R_{DS(ON)}$ MOSFETs are typically chosen to minimize conduction losses at full loads. At light loads, though, the high gate charge and parasitic capacitance of these MOSFETs often cause significant power losses associated with gate driving and switching. Also, the core loses of inductors dominate the overall inductor power losses at light loads. Since the switching losses, gate driving losses, and inductor core losses do not decrease with load currents, light load efficiency suffers.



VOUT: 0.6V TO 1.75V, 45A
SWITCHING FREQUENCY: 300kHz
CIN: SANYO OS-CON 25SP68M
COUT: 270µF/2V ×4 PANASONIC SP EEFSD0D271R

D1 TO D3: B140A DIODES INC
L1 TO L3: SUMIDA 1µH/20A CEP125 IROMC-H OR 1µH/19A PANASONIC PCC-D126H OR TOKO EH125C

M1, M3, M5: IR IRF7811W OR FAIRCHILD FDS6688 OR SILICONIX Si7860DP
M2, M4, M6: IR IRF7811X2 OR SILICONIX Si7856DP
M7: 1/2 SILICONIX Si1034X
M8: SILICONIX Si1034X

Figure 5. IMVP3 compatible, 45A, 3-phase power supply

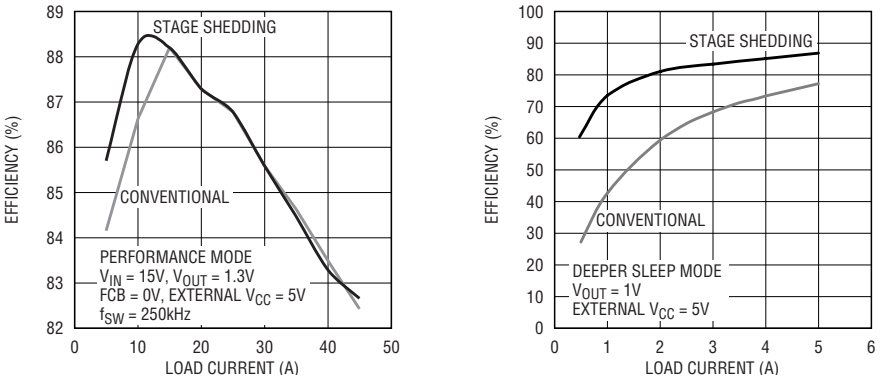


Figure 6. Measured efficiencies of Stage Shedding operation and conventional operation for the 3-phase IMVP3 power supply

Light Load Efficiency Obstacle 2: Circulating Currents

In a PolyPhase synchronous buck converter, the inductor current in each synchronous buck stage is allowed to reverse at light loads due to synchronous rectification. In a practical PolyPhase design, a current sharing error always exists because of tolerances in the sense resistors and slight mismatches between paralleled channels within the controllers. Any current sharing error among the paralleled stages introduces circulating currents that result in additional power losses. As shown in Figure 1, for example, if the current difference between two paralleled channels is 2A (I_{ER}=1A), one channel (Channel 1) will source 1A and the other channel (Channel 2) will sink 1A at no load conditions. Since this 1A current circulates between two channels instead of flowing toward the output, this current introduces unnecessary power losses. Therefore, the circulating current must be minimized to improve light load efficiency in a PolyPhase converter.

The Solution: Stage Shedding Operation

A simple solution is to turn off the bottom FET when the inductor current starts to reverse. This is called pulse skipping in most LTC controllers. This scheme significantly reduces the reverse current. However, an accurate detection of inductor current zero-cross and an immediate turn-off of the bottom FETs are difficult to achieve. A more effective scheme, as implemented in new 3-phase controllers, is the Stage Shedding technique. At light loads, the controllers automatically shut down all but one channel. This scheme completely eliminates the circulating currents and related power losses. Furthermore, Stage Shedding eliminates the gate drive losses, MOSFET switching losses, and inductor core losses of the unused channels. Thus the Stage Shedding technique decreases the conduction losses and switching losses significantly at light loads, resulting in a much higher efficiency at light loads. Since the controller maintains the original regulation loop, Stage Shedding has no effect on output regulation accuracy.

Burst Mode Operation Minimizes Obstacle 3: IC Bias Losses

To further minimize the IC bias losses and switching losses at no load conditions, Burst Mode operation can be enabled by applying a voltage between 0.6V and (V_{CC} – 1V) to the FCB pin.

3-Phase, High Efficiency 65A VRM9.x Power Supply for Pentium 4 CPU

Figure 2 shows a 3-phase VRM9.x power supply for a Pentium® 4 CPU. It uses the LTC3732 to drive nine small PowerPak SO-8 MOSFETs for 65A output current. To provide higher output currents, simply use lower $R_{DS(ON)}$ MOSFETs and higher current rated inductors. R_A and R_B implement a lossless active voltage positioning (AVP) technique to minimize the output capacitor size. For more detailed technical information about AVP see the LTC1736 data sheet or Design Solution 224. Figure 3 shows the measured efficiency under different load conditions. In this case the input is 12V, the output voltage is 1.5V and the switching frequency is 220kHz. The efficiencies are measured for both Stage Shedding operation and for conventional PolyPhase operation (with all channels ON). As the chart shows, Stage Shedding operation significantly improves efficiencies at light loads (≤10A). At 1% of full load (0.6A), Stage Shedding operation improves efficiency more than 25%. Figure 4 shows the load transient response waveform for the 30A load step. With ten POSCAPS (330µF/2.5V,

Pentium is a registered trademark of Intel Corporation

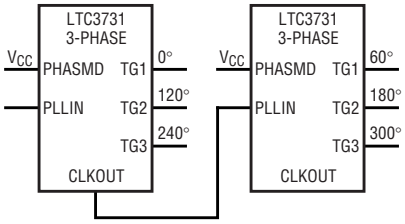


Figure 7a. 6-phase configuration

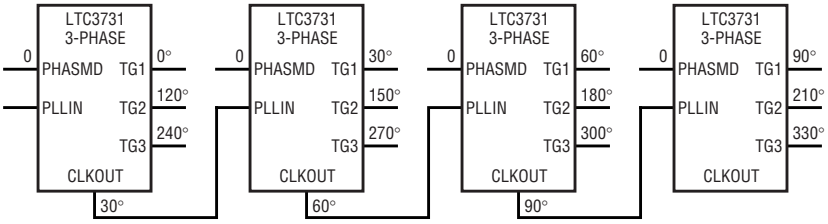
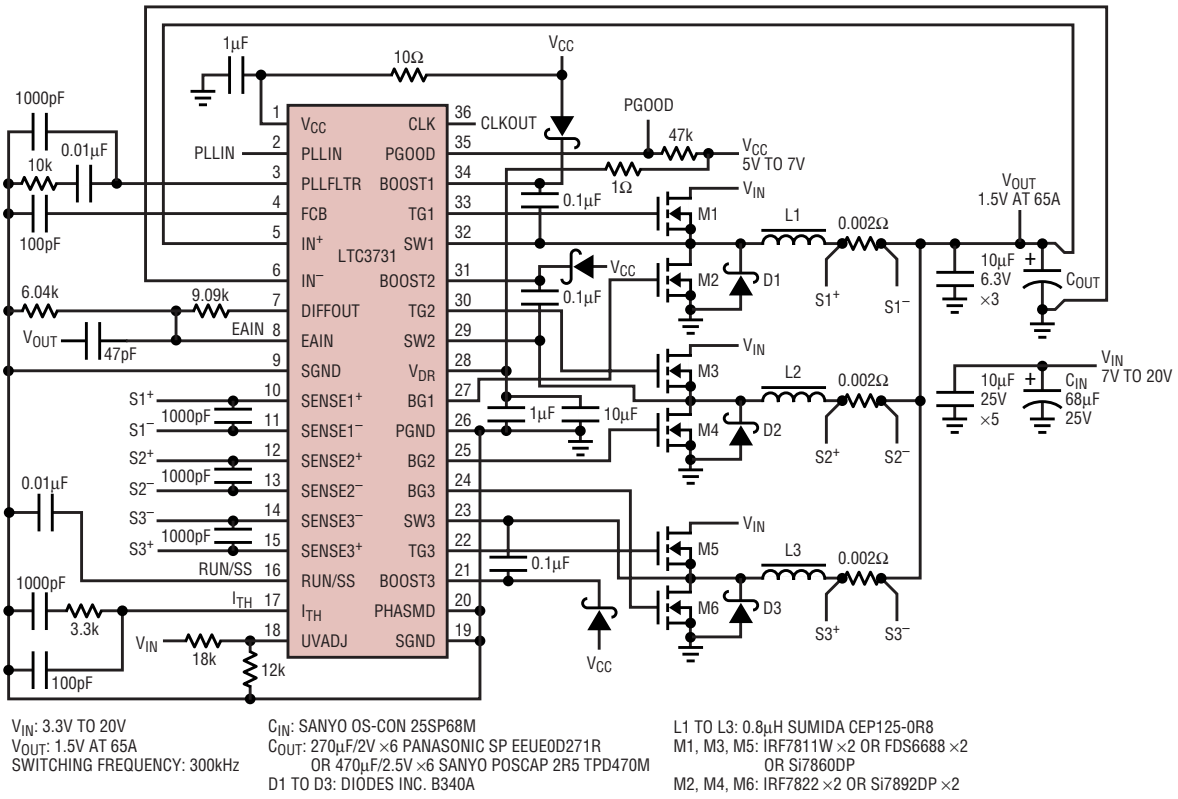


Figure 7b. 12-phase configuration



VIN: 3.3V TO 20V
VOUT: 1.5V AT 65A
SWITCHING FREQUENCY: 300kHz

CIN: SANYO OS-CON 25SP68M
COUT: 270µF/2V ×6 PANASONIC SP EEUE0D271R
OR 470µF/2.5V ×6 SANYO POSCAP 2R5 TPD470M
D1 TO D3: DIODES INC. B340A

L1 TO L3: 0.8µH SUMIDA CEP125-0R8
M1, M3, M5: IRF7811W ×2 OR FDS6688 ×2
OR Si7860DP
M2, M4, M6: IRF7822 ×2 OR Si7892DP ×2

Figure 8. Basic 3-phase block using the LTC3731

12mΩ ESR) at the output, the output voltage variation is about 70mV$_{P-P}$. The AVP loadline slope is 0.9mΩ in this design.

3-Phase IMVP3 Compatible Power Supply for Mobile Northwood CPUs

Figure 5 shows an IMVP3 power supply for a mobile Northwood CPU. It uses the LTC3730 to drive six small PowerPak SO-8 MOSFETs for up to 45A output current. Like in the previous example, R_A and R_B implement the AVP to minimize the output capacitor size. The IMVP3 specs also require three digital signals in addition to the 5 VID bits to set the output voltage under different operational modes: battery optimized mode (BOM), performance optimized mode (POM), deep sleep mode (DPSLP), and deeper sleep mode (DRPSLPVR). Under the BOM, DPSLP and DPRSLPVR modes, the output voltage is reduced to conserve the battery energy.

Figure 6 shows the measured efficiency under performance mode and deeper sleep modes, where the input is 15V and the switching frequency is 250kHz. The efficiency in performance mode exceeds 82% at 1.3V output over a load range of 3A to 45A. Efficiencies in deeper sleep mode were measured for both Stage Shedding operation and conventional PolyPhase operation. Stage Shedding operation improves the efficiencies significantly in deeper sleep mode: about 10% improvement at 5A current. This corresponds to a power loss saving of 0.7W. In a notebook application, the idle time represents about 70% of the run time, this power saving at deeper sleep mode can generate about 4% longer battery run time (assuming 53Whr battery and 4 hour battery run time).

Versatile LTC3731 Powers Up to 200A Current with 12-Phase Operation

The LTC3731 has a CLKOUT pin that produces a 30 degree or 60 degree clock output (referenced to TG1 rising edge) based on the voltage level of the PHASMD pin. Therefore, multiple LTC3731s can be daisy-chained to produce a 6- or 12-phase operation. Since the error amplifier of the voltage feedback loop is a g_m amplifier, the g_m amplifiers of the LTC3731s can be paralleled, creating a common error amplifier that has an equivalent gain of (g_m • n), where n is the number of LTC3731s in parallel. Figure 7 shows the block diagram for a 6-phase and a 12-phase circuit. Figure 8 shows the detailed schematic diagram of one of the 3-phase blocks shown in Figure 7. Each 3-phase block is capable of 65A load current.

Conclusion

LTC3730, LTC3731 and LTC3732 based 3-phase power supplies can deliver high efficiency over a wide load range. Stage Shedding operation significantly improves efficiency at light loads, making this controller family particularly attractive for battery-powered applications where improved light load efficiency can increase battery run time. This family also includes features that make power supplies smaller and more robust, including overcurrent latchoff and overvoltage protection.

Triple and Quad RGB Amplifiers Deliver Full Performance on 3.3V

by Jon Munson and Raj Ramchandani

Introduction

The LT6550 and LT6551 3.3V triple and quad high speed amplifiers make it possible to create compact solutions for driving RGB and component video cables. These voltage feedback amplifiers drive either 50Ω or 75Ω double terminated cables and are preconfigured for a fixed gain of two, thus eliminating six or eight external gain setting resistors.

The industry trend of using lower supply voltages increases the demands placed on analog signal handling characteristics. For example, a 3.3V video amplifier not only requires high slew rates and fast settling times but must also have wide input and output voltage swing ranges to avoid clipping any portion of the video waveform. Current feedback amplifiers cannot be used because they lack sufficient signal swing at low supplies and they require input signal above ground.

The LT6550 and LT6551 are true voltage feedback amplifiers featuring 110MHz (–3dB) bandwidth, 340V/µs slew rate, and fast settling time, making them ideal for low voltage, high resolution, RGB Video Processing.

The LT6550 and LT6551 operate from 3V to 12.6V and are fully specified on single 3.3V and 5V supplies, the LT6550 is also fully specified on ±5V supplies. Both parts are available in compact 10-pin MSOP packages and performance is guaranteed over the industrial temperature range.

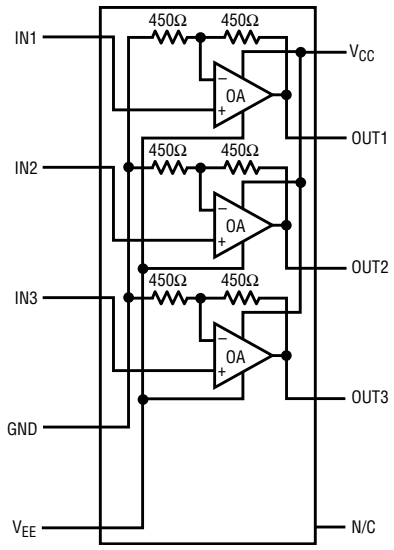


Figure 1a. LT6550 block diagram

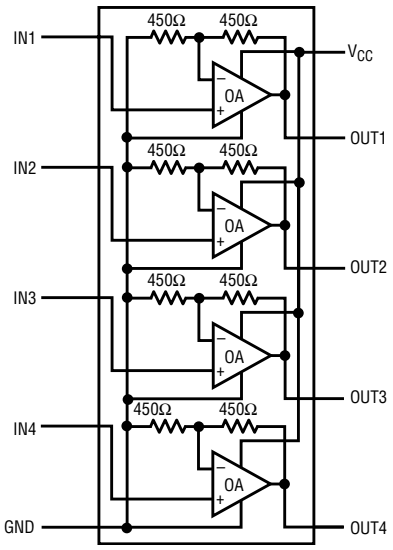


Figure 1b. LT6551 block diagram

Amplifier Characteristics

The block diagrams in Figure 1 show the differences between the LT6550 and LT6551. The LT6551 quad is designed for single supply operation with the feedback returned to ground. The LT6550 triple has a separate V_{EE} pin and can be used on either single or split supplies.

These devices feature internal feedback resistors and a flow-thru pin out, which simplifies PC board layout and enhances performance by minimizing input to output stray capacitance. The amplifiers feature a rail-to-rail output and an input common mode range which includes ground. Figure 2 shows the output swing driving a 150Ω load vs supply voltage. On a single 3.3V supply, the input voltage range extends from ground to 1.55V and the output typically swings to within 400mV of the supply voltage while driving a 150Ω load. Table 1 summarizes the major performance specifications.

Figure 3 shows a simplified schematic of one channel of the LT6551. Resistors R_F and R_G provide an internal gain of 2. (The LT6550 triple is a slight variation with the gain setting resistor, R_G, connected to a separate ground pin). The input stage consists of transistors Q1 to Q8 and resistor R1. This topology allows for high slew rates at low supply voltages. Transistors Q3 and Q4 are class AB biased as are transistors Q5 and Q6. The input stage transconductance is derived from $1/g_m$ of these transistors and resistor R1. The input stage drives the folded cascode degeneration resistors of PNP and NPN current mirrors, Q9 to Q12, which convert the differential signals into a single-ended output. There are back-to-back series diodes, D1 to D4, across the plus and minus inputs of each amplifier to limit the differential input voltage to ±1.4V. R_{IN} limits the current through these

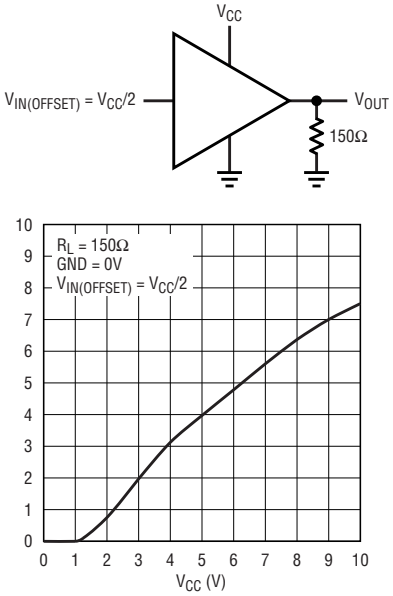


Figure 2. Output swing high vs supply voltage

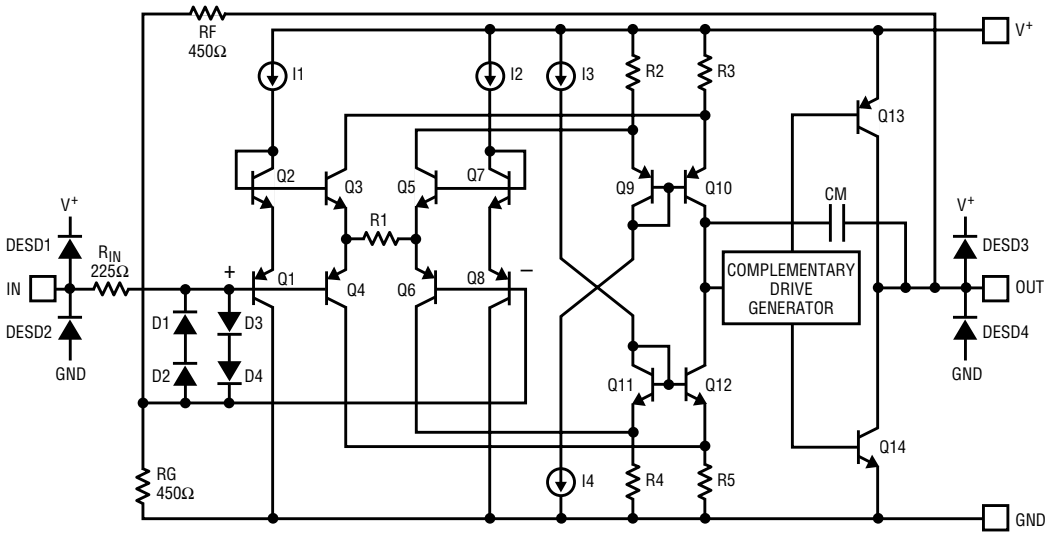


Figure 3. Simplified schematic

diodes if the input differential voltage exceeds ±1.4V. The complementary drive generator supplies current to the output transistors that swing from rail-to-rail.

RGB Video Applications

RGB (Red, Green, and Blue) video format requires three signals that represent the amplitudes of the respective colors plus timing signals (sync) that are sometimes combined with the green component.

With video amplifiers driving double terminated 50Ω or 75Ω cables, the video output taken from the far end of the cable is 6dB lower then the output of the amplifier. For this reason these video amplifiers are configured for a closed loop gain of +2. The black (lowest output for all three colors) to white (highest) voltage range for each of the respective RGB channels is approximately 700mV, sync pulses are typically 300mV lower then the black level resulting in a total voltage range of 1.0V. This means that for DC-

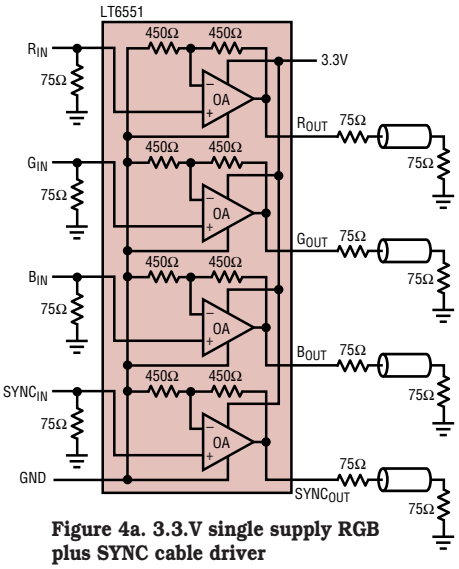


Figure 4a. 3.3.V single supply RGB plus SYNC cable driver

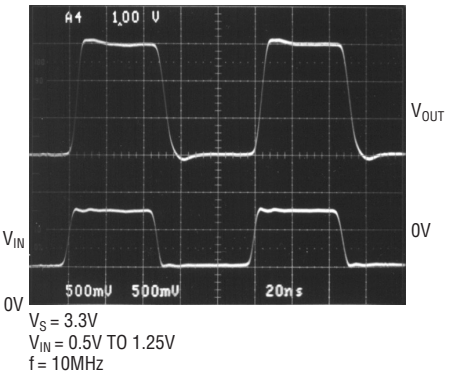


Figure 4b. Output step response

Table 1. Typical performance specifications (T_A = 25°C)

Parameter	Conditions	Typical Values@3.3V/0V	Typical Values@ 5V/0V
–3dB Bandwidth	R_L = 150Ω	90MHz	110MHz
0.25dB Gain Flatness	R_L = 150Ω	30MHz	30MHz
Output Voltage Swing High	R_L = 150Ω	2.5V Minimum	3.5V Minimum
Output Voltage Swing Low	I_{SINK}= 10mA	200mV Maximum	200mV Maximum
Slew Rate	R_L = 150Ω	250V/µs	340V/µs
Settling Time to 3%	V_{OUT} = 1.5V step, R_L = 150Ω	20ns	20ns
Channel Separation	Between all Channels at 10MHz	–60dB	–60dB
Differential Gain	R_L = 150	0.09%	0.05%
Differential Phase	R_L = 150	0.09°	0.05°
Supply Current per Channel		8.5mA	9.5mA

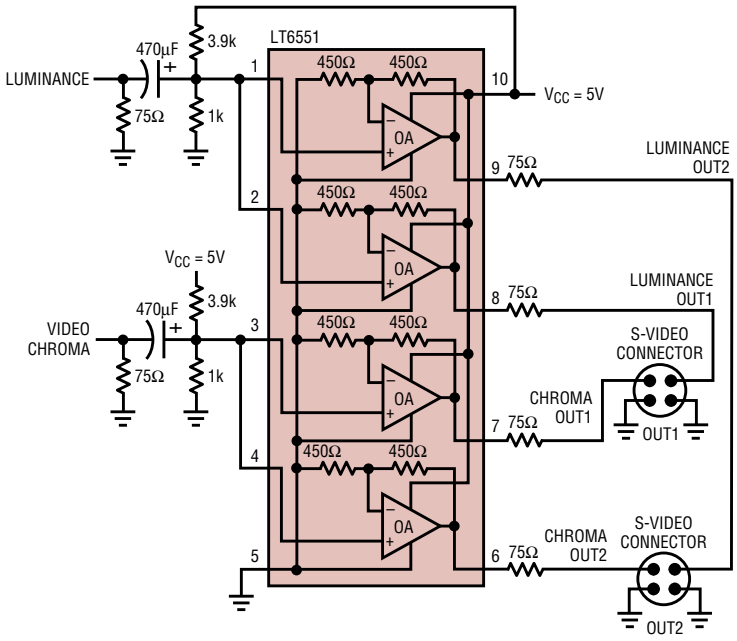


Figure 5. S-video splitter

coupled applications, the output of the amplifier needs to swing at least 2.0V while driving a 150Ω load and the input range should be greater then 1.0V. The LT6550 and LT6551 were designed to meet these requirements.

Figure 4 shows a 3.3V powered RGB cable-driver application that could handle additional sync information on any channel. Using DC-coupled inputs allows precise control of the signal swing within the guaranteed 2.3V available output range. For applications that require a separate sync output, the fourth channel of the LT6551 can be utilized as shown in Figure 4.

AC Coupled S-Video Splitter

The S-video format separates the luma signal (Y) from the chroma subcarrier signal (C), and is usually AC-coupled. AC-coupled applications require the design to accommodate picture-content offset in the signal by allowing output swing of 3.2V for composite or 2.5V for sync-stripped video.

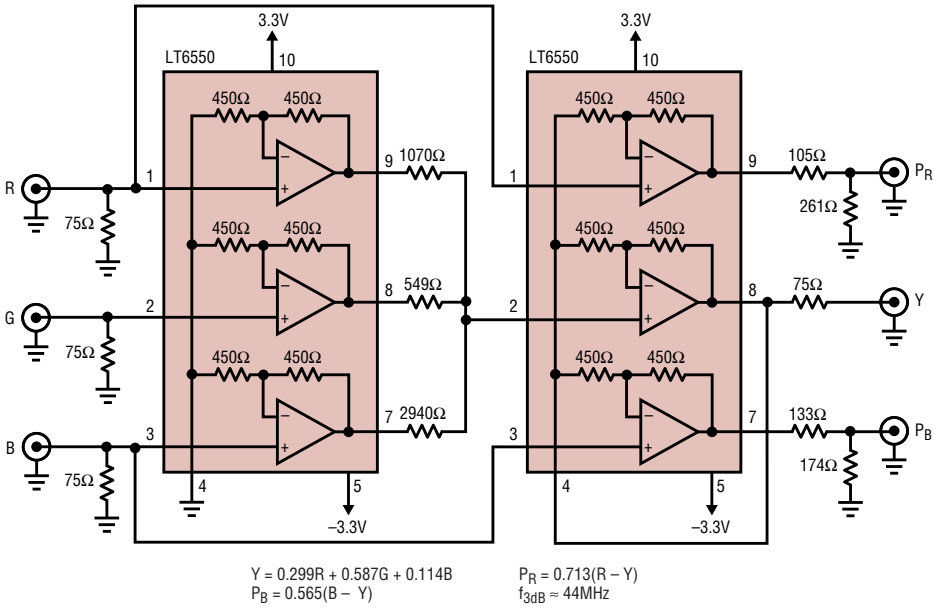


Figure 6. Buffered RGB to color-difference matrix

Figure 5 shows an AC-coupled luma and chroma channel video cable driver that provides dual Y and C output ports. Operating from a single 5V supply, the LT6551 provides a guaranteed output swing of 3.3V, with the bias point established by the input resistor network shown. The chroma signal is a color subcarrier signal with no picture content offset, so it is readily accommodated with the same biasing scheme.

Buffered RGB to Color-Difference Matrix

High performance consumer products require generation of YP_bP_r luminance and chrominance component signals, often from standard RGB source content. The YP_bP_r format has a luma signal and two weighted color difference signals at baseband. Even with their fixed internal gain resistors, two LT6550s connected as shown in Figure 6 easily implement the required conversion matrix equations (also shown in Figure 6). To perform the conversion, the input to the Y channel of the second LT6550 is a simple weighted sum of the 2× amplified RGB signals from the first LT6550, creating a signal of 2Y. The Y channel output in the second LT6550 is fed back to its feedback resistor common pin. This configuration implicitly performs the required Y subtraction function for both of the color difference channels and sets the Y channel output stage to the required unity gain.

The necessary scaling of the color-difference signals is performed passively by their respective output termination resistor networks. Since this circuit naturally produces bi-polar color difference signals (±0.35V at the cable load), the simplest implementation is to power the circuit with ±3.3V split supplies. With an available output swing of about 5.6V for this supply configuration, the circuit handles video with composite syncs and various DC offsets without difficulty. Since the Y channel normally needs to incorporate sync, either all of the RGB signals can have sync included or a 1.8mA gated current-sink can be

continued on page 18

Versatile Over-The-Top Precision Comparator is Ideal for Status Monitoring

by Jon Munson

Introduction

The LT1716 is a micropower, precision rail-to-rail comparator that operates on single or split supply voltages that total anywhere between 2.7V and 44V. The part is unique in that the input threshold range is from V_{EE} up to 44V above V_{EE}, regardless of the V_{CC} voltage being used. This means that operation at low logic levels no longer restricts the range of input levels that can be compared. In addition to the Over-The-Top® feature, the LT1716 will tolerate overdrive of up to –5V with respect to V_{EE} on an individual input without phase inversion. Besides offering robust input voltage swings, precision performance is retained; typical input offset is less than 500µV.

The LT1716 also has some unique output characteristics. When driving high-impedance loads, the output swings close to the rails without need for external components, thanks to an active pull-up current-source. While able to eliminate an external pull-up resistor in many applications, the LT1716 topology also includes an integrated Schottky diode configuration that provides support for traditional "open-collector" operation up to 44V above V_{EE} when load-switching or level-translation is desired.

The LT1716 is offered in the popular SOT-23 5-lead package and typically draws a "micropower" supply current of 35µA. Refer to Table 1 for a summary of the major performance characteristics of the LT1716.

Table 1. Summary of LT1716 performance characteristics (V_{CC} = 5V, V_{EE} = 0V)

Parameter	Value	Condition
Input Voltage Range	–5V to +44V with respect to V_{EE}	Independent of V_{CC}
Input Offset Voltage	<500µV typical	0.5V to 44V above V_{EE}
Supply Voltage Range	2.7V to 44V	$V_{CC} – V_{EE}$
Supply Quiescent Current	35µA typical	V_O = High
Propagation Delay	3µs typical	$V_{OVERDRIVE}$ = 100mV R_L = 10kΩ
Output Sink Current	10mA minimum	$V_{OVERDRIVE}$ > 30mV
Output Source Current	85µA typical	$V_{OVERDRIVE}$ = 5mV
Output Leakage Current	0.5µA typical	V_{OH} = V_{CC} to 44V above V_{EE}

How Does It Work?

Input Architecture

The LT1716 achieves its unique input capabilities by the use of a sophisticated input structure. The topology is completely symmetric differentially and each input signal is processed in four distinctly different ways that vary as a function of the applied voltage. The left-hand portion of the simplified schematic, Figure 1, shows the input

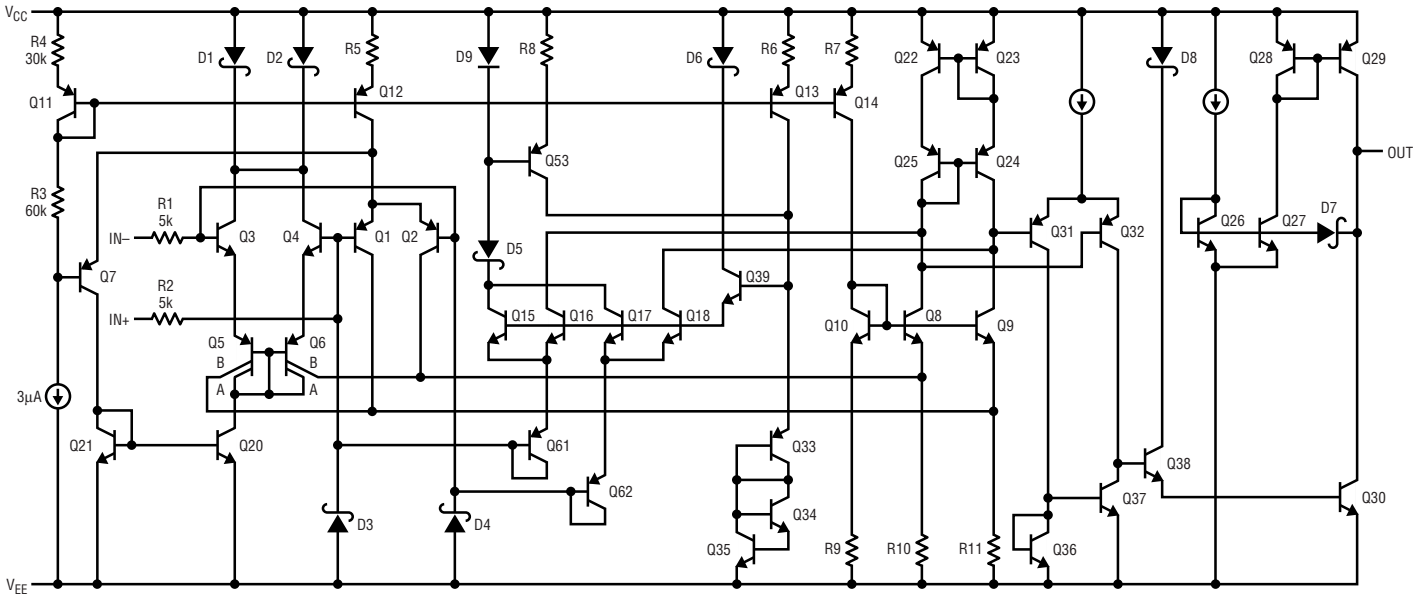


Figure 1. LT1716 simplified schematic

circuitry. The inputs are coupled to the bases of a PNP differential pair (Q1, Q2) and an NPN differential pair (Q3, Q4), as well as the emitters of a secondary NPN differential pair (Q18, Q16) via diodes formed by Q62 and Q61. Q5 and Q6 form a current-mirror biasing stage for the main NPN input pair.

The PNP stage is active when either of the inputs are in the range of about V_{EE} + 0.3V to V_{CC} – 0.8V, delivering differential currents to loads R10 and R11. The biasing section steers current between the PNP stage and the main NPN stage depending on whether the PNP transistors go into cutoff. The NPN stage provides active gain for inputs in the range of about V_{CC} – 0.8V to V_{CC} + 0.3V. The NPN differential currents are passed by the Q5/Q6 pair, arriving at the R10/R11 loads, adding to any currents generated by the PNP stage.

As an input voltage goes above V_{CC} + 0.3V, the NPN gain drops to unity (becomes a diode) and the inputs effectively drive the emitters of Q5/Q6, which continue to mirror currents to the loads R10/R11. During Over-The-Top operation, Schottky diodes D1 and D2 prevent forward biasing of the NPN base/collector junctions, and the PNP stage is completely reverse-biased, effectively removing it from the circuit.

As input voltage falls below V_{EE} + 0.3V the PNP stage becomes saturated and the NPN stage remains off, but the emitter-coupled pair Q16/Q18 becomes active and comes into play to provide a continued differential sensing capability. Signals below V_{EE} – 0.3V are internally clamped by Schottky diodes D3 or D4 and voltage begins to develop across the 5k series input resistors R1 or R2 for voltages down to the rated limit of V_{EE} – 5V. So long as only one input goes under-the-bottom, the comparison function remains correct. Should both inputs drive their clamp diodes into conduction, then the signals look the same to the circuit and the LT1716 output becomes unpredictable, though no harm will come to the device. The differential pair Q8/Q9 serve to combine the R10/R11 signals with the Q16/Q18 outputs to maintain the proper output voltage state over the entire input voltage range.

Figures 2 and 3 show the resulting input current/voltage characteristics of the LT1716. For input comparisons within the rails, the bias currents are very small, in the few nanoamp range, while for Over-The-Top thresholds, a modest 8µA of bias may be required of the higher-potential input signal. For signal-swings below V_{EE}, the 5kΩ protection resistance limits the input current to about –1mA. If desired, external series resistance can be added to reduce the negative-going bias current or to extend the allowable signal swing below V_{EE} to beyond –5V.

Output Architecture

The LT1716 provides its versatile interfacing capability through the use of a specialized output structure. The right-hand portion of Figure 1 shows the output circuitry. Differential pair Q31/Q32 and emitter-follower Q38 provide the differential to single-ended drive for Q30, which is the main output device and provides the pull-down capability of the part. The pull-up feature is accomplished by current mirror Q28/Q29 that is slaved to mirror Q26/Q27. When the output is driven low, Schottky diode D7 conducts and turns off the current mirror stages. The interesting thing about this configuration is that in the high state, the output can be easily forced above V_{CC} by an Over-The-Top load return, reverse biasing D7 and the Q28/Q29 base-emitter junctions. This allows the LT1716 output to behave like an open collector for driving loads up to 10mA, yet providing rail-to-rail output for Hi-Z loading without the pull-up resistor that a traditional open-collector would require.

Some Interesting Design Solutions

Overcurrent Indicator

The LT1716 is well suited to monitoring current in power buses, since the inputs can operate well above the logic-level power supply. An important power bus monitoring function is one that produces a logic signal indicating when an overload condition is taking place. Figure 4 shows a circuit that performs that function using the LT1716.

In this circuit, the LT1716 is powered indirectly from the hot side of the sense resistor, via an LT1643-1.25 shunt reference. The reference permits an accurate offset to be developed (about 120mV) that represents the current-induced drop on the sense resistor at the desired trip point, assumed here to be about 20% over the maximum normal current. The 10MΩ positive-feedback resistor is used to prevent indication chatter at the threshold by producing a consistent 3mV of hysteresis over the range of bus voltages that can be monitored. The 10MΩ connected to the inverting input nominally matches the offset that is induced by the 10MΩ hysteresis resistor. The Schottky diode at the output is used to clamp the LT1716 output at about V_{LOGIC} + 0.3V, to prevent

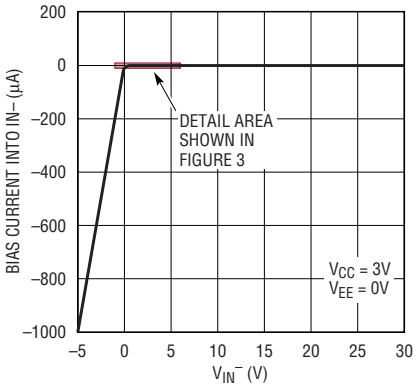


Figure 2. LT1716 input bias current

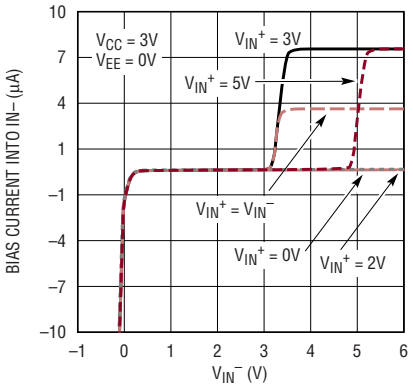


Figure 3. LT1716 input bias current (detail)

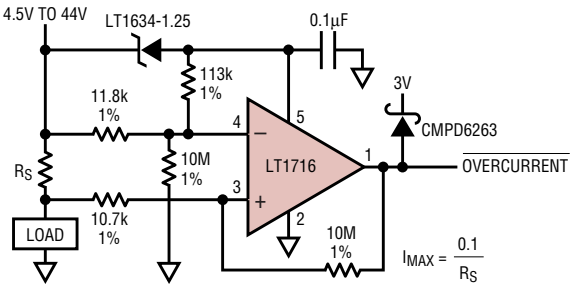


Figure 4. Overcurrent indicator

overvoltage at the logic load and to properly set the hysteresis.

Voltage-Sensing Relay Trigger

Figure 5 shows a circuit that creates a precision voltage-level actuated coil-drive trigger for a miniature relay (or large relay with an additional transistor). With an output capability of sinking more than 10mA, an LT1716 can directly drive low-coil-current relays and provide simple resistor programmable make or break thresholds. This basic circuit offers a convenient solution for providing alarm annunciation or load-protection switching related to DC bus voltage monitoring.

The threshold reference is established by the 1.25V drop of the LT1634-1.25, which is biased by the LT1716 supply current. The resistor divider at the non-inverting input sets the trip-point as a multiplier of the reference. The 10MΩ positive-feedback resistor sets the LT1716 input hysteresis at about 0.5% of the trip voltage for clean state changes and noise rejection. The relay should have guaranteed pull-in capability somewhat below the desired trip-on voltage to allow for the V_{OL} drop and thus ensure that the comparator has full control of the contact state. The Schottky diode at the output provides fast clamping of the relay turn-off transient. The entire circuit uses less than 0.1mA in the "off" state and adds less than 0.4mA to the "on" state current of the relay coil.

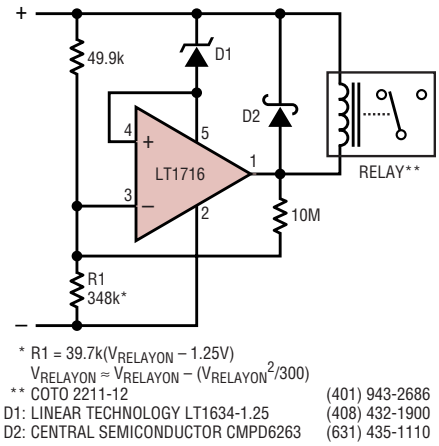


Figure 5. Voltage-sensing relay trigger

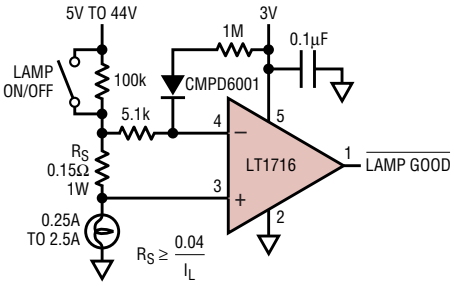


Figure 6. Lamp integrity monitor

Lamp Integrity Monitor

Even with their limited lifetimes, incandescent lamps are still widely used as low-cost hi-level illumination in many products like automobiles and aircraft. With the trend in products to provide more self-diagnostic information, it is optimal to have a circuit that provides a full-time status of the lamp load, whether it is activated or not. Figure 6 shows a circuit using the LT1716 for monitoring a typical automotive lamp-load.

The LT1716 is shown powered from a logic-voltage supply of 3V, while it monitors a lamp powered from a battery system supply like 14V or 28V in vehicles. When the lamp is on, a voltage drop exists across the sense resistor that exceeds the bias-current induced drop on the 5.1kΩ resistor, thereby detecting that a suitable load current is flowing. When the lamp is off, the filament will pull-down through the 100kΩ and the low-leakage diode/1MΩ will cause a slight voltage rise across the 5.1kΩ, signifying to the comparator that the lamp load is intact.

Conclusion

The LT1716 provides the designer with the most flexible power supply and output interfacing options possible in that it has the unique ability to precisely monitor signals that may be completely unrelated to the logic voltage involved. This feature, plus its micropower performance and its easy-to-use SOT-23 footprint, make the LT1716 an ideal choice for integrated system monitoring applications.

LT6550 and LT6551, continued from page 15

introduced to the Y signal summing node to add sync.

Conclusion

The LT6550 and LT6551 triple and quad voltage feedback amplifiers are well suited for use in a variety of video applications. Their high slew rates, fast settling time, and wide input and output ranges make them an excellent choice for 3.3V RGB applications.

For more information on parts featured in this issue, see http://www.linear.com/go/ltmag

Dual Smart Card Interface Simplifies Multicard Reader Designs

by Steven Martin

Introduction

The LTC1955 dual smart card interface provides a complete and compact solution for multicard applications. The LTC1955 and five small capacitors are all that are needed to interface two card sockets to a host microcontroller. Designed to comply with all smart card standards, the LTC1955 can be used for full sized card sockets, smaller vendor card (simlock) sockets, or any combination of smart card and vendor card sockets.

Figure 1 shows the block diagram of the LTC1955, which operates from a battery or a regulated 3.3V supply. The internal charge pump delivers a boosted voltage to two on-chip low dropout regulators. The LDOs provide programmable 1.8V, 3V or 5V regulated outputs to each of the smart card sockets. Two unidirectional channels and one bi-directional communications channel provide the signal translation necessary to interface from a microcontroller at one supply voltage to the smart cards at another supply voltage. Smart card clock and reset control circuits provide the necessary logic functions to prevent glitches or other specification violations during activation or deactivation of the cards. A smart card detection circuit on each channel observes the state of a mechanical switch and delivers the information to the microcontroller after an appropriate debounce period has expired. A simple microprocessor-friendly serial

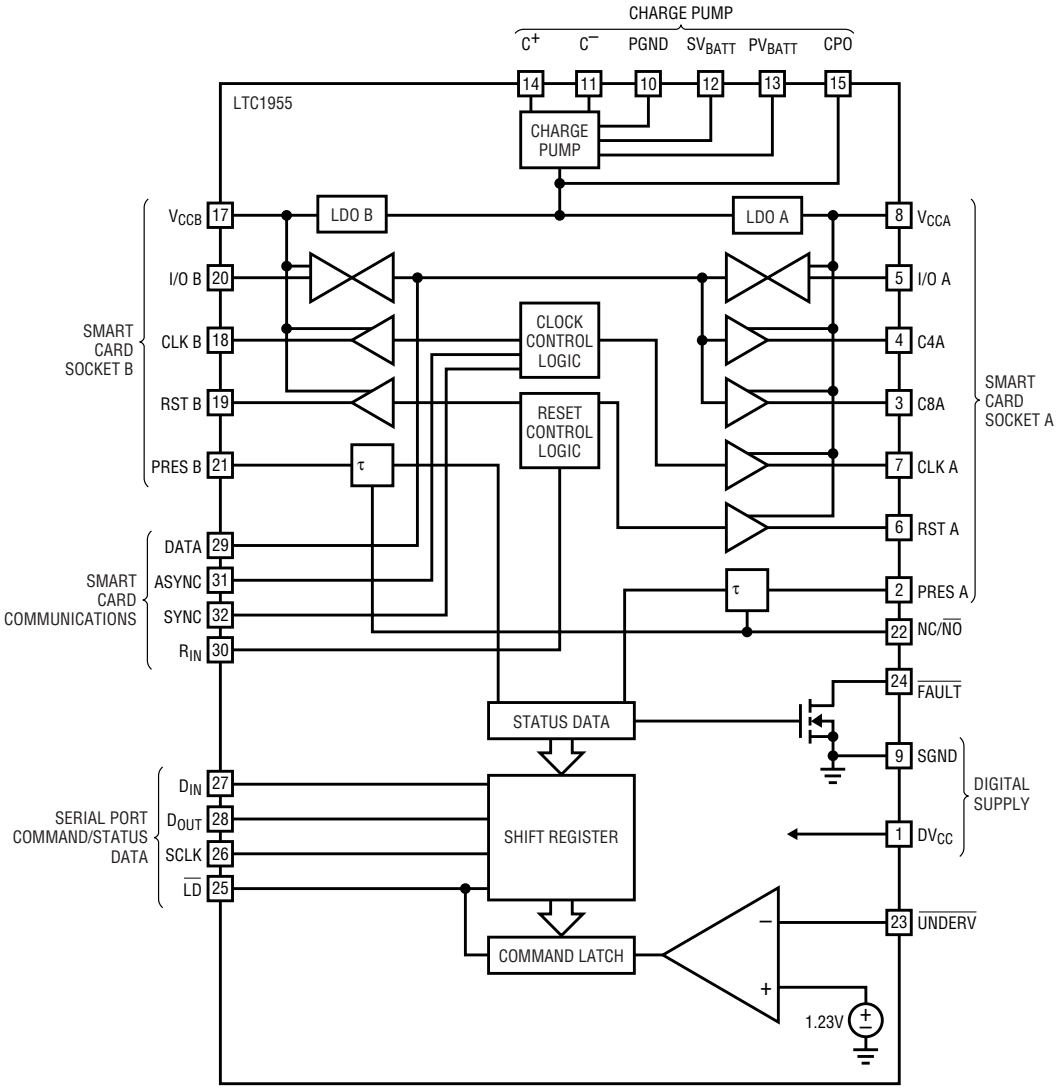


Figure 1. LTC1955 Block diagram

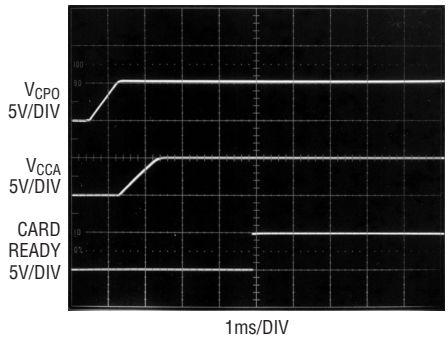


Figure 2. Charge pump and LDO activation

port supplies the data for command and status control, thus minimizing wire count. Finally, the LTC1955 provides all fault detection and ESD protection necessary to comply with both EMV and ISO-7816-3 smart card standards. These include short circuit detection, smart card removal during a transaction, undervoltage and over-temperature faults. In the event of a fault condition, the smart card is properly deactivated and a fault output notifies the microcontroller.

Serial Port

To simplify communication with multiple smart cards, the LTC1955 includes a serial port for control and status data. While command data is sent to the serial port, status data is returned simultaneously. By using a simple 4-wire interface, the LTC1955 is easily controlled by a microcontroller with a dedicated serial port or by bit manipulation of undedicated I/O pins. Since card sockets may be on a separate board from the microcontroller, it's beneficial to keep the number of control and status wires to a minimum. By daisy-chaining several LTC1955s, it is possible to control six cards with the same four serial port wires.

Power Management Unit

In order to support 5V cards from a battery or 3.3V system supply, the LTC1955 includes a voltage doubling charge pump. The charge pump requires only one small flying capacitor, an input bypass capacitor and an output charge storage capacitor to provide step-up capability—no inductors or current sense resistors are necessary. Input sense circuitry determines how much input voltage is available (PVBatt and SVBatt) and determines whether the charge pump should step-up or step-down to provide the required voltage for both cards. For example, if the input supply voltage is 3.3V, and the required smart card voltage is 5V, the LTC1955 operates as a charge pump to deliver the higher voltage. Alternatively, if the input supply voltage is 4V, and the required smart card voltage is 3V or 1.8V, it automatically steps down for improved efficiency.

For maximum flexibility, the LTC1955 includes two low dropout regulators, one for each of the card channels. The LDOs can be independently programmed to 1.8V, 3V or 5V. The LDOs contain fault detection circuitry to determine if a fault, either undervoltage or overcurrent, occurs at the smart card's V_{CC} pin.

The entire LTC1955, including the power management circuitry, is designed to consume low power under light or no load conditions. With no load (e.g. one card powered in clock stop mode) the supply current is nominally only 250µA. This can result in considerable power savings in battery-powered applications. Furthermore the shutdown current is only a few microamperes.

To prevent high inrush current during turn-on, an automatic soft-start circuit ramps the charge pump output (CPO) voltage at a slow rate. Soft start circuits also slow the rise time of the V_{CC} pins when a card socket is activated to avoid start up and interference issues with the charge pump. A status bit in the serial port tells the microcontroller when the output voltage has reached its final value. This signal also enables the communication channels thereby ensuring proper compliance with smart card standards. Figure 2 shows the card supply voltage ramp as well as the internal CARD READY signal indicating that the particular output has reached its final state.

During smart card deactivation, either by user control or by automatic fault deactivation, the LTC1955 correctly sequences the smart card pins to 0V and discharges the smart card V_{CC} pin in under 200µs. Rapid discharge is important to ensure that the card's pins are completely collapsed before the smart card leaves the socket connector. This requirement is specified in various smart card standards.

Smart Card Communication and Control Pins

On the main smart card channel (Channel A) there are four unidirectional pins (CLKA, RSTA, C4A and C8A) and one bi-directional pin (I/OA) for communicating with the smart card. These pins connect directly to the smart card acceptor socket with little or no additional circuitry required.

The I/OA channel, which is an analog I²C™-style input-output, provides level translation as well as short circuit protection. An analog technique is used on this channel to allow true full-duplex communication with the smart card. This is useful for card protocols that require data acknowledge or similar simultaneous "low" assertions.

To meet the stringent rise time requirements imposed by ISO-7816-3 while keeping power dissipation and V_{OL} to a minimum, an accelerator circuit is built into each pull-up current source on this channel. Normally, a small current, I_{START}, pulls each bi-directional pin to its respective power supply rail. An open-drain transistor can easily overcome I_{START} whenever a low is being asserted. When the low is relinquished, I_{START} slowly begins to charge the pin toward its rail again. An internal edge rate detection comparator notices that the node is moving upward and enables a large pull-up current source to assist. Once the larger current source begins to enhance the edge rate of the node, the decision to enhance is reinforced thereby providing a dynamic form of hysteresis. After the node has reached the power supply rail, the comparator resets and only I_{START} is available again. Figure 3 shows the waveform of a bidirectional pin. The 10% to 90% rise time is on the order of 100ns. The DATA pin, which conveys the information to the microcontroller at the correct DC level, has an identical pull up circuit.

I²C is a trademark of Philips Electronics N.V.

Clock and Reset Channels

The clock channels of the LTC1955 provide the level shifted clock signal used by the smart card for synchronization. The clock channels are designed specifically for high speed and can faithfully transmit a 10MHz signal. They also have clock divider modes to be able to accommodate higher system clock speeds. Two clock inputs, SYNC and ASYNC, provide maximum flexibility by allowing the user to connect the cards to a free-running high-speed system clock for asynchronous applications or to an undedicated microcontroller output for synchronous card applications. Clock stop modes, both high and low, are available for power savings in battery applications. In synchronous card applications, either or both cards can be deselected and their clock pins will remain in their current states.

The Reset channels convey the microcontroller's signal to the smart cards and can also be latched either high or low by selecting or deselecting one of the two card sockets.

Both the reset and clock channels are disabled and provide a valid low before the smart card supply voltage has reached its final value. Deactivation can be done manually or it can occur by a fault (e.g. short circuit on a smart card pin) or an undervoltage fault of the entire device. The deactivation sequencing is designed to meet applicable smart card standards.

Additional pins are included on channel A to accommodate older cards that used the C4 and C8 contact locations. These pins are unidirectional (output only) and are controlled by the same data input pin as the smart card I/O pins.

Smart Card Detection Channel

The LTC1955 incorporates a card detection solution that does not require additional de-bounce circuitry or software. This channel detects the presence of a smart card by forcing a small current and monitoring the voltage on a mechanical detection switch. Once a smart card is detected, the channel starts the de-bounce timer.

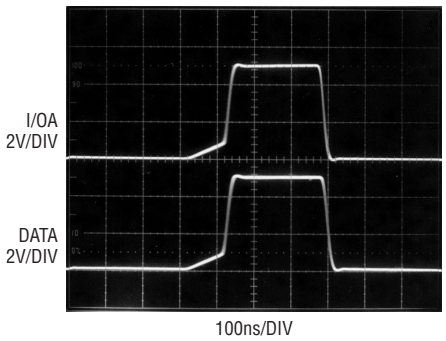


Figure 3. Data – I/O Channel

The presence of a card is reported to the microcontroller only if the card has been present for a minimum of 20ms. The switch sense current is generated by the LTC1955 so no external components are required. Once a valid card indication occurs, the channel alerts the microcontroller by asserting the CARD READY bit in the serial port's status output. On channel A, it is possible to determine the presence of a card by simply observing the state of the DOUT pin without running the serial port.

Fault Detection and Avoidance

Specifications relating to faults on the smart card pins are very stringent. For example, ISO7816-3 (section 1.4.8) specifies that the smart card socket must be capable of surviving a "metal plate" connecting between any or all contacts without damage. To accommodate these fault conditions, the LTC1955 uses voltage sensing on its low impedance pins to detect if that pin is being forced to an inappropriate level. For example, the voltage on the smart card supply pin, V_{CCX}, is compared with an internal reference to determine if a short circuit exists. If a fault persists for a prescribed period, the LTC1955 automatically deactivates the respective smart card and asserts the $\overline{FAULT}$ output. A small timeout period prevents false errors from plaguing the microcontroller. The clock and reset channels respond to faults in a similar way. The digital levels on the outputs of these channels (CLK_X and RST_X) are compared to those being presented at their input. If these signals differ for several microseconds then a fault is declared and the smart card is deactivated. Again, the $\overline{FAULT}$ output alerts the microcontroller that an electrical fault exists. In both cases, since the smart card becomes deactivated, there is no power available to deliver excessive current for a prolonged period.

The bi-directional pins on the smart card sides of the channels are protected against short circuits to the smart card supply voltage by means of a constant current pull down. Instead of a simple pull down transistor to transmit a low to the smart card, these channels use a current source implementation. The 5mA current source provides enough current to meet the edge rate and V_{OL} requirements while limiting the current available during a fault. The available smart card standards specify that no more than 15mA flow during faults on these pins. Of course, short circuits to ground on these channels are indistinguishable from a normal signal and must be detected by the data error checking routines.

Conclusion

The LTC1955 provides all of the necessary level shifting and power circuitry to interface with two smart card sockets. To further reduce board level complexity, the part includes smart card detection channels with built-in debounce circuitry. A straightforward serial port helps reduce the number of wires to the smart card socket board and can easily be expanded to 4- or 6-card applications. Since the LTC1955 provides all of the necessary smart card interface functions, only bypass capacitors and one charge pump capacitor are required for operation. The operation of the LTC1955 is designed for simplicity, and to provide a nearly transparent path to the smart card. Nevertheless, when an electrical error condition occurs, the LTC1955 responds quickly by removing power to the smart card and alerting the microcontroller. The LTC1955 offers all of this functionality in a space saving low profile (0.75mm high) 5mm × 5mm QFN package.

Very Low Dropout (VLDO) Linear Regulator Outperforms Switching Regulators in Low V_{OUT} Applications

by Anthony Bonte

Introduction

Each new generation of computing systems demands more power, lower operating voltages and more supply voltages. CPU core, logic and termination voltages below 1.8V are common. Three or more supply voltages are the norm, where a high efficiency synchronous switching regulator typically generates each voltage. These systems have stringent output voltage regulation specifications for input voltage change, output load current change, temperature change and output load step response. These requirements mandate the need for an accurate, high-speed regulator. In applications that draw 1A–10A of output current, a VLDO™ linear regulator that operates from a low V_{IN} has several advantages over a switching regulator. A VLDO consumes less board space, requires fewer components and costs less than a switcher solution. When the input-to-output voltage differential is low, efficiency is comparable. Figure 1 shows a VLDO replacing a switching regulator in a multiple supply system.

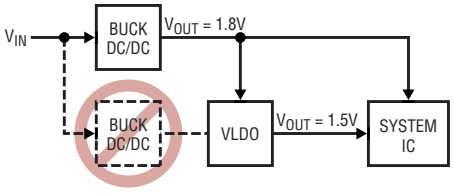


Figure 1. VLDO replaces a switching regulator in a multiple output power supply

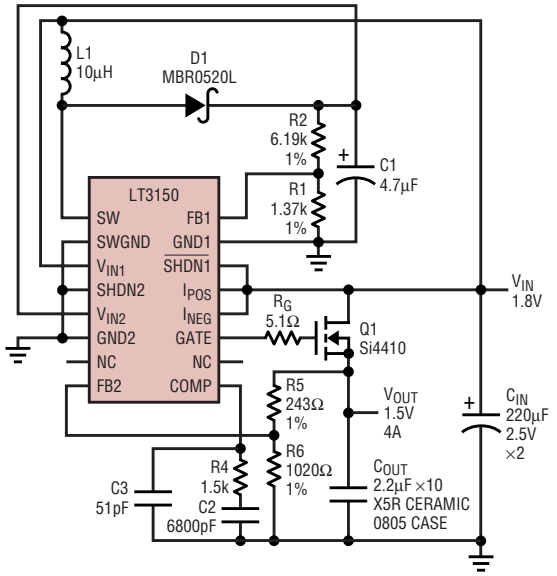
The LT3150 VLDO Combines Accuracy, Fast Response and High Efficiency

The LT3150 controller drives an external N-channel MOSFET as a source follower to create an extremely low dropout, ultra-fast transient response linear regulator. The MOSFET $R_{DS(ON)}$ sets the dropout voltage performance and dropout voltage is proportional to the output load current. The LT3150's precision-trimmed reference provides ±0.6% initial accuracy, ±1% tolerance over temperature and accommodates low-voltage outputs. Transient response performance is optimized around low cost, low ESR, readily available ceramic capacitors. Depending on the individual power supply requirements, the output decoupling network typically consists of multiple 1µF–10µF ceramic capacitors in parallel. Eliminating bulk output capacitors significantly reduces cost.

The LT3150 includes a fixed frequency boost regulator that generates gate drive for the external N-channel MOSFET. The internally compensated current mode PWM architecture combined with a 1.4MHz switching frequency permits the use of tiny, low cost capacitors and inductors. The LT3150 also incorporates current limiting, on/off control for power supply sequencing and overvoltage protection or thermal shutdown with a few external components.

1.8V to 1.5V Linear Regulator

Figure 2 shows a 1.8V to 1.5V linear regulator employing the LT3150 and all surface-mount components. The regulator provides up to 4A of output current using a low-cost, logic-level Siliconix Si4410 N-channel MOSFET for Q1, the pass element. The boost converter composed of L1, D1, R1–R2 and C1 generates a 6.8V gate-drive supply for Q1. The circuit's dropout voltage at 4A is typically 65mV. Due to the low input-to-output voltage differential, efficiency for this circuit is 83.3%. Figure 3 shows the well-behaved transient response of the circuit. Only 22µF of output capacitance limits a 3.9A load step with 50ns rise/fall times to just ±55mV peak deviation in the output. R4, C2 and C3 provide



CIN: PANASONIC SP SERIES EEFUE0E221R 20% (714) 373-7334
C1: AVX TAJA475M020R 20V 20% (207) 282-5111
L1: MURATA LQH32CN100K11 OR SUMIDA CDRH3D16100 (814)237-1431

Figure 2. 1.8V to 1.5V, 4A very low dropout linear regulator (typical dropout voltage is 65mV at 4A)

LT3150 Features

- ❑ Fast transient response optimized with ceramic output capacitors
- ❑ MOSFET $R_{DS(ON)}$ defines dropout voltage
- ❑ ±1% reference tolerance over temperature
- ❑ Multifunction LDO shutdown pin with latchoff
- ❑ Fixed frequency 1.4MHz boost converter generates MOSFET gate drive
- ❑ Current mode PWM boost converter uses tiny capacitors and inductor
- ❑ Independent boost converter shutdown pin permits LDO V_{OUT} supply sequencing
- ❑ Available in 16-Lead SSOP package

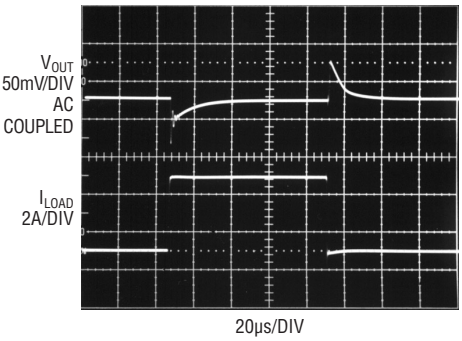


Figure 3. Transient response for a 0.1A to 4A output load step

loop frequency compensation tailored to Q1 and C_{OUT}'s characteristics. Given a worst-case maximum input supply voltage of 1.9V and 4A maximum load current, the Si4410 dissipates 1.6W. Temperature rise in Q1 is about 40°C. No airflow or additional heatsinking beyond that provided by a proper PCB layout is required.

No R_{SENSE} Current Limit

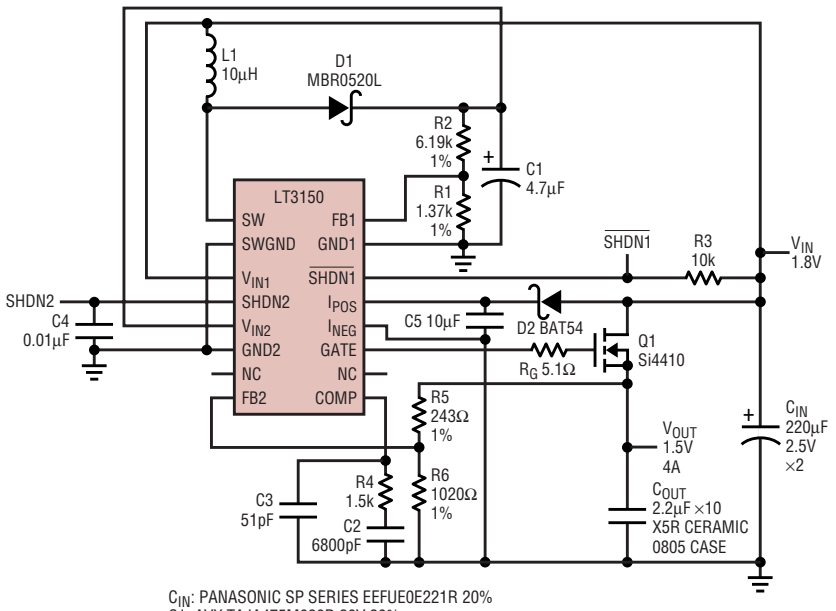
The circuit shown in Figure 2 does not provide any output current limiting under a fault condition. In this scenario, the DC/DC converter generating the 1.8V input supply is the only source of protection and the assumption is that it provides current limiting. Figure 4 shows a solution for users who need further protection but don't want to impact dropout voltage with the loss across a sense resistor. This circuit utilizes the LT3150 No R_{SENSE}™ current limit scheme, which employs a programmable timer. The user sets a time-out period, via C4 at the SHDN2 pin, that limits the duration of a fault condition before latching the VLDO controller off.

The I_{NEG} pin connection to ground activates the No R_{SENSE} internal circuitry. A fault condition, such as an output short circuit, starts the timer at the SHDN2 pin because internal circuitry detects that the GATE pin is driven to within 1V (typically) of the positive rail. During the time-out period, C5's reservoir provides power to the I_{POS} pin's internal circuitry. D2 reverse-biases if V_{IN} is in current limit and its voltage collapses. After exceeding the time out period, V_{OUT} is shut down and latched off. To restore normal operation, reset the timer capacitor with an active pulldown or cycle power to the V_{IN2} pin while providing an external bleed path for the timer capacitor.

Note that this technique does not limit the MOSFET current during the time-out period. Only the input power supply and the input-to-output impedance limit output current. The timer period is set to keep Q1 within its SOA (safe operating area) and its temperature rise under control. Savvy engineers will recognize that this technique imposes two restrictions; a very slow input supply ramp and operation in dropout both activate the timer. Applying the input supply of 1.8V within 50ms starts this circuit properly. Also, a logic signal at the $\overline{SHDN1}$ pin provides on/off control and provides power supply sequencing for the LDO output. As an example, holding this pin low until the 1.8V supply is stable eliminates the input supply startup ramp considerations for the 1.5V supply.

Conclusion

An LT3150-based solution is a cost- and space-saving alternative to a switching regulator in low output voltage applications down to 1.2V. The LT3150 combines the benefits of low input voltage operation, very low dropout voltage performance, precision regulation and fast transient response. The LT3150 drives a variety of MOSFET pass elements, making it simple to scale output power and dropout performance.



CIN: PANASONIC SP SERIES EEFUE0E221R 20%
C1: AVX TAJA475M020R 20V 20%
L1: MURATA LQH32CN100K11 OR SUMIDA CDRH3D16100

Figure 4. 1.8V to 1.5V, 4A VLDO linear regulator with No R_{SENSE} current limiting and on/off control

Next Generation No Compromise Battery Chargers

by Mark Gurries

Introduction

Until now, a *fully-featured* high power battery charger simply did not exist in a single IC. No one had succeeded in squeezing a charger into a small package without compromising some functionality, such as wide voltage range, current range, accuracy, low external part count, or efficiency.

For instance, some single-IC chargers focus on the analog PWM power control side of charging while others just perform the charge termination function. None offered it all in one package, until now.

Linear Technology introduces a family of complete single-IC high power battery charger solutions that *do not compromise any functionality* for small IC size. The new LTC4006, LTC4007 and LTC4008 series of battery chargers pack all of the most desirable charge and protection features into a single IC. These devices also offer novel features that save board space, and modern I/O features for communication with host systems

The First True, All-In-One, No Compromise Battery Chargers

The LTC4006, LTC4007 and LTC4008 battery chargers share a new control architecture, and each device combines many desirable features into a single package, including:

- ❑ Support for batteries up to 28V at charge rates up to 4A with efficiencies higher than 95%.
- ❑ Typical charging voltage and current accuracy is 0.8% and 4% respectively.
- ❑ The PWM controller is a 300kHz synchronous architecture capable of achieving 98% maximum duty cycle for excellent low dropout performance and continuous switching down to zero charge current. The PWM controller is designed to be stable with and suppress the audible noise from ceramic input/output capacitors while also allowing the use of popular 10µH inductors for small size at high currents.
- ❑ A low current sense voltage allows the use of small size and low value current sense resistors. Small IC size, low external part count and the use of small external components result in a very small circuit board footprint.
- ❑ An overvoltage comparator protects against battery over voltage conditions and suspends PWM activity at logic speeds. Input current limiting automatically reduces charge current to prevent overloading the power adapter. A series input MOSFET also provides power adapter protection from reverse battery discharge.
- ❑ All of the chargers have shutdown (SHDN) input pins. If the input power is removed, the charger isolates the voltage feedback path and turns off unneeded internal IC circuits to bring the reverse battery drain current down to only 15µA.
- ❑ A flexible thermistor circuit can be used to monitor battery or ambient temperature.
- ❑ All of these devices have the ability to externally monitor the charge current flowing into the battery.

This just covers the basic feature set. There are other features that differentiate the devices.

So What Are the Differences?

Table 1 compares the three battery chargers.

The LTC4006 and LTC4007 are configured specifically for charging Li-Ion batteries and contain full charge termination and auto restart control. The LTC4008 does not include charge termination support so that it can work with more than just Li-Ion batteries—a host microcontroller can manage the specific charge termination requirements for the particular battery chemistry in use.

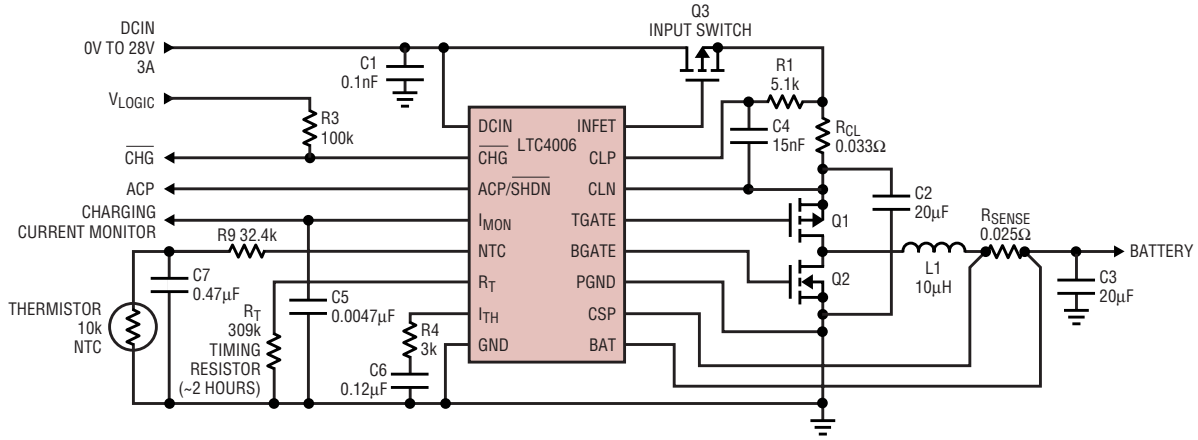


Figure 1. 4A Li-Ion Charger

Table 1. Individual feature matrix (all parts have a shutdown SHDN pin. "Dash Part" means option ordered by part number.)

PART / FEATURE	LTC4006	LTC4007	LTC4008
Voltage Selection	Dash Part 8.4V, 12.6V, 16.8V	Pin Programmed 12.3V, 12.6V, 16.4V 16.8V	Resistor Divider
Voltage Accuracy	0.6% Typ, 0.8% Sys Max	0.8% Typ, 1% Sys Max	0.8% Typ, 1% Max
Current Programming	Sense R	Program R + Sense R	Program R + Sense R
AC Present	Merged with SHDN	●	Merged with SHDN
Charge Termination Timer	●	●	
Low Battery Conditioning	●	●	
Auto Restart Capability	●	●	
Charge State Flag (CHG)	●	●	
Low Bat Flag		●	
C/10 Flag	Merged with CHG	●	●
Fault Flag		●	●
Input Current Limit Flag		●	●
Available without INFET			● (Dash Part)
IC Package	SSOP-16	SSOP-24	SSOP-20

The LTC4006, in an SSOP-16 package, is the smallest of the three; the LTC4007 brings out the maximum number of status monitoring and control signals in a slightly larger, SSOP-24 package.

Battery Charge Termination and Management

The LTC4006 and LTC4007 have on board Li-Ion charge termination capability and over discharge recovery systems. The charge termination system consists of a 2-stage timer and a C/10 charge current detector. The C/10 detector looks for the charger current to fall below 10% of the full-scale current and changes the timer period to 1/4 of the original period. The second time period is used to minimize undesirable float charge time conditions especially if a full battery is inserted into the charger. The watchdog timer period is set by a timing resistor.

The LTC4006 and LTC4007 also have a built in Li-Ion over discharge recovery system called preconditioning. If the initial voltage of the battery is below a preset value, the charger reduces its charge rate to 10% of the full scale current value and maintains that charge rate until the battery voltage goes above a set value.

Both ICs also have an auto-restart capability. If the battery voltage falls below a preset value, the charger automatically restarts the charge process to maintain full charge.

The LTC4006 and LTC4007 have a charge status signal, which indicates when the battery is being charged, and a current monitor pin, which monitors the actual charge current flowing into the battery.

Even though the LTC4008 does not have any of the charge termination timing and preconditioning functions, it does provided a C/10 status flag and charger current monitoring for the host system to use for the same purpose.

Charge Fault Management

All three of the ICs have built-in fault management systems that suspend or shut down the charger for various fault conditions.

The first line of defense is a user-adjustable temperature limit circuit that can work with both NTC or PTC type thermistors. When a temperature fault is detected, charging is suspended until the temperature returns to normal.

The LTC4006 and LTC4007 also monitor the timer state in the preconditioning phase and shut down the charger when the timer times out. The timer runs during this conditioning phase at 1/4 of the original timer period. If the battery voltage has not recovered above the set voltage point before the timer times out, the FAULT flag is set.

The C/10 flag, normally used to indicate an almost full battery, is also protected from premature tripping caused by an active input current limiting condition that forces the charge current to fall below the C/10 trip point. When the input current limit condition is removed, the C/10 flag is allowed to function again.

The LTC4007 and LTC4008 also provide an input current limit flag to tell the system when the adapter is running over 90% of it current capacity. An overvoltage comparator looks for sudden loss of a battery load, com-

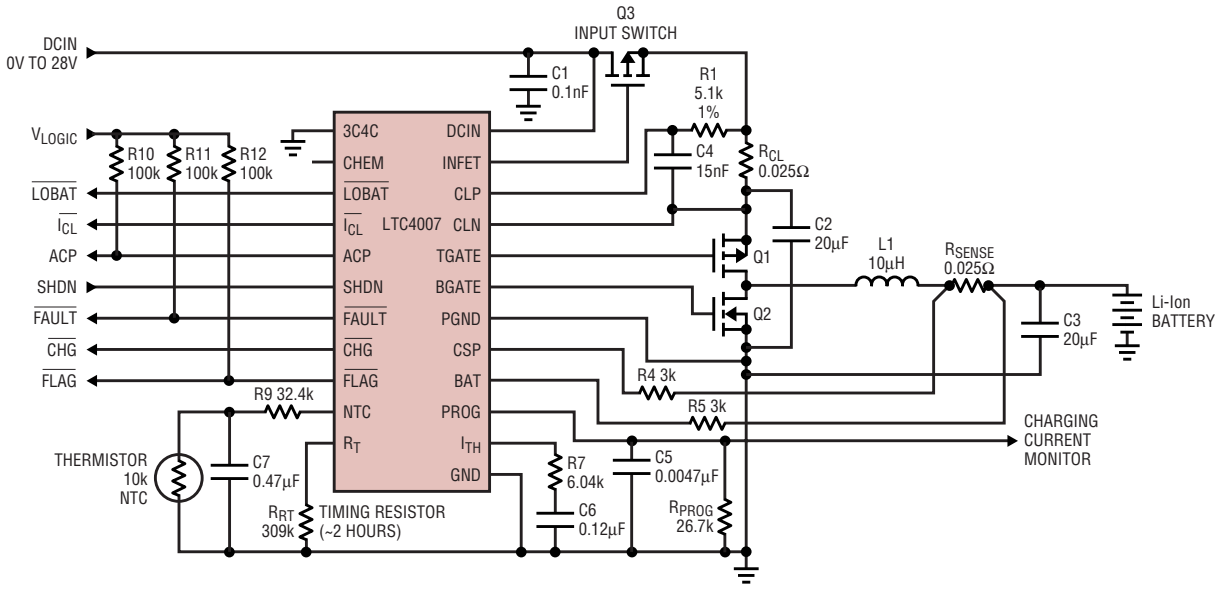


Figure 2. 12.6V, 4A Li-Ion charger

mon in pulse charge applications, and instantly suspends PWM activity when the voltage goes above the programmed voltage by 7%. However, this is more than just a logic function. The charger stays suspended until the internal feedback loop catches up and reports the need to supply current to the load to maintain proper voltage regulation. In other words, recovery is under the analog feedback loop control.

High Performance

The LTC4006, LTC4007 and LTC4008 chargers are designed around a whole new architecture that is quasi-constant frequency, constant off time controller that switches continuously, even with no load current. Normally the charger operates over a wide duty cycle range like a traditional PWM controller running at 300kHz. However as the duty cycle enters the high 80% range, feed-forward circuits looking at V_{IN} and V_{OUT} determine a new nominal switching frequency below 300kHz. Under very low dropout, very high duty cycle conditions, the switching frequency could go down into the audible frequency range on its way to 0Hz (100% DC). However, the charger has an internal timer that prevents the charger from switching activity below 25kHz but still allows the IC to achieve a maximum 98% duty cycle. With a synchronous rectifier, not only are high current applications supported at efficiency levels greater than 95%, but the switching activity is continuous and independent of the load current. Under no load conditions, there is no pulse skipping which can both generate audible noise and provide poor load regulation. Current and voltage accuracy have been improved over older LTC battery chargers in this class. Current accuracy is now 4% typical with 5% over temperature for both charge current and input current limiting. Output voltage reference accuracy is now 0.8% typical with 1% over temperature.

Finally the ICs feature a reverse battery current blocking FET called the INFET (input FET) function, which

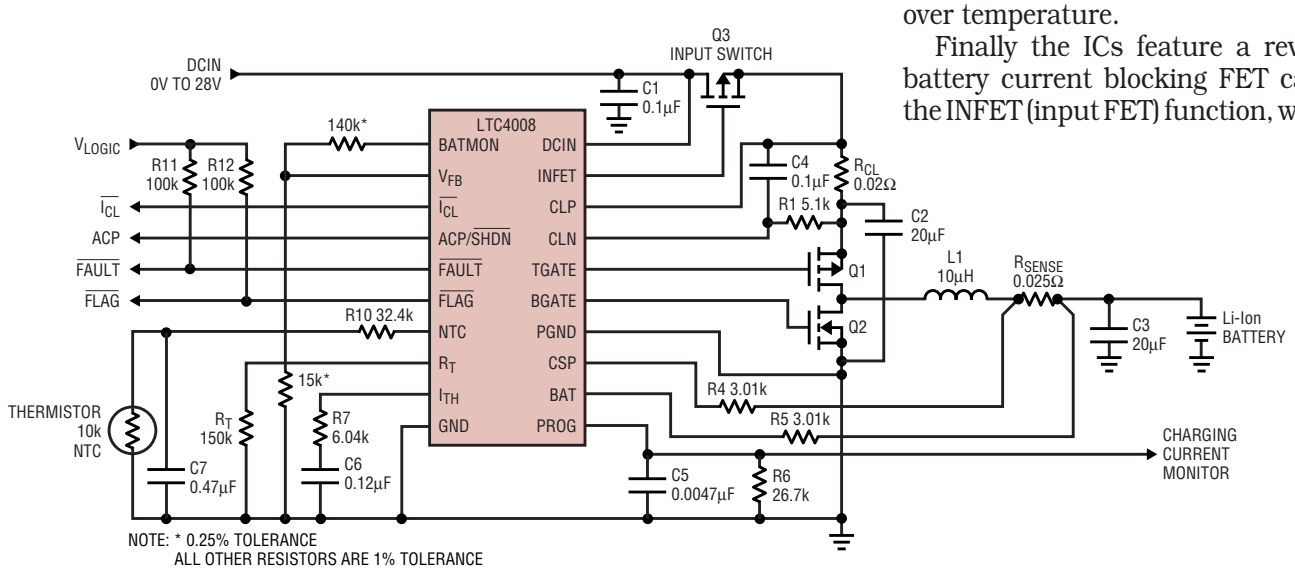


Figure 3. 12.3V, 4A Li-Ion charger

uses a P-channel MOSFET located in series with the wall adapter power path. This MOSFET functions like a lossless ideal diode—replacing the large series diode that is used to prevent battery current from going back to the power adapter. The MOSFET is actively driven in a linear mode to maintain a constant 25mV forward voltage, which makes the MOSFET act as an ideal diode when forward current flows yet allows fast (10µs) cutoff when a current reversal is sensed.

Small PCB Footprint

Traditionally, high current chargers require a large number of external support components, but the LTC4006, LTC4007 and LTC4008 offer features to push solution size down.

For instance, N-channel MOSFETs are traditionally used in high current applications because of their lower $R_{DS(ON)}$. Today, P-channel MOSFETs offer the performance that N-channel MOSFETs were offering only a couple of years ago. Moving from an N-channel to a P-channel MOSFET drastically simplifies the design of the charger circuit. There are no boosted topside gate drive supplies to deal with, saving components and IC pins.

Increasing the switching frequency reduces the inductor size and output capacitance requirements. Loop response is also improved, further reducing the output capacitance such that small ceramic capacitors can be used. Using a 100mV regulation point for current sensing, small 1206 sized sense resistors can be used.

The INFET circuit is also used to generate the AC present flag without requiring an extra comparator to detect the presence of a power adapter. Finally, improved internal circuit design leads to further reduction in both pin count, part count and the size of each external component needed to make the IC work.

These features add up to an overall system solution that meets the needs of today's smaller products.

Conclusion

The LTC4006, LTC4007 and LTC4008 integrate more functions in smaller circuit footprints than any high power battery charger IC available today.

The LTC4006 and LTC4007 provide simple standalone solutions for complete Li-Ion battery care without the need to write software programs and/or design a complex battery charger control system. The LTC4006 is targeted for applications where small circuit size is most important. If complete monitoring or limited host control of the charge process is desired, the LTC4007 offers a complete set of feedback, status and control signals. Finally, the LTC4008 is a general purpose charger that works with multiple battery chemistries by offering direct control over the entire charge process.

LT1934, continued from page 8

microcontroller coding. On the other hand, its charge status and AC-present pins provide useful information to the user through LEDs or to a microcontroller through a few digital I/O pins, making it simple to integrate into a battery powered system.

Hot Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LT1934 and LT1934-1 circuits. However, these capacitors can cause problems if the LT1934 is plugged into a live supply.[1] The low-loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LT1934 can ring to twice the nominal input voltage, possibly exceeding the LT1934's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LT1934 into an energized supply, the input network should be designed to prevent this overshoot.

Figure 7 shows the waveforms that result when an LT1934 circuit is connected to a 24V supply through six feet of 24-gauge twisted pair. The first plot is the response with a 2.2µF ceramic capacitor at the input. The input voltage rings as high as 35V, and the input current peaks at 20A. One method of damping the tank circuit is to add another capacitor with a series resistor to the circuit. In Figure 7b an aluminum electrolytic capacitor has been added. This capacitor's high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit. An alternative solution is shown in Figure 7c. A 1Ω resistor is added in series with the input to eliminate the voltage overshoot (it also reduces the peak input current). A 0.1µF capacitor improves high frequency filtering. This solution is smaller and less expensive than the electrolytic capacitor. For high input voltages its impact on efficiency is minor, reducing efficiency less than one half percent for a 5V output at full load operating from 24V.

Voltage overshoot gets worse with reduced input capacitance. Figure 7d shows the hot plug response with a 1µF ceramic input capacitor, with the input ringing above 40V. The LT1934-1 can tolerate a larger input resistance, such as shown in Figure 7e where a 4.7Ω resistor damps the voltage transient and greatly reduces the input current glitch on the 24V supply.

Conclusion

The LT1934's 34V input range and short circuit robustness make it a great choice for small industrial systems. It delivers up to 300mA output with an all-surface-mount circuit that requires no heat sinks. The integrated power switch, SOT-23 package and high frequency operation result in a very small regulator, requiring less than one square centimeter of PCB area. Efficiency is high over the entire load range, with the 12µA quiescent current extending battery life.

Notes

1. See Linear Technology Application Note 88 for a complete discussion.

–48V Hot Swap Controller Offers Comprehensive Protection for Telecom Systems

by YK Sim and Mitchell Lee

Introduction

High performance, high reliability telecom systems employ distributed power modules to generate low voltage, high current supplies from a –48V bus. These systems require that the individual power modules are hot swappable—they can be inserted and removed at any time without affecting the operation of the main system. Another requirement is that failed elements self-isolate without affecting neighboring elements. The system controller takes notice of any failures and reconfigures the system so that there is no interruption of service. The system controller also signals for service, providing failed board identification and diagnostic details. In order to perform these tasks effectively, the system controller requires a solid first line of defense, specifically a Hot Swap™ controller on the front end of each and every card.

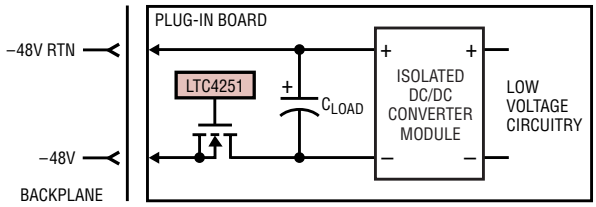


Figure 1. Basic LTC4251 Family Hot Swap Topology

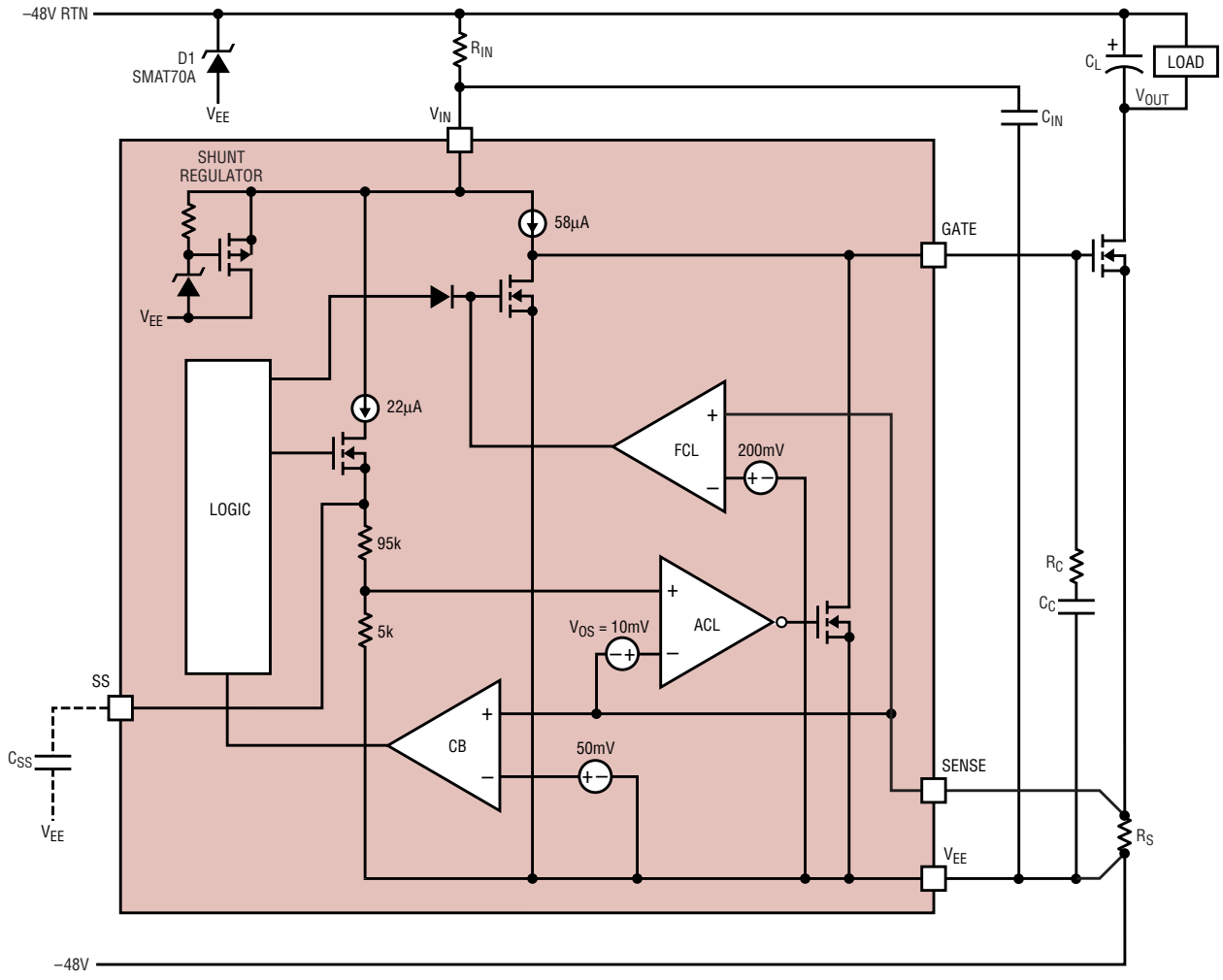


Figure 2. Low-side MOSFET Hot Swap scheme

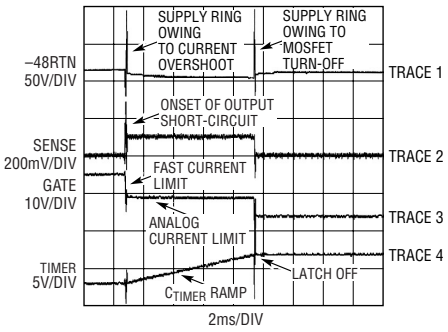


Figure 3. Output short-circuit behavior

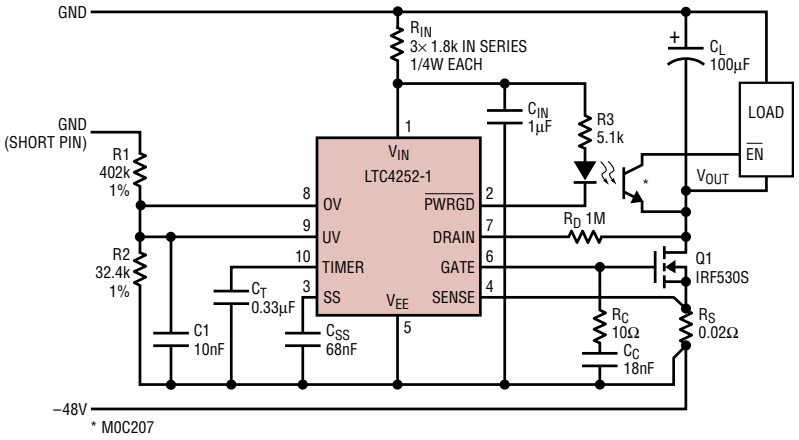


Figure 4. –48V/2.5A LTC4252-1 Hot Swap controller

The new LTC4251, LTC4252 and LTC4253 Hot Swap controllers offer comprehensive circuit protection for –48V applications (and higher) through three stages of current control. They protect the system bus from hot swapped power modules and they protect the power modules from glitches on the system bus. These devices are available in a variety of configurations to fill almost any application need.

Figure 1 shows the major elements of a hot swappable power module. During insertion or commutation of a short circuit fault, the power supply bus can ring to more than twice its nominal supply voltage, easily exceeding the absolute maximum supply rating of most devices. The LTC4251 family uses a floating supply topology with a low side MOSFET drive and a shunt regulator to solve this problem. Thus, operation is limited only by MOSFET voltage and current ratings.

The MOSFETs in Hot Swap circuits are fully enhanced to achieve the lowest on resistance in normal operation. A low resistance MOSFET is chosen because of its low insertion loss and the fact that it does not require a heatsink. The problem is that with a low impedance load fault, huge currents are drawn from the bus, which in turn collapses the bus voltage. Neighboring boards see the loss of bus supply and may reset or fail if the voltage dip lasts too long.

3 Stages of Current Control

The LTC4251 family employs three stages of current limiting to protect the MOSFET and minimize bus disturbances:

- ❑ A timed circuit breaker
- ❑ Active current limiting
- ❑ Fast feedforward path that limits peak current under worst-case catastrophic fault conditions

The LTC4251 family isolates major faults with the fast current limit comparator, FCL as shown in Figure 2. When the SENSE voltage across the current sensing resistor, R_{SENSE} exceeds four times the circuit breaker limit of 50mV, the gate of the external MOSFET is immediately discharged. When the fast comparator no longer detects the excessive sense current, it releases the GATE. Charge stored in the compensation capacitor recharges the GATE while the analog current limit amplifier (ACL) swings in to regulate the sense current to approximately twice the circuit breaker current limit.

With such a fault, the bus voltage collapses at first but quickly recovers when the MOSFET limits the current and isolates the fault. Stray bus lead inductance glitches are clamped by the transient suppressor diode, D1 before reaching MOSFET breakdown voltage. Without D1, the glitch avalanches the MOSFET, interfering with the analog current limit loop.

Figure 3 shows the waveform for a short circuit failure in the power module. The –48VRTN sags a little due to the bus supply load regulation. The SENSE pin voltage briefly peaks to more than four times the circuit breaker voltage at the onset of the fault, but quickly drops to twice the circuit breaker voltage during analog current limiting. The GATE pin is ripped downwards by the fast comparator with a slight voltage undershoot. The undershoot is corrected by the charge from the compensation capacitor C_C. During this fault interval, the circuit breaker comparator (CB) sets the TIMER pin to charge up. When the circuit breaker timer trips, the GATE pin is pulled down, shutting down the MOSFET before it exceeds its safe operating area. The benefit of fast current limiting is obvious from the very short disturbance on the bus supply not causing a circuit breaker trip.

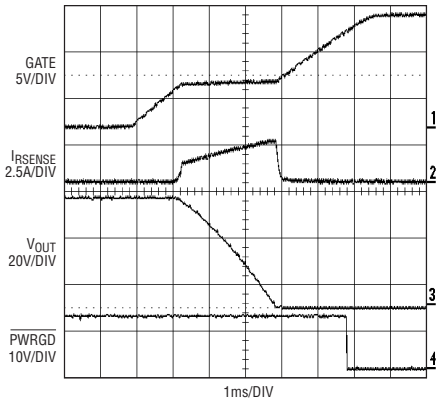


Figure 5. LTC4252 start-up behavior

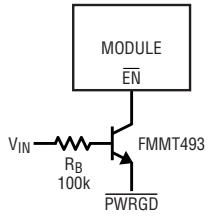


Figure 6. NPN interface between PWRGD and module

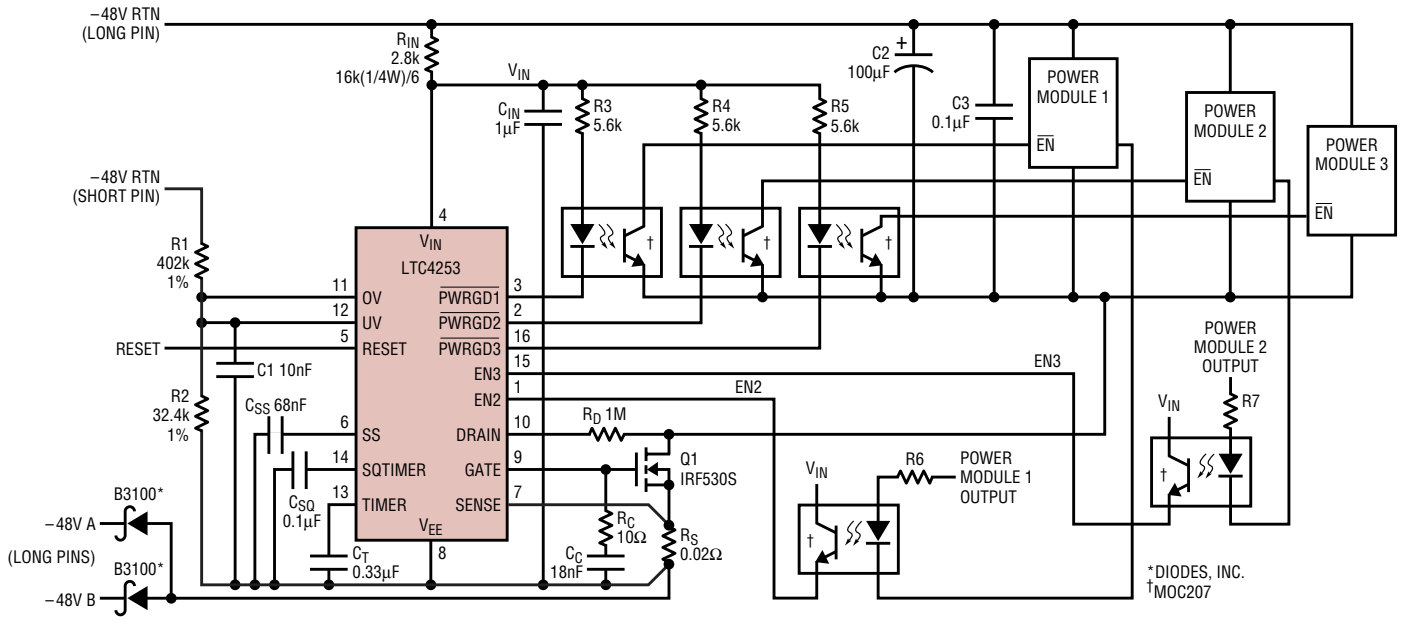


Figure 7. –48V/2.5A Hot Swap sequence controller

Latchoff vs Auto-Retry

When a timed circuit breaker fault occurs, the devices in the LTC4251 family (except the LTC4252-2) latch off and wait for service. The fault latch can be reset by an external pull down device at the TIMER or UV pin. In the LTC4252-2, the TIMER pin starts a retry sequence after allowing a programmable time for the MOSFET to cool.

Floating Shunt Regulator

LTC4251 family uses a simple, fast-responding shunt regulator that floats at the negative bus terminal. This allows the Hot Swap controller, in theory, to adapt to any power supply bus of –24V or more. Wide range supplies, such as those encountered in the telecom world are easily handled by the LTC4251 family's 15:1 shunt current range. Even more dynamic range is available on a transient basis—a guaranteed 50:1 over the operating current—so that the device can operate without interruption in a noisy, spike-ridden environment.

Start-Up Behavior

The current limiting feature of the LTC4251, LTC4252 and LTC4253 makes soft-start (output load voltage ramping) less essential than it would be in a non-current-limiting circuit. Nevertheless, the LTC4252 and LTC4253 offer a current soft-start pin that acts as the reference for the analog current limit amplifier. By attaching a capacitor, the sense current can be modulated at start-up. Figure 5 shows the start-up behavior of the circuit shown in Figure 4.

Undervoltage and Overvoltage Detectors

Programmable undervoltage (UV) and overvoltage (OV) detectors disconnect the load whenever the input supply exceeds the desired operating range. The UV detector enables the device to function above a preset threshold while the OV detector disables the chip above a preset threshold. The LTC4251 (except the LTC4251-2) and LTC4252 MS8 have a single pin with both UV and OV detect function. The external resistor divider (R1 and R2) sets the standard telecom operating range. The LTC4252 MS10 and LTC4253 have separate pins for UV and OV so they can be independently programmed. Separate UV and OV pins allow other user programmable settings. LTC4251-2 has its OV function internally disabled.

Timer with Drain Voltage Accelerated Response

A multifunction timer delays the initial start-up from undervoltage input or internal undervoltage lockout, controls the circuit breaker response time, and controls shutdown cooling timing for LTC4252-2 in auto-retry mode. The

continued on page 38

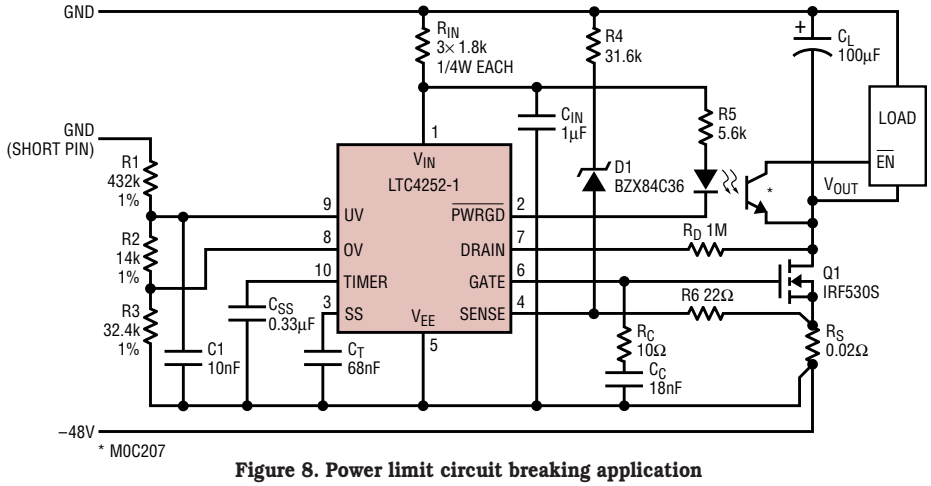


Figure 8. Power limit circuit breaking application

Compact Solution Uses USB Power to Run a Device and Simultaneously Charge its Battery

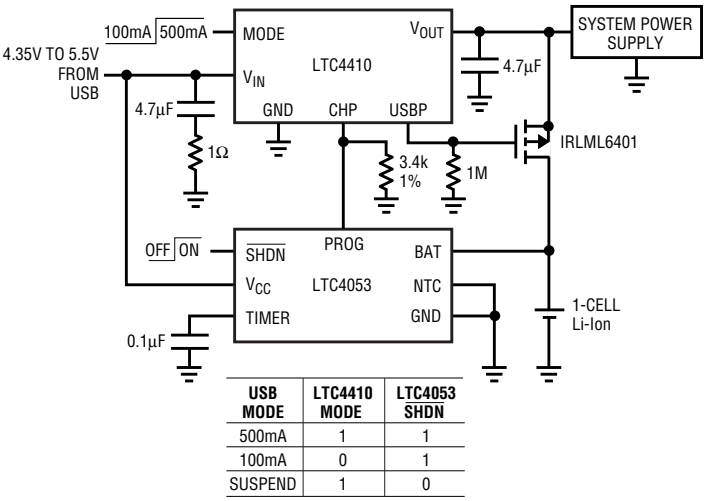
by George Humphrey

Introduction

Increasing numbers of portable devices are tapping into the Universal Serial Bus (USB) to charge their batteries. USB power supplied by the host allows batteries to be recharged at the same time data transfer is occurring, and in some cases, eliminates the need for a bulky wall adapter. The challenge is to provide battery charging and device operation simultaneously in the most efficient manner, while not exceeding either 100mA or 500mA as required by the USB specification.

USB Power Manager and Battery Charger

Figure 1 shows a circuit that allows simultaneous battery charging and device operation using USB power. The LTC4410 USB power manager is a PowerPath™ controller that controls the current that the LTC4053 Li-Ion charger uses to charge the battery. The circuit reduces the battery charging current as the system load current increases, and likewise increases the battery charging current as the system load decreases. This helps to keep the total current within USB spec (assuming the powered device never tries to draw more than the USB spec allows).



USB MODE	LTC4410 MODE	LTC4053 SHDN
500mA	1	1
100mA	0	1
SUSPEND	1	0

Figure 1. USB power manager and battery charger

The battery charge current is set externally with a 3.4kΩ resistor on the PROG pin of the LTC4053, where:

$$I_{BATT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1000 = \frac{1.5V}{3.4k\Omega} \bullet 1000$$

$$= 441mA$$

This is within the 500mA limit imposed by the USB spec. The USB device operating load (I_{LOAD}) is powered through the LTC4410's low voltage drop P-Channel MOSFET switch. The CHP pin produces a replica of the load current equal to $I_{LOAD}/1000$. This current flows to the PROG pin of the LTC4053 where it alters the charge current by the following:

$$I_{BATT} = \left[\left(\frac{1.5V}{3.4k\Omega}\right) - \left(\frac{I_{LOAD}}{1000}\right)\right] \bullet 1000$$

As I_{LOAD} current increases, the battery charging current decreases, to keep the total to less than 500mA. This allows the device to be used even while the battery is charging. The LTC4410 guarantees that the charger current is

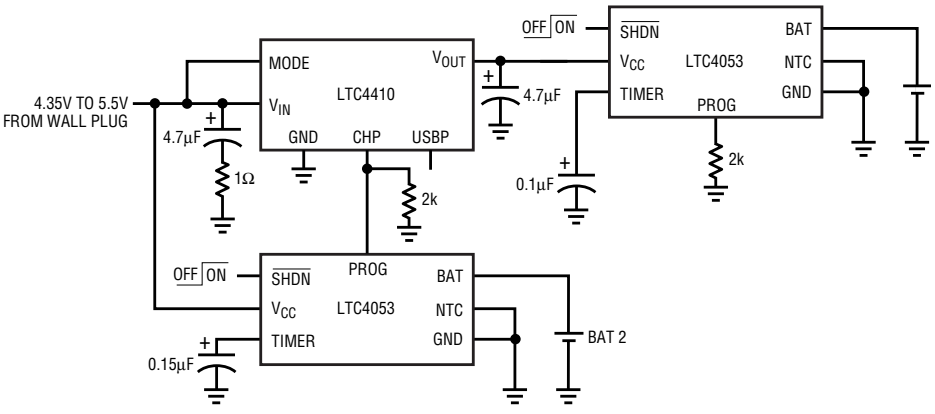


Figure 2. Priority dual battery charging with a wall adapter

reduced to zero when I_{LOAD} = 500mA, or 100mA, depending on the specific USB mode of operation. Note that the LTC4410 can lower the charger current to zero, but it will not limit I_{LOAD}. It is assumed that the load device circuitry draws no more than 500mA, or 100mA, from the USB host.

The LTC4410 MODE pin provides the decoding for the LTC4053 to make it compatible with the different USB modes (100mA, 500mA and Suspend, which are required by the USB specification 1.0 and 2.0 power requirements). When an external controller drives the MODE pin low, an internal circuit sources an additional offset current out of the CHP pin, reducing the battery charge current to under 100mA. When the MODE pin is driven high, this offset current source is disabled (for 500mA and suspend mode). For suspend mode it is the system's responsibility not to exceed 500µA or 2.5mA depending on the specific USB mode.

An important feature of this design is that it fits into the tight spaces required by handhelds. The LTC4410 is offered in the ThinSOT 6-pin package, and the LTC4053 is housed in a thermally enhanced 10-pin MSOP package. Neither part requires a reverse current blocking diode, and the system requires very few external components.

The LTC4410 USB present comparator output (USBP) drives the gate of an external P-channel MOSFET to disconnect the battery from the USB system when a valid USB voltage is present. This enables device operation when connected to the USB port regardless of the state of the battery (even a dead battery). When the USB cable is unplugged, the system reverts to operating off the battery.

Battery Charging with Priority

The LTC4410 is also useful in non-USB applications. A typical example is a wall-adapter powered cell phone charging cradle that has two slots, one for the phone and one for a spare battery. The challenge here is to charge two batteries as fast as possible, while giving charging priority to one of the batteries. When the phone and spare battery are both in the charging cradle, the battery in the phone is charged faster, utilizing all the available current from the wall adapter. As the battery in the phone approaches full charge and its current demand decreases, the spare battery starts charging.

Figure 2 shows a circuit that meets this challenge. The current for the priority charger flows through the LTC4410. A replica current equal to the (priority charger current)/1000 flows from the LTC4410 CHP pin in to the battery charger 2 PROG pin, which reduces the nonpriority charger current to zero. As BAT 1 approaches full charge, the priority charger reduces the current to the battery, which reduces the current out of the CHP pin allowing for the second battery to charge. See Figure 3 for full battery charger cycle.

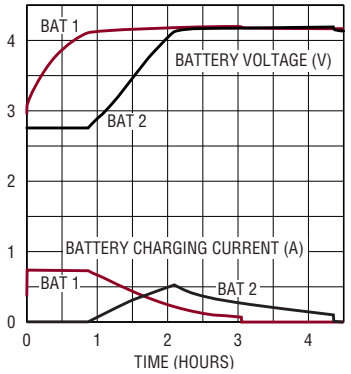


Figure 3. Battery charging cycle with the priority dual battery charger shown in Figure 2

The R_{PROG} resistor for each charger is 2kΩ, equating to 750mA of battery charge current, which is the rated current for the wall adapter. The MODE and USBP pins are not used on the LTC4410. The MODE pin is tied high, disabling its function while the USBP pin is left open. The timer capacitors on the LTC4053 are selected so that the timer for BAT 1 is 3 hours and for BAT 2 is 4.5 hours.

Conclusion

The LTC4410 and LTC4053 provide a complete and compact solution for charging batteries from a USB cable, or for charging two batteries with priority from a standard wall adapter.

Positive Buck Regulator Makes Negative Boost DC/DC Converter

by Keith Szolusha

Power supply designers can choose from a plethora of available positive buck regulators that can also be used as negative boost DC/DC converters. Some buck regulators have a negative feedback reference voltage expressly for this purpose, but they are far outnumbered by the variety of ICs that have positive reference feedback voltages. A designer can take advantage of this greater variety of devices by using a positive buck switch-mode regulator to create an excellent negative boost converter—all that is needed are a few small modifications to the typical buck converter configuration.

Figure 1a shows a –5V input to –9V output at 1.2A negative boost converter using the LT1765EFE positive buck converter switch-mode regulator. The LT1765EFE operates with a 3V to 25V input, uses a 1.2V feedback voltage, and has an internal 3A power switch. The fast 1.25MHz switching frequency of the LT1765EFE helps reduce the size of the inductor and input and output capacitors. Figure 1b shows a typical positive buck converter application for the LT1765EFE, a 12V in to 3.3V out at 2.2A DC/DC converter.

In Figure 1a the V_{IN} pin is connected to system ground and the GND pin of the IC is connected to the negative voltage output. This makes the negative boost converter configuration provide a positive voltage at the V_{FB} pin with respect to the GND pin of the IC. In this topology the maximum input voltage rating of the IC has to be greater than the magnitude of output voltage for the negative boost converter. The IC must also have a minimum input voltage rating that is less than the magnitude of the input voltage in order for the circuit to turn-on upon power-up, since the output voltage can have an initial state of 0V.

Notice that the maximum output current for the negative boost converter in Figure 1a is less than the maximum output current of the positive buck converter Figure 1b, even though they use the same 3A internal power switch.

Inductor Selection

The inductor is chosen based on maximum output current, peak switch current, and desired ripple current. First calculate the duty cycle (DC), and then either calculate the ripple current (I_{P-P}) based on the chosen inductor (L), or the inductor value based on the desired ripple current. It is generally good practice to choose the inductor value so that the peak-to-peak ripple current is about 40% of the input current. These calculations are approximate and ignore the effect of switch, inductor, and Schottky diode power losses.

continued on page 35

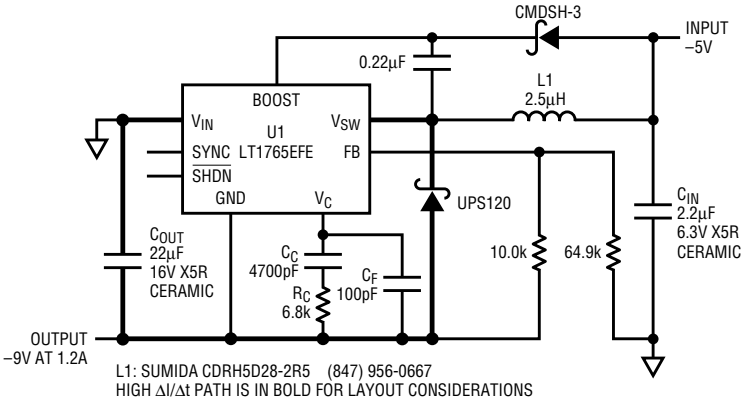


Figure 1a. –5V input to –9V output at 1.2A DC/DC converter

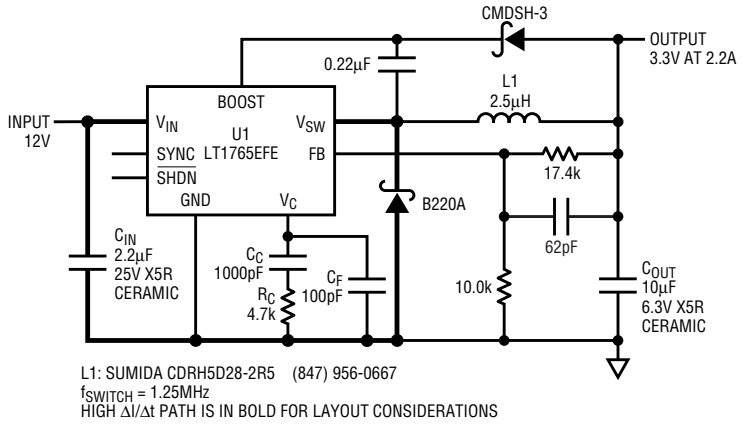


Figure 1b. 12V input to 3.3Voutput at 2.2A DC/DC converter

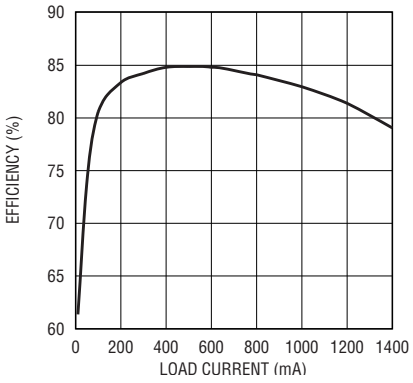


Figure 2. Efficiency of the negative boost converter in Figure 1a is as high as 85% and typically greater than 80%.

Decrease Li-Ion Battery Charge Time with a Monolithic Charger that Prevents Overheating

by Phil Juang

Introduction

The LTC4054 is a constant-current/constant-voltage linear battery charger with an internal power MOSFET in a tiny ThinSOT package. Most linear chargers risk temporary, excessive power dissipation and possible overheating, but the LTC4054 uses internal thermal feedback to regulate the charge current and limit the die temperature to 120°C. This feature allows the designer to program the LTC4054 to higher charge currents with the assurance that the LTC4054 will not overheat and damage itself or other components. This article shows how to use the LTC4054 to maximize the thermally regulated charge current to reduce battery charging times.

The LTC4054 includes other desirable features that save space and reduce circuit costs. It does not require an external sense resistor or blocking diode because of its internal MOSFET architecture. The automatic charge termination feature allows the LTC4054 to act as a standalone Li-Ion battery charger. A charge status output pin indicates the state of the battery charger. It also includes undervoltage lockout protection, low-battery charge conditioning, a charge current monitor pin, and automatic recharge. Furthermore, the LTC4054 is capable of operating from a USB power supply.

Thermal Considerations

The thermal feedback loop of the LTC4054 regulates the die temperature to approximately 120°C by automatically reducing the charge current as the IC heats up. It follows that to maintain high charge currents (and correspondingly shorter charge times), heat must be efficiently transferred away from the LTC4054. The key quantity is the thermal resistance from the die to the PC board to ambient air (see sidebar).

The thermal resistance of the LTC4054 package is dependent on board layout. Since the majority of the heat generated by the IC flows through the copper lead frame and out the package leads (especially the ground lead), the board designer can use the PCB copper as a heat sink to improve the thermal characteristics. By soldering the leads (particularly the ground lead) to wide copper pads that expand out to larger copper areas, the heat from the IC will more easily dissipate to the surrounding ambient. Feedthrough vias to inner or backside copper ground planes further improve the thermal resistance. Other sources of heat dissipation on the board should be considered during PCB layout,

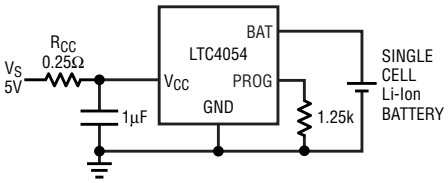


Figure 1. Standalone 800mA Li-Ion battery charger with external power dissipation

Thermal Resistance Calculation

The following example calculates the maximum thermal resistance (θ_{JA}) allowed to charge a battery at 800mA assuming typical charge conditions. The thermal resistance is defined as the steady state difference in temperature between ambient and the silicon junction given a certain amount of power dissipation in the silicon. Since the majority of the power dissipation on the die comes from the internal MOSFET, the power is calculated to be:

$$P = I_{BAT} \bullet (V_{CC} - V_{BAT})$$

where I_{BAT} is the charging current, V_{CC} is the V_{CC} pin voltage, and V_{BAT} is the BAT pin voltage. In this example, we will assume a nominal battery voltage of 3.7V, a 5V typical operating voltage, and an ambient temperature of 25°C.

The silicon junction temperature is calculated by the following formula:

$$T_J = T_A + \theta_{JA} \bullet P = T_A + \theta_{JA} \bullet I_{BAT} \bullet (V_{CC} - V_{BAT})$$

T_J is the junction temperature and T_A is the ambient temperature. The LTC4054 charges at the programmed charge current as long as the power dissipation does not generate enough heat to raise the junction temperature above its thermal regulation point of 120°C:

$$\theta_{JA} \bullet I_{BAT} \bullet (V_{CC} - V_{BAT}) \leq T_J - T_A = 95°C$$

$$\theta_{JA} \leq \frac{95°C}{I_{BAT} \bullet (V_{CC} - V_{BAT})} = \frac{95°C}{1.3V \bullet I_{BAT}}$$

Assuming typical charge conditions, charging at 800mA requires a thermal resistance of less than 91°C/W. If the thermal resistance is too great, the LTC4054 automatically reduces the charge current (I_{BAT}) to maintain a constant die temperature of 120°C.

because they can increase the ambient temperature (T_A) and reduce the maximum charge current.

800mA Charger Circuit

Another method of maximizing charge current is to dissipate some of the power in an external component, thus reducing the power dissipation on the die. Figure 1 shows how the LTC4054 can provide a complete standalone lithium-ion charger solution using few external components.

The external resistor R_{cc} is used to dissipate 160mW of the charger's total power dissipation, enabling the LTC4054 to thermally regulate at higher charge currents. Because the power is dissipated in an external component that also uses the PC board as its heat sink, the temperature of the die is reduced.

When this circuit is programmed to charge at 800mA, the voltage on the V_{CC} pin drops to 4.8V. With a nominal battery voltage of 3.7V and an ambient temperature of 25°C, the LTC4054 enters thermal regulation when (see sidebar):

$$\theta_{JA} \leq \frac{95°C}{1.1V \bullet 800mA} = 108°C/W$$

The thermal resistance of the LTC4054 can now be as high as 108°C/W before thermal regulation limits the charge current.

Dissipating power in an external component is a useful technique, especially when a high input supply voltage is used. However, the designer should avoid dropping the V_{CC} pin voltage low enough to put the LTC4054 into dropout, which could increase the time spent charging in constant-voltage mode. This occurs when the voltage across the internal MOSFET drops low enough to cause the FET to enter the linear region. The transistor does not enter the linear region as long as the following condition is met:

$$V_{CC} - V_{BAT} \geq I_{BAT} \bullet R_{DS(ON)}$$

The $R_{DS(ON)}$ of the LTC4054 FET is nominally 600mΩ. Since Li-Ion battery voltages do not typically exceed 4.2V, an LTC4054 programmed with 800mA will not enter dropout as long as the V_{CC} pin stays above 4.68V.

Conclusion

The LTC4054 standalone Li-Ion battery charger provides a simple, compact solution for charging single cell Li-Ion batteries using very few external components. Its thermal regulation feature allows the designer to eliminate the need for thermal overdesign, maximize charge current, and shorten charge times.

LT1765, continued from page 33

$$DC = \frac{(V_{OUT} - V_{IN})}{V_{OUT}}$$

$$I_{IN} \sim \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet \eta}$$

where η is the overall efficiency

$$I_{P-P} = |I_{IN}| \bullet 40\%$$

$$I_{P-P} = \frac{DC \bullet |V_{IN}|}{f \bullet L}$$

where f is the switching frequency

$$\text{or } L = \frac{DC \bullet |V_{IN}|}{f \bullet I_{P-P}}$$

Maximum inductor current ($I_{L(MAX)}$) is equal to peak switch current in this configuration. The IC has a maximum switch current ($I_{SW(MAX)}$) of 3A, so the maximum inductor current must remain below 3A. To keep switch current below the maximum, more inductance might be needed to keep the ripple current low enough.

$$I_{L(MAX)} = I_{SW(MAX)} = I_{IN} + \frac{I_{P-P}}{2}$$

Maximum output current ($I_{OUT(MAX)}$) is an approximation derived from the maximum allowable input current given the ripple current.

$$I_{OUT(MAX)} = \frac{\left(I_{SW(MAX)} - \frac{I_{P-P}}{2}\right) \bullet V_{IN} \bullet \eta}{V_{OUT}}$$

Input and Output Capacitors

Like a typical boost converter, the input capacitor in the negative boost topology has low ripple current and the output capacitor has high discontinuous ripple current. The size of the output capacitor is typically bigger than the input capacitor in order to handle the greater RMS ripple current.

$$I_{CIN(RMS)} = \frac{I_{P-P}}{\sqrt{12}}$$

$$I_{COUT(RMS)} = \sqrt{(1 - DC) \bullet \left(I_{IN}^2 + \frac{I_{P-P}^2}{12}\right)}$$

The output capacitor ESR has a direct effect on the output voltage ripple of the DC/DC converter. Choosing higher frequency switch-mode regulators reduces the need for excessive RMS ripple current rating. Regardless, a low-ESR output capacitor, such as a ceramic, can minimize the output voltage ripple of the negative boost converter.

$$\Delta V_{OUT(P-P)} = I_{SW(MAX)} \bullet ESR_{COUT}$$

Layout

Figures 1a and 1b show the high $\Delta I/\Delta t$ switching paths of the negative boost and positive buck DC/DC converters. This loop must be kept as small as possible, by minimizing trace lengths, in order to minimize trace inductance. The discontinuous currents in this path create very high $\Delta I/\Delta t$ values. Any trace inductance in this loop results in voltage spikes that can render a circuit noisy or uncontrollable. For this reason, circuit layout can be just as important as component selection. Note that the layout of the negative boost is similar to the positive buck regulator, with the locations of the input and output swapped.

New Device Cameos

Hot Swap Controller for PCI-Bus with 3.3V Auxiliary

The LTC4241 Hot Swap controller is designed for PCI-compliant motherboard applications (those with 3.3V, 5V, 12V and –12V supplies) that also have a 3.3V auxiliary supply.

When a circuit board is inserted into a live PCI slot, the supply bypass capacitors on the board can draw large and potentially damaging transient currents from the four PCI power bus as they charge. The LTC4241 ramps the PCI and auxiliary supply voltages in a controlled manner, allowing a board to be safely inserted and removed from a live PCI-bus slot without glitching the system power supplies. It features a primary controller for four PCI supplies and an independent controller for the auxiliary supply. The primary controller has programmable foldback current limiting and a programmable circuit breaker.

The primary controller controls the power supplies with two discrete N-channel pass transistors for high current 3.3V and 5V power paths and two internal pass transistors for the ±12V power paths. All supply voltages can be ramped at a programmable rate. Foldback current limiting controls current spikes and power dissipation when shorts occur. This allows boards with large capacitances to be powered up without tripping the circuit breaker. The primary controller provides fault and power-good outputs.

The auxiliary controller controls a discrete N-channel pass transistor with programmable ramp rate and current limit. The fault status is wire ORed with the primary controller. The auxiliary controller operates independently of the primary controller so that faults on one do not affect the other.

The LTC4241 is available in 20-pin narrow SSOP package in commercial and industrial temperature ranges.

High Frequency DC/DC Step-Down Controller with LDO Replaces Two ICs

The LTC1704B dual output DC/DC converter combines an integrated step-down synchronous controller and a linear regulator controller in a 16-lead SSOP package. This device is equivalent to the LTC1704, except that it does not shift into Burst Mode® operation at light loads. This eliminates low frequency output ripple at the expense of light load efficiency.

The IC operates from a low input supply ranging from 3.15V to 5.5V. The ability to operate from 3.3V reduces the cost of a system's power supplies by eliminating the need for a 5V auxiliary supply and associated components such as filters, inductors and capacitors. An integrated linear regulator controller provides the second output that drives an external NPN transistor delivering up to 2.5A of load current. The LTC1704B's constant frequency operation and linear regulator provide a low noise dual power supply, which is especially valuable in noise-sensitive telecom, test equipment and imaging systems.

The LTC1704B drives a pair of N-channel MOSFETs in a voltage mode, synchronous buck configuration to provide the main supply. The constant frequency, true PWM architecture switches at 550kHz, which minimizes external component size, lowers cost and optimizes load transient performance. The linear regulator controller is designed to drive an inexpensive external NPN power transistor to deliver current to an auxiliary load. The LTC1704B provides better than 1.5% DC accuracy at its switcher output and 2% at its linear regulator output.

The LTC1704B operates from –40°C to 85°C and is available in a 16-lead SSOP package.

Next Generation Smart Battery Charger Packs More Features into Smaller Package and Uses Fewer Components

The LTC4100 is a new level 2 Smart Battery charger that complies with version 1.1 of the SMBus standard. The 24-pin narrow (209mil) SSOP package and new PWM architecture make it relatively easy to build a highly reliable, high efficiency universal Smart Battery charger in a small space. The charger supports batteries up to 28V and 4A using a 300kHz quasi-constant-frequency PWM with a P-channel top-side switch. The switcher is a current mode synchronous buck, offering efficiency greater than 95%, and is designed to suppress audible noise when using ceramic input/output capacitors. Charging voltage and current accuracy is 1% and 5%, respectively. When supplying load current to a system, charging current is automatically reduced to prevent overloading an input power adaptor.

An 11-bit voltage DAC and 10-bit current DAC provide 16mV voltage granularity and 4mA, 2mA or 1mA current granularity, depending upon the current range selected. User-selectable overvoltage and overcurrent limits offer an additional layer of protection against software mischief. The overvoltage limits of 28.006V, 21.712V, 17.408V, 13.104V and 8.800V allow for pulse-top-off charge techniques for Li-Ion cells while still protecting the battery pack. Overcurrent limits are 1023mA, 2046mA, 3068mA and 4092mA with associated resolutions of 1mA, 2mA, 4mA and 4mA. The overcurrent and overvoltage limit settings

For further information on any of the devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number:

1-800-4-LINEAR

Ask for the pertinent data sheets and Application Notes.

are programmed independently, each by a resistor.

Safety Signal sensing complies with the 5% accuracies required by the version 2.0 Smart Battery Charger specification and offers high immunity from noise and ground offsets. The LTC4100 also includes SMBus accelerators to improve bus rise/fall timing in larger systems or systems with mixed I^2C and SMBus components. The accelerators are compatible with version 1.1 of the SMBus specification. In stand-alone applications, the LTC4100 provides outputs to drive LEDs for Charging and AC Present indicators. In host-driven systems the $\overline{\text{SMBALERT}}$ signal is available and the Alert Response Address protocol is fully supported to eliminate the need for interrupt polling.

Single-Phase and 2-Phase IMVP4 Solutions Power the Intel Mobile Banias Processor Family

The LTC3734 and LTC3735 are single-phase and 2-phase current mode synchronous step-down controllers designed to supply the core voltage for Intel's upcoming Banias and Dothan mobile processors (including the Low Voltage and Ultra-Low Voltage versions). Both devices use a 6-bit VID code to program the output voltage with ±1% accuracy. This programmability allows the core voltage to be dynamically changed depending on the load demand on the processor. Applications such as DVD decoding or virus scanning, for example, require the highest performance possible. In these cases, the core voltage and system clock will run at their maximum levels. Word processing or other productivity applications, however, do not require high performance, so the core voltage and system clock frequency can be scaled back to maximize battery life.

The LTC3735 offers 2-phase operation from 210kHz to 550kHz to reduce the RMS current in the input and output capacitors, reduce output ripple, and improve transient response. It also provides active voltage positioning to reduce the number of output capacitors required to meet a given dynamic output voltage tolerance. The LTC3734 offers single-phase operation for lower current versions in the Banias processor family. Both devices include strong MOSFET gate drivers.

Several pins are dedicated to providing the user with core voltage programmability during system boot-up and during low current operation. Power savings are further improved using a mode control input, which programs either continuous conduction mode (CCM) or discontinuous conduction mode (DCM).

Both devices include an open-drain PGOOD output, along with a 110µs filter for noise-free operation. The PGOOD output responds to FB voltage changes of greater than ±10%. Protection features include programmable soft start, foldback current limiting, and a short circuit shutdown timer. Finally, a low minimum on-time of 120ns allows 20V-to-0.7V step-down ratios while maintaining constant frequency operation.

The 2-phase LTC3735 is ideal for high current applications, up to 40A, whereas the LTC3735 is a better fit for lower current processors (up to 20A). The LTC3735 is available in a narrow G36 SSOP package, and the LTC3734 is available in a convenient 5mm × 5mm QFN package.

A 14-Bit, 6Msps ADC with Low Noise and Good Linearity

The LTC1740 is 14-bit ADC that has excellent dynamics and linearity at sampling rates up to 6Msps, making it ideal for communications and high-speed data acquisition. A new track and hold circuit gives the LTC1740 good AC performance with either single or dual supplies. For a 2.5MHz input signal, the S/(N + D) is 79dB and the spurious free dynamic range (SFDR) is 92dB. The linearity is also very clean, with a typical DNL of 0.5LSB and INL of under 1LSB. The part is guaranteed to have no missing codes over temperature and a maximum INL of 2LSB.

The LTC1740 operates from either a 5V or ±5V supplies, making it easy to interface to single or dual supply systems. The output of a dual supply op amp can be fed directly to the analog input, eliminating the need for a level shifter.

A programmable on-chip reference gives the user a wide selection of input ranges: $5V_{P-P}$ or $2.5V_{P-P}$ by tying a pin high or low, or any range between $2.5V_{P-P}$ and $5V_{P-P}$ by using two external resistors. A separate power supply for the digital output drivers allows direct interfacing to 3V–5V systems.

The LTC1740 is available in a 36-lead SSOP package in both commercial and industrial temperature grades.

2-Channel Differential Input 24-Bit No Latency ΔΣ ADC Provides a Simple and Accurate Solution for Data Acquisition

The LTC2412 combines a 2-channel differential input with the simplicity and high accuracy of the LTC 24-bit No Latency ΔΣ™ ADC family. It provides 2ppm INL and 0.16ppm RMS noise over the entire supply range of 2.7V to 5.5V. The common mode voltage of the reference and the input channels is rail to rail. The internal digital filter settles in a single cycle. This feature is important for multiplexing applications since it guarantees an accurate conversion immediately following a change in input.

The interface of the LTC2412 is simple. The two differential channels are converted alternately and the channel ID is included in the conversion results. The LTC2412 communicates through a 3-wire digital interface that is compatible with SPI and MICROWIRE protocols. The internal oscillator eliminates the need for external frequency setting components, and through a single pin, the LTC2412 can be configured for better than 110dB differential mode rejection at 50Hz or 60Hz ±2%.

The LTC2412 is available in a 16-lead SSOP package. The LTC2412 operates from a single 2.7V to 5.5V power supply and consumes only 200µA.

3V, Low Power, 16-Bit, 150ksps, 1- and 2-Channel ADCs in MSOP

The LTC1864L and LTC1865L are low power, 16-bit, 150ksps, A/D converters that are offered in MSOP and SO-8 packages. They operate on a single 3V supply.

These low-power ADCs are a good fit in battery operated applications. At the maximum sampling frequency of 150ksps, supply current is only 450µA. LTC1864L and LTC1865L automatically power down between conversions, allowing the supply current to drop to only 10µA at a sampling rate of 1ksps.

These differential input, switched capacitor, successive approximation ADCs include sample-and-holds on both inputs to reduce common mode noise. The LTC1864L has a fixed differential analog input with an adjustable reference pin. The LTC1865L provides a software-selectable 2-channel MUX and an adjustable reference pin on the MSOP version. Pin compatible 12-bit parts are also available in the LTC1860L and LTC1861L.

The LTC1864L and LTC1865L perform a conversion in 4.7µs using the ADC's internal clock. The data can then be transferred using the 3-wire serial interface at a data rate from DC to 8MHz. An additional I/O line on the LTC1865L (SDI) allows the ADC to be configured as a single differential channel or two single-ended channels. The low pin count of the serial interface makes it simple to use these parts in remote and isolated applications.

These ADCs can be used in ratiometric applications or with an external reference. The high impedance analog inputs and the ability to operate with reduced spans as low as 1V full scale, allow direct connection to signal sources in many applications, eliminating the need for a gain stage. LT

LTC4251, continued from page 30

initial start-up delay allows time for the board supply voltage to stabilize at plug-in, before activating the MOSFET. The circuit breaker response is set within the safe operating area (SOA) of the MOSFET at worst-case operating voltage and analog limit current. The shutdown cooling period is approximately 5.25 times the initial timing duration.

For the LTC4252-2 in continuous auto-retry, the MOSFET operating temperature will rise above ambient temperature, and the time to SOA limit must be adjusted accordingly. For both the LTC4252 and LTC4253, a resistor, R_D, can be connected between DRAIN pin and the drain of the MOSFET to reduce the current limit period when a high V_{DS} condition is present. The current flowing into the DRAIN pin effectively senses the MOSFET drain source voltage. This DRAIN pin current is amplified eight times and added to the circuit breaker timer pull-up current, accelerating the response. If the worst case is used to determine SOA limit with drain-accelerated current, the timer response at mild overload without drain-accelerated current is now longer and less sensitive. For the LTC4251, there is no DRAIN input pin, the worst case operating voltage is used to set the circuit breaker response.

Power Good and Sequencer

LTC4252 has an open-collector Power Good status pin that can drive an opto-coupler or an NPN to enable the power module. This pin is pulled low after the MOSFET is driven to full enhancement, indicating a successful power-up. The opto-coupler interface takes care of the common-mode voltage difference between the Hot Swap controller and the power module. Figure 6 shows an NPN configuration for $\overline{\text{PWRGD}}$ interface.

The LTC4253 has three sequenced $\overline{\text{PWRGD}}$ outputs and two enable (EN) inputs allowing three modules be sequenced as shown in Figure 7. The LTC4253 allows up to three power modules be turn on sequentially, minimizing the power demand on the –48V bus. When the first module turns on, it signals via the EN input to enable the second module. The minimum sequence interval between each module is set by a capacitor at SQTIMER pin.

Power Limited Circuit Breaker

In applications where timed power limit is preferred over current limit, Figure 8 shows how to create a power limited circuit breaker by tying the current limit to the supply voltage via Zener diode D1, and resistors R4 and R6. Limiting by power permits the control of equipment heat dissipation or power allocation.

Conclusion

This new family of devices offers comprehensive solutions to –48V Hot Swap applications. Higher voltage applications are also supported to the limits of the MOSFET. These devices are rugged and capable of handling large transients from catastrophic failures as well as neighboring board failures that cause large return currents. The LTC4251 is available in SOT-23 with two different UV and OV threshold combinations and one version without an OV threshold. The LTC4252 is available in 8-pin and 10-pin MS packages with latch-off mode and auto-retry. The LTC4253 is available in a 16-pin SSOP package, and also features a latchoff version. LT

DESIGN TOOLS

Databooks and Applications Handbooks

1990 Linear Databook, Vol I—This 1440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices. $10.00

1992 Linear Databook, Vol II—This 1248 page supplement to the 1990 Linear Databook includes all products introduced in 1991 and 1992. $10.00

1994 Linear Databook, Vol III—This 1826 page supplement to the 1990 and 1992 Linear Databooks includes all products introduced since 1992. $10.00

1995 Linear Databook, Vol IV—This 1152 page supplement to the 1990, 1992 and 1994 Linear Databooks includes all products introduced since 1994. $10.00

1996 Linear Databook, Vol V—This 1152 page supplement to the 1990, 1992, 1994 and 1995 Linear Databooks includes all products introduced since 1995. $10.00

1997 Linear Databook, Vol VI—This 1360 page supplement to the 1990, 1992, 1994, 1995 and 1996 Linear Databooks includes all products introduced since 1996. $10.00

1999 Linear Databook, Vol VII—This 1968 page supplement to the 1990, 1992, 1994, 1995, 1996 and 1997 Linear Databooks includes all products introduced since 1997. $10.00

1990 Linear Applications Handbook, Volume I—928 pages full of application ideas covered in depth by 40 Application Notes and 33 Design Notes. This catalog covers a broad range of "real world" linear circuitry. In addition to detailed, systems-oriented circuits, this handbook contains broad tutorial content together with liberal use of schematics and scope photography. A special feature in this edition includes a 22-page section on SPICE macromodels. $20.00

1993 Linear Applications Handbook, Volume II—Continues the stream of "real world" linear circuitry initiated by the 1990 Handbook. Similar in scope to the 1990 edition, the new book covers Application Notes 40 through 54 and Design Notes 33 through 69. References and articles from non-LTC publications that we have found useful are also included. $20.00

1997 Linear Applications Handbook, Volume III—This 976 page handbook includes Application Notes 55 through 69 and Design Notes 70 through 144. Subjects include switching regulators, measurement and control circuits, filters, video designs, interface, data converters, power products, battery chargers and CCFL inverters. An extensive subject index references circuits in LTC data sheets, design notes, application notes and *Linear Technology* magazines. $20.00

PSPICE is a trademark of MicroSim Corp.

Brochures and Software

Power Management Solutions Brochure—This 96 page collection of circuits contains real-life solutions for common power supply design problems. There are over 70 circuits, including descriptions, graphs and performance specifications. Topics covered include battery chargers, desktop PC power supplies, notebook PC power supplies, portable electronics power supplies, distributed power supplies, telecommunications and isolated power supplies, off-line power supplies and power management circuits. Selection guides are provided for each section and a variety of helpful design tools are also listed for quick reference. Available at no charge

Data Conversion Solutions Brochure—This 88 page collection of data conversion circuits, products and selection guides serves as excellent reference for the data acquisition system designer. Over 40 products are showcased, solving problems in low power, small size and high performance data conversion applications—with performance graphs and specifications. Topics covered include delta-sigma ADCs, low power and high speed ADCs and low power and high speed DACs. A complete glossary defines data conversion specifications; a list of selected application and design notes is also included. Available at no charge

Telecommunications Solutions Brochure—This 76 page collection of application circuits and selection guides covers a wide variety of products targeted for telecommunications. Circuits solve real life problems for central office switching, cellular phones, high speed modems, basestation, plus special sections covering –48V and Hot Swap™ applications. Many applications highlight new products such as Hot Swap controllers, power products, high speed amplifiers, A/D converters, interface transceivers and filters. Includes a telecommunications glossary, serial interface standards, protocol information and a complete list of key application notes and design notes. Available at no charge

SwitcherCAD™ III—LTC SwitcherCAD III is a fully functional SPICE simulator with enhancements and models to ease the simulation of switching regulators. This SPICE is a high performance circuit simulator and integrated waveform viewer, and also includes schematic capture. Our enhancements to SPICE result in much faster simulation of switching regulators than is possible with normal SPICE simulators. SwitcherCAD III includes SPICE, macromodels for 80% of LTC's switching regulators and over 200 op amp models. It also includes models of resistors, transistors and MOSFETs. With this SPICE simulator, most switching regulator waveforms can be viewed in a few minutes on a high performance PC. Circuits using op amps and transistors can also be easily simulated. Download at www.linear.com

FilterCAD™ 3.0—FilterCAD 3.0 is a computer aided design program for creating filters with Linear Technology's filter ICs. FilterCAD is designed to help users without special expertise in filter design to design good filters with a minimum of effort. It can also help experienced filter designers achieve better results by playing "what if" with the configuration and values of various components and observing the results. With FCAD, you can design lowpass, highpass, bandpass or notch filters with a variety of responses, including Butterworth, Bessel, Chebychev, elliptic and minimum Q elliptic, plus custom responses. Download at www.linear.com

SPICE Macromodel Disk—This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models and a demonstration copy of PSPICE™ by MicroSim. Available at no charge

Noise Disk—This IBM-PC (or compatible) program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise and calculate noise using specs for any op amp. Available at no charge

www.linear.com and the Linear Online Store

LTC Web Site—Customers can quickly and conveniently find and retrieve the latest technical information covering the company's products on LTC's web site. Located at www.linear.com, the site allows searching of data sheets, application notes, design notes, *Linear Technology* magazine issues and other LTC publications. The LTC web site simplifies searches by providing three separate search engines. The first is a quick search function that provides a complete list of all documentation for a particular word or part number. There is also a product function tree that lists all products in a given product family. The most powerful, though, is the parametric search engine. It allows engineers to specify key parameters and specifications that satisfy their design requirements. Other areas within the site include a sales office directory, press releases, financial information, quality assurance documentation, and general corporate information.

Linear Direct Online Store—The Linear Online Store at www.linear.com now offers a simple way to order LTC products factory direct. The new store accepts major credit cards and allows customers to create personalized accounts where they can check order history, shipment information and reorder products. Also, the maximum quantity per order has increased to 500.

World Headquarters Linear Technology Corporation

1630 McCarthy Blvd.
Milpitas, CA 95035-7417
Phone: (408) 432-1900
FAX: (408) 434-0507
www.linear.com

LTC U.S. Area Sales Offices

NORTHWEST AREA

Bay Area
720 Sycamore Dr.
Milpitas, CA 95035
Phone: (408) 428-2050
FAX: (408) 432-6331

Portland
6700 SW 105th Ave., Ste. 207
Beaverton, OR 97008
Phone: (503) 520-9930
FAX: (503) 520-9929

Sacramento
Phone: (408) 432-6326

Seattle
Phone: (425) 748-5010

Salt Lake City
Phone: (801) 731-8008

Denver
Phone: (303) 926-0002

SOUTHWEST AREA

Orange County
15375 Barranca Pkwy., Ste. A-213
Irvine, CA 92618
Phone: (949) 453-4650
FAX: (949) 453-4765

Los Angeles
21243 Ventura Blvd., Ste. 208
Woodland Hills, CA 91364
Phone: (818) 703-0835
FAX: (818) 703-0517

San Diego
Phone: (858) 638-7131

CENTRAL AREA

Chicago
2040 E. Algonquin Rd., Ste. 512
Schaumburg, IL 60173
Phone: (847) 925-0860
FAX: (847) 925-0878

Cleveland
7550 Lucerne Dr., Ste. 106
Middleburg Heights, OH 44130
Phone: (440) 239-0817
FAX: (440) 239-1466

Columbus
Phone: (614) 488-4466

Minneapolis
Phone: (952) 903-0605

Wisconsin
Phone: (262) 859-1900

Detroit
Phone: (248) 374-2243

Indiana
Phone: (317) 581-9055

Kansas
Phone: (913) 829-8844

NORTHEAST AREA

Boston
15 Research Place
North Chelmsford, MA 01863
Phone: (978) 656-4750
FAX: (978) 656-4760

Philadelphia
3220 Tillman Dr., Ste. 120
Bensalem, PA 19020
Phone: (215) 638-9667
FAX: (215) 638-9764

Connecticut
Phone: (203) 680-6283

Maryland/Virginia
Phone: (410) 884-4036

SOUTHEAST AREA

Dallas
17000 Dallas Pkwy., Ste. 200
Dallas, TX 75248
Phone: (972) 733-3071
FAX: (972) 380-5138

Raleigh
15100 Weston Pkwy., Ste. 202
Cary, NC 27513
Phone: (919) 677-0066
FAX: (919) 678-0041

Austin
Phone: (512) 795-8000

Houston
Phone: (713) 463-5001

Huntsville
Phone: (256) 885-0215

Atlanta
Phone: (770) 888-8137

Tampa
Phone: (813) 634-9434

Orlando
Phone: (407) 688-7616

Fort Lauderdale
Phone: (954) 986-9810

LTC International Sales Offices

CHINA

Linear Technology Corp. Ltd.
Unit 2108, Metroplaza Tower 2
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Phone: +852 2428-0303
FAX: +852 2348-0885

Linear Technology Corp. Ltd.
Room 1610, Central Plaza
No. 227 Huangpi Bei Lu
Shanghai, 200003, PRC
Phone: +86 (21) 6375-9478
FAX: +86 (21) 6375-9479

Linear Technology Corp. Ltd.
Room 707, 7th Floor
Beijing Canway Building
66 Nan Li Shi Lu
Beijing, 100045, PRC
Phone: +86 (10) 6801-1080
FAX: +86 (10) 6805-4030

FRANCE

Linear Technology S.A.R.L.
Immeuble "Le Quartz"
58, Chemin de la Justice
92290 Chatenay Malabry
France
Phone: +33 (1) 41 07 95 55
FAX: +33 (1) 46 31 46 13

Linear Technology
"Le Charlemagne"
140, cours Charlemagne
69286 Lyon Cedex 2
France
Phone: +33 (4) 72 41 63 86
FAX: +33 (4) 72 41 62 99

GERMANY

Linear Technology GmbH
Oskar-Messter-Str. 24
D-85737 Ismaning
Germany
Phone: +49 (89) 962455-0
FAX: +49 (89) 963147

Haselburger Damm 4
D-59387 Ascheberg
Germany
Phone: +49 (2593) 9516-0
FAX: +49 (2593) 951679

Zettachring 12
D-70567 Stuttgart
Germany
Phone: +49 (711) 1329890
FAX: +49 (711) 7285055

JAPAN

Linear Technology KK
8F Shuwa Kioicho Park Bldg.
3-6 Kioicho Chiyoda-ku
Tokyo, 102-0094, Japan
Phone: +81 (3) 5226-7291
FAX: +81 (3) 5226-0268

6F Kearny Place Honmachi Bldg.
1-6-13 Awaza, Nishi-ku
Osaka-shi, 550-0011, Japan
Phone: +81 (6) 6533-5880
FAX: +81 (6) 6543-2588

KOREA

Linear Technology Korea Co., Ltd.
Yundang Building, #1002
Samsung-Dong 144-23
Kangnam-Ku, Seoul 135-090
Korea
Phone: +82 (2) 792-1617
FAX: +82 (2) 792-1619

SINGAPORE

Linear Technology Pte. Ltd.
507 Yishun Industrial Park A
Singapore 768734
Phone: +65 6753-2692
FAX: +65 6752-0108

SWEDEN

Linear Technology AB
Sollentunavägen 63
S-191 40 Sollentuna
Sweden
Phone: +46 (8) 623-1600
FAX: +46 (8) 623-1650

TAIWAN

Linear Technology Corporation
Rm. 602, No. 46, Sec. 2
Chung Shan N. Rd.
Taipei, Taiwan
Phone: +886 (2) 2521-7575
FAX: +886 (2) 2562-2285

UNITED KINGDOM

Linear Technology (UK) Ltd.
The Coliseum, Riverside Way
Camberley, Surrey GU15 3YL
United Kingdom
Phone: +44 (1276) 677676
FAX: +44 (1276) 64851