

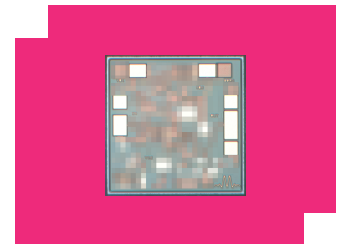
ADM-8095CH

0.09 - 10 GHz High Dynamic Range Gain Block

DEVICE OVERVIEW

General Description

The ADM-8095CH is a high-linearity amplifier capable of providing +20 dBm output power up to 10 GHz. The ADM-8095CH can serve either as a linear signal amplifier, or as a saturated driver amplifier for H- or S-diode mixers. The amplifier has excellent return losses and gain flatness.



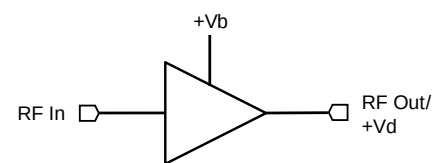
Features

- +21 dBm output power
- +18 dB gain
- 1.2 dB noise figure
- Gain flatness
- Excellent Return Losses
- Single-supply, positive only bias

Applications

- Mobile test and measurement equipment
- Driver Amplifier for H and S - Diode Mixers
- Radar
- SATCOM

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
ADM-8095CH	0.09 - 10 GHz High Dynamic Range Gain Block	CH	REACH RoHS	Released	EAR99

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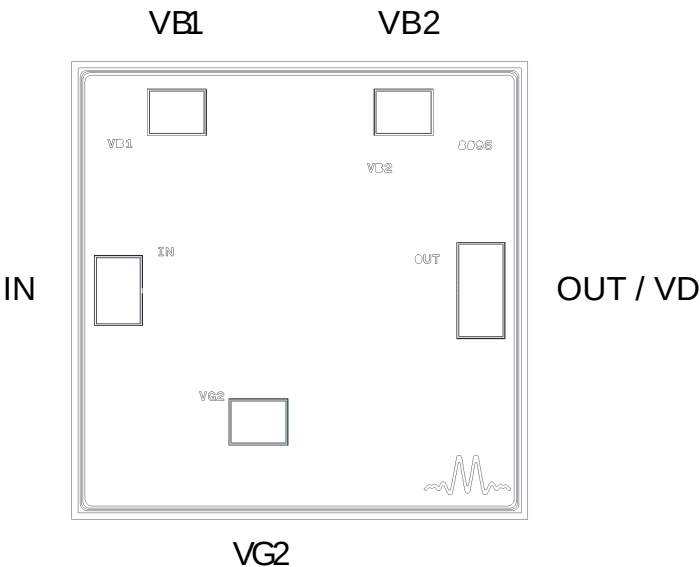
Revision History

Revision Code	Revision Date	Comment
-	2023-12-13	Initial Datasheet Release

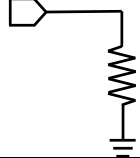
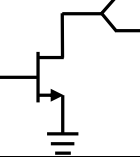
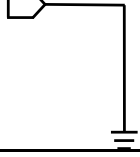
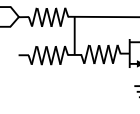
Port Configuration and Functions

Port Diagram

A port diagram of the ADM-8095CH is shown below.



Port Functions

Port	Function	Description	Equivalent Circuit for Package
IN	RF Input	The amplifier's RF Input pad, this pad requires an external blocking capacitor and external stability network as shown in the application schematic.	
OUT / VD	Drain Supply / RF Output	This pad is the RF Output port and is also the Vd port providing the main power supply to the amplifier. This pad is DC coupled and requires an external bias-T or discrete choke and DC blocking capacitor. This port is RF matched to 50 Ω. DC voltage at this pin should be set to 5V for normal operation.	
Paddle	Ground	GND is provided through the backside of the die.	
VB1	Non-connect (NC)	This pad should not be connected.	-
VB2	Positive bias	This pad provides DC bias to the amplifier. Placement of an external series bias resistor allows this pad to be supplied by the same supply line providing 5V to the RF Out/Vd pad. For normal operation at 5V Vd, the recommended series bias resistor value is 3.3kΩ. Device drain current will change proportional to the current flowing into this pin. RF performance can be balanced with DC power consumption by adjusting this current.	
VG2	Non-connect (NC)	This pad should not be connected.	-

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may become inoperable or have a reduced lifetime. Reliability limits are individual, instantaneous catastrophic limits only. Functional operation limits are indicated below. Operation of the device at multiple absolute maximum limits or for extended periods at a single limit can cause degradation and damage to the device.

Parameter	Maximum Rating	Unit
Bias Voltage (Vb)	4	V
Drain Current (RF Applied)	90	mA
Drain Supply Voltage (Vd)	8	V
Maximum Operating Temperature for MTTF > 1E6 hours	85	°C
Maximum Storage Temperature	125	°C
Max Junction Temperature for MTTF of 1E6 hours	175	°C
Max Power Dissipation for MTTF of 1E6 hours	0.26	W
Minimum Operating Temperature for MTTF > 1E6 hours	-40	°C
Minimum Storage Temperature	-65	°C
RF Input Power	15	dBm

Package Information

Parameter	Details	Rating
Dimensions	-	1.05 x 1.05 mm

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications. Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the Electrical Specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

Parameter	Min	Nominal	Max	Unit
Power Supply DC Voltage (Vd)	3	5	6	V
Power Supply DC Current (Id) (No RF Input) ¹	21	39	47	mA
Input Power for Saturation	2	4	6	dBm
Ambient Temperature	-40	25	85	°C

^[1] Recommended operating current conditions without RF input applied.

Sequencing Requirements

There is no sequencing required to power up or power down the amplifier. An output load is recommended to be connected to the amplifier during operation.

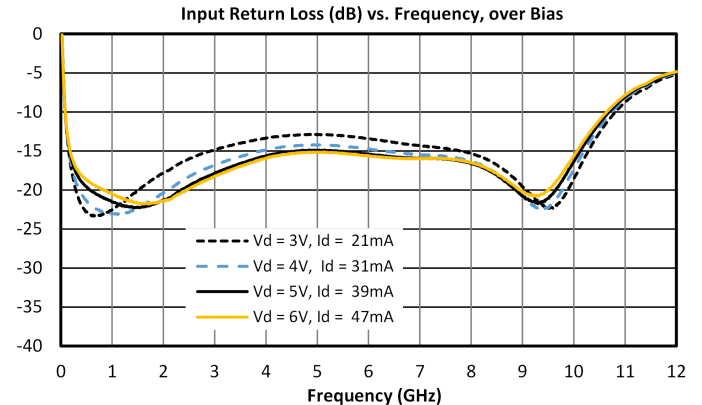
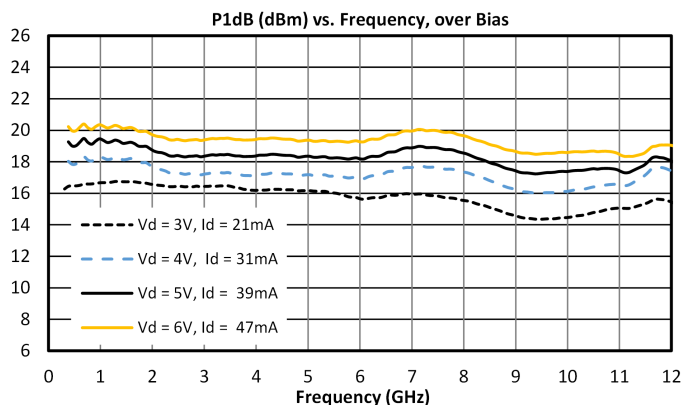
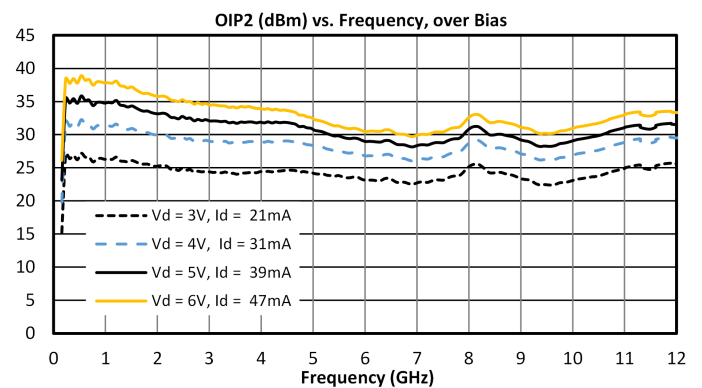
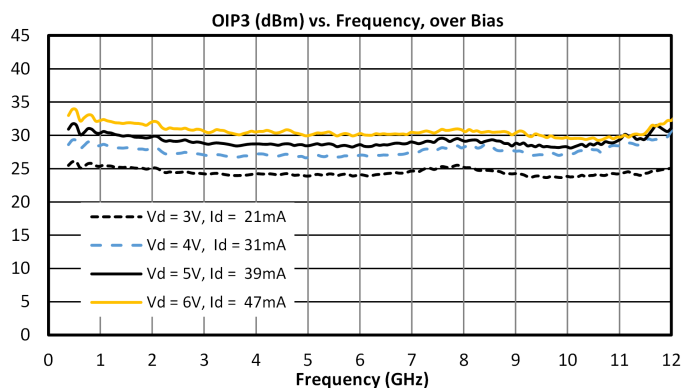
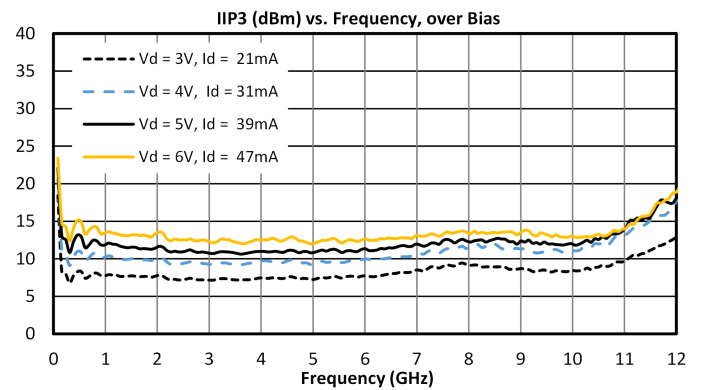
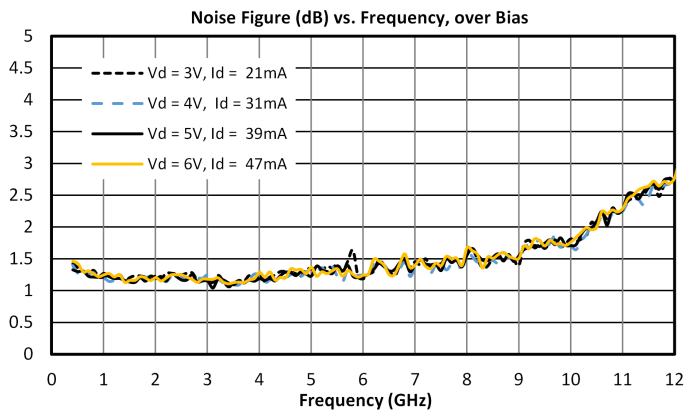
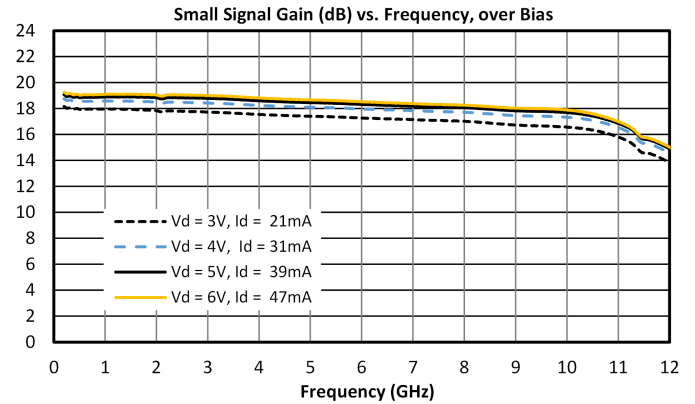
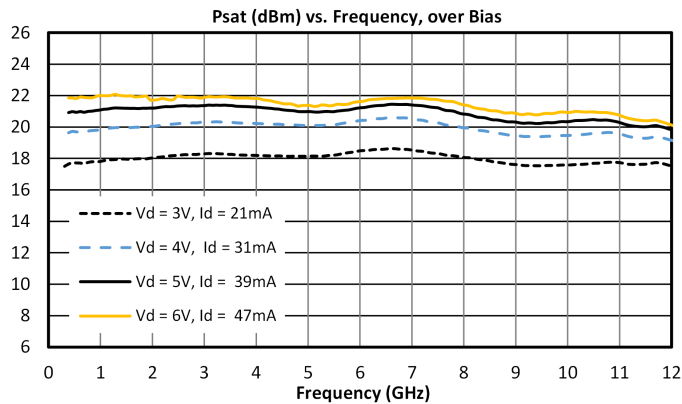
Electrical Specifications

Unless otherwise specified, electrical specifications apply at TA=+25°C, Rb=3.3k, Vd = 5V, and Vb = 5 V.

Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Small Signal Gain	Vd,Vb = 5 V, Pin = -20 dBm	0.09	10	-	18	-	dB
Noise Figure	Vd,Vb = 5 V, Pin = -20 dBm	0.2	5	-	1.2	-	dB
Noise Figure	Vd,Vb = 5 V, Pin = -20 dBm	5	10	-	1.5	-	dB
Saturated Output Power	Vd,Vb = 5 V	0.09	10	-	21	-	dBm
Output IP3	Vd,Vb = 5 V, Pin = -15 dBm per tone, 10 MHz tone spacing	0.09	10	-	30	-	dBm
Input IP3	Vd,Vb = 5 V, Pin = -15 dBm per tone, 10 MHz tone spacing	0.09	10	-	14	-	dBm
Output IP2	Vd,Vb = 5V, Pin = -15dBm per tone, 10 MHz tone spacing	0.09	6	-	33	-	dBm
Output IP2	Vd, Vb = 5V, Pin = -15 dBm per tone, 10 MHz tone spacing	6	10	-	30	-	dBm
Output P1dB	Vd,Vb = 5V	0.09	10	-	18	-	dBm
Input Return Loss	Vd,Vb = 5 V, Pin = -20 dBm	0.09	10	-	17	-	dB
Output Return Loss	Vd,Vb = 5 V, Pin = -20 dBm	0.09	10	-	21	-	dB
Reverse Isolation	Vd,Vb = 5 V, Pin = -20 dBm	0.09	10	-	23	-	dB
Input Power for Saturation	Vd,Vb = 5V	0.09	10	-	4	-	dBm
DC Supply Quiescent Current (Idq)	Vd,Vb = 5 V, no RF input	-	-	-	39	-	mA

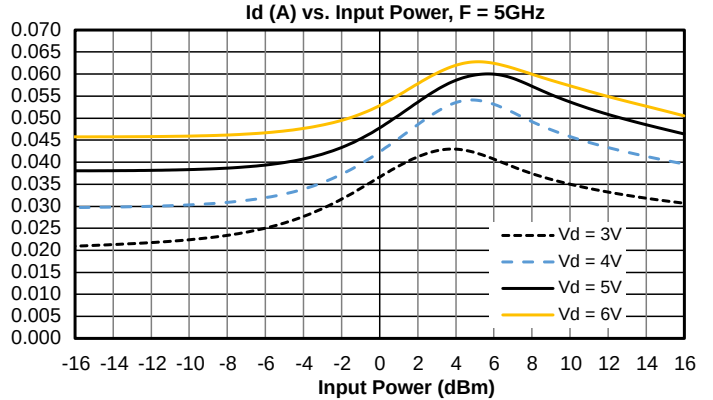
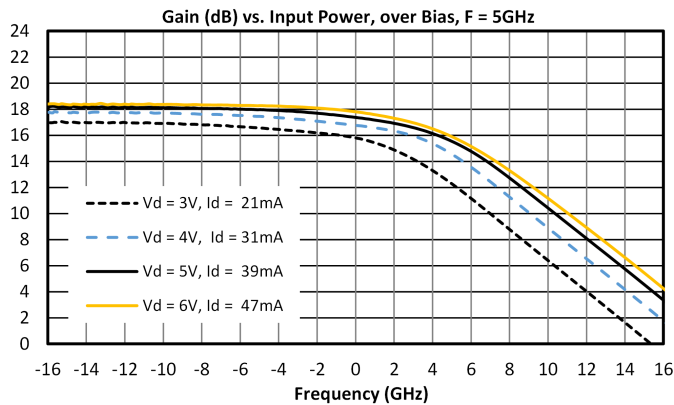
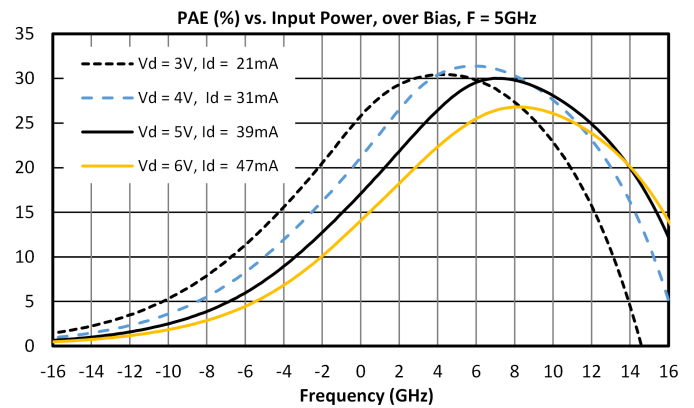
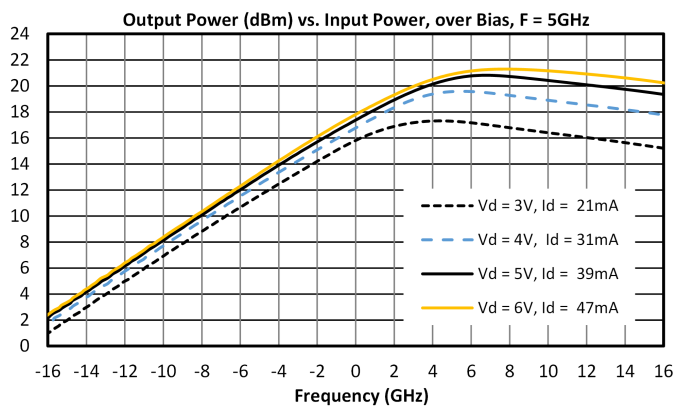
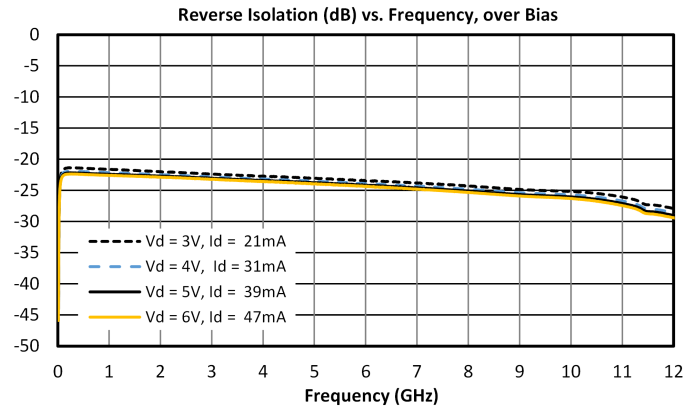
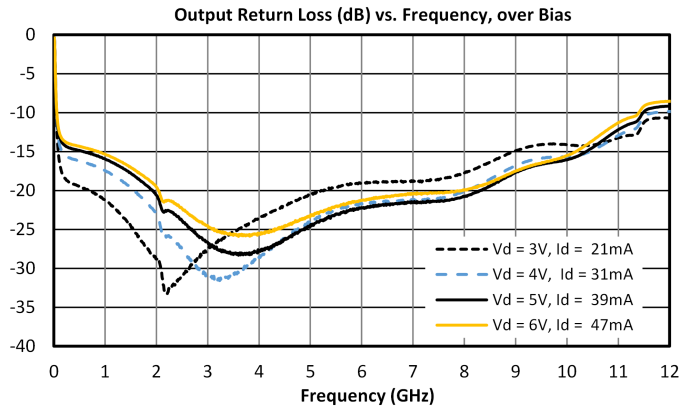
Performance plots measured with Vb resistor of 3.3k Ohms. Psat, Small Signal Gain and Noise Figure plots have fixture losses de-embedded.

ADM-8095CH Typical Performance Plots



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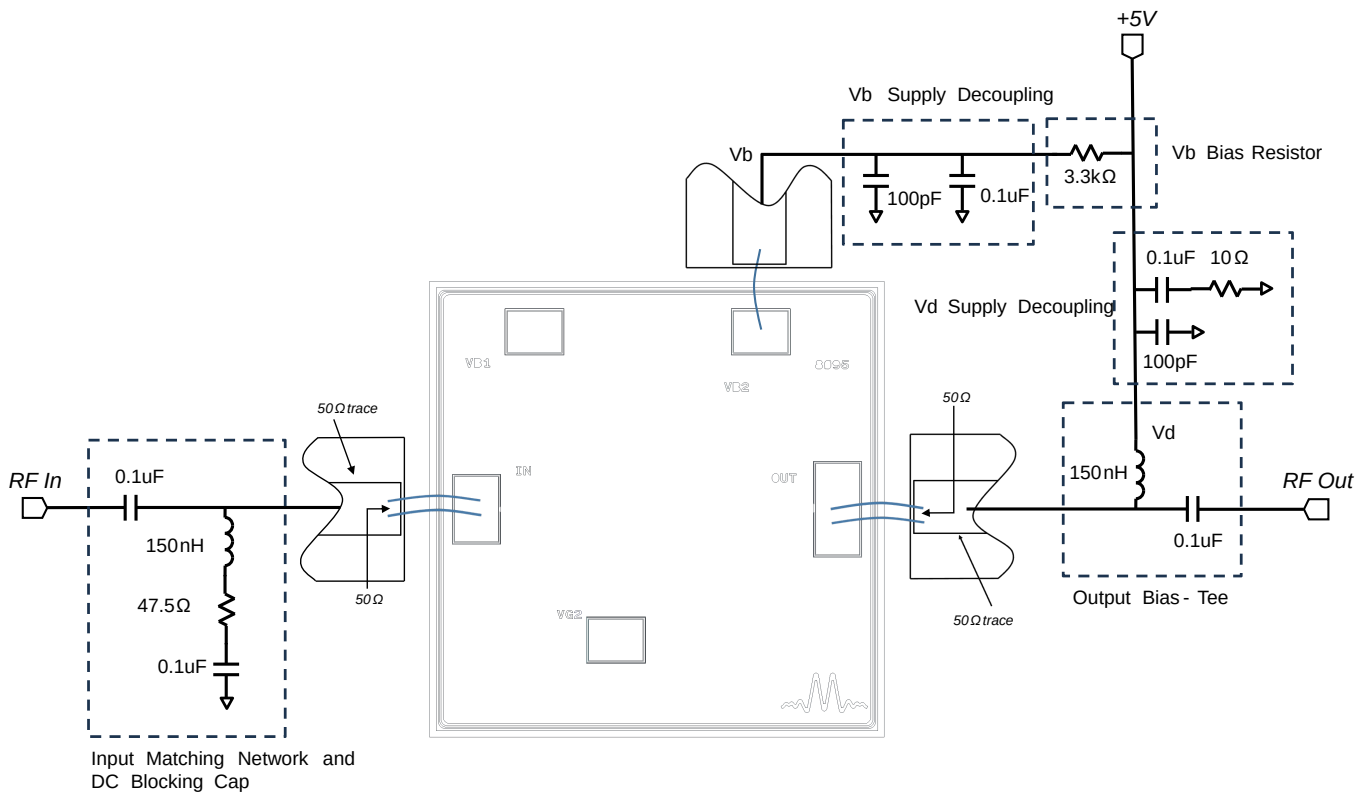
Application Information

Below is the recommended application circuit for the ADM-8095CH. DC power is supplied to RF Out/Vd pad via a 150 nH choke inductor. Supply bypassing is provided by 100pf and 0.1uF capacitors. Drain current Id is controlled by applying voltage to the VB2 pad. Drain current Id is adjusted proportionally to the current flowing into VB2 pad with higher Vb and Ib resulting in increased current Id. Amplifier performance can therefore be optimized for specific applications by adjusting the value of the series resistor on the Vb line. In particular, OIP3 across the band and especially at low voltage Vd can be improved from that shown in Typical Performance Plots by increasing current into VB2 pad. The OIP3 can be improved by up to 4dB with the tradeoff being increased quiescent DC power consumption (See ADM1-8095PC datasheet). The default value for the Vb resistor is 3.3k Ohms. For higher OIP3, it should be reduced to 453 Ohms. The ADM-8095CH requires an RF input matching network at RF IN pad as shown. DC blocking capacitors are also required at RF input and output pads as shown.

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Application Circuit



Die Mounting Recommendations

Mounting and Bonding Recommendations

Marki MMICs should be attached directly to a ground plane with conductive epoxy. The ground plane electrical impedance should be as low as practically possible. This will prevent resonances and permit the best possible electrical performance. Datasheet performance is only guaranteed in an environment with a low electrical impedance ground.

Mounting - To epoxy the chip, apply a minimum amount of conductive epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip. Cure epoxy according to manufacturer instructions.

Wire Bonding - Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. Bond wire inductance will improve return loss. Bondwire inductance in the range of 30pH to 200pH will improve performance.

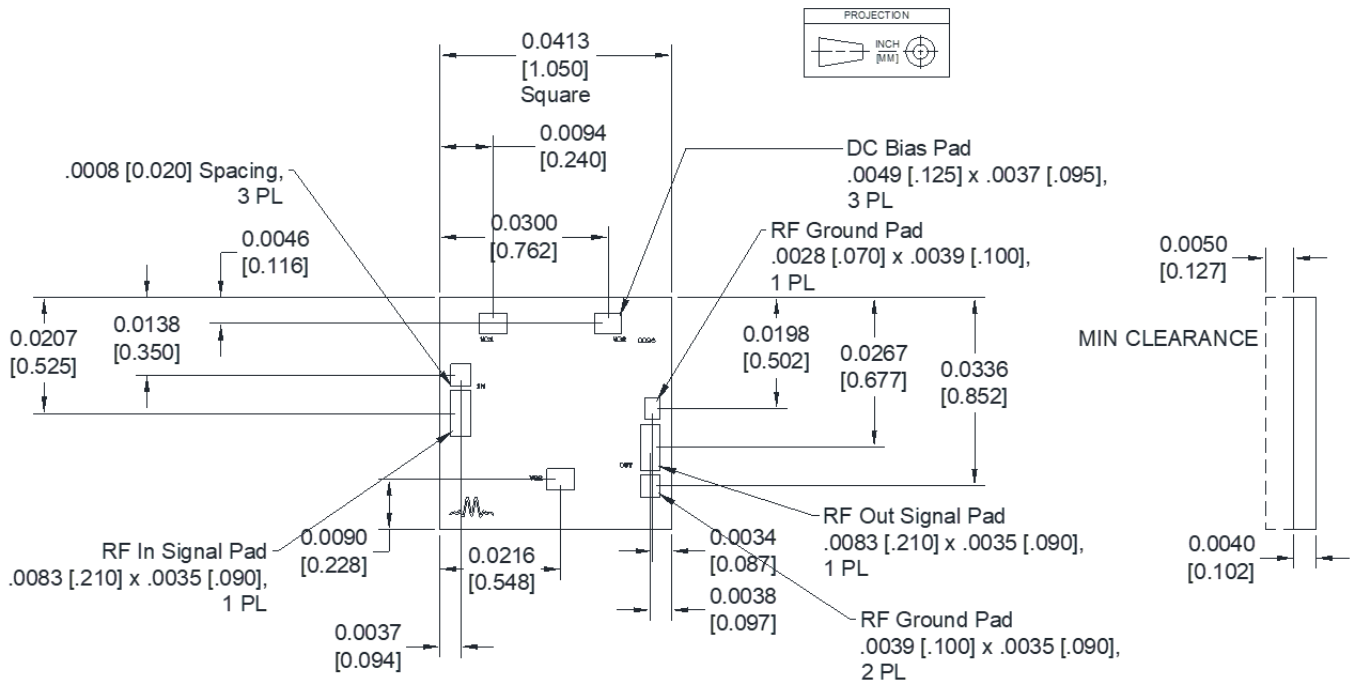
Circuit Considerations – 50 Ω transmission lines should be used for all high frequency connections in and out of the chip. Wirebonds should be kept as short as possible, with multiple wirebonds recommended for higher frequency connections to reduce parasitic inductance. In circumstances where the chip more than .001" thinner than the substrate, a heat spreading spacer tab is optional to further reduce bondwire length and parasitic inductance.

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Mechanical Data

Outline Drawing



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