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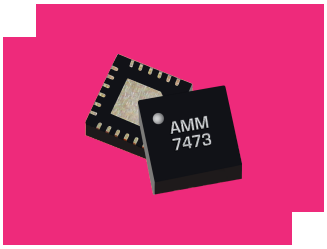
AMM-7473PSM

0.4 - 27 GHz Surface Mount Amplifier

DEVICE OVERVIEW

General Description

The AMM-7473PSM is a high-linearity, low noise distributed amplifier that can provide +25 dBm output power across its 400 MHz to 27 GHz band and features excellent gain flatness. The AMM-7473PSM can serve either as a linear signal amplifier, or as a saturated driver amplifier for H- or S-diode mixers. Additionally, the AMM-7473PSM incorporates an internal choke inductor which eliminates the need for an external bias tee.



Download s-parameters here

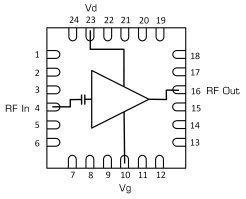
Features

- +25 dBm output power
- 17 dB gain
- Gain flatness
- No external bias tee required

Applications

- Mobile test and measurement equipment
- Radar and satellite communications
- Driver Amplifier for H and S - Diode Mixers

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Packing Size	Green Status	Product Lifecycle	Export Classification
EVB-AMM-7473P	Evaluation Board, 0.4 - 27 GHz Surface Mount Amplifier	-	-	RoHS	Released	EAR99
AMM-7473PSM	0.4 - 27 GHz Surface Mount Amplifier	QFN	-	RoHS	Released	3A001.b.2.d

Table Of Contents

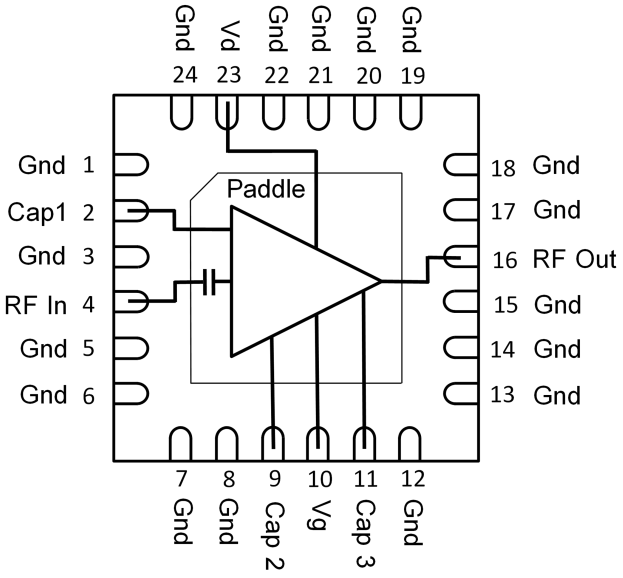
Revision History

Revision Code	Revision Date	Comment
-	2022-08-01	Initial Release

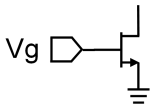
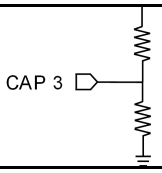
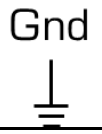
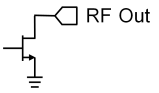
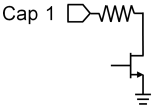
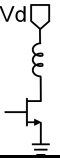
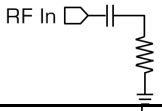
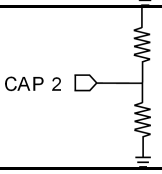
Port Configuration and Functions

Port Diagram

A port diagram of the AMM-7473PSM QFN package is shown below (X-ray view from the top).



Port Functions

Port	Function	Description	Equivalent Circuit for Package
10	Vg	Pin 10 provides a required negative bias which controls the power supply currents to the amplifier. More negative voltages decrease supply current. Apply gate bias voltage Vg before applying drain power supply.	
11	CAP 3	Pin 11 is connected to internal bias circuitry and should be AC grounded through an off-chip bypass capacitor. The value should be at least 100 nF. This pin should not be directly connected to ground.	
1,3, 5-8, 12-15, 17-22, 24, Paddle	Ground	These pins should be connected to ground. Package ground paddle must be connected to a DC/RF ground potential with high thermal and electrical conductivity.	
16	RF Output	Pin 16 is the RF Output port of the amplifier. It is DC coupled, and RF matched to 50 Ω. An external DC blocking capacitor is required.	
2	Cap 1	Pin 2 allows the user to attach additional off chip bypass capacitance to provide adequate low frequency AC grounding termination to the input matching network. The value should be at least 100 nF.	
23	Vd	Pin 23 provides the main power supply for the amplifier. Apply gate bias voltage Vg before applying drain power supply.	
4	RF Input	Pin 4 is the RF Input port of the amplifier die. It is internally DC blocked and RF matched to 50 Ω. RF input pad is GSG with 150 µm pitch.	
9	Cap 2	Pin 9 is connected to internal bias circuitry and should be AC grounded through an off-chip bypass capacitor. The value should be at least 100 nF. This pin should not be directly connected to ground.	

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If any one of these limits are exceeded, the device may become inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Unit
Drain Current (RF Applied)	550	mA
Drain Supply Voltage (Vd)	10	V
Gate Voltage (Vg)	0.5	V
Maximum Operating Temperature for MTTF > 1E6 hours	85	°C
Maximum Storage Temperature	150	°C
Max Junction Temperature for MTTF > 1E6 Hours	175	°C
Max Power Dissipation for MTTF of 1E6 hours at 85°C Baseplate Temperature	3.9	W
Minimum Operating Temperature for MTTF > 1E6 hours	-55	°C
Minimum Storage Temperature	-65	°C
RF Input Power	18	dBm
θ_Jc, Junction to Case Thermal Resistance	23	ºC/W

Package Information

Parameter	Details	Rating
Weight	Package name: QFN	0.05g
Dimensions	-	4x4 mm

Sequencing Requirements

Turn-on Procedure if required biases are unknown:

1. Apply -1 V to Vg.
2. Apply desired Vd.
3. Increase Vg voltage towards -0.5 V until Id = 150 mA.
4. Apply RF input power.

Turn-on Procedure if required biases are known:

1. Apply desired Vg (previously determined to produce 150 mA Idq).
2. Apply desired Vd.
3. Apply RF input power.

Turn-off Procedure:

1. Turn off RF input power.
2. Turn off Vd.
3. Turn off Vg.

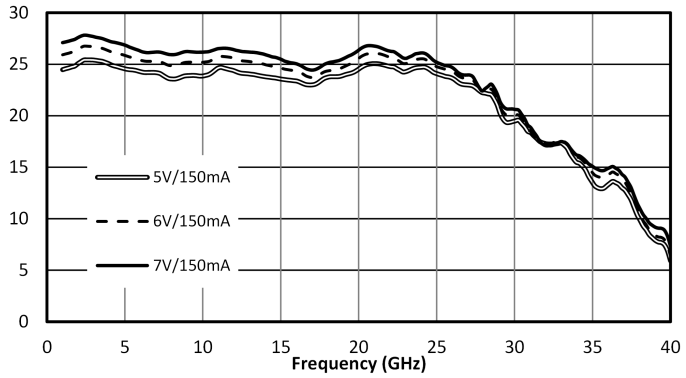
Electrical Specifications

Unless otherwise specified, electrical specifications apply at TA=+25°C, Vd = 7 V, Idq=150 mA (where Idq is the drain current with no RF applied), Vg set as required to achieve Idq = 150 mA in a 50 Ω system.

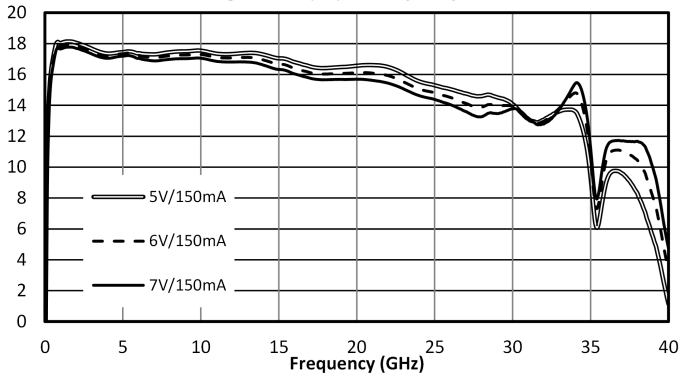
Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)
Small Signal Gain	Vd = 7 V, Vg set to achieve Idq = 150 mA, Pin = -20 dBm	0.4	20
Noise Figure	Vd = 7 V, Vg set to achieve Idq = 150 mA, Pin = -20 dBm	2	5
Noise Figure	Vd = 7 V, Vg set to achieve Idq = 150 mA, Pin = -20 dBm	5	15
Noise Figure	Vd = 7 V, Vg set to achieve Idq = 150 mA, Pin = -20 dBm	15	27
Saturated Output Power	Vd = 7 V, Vg set to achieve Idq = 150 mA, Pin = +15 dBm	0.4	27
Output IP3	Vd = 7 V, Vg set to achieve Idq = 150 mA, Pin = -15 dBm per tone, 10 MHz tone spacing	0.4	27
Input IP3	Vd = 7 V, Vg set to achieve Idq = 150 mA, Pin = -15 dBm per tone, 10 MHz tone spacing	0.4	27
Input Return Loss	Vd = 7 V, Vg set to achieve Idq = 150 mA, Pin = -20 dBm	0.4	27
Output Return Loss	Vd = 7 V, Vg set to achieve Idq = 150 mA, Pin = -20 dBm	0.4	27
Reverse Isolation	Vd = 7 V, Vg set to achieve Idq = 150 mA, Pin = -20 dBm	0.4	27
Input Power for Saturation	Vd = 7 V, Vg set to achieve Idq = 150 mA	0.4	27
DC Supply Quiescent Current (Idq)	Vd = 7 V, Vg = -0.65 V, no RF input applied	-	-

Typical Performance Plots

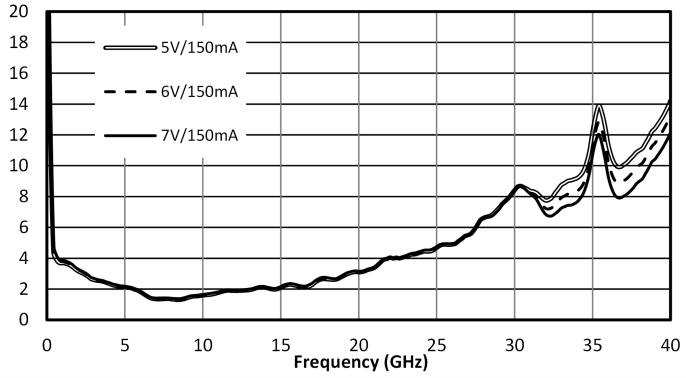
Psat (dBm) vs. Frequency, over Bias



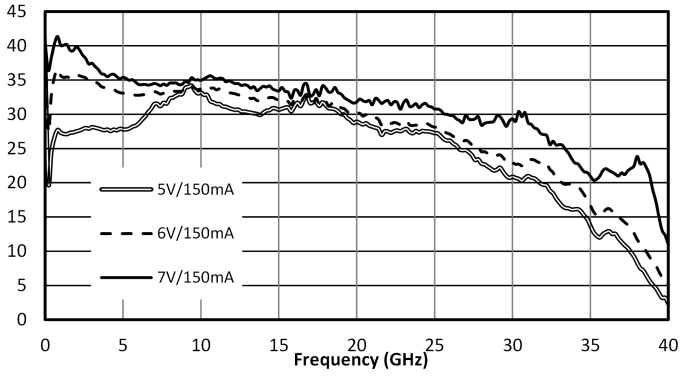
Small Signal Gain (dB) vs. Frequency, over Bias



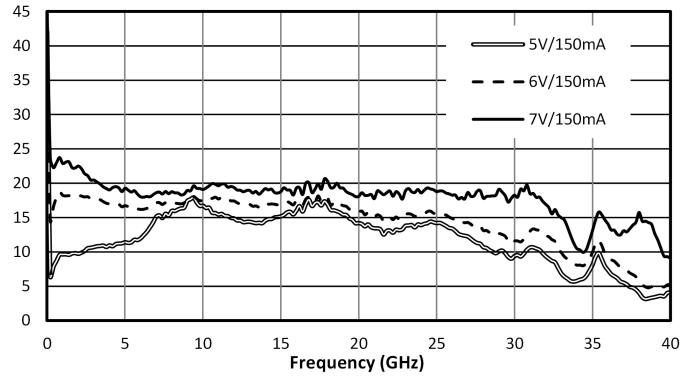
Noise Figure (dB) vs. Frequency, over Bias



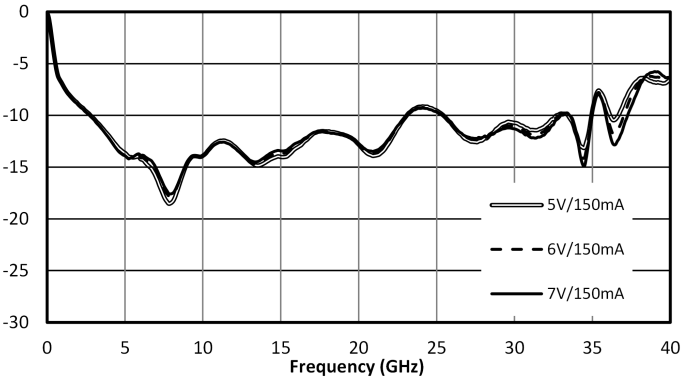
OIP3 (dBm) vs. Frequency, over Bias



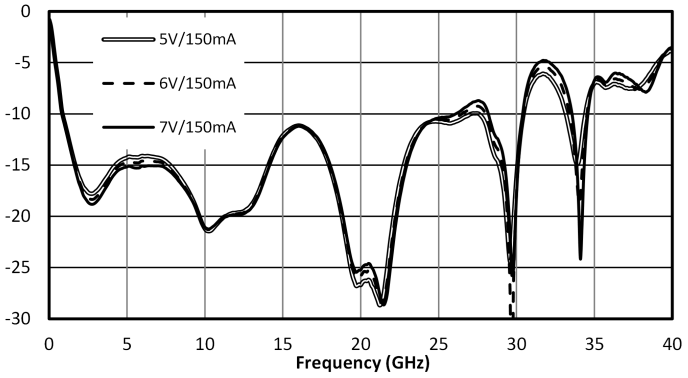
IIP3 (dBm) vs. Frequency, over Bias



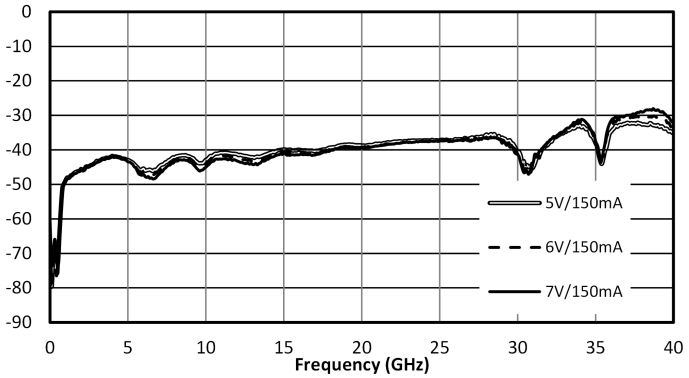
Input Return Loss (dB) vs. Frequency, over Bias



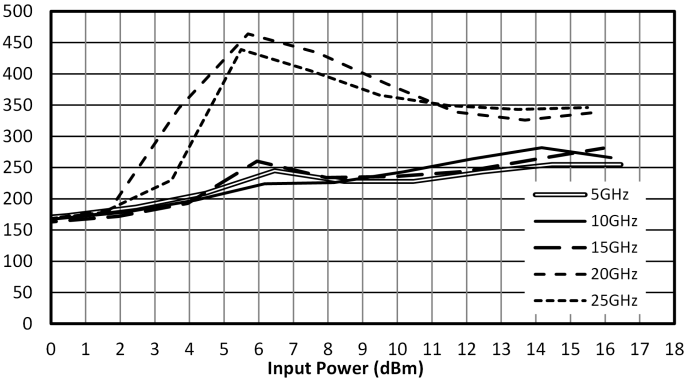
Output Return Loss (dB) vs. Frequency, over Bias



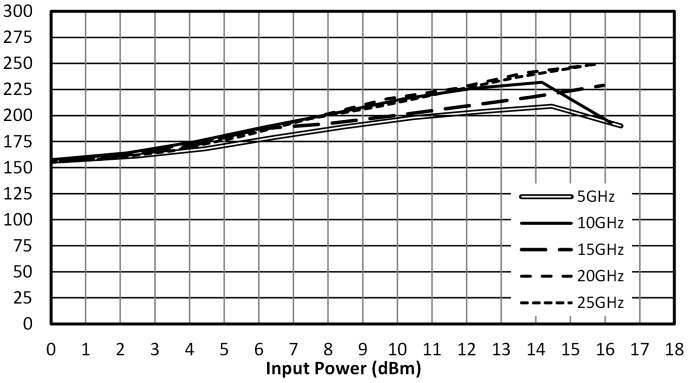
Reverse Isolation (dB) vs. Frequency, over Bias



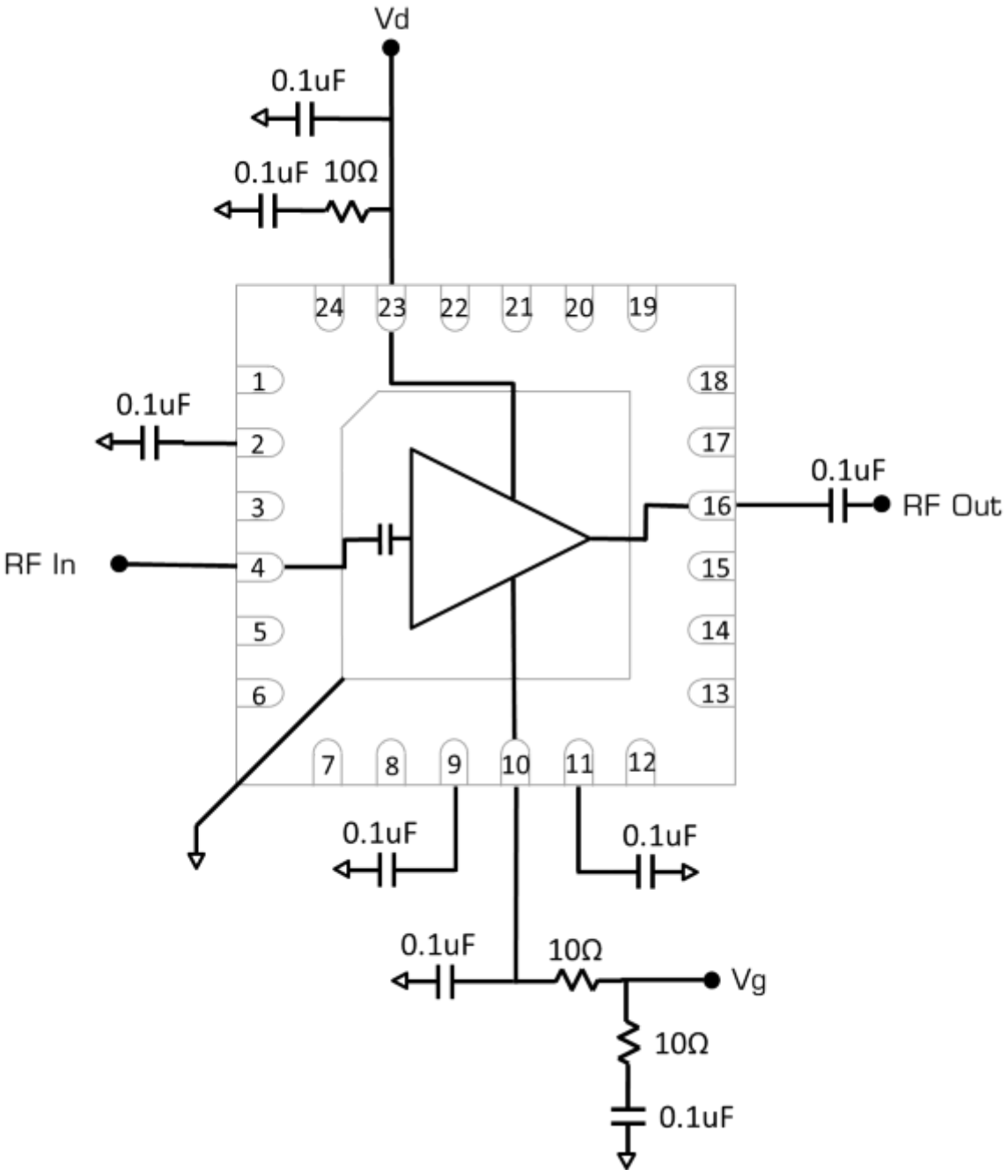
Id (mA) vs. Pin and Frequency (Vd=7V, Idq=150mA)



Id (mA) vs. Input Power and Frequency (Vd=5V, Idq=150mA)



Application Circuit



Application Circuit Description

Bypassing Circuitry

The bypass capacitors on Cap1,2 and 3 (pins 2, 9 and 11) provide an AC ground to internal circuits on the chip. To prevent disruption of the internal biasing circuits or outright damage to the chip, these pins should not be DC coupled to ground. The value should be at least 100 nF to provide adequate AC grounding. Additional 100 nF bypass capacitors should be added to the Vd and Vg lines to stabilize the amplifier and prevent power supply feedback to other parts on the board. A 10 Ω series resistor on the Vg line is also preferred to ensure stable operation across all potential operating conditions. It is recommended to use a broadband capacitor on the RF Out pin to minimize high frequency insertion loss. For more detailed information or specific use recommendations, contact support@markimicrowave.com.

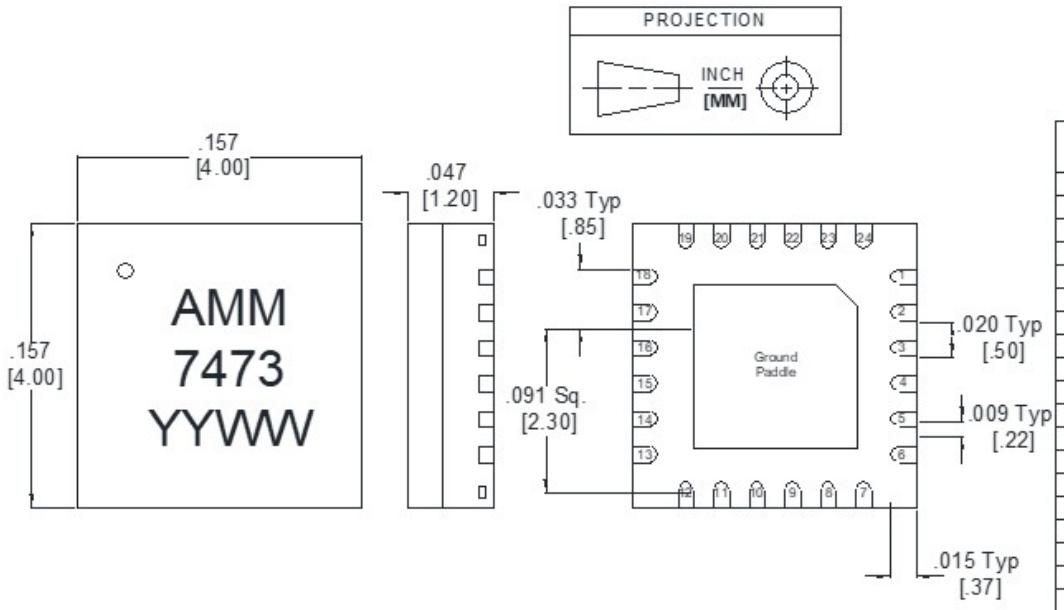
Power Supply and Biasing Circuitry

An internal choke inductor eliminates the need for an external bias tee at the RF Output Port. The main power supply is provided through Vd (pin 23). The power supply should be designed to provide a low noise, constant voltage supply with between 150 and 450 mA. For linear signal operation the current should remain fixed at 150 mA. For saturated LO driver operation the current consumption will increase and depend on operating conditions including input power, frequency, temperature, and bias/power supply voltages. Current should be limited to 450 mA by reducing Vg (more negative) or Vd.

The network attached to the Vg pin should have an impedance of not more than 500 Ω. The current leaving the Vg pin will vary with RF input drive level and can reach up to 1 mA when the amplifier is being used as an LO driver. This could cause an un-intended increase in Vg (less negative) if the Vg pin is being supplied by a high impedance network.

Mechanical Data

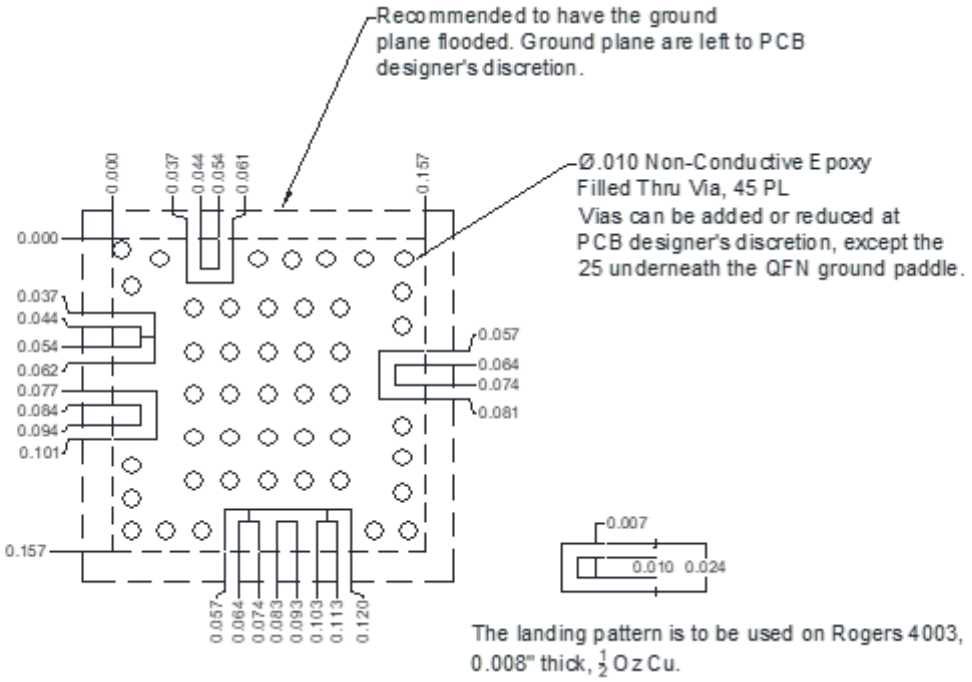
Outline Drawing

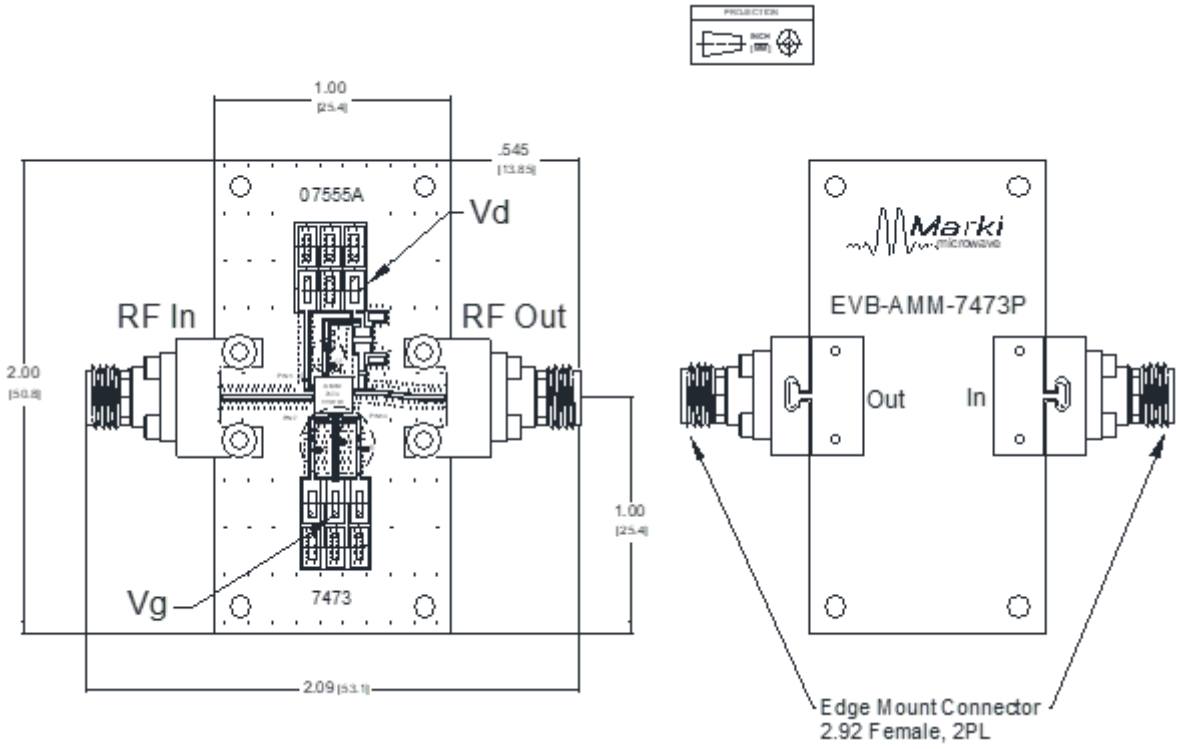


Pin #	Config A
1	GND
2	CAP 1
3	GND
4	RF In
5	GND
6	GND
7	GND
8	GND
9	CAP 2
10	Vg
11	CAP 3
12	GND
13	GND
14	GND
15	GND
16	RF Out
17	GND
18	GND
19	GND
20	GND
21	GND
22	GND
23	Vd
24	GND

1) Substrate material is LCP
2) I/O Leads and Die Paddle is (from base to finish):
   a. Ni: 0.5 um MIN
   b. Pd: 0.02 um MIN
   c. Au: 0.05 um MAX

Footprint Image





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