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AMM-8211PSM

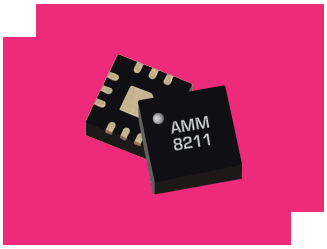
22 - 57 GHz GaAs Driver Amplifier

DEVICE OVERVIEW

General Description

The AMM-8211PSM is a general-purpose broadband MMIC driver amplifier that provides up to +21 dBm output power suitable for driving Marki H or L diode mixers at 22-57 GHz and S diode mixers from 25-50 GHz. This amplifier offers a high +26dBm OIP3 and is offered in a small 3x3mm QFN package.

Download s-parameters here



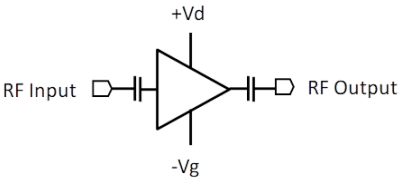
Features

- +21 dBm Output Power
- Broadband Performance
- High Linearity
- Outstanding return loss

Applications

- Mobile test and measurement equipment
- Radar and satellite communications
- 5G transceivers
- Driver amplifier L,H,S – diode mixers

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
AMM-8211PSM	22 - 57 GHz GaAs Driver Amplifier	PSM	REACH RoHS	Released	3A001.b.2.d
EVB-AMM-8211P	Evaluation Board, 22-57 GHz GaAs LO driver amplifier	EVB	REACH RoHS	Released	EAR99

Table Of Contents

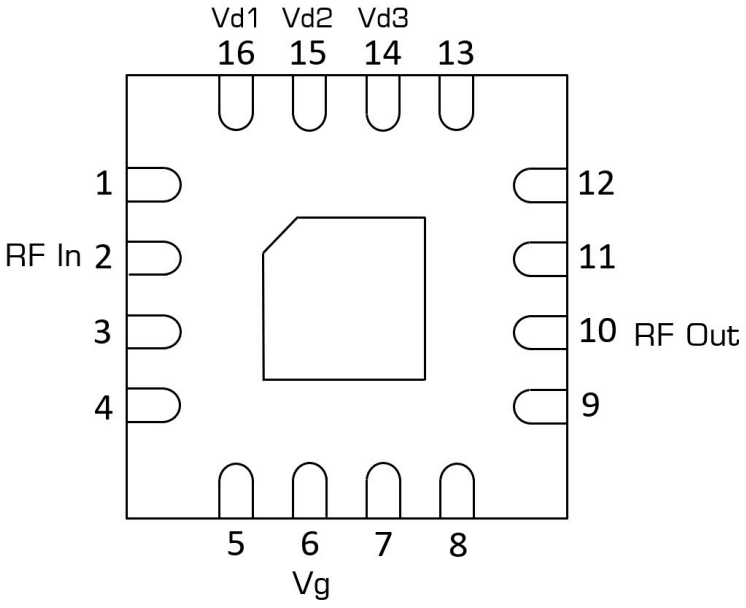
Revision History

Revision Code	Revision Date	Comment
-	2024-09-12	Initial Release

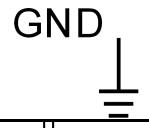
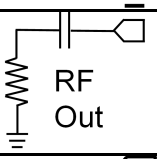
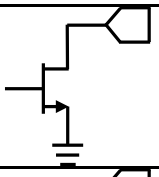
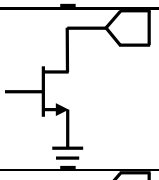
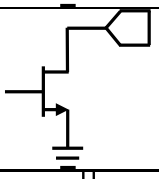
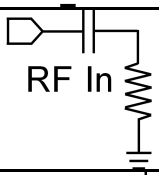
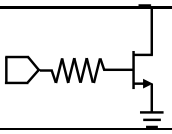
Port Configuration and Functions

Port Diagram

A port diagram of the AMM-8211PSM is shown below. (Top down x-ray view)



Port Functions

Port	Function	Description	Equivalent Circuit for Package
Paddle	Ground	Ground paddle and non-connected pins must be connected to a DC/RF ground potential with high thermal and electrical conductivity, and low inductance.	
Pin 10	RF Output	Pin 10 is the RF output of the amplifier, and is matched to 50 ohms. It is internally DC blocked.	
Pin 14	Positive DC Supply Vd3	Pin 14 provides DC voltage to the amplifier's third stage. Negative voltage must be supplied to Pin 6 before turning on the positive supply voltage.	
Pin 15	Positive DC Supply Vd2	Pin 15 provides DC voltage to the amplifier's second stage. Negative voltage must be supplied to Pin 6 before turning on the positive supply voltage.	
Pin 16	Positive DC Supply Vd1	Pin 16 provides DC voltage to the amplifier's first stage. Negative voltage must be supplied to Pin 6 before turning on the positive supply voltage.	
Pin 2	RF Input	Pin 2 is the RF input of the amplifier, and is matched to 50 ohms. It is internally DC blocked.	
Pin 6	Negative DC Supply Vg	Pin 6 provides -0.4V to -0.6V of DC voltage. This must be turned on before turning on the positive supply voltage to Pins 14-16.	
Pins 1, 3, 4, 5, 7, 8, 9, 11, 12, 13	Non-connect (NC)	These pins are not internally connected to the amplifier. They should be connected to ground for increased RF isolation and mechanical stability. Datasheet RF performance was measured with these pins connected to ground.	-

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If any one of these limits are exceeded, the device may become inoperable or have a reduced lifetime. Reliability limits are individual, instantaneous catastrophic limits only. Functional operation limits are indicated below. Operation of the device at multiple absolute maximum limits or for extended periods at a single limit can cause degradation and damage to the device.

Parameter	Maximum Rating	Unit
Maximum Operating Temperature	85	°C
Maximum Storage Temperature	150	°C
Max Junction Temperature for MTTF of > 1E6 hours	175	°C
Minimum Operating Temperature	-40	°C
Minimum Storage Temperature	-65	°C
Positive Bias Current (Id)	450	mA
Positive Bias Voltage (VB)	5.5	V
RF Input Power	20	dBm
Thermal Resistance, θJC	94	ºC/W

Package Information

Parameter	Details	Rating
Dimensions	-	3 x 3 mm
Moisture Sensitivity Level	-	MSL 1

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

Parameter	Min	Nominal	Max	Unit
Positive DC Current (Id) (No RF Input)	125	175	225	mA
Ambient Temperature	-55	25	85	°C
Positive DC Voltage (Vd)	2.5	3	3	V
Input Power for Saturation	8	11	13	dBm
Gate Bias DC Voltage (Vg)	-0.6	-0.5	-0.4	V

Electrical Specifications

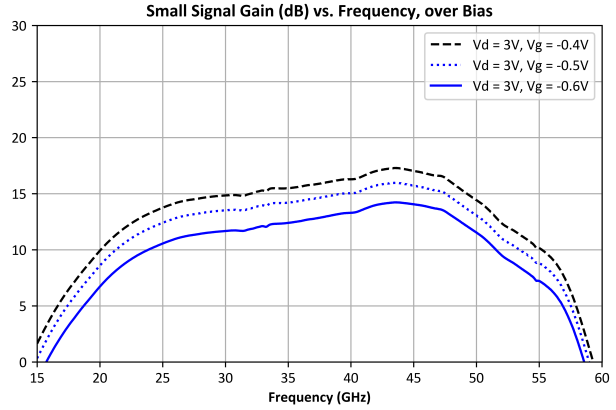
The electrical specifications apply at TA=+25°C in a 50Ω system. Unless otherwise specified, performance is measured with Vd=3V and Vg=-0.5V.

Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Output IP3	Vd = 3V, Vg = -0.5V, -12dBm Input Power, 10MHz tone spacing	50	57	-	20	-	dBm
Bias Requirements [1]	Vd = 3V, Vg = -0.5V	-	-	-	175	-	mA
Input IP3	Vd = 3V, Vg = -0.5V, -12dBm Input Power, 10MHz tone spacing	22	57	-	12	-	dBm
Input Power for Saturation	Vd = 3V, Vg = -0.5V	22	57	-	11	-	dBm
Input Return Loss	Vd = 3V, Vg = -0.5V, -25dBm Input Power	22	57	-	11	-	dB
Noise Figure	Vd = 3V, Vg = -0.5V	22	57	-	6	-	dB
Output IP3	Vd = 3V, Vg = -0.5V, -12dBm Input Power, 10MHz tone spacing	22	50	-	26	-	dBm
Output Power	Vd = 3V, Vg = -0.5V	45	57	-	17	-	dBm
Output Power	Vd = 3V, Vg = -0.5V	30	45	-	20	-	dBm
Output Power	Vd = 3V, Vg = -0.5V	22	30	-	17	-	dBm
Output Return Loss	Vd = 3V, Vg = -0.5V, -25dBm Input Power	22	57	-	10	-	dB
Reverse Isolation	Vd = 3V, Vg = -0.5V, -25dBm Input Power	22	57	-	48	-	dB
Small Signal Gain	Vd = 3V, Vg = -0.5V, -25dBm Input Power	45	57	-	11	-	dB
Small Signal Gain	Vd = 3V, Vg = -0.5V, -25dBm Input Power	30	48	-	14	-	dB
Small Signal Gain	Vd = 3V, Vg = -0.5V, -25dBm Input Power	22	30	-	12	-	dB

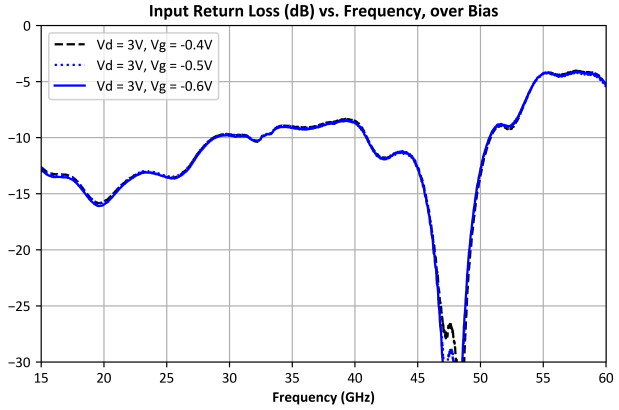
[1] Bias conditions tested with no RF input power.

Typical Performance Plots (Over Bias vs Frequency)

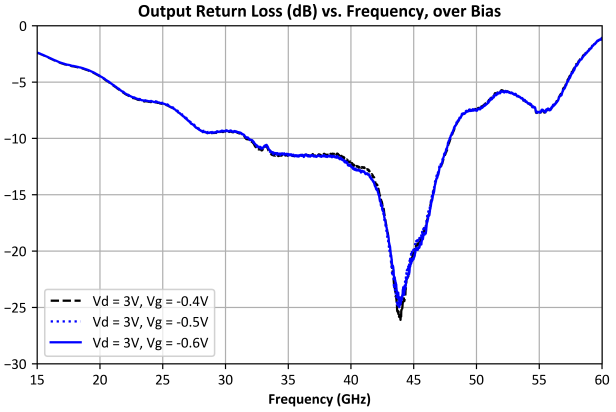
Small Signal Gain (dB) vs. Frequency, over Bias



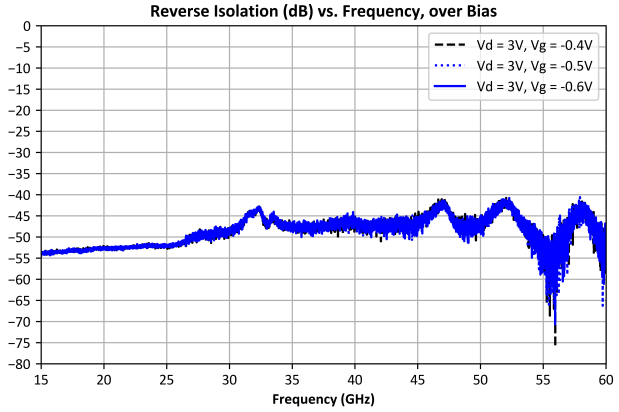
Input Return Loss (dB) vs. Frequency, over Bias



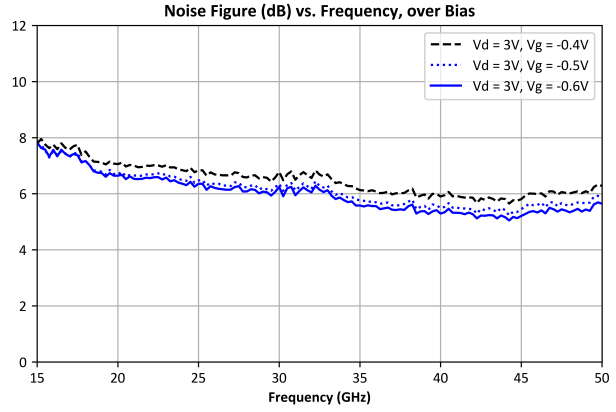
Output Return Loss (dB) vs. Frequency, over Bias



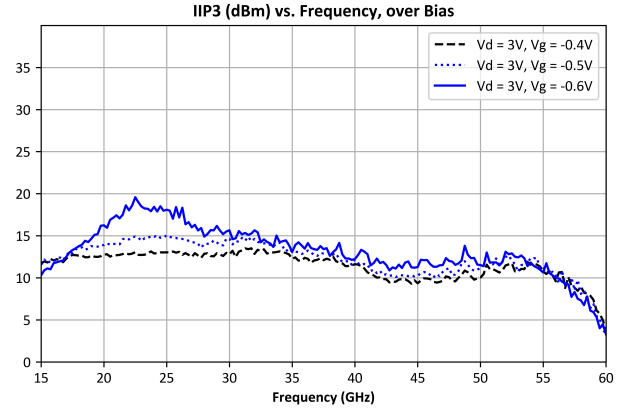
Reverse Isolation (dB) vs. Frequency, over Bias



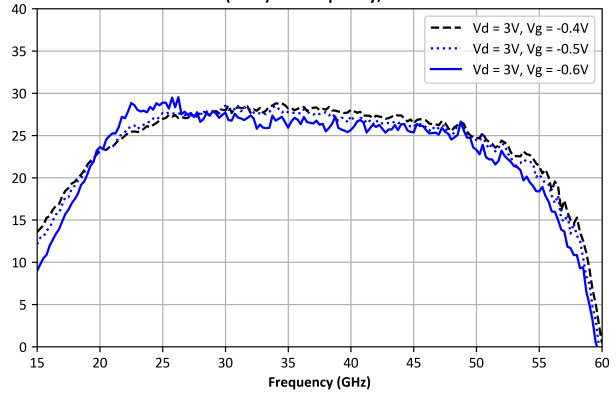
Noise Figure (dB) vs. Frequency, over Bias



IIP3 (dBm) vs. Frequency, over Bias

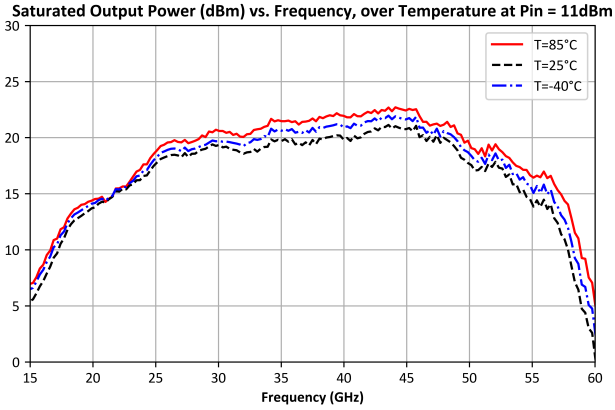


OIP3 (dBm) vs. Frequency, over Bias

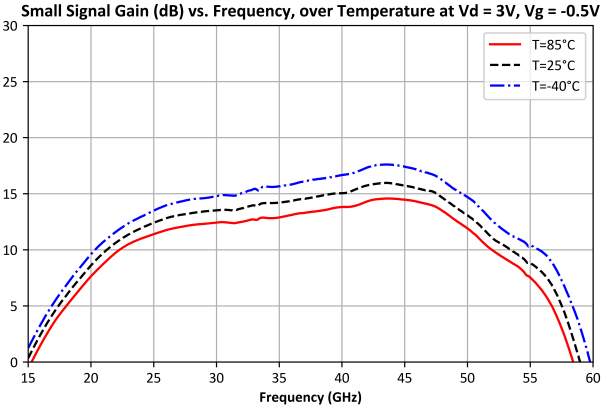


Typical Performance Plots (Over Temp vs Frequency)

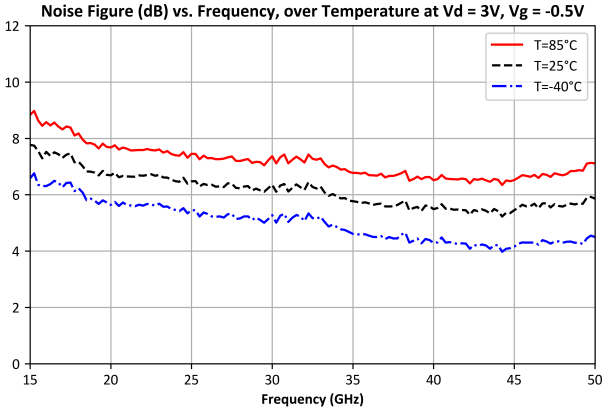
Saturated Output Power (dBm) vs. Frequency, over Temperature at Pin = 11dBm



Small Signal Gain (dB) vs. Frequency, over Temperature at Vd = 3V, Vg = -0.5V

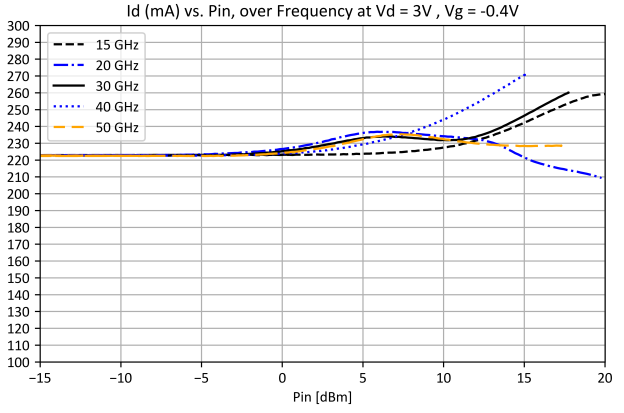


Noise Figure (dB) vs. Frequency, over Temperature at Vd = 3V, Vg = -0.5V

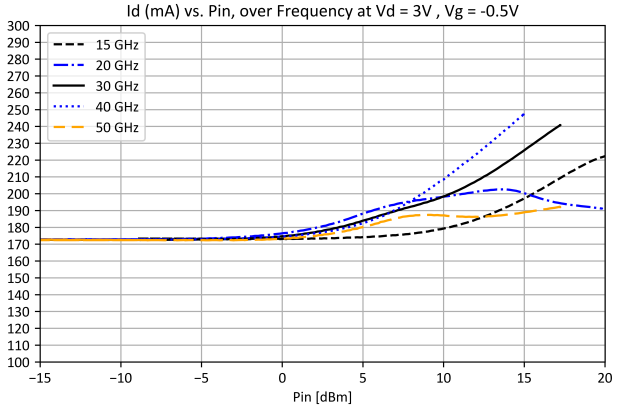


Typical Performance Plots (Over Frequency vs Input Power)

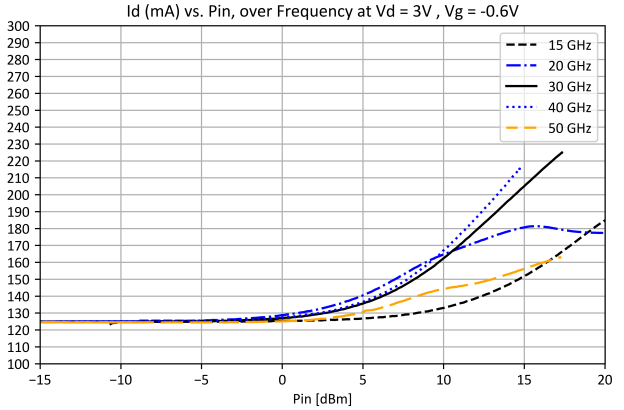
Id (mA) vs. Pin, over Frequency at Vd = 3V , Vg = -0.4V



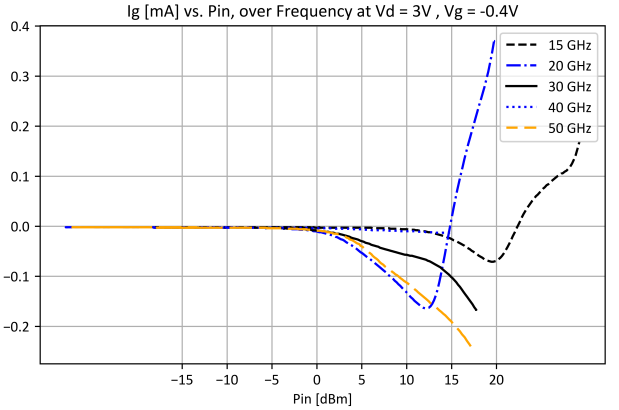
Id (mA) vs. Pin, over Frequency at Vd = 3V , Vg = -0.5V



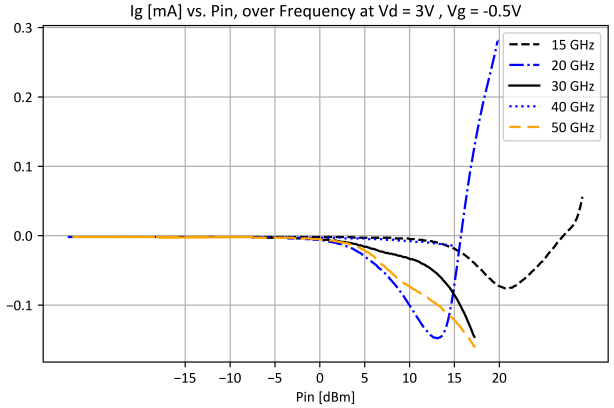
Id (mA) vs. Pin, over Frequency at Vd = 3V , Vg = -0.6V



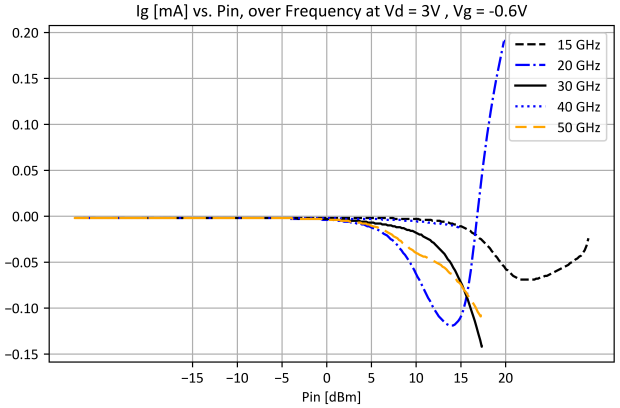
Ig [mA] vs. Pin, over Frequency at Vd = 3V , Vg = -0.4V



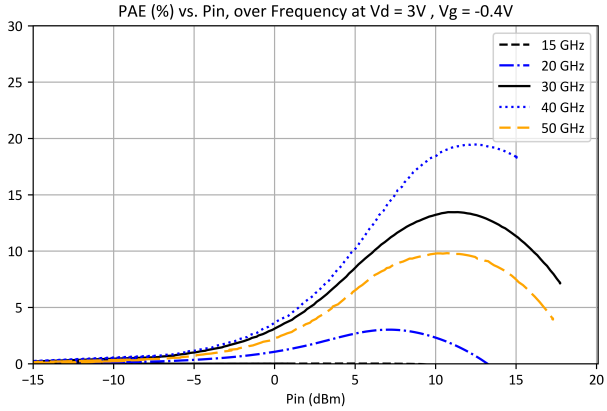
Ig [mA] vs. Pin, over Frequency at Vd = 3V , Vg = -0.5V



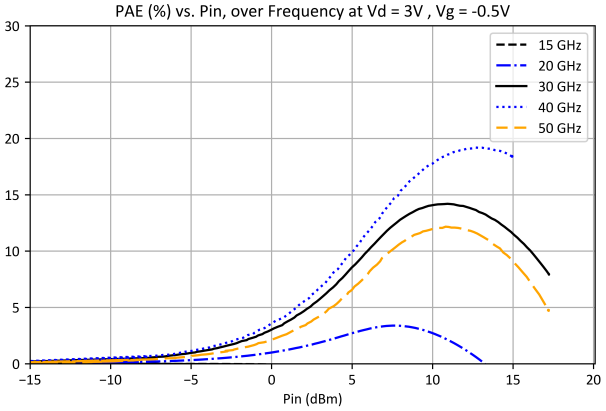
Ig [mA] vs. Pin, over Frequency at Vd = 3V , Vg = -0.6V



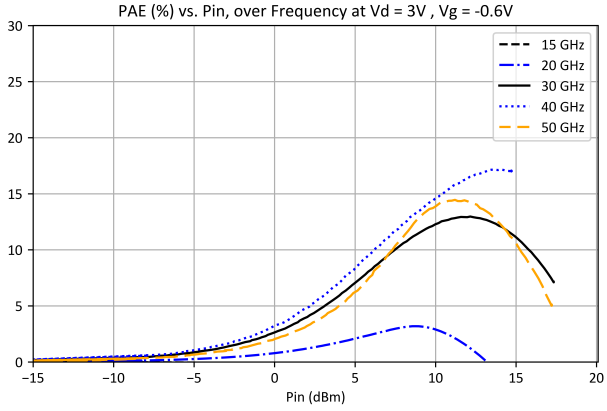
PAE (%) vs. Pin, over Frequency at Vd = 3V , Vg = -0.4V



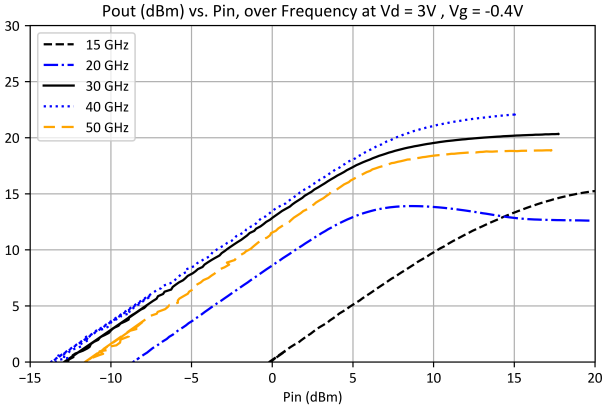
PAE (%) vs. Pin, over Frequency at Vd = 3V , Vg = -0.5V



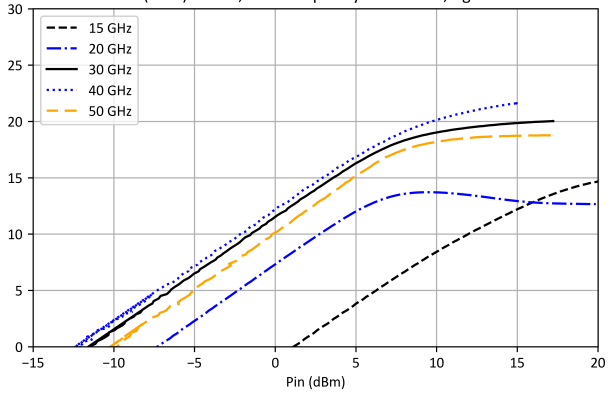
PAE (%) vs. Pin, over Frequency at Vd = 3V , Vg = -0.6V



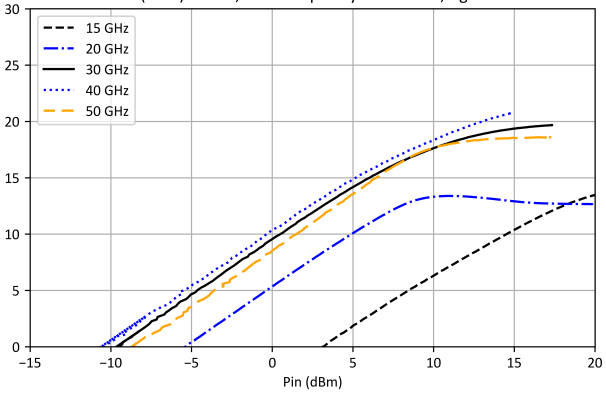
Pout (dBm) vs. Pin, over Frequency at Vd = 3V , Vg = -0.4V



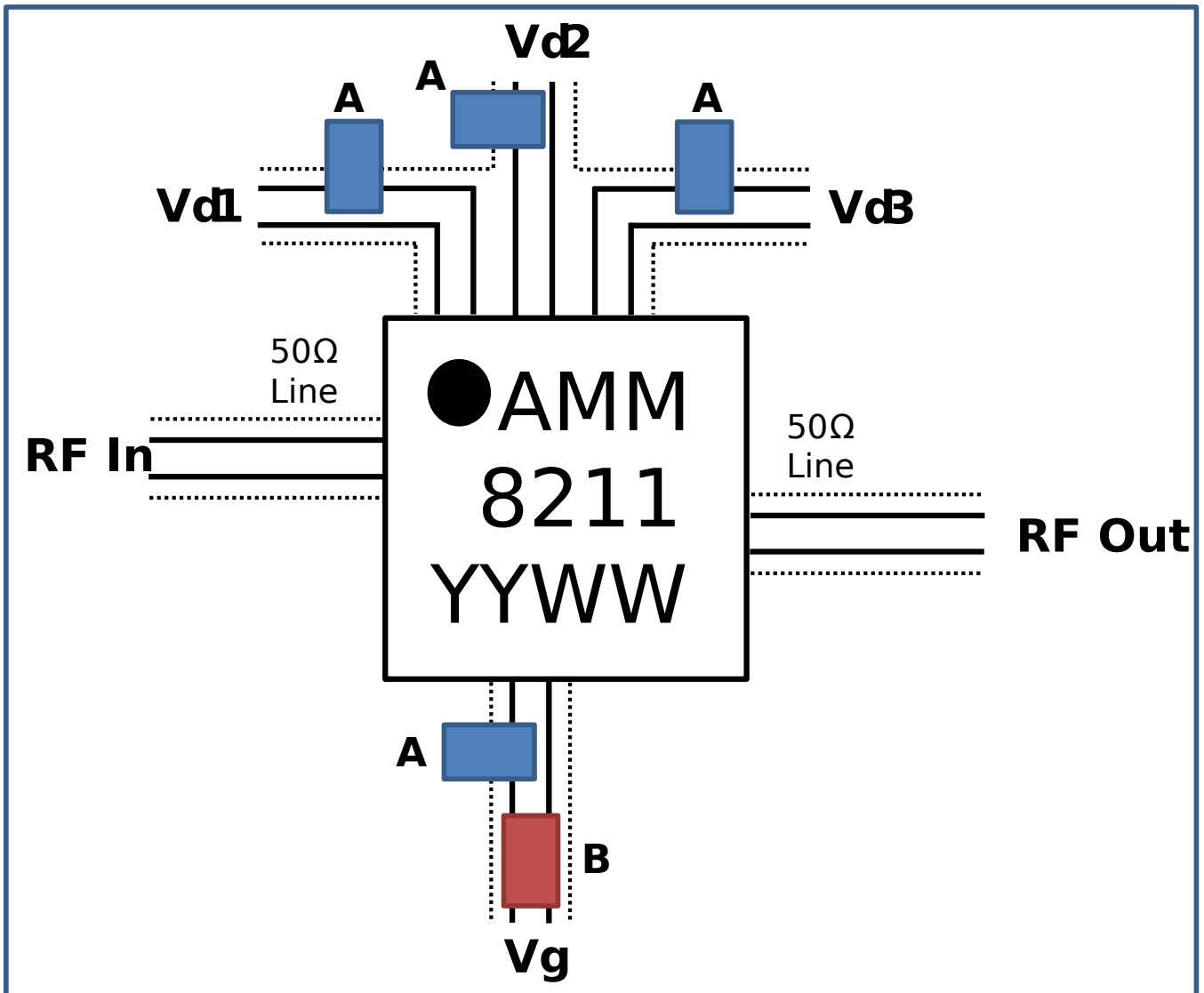
Pout (dBm) vs. Pin, over Frequency at Vd = 3V , Vg = -0.5V



Pout (dBm) vs. Pin, over Frequency at Vd = 3V , Vg = -0.6V



Application Circuit



Designator	Description	Sample Part Number
A	0.1µF 16V 0402 Capacitor	AVX 0402YD104KAT2
B	10Ω 0402 Resistor	TE CPF0402B10RE1

Application Circuit Description

The three Vd lines are separated to minimize feedback between the transistor's stages. The passive devices should be 0402 or 0201 surface mount. Examples of suitable passive devices would be the AVX 0402YD104KAT2A capacitor and TE CPF0402B10RE1 resistor. In addition to the resistor and capacitor on the gate pin, the layout of the board should be designed to minimize stray coupling between the drain and gate biasing traces on the board. Additionally, the gate biasing pin AMM-8211PSM can draw up to 0.3mA at certain combinations of frequency and input power.

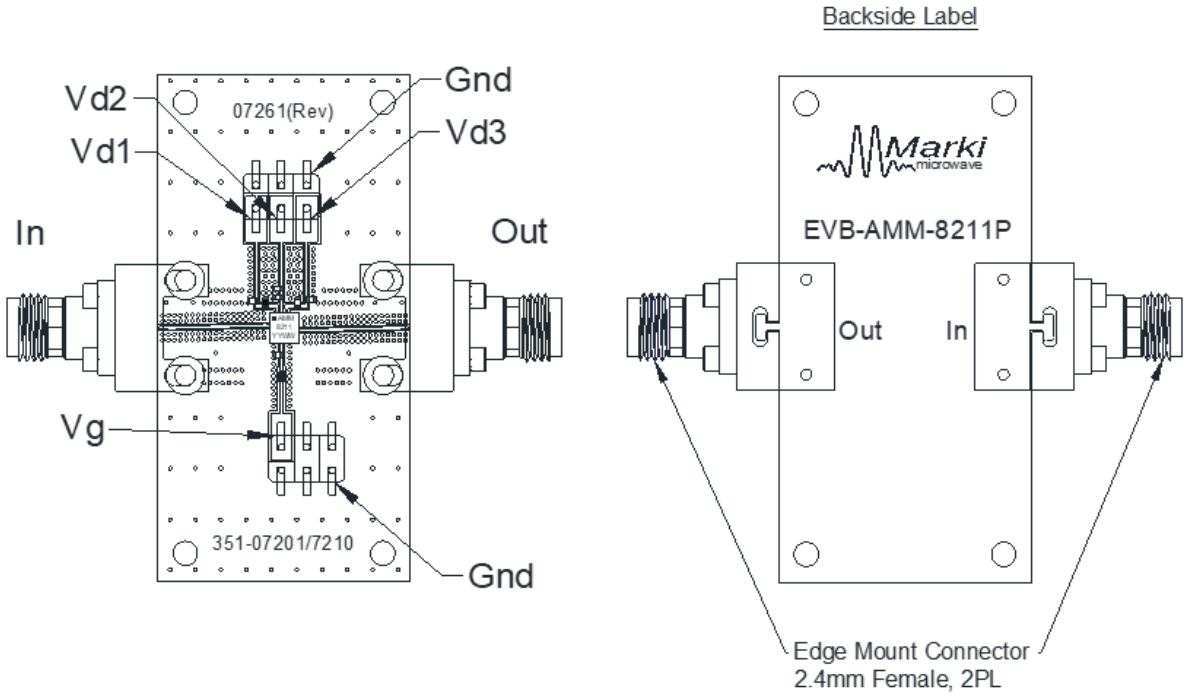
Constant Current and Constant Voltage Operation

As with most amplifiers utilizing HEMT technology, the AMM-8211PSM can be biased with a constant gate and drain voltage, or with a constant drain current by regulating the gate voltage. Using a constant gate and drain voltage for biasing reduces complexity, but has variable current consumption during operation. On the other hand, biasing the gate using a feedback network that samples the drain current minimizes unit-to-unit variation in gain and other parameters.

Under small signal excitation at a fixed temperature, these two approaches are equivalent. However, they will diverge in large signal conditions, where the drain current is affected by the frequency and power of the input signal. In these conditions P1dB, P3dB, and P5dB will be somewhat different, but based on tests with similar parts, they will be within a few dBm of the constant voltage curves.

Header Pinouts

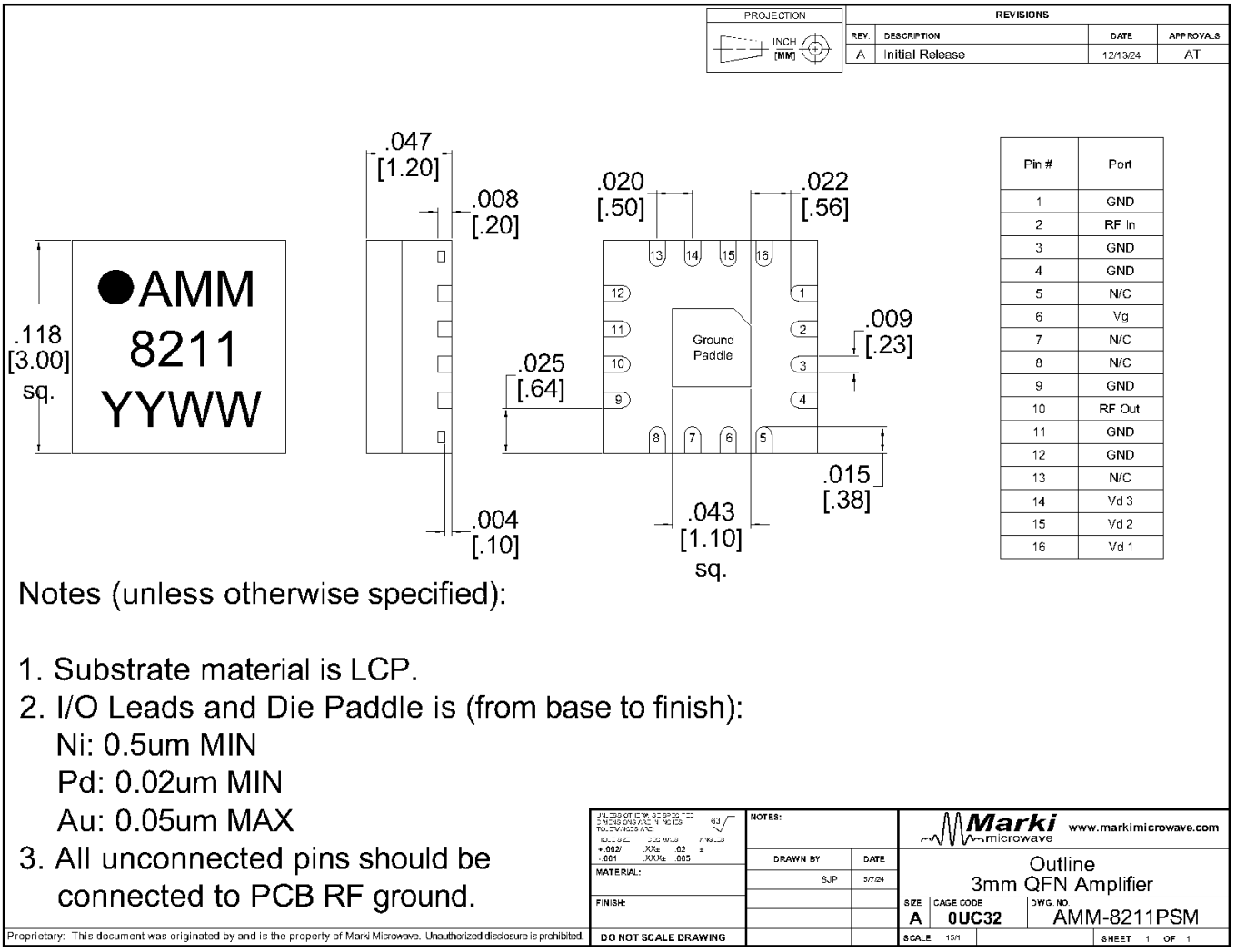
On the EVB-AMM-8211P, there are two headers for biasing the drains and gates of the transistors. The pinout of the headers is given with their location on the evaluation board below:



Mechanical Data

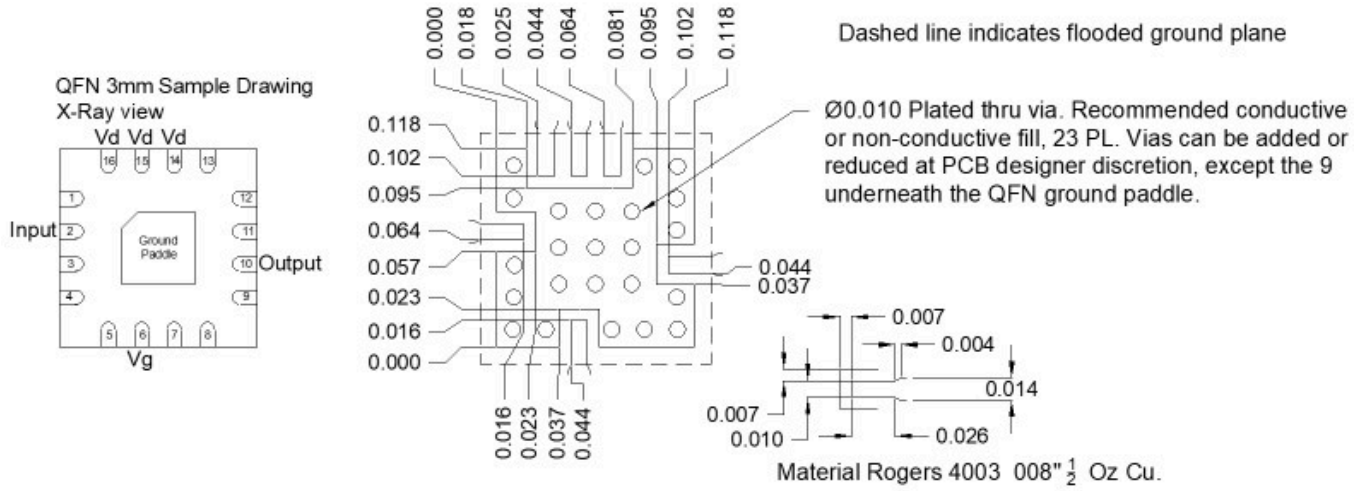
Outline Drawing

Download : Outline 2D Drawing

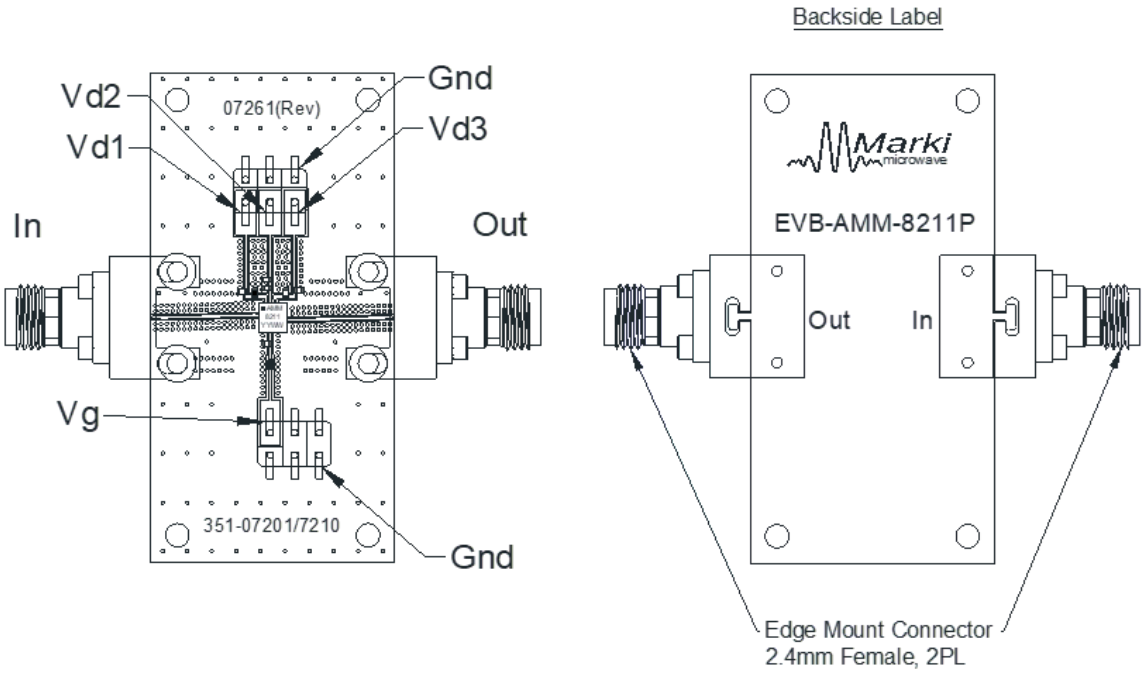


Footprint Image

Download : Footprint Drawing



Evaluation Board - Outline Drawing



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