

AMM-9858PSM

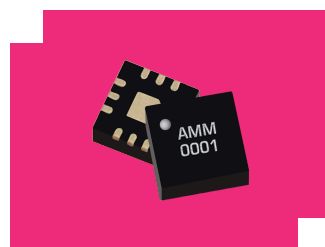
2 - 20 GHz Wideband Low Noise Amplifier

DEVICE OVERVIEW

General Description

The AMM-9858PSM is a wideband low noise amplifier capable of providing 17 dB gain and +30 dBm OIP3 with a low 1.9 dB typical noise figure. The AMM-9858PSM is an ideal linear signal amplifier for applications requiring low power consumption and small form-factors. This amplifier has exceptionally flat response across its entire operating bandwidth.

[Download s-parameters here](#)



Features

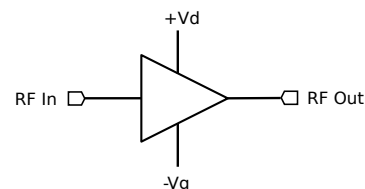
- Broadband 2 to 20GHz Operation
- Low Noise Figure
- Exceptionally Flat RF Performance Across Frequency
- Excellent Return Losses

Applications

- Communication Systems
- Test and Measurement Equipment
- Satellite Communications
- Electronic Warfare

Functional Block

Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
AMM-9858PSM	2 - 20 GHz Wideband Low Noise Amplifier	QFN	RoHS REACH	Released	EAR99
<u>EVB-AMM-9858P</u>	Evaluation Board, AMM-9858PSM Wideband Low Noise Amplifier	-	REACH RoHS	Released	-

AMM-9858PSM

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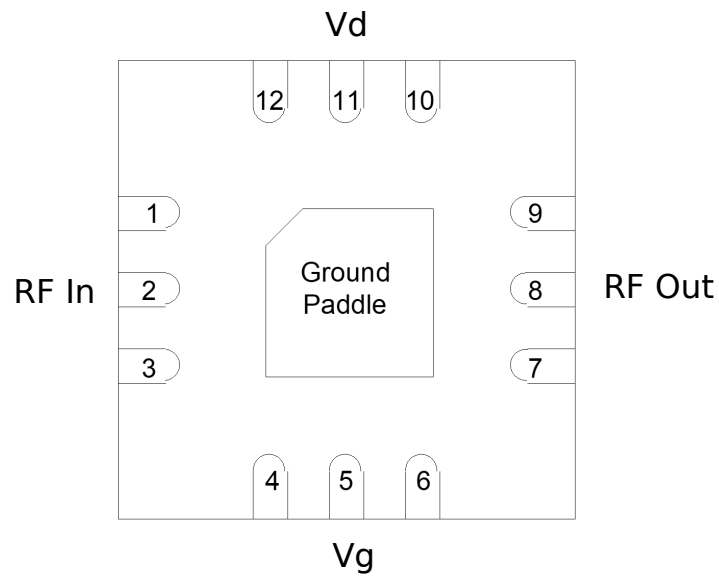
Revision History

Revision Code	Revision Date	Comment
-	2025-03-10	Initial Release

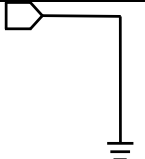
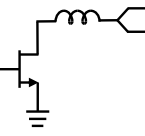
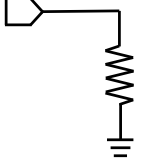
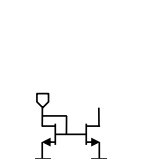
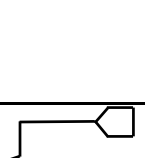
Port Configuration and Functions

Port Diagram

A port diagram of the AMM-9858PSM is shown below.



Port Functions

Port	Function	Description	Equivalent Circuit for Package
Paddle	Ground	DC and RF Ground are provided through the QFN paddle. The paddle should be attached to a DC/RF ground with high thermal and electrical conductivity.	
Pin 11	Vd	This is the positive DC supply voltage for the amplifier IC. This pin is nominally set to +5V. This part requires an off-chip bypass capacitor of 0.1uF installed at this pin as close to the IC as possible. See applications circuit.	
Pin 2	RF Input	This is the amplifiers RF input port. This port is internally matched to 50 Ohms and is internally DC shorted to GND. This pin may be left floating if no DC is present on the line but should be DC blocked otherwise.	
Pin 5	Vg	This is the negative DC bias voltage for the amplifier IC. The voltage at this pin controls the current draw Id of the part. Higher voltage results in higher current. For normal operation, the voltage at this pin is adjusted to produce an Id of 76mA when Vd=5V. This part requires an off-chip bypass capacitor in series with a 10 Ohm resistor installed at this pin as close to the IC as possible. See applications circuit.	
Pin 8	RF Output	This is the amplifiers RF output port. This port is internally matched to 50 Ohms and is internally DC shorted to GND. This pin may be left floating if no DC is present on the line but should be DC blocked otherwise.	
Pins 1,3,4,6,7,9,10 and 12	Non-connect (NC)	These pins are not internally connected. Datasheet performance is measured with these pins connected to ground.	-

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If any one of these limits are exceeded, the device may become inoperable or have a reduced lifetime. Reliability limits are individual, instantaneous catastrophic limits only. Functional operation limits are indicated below. Operation of the device at multiple absolute maximum limits or for extended periods at a single limit can cause degradation and damage to the device.

Parameter	Maximum Rating	Unit
Drain Current (Id) (No RF Applied)	84	mA
Maximum Operating Temperature for MTTF > 1E6 hours	85	°C
Maximum Storage Temperature	125	°C
Minimum Operating Temperature for MTTF > 1E6 hours	-40	°C
Minimum Storage Temperature	-65	°C
Negative Bias Voltage	-2	V
Positive Drain Supply Voltage (Vd)	8	V
RF Input Power	10	dBm

Package Information

Parameter	Details	Rating
Dimensions	-	3 x 3 mm
Moisture Sensitivity Level	-	MSL 1

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications. Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

Parameter	Min	Nominal	Max	Unit
Positive DC Voltage (Vd)	4	5	5	V
Ambient Temperature	-40	25	85	°C
Negative Bias Voltage (Vg)	-0.5	-0.2	-0.2	V
Positive DC Current (Id) (No RF Input)	32	76	76	mA

Sequencing Requirements

Turn-on Procedure:

1. Apply Vg (Pin 5)
2. Apply Vd (Pin 11)

Turn-off Procedure:

1. Turn off Vd (Pin 11)
2. Turn off Vg (Pin 5)

Note: RF input power can be injected at any moment in the bias sequencing procedure.

Electrical Specifications

The electrical specifications apply at TA=+25°C in a 50Ω system. QFNs are 100% RF tested.

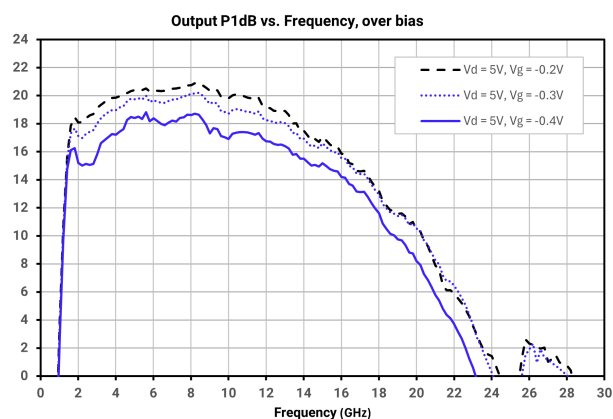
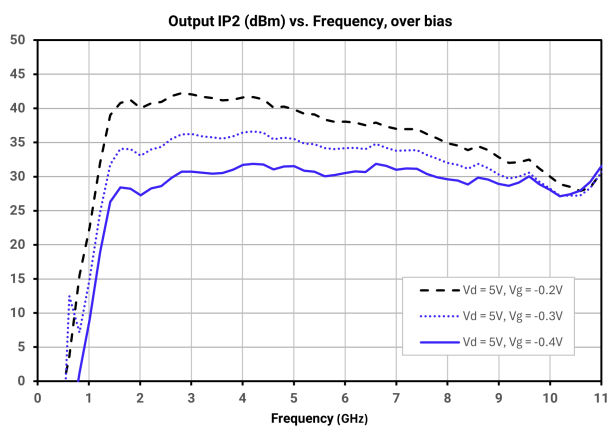
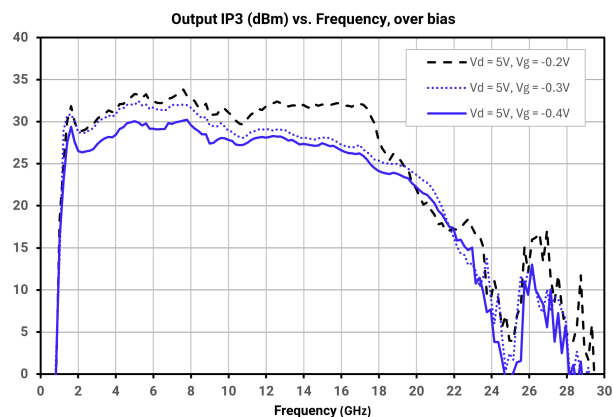
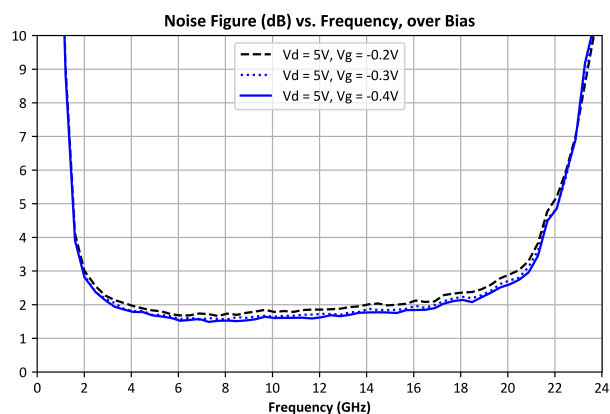
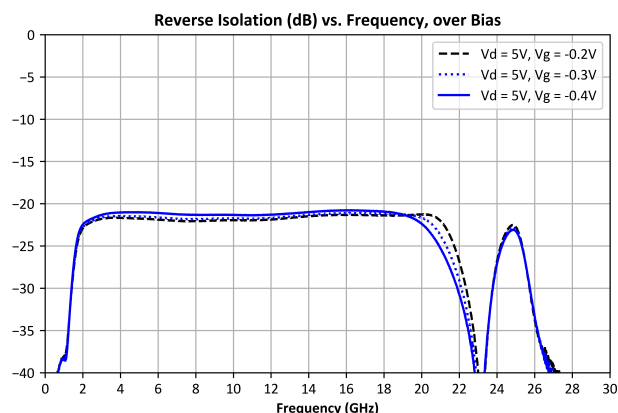
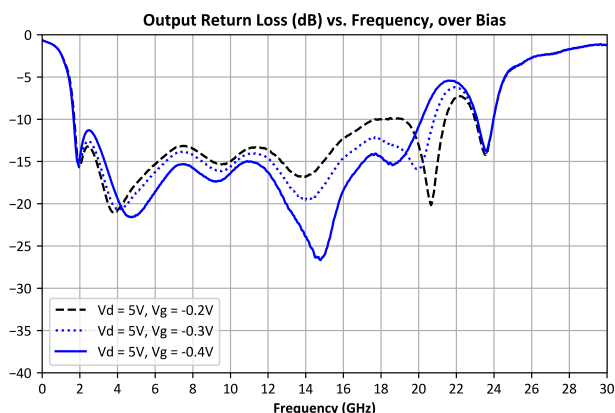
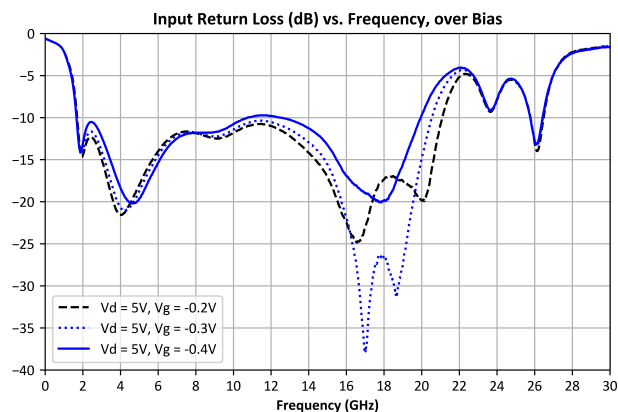
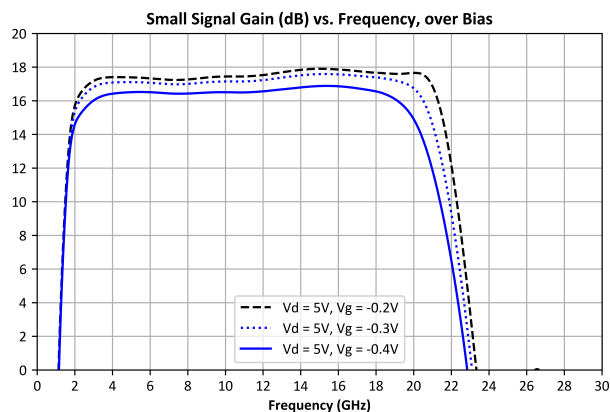
Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Small Signal Gain	Configuration A, 25°C, Input Power = -20.00 dBm Input, Vd1=5, Vb1=-0.2, Id1=76	2	20	-	17.5	-	dB
Input Return Loss	Configuration A, 25°C, Input Power = -20.00 dBm Input, Vd1=5, Vb1=-0.2, Id1=76	2	20	-	14	-	dB
Output Return Loss	Configuration A, 25°C, Input Power = -20.00 dBm Input, Vd1=5, Vb1=-0.2, Id1=76	2	20	-	14	-	dB
Reverse Isolation	Configuration A, 25°C, Input Power = -20.00 dBm Input, Vd1=5, Vb1=-0.2, Id1=76	2	20	-	22	-	dB
Noise Figure	Configuration A, 25°C, Input Power = -20.00 dBm Input, Vd1=5, Vb1=-0.2, Id1=76	2	20	-	1.9	-	dB
Output IP3	5V/-0.2V bias, 20MHz tone spacing, Input Power = -10dBm	2	20	-	30	-	dBm
Output IP2	5V/-0.2 bias, 20MHz tone spacing, Input Power = -10dBm	2	20	-	37	-	dBm
Output P1dB	5V/-0.2V bias	2	20	-	18	-	dBm
Drain Current, Id ¹	5V/-0.2V bias, No RF Applied	-	-	-	76	-	mA

^[1] Bias conditions for Id tested with no RF input power. Bias conditions presented as Vd/Vg.

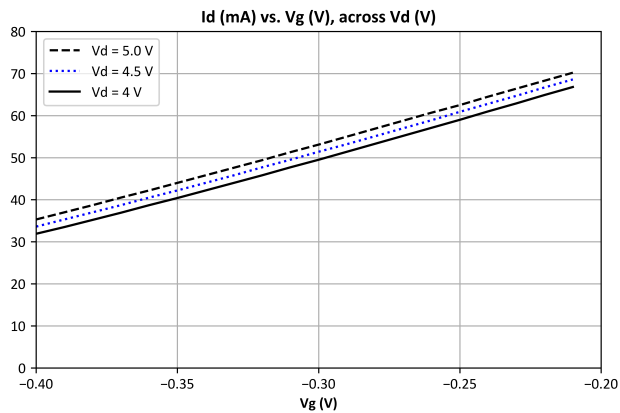
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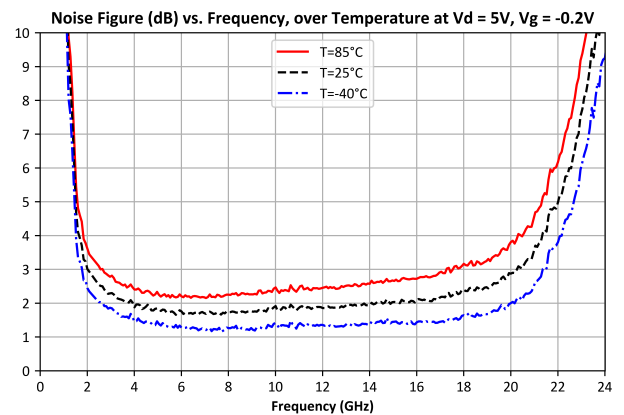
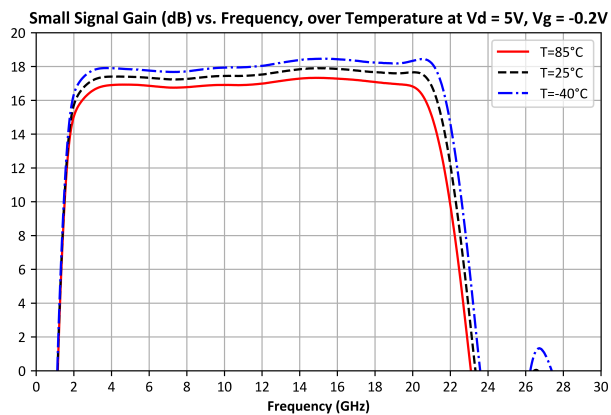
Typical Performance Plots (vs Bias)



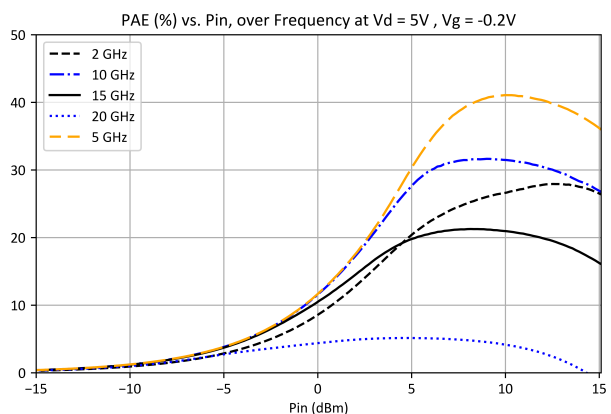
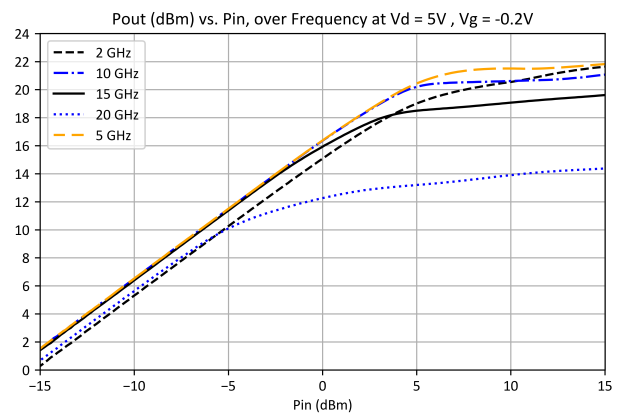
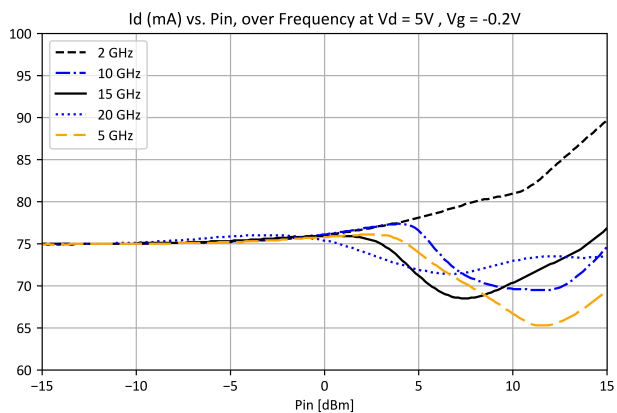
AMM-9858PSM 2 - 20 GHz Wideband Low Noise Amplifier



Typical Performance Plots (vs Temperature)



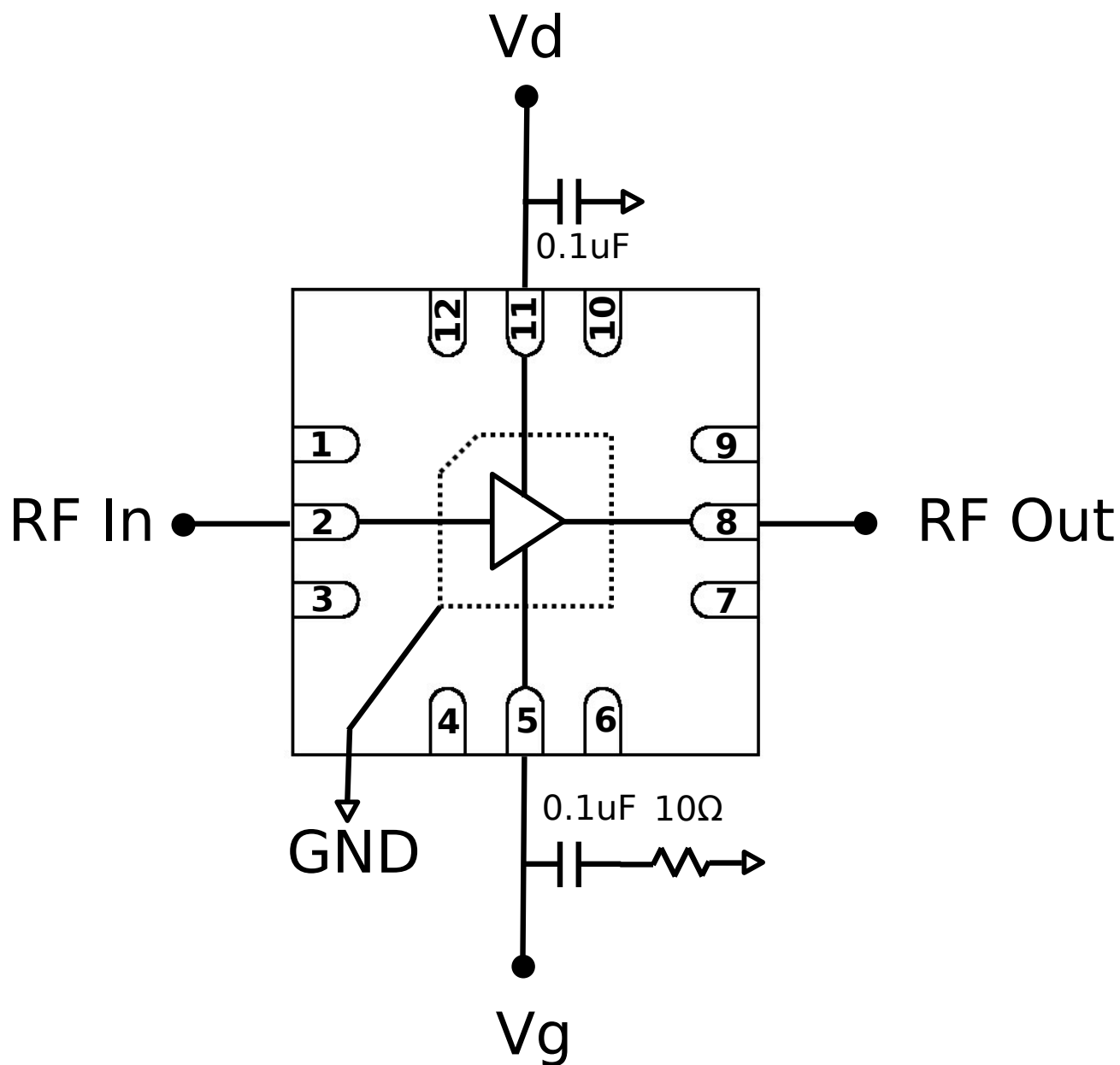
Typical Performance Plots (vs Input Power)



AMM-9858PSM

2 - 20 GHz Wideband Low Noise
Amplifier

Application Circuit



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Application Circuit Description

Above is the recommended application circuit for the AMM-9858PSM. Multiple DC power supply bypassing capacitors are shown around the part. DC drain voltage is supplied to the amplifier across a 0.1uF bypass capacitor to the Vd pin. DC bias voltage is supplied to the Vg pin across a 0.1uF+10Ω bypass capacitor combination. The RF input and output ports are internally shorted to GND but can be left floating if no DC is present on the RF line. If DC is present, blocking capacitors are required at the input and output.

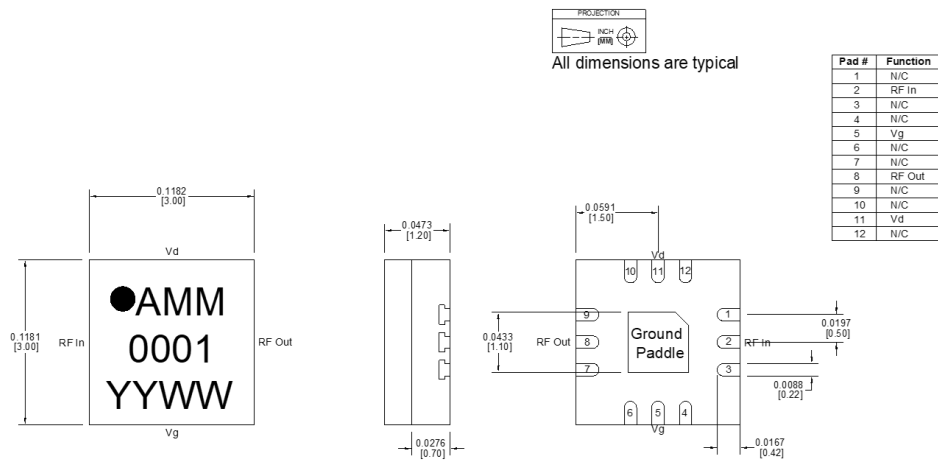
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2 - 20 GHz Wideband Low Noise Amplifier

Mechanical Data

Outline Drawing

Download : [Outline 2D Drawing](#)



Notes (unless otherwise specified):

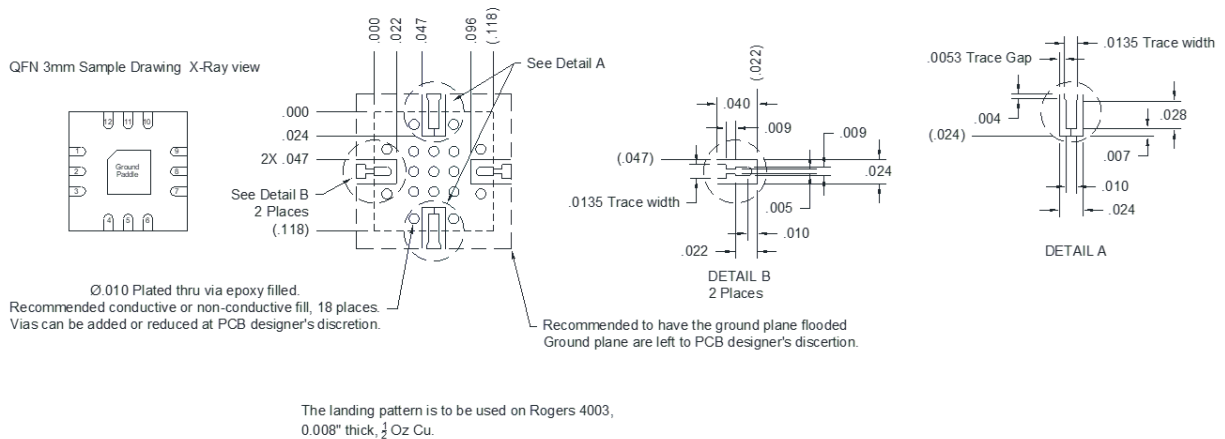
1. Substrate material is LCP.
2. I/O Leads and Die Paddle are 0.05 micron Au over 0.02 microns Pd over 0.5 microns Ni.
3. All unconnected pins should be connected to PCB RF ground.

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Footprint Image

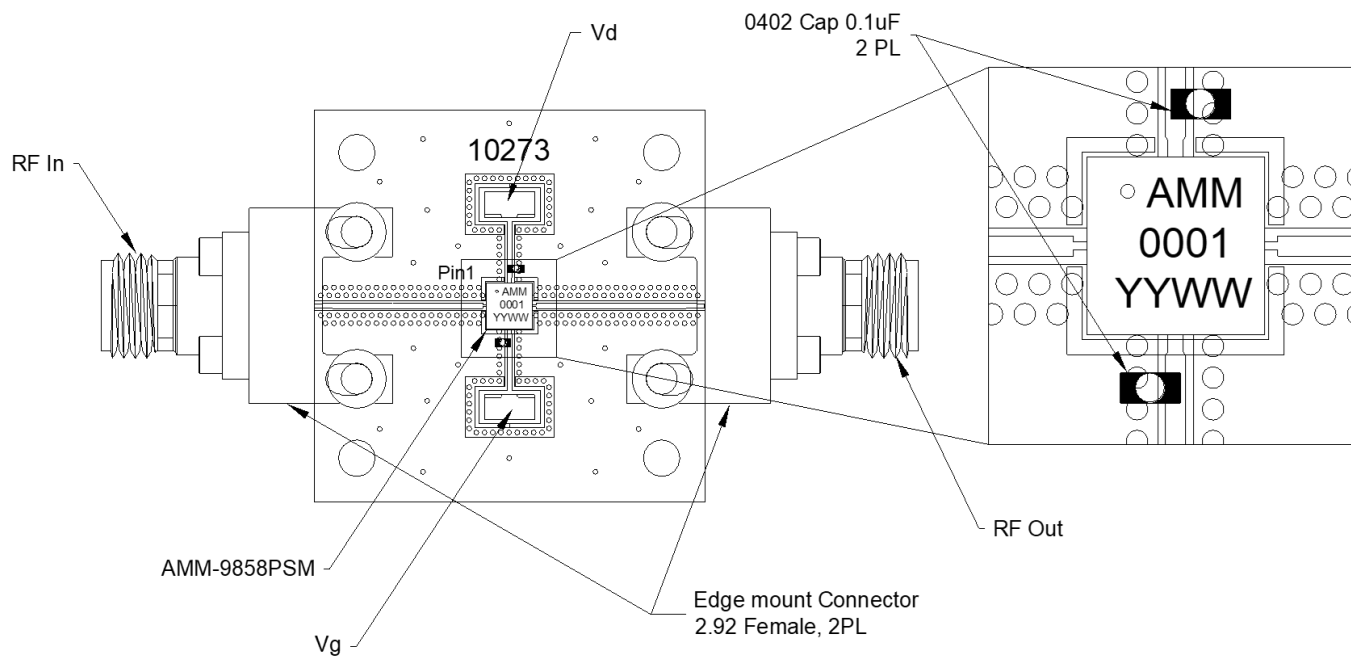
Download : [Footprint Drawing](#)



AMM-9858PSM

2 - 20 GHz Wideband Low Noise
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Evaluation Board - Outline Drawing



AMM-9858PSM

2 - 20 GHz Wideband Low Noise Amplifier

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