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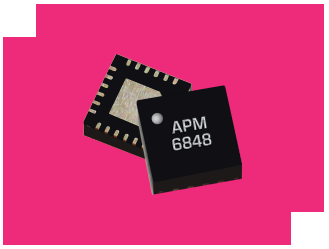
APM-6848SM

2-30 GHz Surface Mount Low Phase Noise Amplifier

DEVICE OVERVIEW

General Description

The APM-6848SM is an integrated 2-stage broadband, low phase noise LO driver amplifier designed to provide a saturated +20 dBm output power from a 0-4 dBm input power with low DC power consumption, packaged in a 4mm QFN. This amplifier uses GaAs HBT technology for low phase noise, and is optimized to provide enough power to drive the LO port of an S-diode mixer from 2 GHz to 20 GHz or an H or L diode mixer from 2 GHz to 32 GHz. This amplifier can be operated with a variety of bias conditions including VC=VB=5V for both low power and high power applications.



Download s-parameters here

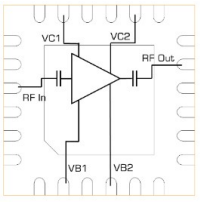
Features

- -165 dBc/Hz phase noise at 10 kHz offset frequency
- Power and gain control
- +22 dB gain
- Low DC power consumption
- Positive-only biasing
- No sequencing required
- Unconditionally stable
- Integrated DC blocks – No bias-tees or off-chip blocking required

Applications

- Mobile test and measurement equipment
- Radar
- SATCOM
- 5G transceivers
- Driver amplifier for S, H, and L – diode mixers
- Suitable as a T3 mixer driver

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
APM-6848SM	2-30 GHz Surface Mount Low Phase Noise Amplifier	QFN	REACH RoHS	Obsolete	EAR99
EVAL-APM-6848SM	Evaluation Board, 2-30 GHz Surface Mount Low Phase Noise Amplifier	EVAL	REACH RoHS	Obsolete	EAR99

APM-6848SM

2-30 GHz Surface Mount Low Phase Noise Amplifier

Table Of Contents

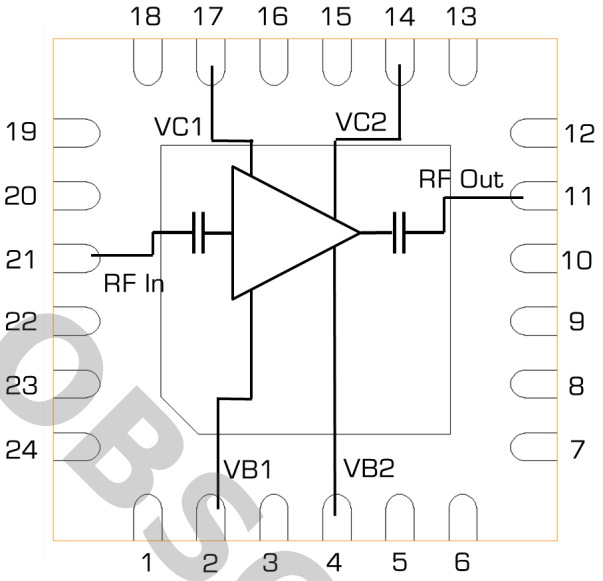
Revision History

Revision Code	Revision Date	Comment
-	2019-12-01	Datasheet Initial Release
A	2020-05-01	Updated EVAL drawing and status
B	2020-07-01	Updated Min small signal gain spec
C	2020-07-01	Updated Max Operating Temperature
D	2020-11-01	Updated Thermal Specs and Min Specs, added link to landing pattern
E	2020-12-01	Adjusted performance plots to adhere to Max input power spec.

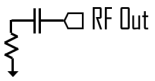
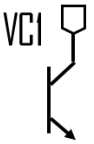
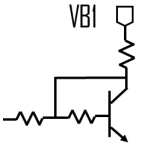
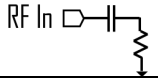
Port Configuration and Functions

Port Diagram

A top-down port diagram of the APM-6848SM is shown below.



Port Functions

Port	Function	Description	Equivalent Circuit for Package
11	RF Output	This is the RF Output port of the amplifier die. It is internally DC blocked and RF matched to 50 Ω. Must have less than 7:1 VSWR when operating with voltage larger than 5V on VC1 or VC2.	
14	Collector Supply Port 2	Pad VC2 is the DC voltage supply pad to the 2nd stage of the amplifier IC. Larger VC voltage will result in larger power consumption and larger power output. See typical performance plots for performance at different bias conditions.	
17	Collector Supply Port 1	Pad VC1 is the DC voltage supply pad for the 1st stage of the amplifier IC. See Typical performance plots for performance at different bias conditions.	
2	Base Supply Port 1	Pad VB1 is the DC voltage supply pad for a current mirror which controls the collector current of the 1st stage (Ic1). Larger voltages result in a higher current draw through pad VC1, effectively functioning as a gain control pin for the 1st stage of the amplifier. See typical performance plots for performance at different bias conditions.	
21	RF Input	This is the RF Input port of the amplifier die. It is internally DC blocked and RF matched to 50 Ω.	
4	Base Supply Port 2	Pad VB2 is the DC voltage supply pad for a current mirror which controls the collector current of the 2nd stage (Ic2). Larger voltages result in a higher current draw through pad VC2, effectively functioning as a gain control pin for the 2nd stage of the amplifier. See typical performance plots for performance at different bias conditions.	
GND	Ground	Backside of the IC must be connected to a DC/RF ground with high thermal and electrical conductivity.	

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may become inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Unit
Collector Positive Bias Voltage (VC, VC1, VC2)	7	V
Current Mirror Positive Bias Current (Ib, Ib1+Ib2)	8	mA
Current Mirror Positive Bias Voltage (VB, VB1, VB2)	7	V
Maximum Operating Temperature	85	°C
Maximum Storage Temperature	150	°C
Max Junction Temperature for MTTF > 1E6 Hours	125	°C
Minimum Operating Temperature	-40	°C
Minimum Storage Temperature	-65	°C
Output Load VSWR	7	-
Positive Bias Current (Ic1)	90	mA
Positive Bias Current (Ic2)	90	mA
RF Input Power	5	dBm
θJC	53	ºC/W

Package Information

Parameter	Details	Rating
Dimensions	-	4 x 4 mm

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

Parameter	Min	Nominal	Max	Unit
Ambient Temperature	-40	25	85	°C
Positive DC Current Mirror Voltage (VB1)	3	5	6	V
Positive DC Current Mirror Current (Ib1)	0.9	2	2.6	mA
Positive DC Current Mirror Voltage (VB2)	3	5	6	V
Positive DC Voltage (VC1)	3	5	6	V
Positive DC Current (Ic1)	8	21	40	mA
Positive DC Voltage (VC2)	3	5	6	V
Positive DC Current Mirror Voltage (Ib2)	0.9	2	2.6	mA
Positive DC Current (Ic2)	8	21	40	mA

Maximum recommended operating current conditions without RF input applied. Please see typical performance plots for relationship between RF input power and DC current draw.

Sequencing Requirements

There is no sequencing required to power up or power down the amplifier.
Amplifier must have an output load connected when operating with a VC1, or VC2 voltage larger than +5V.

Electrical Specifications

The electrical specifications apply at TA=+25°C in a 50Ω system. All Specifications and performance shown with VC1 = VC2 and VB1 = VB2

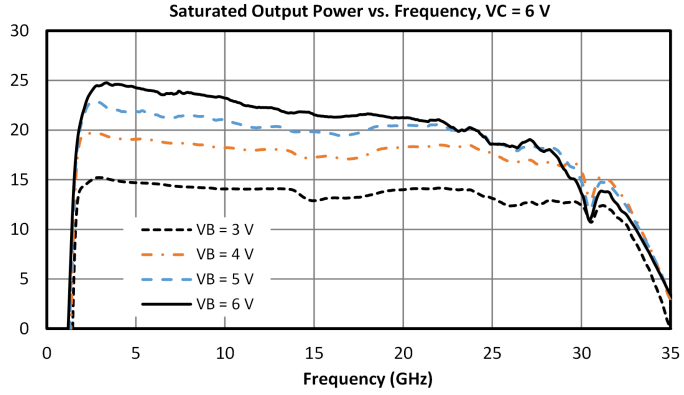
Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Small Signal Gain	5V/5V bias, -25 dBm Input Power	2	20	18	22	-	dB
Small Signal Gain	5V/5V bias, -25 dBm Input Power	20	29	-	18	-	dB
Noise Figure	5V/5V bias, -25 dBm Input Power	2	26.5	-	6	-	dB
Saturated Output Power	5V/5V bias, +6 dBm Input Power	2	20	18	21	-	dBm
Saturated Output Power	5V/5V bias, +6 dBm Input Power	20	29	-	18	-	dBm
Output IP3	5V/5V bias, -25 dBm Input Power	2	29	-	20	-	dBm
Input IP3	5V/5V bias, -25 dBm Input Power	2	29	-	-2	-	dBm
Output P1dB	5V/5V bias	2	20	-	19	-	dBm
Output P1dB	5V/5V bias	20	29	-	15	-	dBm
Input Return Loss	5V/5V bias, -25 dBm Input Power	2	20	-	14	-	dB
Input Return Loss	5V/5V bias, -25 dBm Input Power	20	29	-	7	-	dB
Output Return Loss	5V/5V bias, -25 dBm Input Power	2	20	-	16	-	dB
Output Return Loss	5V/5V bias, -25 dBm Input Power	20	29	-	11	-	dB
Reverse Isolation	5V/5V bias, -25 dBm Input Power	2	29	-	62	-	dB
Input Power for Saturation	5V/5V bias	2	29	-	4	-	dBm
Collector Current, Ic [1]	5V/4V	-	-	-	27	-	mA
Collector Current, Ic [2]	5V/5V	-	-	-	43	-	mA
Collector Current, Ic [3]	5V/6V	-	-	-	67	-	mA
Current Mirror Current, Ib	5V/4V	-	-	-	2.9	-	mA
Current Mirror Current, Ib	5V/5V	-	-	-	4	-	mA
Current Mirror Current, Ib	5V/6V	-	-	-	5.2	-	mA
Frequency	-	-	-	2	-	30	GHz
Phase Noise @ 10 kHz Offset	5V/5V bias, +9 dBm Input power, 4 GHz	2	20	-	-165	-	dBc/Hz

[1][2][3] Bias conditions for Ic and Ib tested with no RF input power. See typical performance plots for DC current vs. RF power. Bias conditions presented as VC/VB.

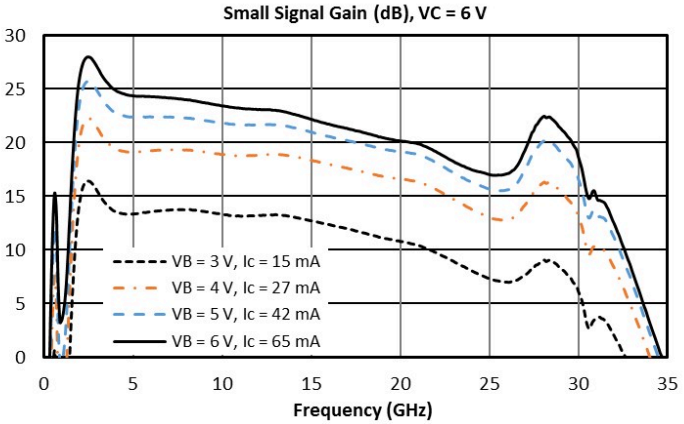
Typical Performance Plots

Surface mount performance plots are taken in the EVAL-APM-6848 connectorized fixture, and include launch, line, and connector insertion losses.

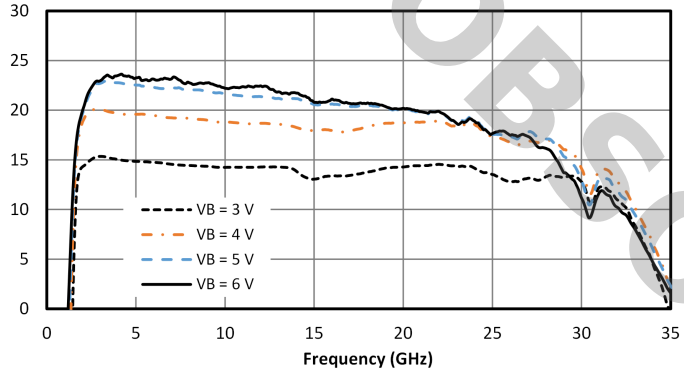
Saturated Output Power vs. Frequency, VC = 6 V



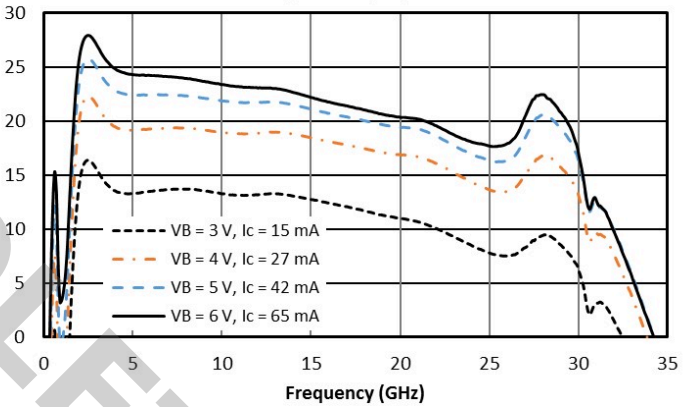
Small Signal Gain (dB), VC = 6 V



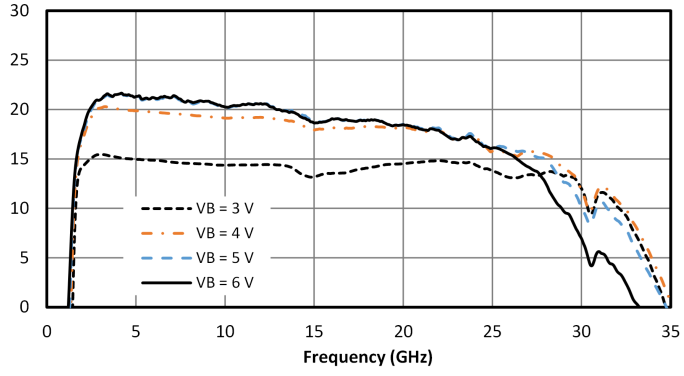
Saturated Output Power vs. Frequency, VC = 5 V



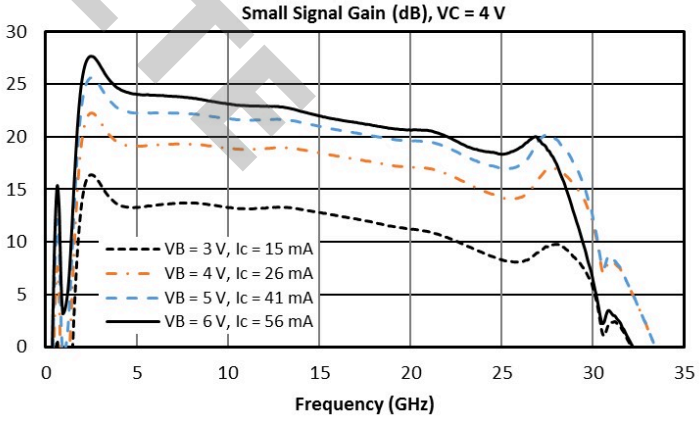
Small Signal Gain (dB), VC = 5 V



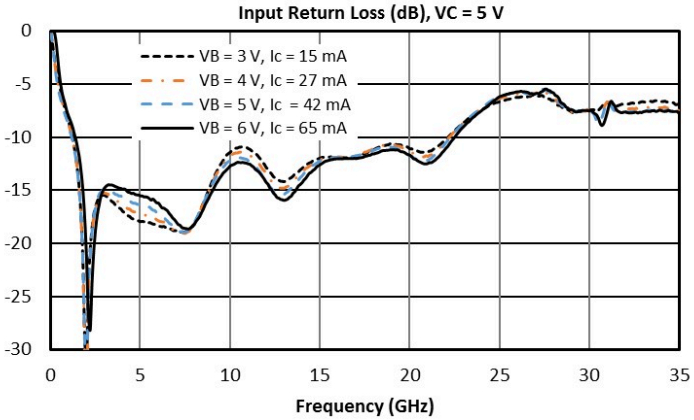
Saturated Output Power vs. Frequency, VC = 4 V



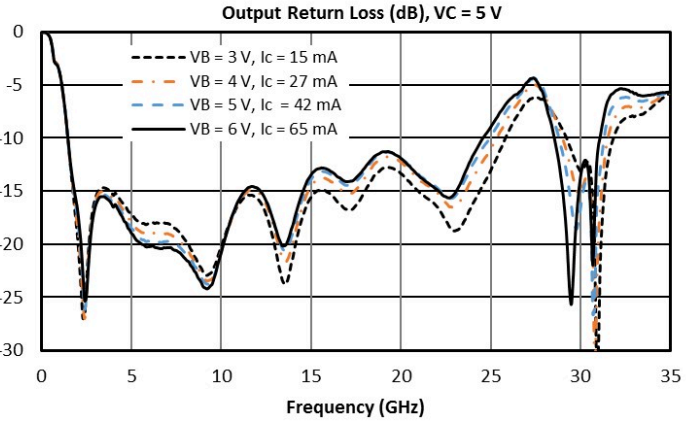
Small Signal Gain (dB), VC = 4 V



Input Return Loss (dB), VC = 5 V



Output Return Loss (dB), VC = 5 V



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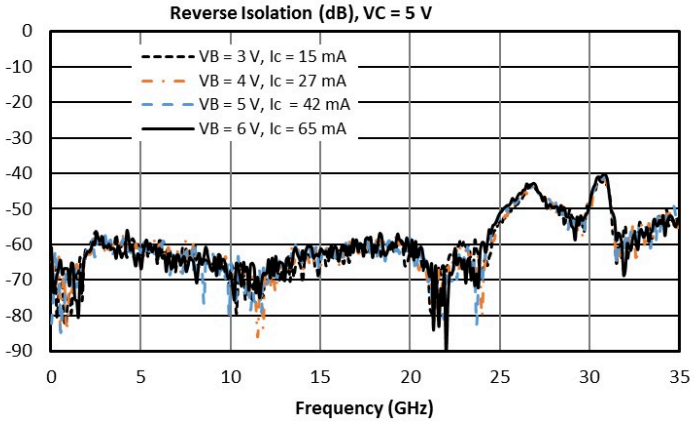
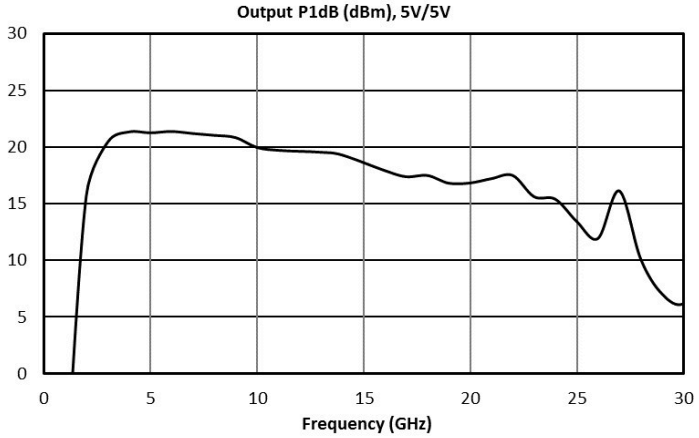
2-30 GHz Surface Mount Low Phase Noise Amplifier

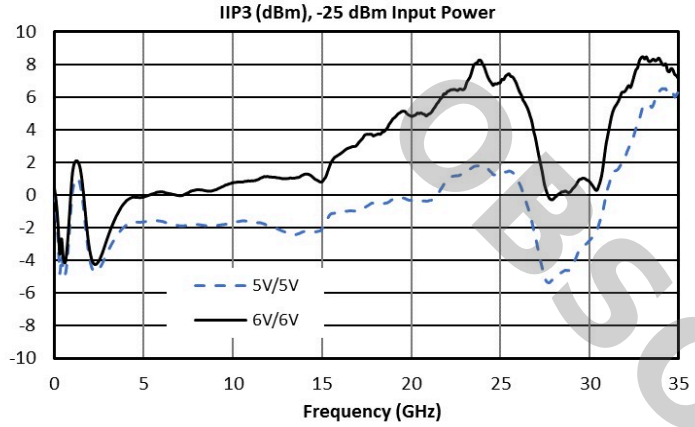
Reverse Isolation (dB), VC = 5 V



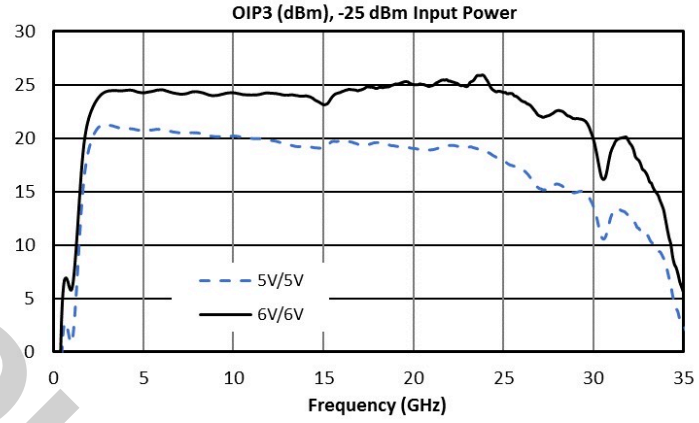
Output P1dB (dBm), 5V/5V



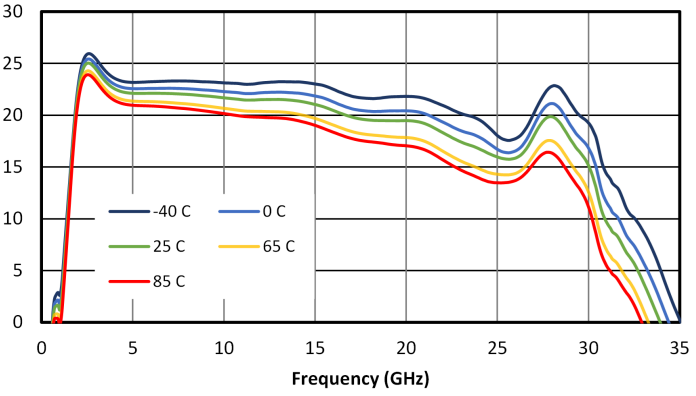
IIP3 (dBm), -25 dBm Input Power



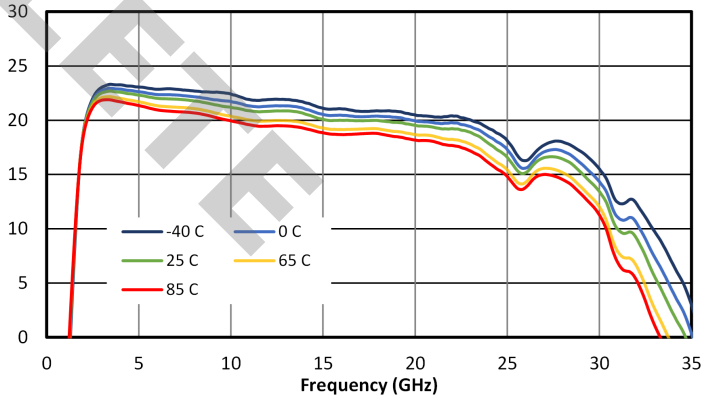
OIP3 (dBm), -25 dBm Input Power



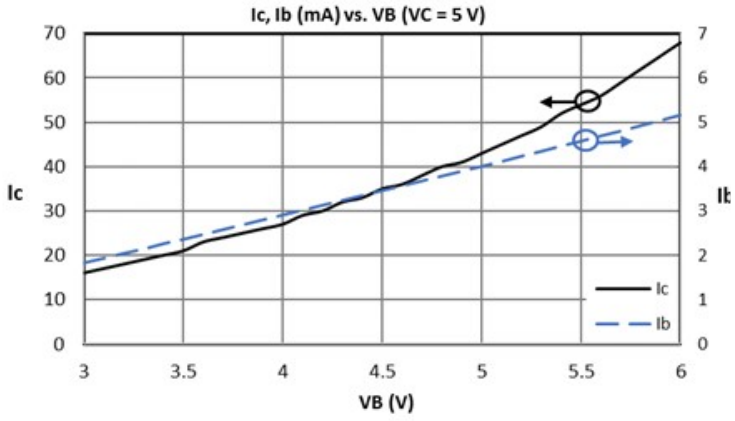
Small Signal Gain (dB) Over Temperature vs. Frequency, 5V/5V Bias



Psat (dBm) Over Temperature vs. Frequency, 5V/5V Bias



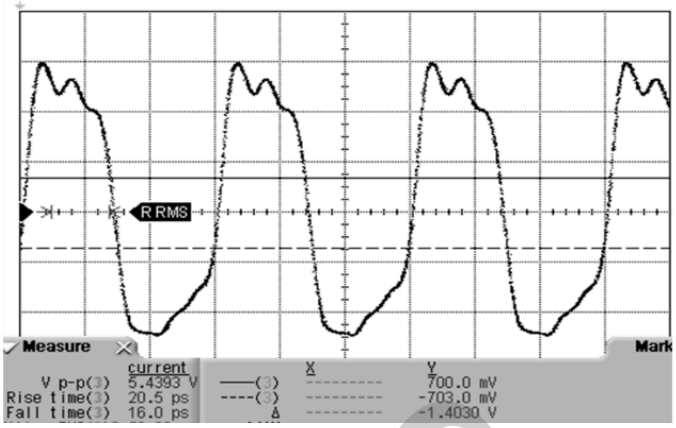
Ic, Ib (mA) vs. VB (VC = 5 V)



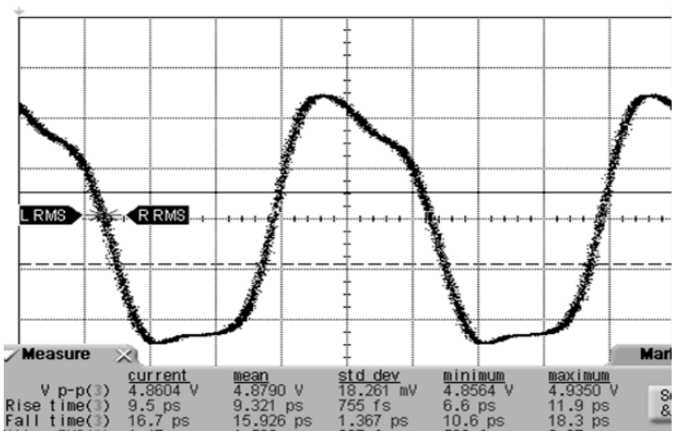
Time Domain Plots

Fast rise time is desirable for linear T3 mixer operation.

5 GHz, +5 dBm In, 5V/5V bias

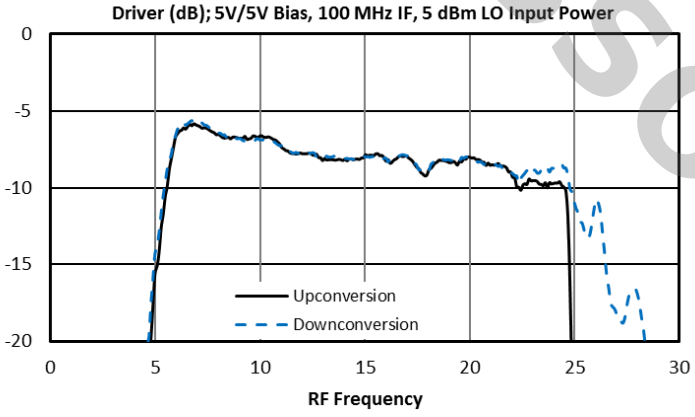


10 GHz, +5 dBm In, 5V/5V bias

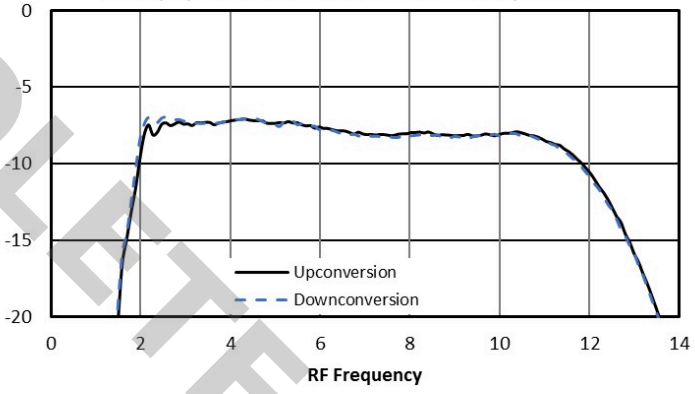


Conversion Loss of Marki Mixers Using APM-6848SM as LO Driver

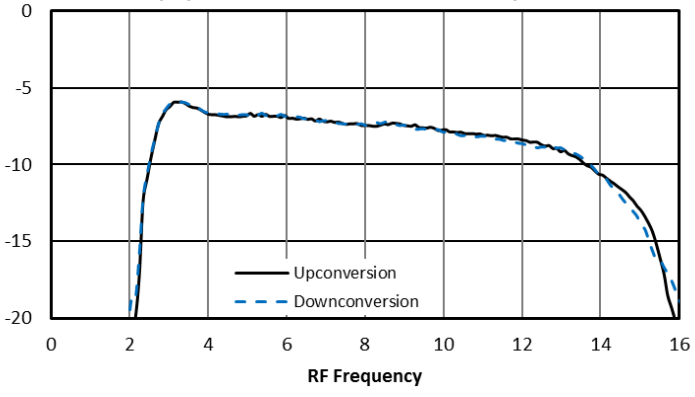
Conversion Loss of MM1-0626SSM Mixer with APM-6848SM as LO Driver (dB); 5V/5V Bias, 100 MHz IF, 5 dBm LO Input Power



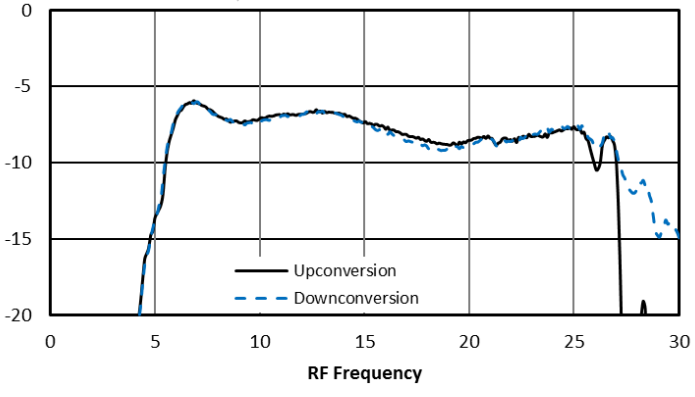
Conversion Loss of MM1-0212H Mixer with APM-6848SM as LO Driver (dB); 5V/5V Bias, 100 MHz IF, 0 dBm LO Input Power



Conversion Loss of MM1-0312H Mixer with APM-6848SM as LO Driver (dB); 5V/5V Bias, 100 MHz IF, 0 dBm LO Input Power

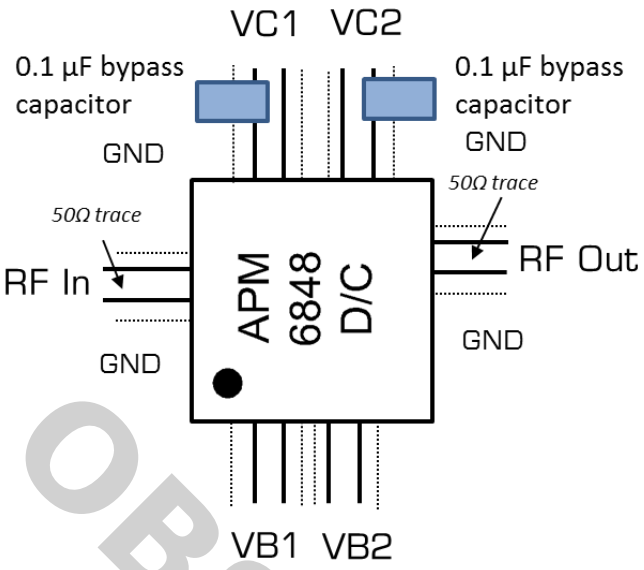


Conversion Loss of MM1-0626H Mixer with APM-6848SM as LO Driver (dB); 5V/5V Bias, 100 MHz IF, 5 dBm LO Input Power

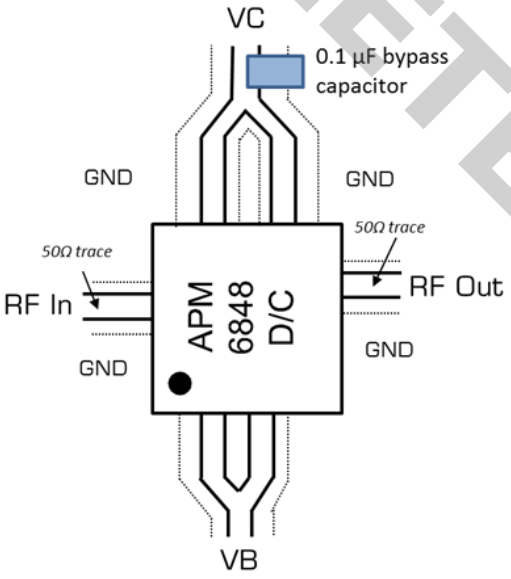


Application Information

Below are the recommended application circuits for the APM-6848SM.



RF input and output should be soldered to 50 Ω traces. Since this is a 2-stage amplifier, VC and VB lines may be biased separately at different voltages for improved efficiency (application circuit shown above), or they may be combined for convenience (below). If combined, feedback oscillations can form along the VC supply lines unless sufficient bypass capacitance to ground is used.



Gain and Power Control

The APM-6848 is a 2-stage amplifier integrated on a single IC. In the APM-6848SM package, the user has some freedom to operate the 2 amplifier stages independently for their application-specific needs. Please refer to Port Functions to see the function of each port on the APM-6848SM, and refer to the gain and Psat plots in Typical Performance Plots to see how bandwidth, saturated output power, and gain profile change for various bias conditions.

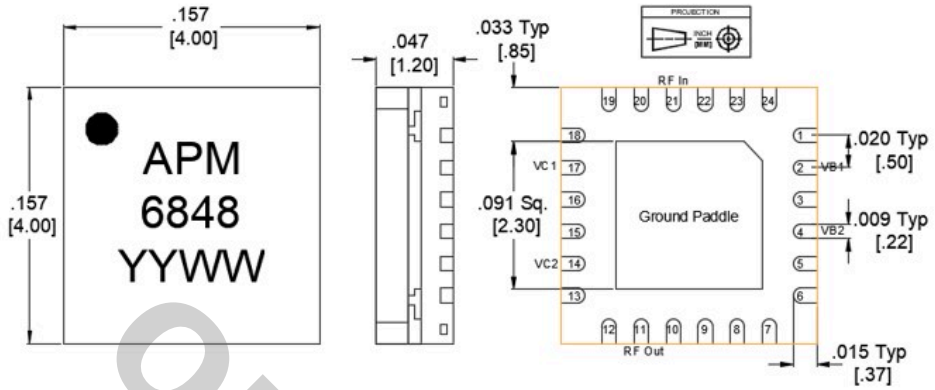
Generally, the gain of the first stage and second stage of the amplifier can be controlled by adjusting VB1 and VB2 respectively. Increasing the voltage applied to a VB pad increases the current drawn into the corresponding amplifier stage, which strongly correlates to the gain of that stage, and some difference to the output power of that stage. Increasing the voltage on a VC pad generally increases the linearity, maximum output power, and DC power consumption of the corresponding amplifier stage.

In the case where a user wants to drive the LO port of a mixer from an initial LO power of +5 dBm at 10 GHz, the user could apply 5V at all 4 DC ports and see an output power of +21.5 dBm and an overall power consumption of about 1 watt (the amplifier stages pull more DC current as the gain compresses in a high input power condition). Alternatively, the user could apply 3.5 V – 4 V to VB1 and VC1, and 6V to VB2 and VC2 and see an output power of 22.5 dBm with very little difference in the overall power consumption. For applications with a strict power budget and performance requirements, optimizing the bias conditions of the amplifier can be a useful tool for the system designer.

Mechanical Data

Outline Drawing

Download : Outline 2D Drawing | Outline 3D Drawing | Outline 3D STP



Pad #	Function
1	N/C
2	VB1
3	N/C
4	VB2
5	N/C
6	N/C
7	N/C
8	N/C
9	N/C
10	N/C
11	RF Out
12	N/C
13	N/C
14	VC2
15	N/C
16	N/C
17	VC1
18	N/C
19	N/C
20	N/C
21	RF In
22	N/C
23	N/C
24	N/C

Notes:

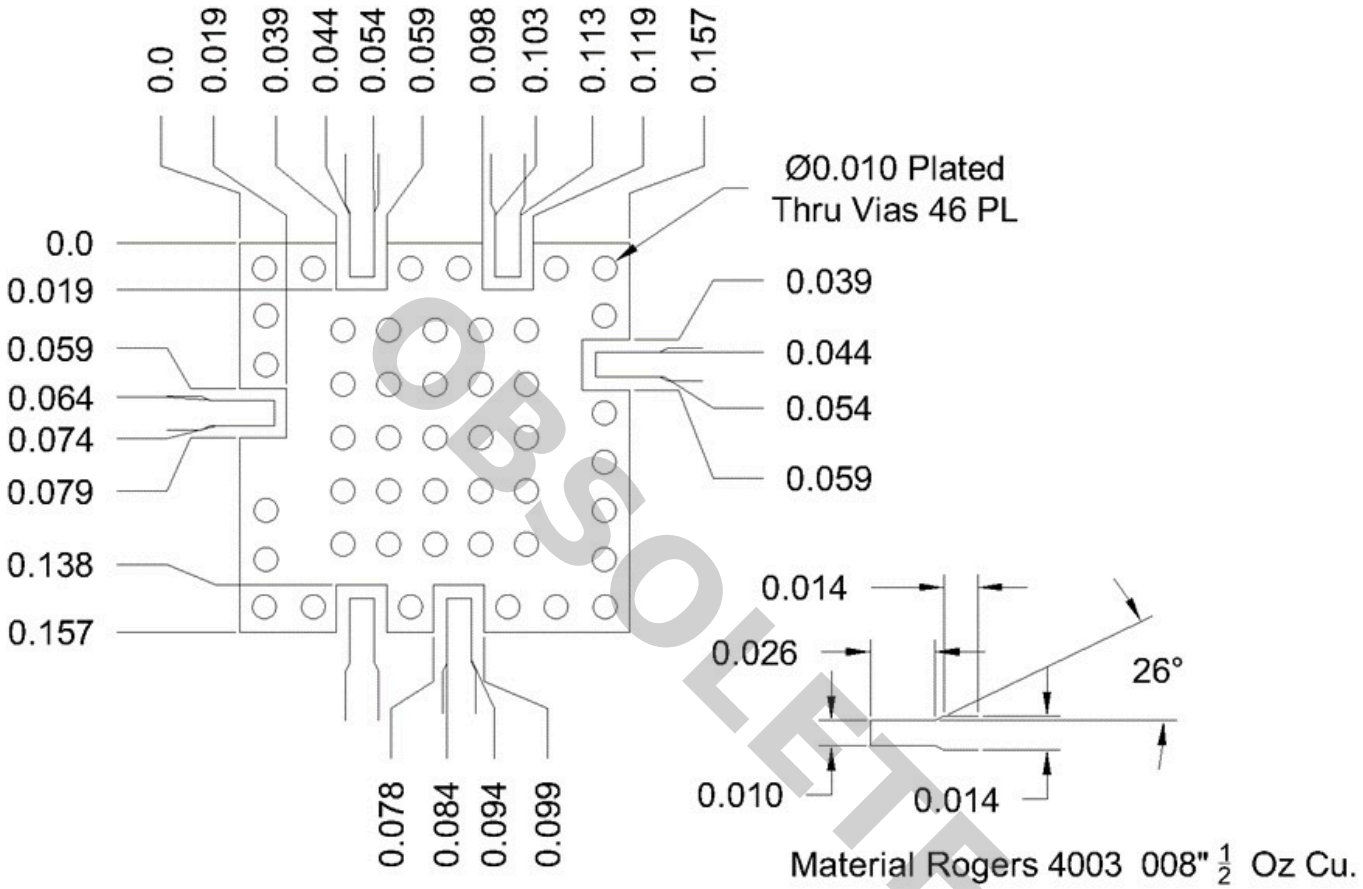
1. Substrate material is Plastic.

2. I/O Leads and Die Paddle are 0.05 µm Au over 0.02 µm Pd over 0.5 µm Ni.

3. All unconnected pins should be connected to PCB RF ground.

Footprint Image

Download : Footprint Drawing



DISCLAIMER