

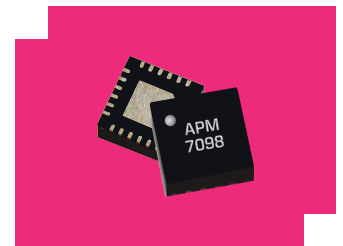
APM-7098SM

0.1-22 GHz Surface Mount Low Phase Noise Amplifier

DEVICE OVERVIEW

General Description

The APM-7098SM is a broadband low phase noise LO driver amplifier designed to provide a saturated +23 dBm output power with low DC power consumption. This amplifier uses GaAs HBT technology for low phase noise, and is optimized to provide enough power to drive the LO port of an S-diode mixer from 100 MHz to 20 GHz or of an H or L-diode mixer from 100 MHz to 30 GHz. This amplifier can be operated with a variety of bias conditions for both low and high-power applications. The APM-7098SM is packaged in a compact 4 mm QFN for surface mount integration on circuit board-based systems.



[Download s-parameters here](#)

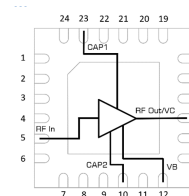
Features

- -165 dBc/Hz phase noise at 10 kHz offset frequency
- +23 dBm output power
- Low DC power consumption
- Positive-only biasing
- No sequencing required
- Unconditionally stable

Applications

- Mobile test and measurement equipment
- Radar and satellite communications
- 5G transceivers
- Driver amplifier L,H,S – diode mixers
- NLTL Driver
- Suitable as a T3 mixer driver

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
EVAL-APM-7098SM	Evaluation Board, 0.1-22 GHz Surface Mount Low Phase Noise Amplifier	EVAL	REACH RoHS	Released	EAR99
APM-7098SM	0.1-22 GHz Surface Mount Low Phase Noise Amplifier	QFN	REACH RoHS	Released	EAR99

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Revision History

Revision Code	Revision Date	Comment
-	2020-09-01	Datasheet Initial Release
A	2021-01-01	Updated Thermal Resistance and Max Input Power Spec, updated Min Spec table
B	2023-03-01	Updated Application Circuit

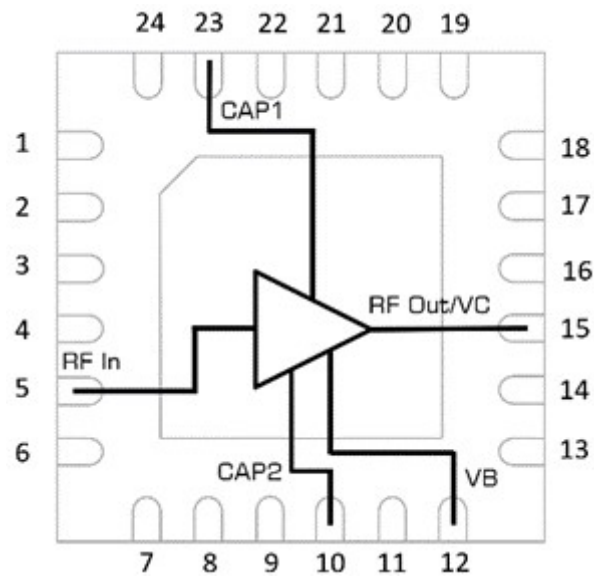
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Port Configuration and Functions

Port Diagram

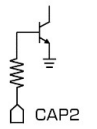
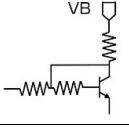
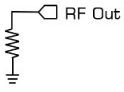
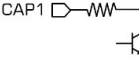
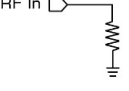
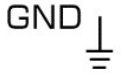
A port diagram of the APM-7098SM is shown below.



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Port Functions

Port	Function	Description	Equivalent Circuit for Package
10	Off-Chip Cap Port 2	Port 10 allows the user to attach additional off chip bypass capacitance to provide adequate low frequency AC grounding termination to the input matching network. The value should be at least 100nF.	
12	Current Mirror Bias Port	Port 12 is the DC voltage bias pad for the current mirror that controls the collector current supplied to the amplifier. See section 3.6 for performance at different bias conditions	
15	RF Output and Collector Supply Port	This is the amplifier's RF Output and positive VC supply voltage pin. It is RF matched to 50 Ω and is DC coupled. Must have less than 7:1 VSWR when operating.	
23	Off-Chip Cap Port 1	Port 23 allows the user to attach additional off chip bypass capacitance to provide adequate low frequency AC grounding termination to the input matching network. The value should be at least 100nF.	
5	RF Input	This is the RF input port of the device, and is RF matched to 50 Ω . This port is DC-coupled, and requires a blocking capacitor.	
GND	Ground	IC backside must be connected to a DC/RF ground with high thermal and electrical conductivity.	

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Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may become inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Unit
Bias (Current Mirror) Voltage (VB)	9	V
Maximum Operating Temperature	85	°C
Maximum Storage Temperature	150	°C
Max Junction Temperature for MTTF > 1E6 hours	125	°C
Max Power Dissipation for MTTF of 1E6 hours at 85°C Baseplate Temperature	630	mW
Minimum Operating Temperature	-40	°C
Minimum Storage Temperature	-65	°C
Output Load VSWR	7	-
Power Supply (Collector) Current (Ic)	150	mA
Power Supply (Collector) Voltage (VC)	9	V
RF Input Power	16	dBm
θJC, Junction to Ambient Thermal Resistance	63	°C/W

Package Information

Parameter	Details	Rating
Dimensions	-	4x4 mm

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications. Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

Parameter	Min	Nominal	Max	Unit
Input Power for Saturation	7	10	16	dBm
Positive DC Voltage (VC)	5	8	9	V
Quiescent DC Current (Ic)	26	44	65	mA
Ambient Temperature	-40	25	85	°C
Positive DC Current Mirror Voltage (VB)	5	7	9	V
DC Current with RF Input (Ic) ¹	-	-	150	mA

^[1] Maximum recommended operating current conditions without RF input applied. Please see typical performance plots on page 9 for relationship between RF input power and DC current draw.

Sequencing Requirements

There is no sequencing required to power up or power down the amplifier. Amplifier must have an output load connected when operating.

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Electrical Specifications

The electrical specifications apply at TA=+25 °C in a 50 Ω system. QFNs are 100% RF tested.

Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Small Signal Gain	8 V/7 V bias, -25 dBm Input Power	0.1	15	11	15	-	dB
Noise Figure	8 V/7 V bias, -25 dBm Input Power	0.1	22	-	4.8	-	dB
Saturated Output Power ¹	8 V/7 V bias	0.015	22	-	12	-	dBm
Saturated Output Power ²	8 V/7 V bias	0.1	15	17	23	-	dBm
Output IP3	8 V/7 V bias, -20 dBm Input Power	0.1	22	-	19	-	dBm
Input IP3	8 V/7 V bias, -20 dBm Input Power	0.1	22	-	8	-	dBm
Output P1dB	8 V/7 V bias	0.1	22	-	19	-	dBm
Input Return Loss	8 V/7 V bias, -25 dBm Input Power	0.1	22	-	11	-	dB
Output Return Loss	8 V/7 V bias, -25 dBm Input Power	0.1	22	-	10	-	dB
Reverse Isolation	8 V/7 V bias, -25 dBm Input Power	0.1	22	-	38	-	dB
Input Power for Saturation	8 V/7 V bias	0.1	22	-	10	-	dBm
Collector Current, Ic ³	8 V/6 V	-	-	-	33	-	mA
Collector Current, Ic	8 V/7 V	-	-	-	42	-	mA
Current Mirror Current, Ib	8 V/6 V	-	-	-	3	-	mA
Current Mirror Current, Ib	8 V/7 V	-	-	-	4	-	mA
Phase Noise @ 10 kHz Offset	8 V/7 V bias, +10 dBm Input power	1	-	-	-165	-	dBc/Hz

^{[1][2]} Saturated output power specification defined using the EVAL-APM-7098SM P7dB compression curve shown in section 3.6

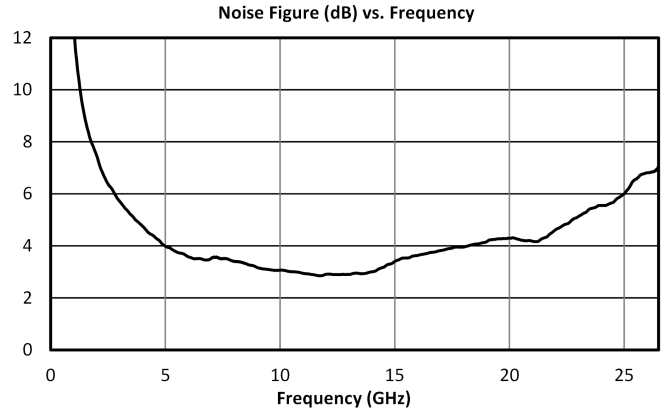
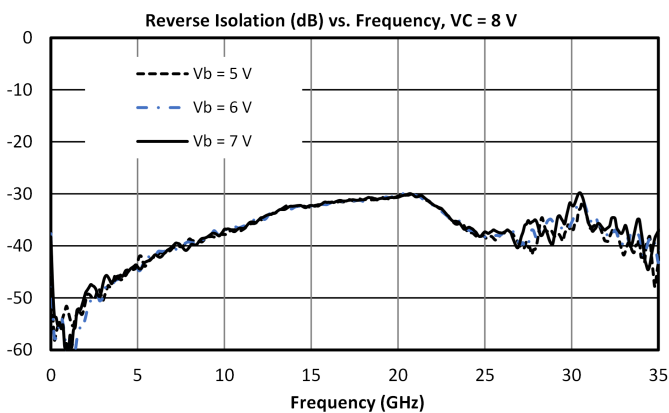
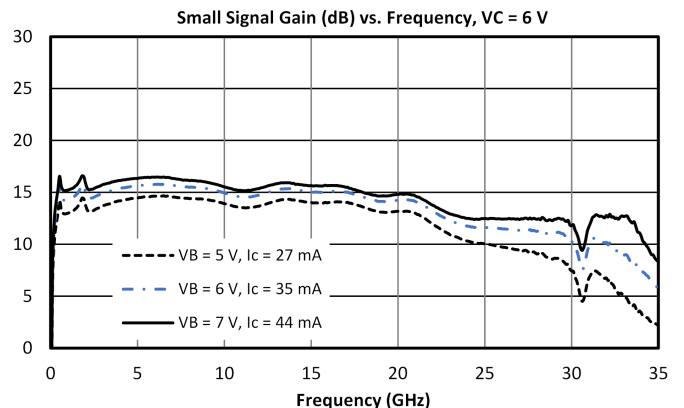
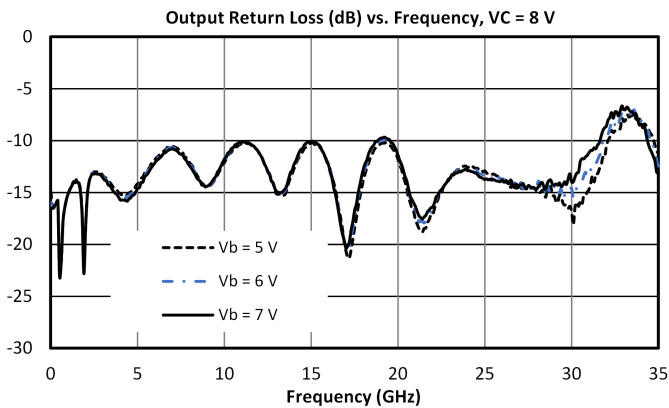
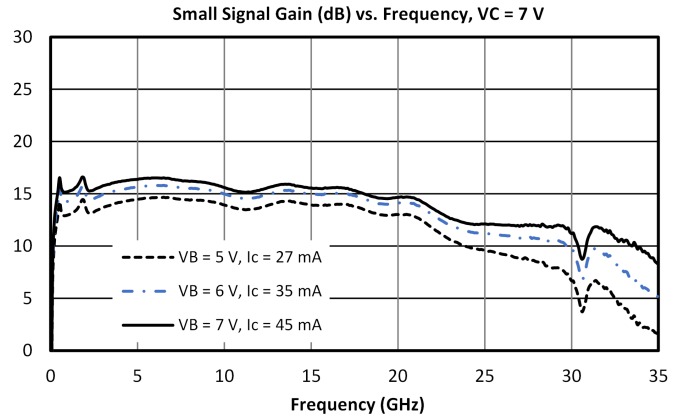
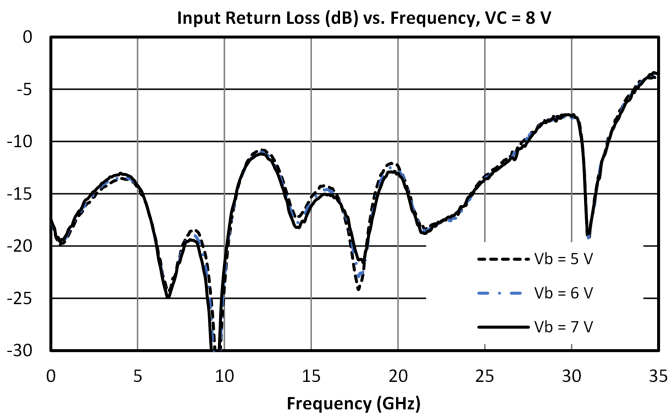
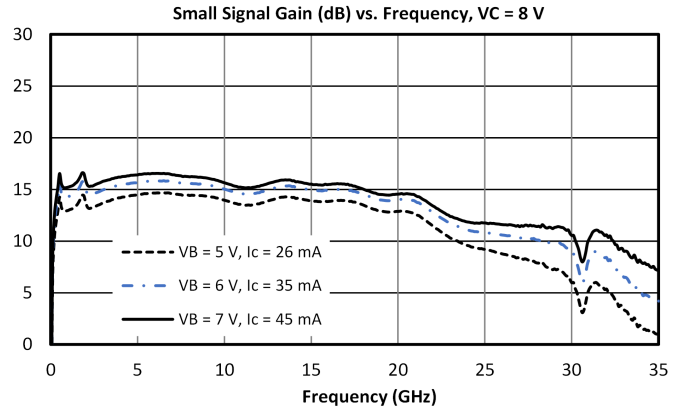
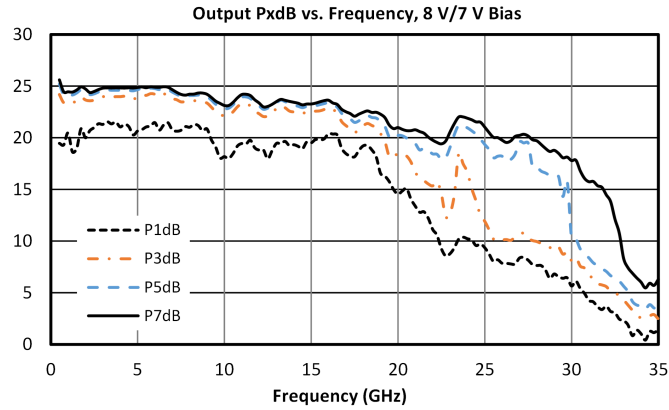
^[3] Bias conditions for Ic and Ib tested with no RF input power. See section 3.6 for DC current vs. RF power. Bias conditions presented as VC/VB.

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Typical Performance Plots

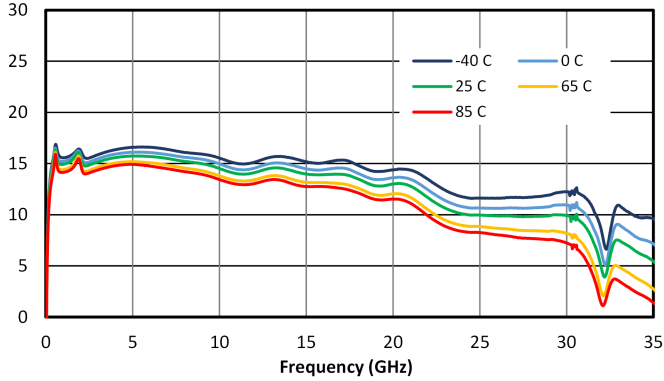
APM-7098SM measurements taken in EVAL-APM-7098SM evaluation board.



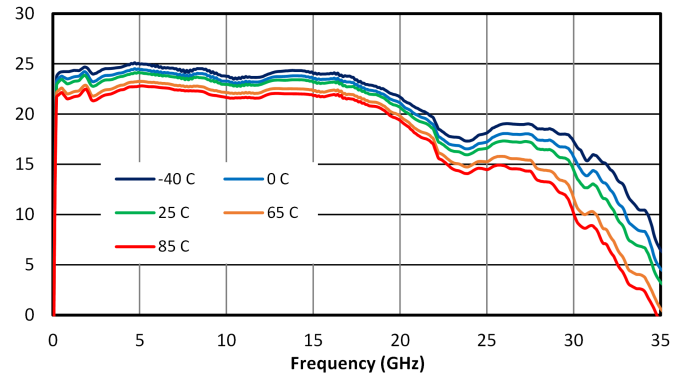
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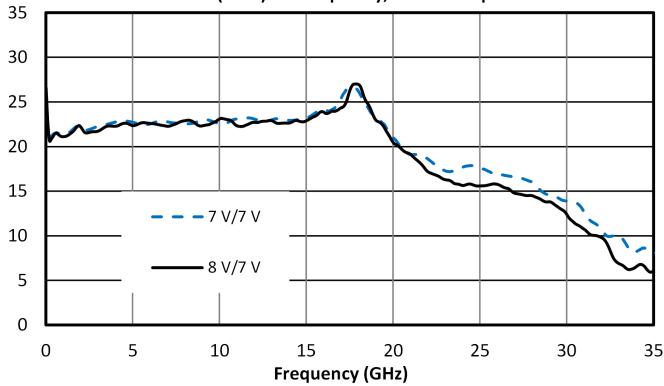
Small Signal Gain (dB) Over Temperature vs. Frequency, 8 V/7 V Bias



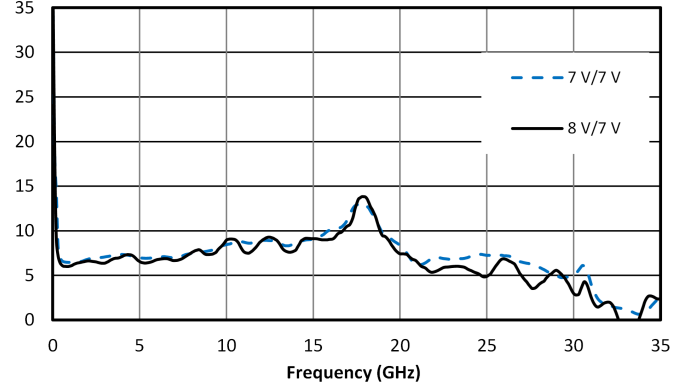
Saturated Output Power over Temperature vs. Frequency, 8 V/7 V



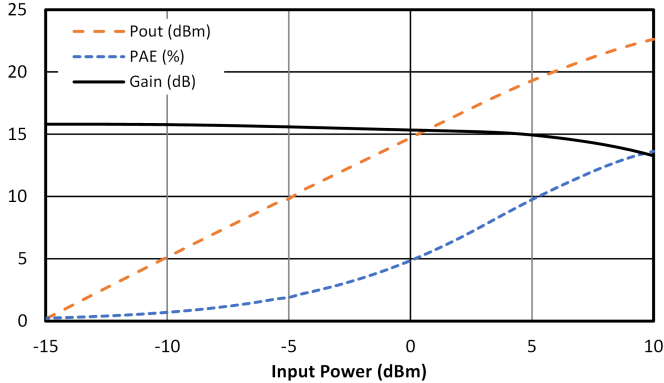
OIP3 (dBm) vs. Frequency, -18 dBm Input Power



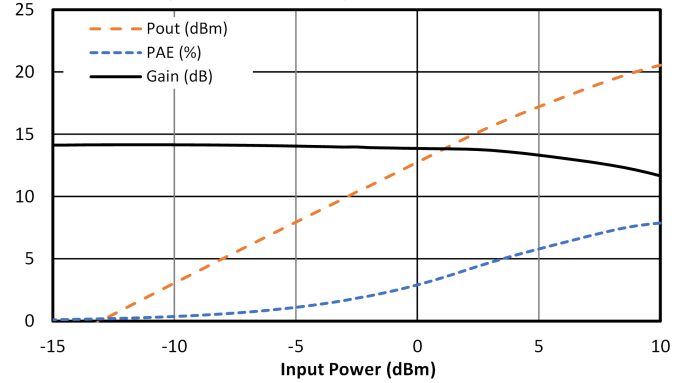
IIP3 (dBm) vs. Frequency, -18 dBm Input Power



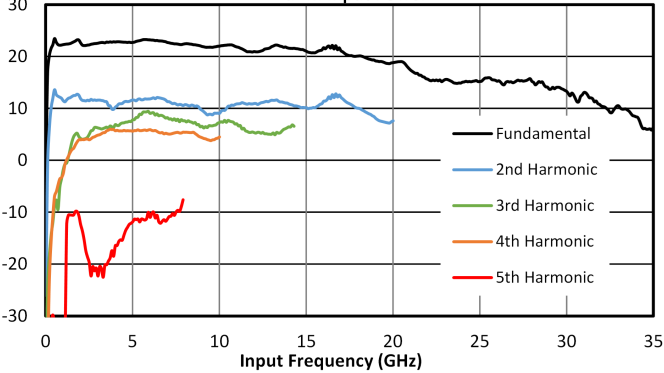
Gain, Output Power, PAE vs. Input Power, 8 V/7 V, F = 5 GHz



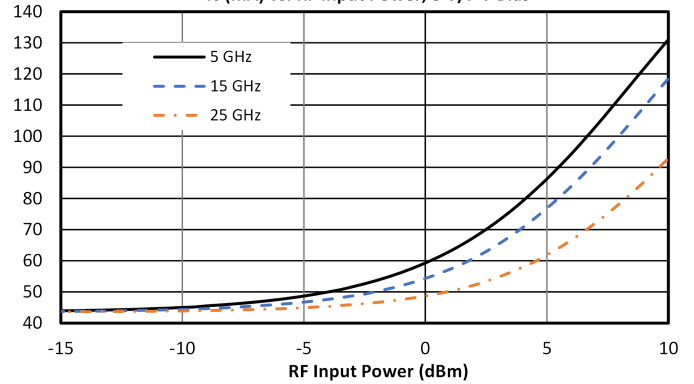
Gain, Output Power, PAE vs. Input Power, 8 V/7 V, F = 15 GHz



Harmonic Response (dBm) vs. Input Freq. 8 V/7 V Bias, +11 dBm Input Power

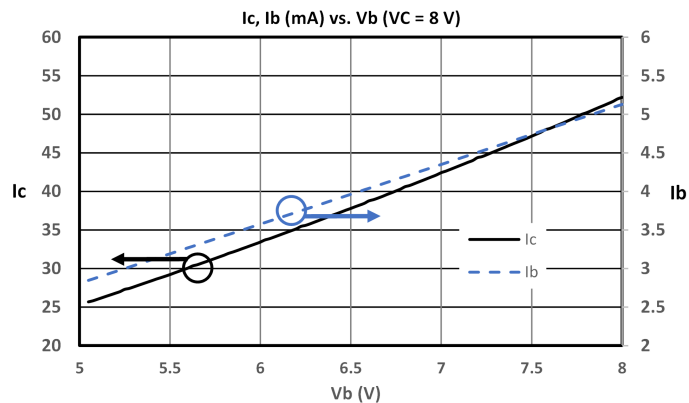


Ic (mA) vs. RF Input Power, 8 V/7 V Bias



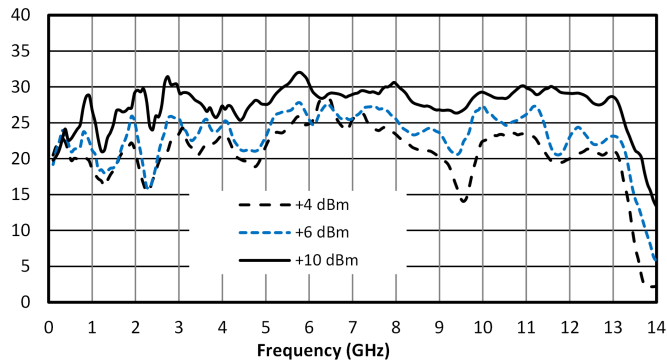
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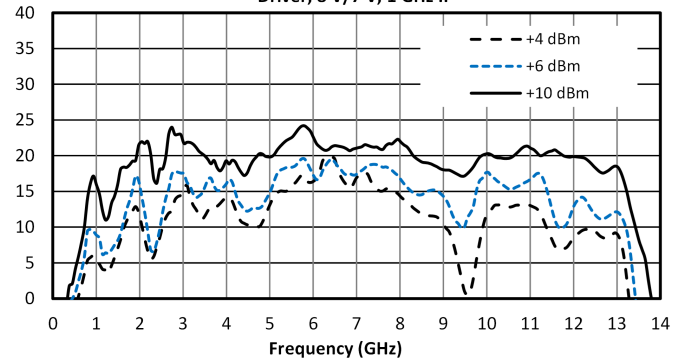


Typical Performance Plots of Marki MT3H-0113H Driven With APM-7098SM

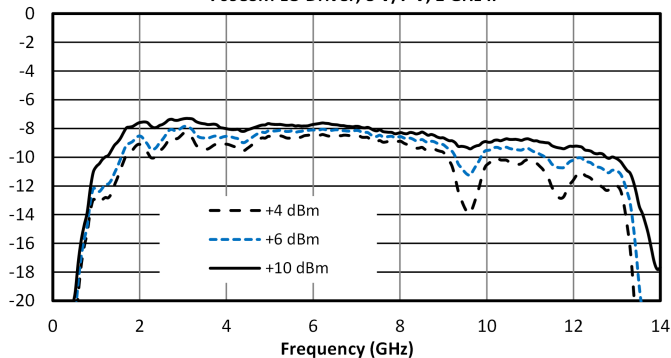
MT3H-0113H Config. A, IIP3 (dBm) vs. Frequency, APM-7098SM LO Driver, 8 V/7 V, 1 GHz IF



MT3H-0113H Config. A, OIP3 (dBm) vs. Frequency, APM-7098SM LO Driver, 8 V/7 V, 1 GHz IF



MT3H-0113H Config. A, Conversion Loss (dB) vs. Frequency, APM-7098SM LO Driver, 8 V/7 V, 1 GHz IF



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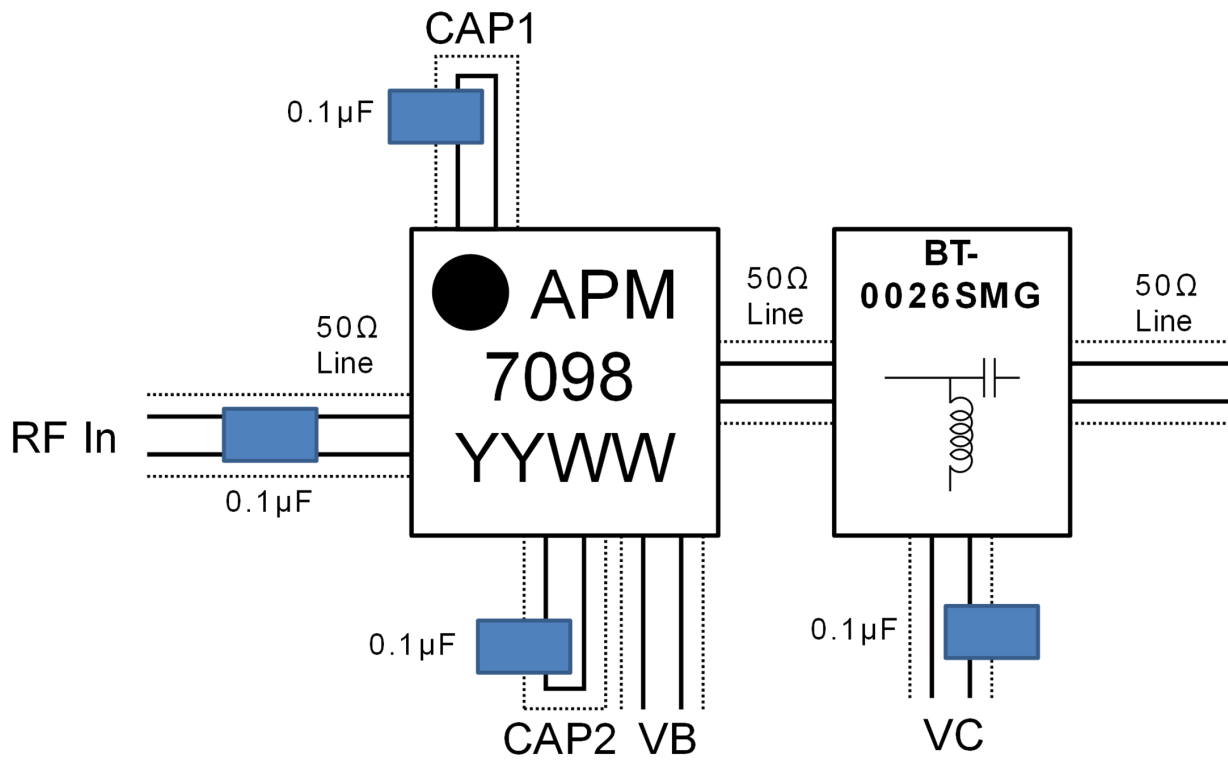
Application Information

Below is the recommended application circuit for the APM-7098SM.

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Application Circuit



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Application Circuit Description

RF input and output should be soldered to 50 Ω traces. A suggested capacitor for the bypass and blocking capacitors would be 0402 0.1 μ F 16 V surface mount capacitors.

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Bypass Capacitors

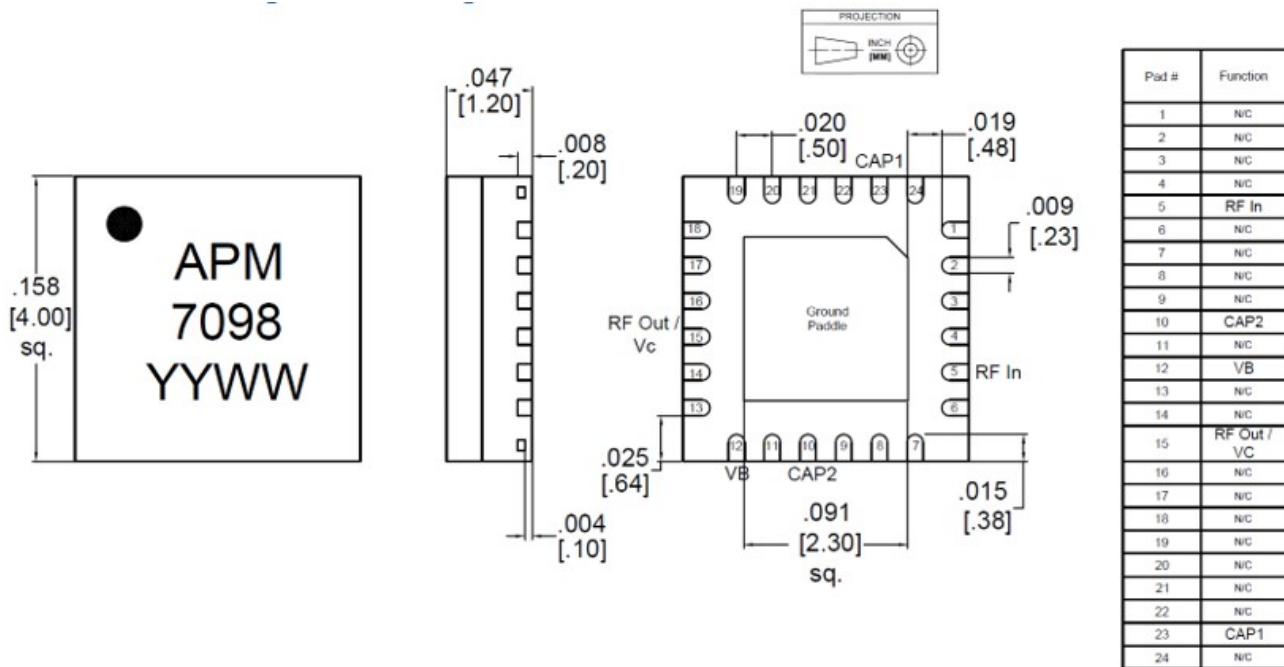
The bypass capacitors on ports CAP1 and CAP2 provide AC ground to the internal circuits on the chip. These should not be DC coupled to prevent disruption of the internal biasing circuits, or outright damage to the chip. The value of these be at least 100nF to provide adequate AC grounding. An additional 100 nF bypass capacitor in series with a 20 Ω resistor should be added to the VC line to stabilize the amplifier and prevent power supply feedback to other parts on the board.

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Mechanical Data

Outline Drawing



Notes:

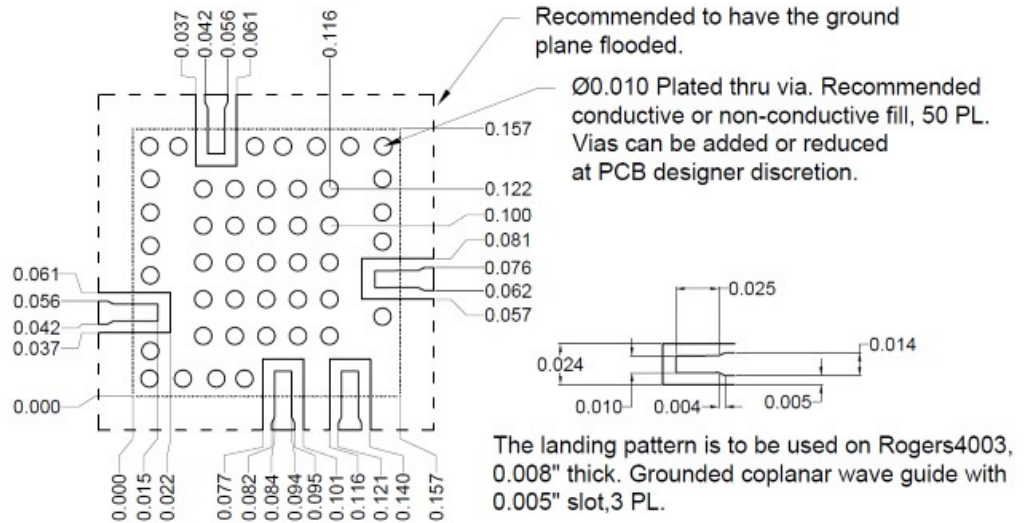
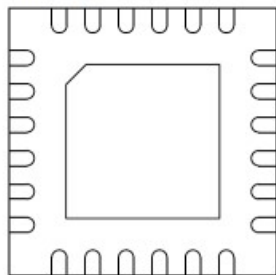
1. Substrate Material is Plastic.
2. I/O Leads and Die Paddle are 0.05 microns Au over 0.02 microns Pd over 0.5 microns Ni.
3. All unconnected pins should be connected to PCB RF ground.

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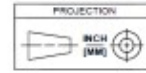
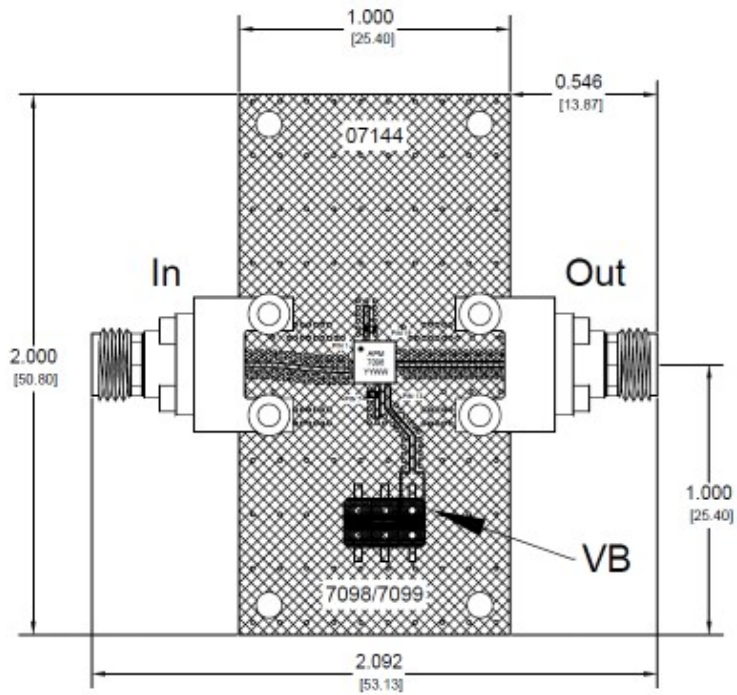
Footprint Image

QFN 4mm Sample Drawing
X-Ray view

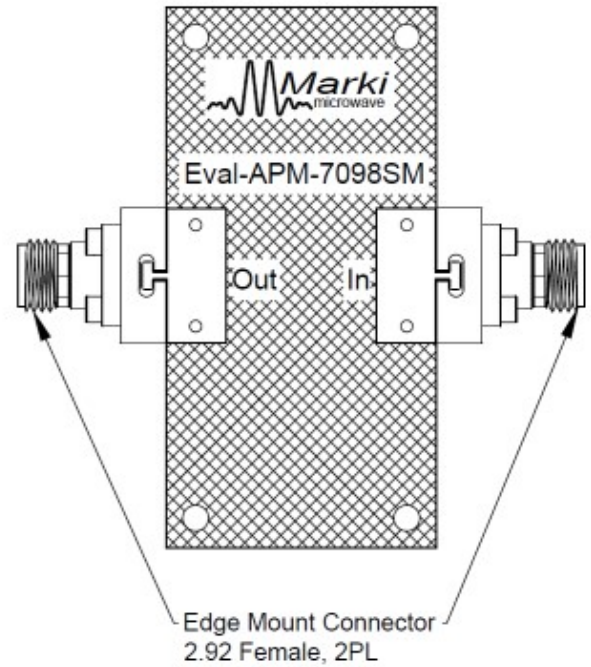


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Backside Label



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