

HLM-70ACH

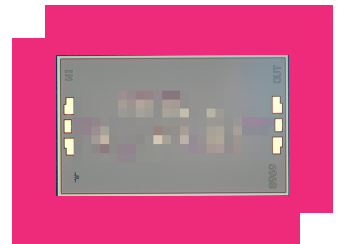
DC - 70GHz High Frequency Limiter

DEVICE OVERVIEW

General Description

The HLM-70ACH is a high-power GaAs Schottky diode signal limiter. It offers low insertion loss and low return loss from DC through V band. Its high power handling makes it ideal for protecting sensitive components and for applications requiring high linearity.

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Features

- DC to 70 GHz limiter
- 1W CW Power Handling @ 2 GHz
- 9dBm Flat Leakage @ 50 GHz CW

Applications

N/A

Functional Block

Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
HLM-70ACH	DC - 70GHz High Frequency Limiter	CH	RoHS REACH	Released	EAR99

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Revision History

Revision Code	Revision Date	Comment
-	2024-04-03	Datasheet Initial Release

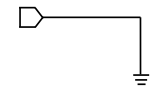
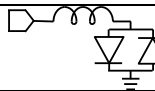
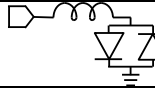
Port Configuration and Functions

Port Diagram

A top-down view of the HLM-70ACH's CH package outline drawing is shown below. The HLM-70ACH has the input and output ports given in Port Functions.



Port Functions

Port	Function	Description	Equivalent Circuit for Package
GND	Ground	CH package ground path is provided through the substrate and ground bond pads.	
IN	Input	IN is the RF input port and is diode connected for the CH package.	
OUT	Output	OUT is the RF output port and is diode connected for the CH package.	

Specifications

Absolute Maximum Ratings

Parameter	Maximum Rating	Unit
Maximum Operating Temperature	100	°C
Maximum Storage Temperature	125	°C
Minimum Operating Temperature	-55	°C
Minimum Storage Temperature	-65	dB
RF Power Handling, CW @ 2GHz, 25°C	1	W

RF Power Handling represents an instantaneous, catastrophic limit and it isn't derated for frequency, temperature, pulse conditions, or unit to unit variation.

Package Information

Parameter	Details	Rating
Dimensions	-	2.28x1.38mm

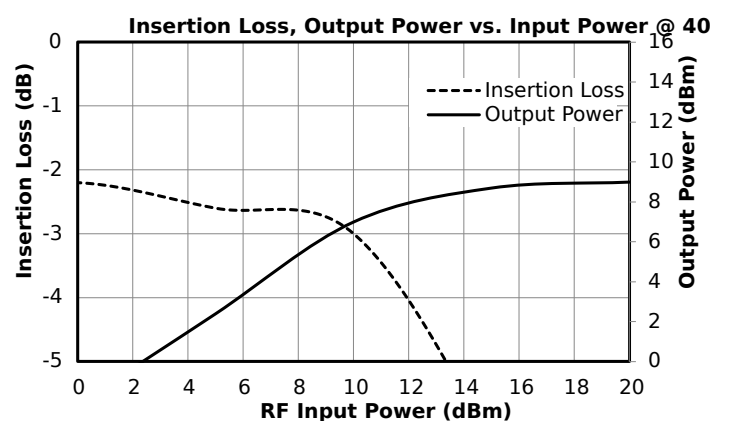
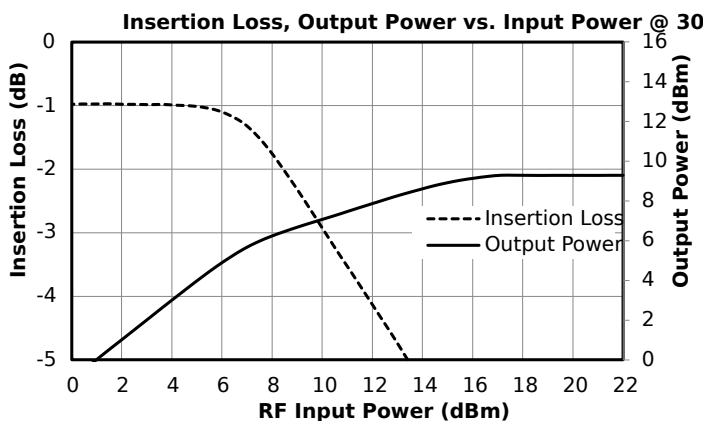
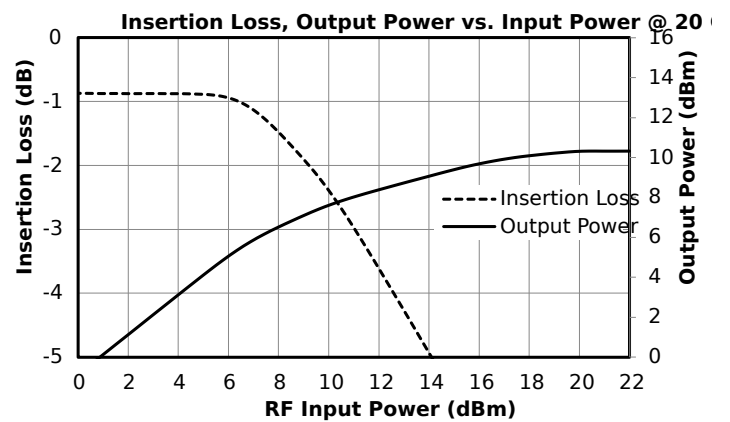
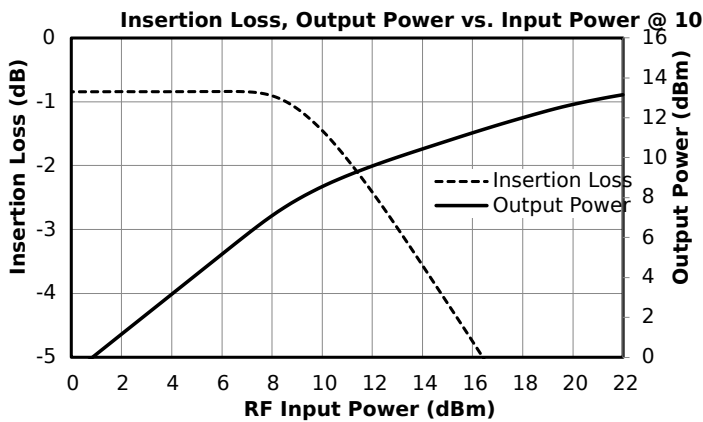
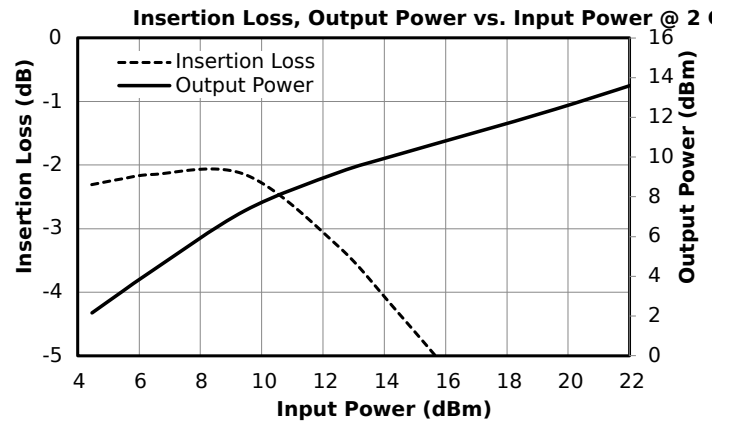
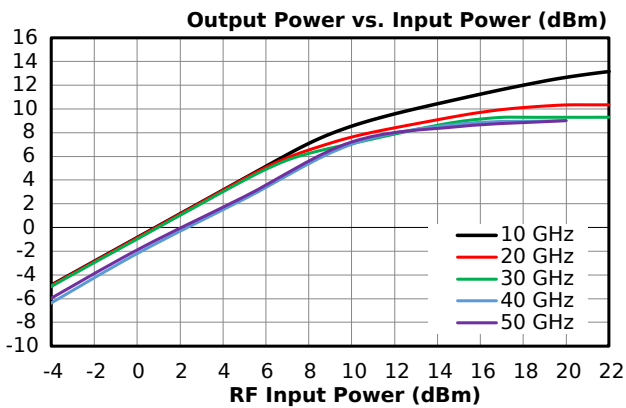
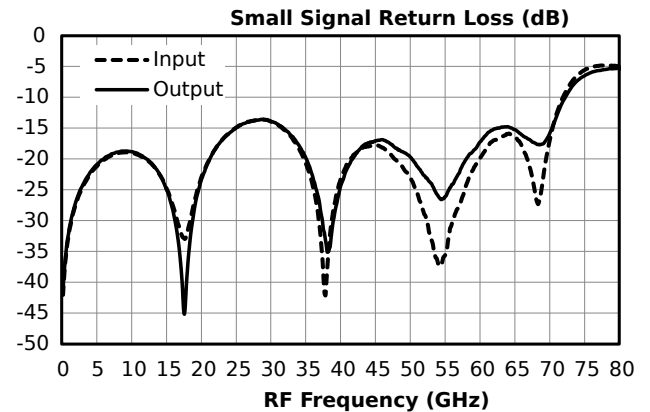
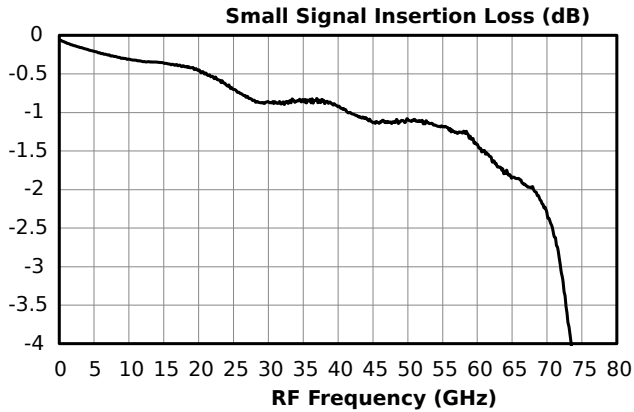
Electrical Specifications

The electrical specifications apply at TA=+25°C in a 50Ω system. Data is measured with 3 wirebonds. Min and Max limits are guaranteed at TA=+25°C. All bare die are 100% visually inspected and RF performance is guaranteed by sample testing.

Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Insertion Loss	-	0	70	-	0.8	2.7	dB
Return Loss	-	0	70	-	19	-	dB
Flat Leakage	-	20	20	-	10.5	-	dBm
Flat Leakage	-	30	30	-	9.5	-	dBm
Flat Leakage	-	40	40	-	9	-	dBm
Flat Leakage	-	50	50	-	9	-	dBm

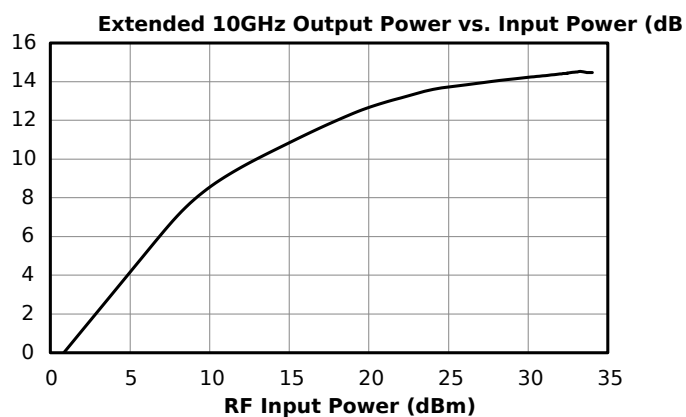
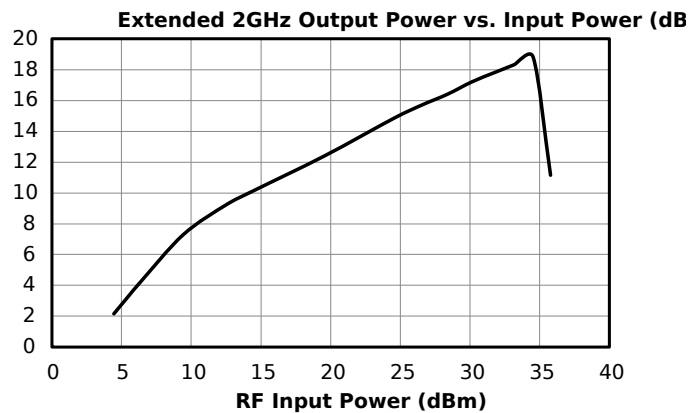
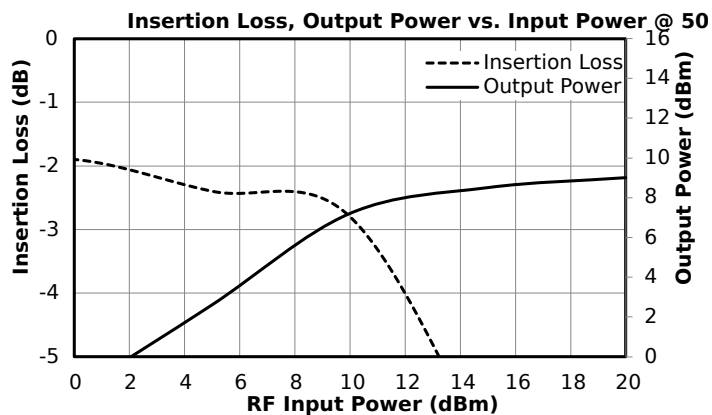
Data is measured with 3 wirebonds.

Typical Performance Plots



HLM-70ACH

DC - 70GHz High Frequency Limiter



Die Mounting Recommendations

Mounting and Bonding Recommendations

Marki MMICs should be attached directly to a ground plane with conductive epoxy. The ground plane electrical impedance should be as low as practically possible. This will prevent resonances and permit the best possible electrical performance. Datasheet performance is only guaranteed in an environment with a low electrical impedance ground.

Mounting- To epoxy the chip, apply a minimum amount of conductive epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip. Cure epoxy according to manufacturer instructions.

Wire Bonding - Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31 mm (12 mils).

Circuit Considerations - 50 Ω transmission lines should be used for all high frequency connections in and out of the chip. Wirebonds should be kept as short as possible, with multiple wirebonds recommended for higher frequency connections to reduce parasitic inductance. In circumstances where the chip more than .001" thinner than the substrate, a heat spreading spacer tab is optional to further reduce bondwire length and parasitic inductance.

Handling Precautions

General Handling

Chips should be handled with care using tweezers or a vacuum collet. Users should take precautions to protect chips from direct human contact that can deposit contaminants, like perspiration and skin oils on any of the chip's surfaces.

Static Sensitivity

GaAs MMIC devices are sensitive to ESD and should be handled, assembled, tested, and transported only in static protected environments.

Cleaning and Storage: Do not attempt to clean the chip with a liquid cleaning system or expose the bare chips to liquid. Once the ESD sensitive bags the chips are stored in are opened, chips should be stored in a dry nitrogen atmosphere.

Bonding Diagram

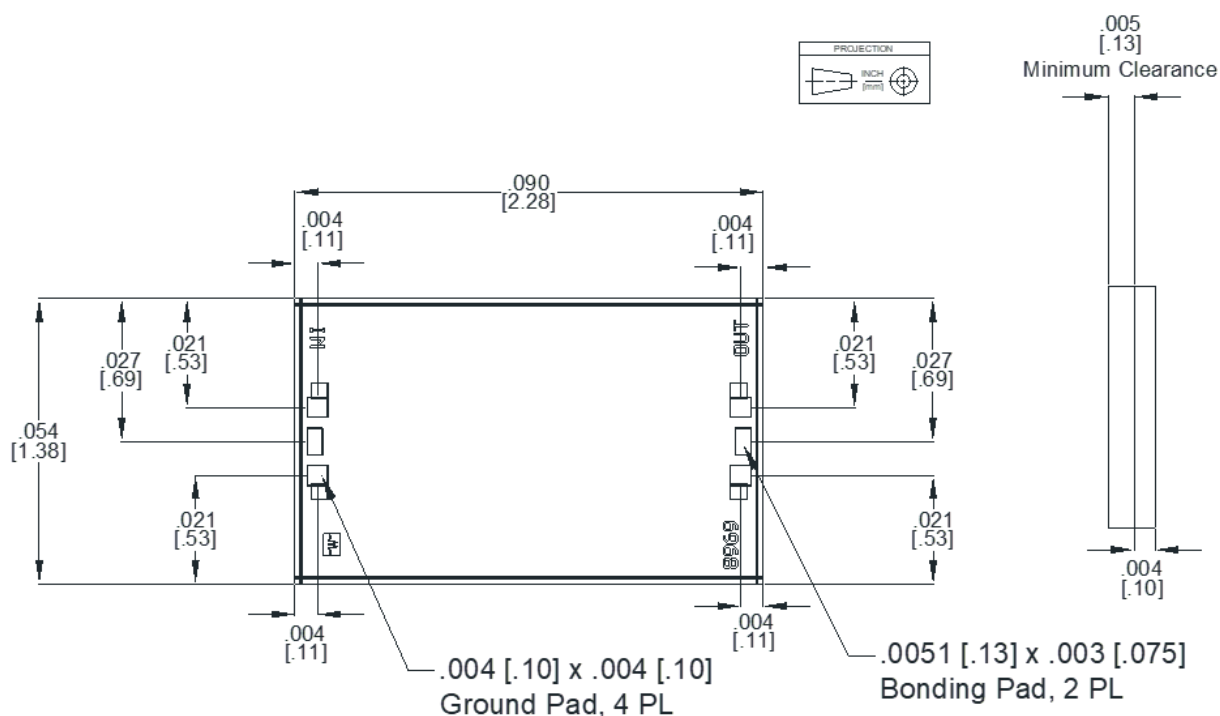


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DC - 70GHz High Frequency Limiter

Mechanical Data

Outline Drawing



Notes:

1. CH substrate is .004 in Thick GaAs.
2. I/O trace finish is 4.2 microns Au. Ground plane finish is 5 microns Au.
3. Tolerance for X, Y dimensions is ± 0.002 in.
Tolerance for Z dimension is ± 0.0005 in.
Tolerance for pad location is ± 0.0001 in.

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