

HLM-8011CH

Low Flat Leakage DC-30GHz Limiter

DEVICE OVERVIEW

General Description

The HLM-8011 is a high-power GaAs Schottky diode signal limiter featuring high IP3 and high power handling. It offers low insertion loss and low return loss from DC through Ka band and has a typical 1dB compression point of +9dBm. Its low flat leakage makes it ideal for protecting sensitive components and for applications requiring high linearity. It is available as a wire bondable die and as a connectorized module.



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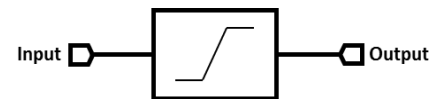
Features

- DC to 30 GHz limiter
- 4.5W Peak Power (pulsed), 30dBm CW
- +7dBm Flat Leakage @ 1W CW
- Typical P1dB of +9dBm

Applications

N/A

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Packing Size	Green Status	Product Lifecycle	Export Classification
HLM-8011CH	Low Flat Leakage DC-30GHz Limiter	CH	-		Released	EAR99
<u>HLM-8011U</u>	Low Flat Leakage DC-30GHz Limiter	U	-		Released	EAR99

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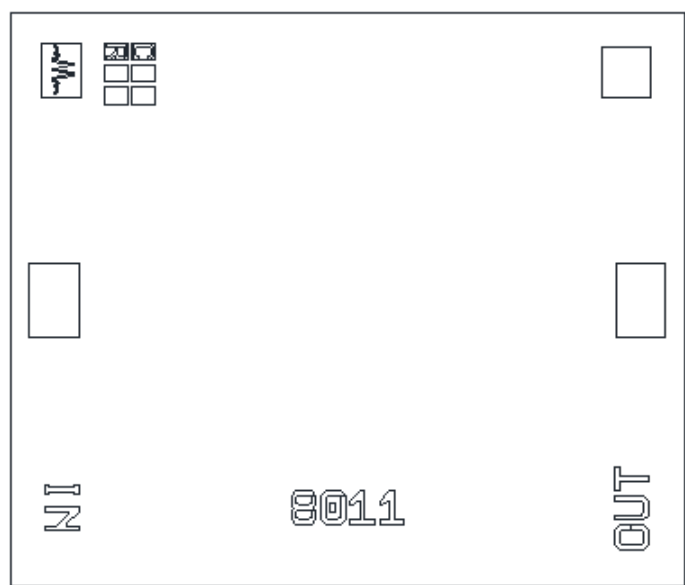
Revision History

Revision Code	Revision Date	Comment
-	2023-03-01	Initial Release

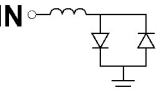
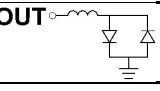
Port Configuration and Functions

Port Diagram

A top-down view of the HLM-8011’s CH package outline drawing is shown below. The HLM-8011 has the input and output ports given in Port Functions.



Port Functions

Port	Function	Description	Equivalent Circuit for Package
GND	Ground	CH package ground path is provided through the substrate and ground bond pads.	GND 
IN	Input	The input port is diode connected for the CH package.	IN 
OUT	Output	The output port is diode connected for the CH package.	OUT 

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Unit
Average Power Handling at Input Port	30	dBm
Maximum Operating Temperature	100	°C
Maximum Storage Temperature	125	°C
Minimum Operating Temperature	-55	°C
Minimum Storage Temperature	-65	°C
Peak Power Handling at Input Port	4.5	W
RF Power Handling , Average	1	W
RF Power Handling , Peak	4.5	W

Package Information

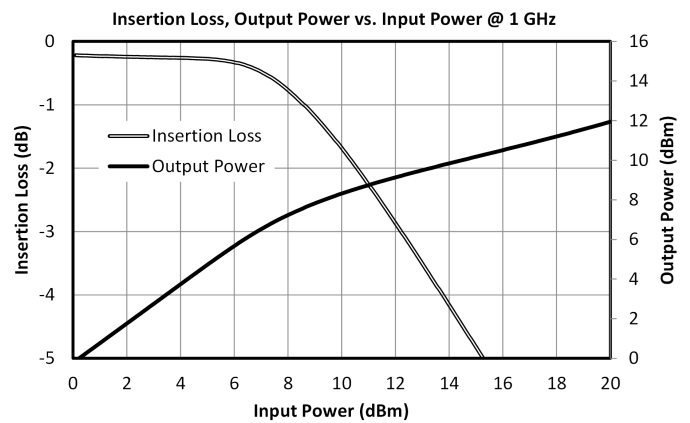
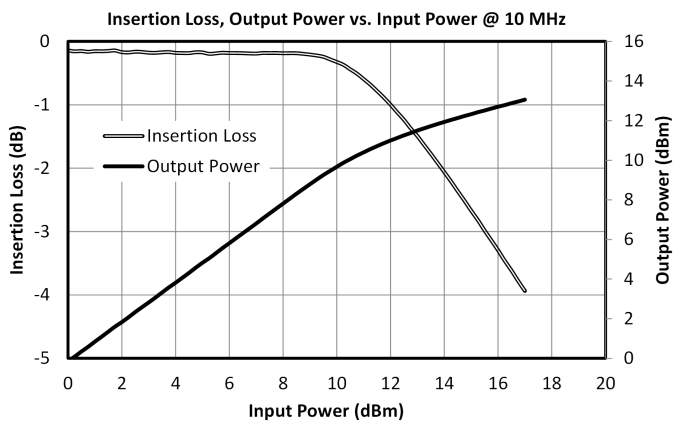
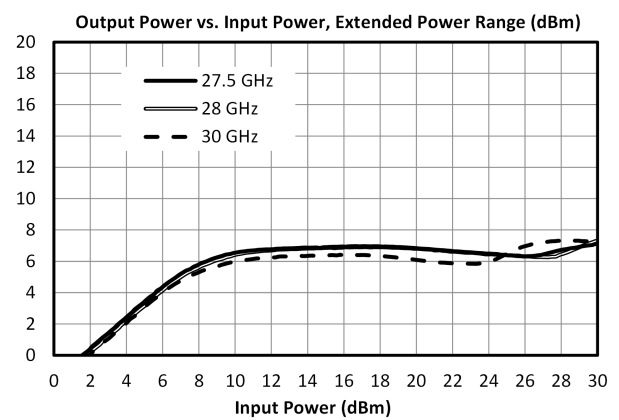
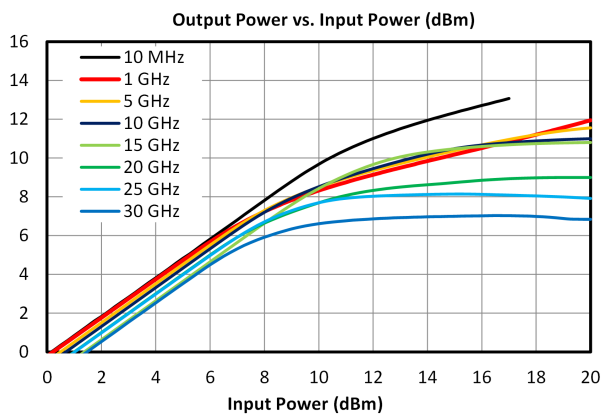
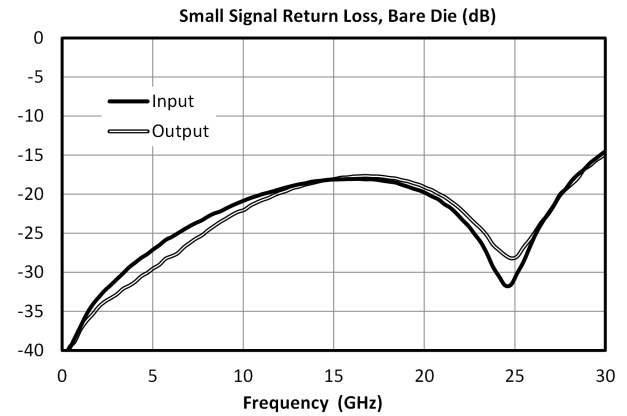
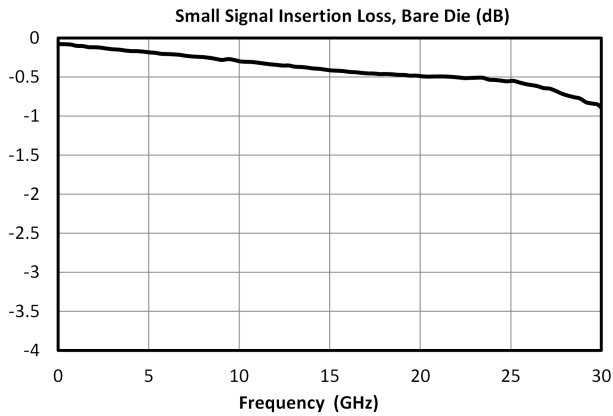
Parameter	Details	Rating
ESD	250 to < 500 Volts	HBM Class 1A
Dimensions	-	1.38x1.17 mm

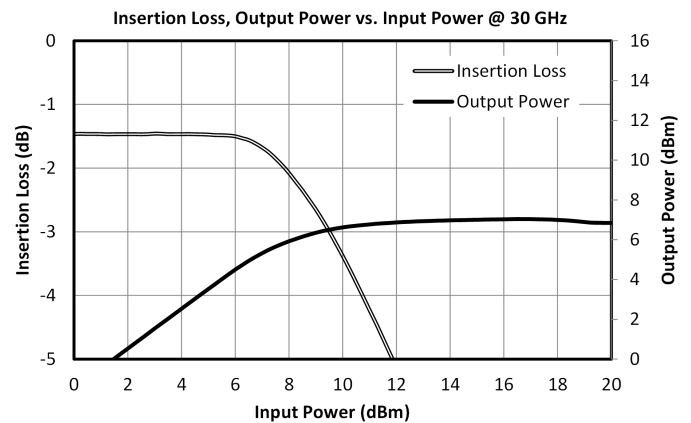
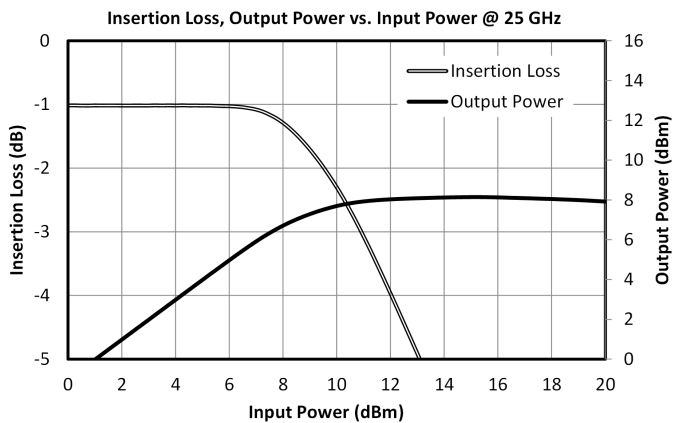
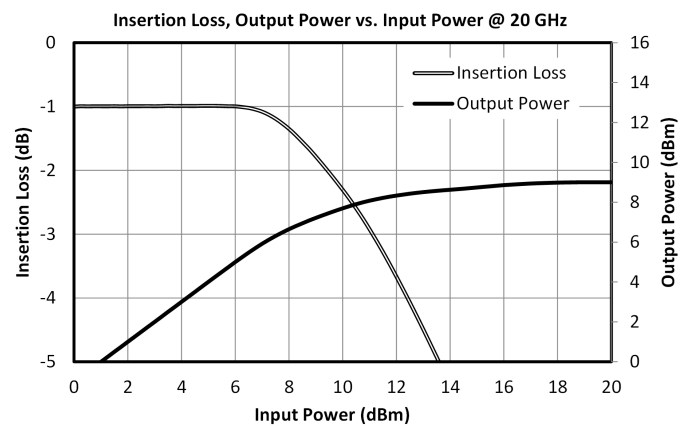
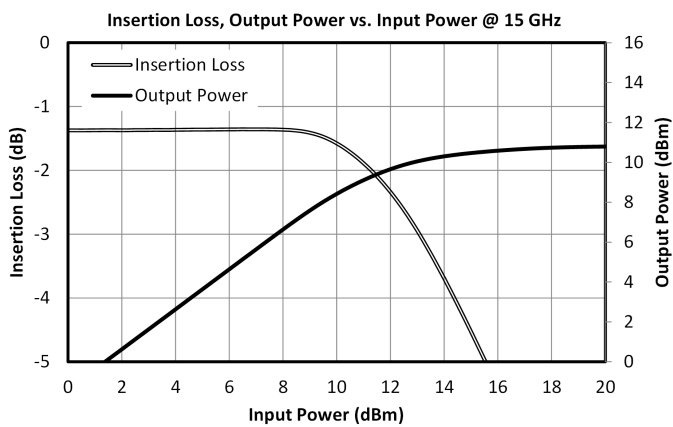
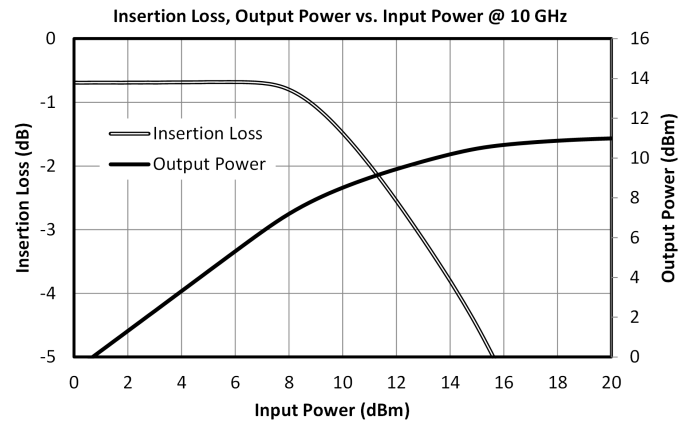
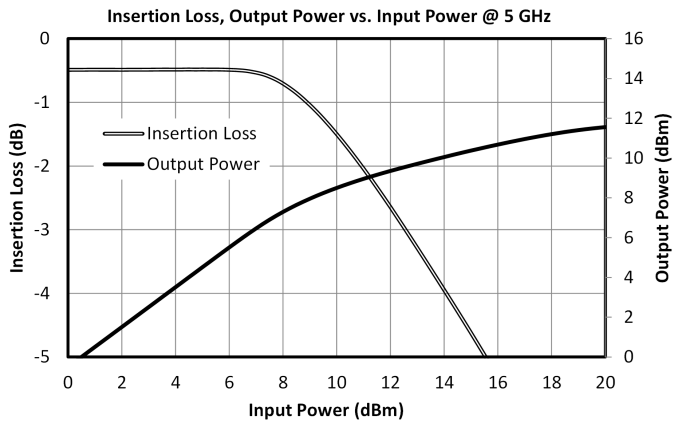
Electrical Specifications

The electrical specifications apply at TA=+25°C in a 50Ω system. Typical data shown is for the connectorized U-package limiter unless otherwise specified. Linear Specifications valid for input power up to the 0.1dB compression point. See typical performance plots for P0.1dB graph. Min and Max limits are guaranteed at TA=+25°C.

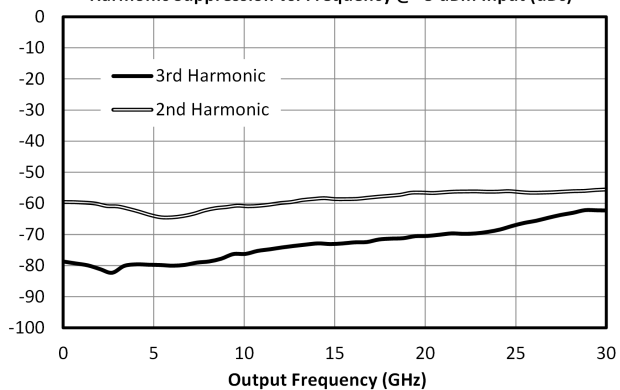
Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Insertion Loss	DC – 30GHz	0	30	-	0.4	1.5	dB
Return Loss	DC – 30GHz	0	30	-	23	-	dB
Flat Leakage	-	-	-	-	7	-	dBm
Input P1dB	-	-	-	-	10	-	dBm
Flat Leakage at 1W at 30GHz	DC – 30GHz	0	30	-	7	-	dBm
Input 1dB Gain Compression Point	DC – 30GHz	0	30	-	10	-	dBm
Flat Leakage at 1W	-	-	-	-	7	-	dBm
Input 1dB Compression	-	-	-	-	10	-	dBm

Typical Performance Plots

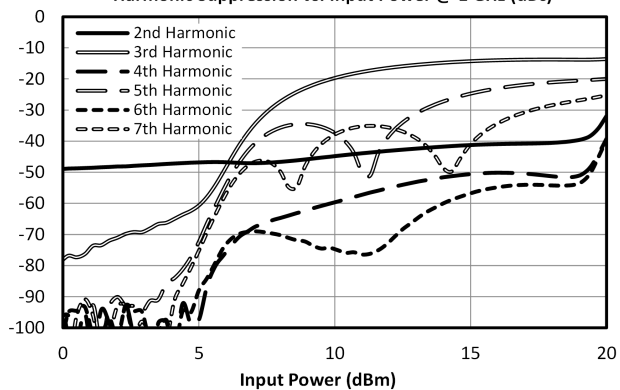




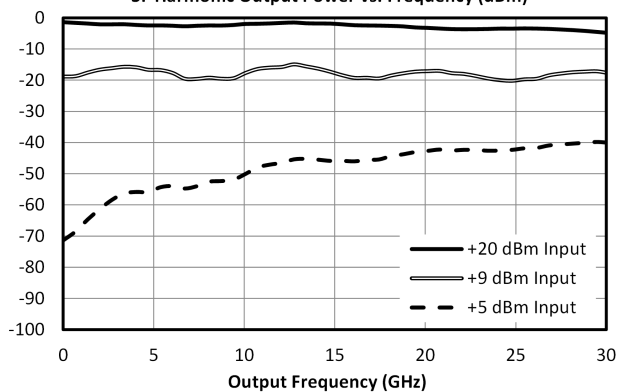
Harmonic Suppression vs. Frequency @ -5 dBm Input (dBc)



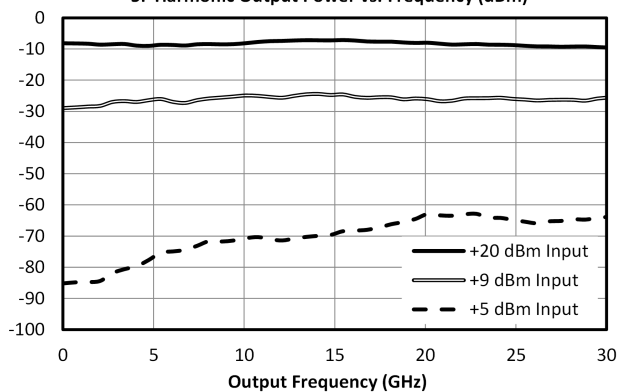
Harmonic Suppression vs. Input Power @ 1 GHz (dBc)



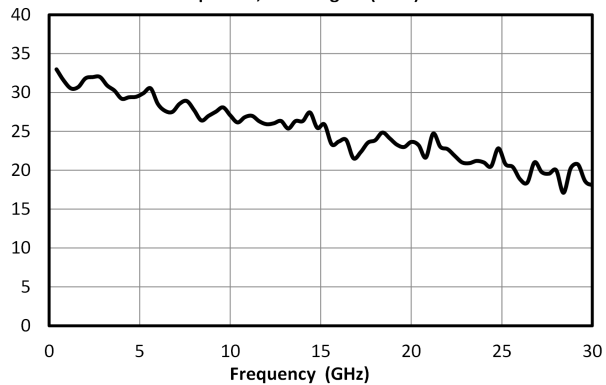
3F Harmonic Output Power vs. Frequency (dBm)



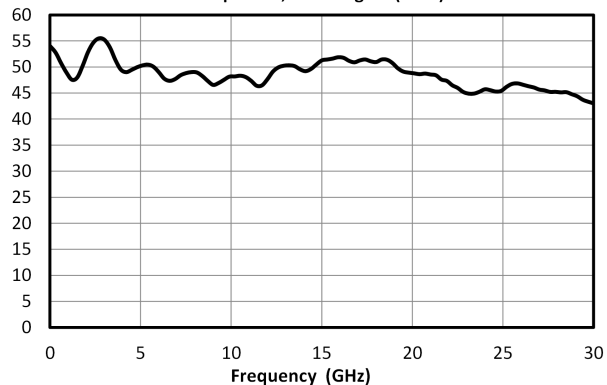
5F Harmonic Output Power vs. Frequency (dBm)



Input IP3, Small Signal (dBm)



Input IP2, Small Signal (dBm)



Input Power at Observed Failure

Power handling specification is based on tests performed at different combinations of temperature and frequency. Input power was increased until catastrophic failure was observed. Results are shown in the following table. The power handling specification listed in Absolute Maximum Ratings is based on the worst observed power handling derated by 3dB.

Frequency	Maximum Average Power Handling	Unit	Frequency	Maximum Peak Power Handling ⁴	Unit
2 GHz	+36.5	dBm	2 GHz	13	W
30 GHz	+33.0	dBm	18 GHz	9	W

Die Mounting Recommendations

Mounting and Bonding Recommendations

Marki MMICs should be attached directly to a ground plane with conductive epoxy. The ground plane electrical impedance should be as low as practically possible. This will prevent resonances and permit the best possible electrical performance. Datasheet performance is only guaranteed in an environment with a low electrical impedance ground.

Mounting- To epoxy the chip, apply a minimum amount of conductive epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip. Cure epoxy according to manufacturer instructions.

Wire Bonding - Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31 mm (12 mils).

Circuit Considerations – 50 Ω transmission lines should be used for all high frequency connections in and out of the chip. Wirebonds should be kept as short as possible, with multiple wirebonds recommended for higher frequency connections to reduce parasitic inductance. In circumstances where the chip more than .001" thinner than the substrate, a heat spreading spacer tab is optional to further reduce bondwire length and parasitic inductance.

Handling Precautions

General Handling

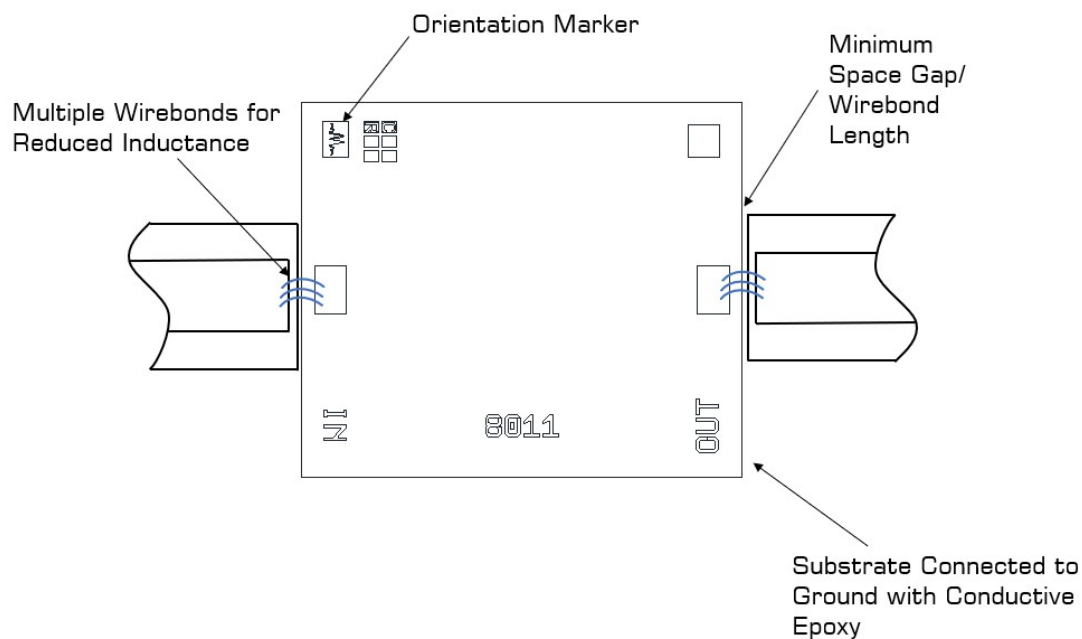
Chips should be handled with care using tweezers or a vacuum collet. Users should take precautions to protect chips from direct human contact that can deposit contaminants, like perspiration and skin oils on any of the chip's surfaces.

Static Sensitivity

GaAs MMIC devices are sensitive to ESD and should be handled, assembled, tested, and transported only in static protected environments.

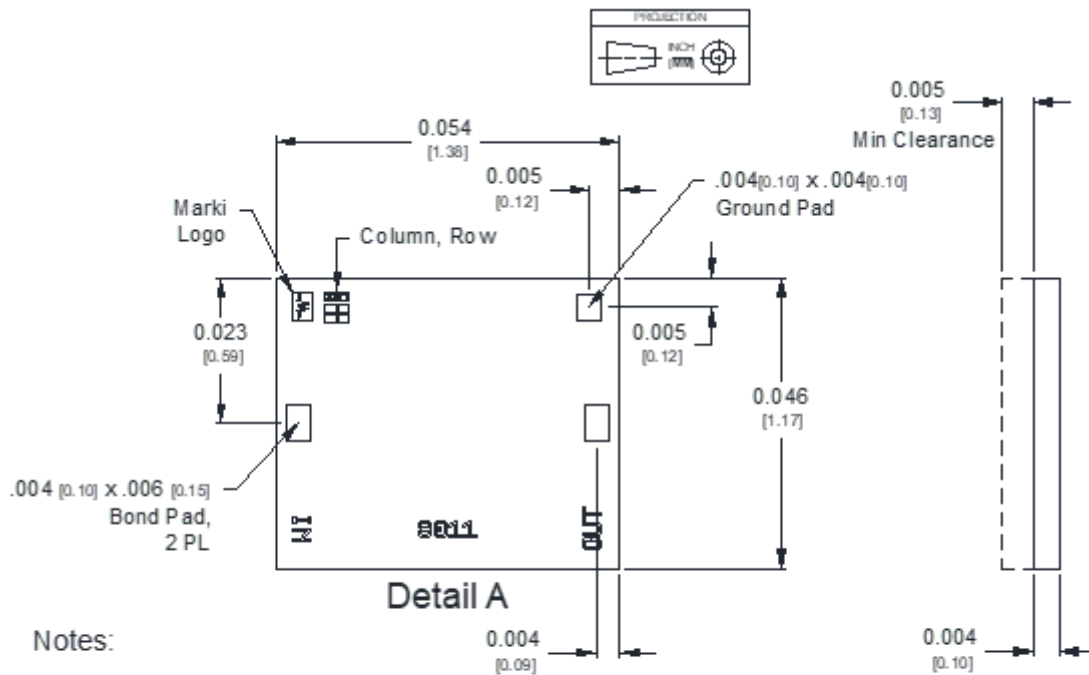
Cleaning and Storage: Do not attempt to clean the chip with a liquid cleaning system or expose the bare chips to liquid. Once the ESD sensitive bags the chips are stored in are opened, chips should be stored in a dry nitrogen atmosphere.

Bonding Diagram



Mechanical Data

Outline Drawing



1. CH substrate is .004 in Thick GaAs.
2. I/O trace is 4 microns Au. Ground is 5 microns Au.
3. Tolerance for X, Y dimensions is ± 0.002 in.
Tolerance for Z dimension is ± 0.0005 in.
Tolerance for pad location is ± 0.0001 in.

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