

1. Device Overview

1.1 General Description

NLTL-6794SM is a MMIC non-linear transmission line (NLTL) based comb generator. This NLTL offers excellent phase noise performance over a low 100MHz to 1 GHz input frequency range with output tones beyond 30 GHz. NLTL-6794SM is fabricated with GaAs Schottky diode-based varactors and packaged into a surface mount 6x6 mm² QFN.



QFN

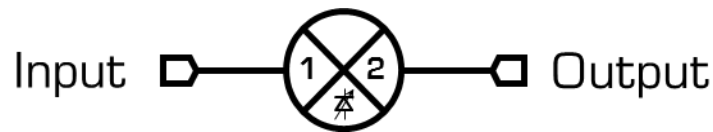
1.2 Features

- Low Phase Noise
- Broadband Input Frequencies
- No External DC Bias Required

1.3 Applications

- Comb Line Generation
- High Efficiency Multiplication
- Samplers
- Phase Locked Loops

1.4 Functional Block Diagram



1.5 Part Ordering Options¹

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
NLTL-6794SM	6mm QFN	SM	RoHS	Active	EAR99
EVAL-NLTL-6794	Connectorized module, QFN reflowed onto PCB	EVAL		Active	EAR99

¹ Refer to our [website](#) for a list of definitions for terminology presented in this table.

Table of Contents

1. Device Overview	1	4.6.2 Typical Performance Plots: Harmonic Output Power w/ Square Wave from APM-7098PA	10
1.1 General Description	1	4.6.3 Typical Performance Plots: Harmonic Output Power w/ Square Wave from ADM1-0026PA	13
1.2 Features	1	4.6.4 Typical Performance Plots: 5 th Harmonic Output Power vs Bias Resistor.....	15
1.3 Applications	1	4.6.5 Typical Performance Plots: 10 th Harmonic Output Power vs Input Power	16
1.4 Functional Block Diagram	1	4.6.6 Typical Performance Plots: Conversion Loss and Output Power vs Input Power.....	16
1.5 Part Ordering Options.....	1	4.6.7 Typical Performance Plots: Time and Frequency Domain Plots	18
2. Port Configurations and Functions	3	4.6.8 Typical Performance Plots: Residual Phase Noise	24
2.1 Port Diagram	3	5. Mechanical Data	25
2.2 Port Functions	3	5.1 SM Package Outline Drawing	25
3. Application Information	4	5.2 SM Package Footprint	25
3.1 Detailed Description	4	5.3 Evaluation Board Outline Drawing...	26
3.2 Application Circuit: SM Package and EVAL Package	5		
4. Specifications	6		
4.1 Absolute Maximum Ratings.....	6		
4.2 Package Information	6		
4.3 Recommended Operating Conditions .	6		
4.4 Sequencing Requirements	6		
4.5 Electrical Specifications	7		
4.6 Typical Performance Plots	8		
4.6.1 Typical Performance Plots: Harmonic Output Power w/ Sine Input .	8		

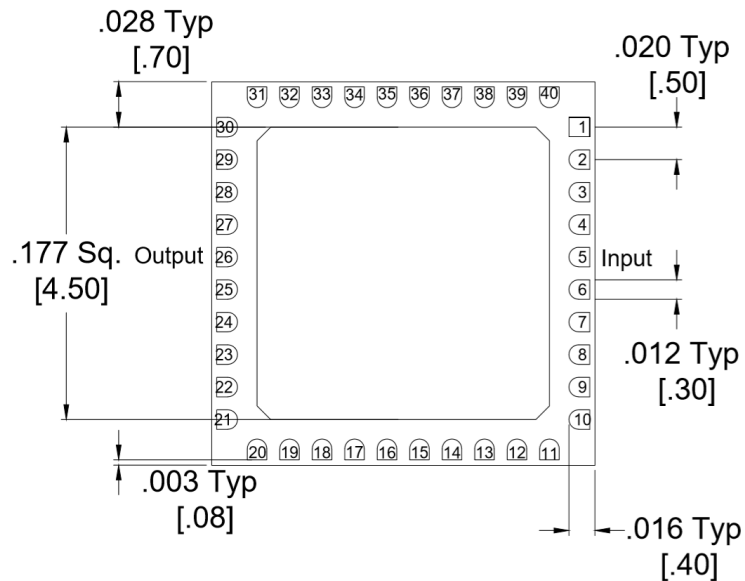
Revision History

Revision Code	Revision Date	Comment
-	December 2019	Initial Release
A	January 2022	Phase Noise Plot Added
B	October 2022	Recommended Input Power Updated

2. Port Configurations and Functions

2.1 Port Diagram

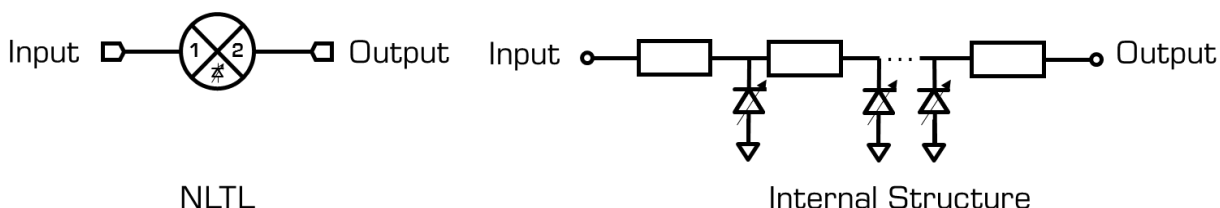
A bottom-up view of the NLTL-6794's SM package outline drawing is shown below. The NLTL should only be used in the forward direction, with the input and output ports given in Port Functions.



2.2 Port Functions

Port	Function	Description	Equivalent Circuit for Chip
Pin 5	Input	Pin 5 is diode connected and AC matched to 50Ω.	Pin 5
Pin 26	Output	Pin 26 is diode connected and AC matched to 50Ω.	Pin 26
GND	Ground	SM package ground path is provided through the ground paddle.	GND

3. Application Information



3.1 Detailed Description

The NLTL-6794SM belongs to Marki Microwave's NLTL family of multipliers and non-linear transmission lines. The NLTL product line consists of passive GaAs MMIC non-linear transmission lines designed and fabricated with GaAs Schottky diode-based varactors. NLTLs take an input signal and create an impulse train of harmonics. Harmonic outputs up to and beyond 30 GHz are generated by the NLTL. The NLTL-6794SM is a 6 mm QFN and the EVAL-NLTL-6794 is a connectorized module with the QFN reflowed onto a PCB.

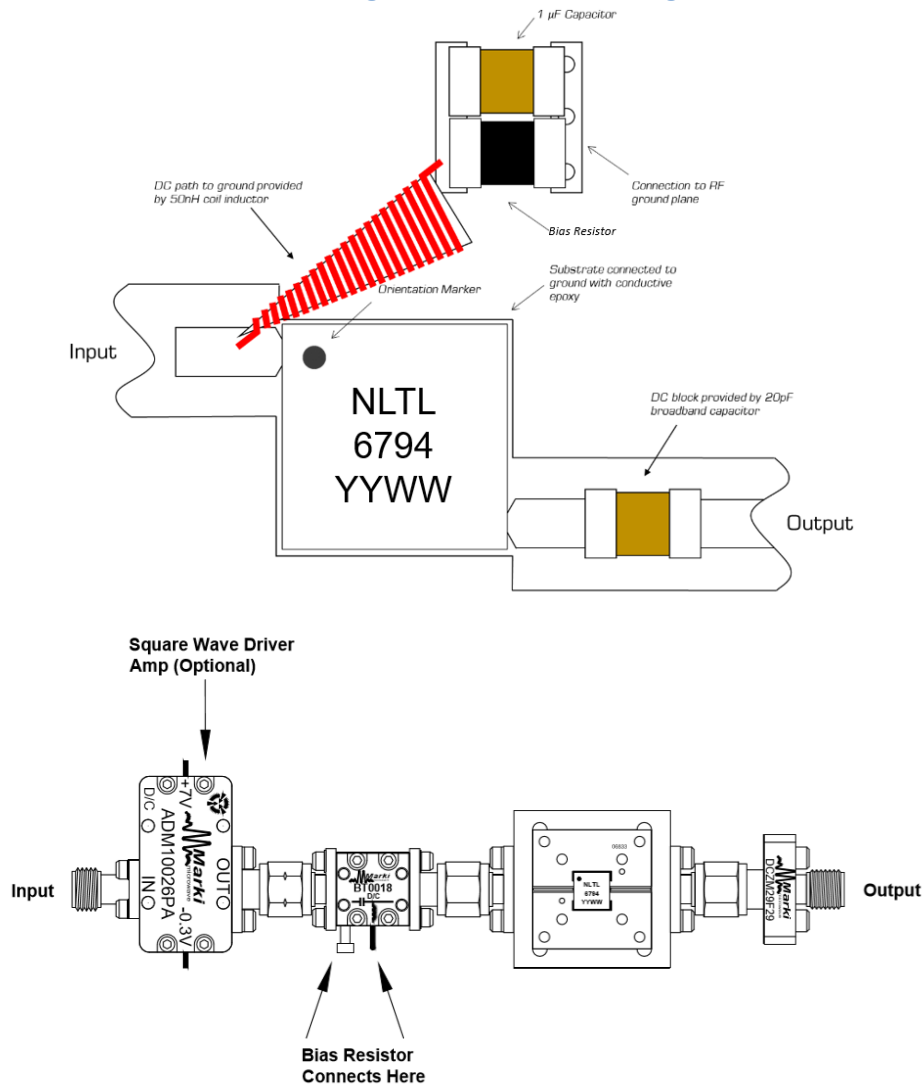
Port 1 supports up to 1GHz input signals. Port 2 will output integer multiples of the input signal (i.e., x_2 , x_3 , x_4 , etc.) up to a maximum of ~30 GHz given a -60dBm threshold. Higher harmonics are generated but at a lower efficiency.

The operating conditions of the NLTL are extremely important to optimize performance. High power inputs will increase the output power observed; however, the conversion efficiency will decrease. This is increasingly true for higher input frequencies and at input powers above the recommended limit. Optimal conversion efficiency of the NLTL is achieved using a square wave input with a fast rise time. Doing so causes a degradation in the 2nd output harmonic but otherwise improves the conversion efficiency at all other harmonics. It is for this reason that the typical performance plots in section 4.6 are shown driven with a sine wave input as well as with two amplifiers, the [ADM1-0026PA](#), a square wave driver amp, and the APM-7098PA, a low phase noise amplifier. Section 4.6.7 shows the results of these driver amplifiers in time and frequency domain.

NLTL-6794SM requires no external DC bias. The self-bias of the diodes caused by the rectified RF input signal is sufficient for operation. For the best performance, optimization of the DC return path through a bias resistor is recommended for each specific application to optimize the harmonic output power distribution.

The phase noise of a non-linear transmission line is outstanding. If verification of performance is necessary, the application circuit used and input conditions are extremely important. NLTLs are AM sensitive. If there is excessive AM noise on the input of the NLTL, observing the output of the NLTL will show excessive PM/phase noise because of the high AM to PM conversion property of NLTLs.

3.2 Application Circuit: SM Package and EVAL Package



DC Path to Ground — An RF choke followed by a bias resistor should be used to provide a DC path to ground on the input port of the NLTL SM package. The current through the resistor will create Johnson/white noise; a shunt capacitor (for example 1uF) is used to filter noise generated by the resistor. This forms the circuit which self-biases the NLTL. The DC return to ground removes DC rectified current created by high power RF signal injection. A conical coil inductor is recommended to push the self-resonance frequency of the inductor past the operating bandwidth of the NLTL. The recommended inductance value of the conical coil inductor is 50nH or higher. If using a connectorized application setup, a bias tee will provide a DC path to ground and the NLTL can be biased with an additional resistor on the bias tee. See section 4.6.4 for output power vs bias resistor plots.

Blocking Capacitor — A DC blocking capacitor on the output of the NLTL-6794SM's integrated circuit is there to prevent unwanted DC current flow from or to the output. If there is a DC signal on the input, place a DC block or bias tee on the input to avoid disrupting the self-biasing of the diodes.

4. Specifications

4.1 Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Units
Power Handling, at any Port	+33	dBm
Operating Temperature	-55 to +100	°C
Storage Temperature	-65 to +125	°C

4.2 Package Information

Parameter	Details	Rating
ESD	Human Body Model (HBM), per MIL-STD-750, Method 1020	1A
Weight	EVAL Package	18.3 g

4.3 Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits inside which the device should be operated to guarantee the performance given in Electrical Specifications. Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

	Min	Nominal	Max	Units
T _A , Ambient Temperature	-55	+25	+100	°C
Input Power		+20	+28	dBm

4.4 Sequencing Requirements

This is a passive NLTL that requires no external DC bias. Self-bias of the diodes is sufficient for operation. It is not required, but is recommended to provide a 50Ω termination to each port before applying RF power.

4.5 Electrical Specifications

The electrical specifications apply at $T_A=+25^{\circ}\text{C}$ in a 50Ω system. Typical data shown is for the NLTL used in the forward direction with a +20 dBm 250MHz sine wave input and no bias resistor (open circuit) unless otherwise stated².

Min and Max limits apply only to our connectorized units and are guaranteed at $T_A=+25^{\circ}\text{C}$. All bare die are 100% DC tested and visually inspected.

Parameter	Test Conditions	Min	Typical	Max	Units
Input (Port 1) Frequency Range		0.1		1	GHz
Output (Port 2) Frequency Range		0.1		30	
Input Power			+20 ³		dBm
Highest Frequency Harmonic Output ⁴	100 MHz Input		6.1		GHz
	250 MHz Input		23.25		
	500 MHz Input		29.5		
	750 MHz Input		27		
	1 GHz Input		22		
Approximate Harmonic Output Power with 100 MHz Input ⁵	$P_{\text{Harmonic}} = -0.82 * (\text{Harmonic Order}) - 10.7$				dBm
Approximate Harmonic Output Power with 250 MHz Input ⁵	$P_{\text{Harmonic}} = -0.6 * (\text{Harmonic Order}) - 3.3$				
Approximate Harmonic Output Power with 500 MHz Input ⁵	$P_{\text{Harmonic}} = -1.1 * (\text{Harmonic Order}) + 4.2$				
Approximate Harmonic Output Power with 750 MHz Input ⁵	$P_{\text{Harmonic}} = -1.9 * (\text{Harmonic Order}) + 5.5$				
Approximate Harmonic Output Power with 1 GHz Input ⁵	$P_{\text{Harmonic}} = -2.8 * (\text{Harmonic Order}) + 6.0$				

² Square Wave input generated using either the ADM1-0026PA or the APM-7098PA amplifier at +7V/-0.3V and +8V/+8V respectively.

³ Input power to square wave driver amps is lower but high enough to saturate the amplifier. Power levels in square wave plots refer to input power to the amplifier, not the amplifier's output power.

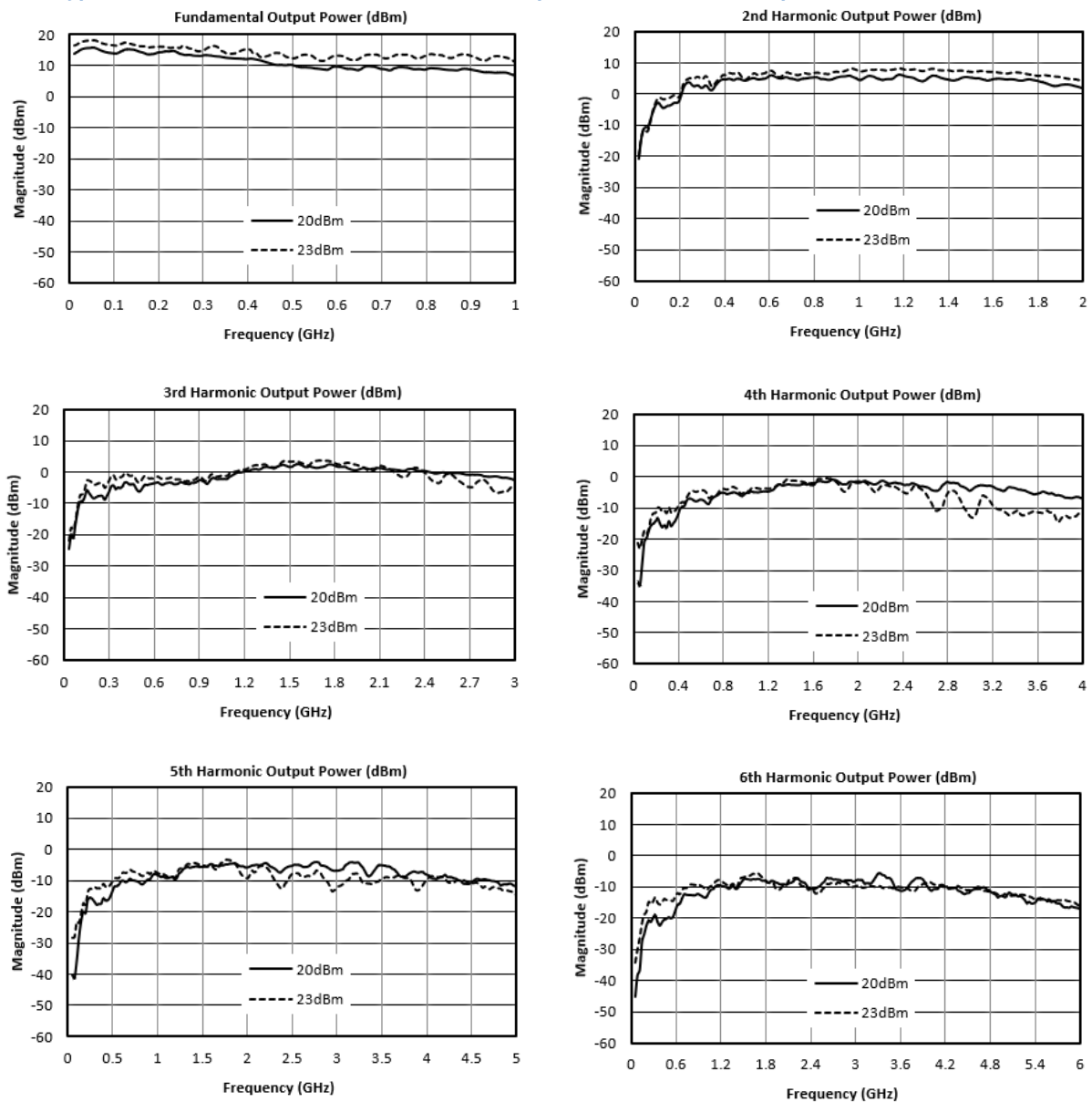
⁴ The Highest Frequency Harmonic Output was determined as the highest frequency harmonic that was above a -60dBm threshold as seen on a spectrum analyzer.

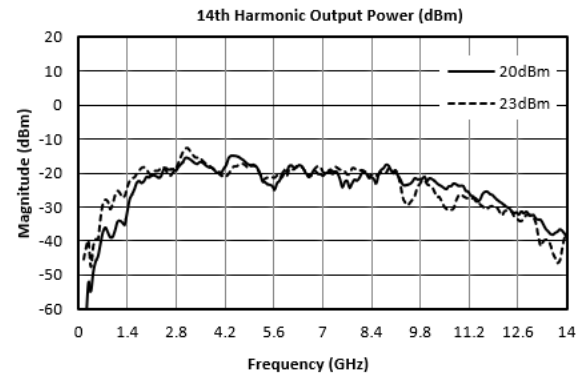
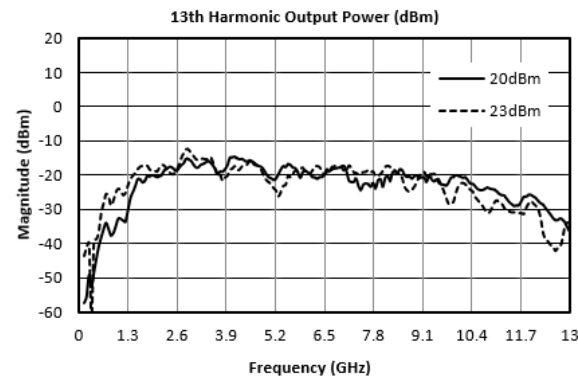
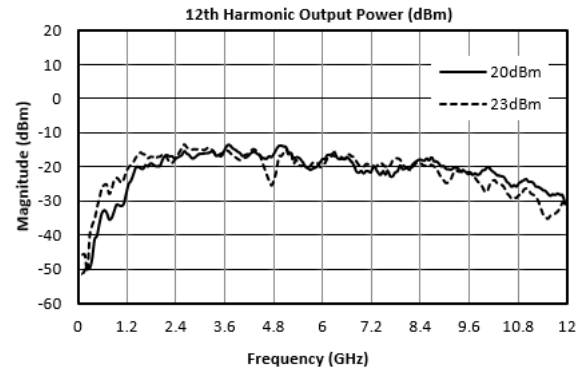
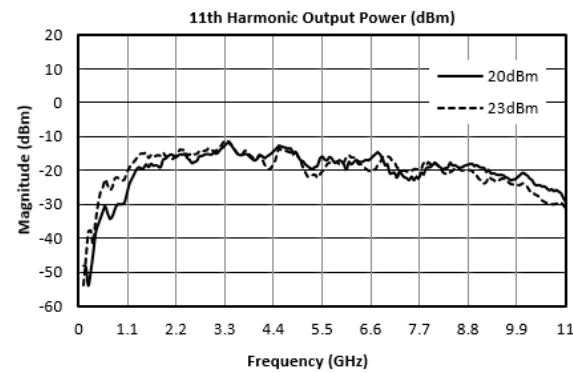
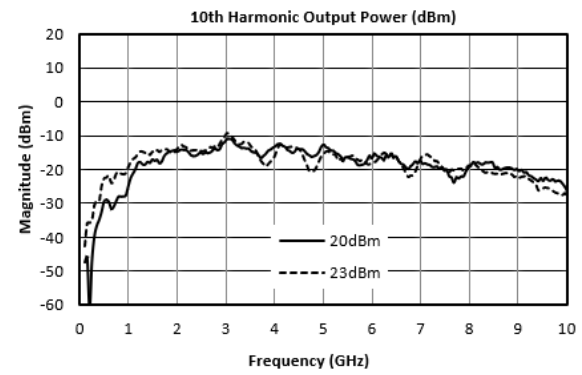
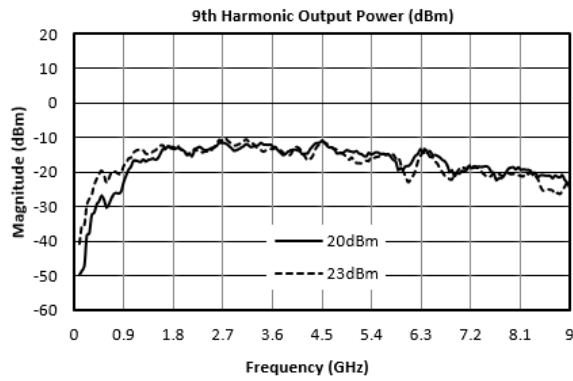
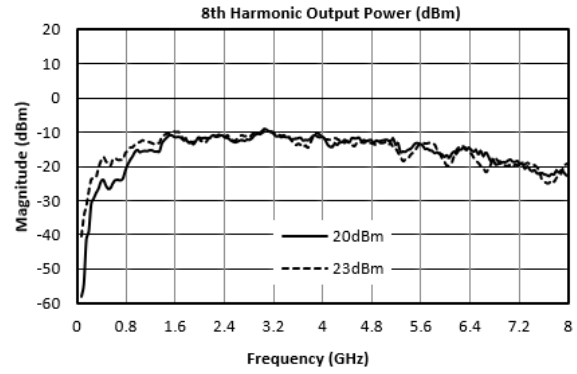
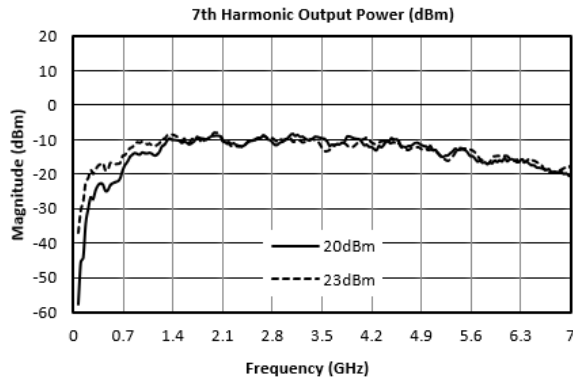
⁵ Approximate Harmonic Output Power equations are determined by taking points on the output comb on a spectrum analyzer and creating a linear fit equation to relate the harmonic order to its power level. Consequently, the equations offer an approximation of output harmonic level, not an exact measurement.

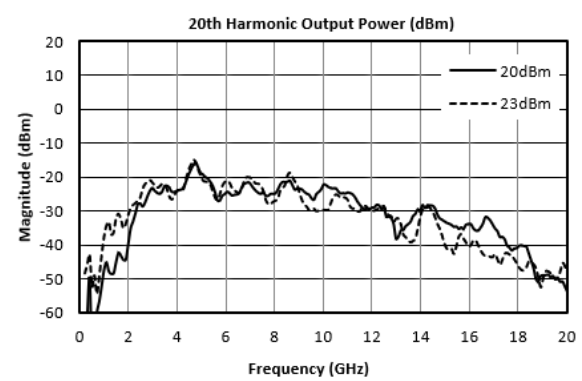
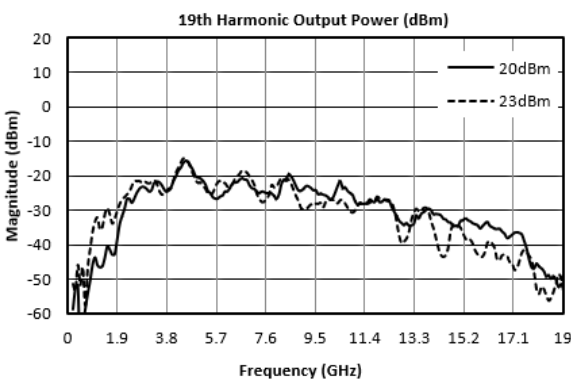
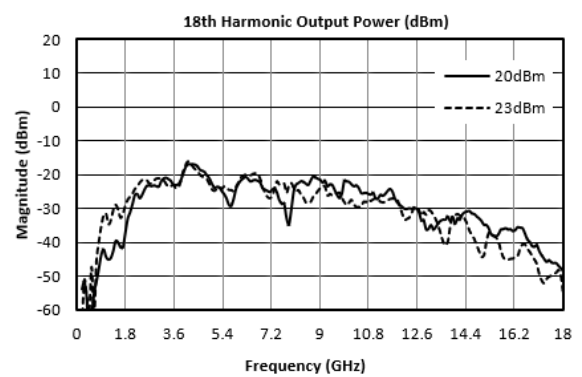
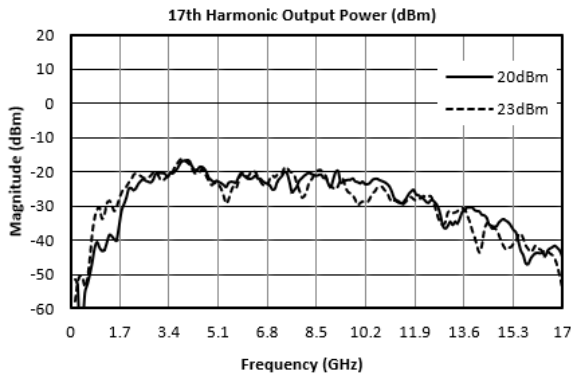
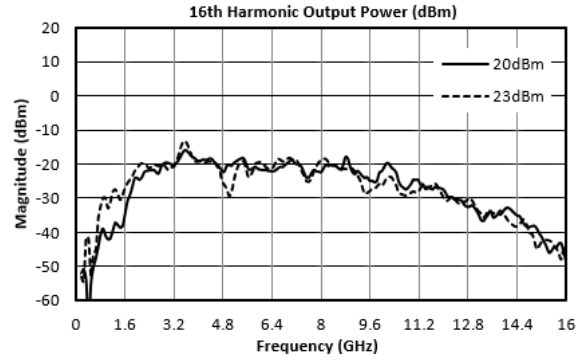
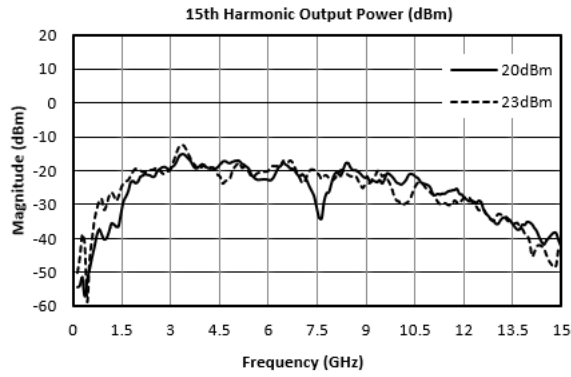
4.6 Typical Performance Plots

Input power levels refer to drive level going into the NLTL chain input in section 3.2. Square wave plots are referenced to drive level entering the square wave driver amplifier, not the output power of the amplifiers.

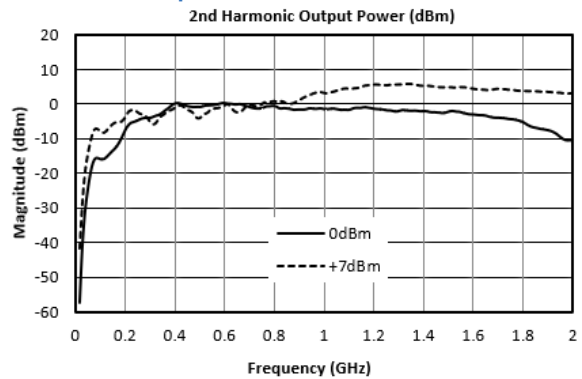
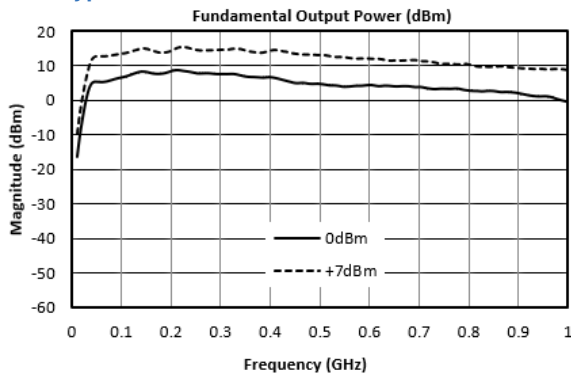
4.6.1 Typical Performance Plots: Harmonic Output Power w/ Sine Input

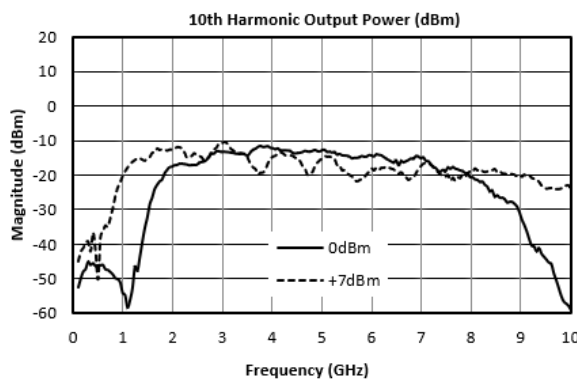
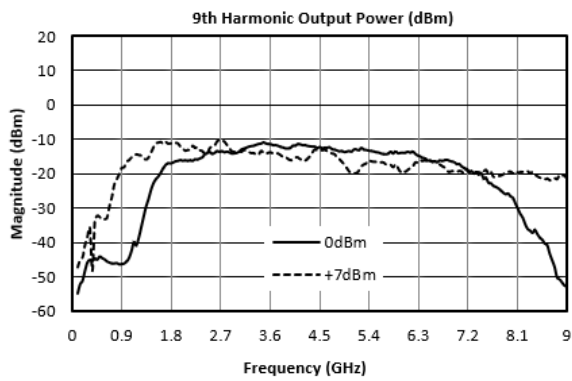
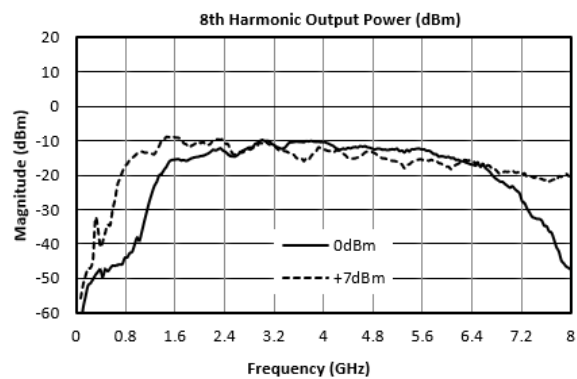
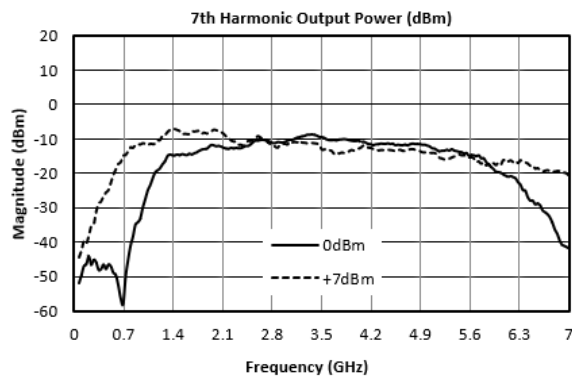
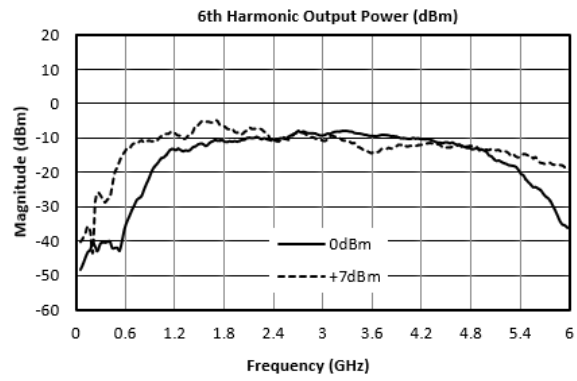
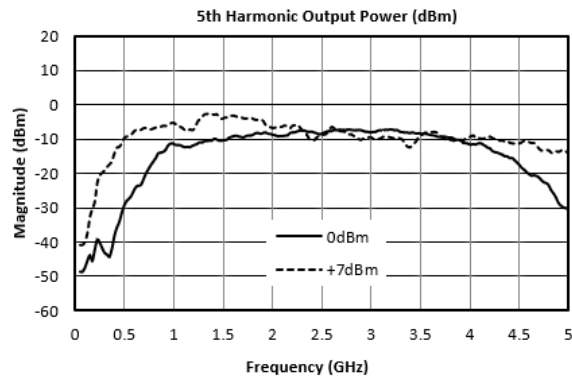
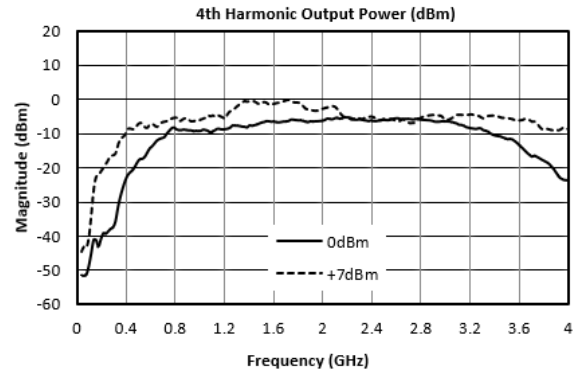
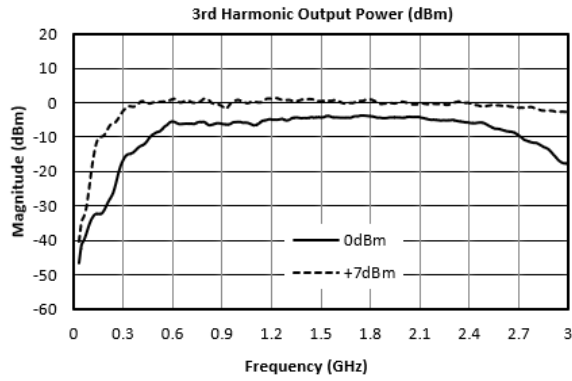


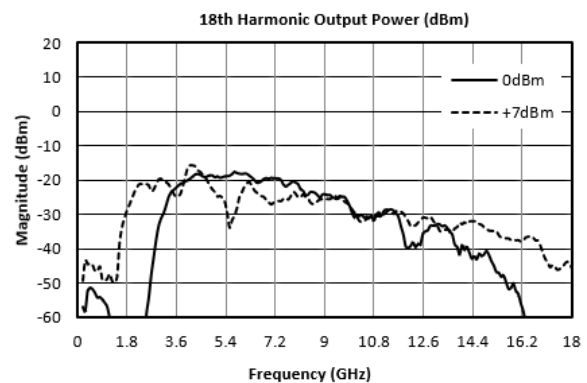
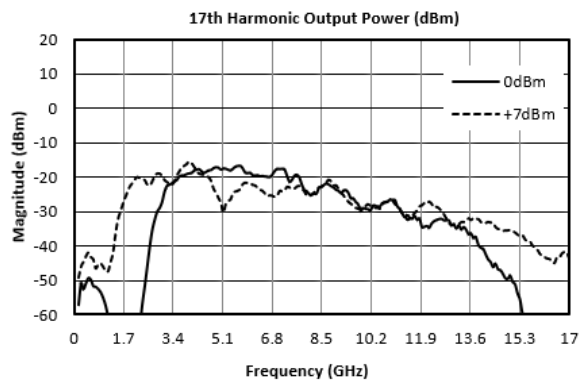
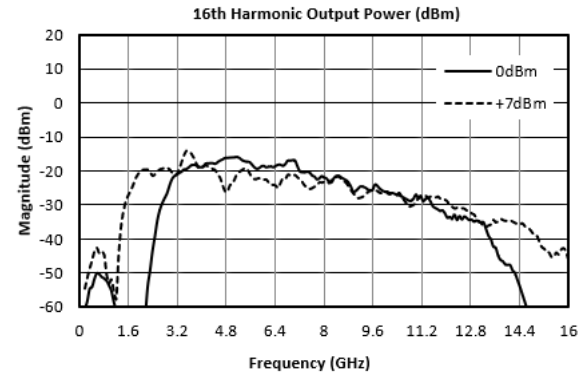
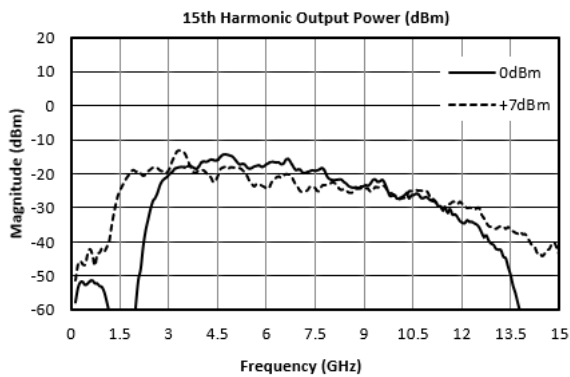
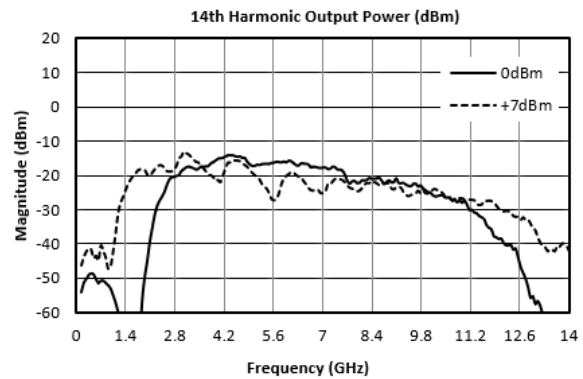
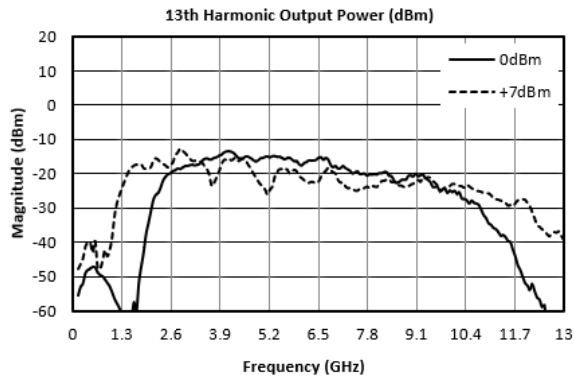
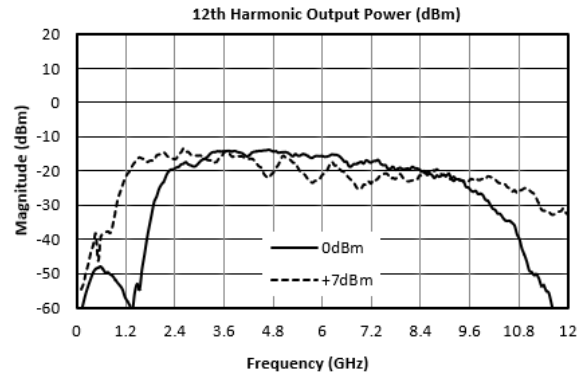
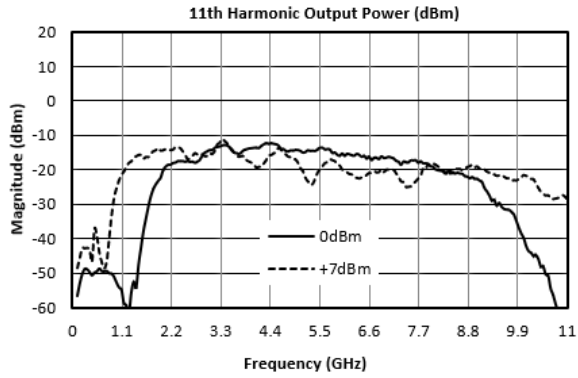


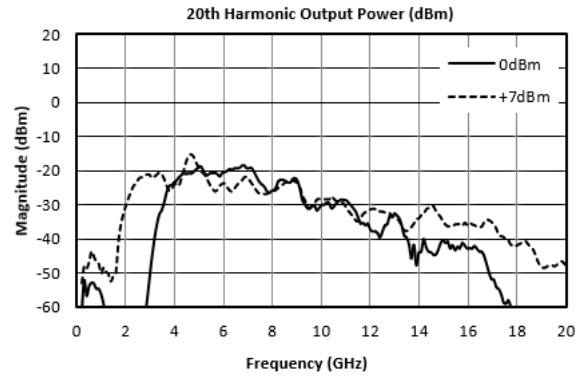
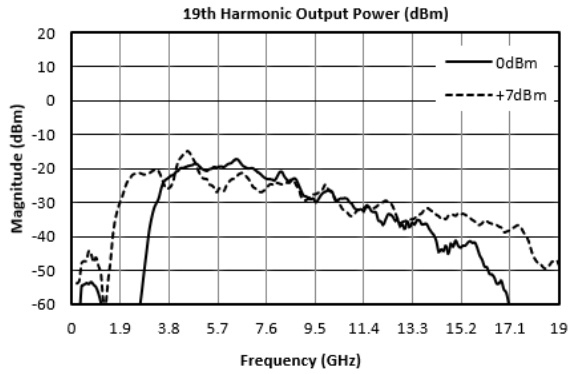


4.6.2 Typical Performance Plots: Harmonic Output Power w/ Square Wave from APM-7098PA

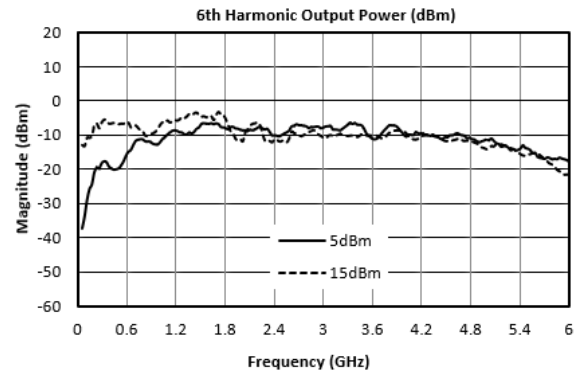
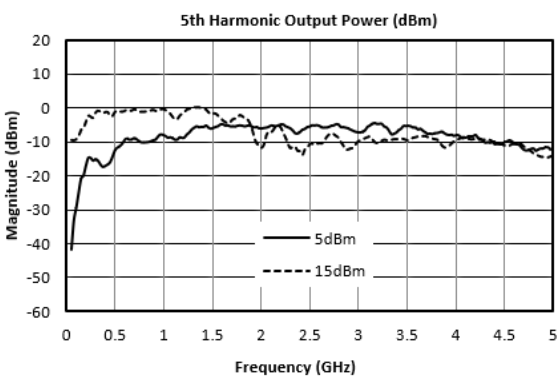
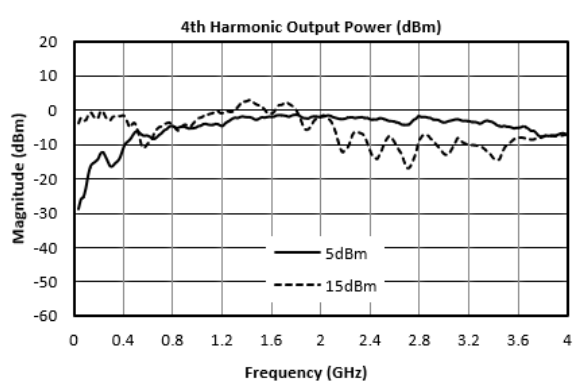
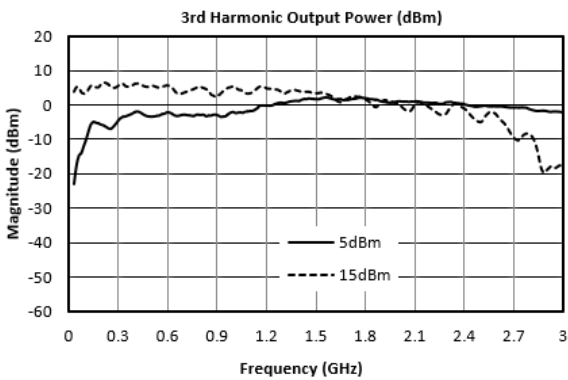
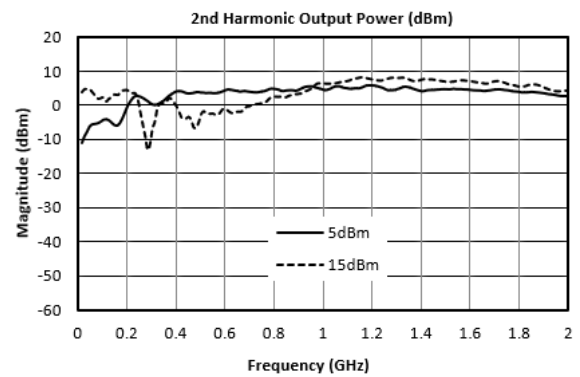
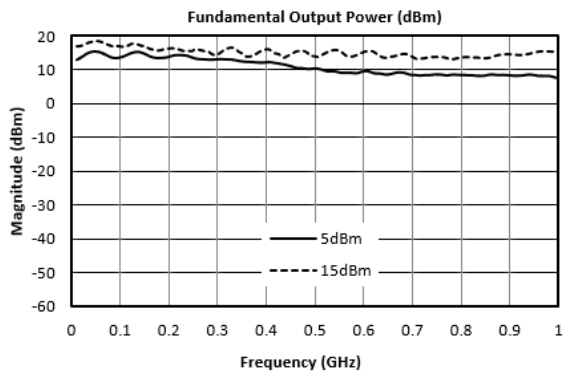


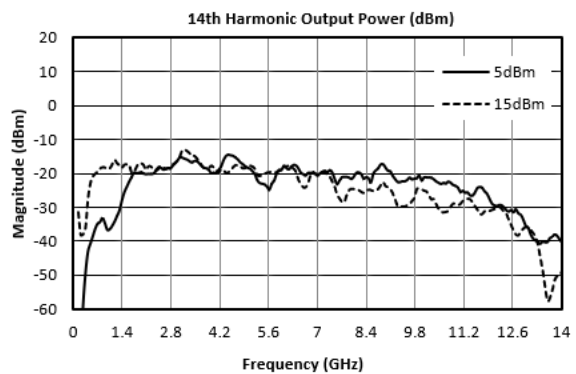
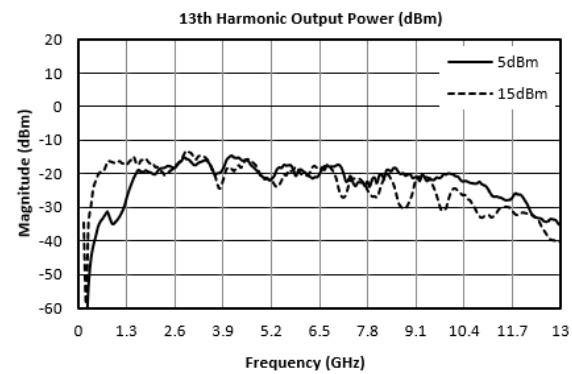
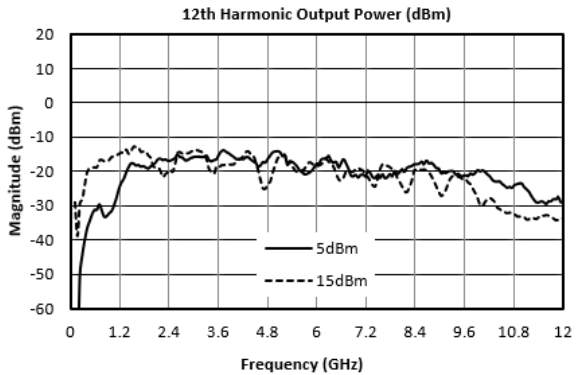
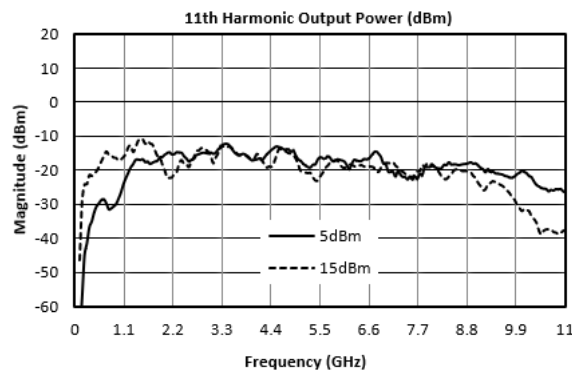
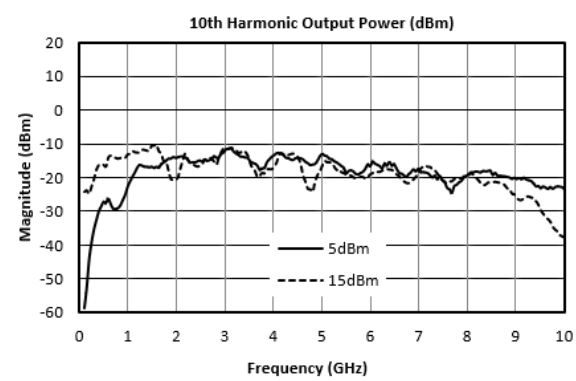
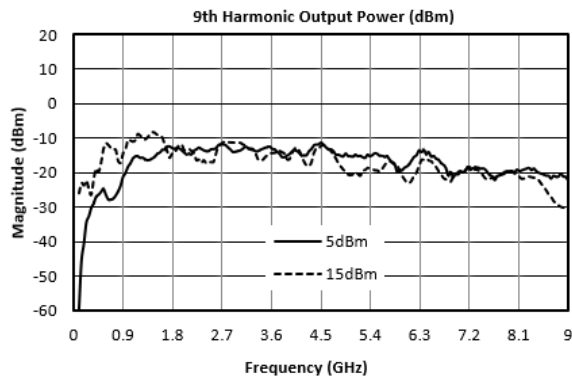
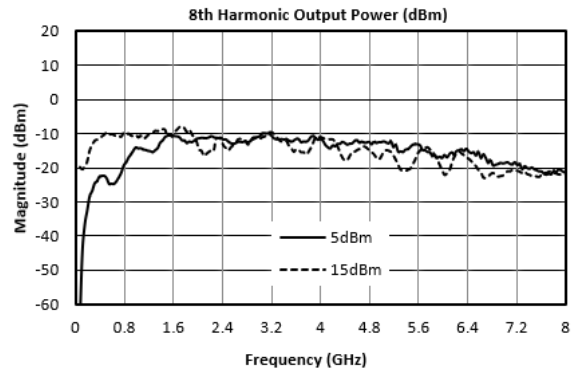
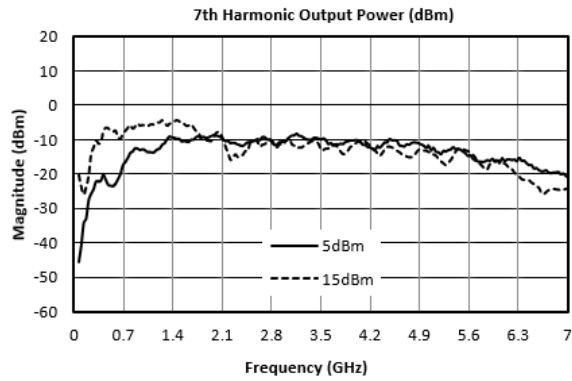


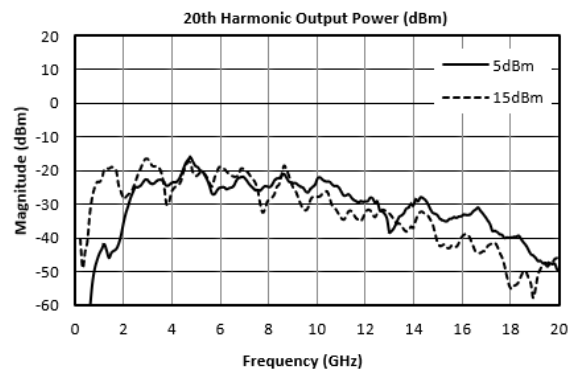
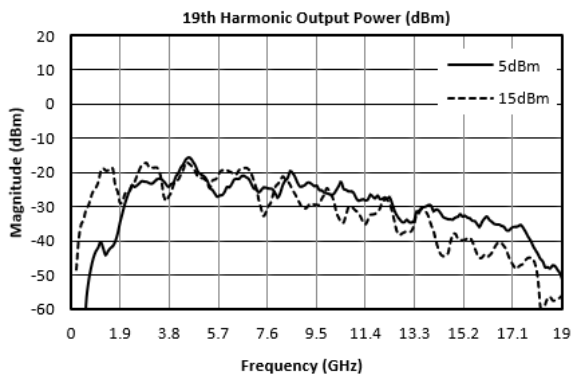
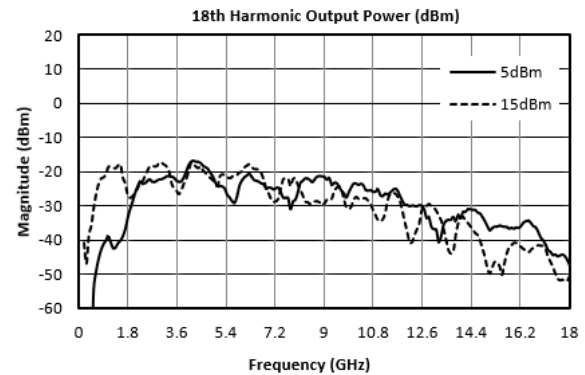
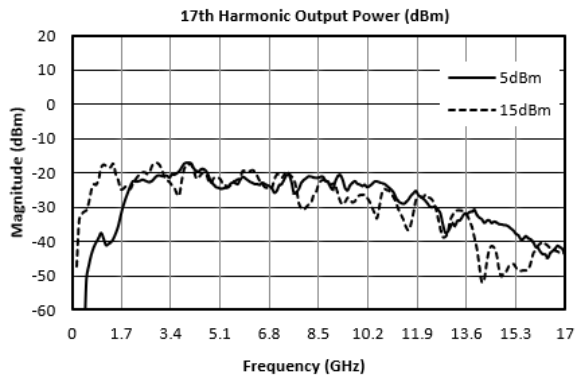
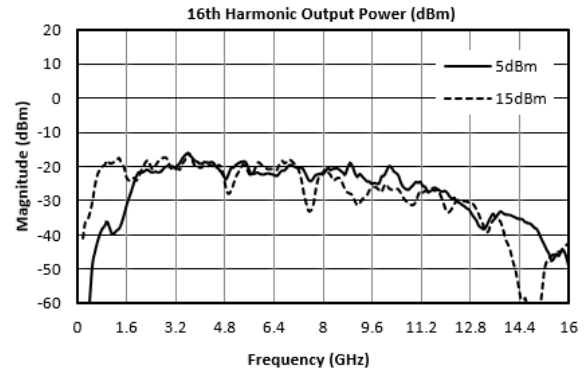
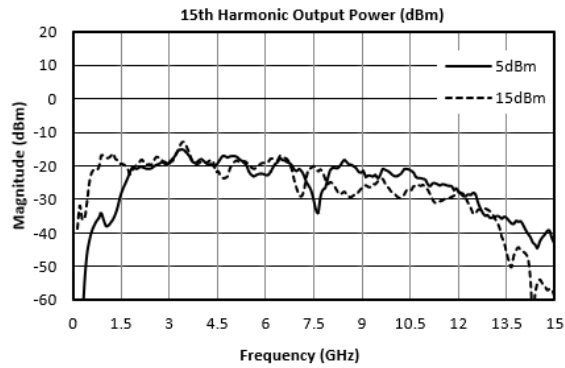




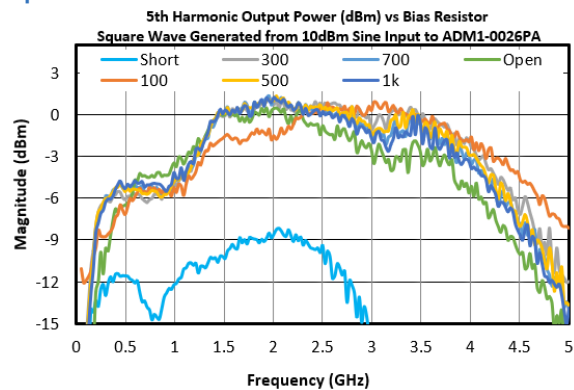
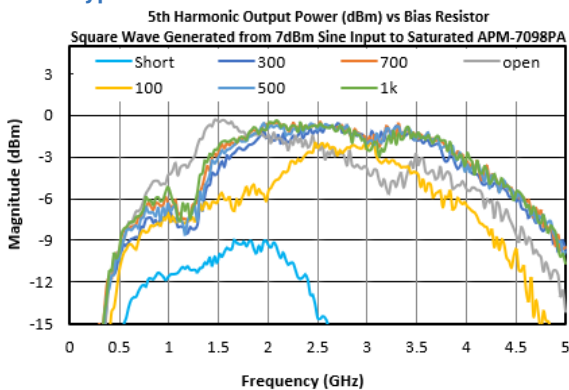
4.6.3 Typical Performance Plots: Harmonic Output Power w/ Square Wave from ADM1-0026PA

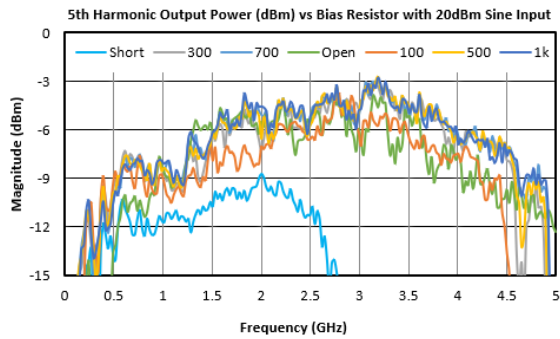






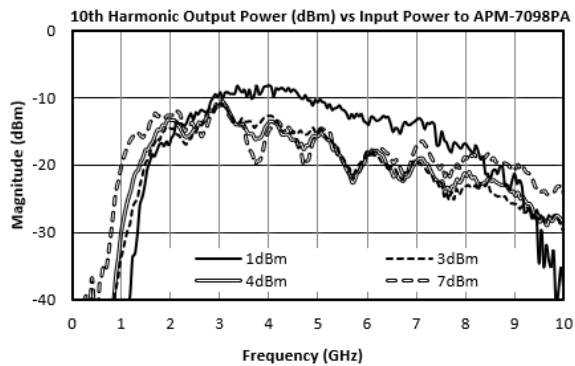
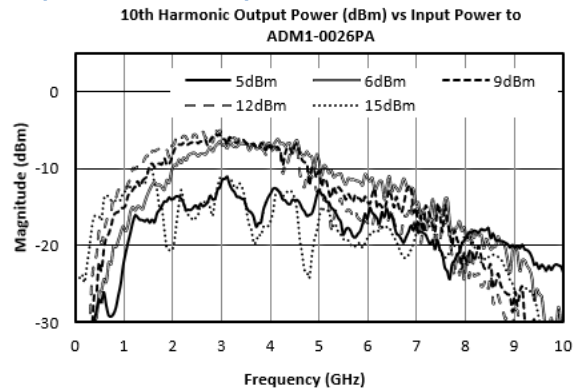
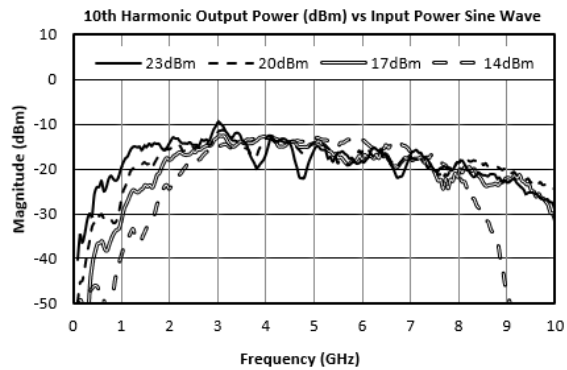
4.6.4 Typical Performance Plots: 5th Harmonic Output Power vs Bias Resistor





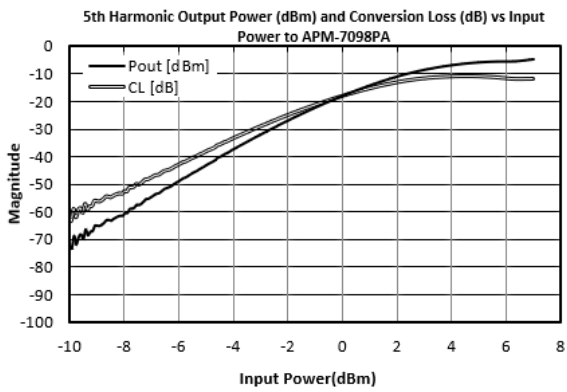
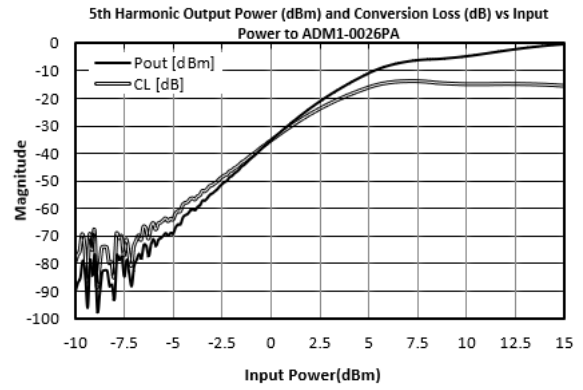
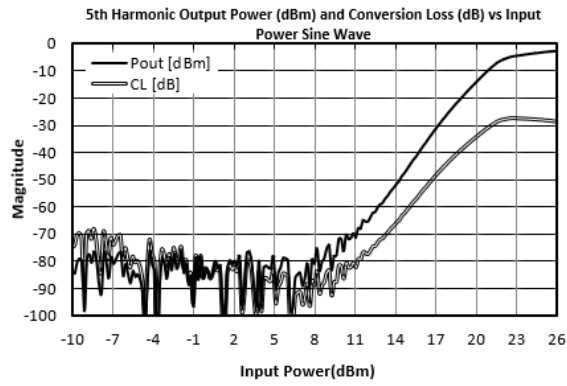
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4.6.5 Typical Performance Plots: 10th Harmonic Output Power vs Input Power



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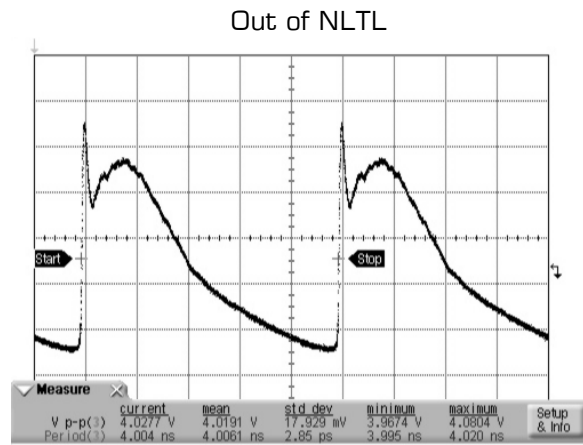
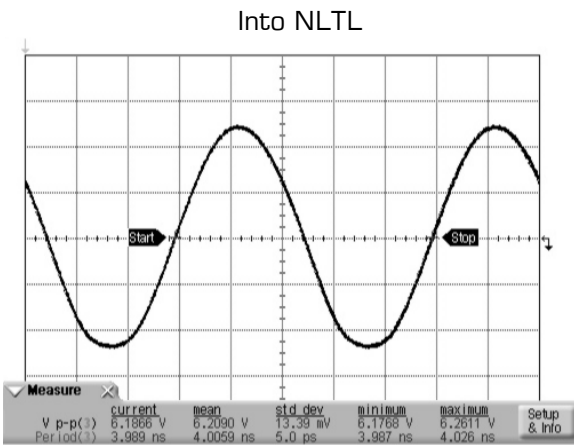
4.6.6 Typical Performance Plots: Conversion Loss and Output Power vs Input Power



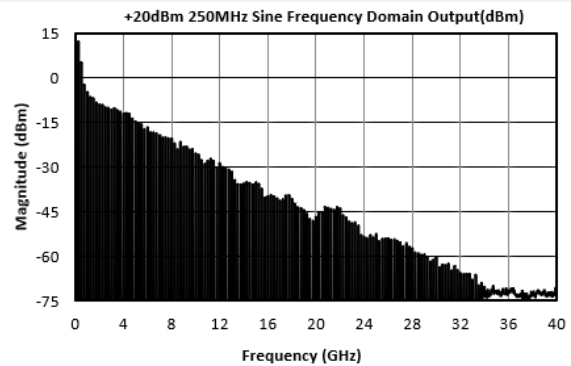
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4.6.7 Typical Performance Plots: Time and Frequency Domain Plots

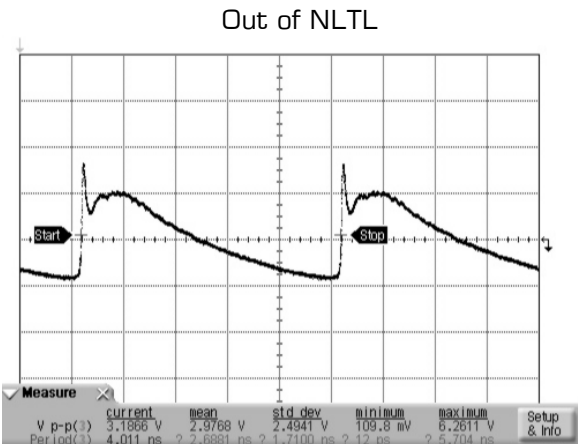
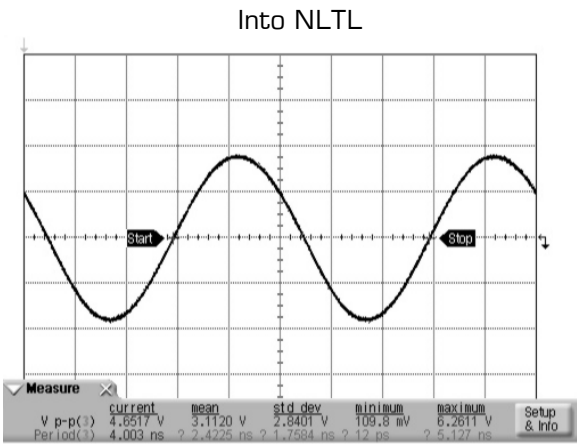
+20dBm 250MHz Sine Wave Input



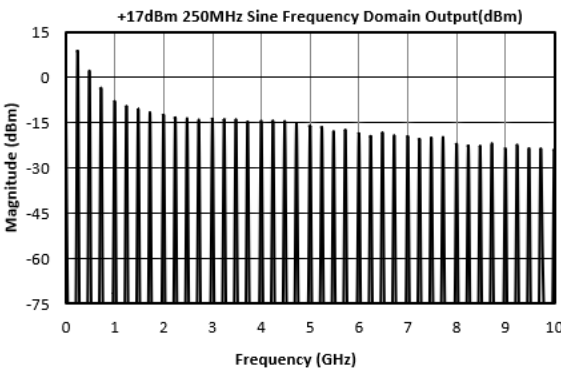
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+17dBm 250MHz Sine Wave Input

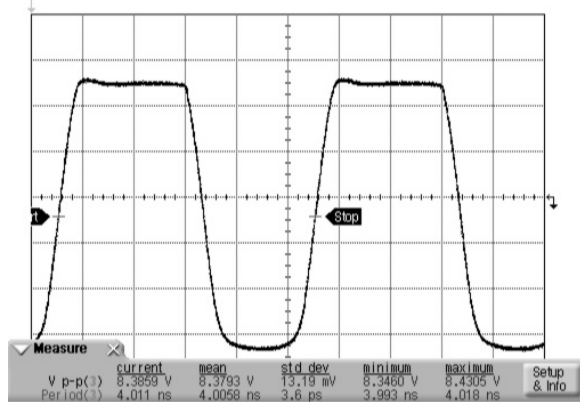


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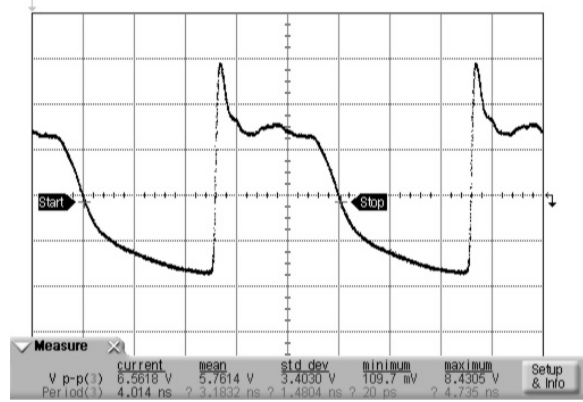


+15dBm 250MHz Sine Wave into ADM1-0026PA

Out of ADM1-0026PA (Into NLTL)

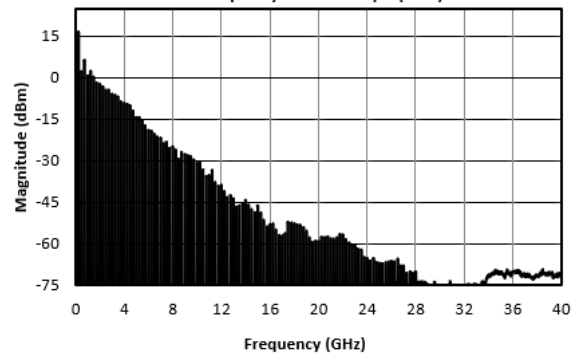


Out of NLTL



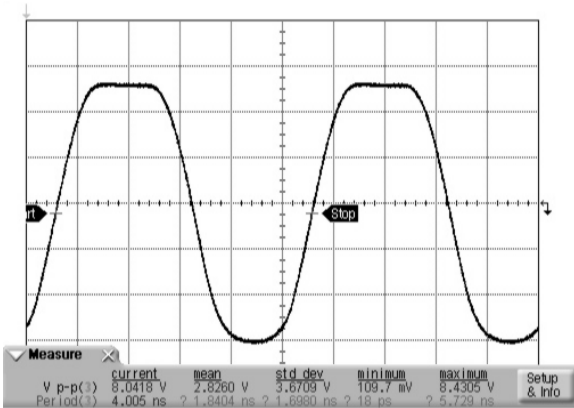
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+15dBm 250MHz into ADM1-0026PA
Frequency Domain Output(dBm)

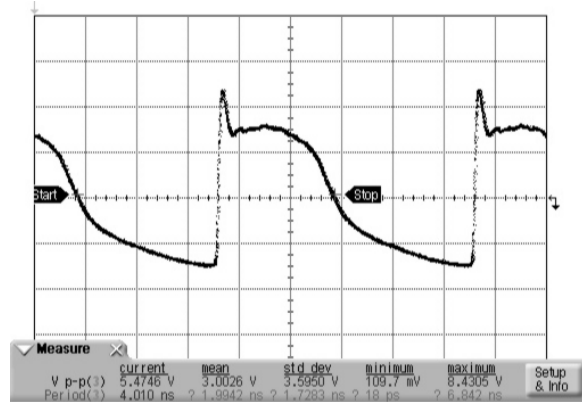


+10dBm 250MHz Sine Wave into ADM1-0026PA

Out of ADM1-0026PA (Into NLTL)

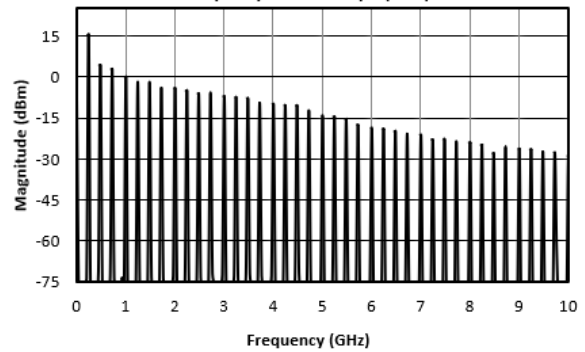


Out of NLTL



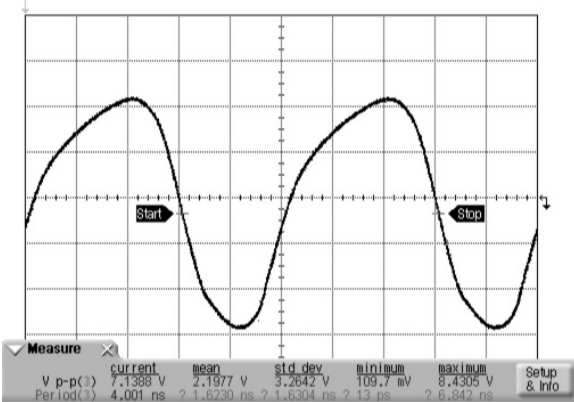
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+10dBm 250MHz into ADM1-0026PA
Frequency Domain Output(dBm)

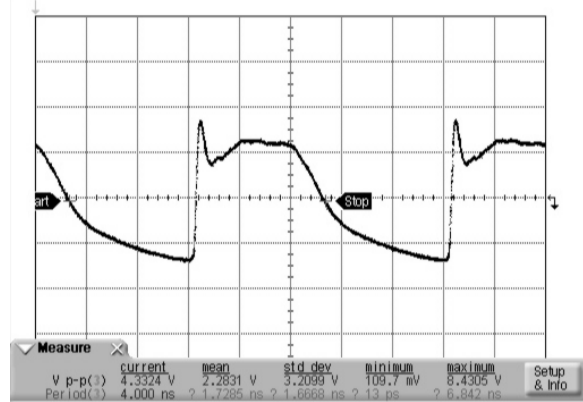


+7dBm 250MHz Sine Wave into APM-7098PA

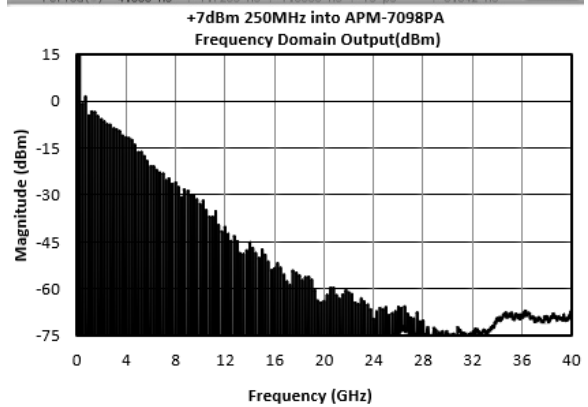
Out of APM-7098PA (Into NLTL)



Out of NLTL

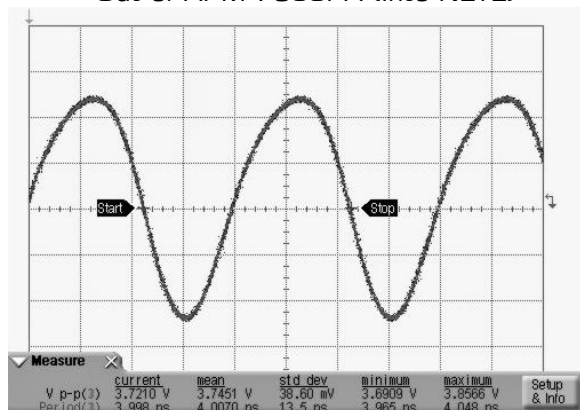


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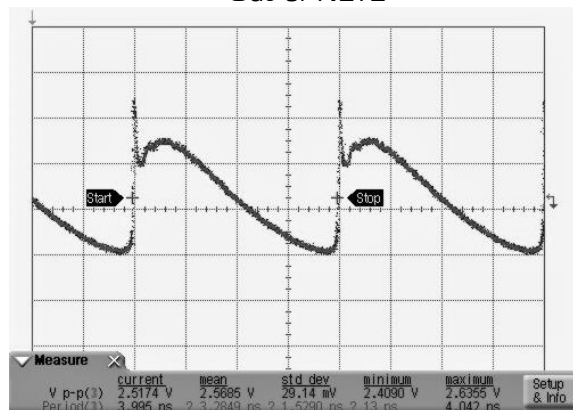


+0dBm 250MHz Sine Wave into APM-7098PA

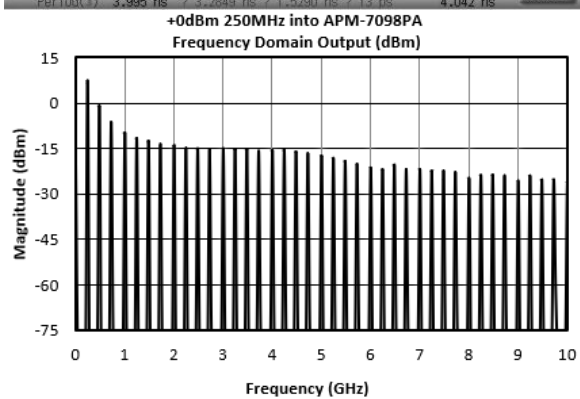
Out of APM-7098PA (Into NLTL)



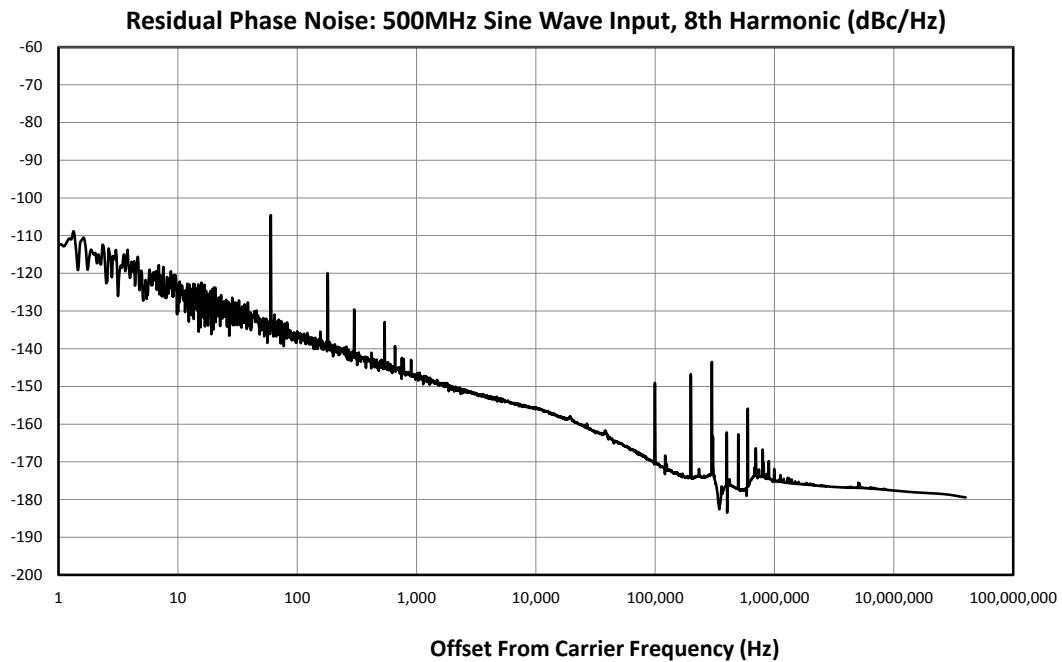
Out of NLTL



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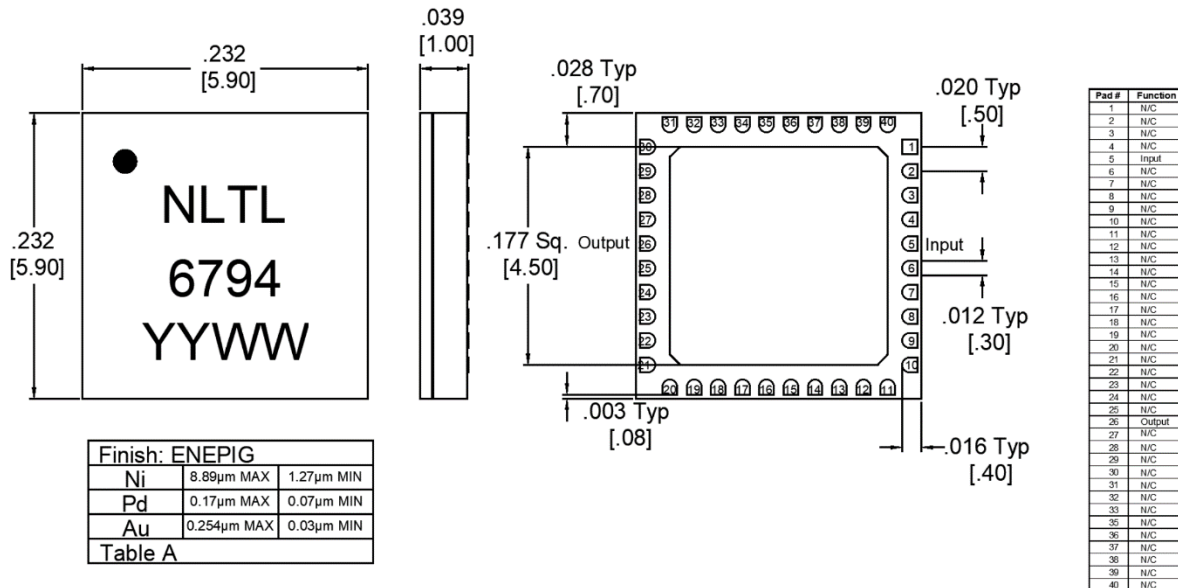
4.6.8 Typical Performance Plots: Residual Phase Noise



500 MHz, +23 dBm Sine Wave Input	Parameter	Min	Typical	Max	Units
8 th Output Harmonic	1 Hz Offset		-112		dBc/Hz
	10 Hz Offset		-125		
	100 Hz Offset		-135		
	1 KHz Offset		-147		
	10 KHz Offset		-155		
	100 KHz Offset		-170		
	1 MHz Offset		Thermal Floor		

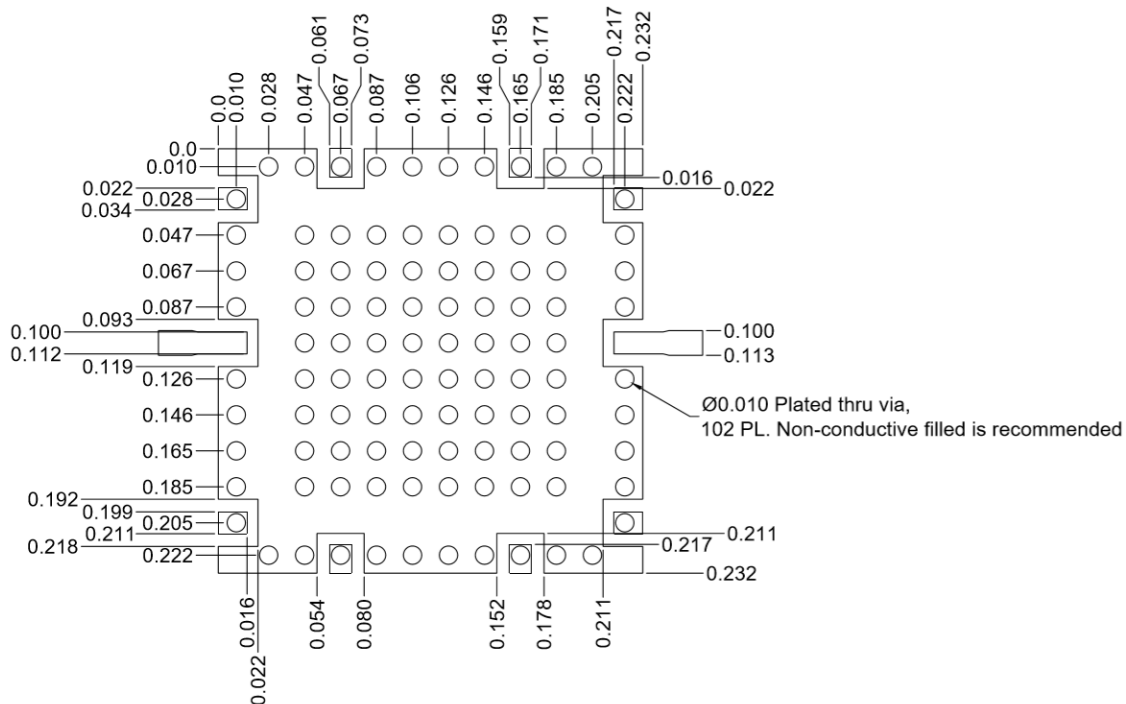
5. Mechanical Data

5.1 SM Package Outline Drawing



1. Substrate material is Ceramic.
2. All unconnected pins should be connected to PCB RF ground.

5.2 SM Package Footprint

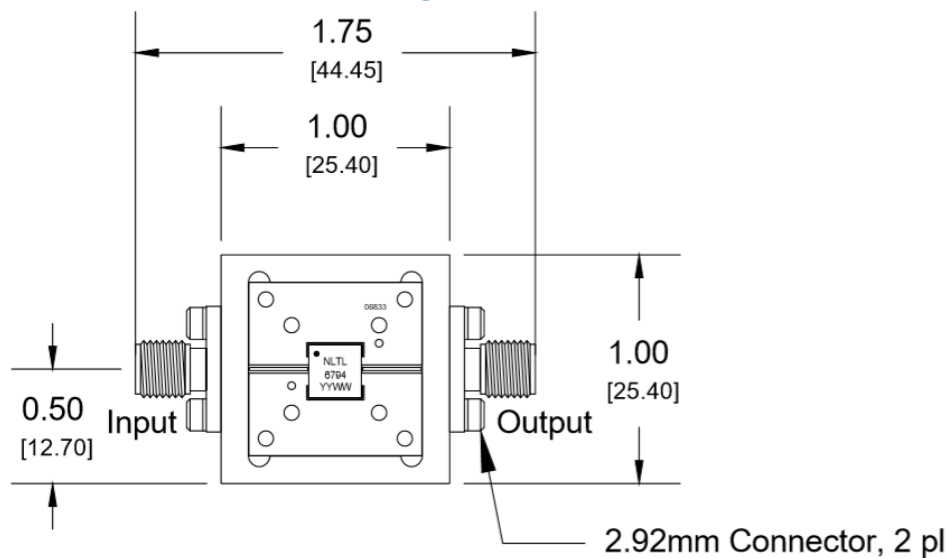


QFN-Package Surface-Mount Landing Pattern

[Click here for a DXF of the above layout.](#)

[Click here for leaded solder reflow.](#) [Click here for lead-free solder reflow](#)

5.3 Evaluation Board Outline Drawing



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