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Compact, four-quadrant lock-in amplifier generates two analog outputs

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The circuit in this Design Idea realizes a simple, low-cost lock-in amplifier employing an Analog Devices (www.analog.com) AD630 balanced modulator-demodulator IC (**Reference 1**). The device uses laser-trimmed thin-film resistors, yielding accuracy and stability and, thus, a flexible commutation architecture. It finds use in sophisticated signal-processing applications, including synchronous detection. The amplifier can detect a weak ac signal even in the presence of noise sources of much greater amplitude when you know the signal's frequency and phase.

As an analog multiplier, the AD630 reveals the component of the input-voltage signal in a narrow band around the frequency of the reference signal. The lowpass filter at the AD630's output allows you to gain information on the weak signal amplitude, which the uncorrelated noise originally masked. When the input voltage and the reference voltage are in phase, the lowpass filter's output, V_{OUT}, assumes the maximum amplitude. Conversely, if the input voltage and the reference voltage are in quadrature, the output voltage would ideally be 0V. In this way, if both in-phase and quadrature reference signals are available, two balanced demodulators reveal the in-phase output voltage to be 0° and the in-quadrature output voltage to be 90°. You can calculate the module and phase shift as follows:

$$|V_{OUT}| = \sqrt{V_{OUT0°}^2 + V_{OUT90°}^2};$$

$$\angle V_{OUT} = \tan^{-1}\left(\frac{V_{OUT90°}}{V_{OUT0°}}\right).$$

The two AD630s have a gain of ±2 and receive the amplified signal, V_{IN}, through two identical amplifiers, A_1 and A_2. At Pin 7 of IC_1, a bipolar ±5V squared signal appears in phase with

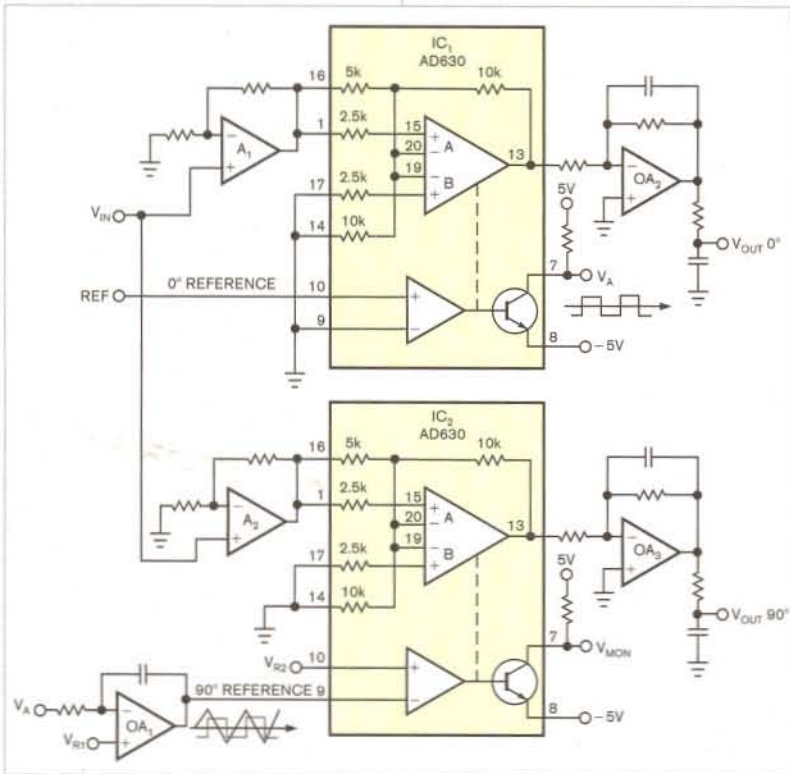

Figure 1 OA_1 integrates the bipolar V_A signal and creates a triangular wave. V_{R1} and V_{R2} obtain a 90°-shifted reference voltage with respect to V_A.

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the reference signal. OA_1 integrates the amplifier voltage, which generates a triangular wave that IC_2's comparator compares with the V_{R2} voltage. You must regulate V_{R1} and V_{R2} to obtain a perfect 90°-shifted command for IC_2. You can monitor the voltage at IC_2's Pin 7. Measurement accuracy and repeatability depend strongly on the RC time constant of the integrator and the values of V_{R1} and V_{R2}.

You can use a different approach to generate in-phase and in-quadrature reference signals. **Figure 2** shows an all-digital circuit, which you can implement in a small CPLD (complex programmable-logic device) to generate the 0 and 90° reference signals in **Figure 1**. Counter 1 measures the reference-signal time in terms of the N number of digital clock pulses, where the reference time can be different from 50%. It receives a preset command at the $N_1=1$ value at each positive front edge of the reference signal. D-type flip-flop IC_1 generates such pulses. At each positive edge of the reference signal, IC_2 acquires the N/4 value. Meanwhile, Counter 2 counts the clock periods and receives a restart command at the $N_2=1$ value when its value reaches the comparator-measured N/4 quantity.

AN INCREASE IN THE NUMBER OF BITS DECREASES THE MAXIMUM REFERENCE FREQUENCY.

To overcome the lack of the last EQ signal when the reference time is greater than approximately four times the N/4 integer value, the OR combination of the two RST and EQ pulses yields four almost-equidistant positive-edge commands in each reference-time period. The N/4 integer division, a logical right shift by 2 bits of N_1, gives a maximum error of three on the last pulse position. These pulses generate the in-phase and in-quadrature signals, 0 and 90°, respectively, resulting from simple commutations on the positive or negative edges of the signal. T-type flip-flop IC_3 generates a signal with twice the frequency of the reference signal. In this way, the accuracy is equal to $3/N_1$.

To maintain accuracy at least comparable with that of the AD630, the N_1 output of Counter 1 would be the highest. However, an increase in the number of bits decreases the maximum reference frequency for a given digital-clock frequency if you want N_1 to reach high values. For example, if N is 15 bits, the N_1 output assumes the 32,767 maximum value with an accuracy of approximately 0.01%. If the reference-time period decreases, you can assume a minimum value of 3277—that is, one-tenth of the maximum value—for N_1, with a correspondingly lower accuracy of 0.1%, which is comparable to the gain accuracy of the AD630. To increase the reference frequency, divide the digital clock's frequency to select low values when the reference time becomes too long. EDN

REFERENCE

1 "AD630 Balanced Modulator/Demodulator," Revision E, Analog Devices, 2004, www.analog.com/static/imported-files/data_sheets/AD630.pdf.

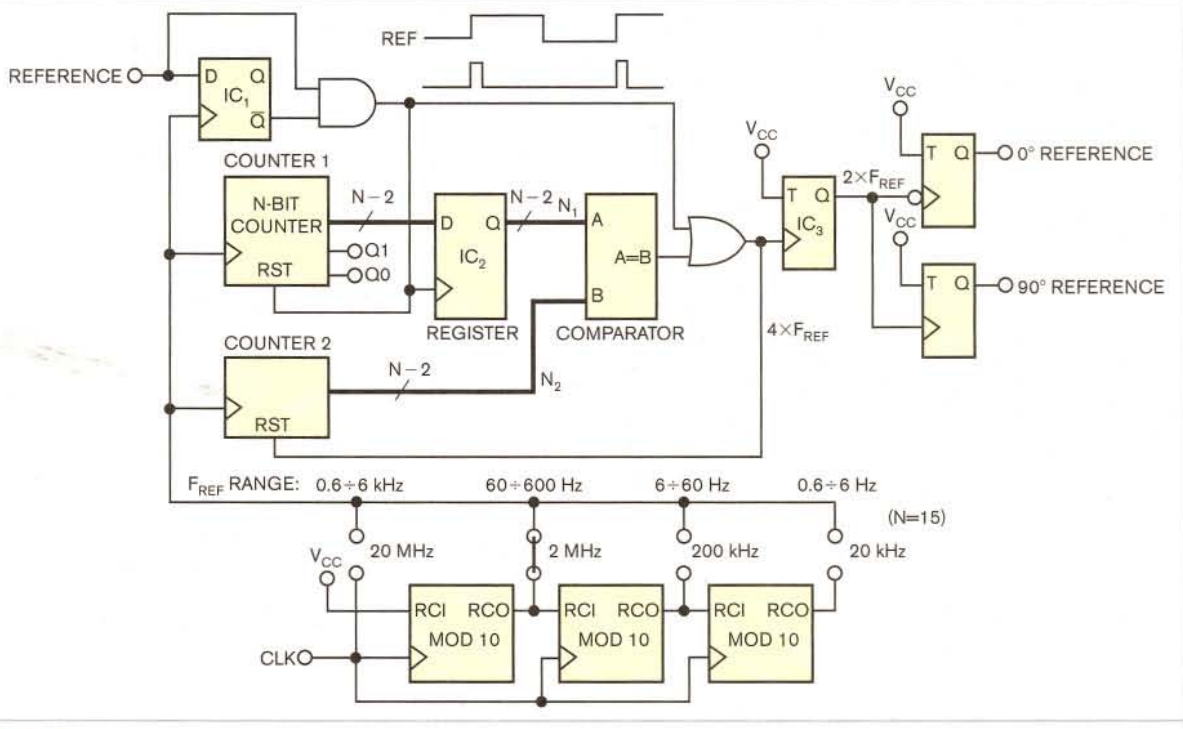

Figure 2 You can implement this all-digital circuit in a small CPLD.