Pulsed RF Circuits for Ultra Wideband Communications and Radar Applications

by

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Abstract

This thesis explores the design of fast-settling pulse generators and pulsed low noise amplifiers (LNAs) for Ultra-Wideband (UWB) applications. These components are critical in pulsed UWB transceivers, and a high energy efficiency is sought without adversely affecting RF performance and functionality. To this end, new pulse generators with a subnanosecond settling time and a low energy consumption of only a few picojoules per pulse are targeted. Moreover, a novel pulsed LNA is investigated for a low power consumption that can be scaled with the duty cycle.

First, an energy-efficient tunable pulse generator is proposed for high-data-rate 3.1-10.6 GHz UWB applications. A current-starved ring oscillator is quickly switched on and off, and the amplitude envelope is shaped using a passive attenuator. The energy consumption per pulse is below 4.2 pJ while the pulse amplitude is 150 mV, yielding a high energy efficiency.

A quadrature pulse generator is then presented for 22-29 GHz UWB applications with a settling time below 0.5 ns. An inductor-capacitor (LC) oscillator is quickly switched on and off with a new technique, and the amplitude envelope is shaped using a variable passive attenuator. The energy consumption per pulse is only 6.2 pJ, and the pulse amplitude is more than 240 mV, yielding the highest energy efficiency reported to date in CMOS.

Next, a 3–10 GHz pulsed ring oscillator that offers direct quadrature phase modulation is demonstrated. Current impulses are injected into the oscillator to enable fast startup and implement quadrature phase modulation. The energy consumption and voltage swing varies from 13 pJ and 300 mV at 3 GHz to 18 pJ and 200 mV at 10 GHz respectively, yielding a high energy efficiency.

Lastly, a fast switching noise cancelling LNA is proposed for 3.1-10.6 GHz UWB applications that settles within 1.3 ns for switching speeds as high as 200 MHz. Inductive peaking is introduced in the noise cancelling topology to achieve a sub-4dB flat noise figure and a high gain of 16.6 dB for frequencies up to 10 GHz. The average power consumption is also below 10 mW with a 50% duty cycle clock.

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Table of Contents

List of Tables

List of Figures

List of Abbreviations

AC Alternating Current.

ACC Active Cruise Control.

ADC Analog-to-Digital Converter.

BiCMOS Bipolar and CMOS.

BPF Bandpass Filter.

BPG Baseband Pulse Generator.

BPSK Binary Phase Shift Keying.

CML Current Mode Logic.

CMOS Complimentary Metal Oxide Semiconductor.

CPW Coplanar Waveguide.

DA Driver Amplifier.

DAC Digital-to-Analog Converter.

DC Direct.

DSA Digital Serial Analyzer.

DWG Distributed Waveform Generator.

EM Electromagnetic.

FCC Federal Communications Commission.

FF Fast-Fast.

FOM Figure of Merit.

GaAs Gallium Arsenide.

GPS Global Positioning System.

IC Integrated Circuit.

InP Indium Phosphide.

IR Infrared.

LC Inductor-Capacitor.

LHS Latin Hypercube Sampling.

LNA Low Noise Amplifier.

LO Local Oscillator.

LPF Low-Pass Filter.

MESFET Metal Semiconductor Field Effect Transistor.

MIM Metal-Insulator-Metal.

NF Noise Figure.

NMOS N-channel Metal Oxide Semiconductor Field-Effect Transistor.

OOK On-Off Keying.

PA Power Amplifier.

PCS Personal Communications Service.

PEG Pseudo-Gaussian Envelope Generator.

PLL Phase-Locked Loop.

PMOS P-channel Metal Oxide Semiconductor Field-Effect Transistor.

PN Phase Noise.

PPM Pulse Position Modulation.

PRF Pulse Repetition Frequency.

PRT Pulse Repetition Time.

PSD Power Spectral Density.

PVT Process-Voltage-Temperature.

Q Quality factor.

RC Resistor-Capacitor.

RCS Radar Cross Section.

RF Radio Frequency.

RMS Root Mean Square.

S-parameter Scattering parameter.

SiGe Silicon Germanium.

SoC System-on-Chip.

SRD Step Recovery Diode.

SS Slow-Slow.

TT Typical-Typical.

UWB Ultra-Wideband.

VCO Voltage Controlled Oscillator.

VGA Variable Gain Amplifier.

VNA Vector Network Analyzer.

Chapter 1

Introduction

1.1 Pulsed Ultra-Wideband Technology

Ultra-Wideband (UWB) systems, which are regulated by the Federal Communications Commission (FCC) for commercial use in the 3.1 GHz to 10.6 GHz frequency band, are promising for short-range wireless data communication, imaging and high-precision ranging applications. The FCC defines an UWB device as having a –10 dB bandwidth of at least 500 MHz or more than 20% of the centre frequency [1]. The power spectral density (PSD) at the output of the transmit antenna is limited to less than –41 dBm/MHz as shown in Fig. 1.1 [1]. This spectral mask allows UWB devices to coexist with existing narrowband systems, ensuring sufficient attenuation to prevent adjacent channel interference. In particular, tight limits have been imposed below 2 GHz to help protect critical, sensitive applications such as global positioning systems (GPS) at 1.5 GHz and digital cellular personal communications services (PCS) at 1.9 GHz.

The frequency spectrum from 22 GHz to 29 GHz was also made available by the

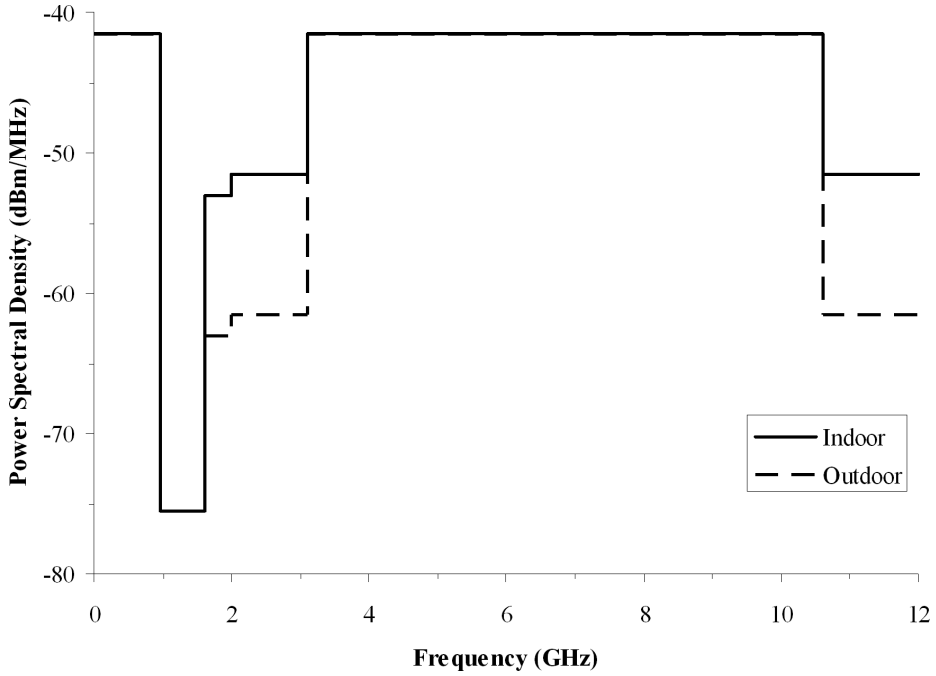


Figure 1.1: FCC UWB spectral mask for indoor and outdoor systems.

FCC for short-range radar (SRR) systems on terrestrial transportation vehicles [1]. Normally, the average PSD should not exceed –41.3dBm/MHz as shown in Fig. 1.2 to avoid interference [1]. UWB SRR is considered a key element in comprehensive environment sensing for automobiles, complementing other technologies such as infrared (IR), ultrasonic, video and long-range Active Cruise Control (ACC) radars as shown in Fig. 1.3 [2]. It is less susceptible to inclement weather and harsh environmental conditions compared to the other technologies, and offers a stylistic advantage to vehicle manufacturers as sensors can be readily mounted behind a plastic bumper which is nearly transparent to the radar signal without requiring custom cutouts or similar accommodations. A network of 16 or more UWB radar sensors around the vehicle [3] can provide a variety of features to improve passenger safety, ranging from simple parking aids to more sophisticated blind-spot monitoring, pre-crash detection and

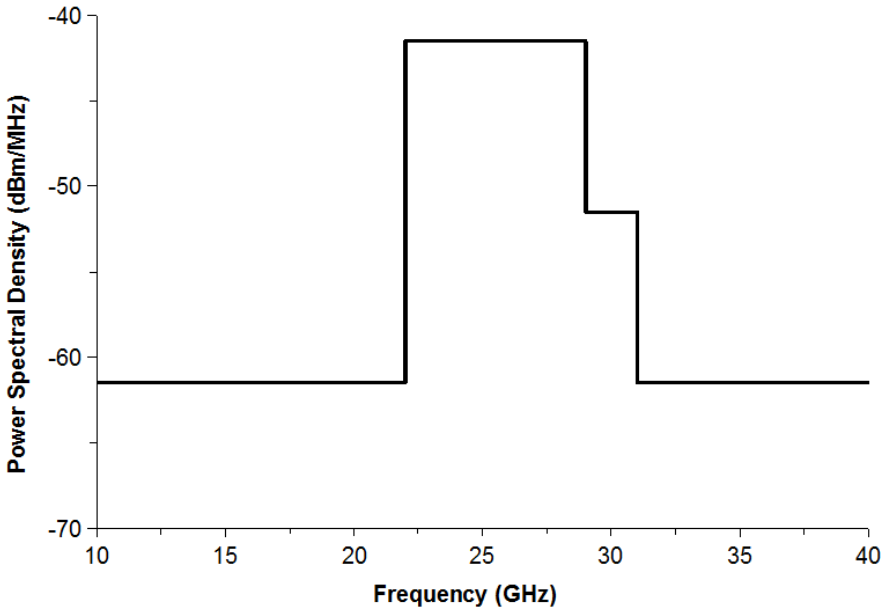


Figure 1.2: FCC UWB spectral mask for vehicular radar systems.

stop-and-go or short-range cruise control. Such applications require a high resolution of about 10 cm. Increasing the number of radar sensors can increase the processing capability and reliability of the SRR system.

Pulsed UWB technology is based on the transmission of pulses that have a very short time duration, on the order of a nanosecond or sub-nanosecond, thereby spreading the radio signal power over a wide bandwidth. It potentially offers high time and range resolution, reduced multipath fading, low power and complexity, high data rates and low probability of undesired detection and interception. Energy-efficient and low-cost pulsed UWB transceivers [4] are attractive for wireless communication and biomedical applications such as wireless personal and sensor networks [5–16], interchip communications [17–20] and UWB biotelemetry [21–23].

From a radar perspective, pulsed UWB techniques potentially offer high range

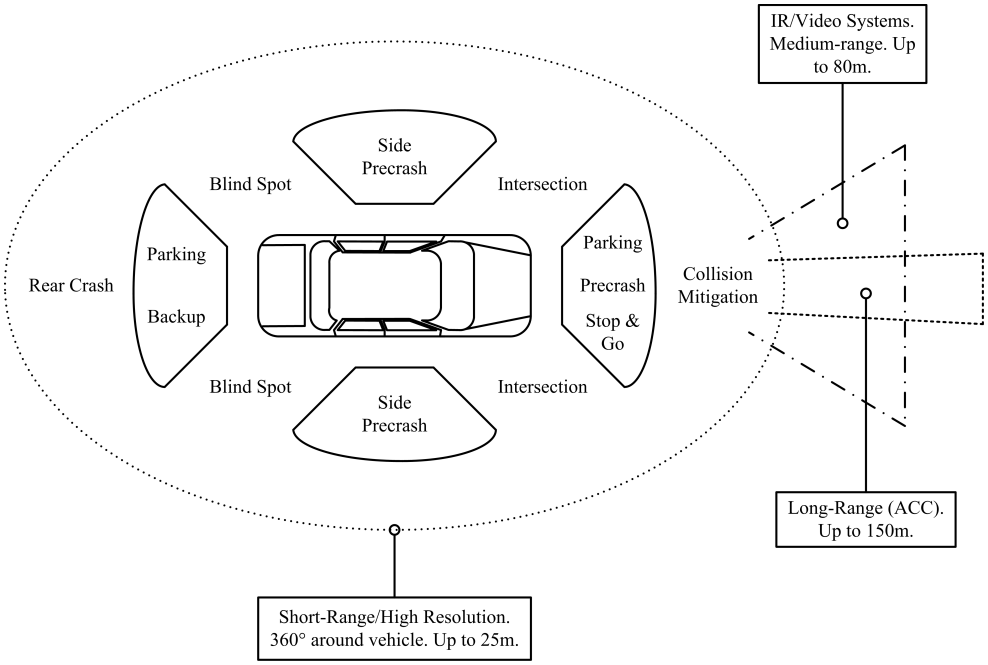


Figure 1.3: Complete environment sensing for automobiles. Short-range radar provides a variety of applications.

measurement accuracy and range resolution, enhanced target radar cross section (RCS) and identification, increased immunity to passive interference (e.g. rain), and the ability to detect very slowly moving targets [24–26]. Their transceiver architecture is also one of the simplest to implement, potentially making them very cost-effective. Furthermore, time-gating can increase isolation between the transmitter and receiver for a longer operating range, and low duty cycling can significantly reduce the power consumption [2, 27–32].

1.2 Pulsed UWB Transceiver Architecture

Direct-conversion architectures are used in pulsed UWB transceivers as opposed to the conventional heterodyne approach. The transceiver architecture is thus relatively

simple compared to that of other wireless technologies, offering significant cost and power savings. It can also be entirely integrated in CMOS for a System-on-Chip (SoC) solution.

Fig. 1.4 shows a block diagram of a commonly used architecture for pulsed UWB transceivers. The transmitter is simply accomplished by using a pulse generator, a pulse modulator, and a driver amplifier (DA). Sub-nanosecond pulses are generated and modulated by the binary data or code before being amplified (if required) and emitted. Pulse formation is typically achieved by time gating the output of the local oscillator (LO) for the duration of the pulse. The length and bandwidth of the transmitted pulse can be varied by manipulating the length of the switching control signal. Commonly used modulation schemes are binary phase shift keying (BPSK), on-off keying (OOK) and pulse position modulation (PPM). The low complexity of the transmitter lends itself particularly well to wireless sensor networks, where the sensors usually have a tight power budget and can operate solely as a transmitter in many applications.

The pulsed UWB receiver usually consists of a wideband low noise amplifier (LNA), a multiplier, a variable gain amplifier (VGA), a low-pass filter (LPF) and an analog-to-digital converter (ADC). The received weak pulse sequence is first amplified by the LNA while adding as little noise as possible. Pulse correlation for optimum detection is performed by multiplying the incident signal with locally-generated template pulses and integrating the result using the multiplier and LPF respectively. By performing the pulse correlation in the analog domain, the complexity and power consumption of the ADC and the digital backend can be reduced as the required sampling speed is minimized to the pulse rate [2, 33]. Quadrature correlation with

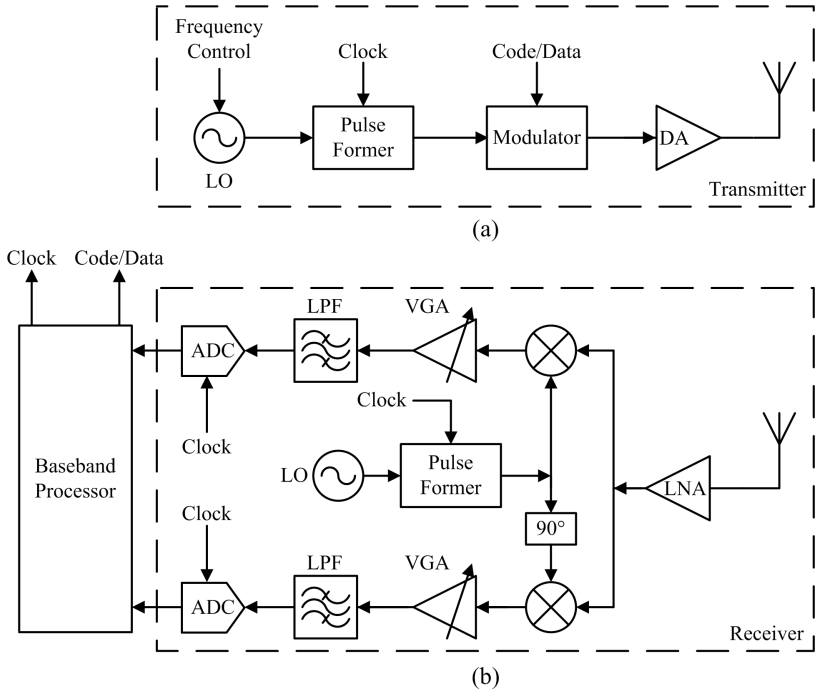


Figure 1.4: Pulsed UWB transceiver architecture: (a) Transmitter and (b) Receiver.

in-phase and quadrature-phase channels is typically employed to extract complete information from the received signal including phase and Doppler information [2, 3]. The quadrature projection can also facilitate signal tracking and synchronization [34].

1.3 Motivation

UWB pulse generation is the most critical function in pulsed UWB transceivers, significantly affecting the overall performance of the UWB system. First, the time duration and frequency bandwidth of the generated UWB pulse specifies the range measurement accuracy, multipath resolution and data rate that can be achieved by the UWB system. The pulse shaping properties of the pulse generator also play a major role in specifying the characteristics of the emitted PSD and whether it

complies with the FCC mask. In addition, the tunability provided by the pulse generator for different pulse shapes and frequency spectra allows the transceiver to be robust against process variations, regulatory differences, interference and changes in the channel or antenna characteristics, which is important for practical systems. Furthermore, built-in modulation capability in the pulse generator would eliminate the need for a wideband modulator and simplify the transmitter architecture as much as possible. The wide signal bandwidth, complex pulse shaping, reconfigurability and modulation capability required in the pulse generator make it one of the most challenging components to design. These requirements typically result in high power consumption and high circuit complexity (i.e. cost).

One of the most important performance parameters for pulse generators is the amount of energy consumed per pulse, which is suitable for capturing the intermittent nature of pulsed UWB. The energy consumption per pulse (E_p) is defined as:

$$E_p = P_{AVG} \times PRT = P_{AVG}/PRF \tag{1.1}$$

where P_{AVG} is the average power consumption, PRT is the pulse repetition time and PRF is the pulse repetition frequency. The energy efficiency of the pulse generator is directly related to its energy consumption per pulse E_p. A commonly used formula for the energy efficiency η is given by:

$$\eta = E_p/V_{pp} \tag{1.2}$$

where V_{pp} is the peak-to-peak voltage amplitude of the generated UWB pulse.

Pulses are typically generated in pulsed UWB transceivers by first forming an

impulse at baseband and then upconverting it to the target UWB frequency band [15, 30–32, 35, 36]. The upconversion may be performed by using a switch instead of an explicit mixer. This technique offers precise control and diversity over the generated pulse frequency spectrum, but at the cost of high power consumption due to the use of a continuously running high-frequency local oscillator (LO) phase-locked loop (PLL). In addition, the power consumption of the LO PLL does not scale with the pulse repetition frequency, causing the energy consumption per pulse to increase significantly as the pulse repetition frequency is reduced. Another problem of this approach is the LO signal leakage that occurs due to the finite isolation between ports of the mixer or switch. This gives rise to an LO spike appearing at the center of the generated spectrum, which reduces the power spectral efficiency and the maximum pulse power level that can be transmitted within the FCC mask. The transmitted LO leakage can also cause significant interference. Similarly, LO feedthrough between ports in the multiplier on the receiver side also leads to LO self-mixing which induces a DC offset that corrupts the pulse detection process. Switched or gated local oscillators have been investigated to reduce the circuit complexity, power consumption and LO leakage [13, 14]. Nevertheless, they can have a relatively long stabilization time which limits the pulse bandwidth and energy efficiency. In addition, there is little control over the startup and turn off transients of the oscillator, and the output pulse shape cannot be readily tuned. Furthermore, they do not provide quadrature outputs or phase modulation capability.

The LNA is a crucial component in the receiver front-end, with its performance being a major bottleneck in the overall performance of the UWB system. Since the LNA is the first component in the receiver chain, its contribution to the overall noise

performance of the receiver is the most significant. The Friis equation indicates that the noise added by the LNA and thus its noise figure (NF) directly appear in the total NF of the receiver. In addition, the gain provided by the LNA reduces the noise contribution of the following stages in the total NF. The NF of the receiver dictates its sensitivity, which is a measure of the minimum signal power that can be detected by it. This in turn affects the operating range and/or the transmitter power. Thus the LNA NF and gain are critical performance parameters that need to be minimized and maximized respectively. To achieve this at high frequencies and over a wide bandwidth in UWB systems, the LNA consumes a significant amount of power and is quite complex. In fact, the UWB LNA typically consumes the most power in the UWB receiver front-end.

Several broadband amplifier topologies have been used for UWB low noise amplification, the most common of which are the resistive feedback amplifier and the distributed or travelling wave amplifier [37–41]. Both types of amplifiers can consume a significant amount of power to simultaneously achieve a low NF, a high gain and a good input impedance match over a wide range of frequencies for UWB applications. They can also suffer from instability or occupy a particularly large chip area respectively. Moreover, most if not all of the UWB LNAs reported in the literature are biased with a constant DC current, therefore their power consumption can not be scaled with the duty cycle to achieve significant power savings.

The UWB RF front-end is not required to operate continuously in pulsed UWB systems, but only when a pulse is being transmitted or received. This is also applicable to pulsed UWB radars, where a time-gated correlation is performed between the echo signal and the delayed replica of the transmitted pulse. By varying the time delay

between pulse transmission and correlation, it is possible to detect objects at varying distances (range gates) from the radar, with the shortest time delay corresponding to the closest range gate and the longest time delay corresponding to the farthest range gate [2]. Indeed, all circuits can be switched off between pulses for significant power savings that might not be possible otherwise to achieve a low energy consumption per pulse and a high energy efficiency. For example, for a transmitted pulse of 500 ps duration and a PRF of 500 MHz, a power reduction of up to 75% can be achieved if the frontend blocks can be turned on only during the pulse time. Furthermore, LO leakage, DC offsets and interference can be reduced, if not eliminated, while the isolation between components is increased. Such duty-cycled operation however requires fast-settling pulsed RF circuits. To this end, pulse generators and pulsed low noise amplifiers are proposed in this thesis that can settle within one nanosecond. These components are the most critical in pulsed UWB transceivers and as such are the focus of this thesis. The main goal of this work is to achieve a high energy efficiency without adversely degrading RF performance and desired functionality, including the pulse bandwidth and tunability for pulse generators, and the NF and gain for low noise amplifiers.

1.4 Thesis Contributions

In this thesis, new pulse generators with a settling time of less than one nanosecond and a low energy consumption of only a few picojoules per pulse are developed for a high energy efficiency. The proposed pulse generators feature a high pulse bandwidth, high versatility and support for quadrature phase modulation. In addition, a pulsed low noise amplifier is investigated for a low power consumption that can be scaled

with the duty cycle. Novel, fast power switching is introduced for a short settling time without adversely affecting critical parameters such as the NF and gain. In particular, the main contributions of this thesis are as follows:

- The first 24 GHz quadrature pulse generator presented in CMOS technology for 22-29 GHz UWB applications with a settling time below 0.5 ns. The energy consumption is only 6.2 pJ per pulse, and the pulse amplitude is 240 mV, yielding the highest energy efficiency reported to date in CMOS. Furthermore, the pulse width can be tuned to be as short as 375 ps (Chapter 4) [42].

- The first tunable 3–10 GHz quadrature pulsed oscillator demonstrated in CMOS technology that offers quadrature phase modulation, with a settling time well within one nanosecond. The energy consumption per pulse varies from 13 pJ at 3 GHz to 18 pJ at 10 GHz, while the output voltage swing varies from 300 mV to 200 mV, yielding a high energy efficiency (Chapter 5) [43].

- A new tunable pulse generator for high-data-rate 3.1-10.6 GHz UWB applications that achieves a low energy consumption of less than 4.2 pJ per pulse at a pulse repetition frequency of 900 MHz. The output voltage amplitude is about 150 mV yielding a high energy efficiency (Chapter 3) [44].

- A novel fast switching noise cancelling LNA for 3.1-10.6 GHz UWB applications that can settle within 1.3 ns for switching speeds as high as 200 MHz. To the author's best knowledge, this is the shortest settling time reported to date. The power consumption is also below 10 mW at 50% duty cycle (Chapter 6) [45].

1.5 Thesis Organization

This thesis is organized topically by chapter. After a literature review, each chapter describes one of the proposed pulsed RF circuits for UWB communications and radar applications, with a summary given in the last chapter.

A brief study and literature review of UWB pulse generators is first conducted in Chapter 2 that allows the contributions of this thesis to be placed into context. In Chapter 3, an energy-efficient tunable pulse generator is demonstrated for high-data-rate 3.1–10.6 GHz UWB applications. A current-starved ring oscillator is quickly switched on and off over the pulse duration, and the amplitude envelope is shaped using a variable passive attenuator. The attenuator is controlled with an impulse which is created by a low-power, tunable glitch generator. The ring oscillator is optimized to generate the desired oscillation frequency with the lowest power consumption, and the variable attenuator is analyzed to achieve more than 20 dB of out-of-band rejection. Several UWB pulses were measured and presented, with the pulse time duration varying over a wide range. The spectrum roll-off is also quite sharp with high out-of-band rejection to help satisfy the FCC mask. The entire circuit operates in switched-mode with a very low average power consumption and a high energy efficiency. The inductorless design is also fairly compact.

Chapter 4 presents a quadrature tunable pulse generator for 22–29 GHz UWB applications in 130 nm CMOS. A quadrature inductor-capacitor (LC) oscillator is switched on and off for the pulse duration, and the amplitude envelope is shaped using a variable passive attenuator. By switching on one side of each differential oscillator just before the other, a current impulse with a short time duration and large harmonic components out to 24 GHz can be injected, creating a large initial

condition for fast startup and setting the initial phase of the oscillations for high pulse-to-pulse coherence. The attenuator is controlled with an impulse which is created by a digital, tunable glitch generator. The entire circuit operates in switched-mode with a low average power consumption and a high energy efficiency. Several UWB pulses are measured and demonstrated, with the pulse time duration and frequency bandwidth varying over a wide range. The output power levels, frequency tuning range and locking bandwidth of the oscillator were also characterized.

Chapter 5 explores a quadrature pulsed oscillator with quadrature phase modulation for 3.1–10.6 GHz UWB applications. It can be used to provide template pulses for quadrature pulse correlation and/or support binary and quadrature phase modulation. A two-stage CMOS ring oscillator with shunt-shunt resistive feedback is investigated to achieve a wide tuning range. Current impulses are injected into the oscillator to enable fast oscillation startup (within one nanosecond) and to specify the phase of the oscillations. Direct quadrature phase modulation is thus made possible by manipulating the directions of these current impulses. A mathematical model of the oscillator is analyzed to explain the effects of shunt-shunt resistive feedback and to illustrate the quadrature phase modulation feature. The oscillator is completely switched off between pulses for a low power consumption and a high energy efficiency. The inductorless design is also very compact. Measurement results are shown for the quadrature pulsed oscillator including the output power levels, frequency spectra, phase noise and time-domain waveforms.

In Chapter 6, a fast switching noise cancelling low noise amplifier (LNA) is investigated for 3.1–10.6 GHz UWB applications. A noise cancelling technique with inductive degeneration and series inductive peaking is introduced to simultaneously

achieve a flat sub-4dB noise figure (NF) and a good impedance match for frequencies up to 10 GHz. A second amplification stage is added (AC coupled) to increase the gain to more than 16 dB and provide an output impedance match from 3 GHz to 10 GHz. Fast switching can only be achieved by bypassing the large DC bias resistors that lead to long charging time constants. This is performed by adding switches in parallel to the DC bias resistors, which are activated only for a short time period (0.8 ns) after startup. The output voltage amplitude can thus settle within 1.3 ns for fast switching speeds of up to 200 MHz. Measurement results are shown for the LNA including S-parameters, noise figure, and group delay. The phase noise and jitter added by the switched LNA were also characterized. The circuit consumes less than 10 mW of average power with a 50% duty-cycle clock.

Chapter 7 concludes the thesis with a summary of the performance features and benefits offered by the proposed pulsed RF circuits. Recommendations for additional enhancements and feature extensions of the proposed circuits are also given for future work.

Chapter 2

Literature Review

2.1 Introduction

Sub-nanosecond pulse generation is a critical function in UWB transceivers and poses some serious challenges in circuit design. In addition to the wide signal bandwidth required, low power consumption and low complexity (for low cost) are necessary. A pulse generator should also be reconfigurable for different pulse shapes and spectra to provide more flexibility and to handle process variations, regulatory differences, and changes in the channel or antenna characteristics. Furthermore built-in modulation capability is usually desirable to further simplify the transceiver architecture for lower power consumption and cost.

The low noise amplifier (LNA) is the most important component and the main performance bottleneck in UWB receiver front-ends, making its design a very challenging task with difficult tradeoffs involved. A low noise figure (NF) and a high gain are simultaneously required over a wide bandwidth, which causes the LNA to be the most power hungry component in UWB receiver front-ends. Yet low circuit

complexity is often necessary to reduce cost.

In this chapter, commonly used pulse shapes and generation techniques are first discussed, with a focus on CMOS implementation. This is followed by a brief overview of the circuit topologies employed for UWB low noise amplification, as reported in the recent literature.

2.2 UWB Pulse Shape Definitions

While the FCC has specified the frequency bandwidth and PSD of UWB devices, there are very few regulations (if any) on the characteristics of the time-domain waveform. Therefore there is flexibility in choosing the pulse waveform that best suits the application at hand, and the design of the UWB pulse generator can be tailored for a low hardware complexity and power consumption for example. The Gaussian pulse and its derivatives are the most common UWB pulse shapes reported in the literature. This is because they feature a sharper frequency roll-off and a higher out-of-band sidelobe rejection compared to other pulse shapes. The standard Gaussian pulse waveform is given by:

$$x(t) = \frac{A}{\sqrt{2\pi}\sigma} \exp -\frac{t^2}{2\sigma^2} \tag{2.1}$$

where A is a constant amplitude, and σ is the original Gaussian standard deviation. The first and second derivatives of the Gaussian pulse are widely known as the Gaussian monocycle and doublet respectively [46]:

$$x^{(1)}(t) = -\frac{At}{\sqrt{2\pi}\sigma^3} \exp -\frac{t^2}{2\sigma^2} \tag{2.2}$$

$$x^{(2)}(t) = -\frac{A}{\sqrt{2\pi}\sigma^3}\left(1 - \frac{t^2}{\sigma^2}\right)\exp -\frac{t^2}{2\sigma^2} \tag{2.3}$$

The Gaussian, monocycle and doublet pulse waveforms given by equations (2.1), (2.2) and (2.3) respectively are plotted in Fig. 2.1.

In general, the fourier transform ($X(f)$) and PSD ($P(f)$) of the nth-order derivative of the Gaussian waveform can be shown to be:

$$X(f) = A(j2\pi f)^n \exp -\frac{(2\pi f\sigma)^2}{2} \tag{2.4}$$

$$P(f) = A^2(2\pi f)^{2n} \exp -(2\pi f\sigma)^2 \tag{2.5}$$

This PSD depends highly on the values of n and σ, shifting to higher frequencies for larger n and smaller σ. This is clearly observed in (2.5) and in the peak emission (center) frequency f_m [46]:

$$f_m = \frac{\sqrt{n}}{2\pi\sigma} \tag{2.6}$$

The low- and high-frequency components also scale differently with n and σ [46, 47]. Ultimately one needs to take at least the fifth- or seventh-order derivative to fit the PSD in the indoor or outdoor FCC mask respectively (Fig. 1.1) without shifting the center frequency (i.e. modulating the pulse with a sinusoid) or performing additional filtering [46]. Fig. 2.2 shows the time-domain waveform and PSD of the fifth- and seventh-order derivatives of the Gaussian pulse, with σ chosen to be 51 ps and 65 ps respectively to satisfy the FCC mask at maximum bandwidth [46]. However a higher-order derivative typically increases the circuit complexity and can be more sensitive to process variations and component mismatches.

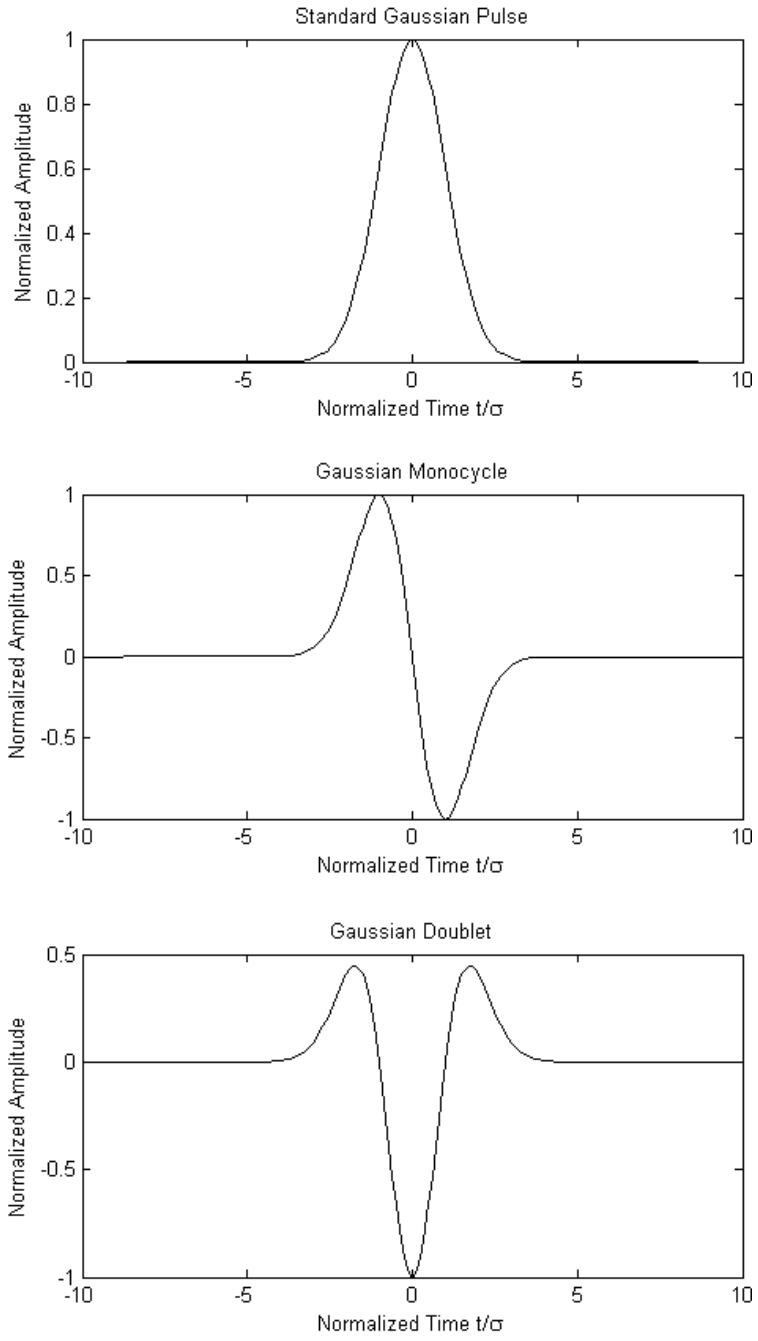


Figure 2.1: Gaussian-based pulse waveforms.

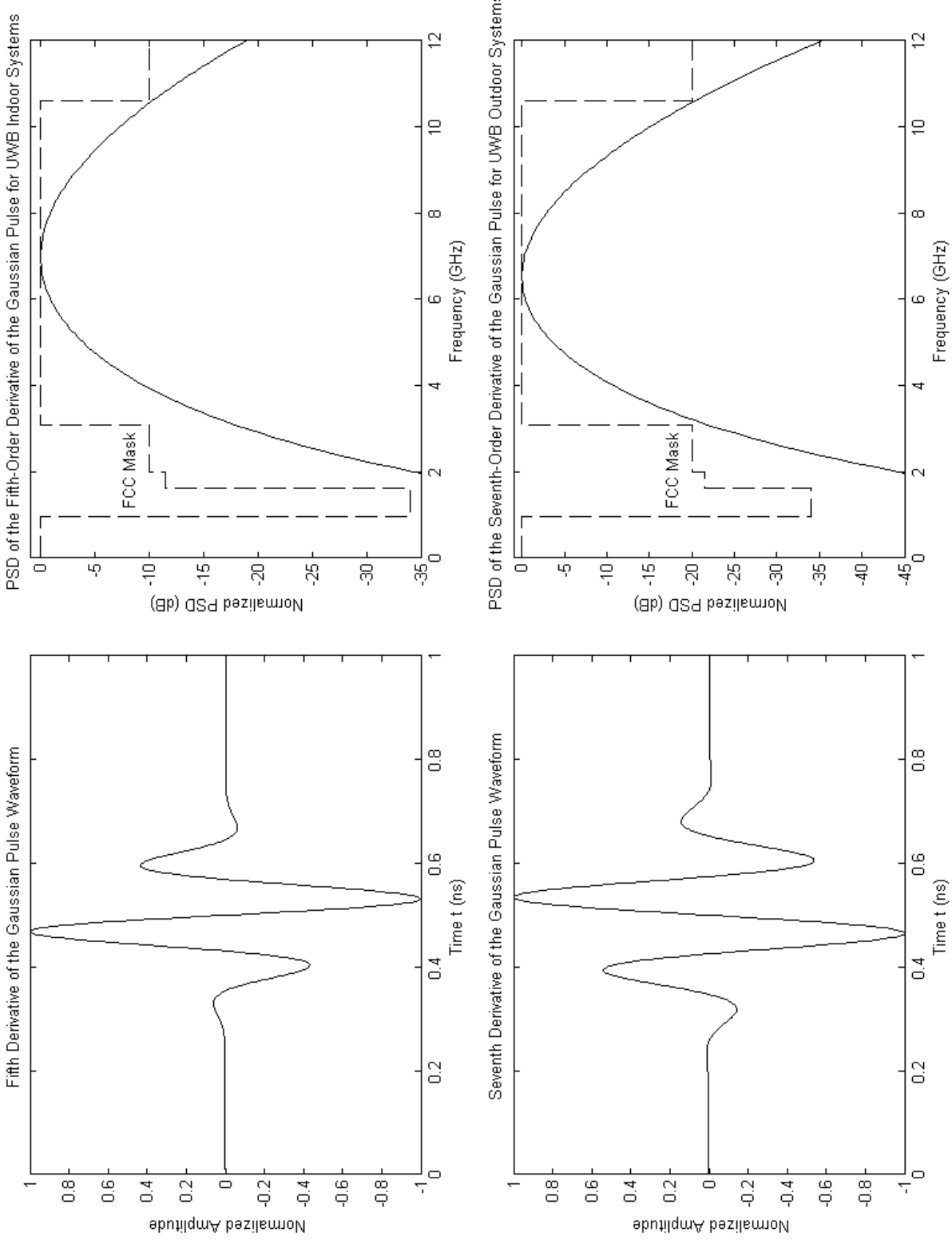


Figure 2.2: Time-domain waveforms and PSD of the fifth- and seventh-order derivatives of the Gaussian Pulse.

2.3 Ultra-Wideband Pulse Generation Techniques

2.3.1 Traditional Methods

Early techniques for generating Gaussian-based UWB pulses employed fast step generators and microwave transmission lines. A commonly used delay-type configuration is shown in Fig. 2.3. In [48], a square-wave oscillator is used to drive a fast-switching step recovery diode (SRD) and generate a fast-transition step signal. The SRD turns on during the positive half-cycle of the oscillator, storing some of the available charge. When the oscillator signal makes a transition into the negative half-cycle, the SRD discharges this energy and turns off abruptly, exciting the transmission lines with a fast-transition step signal. This step signal divides into two upon arriving at the junction between the main transmission line and the short-circuited stub: one propagating down the main transmission line towards the output and the other along the short-circuited stub. The one travelling towards the short circuit is reflected back with inverted polarity, eventually combining with the other step function to form a Gaussian impulse at the output. The short-circuit stub effectively acts as a delay line and the duration of the output pulse is thus approximately given by [48]:

$$\tau = \frac{2L_d}{v_p} \tag{2.7}$$

where L_d is the length of the short-circuit stub and v_p is the propagation velocity through it. Shorter stubs would create shorter delays and pulse durations. However excessive reduction of the stub length could reduce the pulse amplitude significantly, as the delay becomes too short compared to the rise time. With a pulse repetition frequency (PRF) of 10 MHz, this pulse generator can produce pulses with 154 ps time

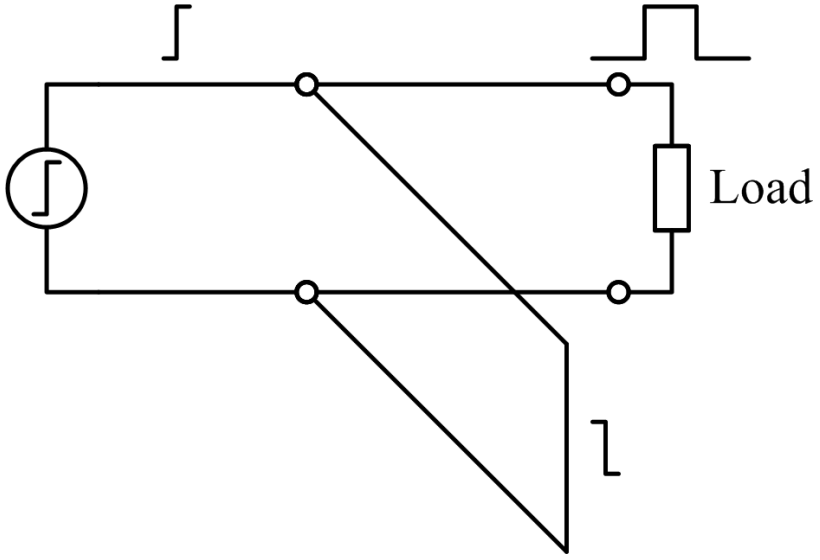


Figure 2.3: Gaussian pulse generator using a fast step generator and transmission lines.

duration, 3.5 V amplitude and good shape symmetry [48]. The impulse duration was also tuned in [49, 50] by varying the length of the short-circuited stub L_d. In [49], a transmission line is loaded with diodes or MESFETs connected to ground at multiple locations, thereby synthesizing a short-circuited stub with a variable length. The pulse time duration and amplitude varies from 300 ps to 800 ps and 1.3 V to 1.9 V respectively using MESFETs [49]. In [50], one of multiple short-circuited stubs with different lengths is connected to the main transmission line using diodes, allowing the pulse duration to vary from 300 ps to 1 ns.

This concept was extended in [50–53] to generate the monocycle pulse from the Gaussian pulse. In [50–52] the monocycle pulse is achieved by using a second short-circuited stub to combine two of the generated Gaussian pulses with opposite polarities and a time delay between them. The produced monocycle pulse had a duration of about twice that of each individual Gaussian pulse. In [53], the monocycle pulse is

generated directly by differentiating the Gaussian pulse using an RC high-pass filter. Therefore the resulting pulse duration can be reduced to be almost the same as that of the Gaussian pulse before differentiation. The fabricated microstrip circuit in [53] generates a monocycle pulse with 300ps time duration, 200mV peak-to-peak voltage, –17dB ringing level, and good pulse symmetry.

Although all of these pulse generators can provide ultra-short Gaussian-based pulses exhibiting high voltage amplitude and good symmetrical shape, they inherently employ some specific components such as SRDs, making them quite difficult to integrate with standard digital CMOS circuits.

2.3.2 Recent UWB Pulse Generators

Several alternative UWB pulse generators have been proposed more recently in the literature, which are integrated into digital CMOS for a low cost and also provide reconfigurable pulse shapes and frequency spectra. For short-range UWB applications and the low emission limits imposed by the FCC, a CMOS chip can provide the requisite power levels with a fast rise time. The new techniques proposed can be split into four main categories: carrier-based, analog filtering, digital filtering and direct digital synthesis. Each will be discussed here with examples given from the current literature.

2.3.2.1 Carrier-based Approaches

Carrier-based UWB pulse generation techniques include heterodyning and time-gated oscillators. In heterodyning, a pulse is first generated at baseband with a low-pass spectrum and then upconverted to the target frequency band. This typically employs

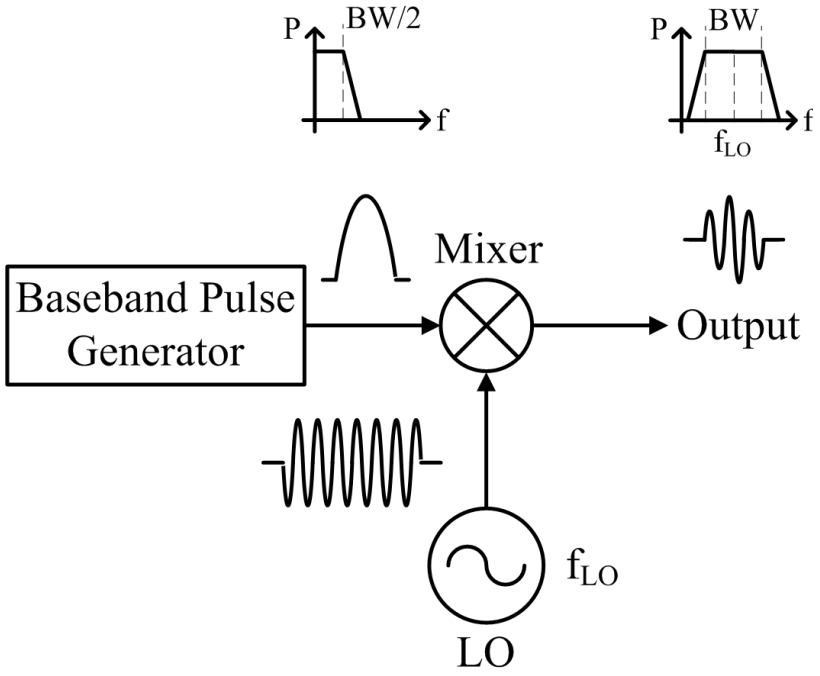


Figure 2.4: Heterodyning for pulse generation.

a local oscillator (LO) and a mixer (multiplier) with the architecture shown in Fig. 2.4. Control of the radiated center frequency is achieved by the LO, which can either have a known fixed frequency or be voltage-controlled for frequency-hopping and multiband applications. In addition, the radiated bandwidth is readily controlled by manipulating the time duration of the baseband pulse. As depicted in Fig. 2.4, frequency upconversion can relax the signal bandwidth required from the baseband pulse generator. Another variant of this is derived through the use of time gating as illustrated in Fig. 2.5, where the output of a continuously-running LO is time gated using an external switch, and/or the LO itself is switched on and off. The output generated by this approach typically exhibits a few cycles of the LO having a rectangular amplitude envelope, which can result in an inefficient sinc spectrum with high out-of-band power that will need to be filtered.

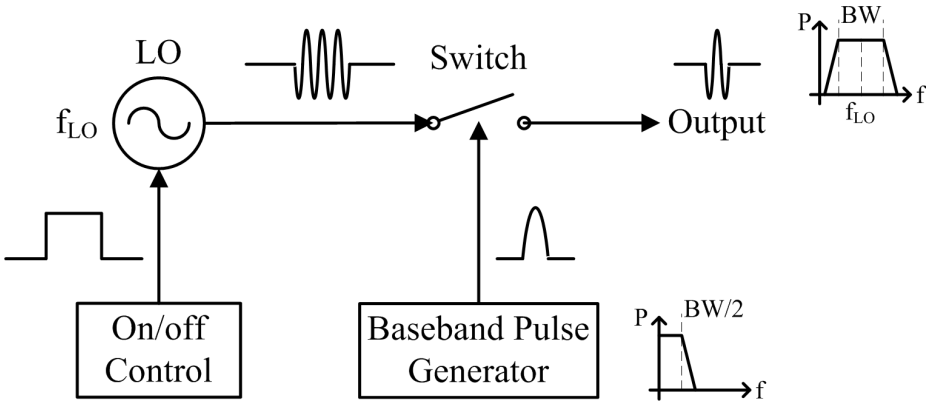


Figure 2.5: Alternative time gating for pulse generation.

Cavallaro et al. [15, 35] recently demonstrated an UWB pulse generator based on the heterodyning technique in 90 nm CMOS. The LO is realized using an inductor-capacitor (LC) voltage-controlled oscillator (VCO) locked in a phase locked loop (PLL). A switched capacitor bank is added in the LC VCO to synthesize carrier frequencies between 3.5 GHz to 4.5 GHz in steps of 500 MHz. The carrier is then BPSK modulated using the well-known Gilbert cell. A switch is added at the output of the BPSK modulator to reduce LO leakage between pulses, which also has a Gilbert cell topology. A ramp generator and a pseudo-Gaussian envelope generator (PEG) form the baseband pulse generator in this design. The ramp generator employs a shift register and a digital-to-analog converter (DAC) to produce a staircase waveform, which is then smoothed by a low pass filter. The PEG then creates a Gaussian-like baseband pulse using the ramp signal as the input. It mainly consists of two differential pairs with their outputs cross-coupled to each other. The large-signal voltage-to-current transfer characteristic of a differential pair is known to be given

by:

$$I_O = \begin{cases} -I_B & V_{id} \leq -\sqrt{2}V_{OV}, \\ \frac{I_B}{V_{OV}} V_{id} \sqrt{1 - \frac{V_{id}^2}{4V_{OV}}} & -\sqrt{2}V_{OV} < V_{id} < \sqrt{2}V_{OV}, \\ I_B & V_{id} \geq \sqrt{2}V_{OV}. \end{cases} \tag{2.8}$$

where I_O is the differential output current, V_{id} is the differential input voltage, I_B is the DC bias current and V_{OV} is the gate overdrive voltage. The current-voltage relationship in (2.8) is exploited to approximate the Gaussian pulse shape. An offset is introduced between the gate overdrive voltages of the two differential pairs, causing the net output current of the cross-coupled structure to rise and fall for a Gaussian-like current impulse. The generated pseudo-Gaussian pulse is then upconverted to the LO frequency band using a folded Gilbert quad. Measurements were demonstrated showing 4 GHz pulses with a Gaussian amplitude envelope. The pulse peak-to-peak voltage is 200 mV and the LO ringing level is below 3 mV. The pulse time duration is 2.8 ns for a 628 MHz –3 dB bandwidth. The maximum PRF can reach 500 MHz and the energy dissipated per pulse is 56 pJ. Switched local oscillators have also been investigated for UWB pulse generation. In [14], an LC oscillator is switched on and off to generate an UWB pulse in response to the digital data. A switched capacitor bank is used in the LC oscillator to be able to switch the oscillation frequency to one of three 528 MHz subbands centered at 3.5 GHz, 4 GHz and 4.5 GHz. A triangular pulse envelope is realized by exploiting the turn-on and turn-off transients of the LC oscillator. The oscillator is turned on by simply activating the tail current source. The rise time, which is designed to be one half of the pulse duration for a symmetrical triangular pulse shape, should be in the range of 1 ns for more than 500 MHz of bandwidth. It can be reduced by increasing the transconductance of the

active devices, which typically requires increasing the DC current. Thus, achieving a rise time on the order of a nanosecond can be challenging depending on power consumption and technology. The oscillator turn off procedure involves simultaneously switching off the tail current source and activating an NMOS switch across the LC tank. The on-resistance of the switch reduces the equivalent parallel resistance across the LC tank for a shorter turn off transient. The size and on-resistance of the NMOS switch is designed to make the fall time equal to the rise time for a symmetrical triangular pulse. The circuit was fabricated in 0.18 μm CMOS with a die area of 560μm$\times$550μm. Measurements were demonstrated showing an output pulse with a peak-to-peak voltage of 160 mV, a time duration of 3.5 ns and a 520 MHz bandwidth at 100 MHz PRF. The energy dissipated per pulse is only 16.8 pJ [14].

Sim et al. [13] presented a pulse generator for 6-10 GHz UWB applications based on the switched oscillator technique. A pulsed three-stage ring oscillator followed by an on-chip pulse shaping filter is proposed. The oscillator has an oscillation frequency in the center of the 6 - 10 GHz band around 8 GHz. It is quickly switched on and off over a short time duration to generate an UWB pulse with a rectangular amplitude envelope. The ring oscillator has a fast on/off transient response due to the low quality factor (Q). A high-pass LC filter is then used to suppress the out-of-band spectral components. The circuit was fabricated in 0.18 μm CMOS, occupying an area of 0.11 mm^2. The average power consumption is 1.38 mW at a supply voltage of 2.1 V for a PRF of 50 MHz. This corresponds to a low energy consumption of 27.6 pJ per pulse. Time- and frequency-domain measurements show a pulse peak-to-peak amplitude of 673 mV, a pulse time duration of 500 ps and a –10 dB bandwidth of 4.5 GHz from 5.9 to 10.4 GHz.

Most if not all of the UWB pulse generators reported for 22-29 GHz UWB applications use an LC VCO locked in a PLL followed by an external switch [30–32, 36]. In [31,36], the Gilbert cell configuration is used to realize a differential current-steering switch. The synthesized 24.125 GHz signal drives the differential transconductor, while the control signal triggers the Gilbert quad to steer the differential current to the output. An integrated center-tapped transformer and a MIM capacitor form a resonant load and convert the differential current to a single-ended voltage output. The circuit was fabricated in a 0.13 μm SiGe BiCMOS technology, and pulses were measured at 10 MHz PRF with time durations of 0.5 and 1 ns and a peak output power of 0 dBm. The total power consumption of the chip is 115 mW. In [32], the 24.125 GHz carrier is first BPSK modulated using a Gilbert cell. A differential current-steering switch based on the Gilbert cell is then used to generate the pulse, followed by a power amplifier (PA) to increase the peak output power to 3 dBm. The PA has a differential cascode topology with a transformer resonant load that provides the needed differential-to-single-ended conversion for the output. The fabricated circuit in 0.13 μm SiGe BiCMOS generates 1 ns and 0.5 ns pulses with a pulse repetition time (PRT) of 270 ns and 135 ns. It consumes about 64 mA from a 2.5 V supply.

2.3.2.2 Analog Filtering

A common way of directly generating an UWB pulse without using a carrier is to first form a baseband impulse with a very short time duration and a high frequency bandwidth, and then filter the impulse using a bandpass or a pulse shaping filter as illustrated in Fig. 2.6. This design is typically more suitable for non frequency-agile applications, as the UWB signal's center frequency and bandwidth are primarily

determined by the bandpass or pulse shaping filter.

Zheng et al. [9, 17, 54, 55] proposed a CMOS circuit that generates the Gaussian doublet, by directly performing the squaring, exponential and second derivative functions required. For the squaring circuit, a transistor operating in the saturation region is used. Non-minimum channel length is chosen for this transistor to reduce velocity saturation and channel length modulation effects [56]. Meanwhile, the exponential circuit consisted of a transistor biased in the subthreshold or weak inversion region. In the absence of a conducting channel the n^+ source, p bulk and n^+ drain form a parasitic bipolar transistor. Thus the current-voltage relationship is exponential in this region and can be approximated as [56]:

$$I_{DS} = I_{D0} e^{\frac{V_{GS}}{\lambda}} \tag{2.9}$$

where I_{D0} and λ are CMOS process dependent parameters. Finally, an LC network (Fig. 2.7) is used at the output to perform second-order differentiation, and its

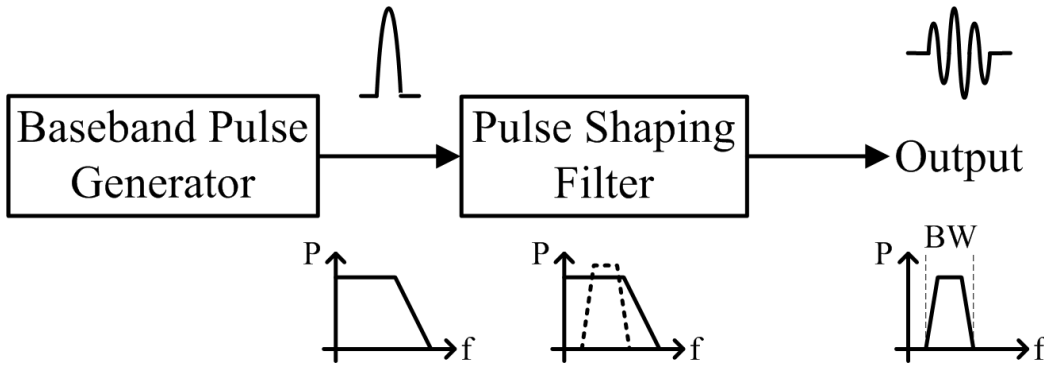


Figure 2.6: Filtering for pulse generation.

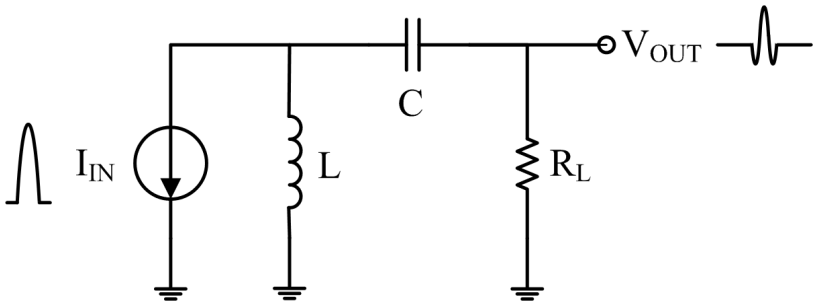


Figure 2.7: RLC pulse shaping circuit as a second-order differentiator.

transimpedance V_{OUT}/I_{IN} can be expressed in the frequency domain (s-domain) as:

$$\frac{V_{out}(s)}{I_{IN}(s)} = \frac{-sR_L L}{R_L + sL + 1/sC} \approx -s^2 R_L LC \tag{2.10}$$

where the approximation is valid if the inductor L and capacitor C values satisfy $R_L + sL << 1/sC$. This is readily achieved in the UWB frequency range with the typical values of on-chip spiral inductors and MIM capacitors. Therefore the voltage V_{OUT} is a second-order derivative of the current I_{IN}. The circuit was fabricated in 0.18μm CMOS and tested with a 200 MHz input clock [54]. The measured output pulse has a Gaussian doublet shape and a good symmetry. It also has a time width of less than 0.8 ns and a –10 dB bandwidth of approximately 2 GHz in the 3 GHz to 5 GHz band. The largest peak-to-peak amplitude is limited to about 35 mV, giving rise to the need for subsequent wideband amplification [9,17,54,55]. This is primarily due to the low subthreshold current levels in the exponential circuit and the significant insertion loss of the differentiating LC network.

S. Bourdel et al. [57] recently demonstrated a pulse generator using digital logic for baseband impulse generation and a third order LC ladder Bessel filter for UWB pulse shaping. Digital logic circuits can be employed to create baseband impulses

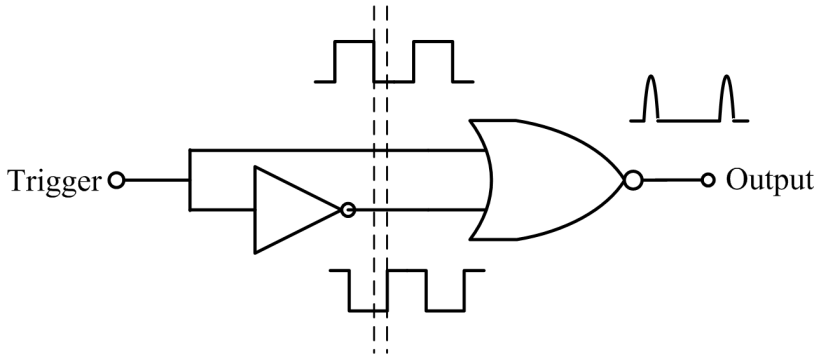


Figure 2.8: Digital logic for impulse generator.

as shown in Fig. 2.8. They typically consist of inverters to introduce a small delay followed by a NOR gate to generate an impulse on every falling edge of a trigger signal. The relative timing of the signals at the input of the NOR gate is shown in Fig. 2.8. The NOR gate combines the falling edge of the trigger signal and its delayed inverted replica to form a positive impulse. NAND gates have also been used in place of the NOR gate to realize impulses with the opposite polarity on every rising edge of the trigger. In [57], high-speed current mode logic (CML) is used for the delay cell to create a baseband impulse with a very short time duration of 75ps and a flat frequency spectrum out to 10 GHz. The generated impulse is then applied to the third-order LC ladder Bessel filter to form the UWB pulse. The filter order is kept to three to limit its signal power loss to within 3 dB, which arises due to the low quality factor (Q) of on-chip passive devices. The measured pulse peak-to-peak amplitude and time duration are 1.42V and 460 ps respectively. The IC occupies an area of 0.54 mm^2 in 0.13μm CMOS technology and consumes 3.84 mW of power at 100 MHz PRF [57].

Kawano et al. [58] designed a pulse generator in 0.13μm Indium Phosphide (InP)

technology for 22-29 GHz UWB applications using a filter-based technique. A baseband impulse with a peak-to-peak voltage of 0.8 V and a very short time duration of only 9 ps is first generated that has a flat frequency spectrum in the 22–29 GHz band. The baseband pulse generator is similar to that of Fig 2.8 and consists of a CML delay inverter and a CML AND gate. The cascode circuit configuration is utilized in the AND gate to reduce the miller capacitance and increase the switching speed for an ultra-short impulse. The chip area and power consumption of the baseband pulse generator is 1.5 mm $\times$ 1.7 mm and 620 mW respectively. A cosine roll-off bandpass filter (BPF) is then used for pulse shaping, with a roll-off factor between 0.9 and 1 to reduce the ringing level at the cost of a longer pulse duration. Transmission lines were used to realize the BPF as opposed to lumped element components. This is due to the low quality factor (Q) of on-chip inductors and capacitors at millimeter wave frequencies. The measured insertion loss of the BPF is 2.6 dB at the center frequency of 26.5 GHz, and the attenuation is about 16 dB and 26 dB at 24 GHz and 29 GHz respectively. The chip area of the BPF is 8 mm $\times$ 5 mm. The generated UWB pulse has a measured swing of about 60 mV, a time duration of less than 500 ps and ringing level of less than –20 dB.

2.3.2.3 Digital Filtering

An alternative to analog filtering is a technique based on a digital filter as shown in Fig. 2.9. Multiple delayed copies of a baseband impulse can be individually scaled with the desired polarity and amplitude, and then added together to form an UWB pulse. Using this method, the UWB pulse waveform and frequency spectrum can be more readily controlled. A trigger signal is distributed to N baseband pulse generators

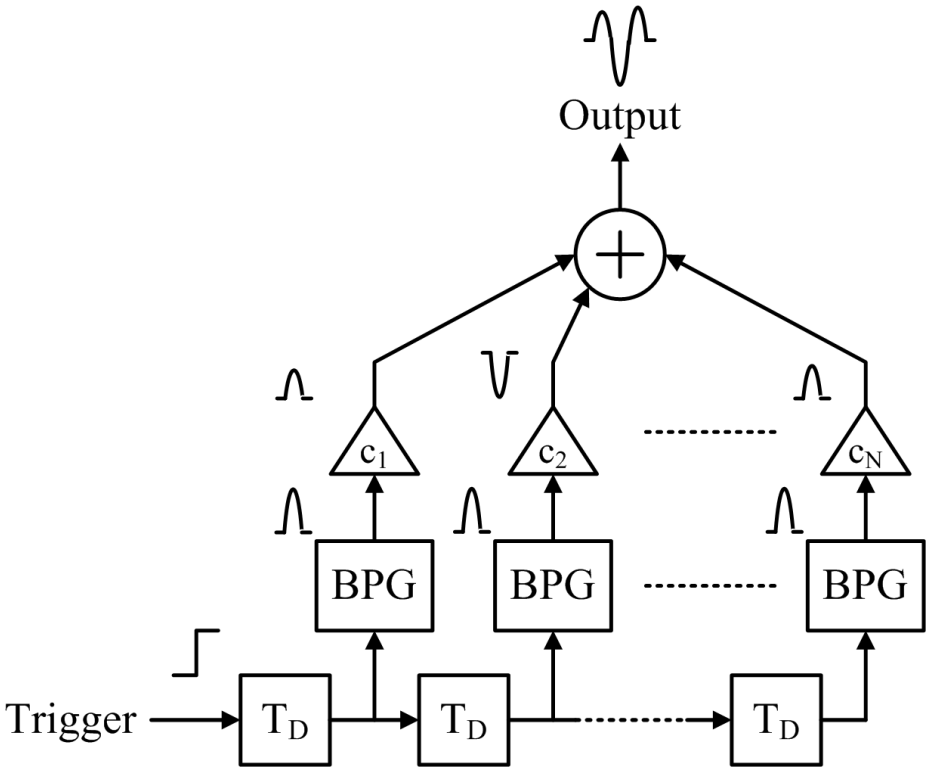


Figure 2.9: Baseband impulse combination for UWB pulse generation.

(BPG) using a digital delay line, with a time delay of T_D per stage (or tap). This triggers the BPGs to produce impulses at sampling times of T_D, $2T_D$, ..., NT_D with a sampling frequency of $f_s = 1/T_D$. These are then independently scaled with tap coefficients c_i, $i = 1, 2, \ldots, N$ using amplifiers. The resulting pulses are finally combined by a wideband pulse combiner at the output. Another variant of this can be derived by directly scaling the delayed edges of the trigger signal and combining them, without generating baseband impulses as shown in Fig. 2.10. In this case, the sum of all of the tap coefficients c_i $i = 1, 2, \ldots, N$ must be equal to zero, to ensure that the generated pulse has a finite time duration.

A digital circuit that approximates the fifth-order derivative Gaussian pulse was

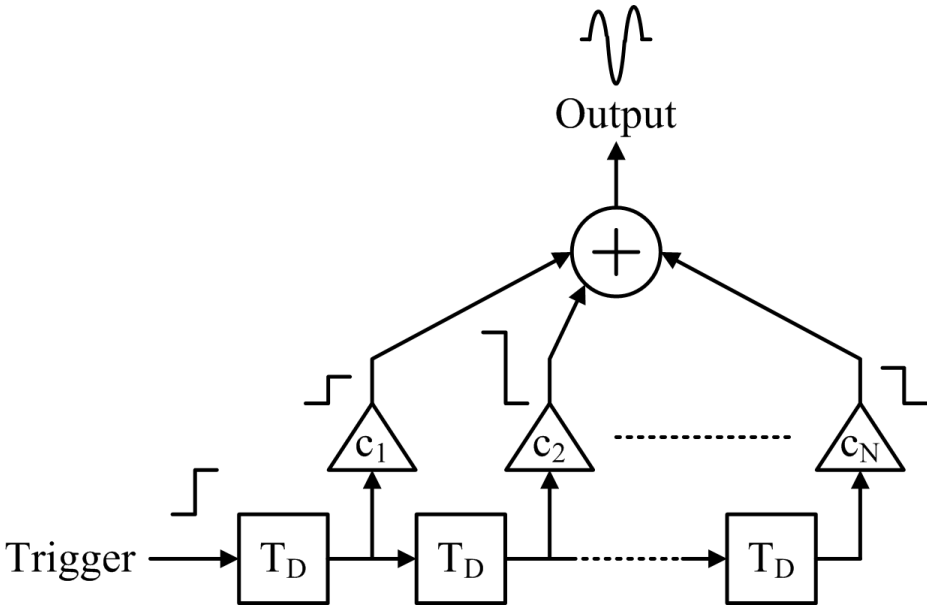


Figure 2.10: Trigger edge combination for UWB pulse generation.

proposed by Kim et al. [59, 60]. It consists of a digital CMOS impulse generator connected to an output stage for driving the 50Ω load. In the digital impulse generator, the input clock edge and its delayed inverse triggers two NAND and two NOR gates to generate four full-swing impulses: two with negative polarities and two with positive polarities respectively. The number and sizing of the inverters are designed to adjust the timing of the four signals appropriately. In the output stage, the four impulses are combined successively. The output stage is designed with a push-pull topology such that the negative impulses switch on PMOS devices and drive current into the load, while the positive impulses switch on NMOS devices and drive current out of the load. The voltage amplitude of each impulse at the output is determined by the size of the corresponding transistor in the output stage. The circuit was designed and simulated using 0.18μm CMOS technology in [60]. The output pulse shape resembles that of the fifth derivative Gaussian pulse. The pulse time width and –10

dB frequency bandwidth are 380 ps and 7.2 GHz respectively. The average power consumption is proportional to the PRF, being 675μW at 1 MHz and 15.4 mW at 500 MHz. The circuit was also designed and fabricated using a 0.50μm CMOS process in [59], occupying an area of $499\mu m \times 370\mu m$ and consuming less than 1.2 mW at 20 MHz PRF. The measured output pulses have the same shape but the peak-to-peak amplitude is 148 mV and the time width is about 2.4 ns.

Zhu et al. [8, 61–63] presented a distributed waveform generator (DWG), which is based on the addition of delayed scaled copies of a baseband pulse (Fig. 2.9). In this design, a CMOS inverter delay line is used to distribute the trigger signal to ten baseband pulse generators. The nominal delay per stage is set to 100 ps for a sampling rate of 10 GHz. Digital CMOS logic with inverters, NAND gates and NOR gates is used to generate the baseband impulses (Fig. 2.8). Switched current sources (cascode current mirrors) are used to implement impulse scaling. The amplitude scaling is achieved by varying the reference current of the cascode current mirror. The outputs of all the switched current sources are connected to an on-chip coplanar waveguide (CPW) transmission line for pulse combining and impedance matching. A transmission line is employed here to provide the wide analog bandwidth necessary for pulse combination. This is very similar to the technique used in travelling wave amplifiers. Neglecting losses, the cut-off frequency f_c and characteristic impedance Z_0 of the transmission line are known to be given by:

$$f_c = \frac{1}{\pi\sqrt{LC}} \tag{2.11a}$$

$$Z_0 = \sqrt{\frac{L}{C}}, \tag{2.11b}$$

which are independent of the number of stages, and only depend on the inductance L and the total (loaded) capacitance C per unit length of the transmission line. The circuit was implemented using a 0.18μm CMOS, with an active circuit area of 1.6 mm $\times$ 0.2 mm. Different waveforms can be generated with on-off keying (OOK) and pulse position modulation (PPM). An UWB pulse was demonstrated with a voltage swing of 70 mV, time duration of 0.8 ns and a –10 dB frequency bandwidth of 6 GHz (3–9 GHz). The maximum PRF is 2.5 GHz and the energy consumption per pulse is 45 pJ.

A circuit with the architecture depicted in Fig. 2.10 was demonstrated by Demirkan et al [6]. In this design, the delay line consists of a chain of CML D flip-flops that are clocked by a 14.4 GHz clock signal. Hence, the time delay between the consecutive stages is equal to the period of the 14.4 GHz clock signal. The 14.4 GHz clock signal is realized on-chip using an LC VCO in a PLL. The output trigger edges of the delay line are first buffered and then sent to the taps. The buffers employ series inductive peaking to achieve a short trigger edge rise time of 40 ps. The tap cells are implemented as CML XOR gates with tail current sources. The tap weights are determined by the relative values of the tail currents. The differential outputs of all the taps are tied together to obtain a combined differential output current. This differential current pulse is converted to a single-ended voltage pulse by an on-chip wideband balun, which is implemented using two-turn coupled spiral inductors. The IC was fabricated in 90 nm CMOS with a die area of 2.83 mm^2. UWB pulses with binary phase shift keying (BPSK) and PPM were demonstrated, having a voltage swing of 220 mV and a time duration of 0.53 ns. The power consumption of the pulse generator and PLL are 129 mW and 98 mW respectively at a PRF of 1.8 GHz.

Oncu et al. [64] demonstrated a pulse generator with an architecture similar to that shown in Fig. 2.9 for 22-29 GHz UWB applications. A chain of CMOS inverters forms the delay line in this implementation. Edge combiners are then used to directly perform a NAND operation on each pair of delayed (inverted) trigger edges on the delay line. This generates impulses with both the time shift and time duration being equal to the delay per stage on the line. Each edge combiner is essentially the pull-down network of a two-input CMOS NAND gate. No PMOS devices are used in this design due to their inferior high-frequency performance that will decrease the sampling frequency of the delay line and thus the center frequency of the pulse. A short impulse of 39.2 ps can thus be realized for a center frequency of about 25.5 GHz. The impulses are then combined by directly connecting the outputs of the edge combiners together to an external bias tee. The relative sizing of the edge combiners determines the tap weights, which are designed to give a pseudo raised cosine (PRC) pulse shape for higher spectral efficiency. The generated pulse has a time duration of 552 ps and a peak-to-peak voltage of 71 mV, which corresponds to a peak power of only –16 dBm. The power consumption is only 1.4 mW at 500 MHz PRF, corresponding to an energy consumption of 2.8 pJ per pulse.

2.3.2.4 Direct Digital Synthesis

Another approach for UWB pulse generation is waveform synthesis based on high speed digital-to-analog converters (DAC) as shown in Fig. 2.11. A high speed DAC with a good resolution can directly generate UWB pulses with different shapes and is fully reconfigurable. Such a DAC-based UWB pulse generator, however, requires

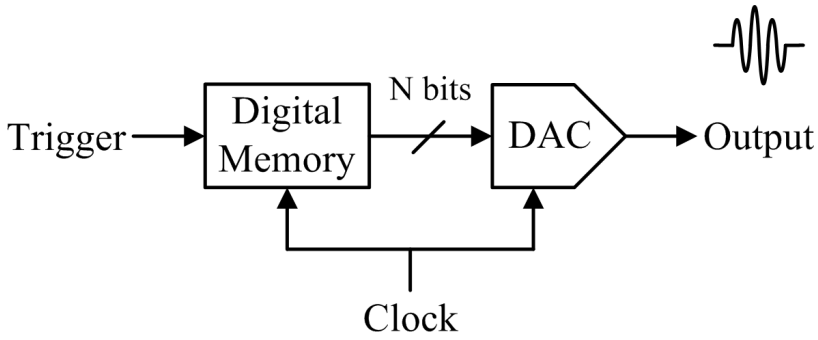


Figure 2.11: Direct digital waveform synthesis for UWB pulse generation.

a sampling rate of more than the Nyquist rate, e.g., more than 20 GHz for a 3-10 GHz UWB pulse. A 20 GHz 6-bit DAC was reported in [65] for UWB pulse generation, creating various pulse shapes and supporting several modulation formats. The high sampling rate poses a real challenge not only for the DAC, but also for generating the input digital data stream. This typically leads to power-hungry high speed digital CML circuits, using more advanced technologies such as SiGe BiCMOS [65]. Therefore, it is imperative to leverage some analog and RF techniques to reduce the required power consumption in an UWB pulse generator.

2.4 Ultra-Wideband Amplifiers

There are many different topologies commonly used for wideband LNAs as shown in Fig. 2.12 [37–41, 66–73]. Conventional wideband amplifiers such as the common-gate amplifier or the common-source resistive shunt-feedback amplifier can have difficulties in achieving a low NF while maintaining a good impedance match over a wide range of frequencies, or suffer from limited gain and stability. Distributed and travelling wave amplifiers can provide a low NF, good impedance match, and flat gain over a very wide frequency bandwidth, but can suffer from limited gain, consume a

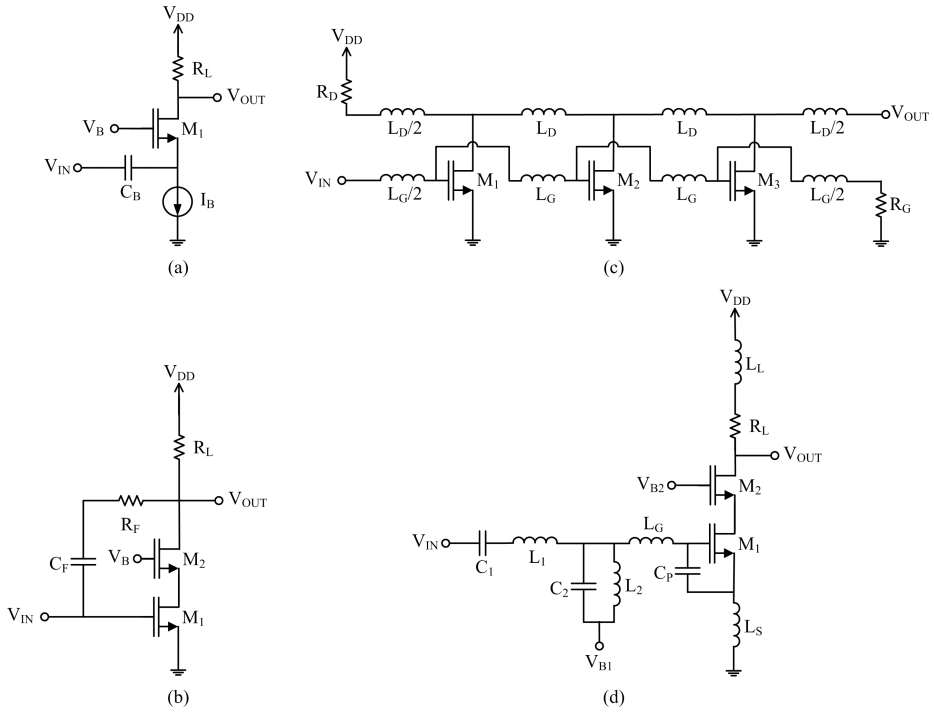


Figure 2.12: Common wideband LNA topologies: (a) Common-gate, (b) shunt resistive feedback, (c) distributed, and (d) passive input matching

significant amount of power or occupy a particularly large chip area. More recently, inductive degeneration and multi-section inductor-capacitor (LC) networks have been reported for wideband noise and impedance matching. However, the insertion loss of the matching network in the input path degrades the NF rapidly as the frequency increases. Noise cancelling has been shown to be an effective approach for achieving a low NF and an impedance match simultaneously [74–77]. Nevertheless, the input voltage sensing and auxiliary amplifier stages used for noise canceling can contribute significant input-referred noise at high frequencies thus degrading the NF.

2.5 Summary and Conclusions

In this chapter, short-time pulse generators and broadband low noise amplifiers for UWB have been discussed with a focus on implementation in CMOS processes. Sub-nanosecond pulse generation and low noise amplification are critical functions in pulsed UWB transceivers and pose real challenges requiring a wide signal bandwidth along with a low circuit complexity (for low cost) and a low power consumption. The Gaussian pulse and its derivatives are the most commonly used UWB pulse shapes in the literature. At least the fifth-order derivative is required to fit the frequency spectrum in the FCC mask without using additional filtering or frequency shifting. However a high-order derivative typically increases the circuit complexity, power consumption and sensitivity to component mismatches.

Traditional UWB pulse generators have employed some specific components such as step recovery diodes (SRDs), which are difficult to integrate in standard CMOS. Carrier-based pulse generators form an impulse at baseband and then upconvert it to the target frequency band, which inherently provide good control of the center frequency and bandwidth of the pulse spectrum. These tend to be quite complex and power hungry however due to the use of continuously running local oscillators (LO) and/or mixers. The LO phase locked loop (PLL) is continuously running since its turn-on and locking transient are usually not short enough for it to be switched off and on during the inter-pulse period, resulting in high LO leakage and low energy efficiency. Switched or gated local oscillators have been reported with a low circuit complexity and a high energy efficiency. Nevertheless, they can have a relatively long stabilization time which limits the pulse bandwidth. In addition, there is little control over the startup and turn off transients of the oscillator, and the output pulse shape

cannot be readily tuned.

Direct (carrier-less) UWB pulse generators have been demonstrated by generating a very short baseband impulse and then shaping it using analog filters. They generally employ large passive devices and provide only one specific pulse shape. Furthermore, the high bandwidth required from the baseband impulse and the low quality factor (Q) of on-chip inductors and capacitors often leads to a low energy efficiency. Distributed waveform generators based on combining multiple delayed impulses or edges have also been reported that are reconfigurable for various pulse shapes and modulation schemes. They typically employ digital delay lines, digital logic gates and wideband analog combiners. Nevertheless their distributed nature typically leads to a large area and a low energy efficiency. Finally, fast digital-to-analog converters (DACs) with good resolution have been used for direct UWB waveform synthesis and can provide high tunability. However high sampling and data rates are required (20 GHz), which usually results in high power consumption.

Conventional wideband amplifiers such as the common-gate amplifier often have difficulties in achieving a low noise figure (NF) while maintaining a good impedance match. Distributed amplifiers on the other hand can provide a low NF, good impedance match, and flat gain, but can suffer from limited gain. Multi-section inductor-capacitor (LC) networks have also been reported for wideband matching. However, the insertion loss of these networks degrades the NF. Finally, noise cancelling is effective for achieving a low NF and an impedance match. Nevertheless, the auxiliary amplifiers can contribute significant noise at high frequencies.

Chapter 3

Energy-Efficient Tunable UWB Pulse Generator

This chapter demonstrates a new energy-efficient tunable pulse generator in 0.13 μm CMOS for short-range high-data-rate 3.1–10.6 GHz UWB applications [44]. A ring oscillator consisting of current-starved CMOS inverters is quickly switched on and off to create pulsed oscillations at a high rate. The amplitude envelope of the pulsed oscillations is then shaped using a variable passive attenuator to form UWB pulses that can satisfy the FCC mask. The variable passive attenuator consumes zero DC power and has a wide bandwidth. It is controlled using an impulse which is created by a low-power glitch generator (CMOS NOR gate). The glitch generator combines the falling-edge of the clock signal and its delayed inverse to form the impulse. It allows the duration and rise/fall times (slopes) of the UWB pulse to be changed over a wide range by simply varying the delay between the edges and controlling the (dis)charging currents of the NOR gate respectively. The proposed pulse shaping technique consisting of the variable passive attenuator and the glitch

generator provides a low power and low complexity (small footprint and low cost) solution featuring a high bandwidth and tunable performance. This is in contrast to using a variable gain amplifier or an inductor-capacitor (LC) filter. The generated pulses can provide a sharp frequency roll off with high out-of-band rejection to meet the FCC spectrum limits. The entire circuit operates in switched-mode with zero static current for a low average power consumption of less than 3.8 mW at 910 MHz pulse repetition frequency (PRF), or below 4.2 pJ of energy per pulse. It occupies a total area of 725×600 μm^2 including bonding pads and decoupling capacitors, and the active circuit area is only 360×200 μm^2.

3.1 Circuit Architecture and Design

A block diagram of the UWB pulse generator is shown in Fig. 3.1(a). It mainly consists of a current-starved ring oscillator, a glitch generator and a variable attenuator. An inverter chain first sharpens the rising/falling edge of the clock signal, which is used to turn the ring oscillator on and off. The clock signal is then split into two branches in the glitch generator, one of which is delayed and inverted with respect to the other. A NOR gate combines the falling and rising edges of these signals to form an impulse, whose duration can be tuned over a wide range by varying the delay between the edges. This impulse controls the variable attenuator to shape the amplitude envelope of the ring oscillator's signal and form an UWB pulse with the desired bandwidth and frequency spectrum that can meet the FCC mask. Note that the pulse generator can support on-off keying modulation (OOK) and pulse position modulation (PPM) by directly modulating the input clock signal with the baseband digital data. Fig. 3.1(b) shows the complete circuit schematic.

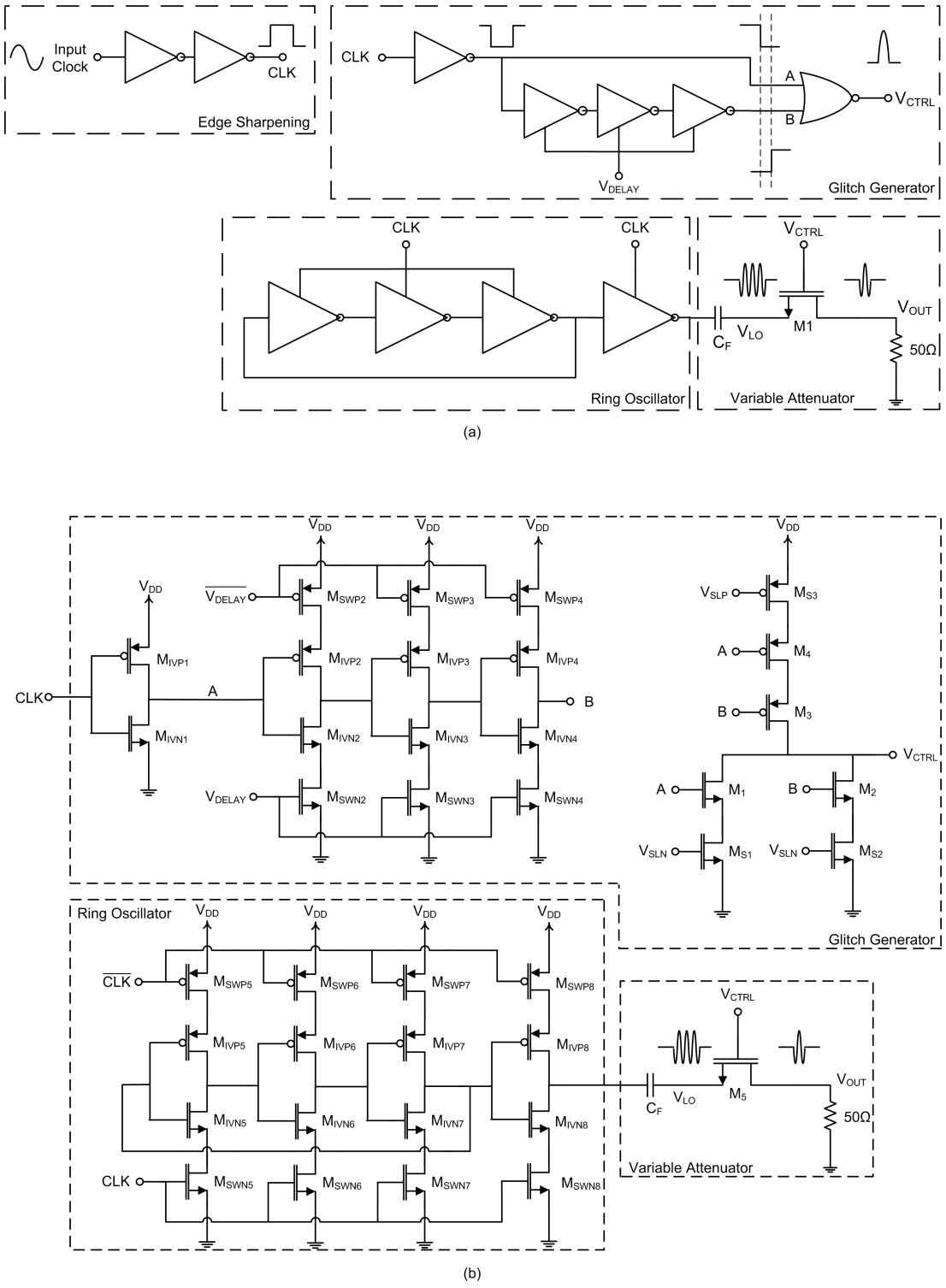


Figure 3.1: Proposed UWB pulse generator: (a) block diagram and (b) circuit schematic.

3.1.1 Current-Starved Ring Oscillator

The ring-oscillator [18, 19, 47, 78–80] has a very short startup time due to its low quality factor, which is important for low-power high-data-rate UWB applications. An inductor-capacitor (LC) resonator-based oscillator can not be quickly switched on and off at a high rate due its comparatively high quality factor and long startup time ($>$ 1 ns). However the maximum oscillation frequency of a ring oscillator is limited, and it consumes more power than its LC counterpart. In this work, three current-starved CMOS inverters are cascaded in a ring or loop as shown in Fig. 3.1, to produce an oscillating waveform with a fixed frequency when the series NMOS and PMOS devices (M_{SWN} and M_{SWP} in Fig. 3.1(b)) are switched on by the clock signals. To compensate for the lower mobility of holes and generate a symmetric waveform with equal rise and fall times, PMOS devices (M_{IVP} and M_{SWP}) are made larger than NMOS devices (M_{IVN} and M_{SWN}) such that their effective on-resistance are approximately equal to that of the NMOS devices. The equivalent on-resistance of the NMOS and PMOS devices (R_{eqn} and R_{eqp}) are given by [81]:

$$R_{eqn} \propto \frac{1}{I_{dsatn}}, \quad R_{eqp} \propto \frac{1}{I_{dsatp}}, \tag{3.1}$$

where

$$I_{dsatn} = \frac{\mu_n C_{oxn}}{2} \frac{W_n}{L} \left(V_{dd} - V_{tn}\right)^2 \frac{1}{1 + \frac{(V_{dd} - V_{tn})}{LE_{satn}}}, \tag{3.2a}$$

$$I_{dsatp} = \frac{\mu_p C_{oxp}}{2} \frac{W_p}{L} \left(V_{dd} - |V_{tp}|\right)^2 \frac{1}{1 + \frac{(V_{dd} - |V_{tp}|)}{LE_{satp}}}. \tag{3.2b}$$

I_{dsatn} and I_{dsatp} are the drain currents through the NMOS and PMOS devices respectively under velocity saturation. μ_n and μ_p are the electron and hole mobilities, C_{oxn} and C_{oxp} are the gate oxide capacitances per unit area, W_n and W_p are the device widths, L is the gate length, E_{satn} and E_{satp} are the saturation electric fields, and V_{tn} and V_{tp} are the threshold voltages. For the 0.13 μm CMOS technology used: $\mu_n = 5.27 \times 10^{-2}$ m^{2}V/s, $\mu_p = 0.89 \times 10^{-2}$ m^{2}V/s, $C_{oxn} = 1.16 \times 10^{-2}$ F/m^2, $C_{oxp} = 1.08 \times 10^{-2}$ F/m^2, $L = 120$nm, $E_{satn} = 3.27 \times 10^6$ V/m, $E_{satp} = 1.39 \times 10^7$ V/m, $V_{tn} = 0.43$ V, and $V_{tp} = -0.43$ V. Therefore, from (3.2), the saturation drain current through the NMOS and PMOS devices (I_{dsatn} and I_{dsatp}) are approximately equal if:

$$W_p = 3.12W_n \approx 3W_n, \tag{3.3}$$

at which point:

$$R_{eqn} \approx R_{eqp}. \tag{3.4}$$

The oscillation time period T and frequency f are set by the propagation delay t_p through an inverter: $T = 2Nt_p = 6t_p$, $f = 1/T = 1/6t_p$. The inverter delay can be minimized by careful design to maximize the oscillation frequency without consuming excessive power. The series connection of the switching and inverter devices (M_{SW} and M_{IV} in Fig. 3.1(b)) can be viewed as a distributed resistor-capacitor (RC) network, consisting of the transistors' equivalent on-resistance (R_{sw} and R_{iv}) and the internal and output node capacitances (C_{int} and C_{out}), as illustrated in Fig. 3.2. It is important to note that the NMOS and PMOS device widths are ratioed ($W_{swp} = 3W_{swn}$, $W_{ivp} = 3W_{ivn}$) for equal on-resistance to yield a symmetric output waveform with equal rise and fall times. The RC network shown in Fig. 3.2 can be used to

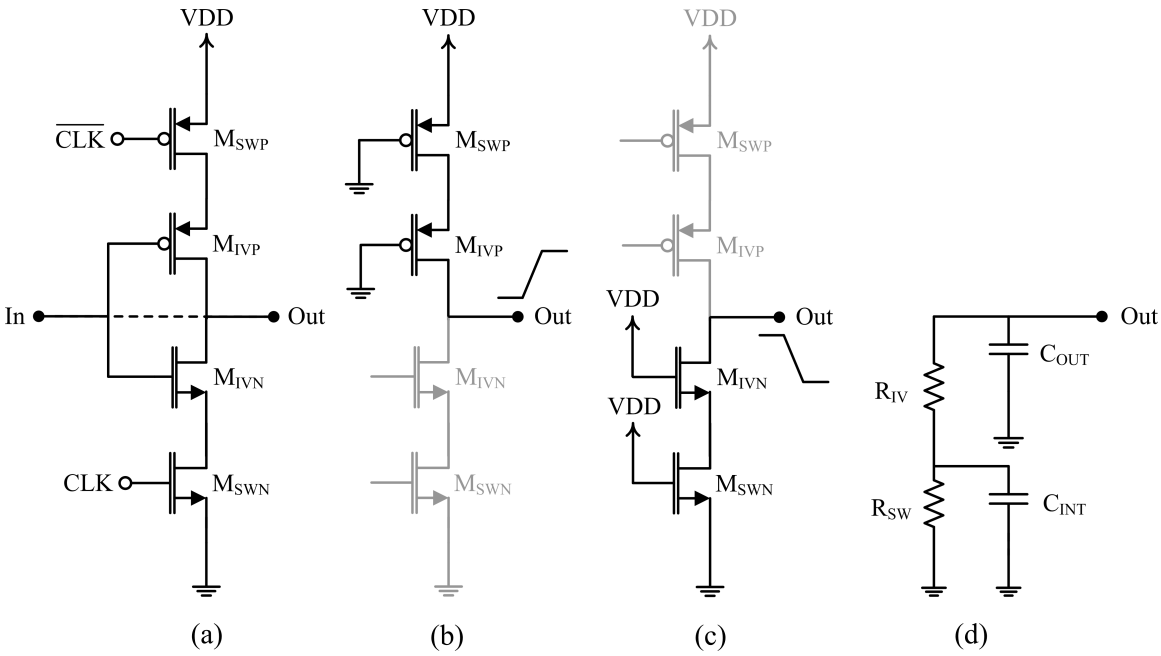


Figure 3.2: Current-starved inverter cell: (a) Inverter schematic, (b) State in the low-to-high transition, (c) State in the high-to-low transition and (d) Equivalent RC network.

represent the NMOS half and the PMOS half of the inverter, during the high-to-low and low-to-high output transition respectively. The time constant τ associated with the output transitions can also be approximated as [82]:

$$\tau \approx R_{sw}C_{int} + R_{sw}C_{out} + R_{iv}C_{out} \tag{3.5}$$

As the on-resistance (R_{sw}) of the switching device and the output capacitance (C_{out}) each appear in two of the terms and thus dominate the delay, the width of the switching device should be made as large as possible (limited by power constraints), while that of the inverter device should be made relatively small for an oscillation frequency in the 5 GHz range.

A more detailed analysis of the ring oscillator was performed to arrive at the

optimum inverter device sizes that lead to the maximum oscillation frequency for the chosen switching device sizes of $W_{swn} = 24$ μm and $W_{swp} = 72$ μm. Two of the small-signal models shown in Fig. 3.3(a) are used to represent each inverter, one for the NMOS half and another for the PMOS half. The models include the parasitic capacitances (C_{gsiv}, C_{gdiv}, C_{dbiv}, C_{sbiv}, C_{gdsw}, C_{dbsw}), transconductance (g_{miv}) and output resistances (R_{oiv}, R_{osw}) of the devices. The parasitics and transconductance are calculated by assuming that the inverter and switching devices are operating in velocity saturation and triode respectively. The Y-parameters (Y_{11}, Y_{12}, Y_{21}, Y_{22}) shown in Fig. 3.3(b) for the small-signal model are given by:

$$Y_{11} = \frac{Y_{gs}\left(Y_{ds} + Y_s\right)}{Y_s + Y_{gs} + G_m + Y_{ds}} + Y_{gd} \tag{3.6a}$$

$$Y_{12} = \frac{-Y_{gs}Y_{ds}}{Y_s + Y_{gs} + G_m + Y_{ds}} - Y_{gd} \tag{3.6b}$$

$$Y_{21} = \frac{G_m Y_s - Y_{gs}Y_{ds}}{Y_s + Y_{gs} + G_m + Y_{ds}} - Y_{gd} \tag{3.6c}$$

$$Y_{22} = Y_{db} + \frac{Y_{ds}\left(Y_{gs} + Y_s\right)}{Y_s + Y_{gs} + G_m + Y_{ds}} + Y_{gd} \tag{3.6d}$$

and the admittances (Y_s, Y_{gs}, Y_{gd}, Y_{ds}, Y_{db}) and transconductance G_m are:

$$Y_s = \frac{1}{R_{osw}} + j\omega\left(C_{gdsw} + C_{dbsw} + C_{sbiv}\right) \tag{3.7a}$$

$$Y_{gs} = j\omega C_{gsiv}, \quad Y_{gd} = j\omega C_{gdiv} \tag{3.7b}$$

$$Y_{ds} = \frac{1}{R_{oiv}}, \quad Y_{db} = j\omega C_{dbiv} \tag{3.7c}$$

$$G_m = g_{miv} = \frac{\mu C_{ox}}{2}\frac{W}{L}\left[V_{ov}||LE_{sat}\right]\frac{V_{ov} + 2LE_{sat}}{V_{ov} + LE_{sat}} \tag{3.7d}$$

where the overdrive voltage V_{ov} is $V_m - V_t$. V_m is the switching threshold of the inverter

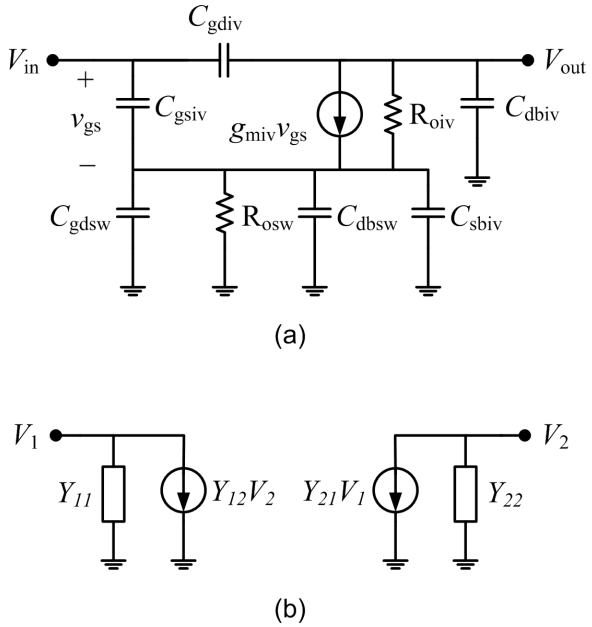


Figure 3.3: Inverter cell modelling and analysis: (a) Small-signal model for the PMOS or NMOS half with parasitic capacitances and output resistances, and (b) Equivalent Y-parameter network.

which is approximately $V_{dd}/2$, since the PMOS and NMOS device widths are ratioed ($W_{swp} = 3W_{swn}$, $W_{ivp} = 3W_{ivn}$) for a symmetrical voltage transfer characteristic.

The equivalent Y-parameter model for the inverter can be calculated by adding the Y-parameters computed for the NMOS and PMOS circuits, since they are connected in parallel between the input and output nodes. The complete ring oscillator can then be analyzed by cascading three of these Y-parameter models in a positive feedback loop as shown in Fig. 3.4. Performing KCL at nodes V_2 and V_3 and solving for the voltage gain per stage ($A_v = V_2/V_1$, etc) gives:

$$A_v = \frac{Y_{12}^2 - Y_{21}\left(Y_{22} + Y_{11}\right)}{\left(Y_{22} + Y_{11}\right)^2 - Y_{12}Y_{21}} \tag{3.8}$$

The zero-loop-phase condition of the Barkhausens criterion for oscillation can thus

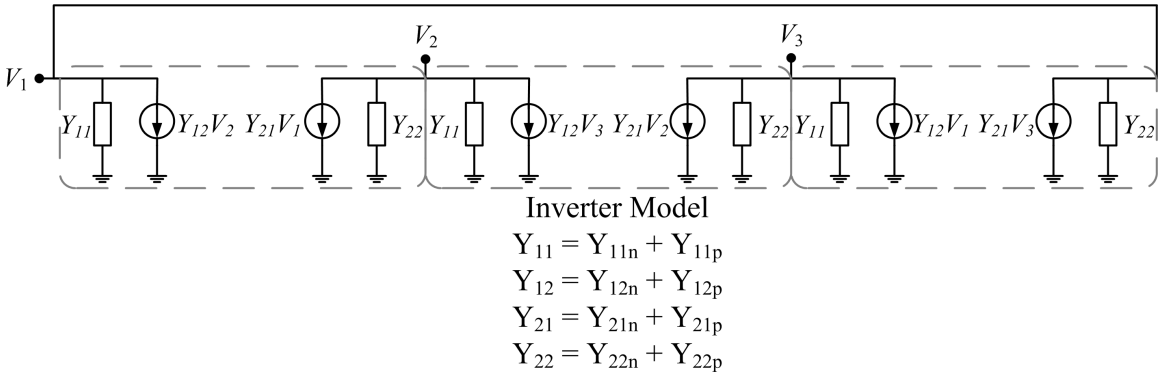


Figure 3.4: Ring oscillator model with three inverter Y-parameter models and positive feedback.

be met if:

$$\angle A_v = \angle \left[\frac{Y_{12}^2 - Y_{21}\left(Y_{22} + Y_{11}\right)}{\left(Y_{22} + Y_{11}\right)^2 - Y_{12}Y_{21}} \right] = 120^\circ \tag{3.9}$$

Equation (3.9) yields a relationship between the oscillation frequency (ω) and the inverter device width (W_{ivn}). Fig. 3.5(a) shows a plot of the oscillation frequency versus the inverter device width (W_{ivn}) that satisfy (3.9). Theoretically, the maximum (unloaded) oscillation frequency of the oscillator is 5.94 GHz when the inverter device width is 6.5 μm as observed in Fig. 3.5(b). Using a wider device does not increase the oscillation frequency and only consumes more power. In simulation, the optimum inverter device size was ultimately found to be slightly below 6.5 μm at 5 μm. This minimizes the delay to less than 28.5ps for a maximum (unloaded) oscillation frequency of 5.88 GHz. Note that this analysis and optimization of the inverter device width was repeated for a range of switching device sizes. Using a switching device width smaller than $W_{swn} = 24$ μm can only generate a lower oscillation frequency, while using a larger device width can generate the desired oscillation frequency but at the cost of increased power consumption.

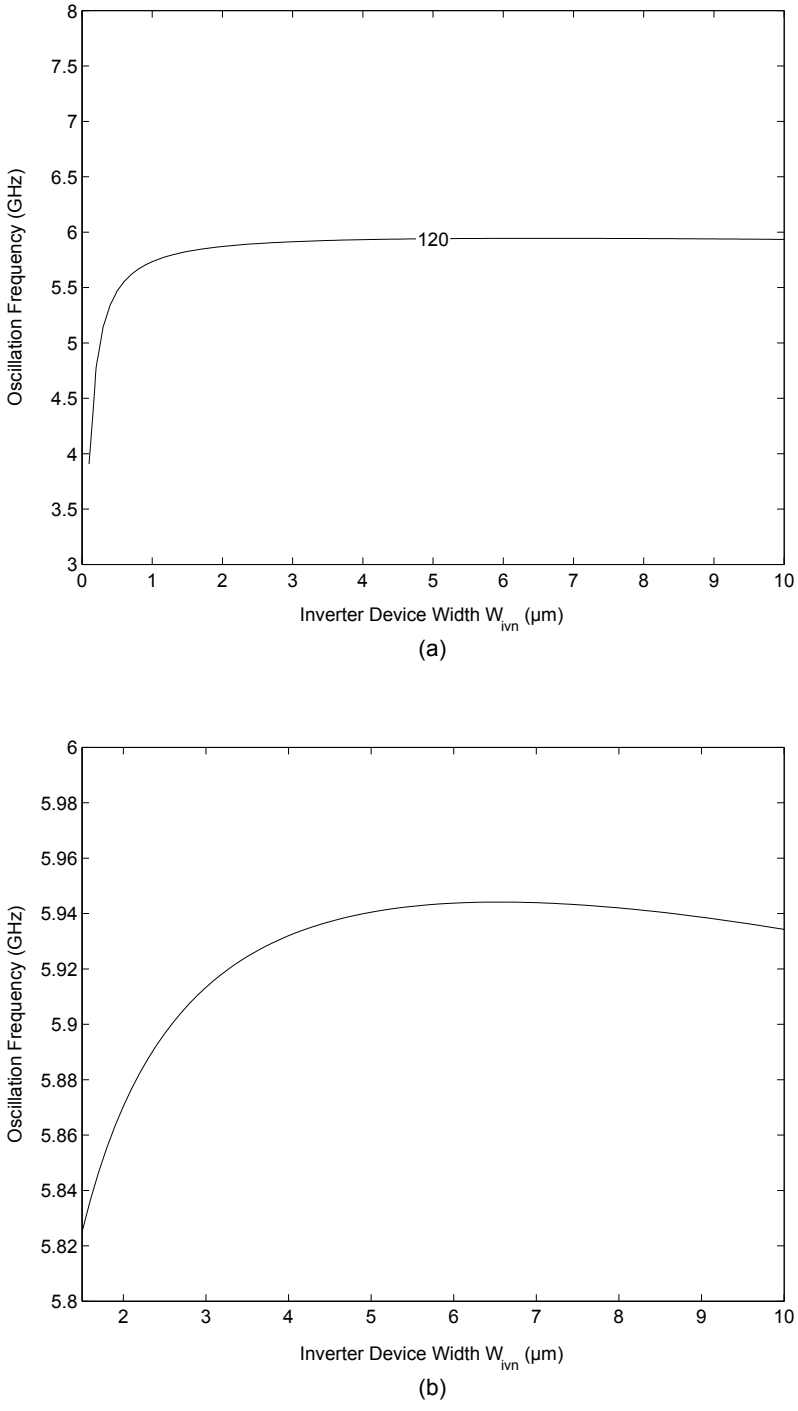


Figure 3.5: Ring oscillator frequency variation with inverter device width W_{ivn} for chosen switching device width of $W_{swn} = 24\mu$m: (a) Plot of 120° phase contour, and (b) Plot of 120° contour more closely shown to depict the optimum device width for the maximum oscillation frequency.

3.1.2 Glitch Generator

The sub-nanosecond glitch generator [59, 83–85] shown in Fig. 3.1 is an important component in creating the wideband signal having the required duration and shape. The pulse produced must be sharp and narrow enough (sub-nanosecond duration) to ensure high bandwidth. At the same time it should be tunable to allow for longer durations and lower bandwidths. The main block in the glitch generator is the CMOS NOR gate shown in Fig. 3.1(b). The output of this gate is high only if both inputs are low. An impulse can be created in a glitch fashion by feeding the gate with a clock falling edge along with its delayed inverse (A and B in Fig. 3.1). The short duration where both signals are low causes the NOR gate's output (V_{CTRL}) to be temporarily pulled high thus generating the pulse (Fig. 3.1). This period of time also specifies the duration of the pulse. The delayed, inverted signal is realized using three cascaded current-starved CMOS inverters similar to those in the ring oscillator, as shown in Fig. 3.1. This allows for the delay and thus the pulse duration to be varied by changing the gate voltage of the series devices. In addition, series devices are also added to the NOR gate (M_{S1}, M_{S2} and M_{S3} in Fig. 3.1(b) to control the (dis)charging current and thus tune the rise/fall times (slopes) of the output pulse for a high out-of-band rejection. A NOR gate is used in this circuit as opposed to a NAND gate, since it directly provides a positive impulse without the need for an additional inverter at the output thus minimizing power consumption.

The performance of the NOR gate can be optimized to maximize the pulse bandwidth. The PMOS (M_3, M_4 and M_{S3}) and NMOS (M_1, M_2, M_{S1} and M_{S2}) devices are sized such that the pull-up and pull-down equivalent path resistances are roughly equal for a symmetric output pulse with equal rise and fall times. Furthermore the

pull-up (M_3, M_4 and M_{S3}) and pull-down (M_1, M_2, M_{S1} and M_{S2}) series devices are progressively sized to minimize the RC time constants (Equation (3.5)) and maximize pulse bandwidth. The performance of the NOR gate also depends on input ordering. The critical input signal, i.e. the last signal that undergoes a transition and switches the output, should be connected to the transistor closest to the output of the gate. The delayed rising-edge (B) that signals the end of the pulse is the most critical and is thus connected to the PMOS device M_3 at the output. As soon as the rising-edge arrives, M_3 turns off and the pull-down NMOS devices M_1, M_2, M_{S1} and M_{S2} need to discharge only the output (V_{CTRL}) node capacitance. This speeds up the high-to-low transition of the output pulse for faster operation. Otherwise M_3 would remain on and both output and internal node capacitances would need to be discharged, slowing down the transition.

The optimum size for each device is determined by extensive simulation. Fig. 3.6 is a comparison between the generated impulse in simulation and the Gaussian pulse given by:

$$p(t) = A_p e^{-\left(\frac{t}{\tau}\right)^2} \tag{3.10}$$

where A_p is the pulse amplitude which is the supply voltage $V_{dd} = 1.2$V in this case, and $\tau = 155$ps is the pulse width and shape parameter. The shape of the generated impulse is close to that of the Gaussian pulse with a mean squared error of only 1.3%, expressed as a percentage of the mean square value of the Gaussian pulse. The time duration of the impulse is also about 400 ps. Fig. 3.7 shows the simulated glitch generator output as the impulse time duration and shape are tuned. It is clear that the pulse can have a time duration ranging from about 350 ps to about 800 ps.

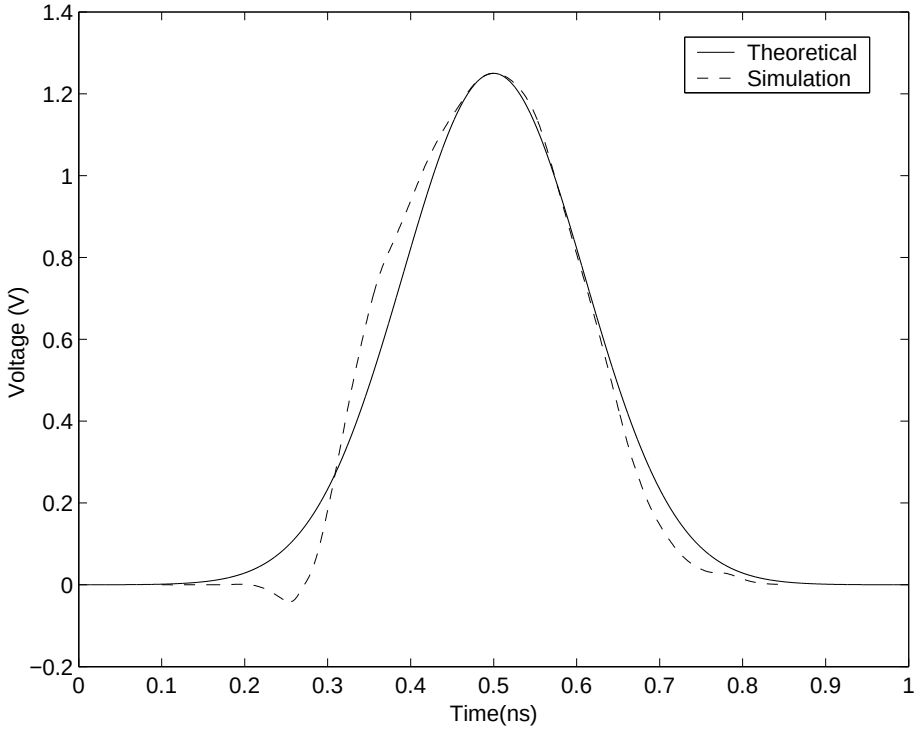


Figure 3.6: Generated baseband impulse and the Gaussian pulse with an amplitude of 1.2 V and time duration of 400 ps.

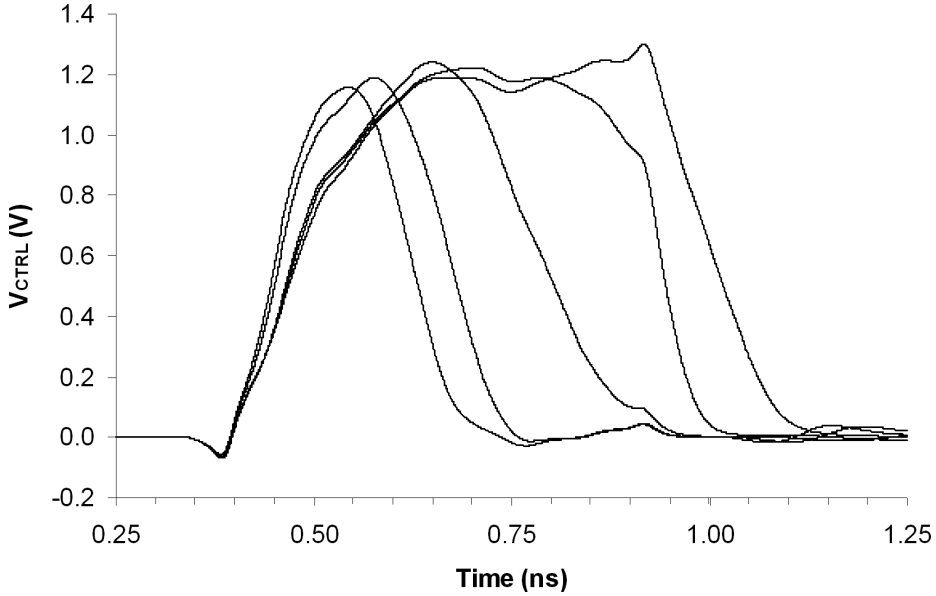


Figure 3.7: Simulated impulses with varying durations.

3.1.3 Variable Attenuator

A variable passive attenuator is used for pulse shaping as opposed to a variable gain amplifier for instance since the attenuator consumes zero DC power and has a small footprint which is particularly useful in low-power, low-cost UWB applications. It also has a wider bandwidth and higher dynamic range with comparable devices. This comes at the cost of insertion loss. An inductor-capacitor (LC) filter is unsuitable since it cannot be readily tuned for different pulse durations and shapes.

A variable resistor-based attenuator can be readily implemented on-chip by using a zero-biased MOSFET, with the resistance and attenuation controlled by the gate voltage. The bandwidth of the attenuator is thus inherently limited by the parasitic capacitances of the MOSFET. To reduce the parasitic capacitance for higher bandwidth, a single series NMOS device M_5 is used as shown in Fig. 3.1(b). The conventional π-network has a higher attenuation range, but two inverted impulse signals are needed to control the series and shunt devices, and the higher parasitic capacitance can diminish the gain in attenuation range at higher frequencies. Furthermore, since the oscillator is switched off after pulse transmission, the required attenuation range for the attenuator is relaxed. As shown in Fig. 3.1(b), M_5 is driven by the pulse V_{CTRL} produced by the glitch generator. When the impulse voltage level is low (0 V), the device M_5 is switched off, blocking the oscillator's signal V_{LO} from reaching the output V_{OUT}. When the impulse voltage level is high ($V_{dd} = 1.2$ V), the signal is passed to the output with minimum loss. This in effect performs the desired envelope shaping as the pulse varies with time. The size of M_5 affects the performance of this circuit considerably, and a device width W of 8 μm gives a good tradeoff between insertion loss, bandwidth and attenuation range.

The envelope shaping performed by the variable attenuator can be analyzed by first considering the drain-source current I_{ds} through the NMOS device M_5. When the gate control voltage V_{ctrl} is less than the device threshold voltage V_t, the device operates in the subthreshold or weak inversion region and the current is given by [81]:

$$I_{ds} \approx I_S e^{\frac{V_{ctrl}}{nkT/q}} \left(1 - e^{\frac{V_{ds}}{kT/q}}\right) \tag{3.11}$$

where I_S and n are empirical fitting parameters with values of 2.4 nA and 1.4 respectively for the 0.13 μm CMOS technology used and the chosen device width W of 8 μm. Equation (3.11) amounts to a relatively small subthreshold current I_{ds}, yielding a large device resistance compared to the 50 Ω load. This results in negligible signal transmission from the input to the output and this mode of operation can thus be ignored.

However when the gate control voltage V_{ctrl} exceeds the device threshold voltage V_t, the device enters the triode region of operation [81]:

$$I_{ds} \approx \frac{\mu C_{ox}}{1 + V_{ds}/LE_{sat}} \frac{W}{L} \left[(V_{ctrl} - V_t)\, V_{ds} - \frac{V_{ds}^2}{2}\right] \tag{3.12}$$

Therefore the resistance R_{ds} of M_5 is approximately:

$$R_{ds} \approx \frac{V_{ds}}{I_{ds}} = \frac{1 + V_{ds}/LE_{sat}}{\mu C_{ox} \frac{W}{L} (V_{ctrl} - V_t - V_{ds}/2)} \tag{3.13}$$

which is a function of the gate control voltage V_{ctrl} and the drain-source voltage V_{ds} across the device M_5. It varies from $1/\left[\mu C_{ox} W/L\,(V_{ctrl} - V_t)\right]$ to $2/\left[\mu C_{ox} W/L\,(V_{ctrl} - V_t)\right]$ as V_{ds} varies from 0 V to the velocity saturation voltage $V_{dsat} = (V_{ctrl} - V_t)\,||LE_{sat}$.

The average resistance of M_5 with respect to V_{ds} (R_{dsavg}) can be found as:

$$\begin{aligned} R_{dsavg} =& \frac{\int_0^{V_{dsat}} R_{ds} \mathrm{d}V_{ds}}{V_{dsat} - 0} \\ =& \frac{2}{KV_{dsat}} \left(1 + \frac{2V_{ov}}{LE_{sat}}\right) \ln \left| \frac{2V_{ov}}{2V_{ov} - V_{dsat}} \right| - \frac{2}{KLE_{sat}} \\ \approx& \frac{1.5}{KV_{ov}} \end{aligned} \tag{3.14}$$

where $K = \mu C_{ox} W/L$ and $V_{ov} = V_{ctrl} - V_t$. The transmission coefficient T through the variable attenuator can thus be evaluated as:

$$T = \frac{Z_0}{R_{dsavg} + Z_0} = \frac{\mu C_{ox} \left(W/L\right) Z_0 \left(V_{ctrl} - V_t\right)}{1.5 + \mu C_{ox} \left(W/L\right) Z_0 \left(V_{ctrl} - V_t\right)} \tag{3.15}$$

where Z_0 is the 50 Ω load impedance.

The envelope shaping waveform is computed using (3.15) for the Gaussian pulse given in (3.10), with $V_{ctrl}(t) = p(t)$, and the chosen device width W of 8 μm. Fig. 3.8 shows the control voltage $V_{ctrl}(t)$, the amplitude shaping waveform $T(t)$ and its Fourier transform $|T(j\omega)|$. It is apparent that the envelope shaping waveform $T(t)$ is different from that of the Gaussian control voltage $V_{ctrl}(t)$, having a shorter time duration and sharper edges due to the nonlinearity of the transfer function T with respect to the control voltage V_{ctrl}. Despite this pulse compression effect, the variable attenuator can theoretically provide 22 dB of out-of-band rejection as evident in Fig. 3.8(c). In simulation, the out-of-band rejection is more than 20 dB using the generated impulse shown in Fig. 3.6 for V_{ctrl}. The series capacitor C_f shown in Fig. 3.1(b) also acts as a high-pass filter and provides additional rejection of low-frequency components. This relaxes the filtering requirements for meeting the FCC mask, especially in the 1–1.6 GHz band where tight limits are imposed for Global Positioning Systems (GPS).

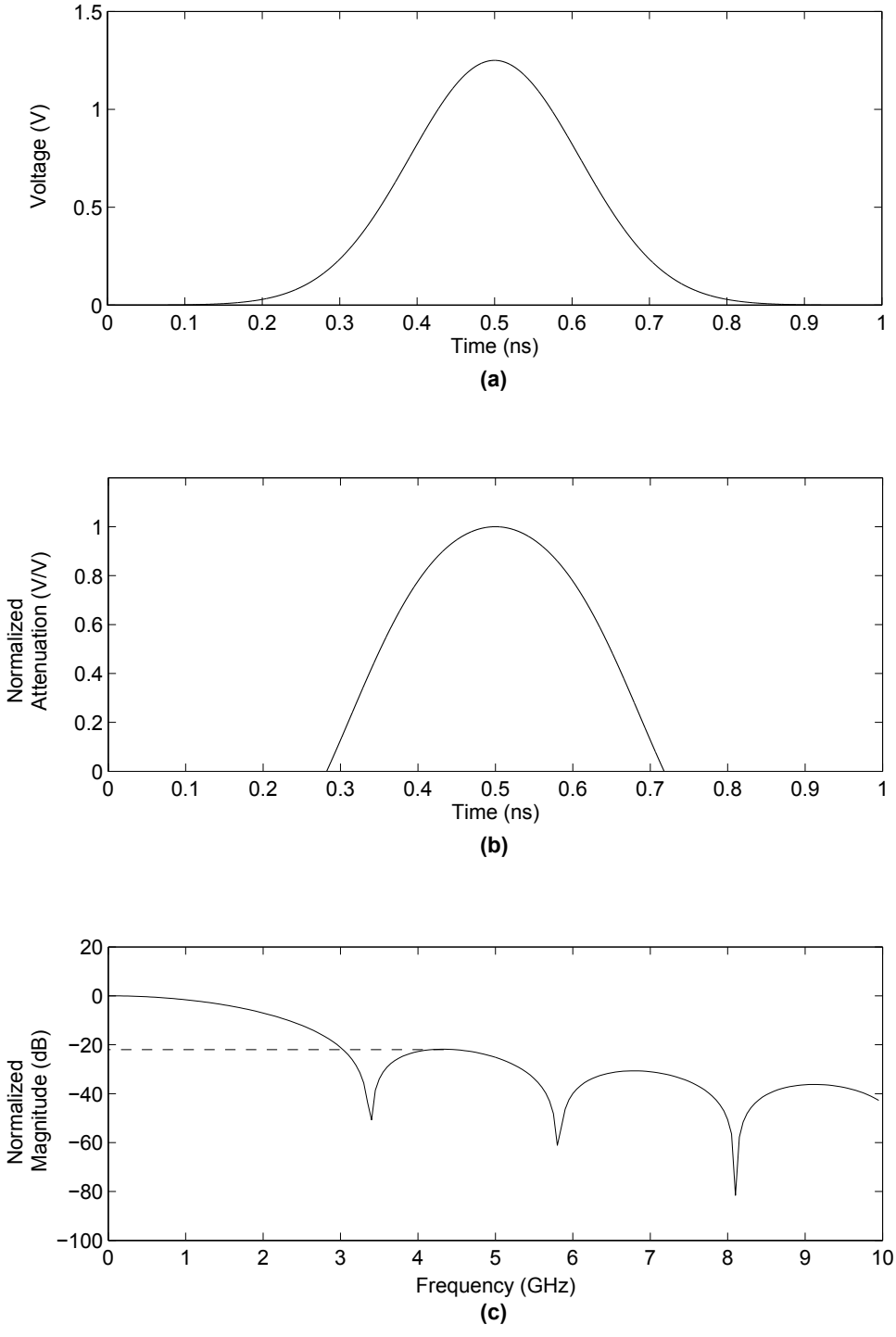


Figure 3.8: Envelope shaping through variable attenuator: (a) Control voltage Vctrl(t), (b) Amplitude shaping waveform $T(t)$, and (c) Amplitude shaping in frequency domain $|T(j\omega)|$.

3.2 Measurement Results

The pulse generator was fabricated in a standard 0.13 μm CMOS process and a photograph of the IC is shown in Fig. 3.9. It occupies a die area of 725×600 μm^2 including bonding pads, decoupling capacitors and the chip guard ring (plus chamfer regions), while the core circuit area is only 360×200 μm^2. The circuit consumes less than 3.8mW of average power (P_{AVG}) at a PRF of 910 MHz. This gives an energy consumption E_p of less than 4.2pJ over the pulse repetition time (PRT) of 1.1ns:

$$E_p = P_{AVG} \times PRT = P_{AVG}/PRF = 4.2\text{pJ} \tag{3.16}$$

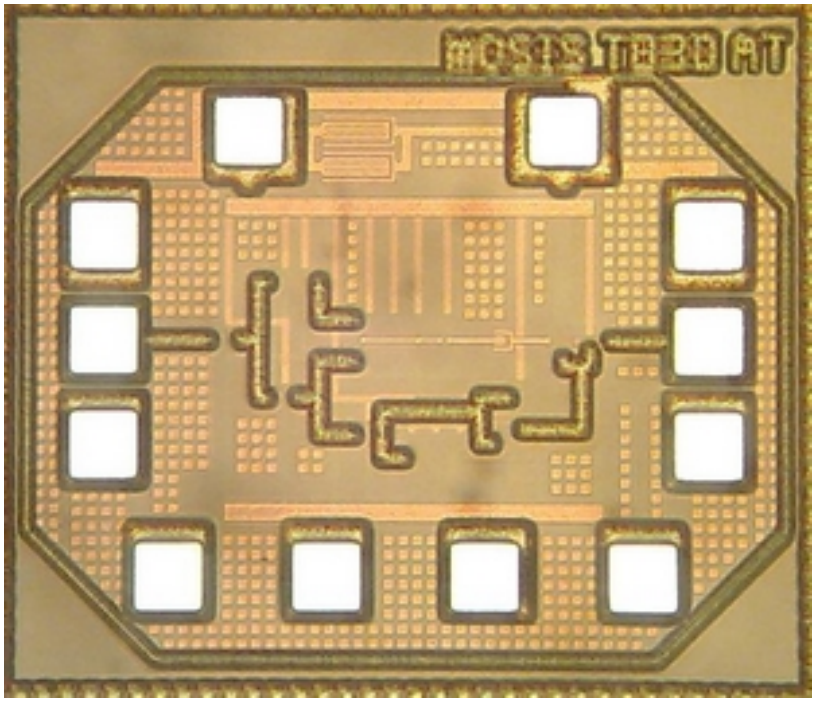
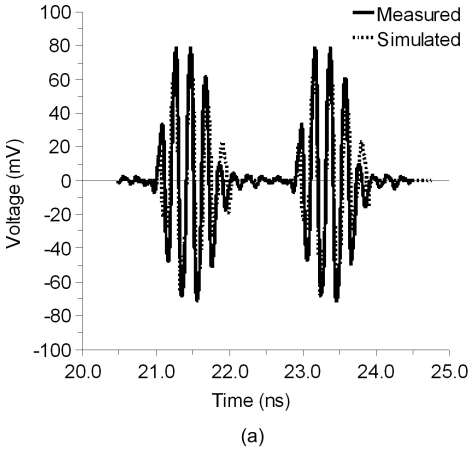


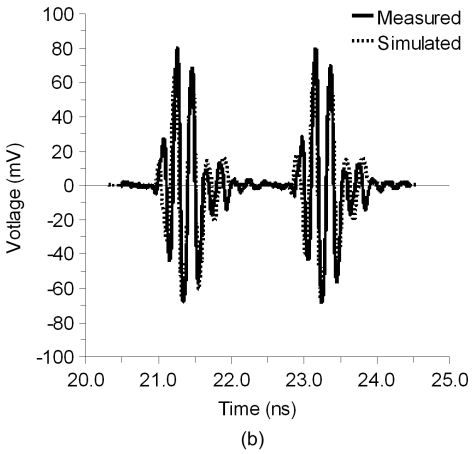
Figure 3.9: Photograph of UWB Pulse Generator IC.

The UWB pulse generator IC was measured directly on-wafer using 40 GHz coplanar waveguide (CPW) probes and DC probes. A 60 GHz Tektronix Digital Serial Analyzer (DSA8200) was used to observe the pulses in the time domain, while a 50 GHz Agilent spectrum analyzer (E4448A) was used to examine the output power spectrum. The input clock is a periodic sinusoidal signal which is converted on-chip into a digital square wave using the edge sharpening inverters (Fig. 3.1).

Fig. 3.10 and Fig. 3.11 illustrate the generated UWB waveforms at 525 MHz and 910 MHz PRFs respectively. The pulses have a peak-to-peak voltage amplitude (V_{pp}) of about 150 mV and a maximum ringing level of –15 dB, with good symmetry about the 0 V (ground) level $(V_{pk+} + V_{pk-})/(V_{pk+} - V_{pk-}) \approx 5.5$ %. The pulse time duration can also be tuned over a wide range from about 500 ps to 900 ps. There is also good agreement between simulated and measured waveforms as observed on the plots.

Fig. 3.12 and Fig. 3.13 show the average power spectrum for the waveforms in Fig. 3.10(c) and Fig. 3.11(c) with a resolution bandwidth of 1 MHz and a frequency span of 10 GHz. The power spectra exhibit well-defined peaks at multiples of the PRF since the output is a periodic (unmodulated) extension of the pulses. Fig. 3.14 shows the pulse power spectra computed from the pulse waveforms in Fig. 3.11 with a frequency resolution of 1 MHz and a span of 10 GHz. It is clear that the –10 dB bandwidth of the pulses varies from about 2 GHz to 3 GHz and that the center frequency is about 4.8 GHz, which corresponds to the ring-oscillator's signal frequency. The spectrum roll off is also quite sharp, with more than 25 dB of out-of-band rejection relative to the peak power level. Furthermore, only little attenuation is needed below 3 GHz to ensure compliance with the indoor and/or outdoor FCC masks.





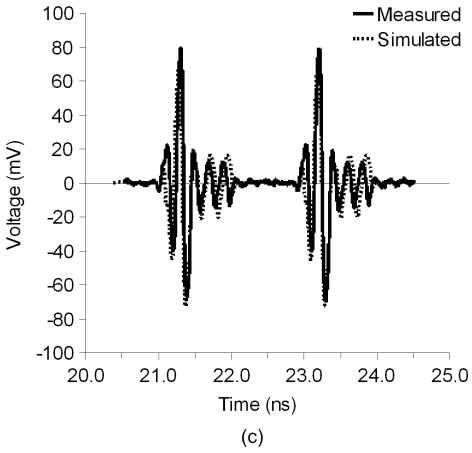
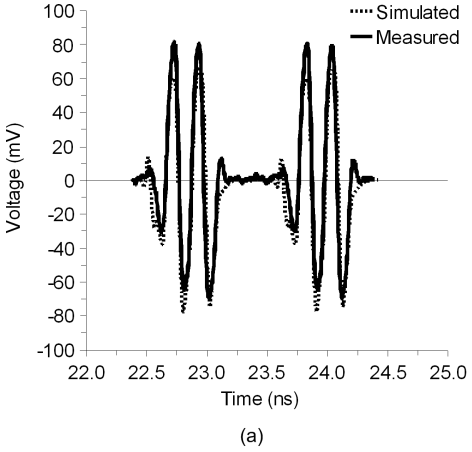
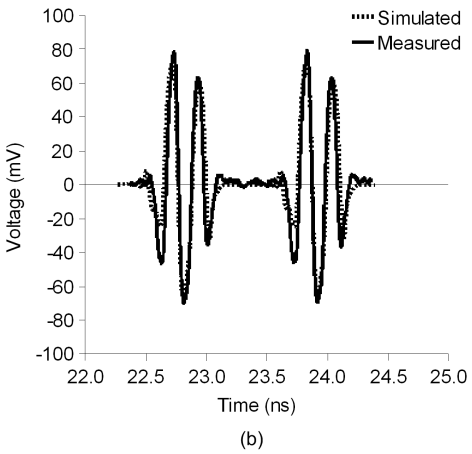


Figure 3.10: Pulses at 525 MHz PRF with: (a) 900 ps, (b) 700 ps and (c) 500 ps time durations.





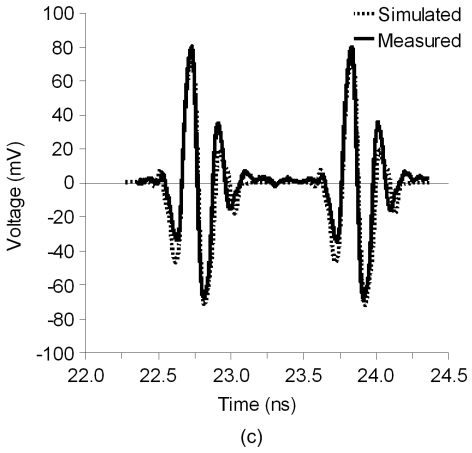


Figure 3.11: Pulses at 910 MHz PRF with: (a) 600 ps, (b) 525 ps and (c) 500 ps time durations.

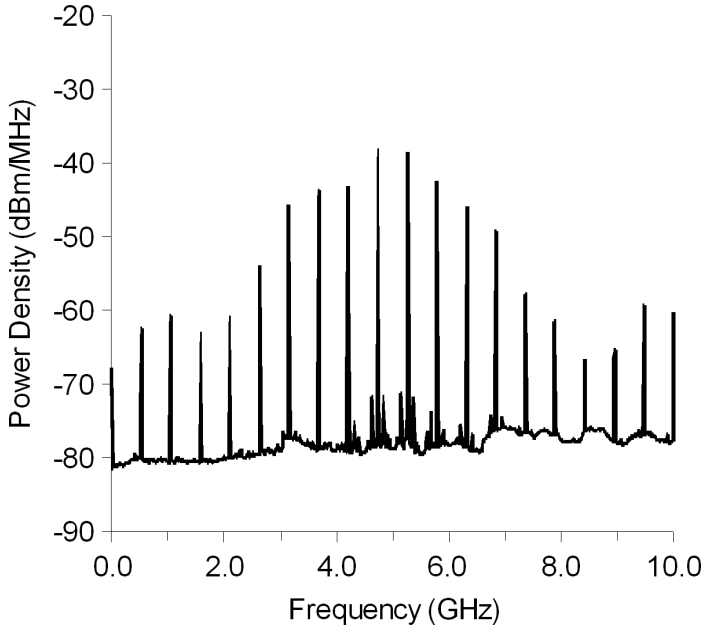


Figure 3.12: Measured power spectrum at 525 MHz PRF.

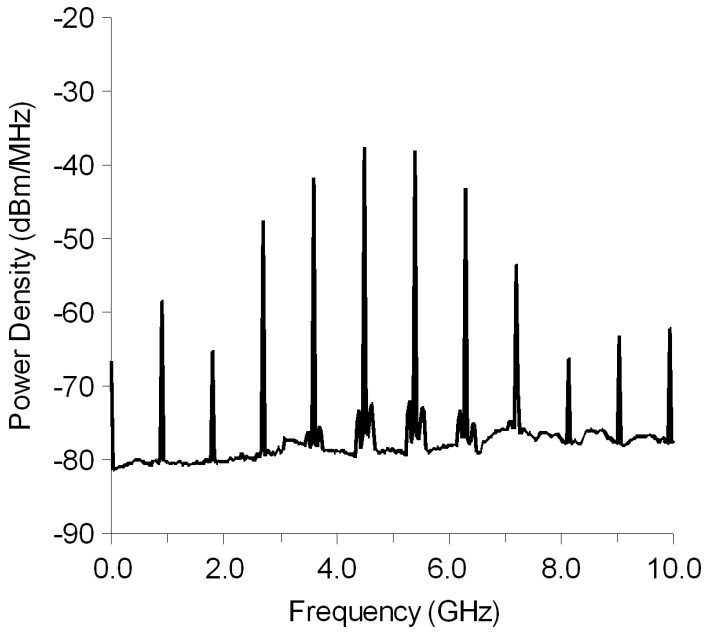


Figure 3.13: Measured power spectrum at 910 MHz PRF.

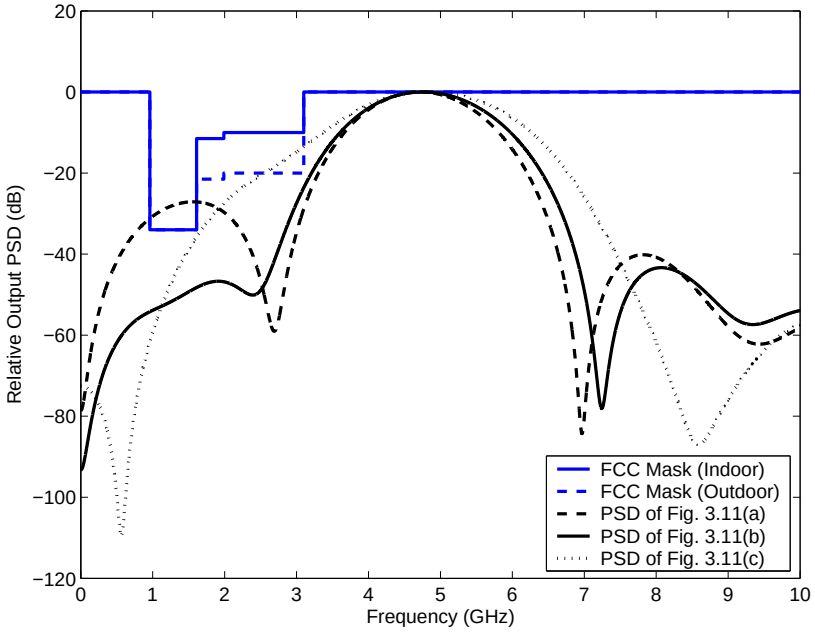


Figure 3.14: Computed pulse frequency spectrum for the waveforms in Fig. 3.11.

The ring oscillator's oscillation frequency and thus the output pulse center frequency may drift due to changes in process, temperature and supply voltage. A statistical Monte Carlo simulation with *global* variations in the process and device parameters including the device width W, length L and threshold voltage V_t was conducted for the output center frequency. The variations in the process and device parameters are approximated using Gaussian distributions with a mean (μ) equal to the design target value and a standard deviation (σ) defined by lower and upper limits provided by the foundry (3σ limits). For this simulation, $N = 100$ trials with *standard* sampling was used (as opposed to Latin Hypercube Sampling - LHS). It is apparent that the center frequency has a mean of 4.8 GHz and a standard deviation of ± 0.31 GHz or approximately ± 6 %. Simulations of the center frequency as a function of temperature and power supply voltage are also shown in Fig. 3.16. As the temperature changes from 0 °C to 75 °C at the nominal supply voltage of 1.2 V, the pulse

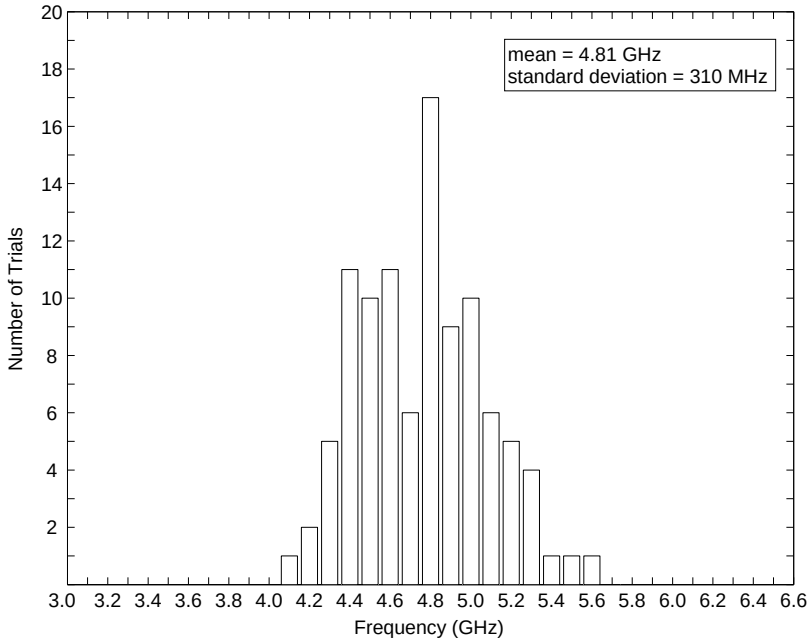


Figure 3.15: Statistical Monte Carlo simulation of the oscillator center frequency with process variations

center frequency shows a variation of less than ±4 % (Fig. 3.16(a)). In addition, the pulse center frequency changes by about ±5 % (Fig. 3.16(b)) as the power supply voltage changes by ±5 % (from 1.15 V to 1.25 V) at the nominal temperature of 25 °C. These variations should be tolerable, since they are relatively small compared to the pulse frequency bandwidth of more than 2 GHz or 40 %. The integrated power lost into adjacent channels, over a 2 GHz bandwidth would be relatively small and the receiver would still be able to detect the pulse to a certain extent.

Table 3.1 summarizes the proposed pulse generator's performance in comparison with other work that has been reported recently. Although it can be difficult to make fair comparisons when different specifications and technologies are used, it is clear that the proposed circuit achieves a relatively low energy consumption of 4.2 pJ/pulse. It is important to note that the low energy consumption of 2.5 pJ/pulse

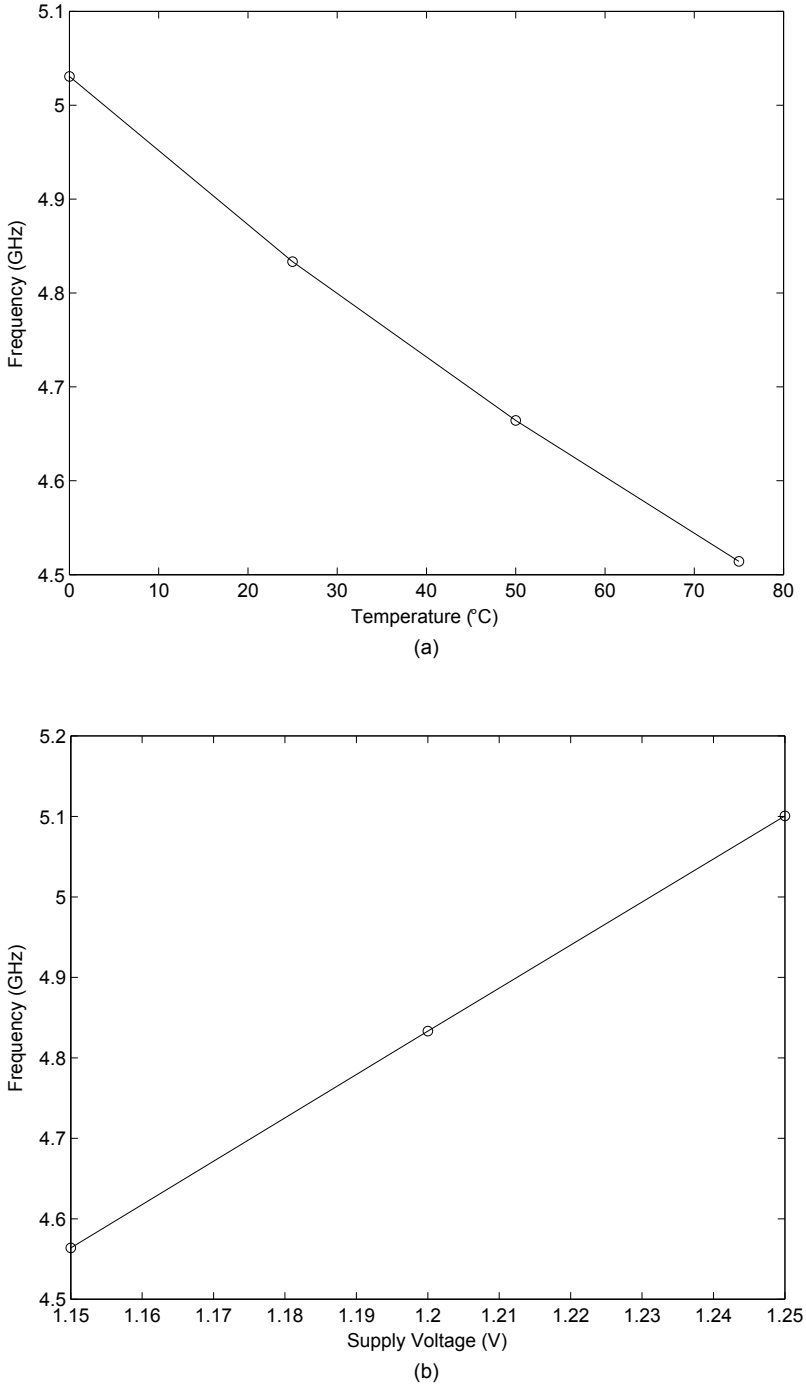


Figure 3.16: Variation of the oscillator center frequency with: (a) temperature and (b) supply voltage.

and 9 pJ/pulse reported in [86] and [57] does not include 6 mW and 3.2 mW of power consumed in the output buffer and MOS current mode logic (CML) gates respectively. The proposed pulse generator is also more efficient than most of the other designs if the total energy consumption per pulse is normalized with respect to the output peak-to-peak voltage.

Table 3.1: Summary of pulse generator characteristics.

	Process	**Supply (V)**	**Power (mW)**	**PRF (MHz)**	**Energy (pJ/p)**	**Pulse Amplitude**	**Pulse Duration (ns)**
[6]	90nm CMOS	1.0	129	1800	–	220mV	0.53
[9]	180nm CMOS	1.8	76	400	–	195mV	<1.0
[12]	180nm CMOS	1.8	–	750	12	30mV	0.5
[16]	180nm CMOS	1.8	–	500	0.56	–	1.0
[18]	180nm CMOS	1.8	12.6	1160	–	123mV	0.28
[20] [1]	90nm CMOS	1.0	3.0	5000	–	200mV	0.045
[86]	350nm SiGe	2.4	2.5 [2]	1000	2.5 [2]	300mV	0.6
[57]	130nm CMOS	1.2	3.84	100	9 [3]	1.42V	0.46
[61]	180nm CMOS	–	50	1000	50	110mV	0.14–1.0
[62]	180nm CMOS	–	–	2500	25	80mV	0.12–>1.0
This work	**130nm CMOS**	**1.2**	**3.8**	**910**	**4.2**	**150mV**	**0.5–0.9**

[1] Simulation results.
[2] Does not include 6mW of power in output buffer.
[3] Does not include 3.2mW of power in MOS CML gates.

3.3 Summary

A new energy-efficient tunable pulse generator was presented in this chapter using 0.13 μm CMOS for high-data-rate 3.1–10.6 GHz UWB applications. A current-starved ring

oscillator is quickly switched on and off for the pulse duration, and the amplitude envelope is shaped using a variable passive CMOS attenuator. The attenuator is controlled with an impulse which is created by a low-power, tunable glitch generator (CMOS NOR gate). Several UWB pulses were measured and demonstrated, with the pulse time duration varying over a wide range (500 ps – 900 ps). The spectrum roll-off is also quite sharp with high out-of-band rejection to help satisfy the FCC mask. The entire circuit operates in switched-mode with a low average power consumption of less than 3.8 mW at 910 MHz PRF, or below 4.2 pJ of energy per pulse. It occupies a total area of 725×600 μm^2 including bonding pads and decoupling capacitors, and the active circuit area is only 360×200 μm^2.

Chapter 4

Quadrature Tunable UWB Pulse Generator

4.1 Introduction

In this chapter, a new quadrature pulse generator is proposed in 0.13 μm CMOS for short-range 22–29 GHz UWB vehicular radar [42]. It can be used in pulsed UWB vehicular radar transceivers to provide template pulses for quadrature pulse correlation and detection, or to enable quadrature phase modulation for enhanced pulse compression, detection, and interference mitigation. A quadrature inductor-capacitor (LC) oscillator operating at 24 GHz is used in this work, which can be quickly switched off and on between pulses to reduce power consumption, LO leakage, LO self mixing and DC offsets. A new switching technique is introduced in the LC oscillator to create a large initial condition upon startup and reduce the settling time to about 0.5 ns, by injecting a short-time current impulse with large harmonic components out to 24 GHz. It also locks the initial phase of the oscillations to

the input clock for high pulse-to-pulse coherence. The measured output phase noise matches that of the clock signal, yielding a low phase noise of -70 dBc/Hz at 1 kHz offset, and -100 dBc/Hz at 1 MHz offset. A π-network attenuator then modulates the LO signal to generate the UWB pulse. The attenuator is controlled with two inverted impulses, which can be readily tuned to vary the width of the UWB pulse over a wide range from 375 ps to more than 1 ns. This pulse shaping technique offers a low power solution with a high bandwidth and tunable performance, compared to using a variable gain amplifier or an LC filter. It also provides good control of the radiated frequency spectrum, as the –10 dB bandwidth can reach 4.9 GHz and the out-of-band rejection can exceed 23 dB to help satisfy the FCC mask. The pulse generator can operate with a pulse repetition frequency (PRF) as high as 600 MHz, allowing it to be readily shared between the transmitter and receiver with a time delay as short as 1.66 ns. The circuit is fully differential and operates in switched mode with zero static current for a low power consumption of only 2.2 mW and 14.8 mW at PRFs of 50 MHz and 600 MHz respectively, or less than 11 pJ of energy for each of the four differential quadrature pulses. The integrated circuit (IC) occupies a die area of 0.94 mm^2 including bonding pads and decoupling capacitors, and the active circuit area is only 0.41 mm^2.

4.2 Circuit Architecture and Design

A circuit schematic of the 22–29 GHz UWB pulse generator is shown in Fig. 4.1. It consists of a quadrature LC local oscillator (LO), buffers, a glitch generator and variable π-network attenuators. An inverter chain first sharpens the rising/falling edge of the clock signal (CLK), which is used to turn the LO and buffers on and

off. The clock signal (TRIG) then triggers the glitch generator, where a NAND gate operates on the rising-edge and its delayed inverse to form a short impulse (V_{CTRL}). This impulse and its inverse control the variable π-network attenuators to shape the amplitude envelope of the LO signals (LO_{I+}, LO_{I-}, LO_{Q+}, LO_{Q-}) and form the desired quadrature UWB pulses at the outputs ($I+$, $I-$, $Q+$, $Q-$). Fig. 4.2 illustrates the timing of the clock signals (CLK, TRIG) and the generated pulse waveforms. Note that the glitch generator clock signal (TRIG) is delayed with respect to the LO's clock signal (CLK) using current-starved inverters (Fig. 4.1). This in turn delays the onset of V_{CTRL}, allowing sufficient time for the oscillations to stabilize and reach steady-state before amplitude shaping takes place. The delay between TRIG and CLK can be tuned using the control voltage V_{DELAY} (Fig. 4.1).

4.2.1 Pulsed Quadrature LC Oscillator

The high oscillation frequency of 24 GHz required for the pulsed quadrature oscillator necessitates the use of an LC resonator-based oscillator as opposed to a ring oscillator. An LC oscillator has a higher quality factor, lower phase noise and lower power consumption compared to a ring oscillator. However the higher quality factor leads to a longer settling time (> 1 ns), and a new startup technique is needed to reduce the settling time significantly for a low energy consumption.

A common way of implementing a differential LC oscillator is to use a cross-coupled pair of transistors to generate the negative resistance required and overcome the losses in the LC tank. The resistance R_{IN} seen looking into the cross-coupled pair is given by $-2/g_m$, where g_m is the transconductance of each of the transistors. Therefore, with sufficient device size and biasing current, a negative resistance larger

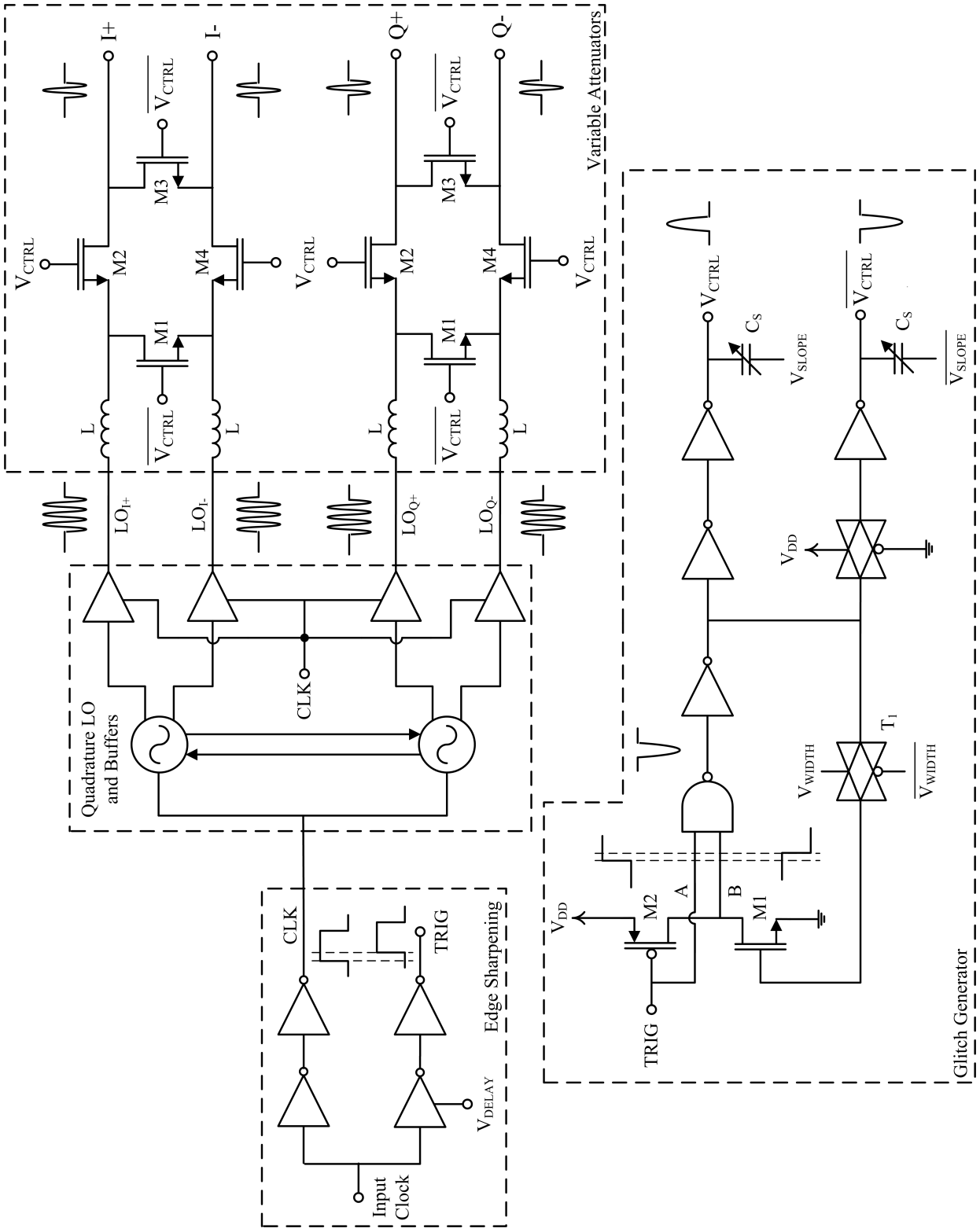


Figure 4.1: Proposed UWB pulse generator circuit diagram.

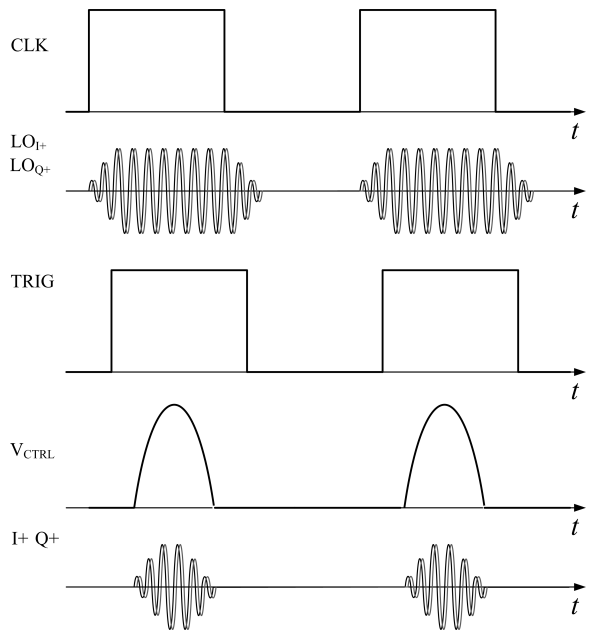


Figure 4.2: Pulse generator clock timing and output waveforms.

than the equivalent parallel resistance of the tank (R_P) can be realized to sustain the oscillations.

The quadrature LC oscillator circuit designed in this work is shown in Fig. 4.3. It consists of two cross-coupled oscillators that are connected together through the body terminals (or back-gates) of the PMOS devices M_{P1}, M_{P2}, M_{P3} and M_{P4}. Adding cross-coupled PMOS transistors ($M_{P1}-M_{P2}$ and $M_{P3}-M_{P4}$) above the cross-coupled NMOS transistors ($M_{N1}-M_{N2}$ and $M_{N3}-M_{N4}$) increases the transconductance per unit current (g_m/I) for a low power consumption. It also improves the symmetry and phase noise of the oscillations as shown in [87, 88]. Quadrature-coupling the two oscillators using the body terminals of the core PMOS devices saves power as opposed to using additional transistors which will also add noise [89, 90]. The resistors R_B are added for DC biasing of the body terminals and the capacitors C_B for AC coupling. The free-running oscillation frequency ω_0 for each oscillator is specified by the resonant

frequency of the LC tank $1/\sqrt{LC}$, where L is the value of the on-chip spiral inductor and C is the total parasitic capacitance at the output nodes. The inductors used in this circuit are symmetric spirals, and are 100 μm $\times$ 100 μm in size with one turn and 7.5 μm trace width. An electromagnetic (EM) simulation of the inductors predicts an inductance of 0.16 nH and a quality-factor (Q) of approximately 26 at 24 GHz. The total capacitance C including the parasitic capacitance of the cross-coupled transistors, common-source buffers ($M_{N5} - M_{P5}$, $M_{N6} - M_{P6}$, $M_{N7} - M_{P7}$ and $M_{N8} - M_{P8}$) and metal interconnects is about 0.27 pF to provide oscillation at 24 GHz.

The initial startup transient of the oscillations can be characterized by the well-known "van der Pol" non-linear differential equation [91] given by:

$$\ddot{v} + \epsilon\omega_0 \left[v^2 - 1\right] \dot{v} + \omega_0^2 v = 0 \tag{4.1}$$

where $\epsilon = (g_m - 1/R_P)\sqrt{L/C}$ is a damping factor. An approximate solution to (4.1) for the differential output voltage v can be found as [92]:

$$v(t) = \frac{2v_0}{\sqrt{1 + \left(\left(\frac{2v_0}{v(0)}\right)^2 - 1\right) e^{-\epsilon\omega_0 t}}} \cos\left(\omega_0 t - \phi\right) \tag{4.2}$$

where $v(0)$ is the initial condition and $2v_0$ is the steady-state oscillation amplitude. The oscillation phase ϕ depends on the initial conditions. The settling time t_s for the oscillation $v(t)$ to reach 90% of its steady state value ($2v_0$) can be derived from (4.2) [92]:

$$t_s \approx \frac{Q_{res}}{\omega_0 \left(A_{OL} - 1\right)} \left[2 \ln\left(\frac{2v_0}{v(0)} - 1\right) + 1.45\right] \tag{4.3}$$

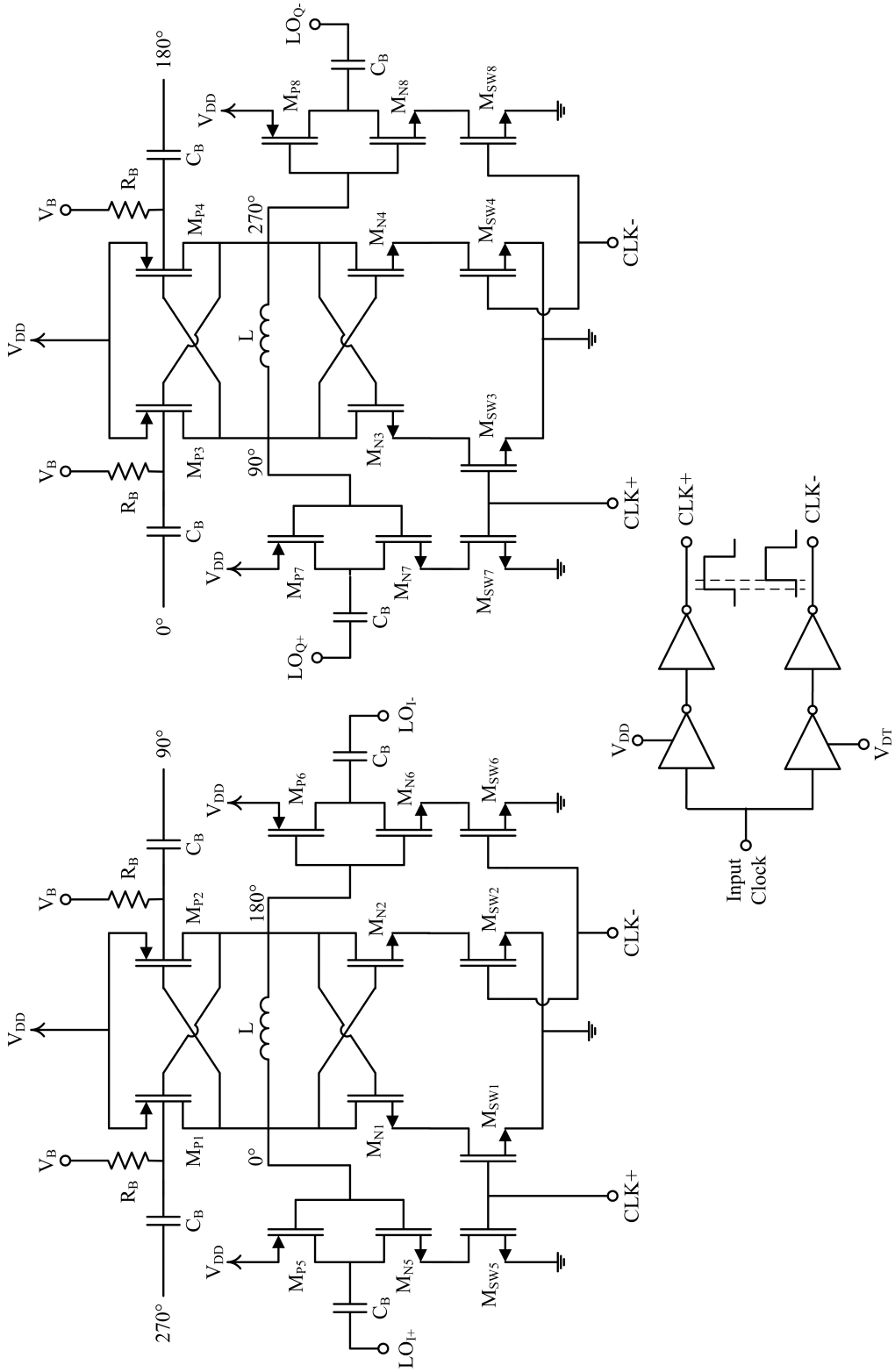


Figure 4.3: Circuit schematic of quadrature LC oscillators and buffers.

where $A_{OL} = g_m R_P$ is the open-loop gain and $Q_{res} = R_P\sqrt{C/L}$ is the quality-factor of the LC tank. It is clear that the settling time t_s is shorter for larger initial conditions $v(0)$. In addition, the settling time can be reduced by decreasing $\frac{Q_{res}}{\omega_0(A_{OL}-1)}$, which can be approximated for $A_{OL} >> 1$ as:

$$\frac{Q_{res}}{\omega_0\left(A_{OL}-1\right)} \approx \frac{Q_{res}}{\omega_0 A_{OL}} = \frac{R_P\sqrt{C/L}}{g_m R_P/\sqrt{LC}} = \frac{C}{g_m} \tag{4.4}$$

From (4.4), the settling time t_s can be reduced by decreasing the tank capacitance C or increasing the transistor transconductance g_m. Thus the capacitance C is minimized to include only the parasitic capacitance of the cross-coupled transistors (M_{N1}, M_{N2}, M_{P1}, M_{P2}) and the connecting common-source buffers ($M_{N5} - M_{P5}$ and $M_{N6} - M_{P6}$).

The biasing currents of the two differential oscillators are switched on and off using a pair of NMOS switches ($M_{SW1} - M_{SW2}$ and $M_{SW3} - M_{SW4}$) as shown in Fig. 4.3. Similarly the biasing currents of the four output common-source buffers are switched using NMOS switches $M_{SW5} - M_{SW6}$ and $M_{SW7} - M_{SW8}$. By switching on one side of each differential oscillator before the other (i.e. switching on M_{SW1} before M_{SW2}, and M_{SW3} before M_{SW4}), a current I_{inj} initially flows through the LC tank as shown in Fig. 4.4. The current-starved inverters shown in Fig. 4.3 are used to introduce a short delay between the clock signals $CLK+$ and $CLK-$ that trigger the pair of switches, and thus the initial current I_{inj} only flows for a short time. In effect, a current impulse with a short time duration and high frequency content out to 24 GHz is injected through the LC tank. This creates a large initial condition ($v(0)$) for a short settling time as indicated by (4.3) [92]. It also sets the initial phase of the oscillations at the turn-on instant. By setting the same initial oscillation phase at each clock rising edge, the LO pulses are phase coherent with the input clock and

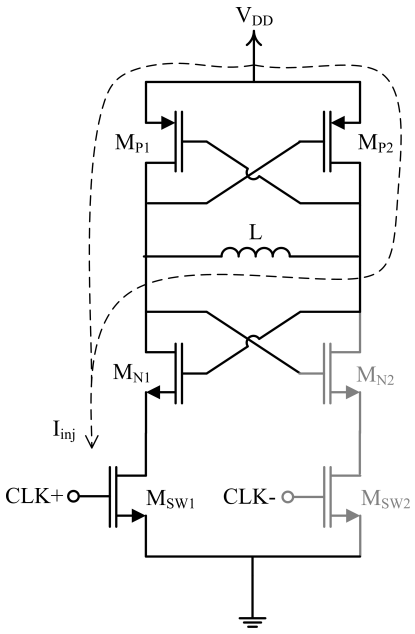


Figure 4.4: Illustration of the current injected into the differential LC oscillator.

pulse-to-pulse coherency is maintained. Note that the delay Δt between the clock signals $CLK+$ and $CLK-$ can be tuned using the control voltage V_{DT} (Fig. 4.3) to vary the time duration of the current impulse I_{inj}.

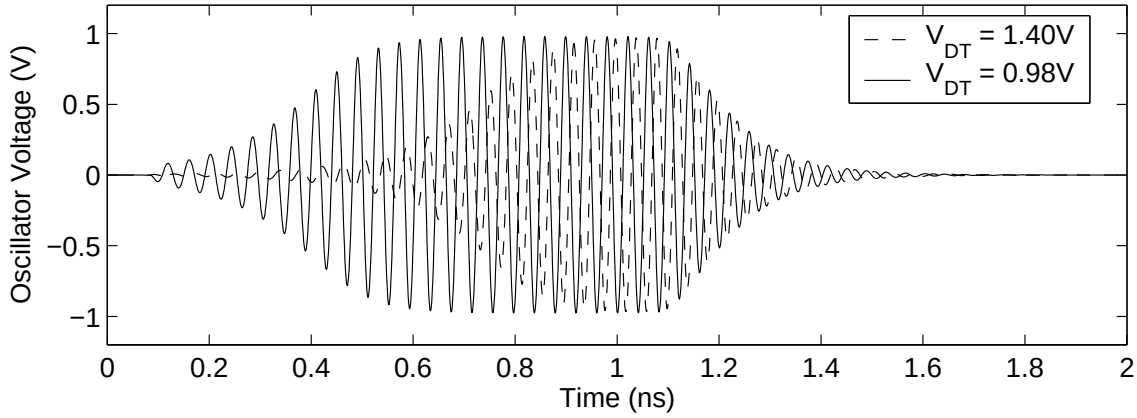
Time-domain simulations of the oscillator differential output voltage $v(t)$ are shown in Fig. 4.5, with different delays Δt introduced between the clock signals $CLK+$ and $CLK-$ using the control voltage V_{DT}. The input clock frequency is set to 500 MHz for these simulations. Fig. 4.5a shows the output voltage for V_{DT} = 0.98 V and Δt = 18 ps in comparison with that obtained for $V_{DT} = V_{DD}$ = 1.4 V and Δt = 0 ps. It is clear that the settling time is reduced by roughly a factor of 2 when a delay of Δt = 18 ps is applied. Fig. 4.5b shows the output voltage with V_{DT} set to 0.8 V, 0.98 V and 1.2 V, and it is clear that the shortest settling time is achieved with V_{DT} = 0.98 V and Δt = 18 ps. The injected current impulse I_{inj} is also illustrated in Fig. 4.6a for the same control voltages, and its frequency spectrum is plotted in

Fig. 4.6b. The injected current impulse for $V_{DT} = 0.98$ V has an amplitude of 4 mA and a short time duration of about 48 ps. It also has a large frequency component at 24 GHz compared to the injected current impulses for $V_{DT} = 0.8$ V and $V_{DT} = 1.2$ V, yielding a relatively large initial condition voltage $v(0)$ of about 45 mV for the shortest settling time.

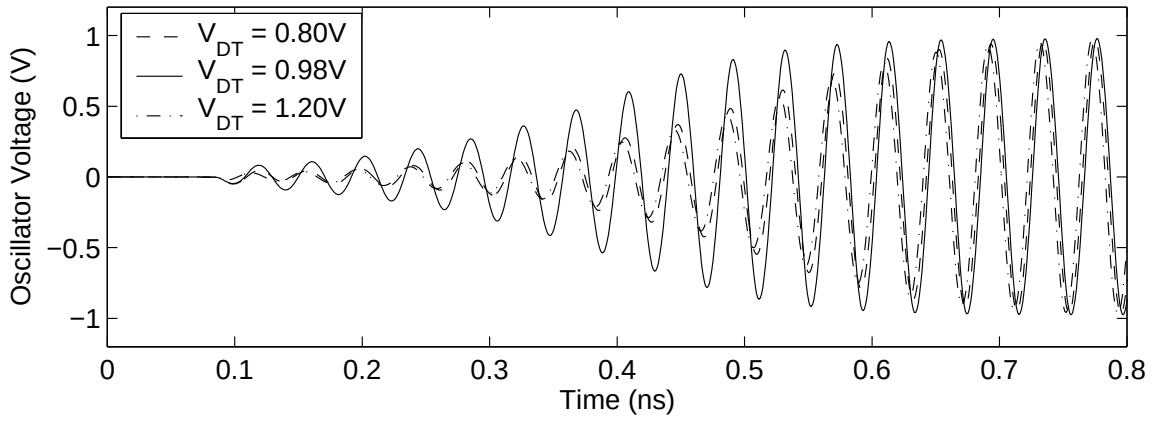
Timing diagrams for the clock signals ($CLK+, CLK-$) and the differential quadrature oscillating waveforms ($LO_I = LO_{I+} - LO_{I-}$ and $LO_Q = LO_{Q+} - LO_{Q-}$) are shown in Fig. 4.7 for $V_{DT} = 0.98$ V. It is clear that the LO signals (LO_I and LO_Q) reach steady-state within 0.5 ns from startup (i.e. $CLK+$ rising edge). The LO remains on for the duration of the clock signal $CLK+$ when it is in logic 1 to allow sufficient time for amplitude shaping using the generated impulse signals.

4.2.2 Glitch Generator

The sub-nanosecond glitch generator [31, 59, 61, 84] shown in Fig. 4.1 creates a wideband impulse having the required width and shape. The pulse produced is also tunable to allow for different pulse durations and bandwidth. The circuit is implemented using low-power CMOS digital logic, providing full voltage swing required to operate the variable attenuator. A Gaussian-like pulse is created in a glitch fashion by feeding the NAND gate with a clock rising edge along with its delayed inverse (A and B in Fig. 4.1). The short duration where both signals are high causes the NAND gates output to be temporarily pulled low thus generating the pulse (Fig. 4.1). The propagation time through the feedback loop, which consists of the propagation time through the NAND gate, the following inverter and the charging time of transistor M_1, specifies this duration and thus the pulse width. A CMOS transmission gate T_1 is

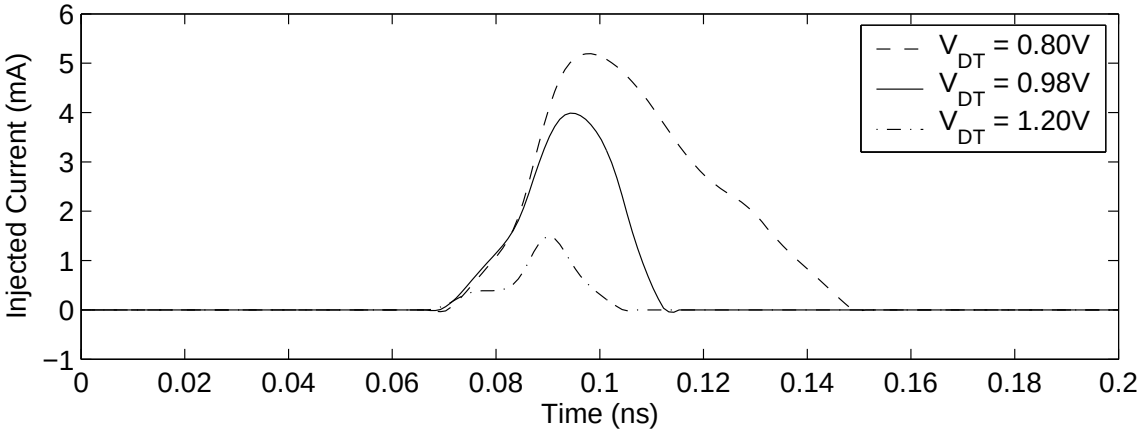


(a)

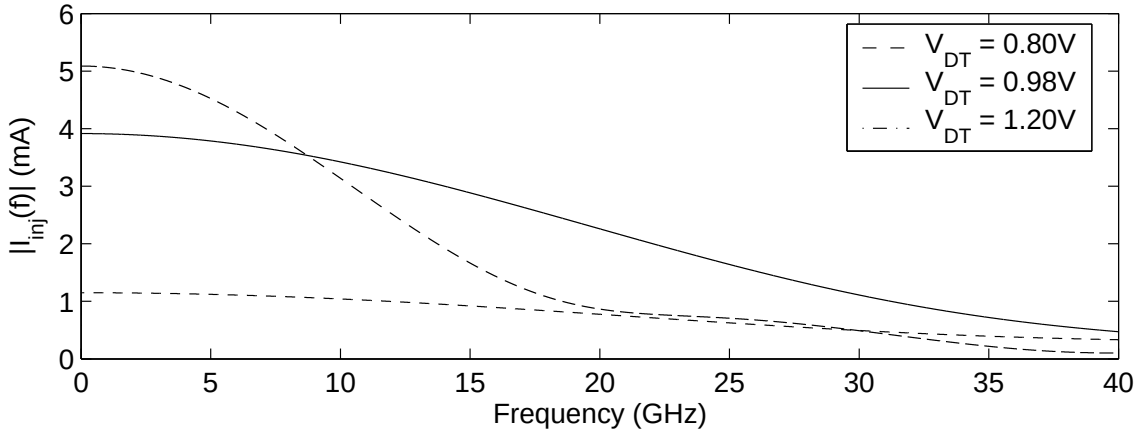


(b)

Figure 4.5: Simulated oscillator output voltage $v(t)$ for (a) V_{DT} set to 0.98 V and 1.4 V, and (b) V_{DT} set to 0.8 V, 0.98 V and 1.2 V.

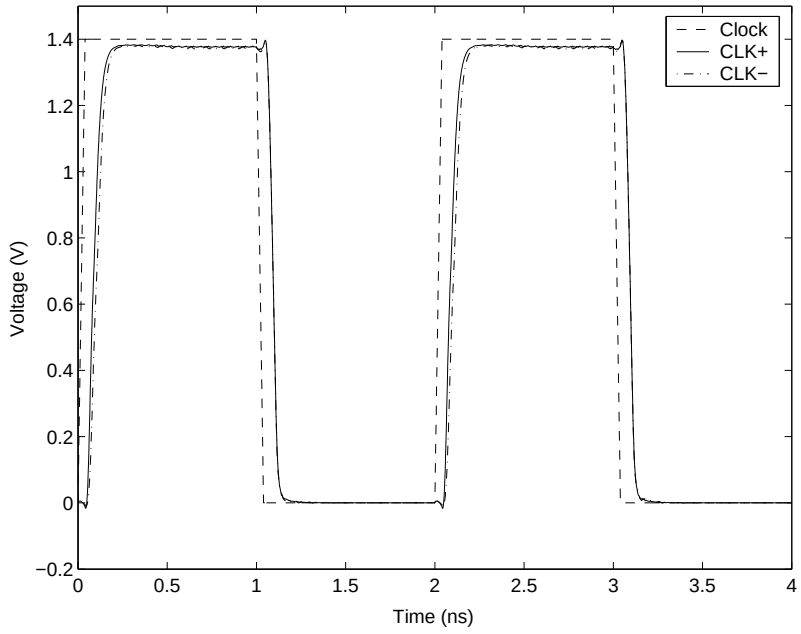


(a)

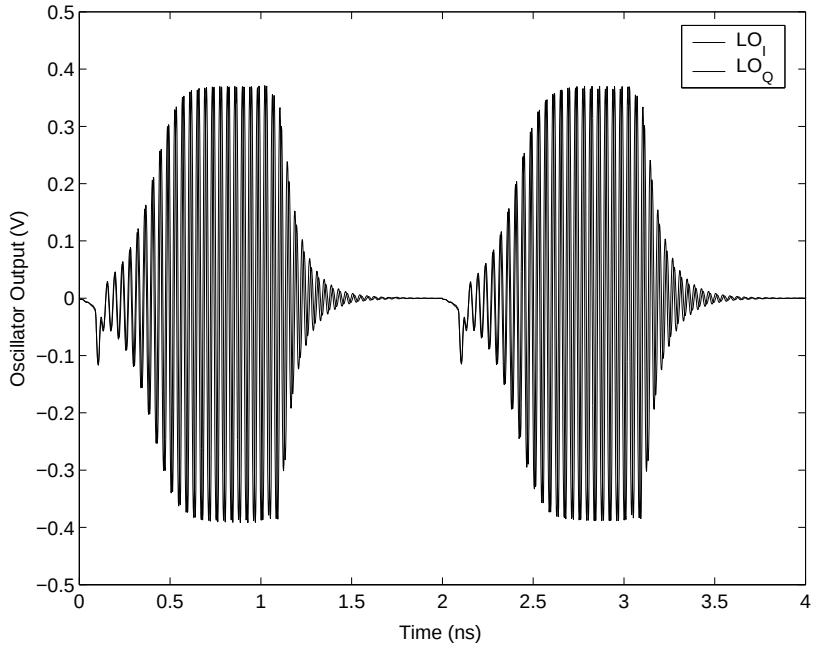


(b)

Figure 4.6: Simulated injected current impulse I_{inj} for V_{DT} set to 0.8 V, 0.98 V and 1.2 V: (a) time-domain waveform and (b) frequency spectrum.



(a)



(b)

Figure 4.7: Simulated timing diagrams for: (a) clock signals, and (b) oscillator waveforms.

added in the feedback path to control the charging (RC) time constant of transistor M_1. By varying the control voltage V_{WIDTH}, the charging time-constant changes, which tunes the generated pulse width. Two cascaded inverters serve as a buffer to drive the variable attenuator for the generated pulse V_{CTRL}, while a transmission gate followed by an inverter realize the inverted pulse $\overline{V_{CTRL}}$. In addition, varactors C_S are connected to the outputs V_{CTRL} and $\overline{V_{CTRL}}$ as shown in Fig. 4.1 to vary the loading capacitance and thus tune the rise/fall times (slopes) of the generated pulses. Here a NAND gate is employed instead of a NOR gate for faster operation and shorter pulse time durations. This is because the output of a NAND gate is pulled down using two NMOS devices connected in series, as opposed to the NOR gate where the output is pulled up using two series-connected PMOS devices which are inherently slower.

The optimum size for each device in the glitch generator is determined by extensive simulation. Simulations indicate that pulses with different time durations can be generated, with the minimum duration being below 400 ps and the maximum duration being bounded by the on period of the clock signal (TRIG). The pulse peak voltage is equal to the supply voltage of $V_{DD} = 1.4$ V for all pulse durations.

4.2.3 Variable Attenuator

A variable passive attenuator is used for pulse shaping as opposed to a variable gain amplifier for instance since the attenuator has a wider bandwidth and higher dynamic range with comparable devices at high frequencies. It also consumes zero DC power which is useful in minimizing the energy consumption per pulse. However these benefits come at the cost of insertion loss. An inductor-capacitor (LC) filter is typically difficult to control for different pulse durations and shapes.

The variable attenuator consists of two series NMOS devices M_2 and M_4 connected to two shunt NMOS devices M_1 and M_3 in a π-network configuration as shown in Fig. 4.1. These are driven by the glitch generator pulses V_{CTRL} and $\overline{V_{CTRL}}$. When V_{CTRL} is low and $\overline{V_{CTRL}}$ is high, the series NMOS devices are off and the shunt NMOS devices are on, blocking the LC oscillator's signal and shorting the output for maximum attenuation. When V_{CTRL} is high and $\overline{V_{CTRL}}$ is low, the opposite occurs and the signal is passed to the output with minimum loss. This in effect performs the desired envelope modulation as V_{CTRL} and $\overline{V_{CTRL}}$ vary with time.

The π-network attenuator configuration offers a higher attenuation range than using a single NMOS device but at the cost of a higher insertion loss and a lower bandwidth. Transistor M_1 also serves as a load for the LO when the control impulse V_{CTRL} is low. This ensures an approximately constant loading impedance at the LO outputs regardless of the state of the impulse. The design of the variable attenuator involves several tradeoffs, such as minimizing the on-state insertion loss, the off-state LO leakage and the pulse rise and fall times. Larger devices tend to reduce the insertion loss and increase the attenuation range, however the increased parasitic capacitance adversely affects the bandwidth. In this design, on-chip spiral inductors are connected in series (series-peaking) as shown in Fig. 4.1 to absorb the transistors' parasitic capacitances and increase the bandwidth. The AC voltage gain $|A_V|$ of the attenuator has been simulated and plotted in Fig. 4.8. The minimum loss at the maximum gate voltage of $V_{CTRL} = V_{DD} = 1.4$V is about 4.0 dB. It is also evident that the maximum attenuation achieved at the center frequency of 24.0 GHz is 41 dB, giving an attenuation range of more than 30 dB. Note that 30 dB of attenuation range is sufficient since the LO can be switched off shortly after the pulse to mitigate

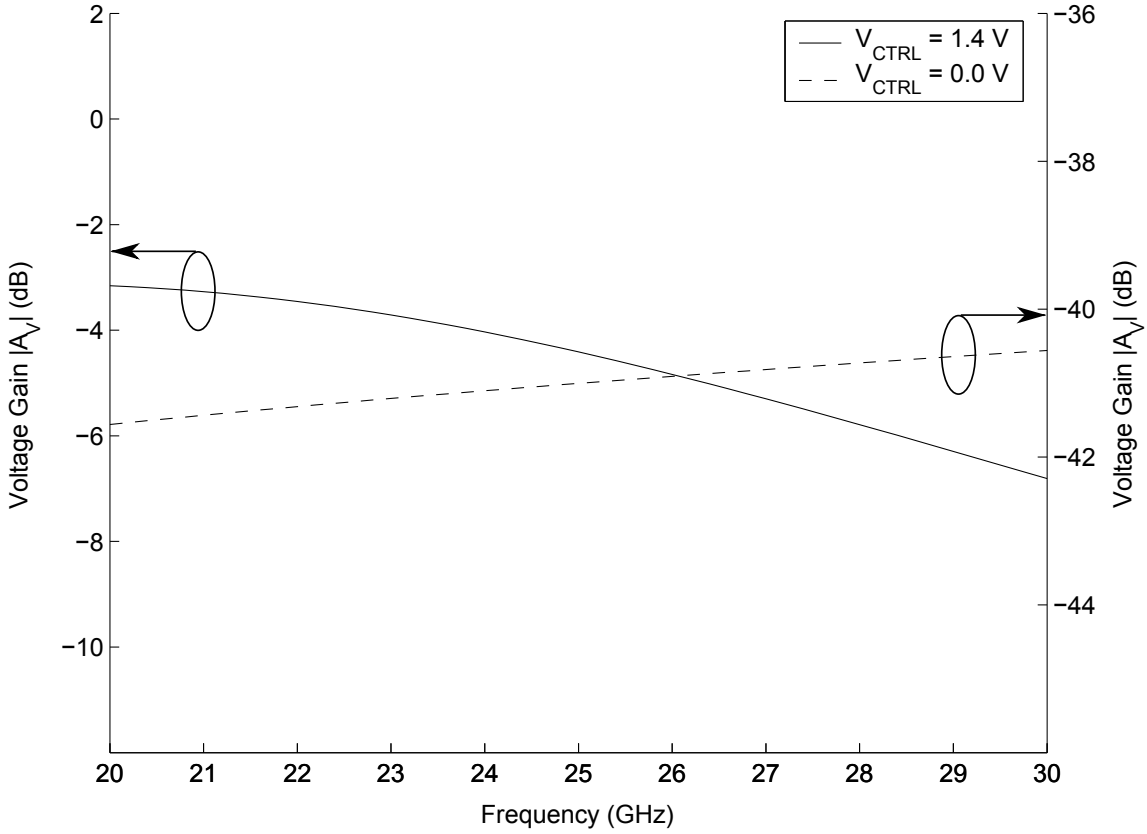


Figure 4.8: Simulated voltage gain $|A_V|$ of the variable attenuator in the on-state ($V_{CTRL} = 1.4$ V) and off-state ($V_{CTRL} = 0.0$ V).

LO leakage. Furthermore, the transmission in the on state remains quite flat, with less than 2.8 dB deviation over the 22–29 GHz UWB bandwidth.

4.3 Measurement Results

4.3.1 Pulsed Quadrature Oscillator

The pulsed quadrature oscillator was first fabricated and characterized separately in 0.13 μm CMOS. A photograph of the IC is shown in Fig. 4.9. It occupies a die area of 0.54 mm^2 including bonding pads, decoupling capacitors and the chip guard ring

(plus chamfer regions), while the core circuit area is 0.17 mm^2.

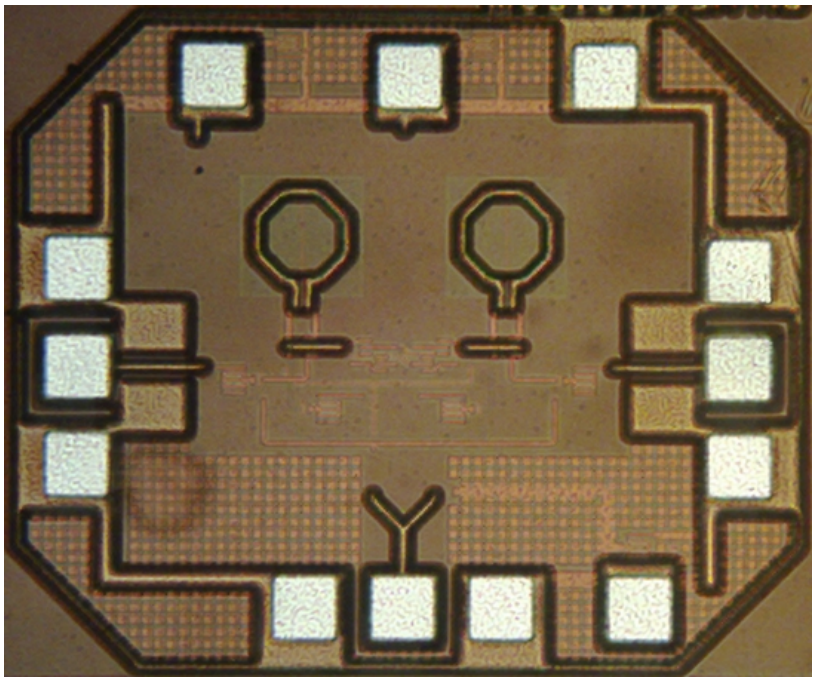


Figure 4.9: Photograph of quadrature pulsed oscillator IC.

The pulsed oscillator IC was measured directly on-wafer using 40 GHz coplanar waveguide (CPW) probes and DC probes. The Agilent 50 GHz spectrum analyzer (E4448A) was used to examine the output power spectrum and phase noise. Fig. 4.10 shows the measured output power spectrum when the quadrature oscillator is in free running mode, i.e. the input clock is held at logic high (V_{DD} = 1.4V). The spectrum plot is centered at 23.9 GHz and covers a span of 500 MHz. It is clear that the free-running output power level is about –4.5 dBm at a frequency of 23.9 GHz. A few spurs are also visible in the spectrum, which are most likely due to power supply noise and electromagnetic interference (EMI). For example, spurs at offsets of about 100 MHz from the 23.9 GHz carrier are most likely caused by interference from FM radio operating at around 100 MHz. The phase noise of the free-running oscillations

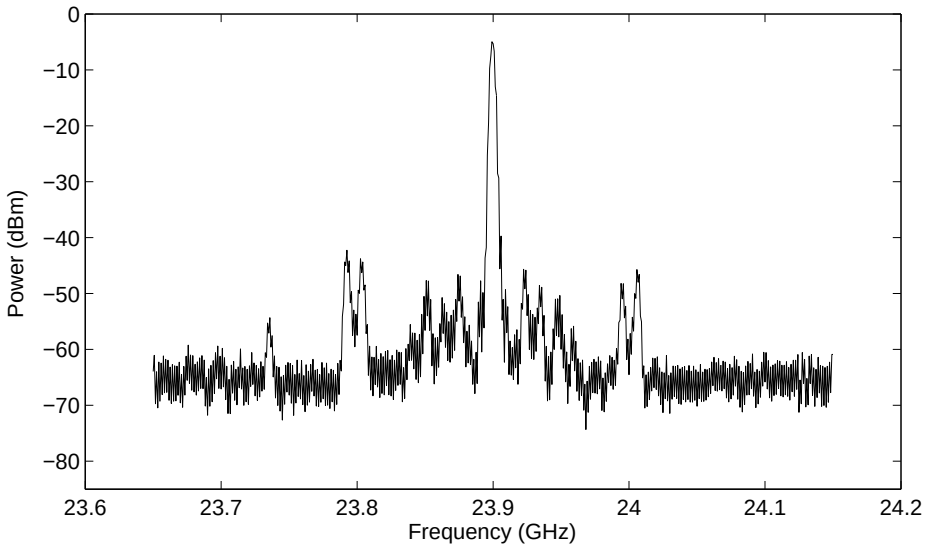


Figure 4.10: Measured free-running output spectrum over a span of 500 MHz centered at 23.9 GHz.

was measured and is plotted in Fig. 4.11 against the simulated phase noise. It is apparent that there is good agreement between measurement and simulation, and that a relatively low phase noise of -100 dBc/Hz is achieved at 1 MHz offset. The oscillation frequency can be tuned using the body biasing voltage V_B of the PMOS devices M_{P1}–M_{P4} (Fig. 4.3), and Fig. 4.12 shows the measured oscillation frequency and output power level with different values of V_B. The results indicate that the tuning range is about 600 MHz, over which the output power varies by less than $\pm$1.5 dB.

The pulsed output power spectrum was also measured directly using a spectrum analyzer over a span of 8 GHz and is plotted in Fig. 4.13a. The input clock is a periodic sinusoidal signal which is readily converted on-chip into a digital square wave using the edge sharpening inverters (Fig. 4.1). The clock frequency was set to about 500 MHz (508 MHz) for this measurement. The power spectrum exhibits peaks

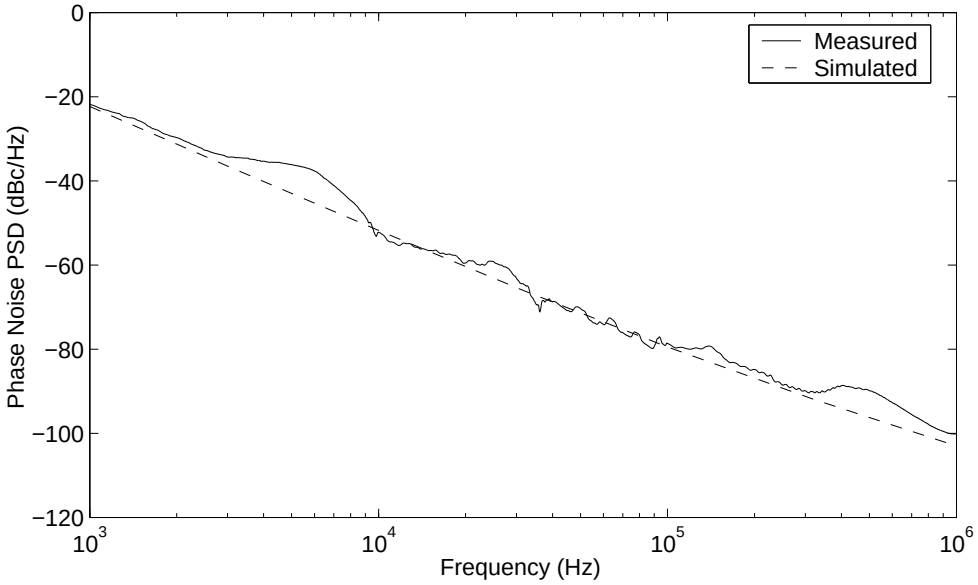


Figure 4.11: Measured and simulated free-running output phase noise PSD.

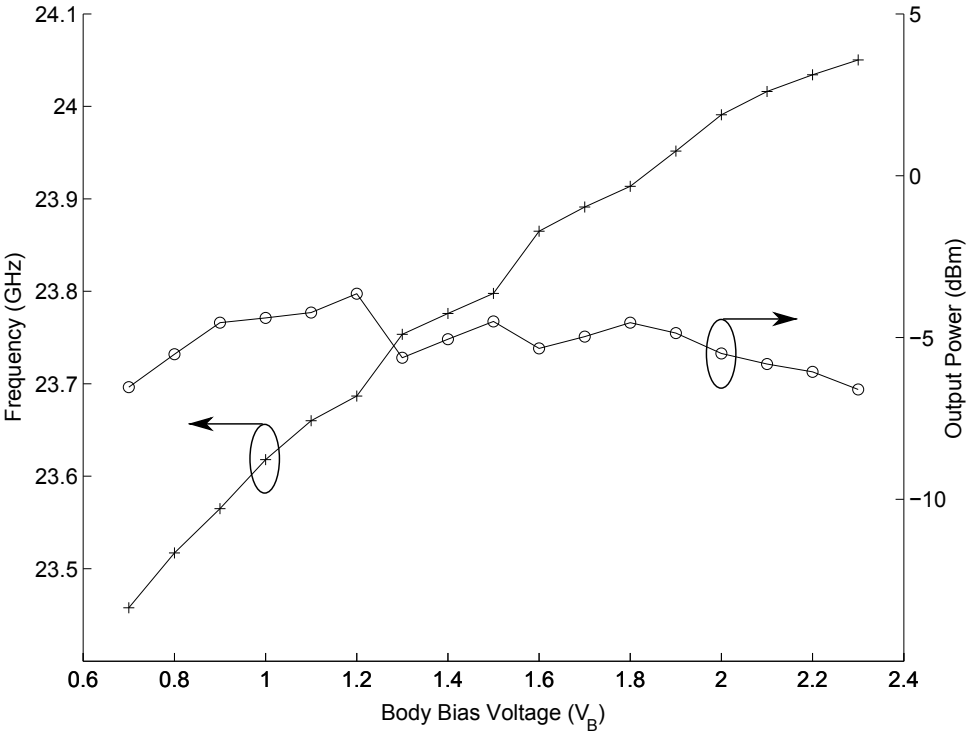


Figure 4.12: Measured oscillation frequency and output power with different values of V_B.

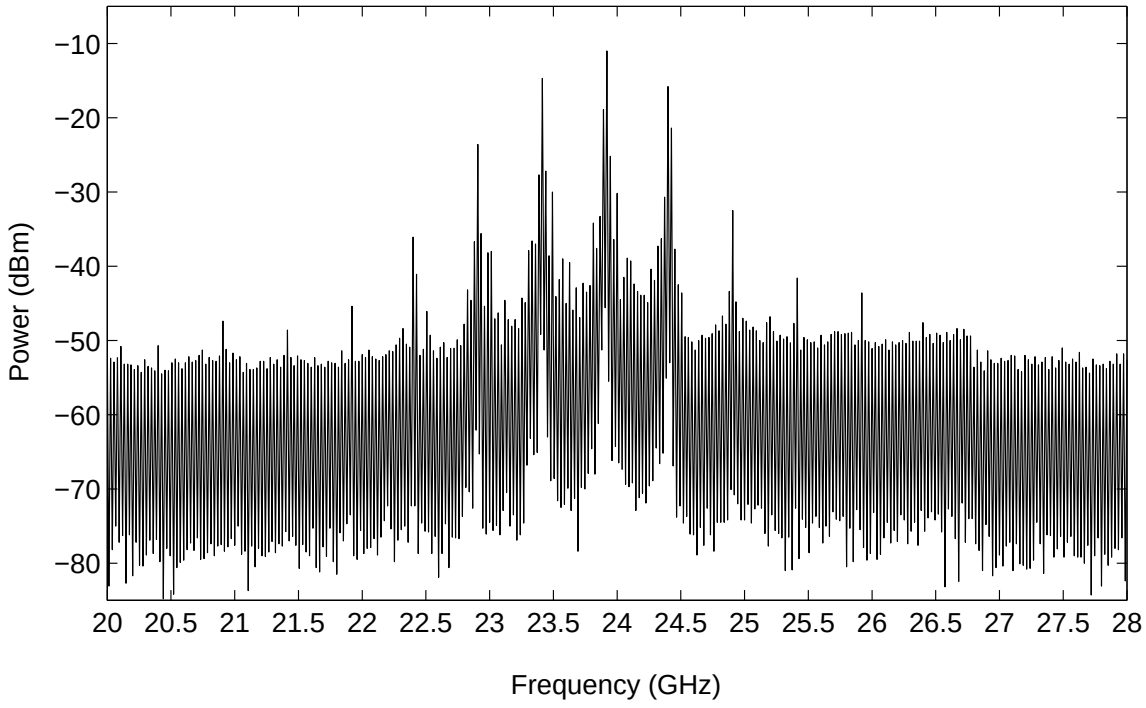
at multiples of the PRF since the output is a periodic (unmodulated) extension of the pulses. It is also apparent that the generated harmonic components are coherent and well-defined. Fig. 4.13b shows the generated peak at 23.92 GHz in more detail over a span of only 1 MHz, clearly showing stable and locked operation.

Fig. 4.14 shows the measured phase noise of the generated pulsed output at 23.92 GHz. The measured phase noise of the clock reference and that of the free-running output shown in Fig. 4.11 are also included in Fig. 4.14 for comparison. As depicted in Fig. 4.14, the output phase noise matches that of the clock reference but is approximately 33 dB higher. This corresponds to the frequency ratio between the output and the clock reference since 20 log (23.92/0.508) = 33 dB. Fig. 4.14 verifies that the 24-GHz pulsed oscillator is phase locked to the 500 MHz clock reference, achieving a relatively low phase noise of –62 dBc/Hz at 100 Hz, –70 dBc/Hz at 1 kHz and –65 dBc/Hz at 10 kHz. This amounts to a low integrated rms jitter of 720 fs from 100 Hz to 1 MHz.

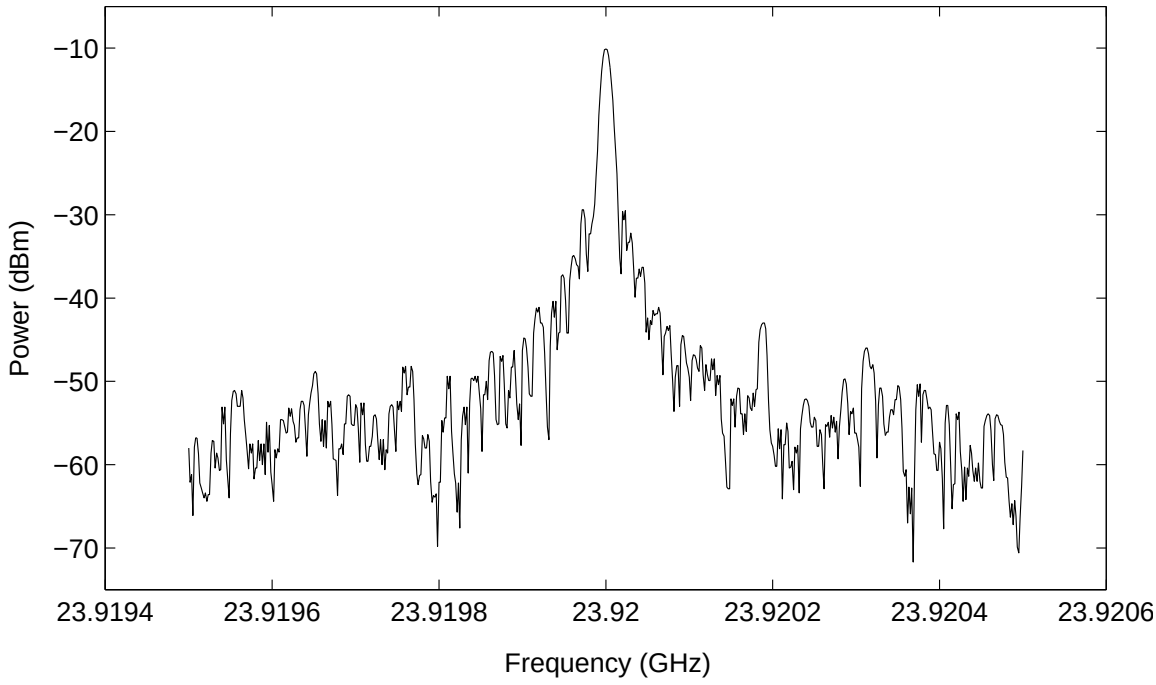
The locking bandwidth of the oscillator was verified in both continuous and pulsed operation. In continuous operation, the input clock is held at logic high ($V_{DD} = 1.4$V) and a 24 GHz sinusoidal signal is added using a bias-T for injection locking. The locking bandwidth f_L of the oscillator can be characterized by the well-known "Adler" formula given by:

$$f_L = \frac{f_0}{Q}\sqrt{\frac{P_{inj}}{P_0}} \tag{4.5}$$

where f_0 is the free-running oscillator frequency, P_{inj} is the injected power level, P_0 is the oscillator output power level, and Q is the quality factor of the LC tank. Thus the locking bandwidth f_L can be controlled by the injected-to-output power ratio P_{inj}/P_0. Fig. 4.15 shows the measured locking bandwidth for different injected power levels. It



(a)



(b)

Figure 4.13: Measured pulsed output spectrum at 24 GHz: (a) 8 GHz span and (b) 1 MHz span.

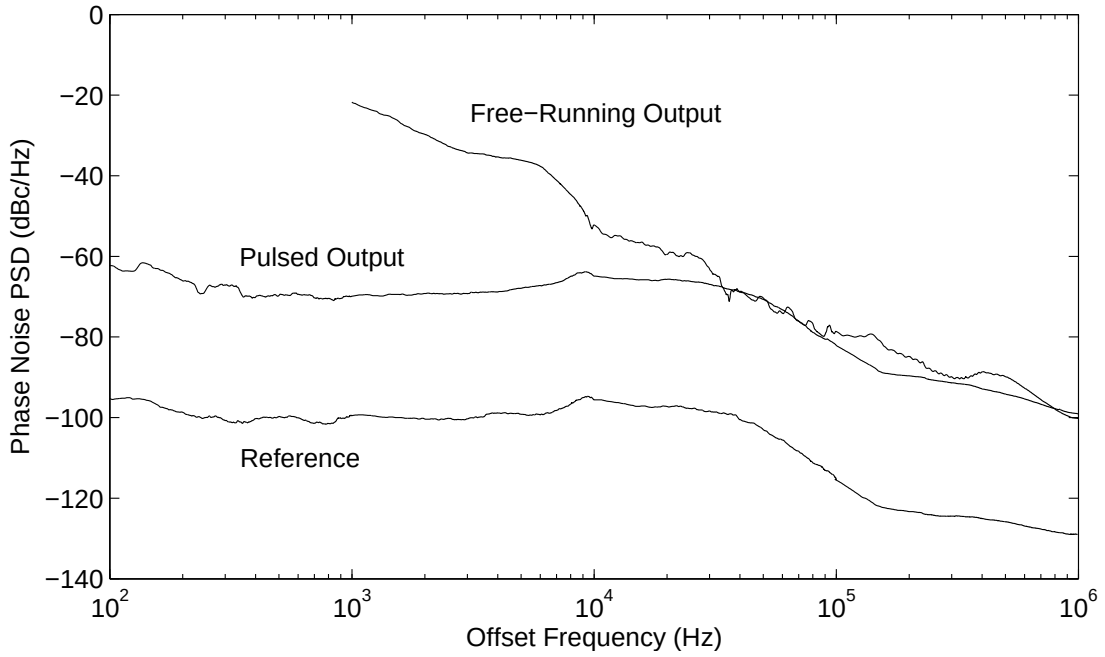


Figure 4.14: Measured phase noise of pulsed output at 24 GHz.

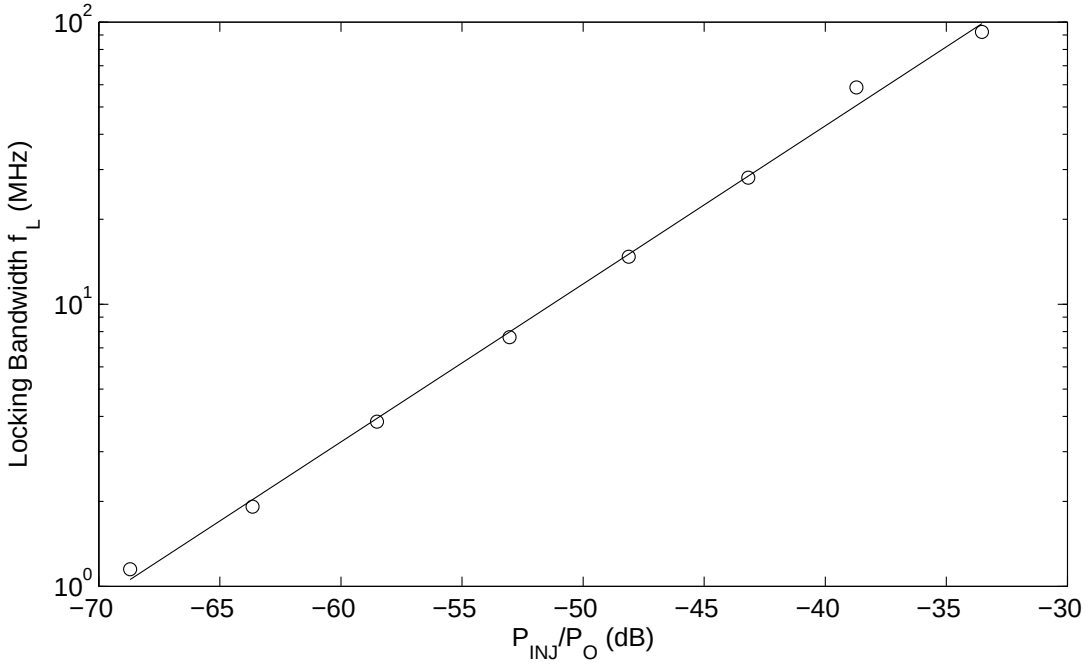


Figure 4.15: Measured locking bandwidth for different levels of injected power P_{inj}.

is clear that the locking bandwidth varies with the injected power according to (4.5), and that a locking bandwidth of 100 MHz is achieved at a low injected power level ($P_{inj}/P_0 \approx$ -33 dB). In pulsed operation, the oscillator output voltage amplitude and power level P_0 at startup are small compared to those in steady-state. The current impulse I_{inj} injected at startup can also have a relatively large frequency component at 24 GHz as shown in section 4.2.1. Therefore a higher injected-to-output power ratio P_{inj}/P_0 can be achieved for a wider locking bandwidth. The locking bandwidth was measured in pulsed operation and it was found to exceed 11 MHz around the 500 MHz input clock frequency. This translates to a locking bandwidth of more than 500 MHz at the output frequency of 23.9 GHz, thus ensuring phase-coherent pulsed operation.

The oscillator center frequency may drift due to changes in process, supply voltage and temperature (PVT). Simulations of the center frequency as a function of PVT variations are shown in Fig. 4.16. Corner simulation is performed in three modes (SS, TT, FF) to capture variations in process at the nominal supply voltage of 1.4 V and temperature of 25 °C. From Fig. 4.16a, the oscillator frequency varies by about ±1.6% due to the process. Meanwhile, as the temperature changes from 0 °C to 75 °C in typical process conditions and at the nominal supply voltage, the oscillation frequency shows a variation of less than ±0.75% (Fig. 4.16b). In addition, the oscillation frequency changes by only ±0.15% (Fig. 4.16c) as the power supply voltage changes by ±0.1 V at nominal process and temperature. These variations should be tolerable, since they are relatively small compared to the pulse frequency bandwidth of more than 2.7 GHz or 11%. The integrated power lost into adjacent channels, over a 2.7 GHz bandwidth would be relatively small and the receiver would

still be able to detect the pulse to a certain extent. Furthermore, the oscillator frequency tuning range of 600 MHz and the available locking bandwidth of more than 500 MHz are sufficient to account for the PVT variations.

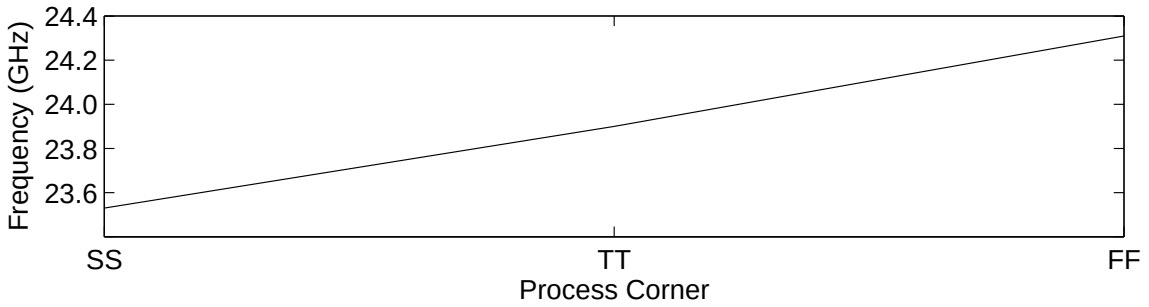
4.3.2 Quadrature Pulse Generator

The complete quadrature pulse generator was also fabricated in 0.13 μm CMOS and a photograph of the IC is shown in Fig. 4.17. It occupies a die area of 0.94 mm^2 including bonding pads, decoupling capacitors and the chip guard ring (plus chamfer regions), while the core circuit area is 0.41 mm^2. The circuit consumes less than 2.2 mW of average power (P_{AVG}) at a PRF of 50 MHz. The power consumption increases with the PRF, reaching 14.8 mW at the maximum PRF of 600 MHz. This gives an energy consumption E_p of less than 11.0 pJ and 6.2 pJ at 50 MHz and 600 MHz PRF respectively for each of the four differential quadrature pulses. The energy consumption E_p is given by:

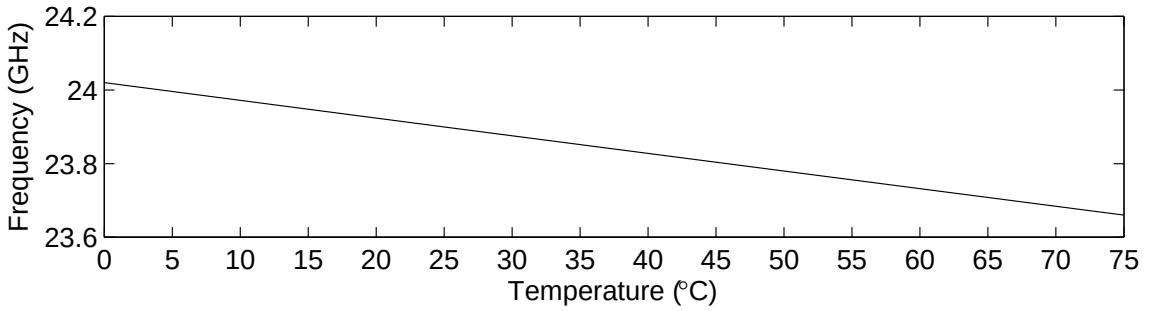
$$E_p = \frac{P_{AVG} \times PRI}{4} = \frac{P_{AVG}}{PRF \times 4} \tag{4.6}$$

where PRI is the pulse repetition time.

The UWB pulse generator IC was also measured directly on-wafer and a 60 GHz Tektronix Digital Serial Analyzer (DSA) was used to observe the pulses in the time domain. The input clock is a periodic sinusoidal signal which is readily converted on-chip into a digital square wave using the edge sharpening inverters (Fig. 4.1). Fig. 4.18 shows a comparison between a simulated output signal and the DSA's measurement result. Both simulation and measurements have the same bias conditions, and there is good agreement between the simulated and measured waveforms. The measured



(a)



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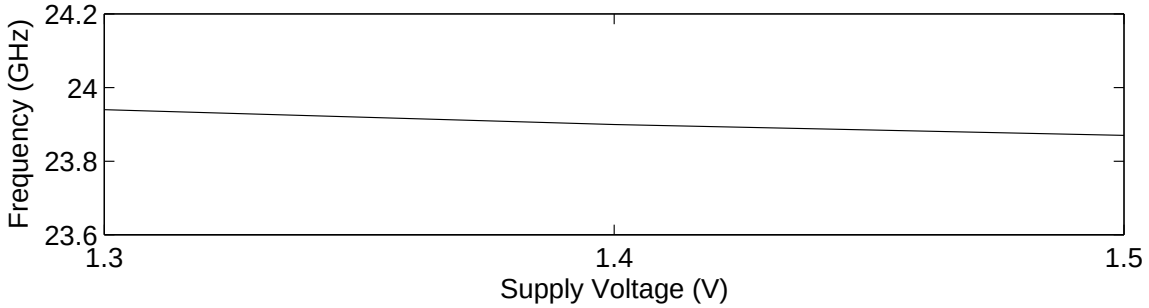


(c)

Figure 4.16: Variations of the pulse center frequency with: (a) process, (b) temperature and (c) supply voltage.

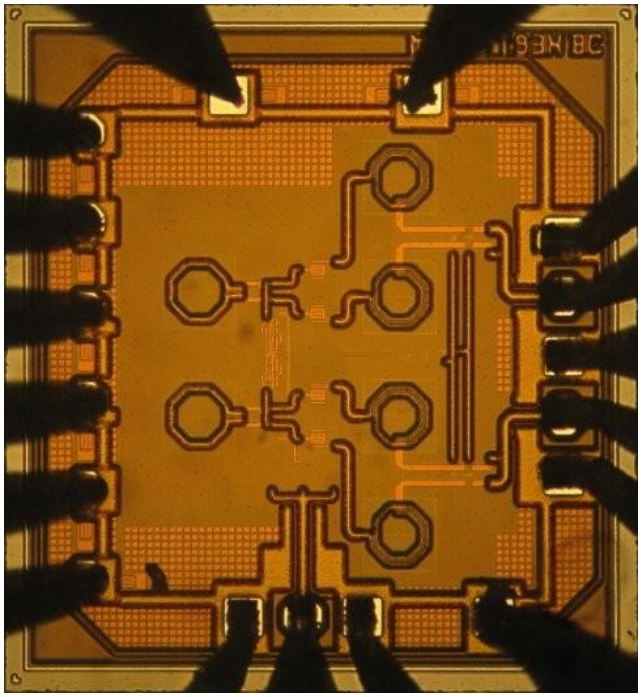
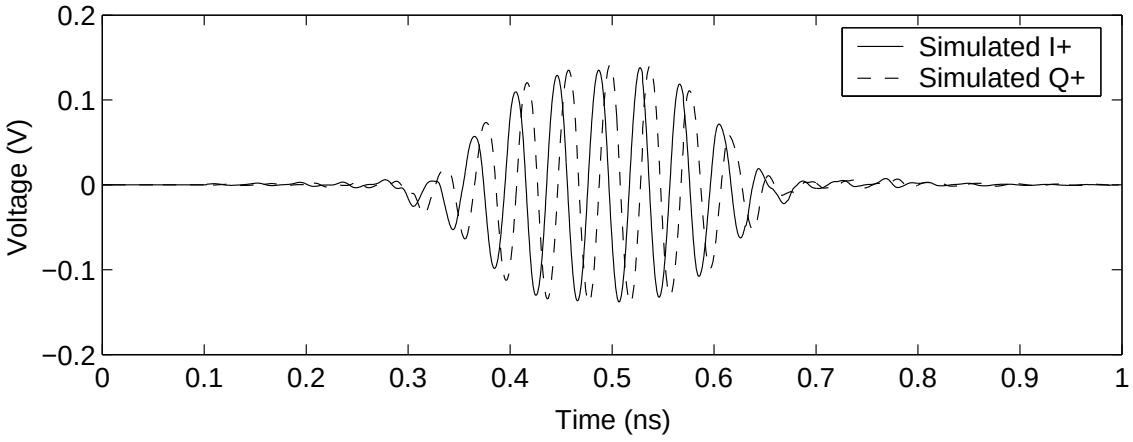
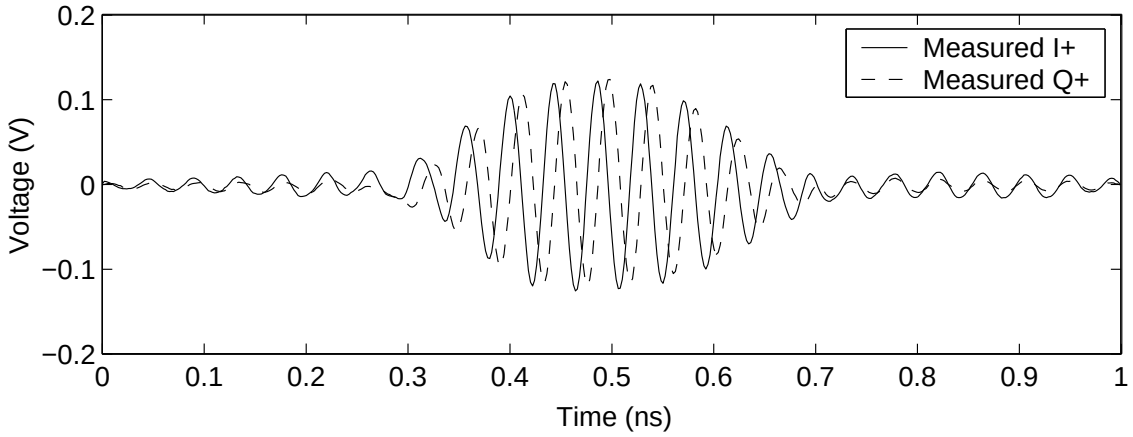


Figure 4.17: Photograph of quadrature UWB Pulse Generator IC.

pulses have a peak-to-peak voltage amplitude of 240 mV and a peak power level of –5.4 dBm, with good symmetry about the 0 V (ground) level $(V_{pk+}+V_{pk-})/(V_{pk+}-V_{pk-}) \approx$ 2 %. The ringing level is also about –24.0 dB, which is somewhat higher than simulated, due to unmodelled substrate coupling and inductive parasitics. The pulse time duration can be tuned over a wide range using the control voltages V_{WIDTH} and V_{SLOPE} in the glitch generator and Fig. 4.19 shows the measured pulses with time durations of 375 ps, 525 ps and 650 ps. Moreover, the phase difference between the $I+$ and $Q+$ outputs is about 90±3.0°. It should be noted that the DSA is an equivalent time sampling oscilloscope and not a real-time oscillocope, sampling the signal only once per trigger event. The DSA is thus triggered using the input clock for this measurement. Since 24 GHz cycles with a time period of around 40 ps are clearly visible, the generated oscillations are indeed coherent with the input clock,



(a)

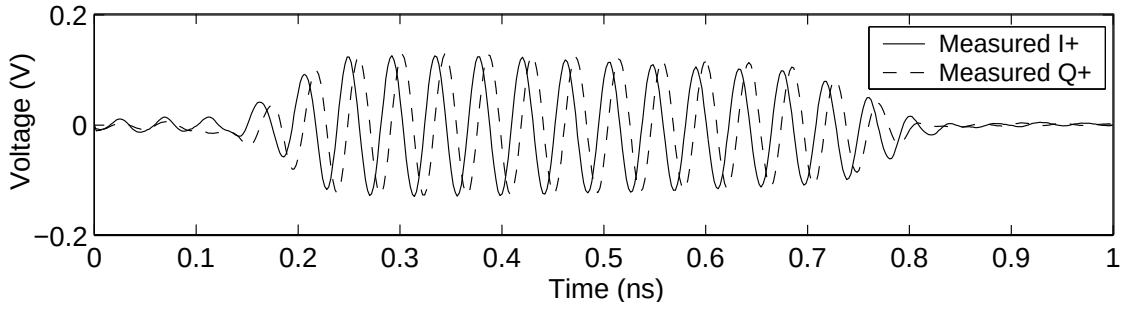


(b)

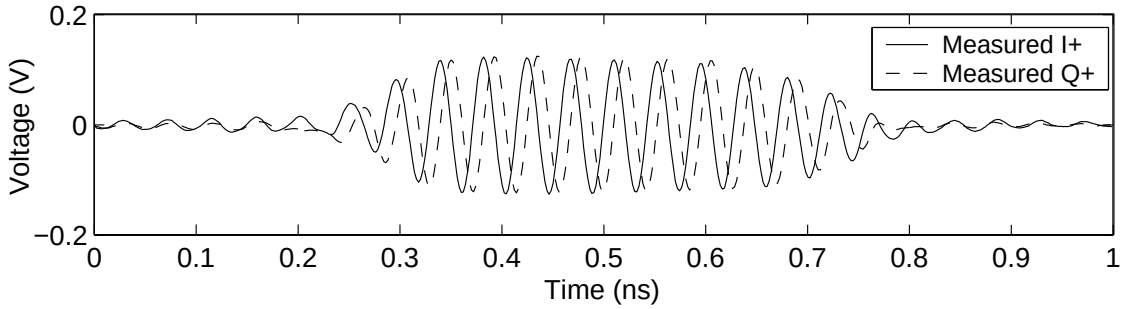
Figure 4.18: Output UWB waveforms: (a) simulated and (b) measured.

and thus pulse-to-pulse coherency is maintained.

The normalized power spectral density (PSD) of the measured signals shown in Fig. 4.19a and Fig. 4.19c was calculated and is illustrated in Fig. 4.20. It is apparent that the measured –10 dB bandwidth varies from about 2.7 GHz to 4.9 GHz and is centered at 23.9 GHz which corresponds to the LO signal frequency. The spectra are also free from spikes or spectral lines that occur due to LO leakage in typical pulse generators. Furthermore the spectrum roll-off can be quite sharp with more than



(a)



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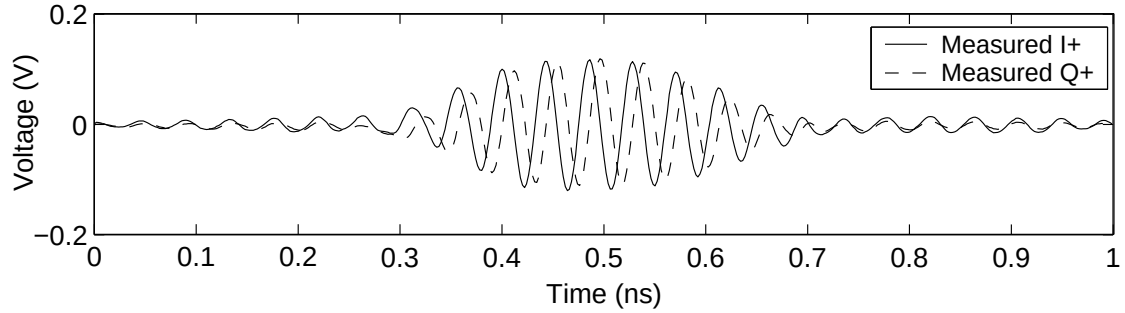


(c)

Figure 4.19: Measured UWB waveforms with different time durations: (a) long (650ps), (b) moderate (525ps) and (c) short (375ps).

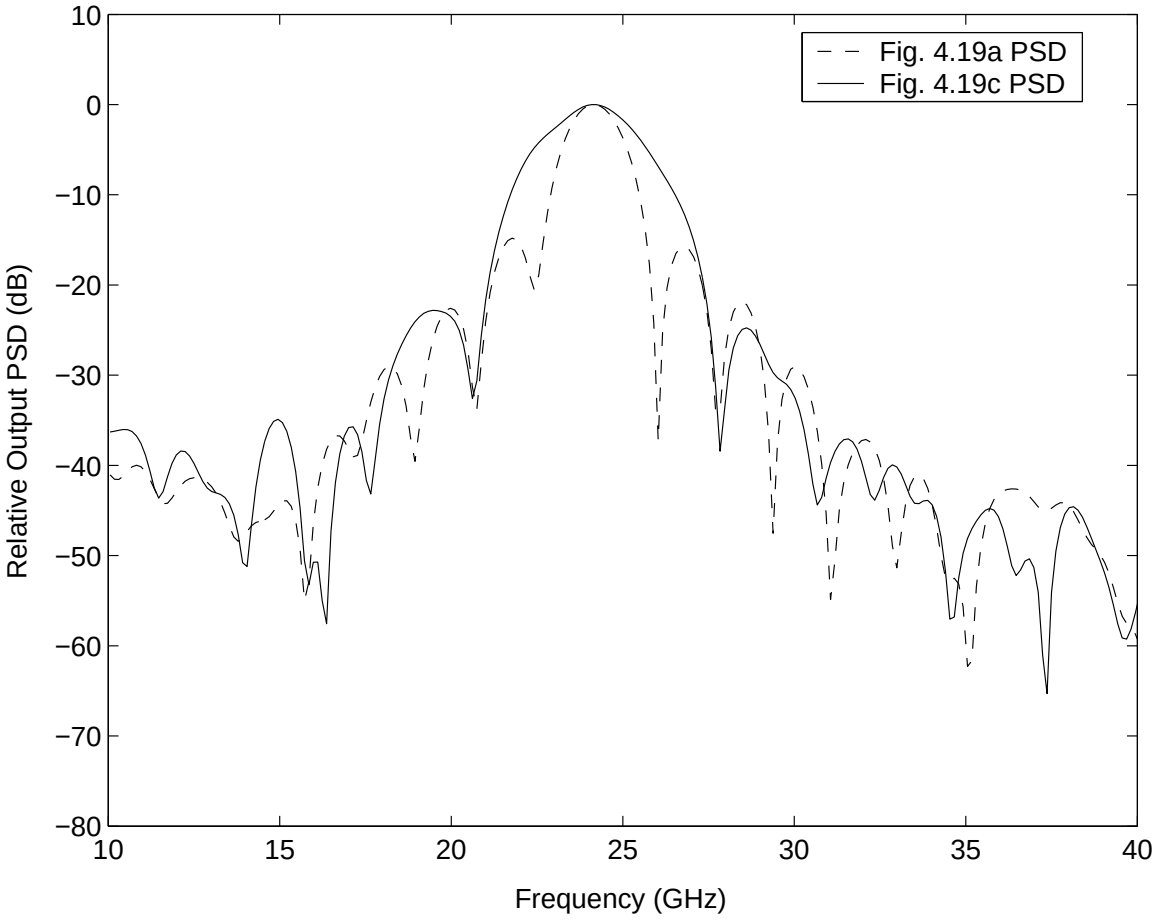


Figure 4.20: Calculated normalized PSD of the measured output UWB signals.

23 dB of out-of-band rejection relative to the peak power level for the pulse in Fig. 4.19c, which is useful in satisfying the FCC spectrum limits.

Table 4.1 summarizes the circuit's characteristics in comparison with other work [29, 36, 64, 93]. The proposed pulse generator offers quadrature tunable outputs with comparable or better phase noise (PN) at a low energy consumption of 6.2 pJ/pulse. It is also more energy efficient than most of the other designs if the energy consumption is normalized with respect to the output peak-to-peak voltage. Furthermore, the proposed circuit has a relatively small area compared to the other work.

Table 4.1: Summary of pulse generator characteristics.

Characteristic	**This work**	[36]	[29]	[64]	[93]
Process	**0.13 μm**	0.13 μm	0.18 μm	90 nm	GaAs
	CMOS	SiGe	CMOS	CMOS	HBT
Chip Area (mm^2)	**0.41**	–	–	0.0014 [1]	1.17
Power (mW)	**14.8**	14.5 [2]	42	1.4	55
PRF (MHz)	**600**	10	–	500	62.5
Energy	**6.2 pJ/pulse**	–	–	2.8 pJ/pulse	–
Amplitude	**240 mV**	630 mV	80 mV [3]	71 mV	1.4 V
Duration	$\geq$ **375 ps**	1.1 ns	250 ps	552 ps	1.0 ns
Frequency (GHz)	**23.9**	24.125	26.5	25.5	24.31
PN (dBc/Hz)	**-70 at 1 kHz**	-56 at 1 kHz	-57 at 10 kHz	–	-102.5 at 100 kHz
	-100 at 1 MHz	-104.3 at 1 MHz	-107 at 1 MHz		-120.83 at 1 MHz

[1] External bias-tee (choke inductor) used for edge and pulse combining.
[2] Power consumption of the VCO only.
[3] Peak-to-peak voltage of the receiver pulse output.

4.4 Summary

A new quadrature tunable pulse generator has been demonstrated in 0.13 μm CMOS for 22–29 GHz UWB applications. A quadrature LC oscillator is quickly switched on and off for the pulse duration, and the amplitude envelope is shaped using a variable passive attenuator. By switching on one side of each differential oscillator just before the other, a current impulse is injected with a short time duration and large harmonic components out to 24 GHz, creating a large initial condition for fast startup and setting the initial phase of the oscillations for high pulse-to-pulse coherence. The measured output phase noise thus matches that of the clock signal, yielding a relatively low phase noise of -70 dBc/Hz at 1 kHz offset, and -100 dBc/Hz at 1 MHz offset. This amounts to a low integrated rms jitter from 100 Hz to 1 MHz of less than 720 fs. The attenuator is controlled with an impulse which is created by a digital,

tunable glitch generator (CMOS NAND gate). Several UWB pulses were measured and demonstrated, with the pulse time duration and –10 dB bandwidth varying over a range of 375–650 ps and 2.7–4.9 GHz respectively. The entire circuit operates in switched-mode with a low average power consumption of less than 2.2 mW and 14.8 mW at 50 MHz and 600 MHz PRFs, or below 11 pJ for each of the four differential quadrature pulses. It occupies a total area of 0.94 mm^2 including bonding pads and decoupling capacitors, and the active circuit area is only 0.41 mm^2.

Chapter 5

Quadrature Pulsed Oscillator with Quadrature Phase Modulation

5.1 Introduction

This chapter demonstrates a new quadrature pulsed oscillator in 0.13 μm CMOS for 3.1–10.6 GHz Ultra-Wideband (UWB) applications that can produce pulsed oscillations with either binary and quadrature phase modulation. It can be used in a quadrature pulse generator, providing UWB pulses for quadrature pulse correlation and supporting binary and quadrature phase modulation [43]. The circuit employs a two-stage ring oscillator with shunt-shunt resistive feedback for a wide tuning range and a high oscillation frequency ($>$ 10 GHz). A novel switching technique is proposed that enables fast oscillator startup within 1 ns while having a negligible effect on the oscillation frequency. It also locks the phase of the oscillations to the input clock for high pulse-to-pulse coherence, achieving a low integrated RMS jitter (from 100 Hz to 100 MHz) of less than 3.8 ps. Furthermore, both binary and quadrature

phase modulation are directly implemented using the proposed switching technique, eliminating the need for a high-power wideband modulator or a large balun. To the author's best knowledge, this is the first short-time quadrature pulsed oscillator with built-in quadrature phase modulation over the full UWB bandwidth. The oscillator is completely switched off between pulses for a low power consumption of less than 13 mW at 3 GHz and 18 mW at 10 GHz with a 250 MHz clock frequency, or less than 13–18 pJ of energy consumption per pulse. The integrated circuit (IC) occupies a total die area of 0.85 mm^2 including bonding pads and decoupling capacitors, while the active circuit area is only 0.05 mm^2.

5.2 Circuit Architecture and Design

A circuit diagram of the 3-10 GHz quadrature pulsed oscillator is shown in Fig. 5.1. It consists of a startup network, a two-stage ring oscillator with two cross-coupled inverter pairs, and two output buffers. The startup network first realizes four clock signals CLK_{I+}, CLK_{I-}, CLK_{Q+} and CLK_{Q-} according to the binary values of V_{PI} and V_{PQ}. The input clock signal CLK is used to turn the ring oscillator and output buffers on and off, while the signals CLK_{I+}, CLK_{I-}, CLK_{Q+} and CLK_{Q-} are used to trigger the cross-coupled pairs. Differential quadrature 3-10 GHz pulsed oscillations are generated at $I+$, $I-$, $Q+$ and $Q-$ which are quadrature phase modulated according to V_{PI} and V_{PQ}.

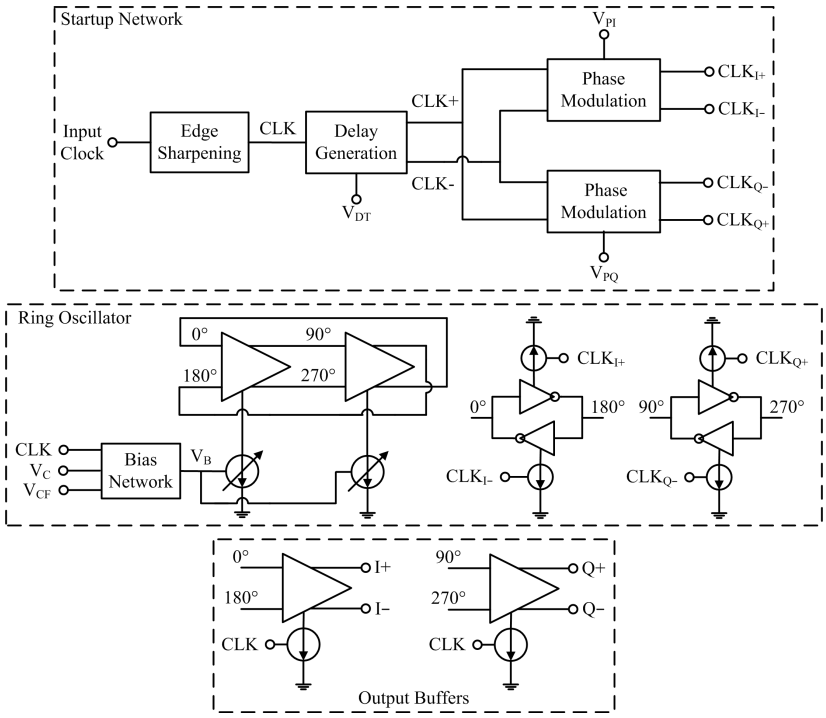


Figure 5.1: Circuit diagram of quadrature pulsed oscillator.

5.2.1 Pulsed Quadrature Ring Oscillator

A ring oscillator can provide the wide frequency tuning range (3–10 GHz) and short startup time (< 1 ns) required in UWB applications due to its low quality factor (Q) compared to an inductor-capacitor (LC) resonator-based oscillator. Such a wide frequency tuning range of 7 GHz is difficult to achieve using an LC oscillator. A ring oscillator also has a smaller footprint compared to its LC counterpart, which is desired for a low cost. The higher phase noise (PN) of the ring oscillator is circumvented by the short time duration (< 2 ns) and wide bandwidth (> 1 GHz) of the pulsed oscillations. However the maximum oscillation frequency of a ring oscillator is limited and it consumes more power than its LC counterpart.

The ring oscillator circuit designed in this work is shown in Fig. 5.2. It consists

of two differential delay stages which are cascaded in a ring or loop as shown in Fig. 5.2. The CMOS inverter-based topology (M_{IP1}-M_{IN1}, M_{IP2}-M_{IN2}) of the delay stage provides a fairly constant output voltage swing over large variations in the bias current for a frequency tuning range of more than three to one. Shunt-shunt feedback (R_F) further reduces the variation of the output voltage swing with the bias current thus increasing the tuning range. It also increases the oscillation frequency for a given DC current and power consumption [13, 94].

A linearized model of the two-stage ring oscillator is constructed as shown in Fig. 5.3 to analyze the effect of shunt-shunt resistive feedback and to illustrate the quadrature phase modulation property of the oscillator. Each delay stage is modeled using its two-port Y-parameters (Y_{11}, Y_{12}, Y_{21}, Y_{22}), while each cross-coupled pair is represented by a negative admittance Y_c. The current sources $I_1(t)$ and $I_2(t)$ are the injected current stimuli to startup the ring oscillator. The Y-parameters of each delay stage and the negative admittance Y_C of each cross-coupled pair can be written as:

$$Y_{11} = 1/R_F + 1/R_{IN} + j\omega C_{IN}, \tag{5.1a}$$

$$Y_{12} = -1/R_F - j\omega C_F, \tag{5.1b}$$

$$Y_{21} = G_m - 1/R_F - j\omega C_{G_m} - j\omega C_F, \tag{5.1c}$$

$$Y_{22} = 1/R_F + 1/R_{OUT} + j\omega C_{OUT} \tag{5.1d}$$

$$Y_C = -G_{mC} + j\omega C_C \tag{5.1e}$$

where R_F is the feedback resistance, R_{IN} and C_{IN} are the equivalent input resistance and capacitance, and R_{OUT} and C_{OUT} are the equivalent output resistance and capacitance of the delay stage. G_m and G_{mC} denote the DC transconductance of the delay

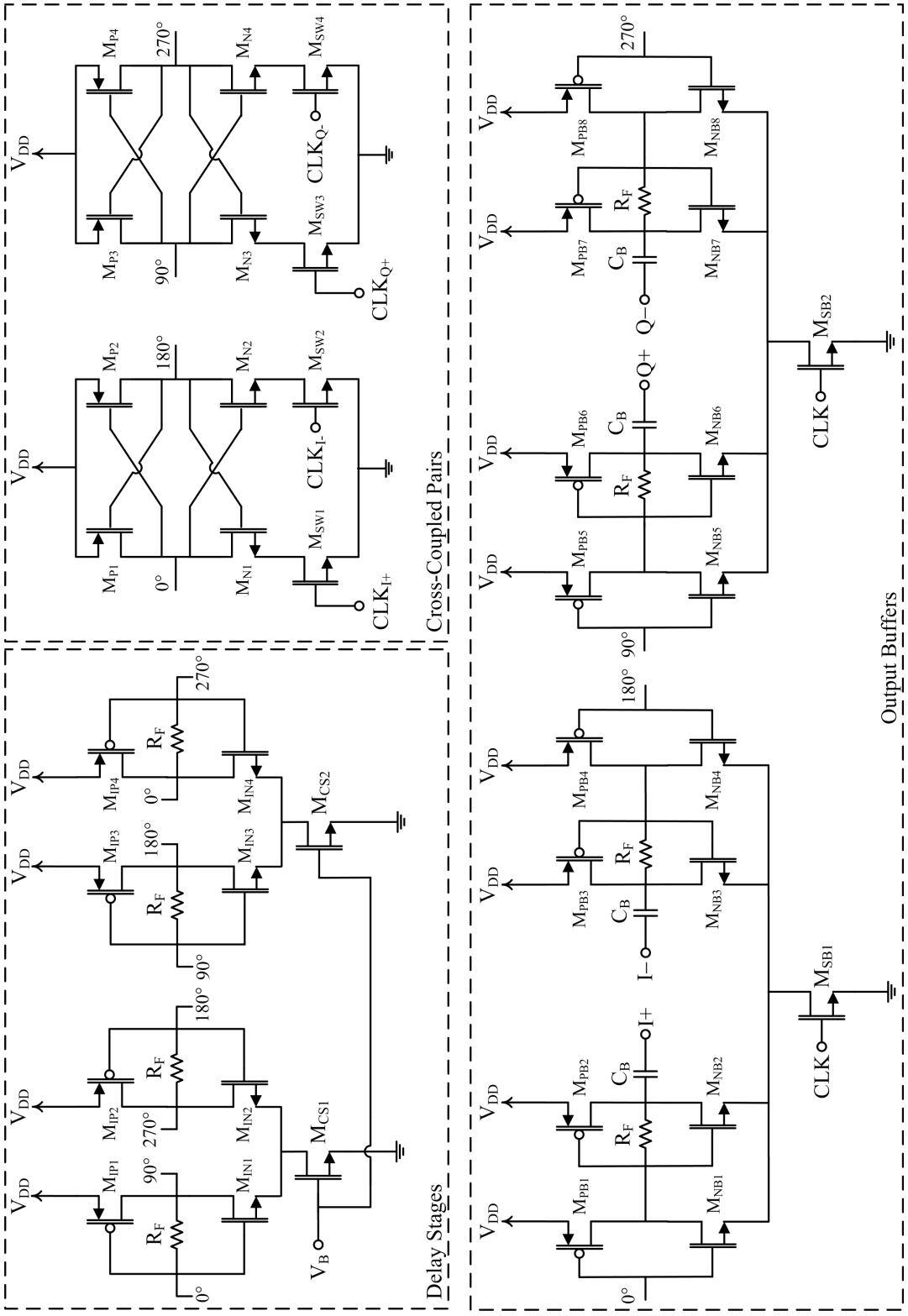


Figure 5.2: Circuit schematic of the quadrature pulsed oscillator.

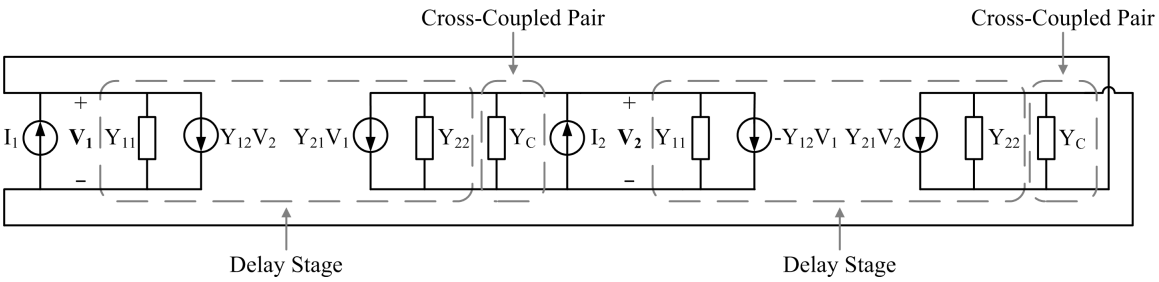


Figure 5.3: Linearized Y-parameter model of the two-stage ring oscillator with injected current impulses.

stage and the cross-coupled pair respectively, and C_C is the parasitic capacitance of the cross-coupled pair. The capacitance C_F is a feedback capacitance consisting of the gate-drain parasitic capacitance of the transistors C_{GD}, while the capacitance C_{G_m} captures the frequency dependence of the transconductance due to resistive parasitics at the gate and source for example.

The complete oscillator model in Fig. 5.3 is analyzed and the loop gain $H(j\omega)$ can be calculated as:

$$\begin{aligned} H(j\omega) &= -\left(\frac{Y_{21}-Y_{12}}{Y_{11}+Y_{22}-Y_c}\right)^2 \\ &= -\left(\frac{G_m - j\omega C_{G_m}}{G_L + j\omega C_L}\right)^2 \end{aligned} \tag{5.2}$$

where $G_L = 2/R_F + 1/R_{IN} + 1/R_{OUT} - g_{mC}$ and $C_L = C_{IN} + C_{OUT} + C_C$ are the effective loading conductance and capacitance respectively at each node. The loop gain $H(j\omega)$ in (5.2) must be equal to 1 for steady oscillation (Barkhausen's criterion).

This gives the following oscillation frequency ω_0 and transconductance G_m:

$$\omega_0 = \frac{G_L}{C_{G_m}} \tag{5.3a}$$

$$G_m = \frac{G_L C_L}{C_{G_m}} \tag{5.3b}$$

Equation (5.3a) verifies that the oscillation frequency ω_0 increases with the loading conductance G_L and thus with smaller values of feedback resistance R_F. This is accompanied with an increase in the transconductance G_m, which occurs due to the drop in the output voltage swing about the trip point of the delay stages.

The oscillator's steady-state impulse response ($V_1(t)$ and $V_2(t)$) with $I_1(t) = A\delta(t)$ and $I_2(t) = B\delta(t)$ where $A = \pm 1$ and $B = \pm 1$ can thus be evaluated as:

$$V_1(t) = A_0 \cos(\omega_0 t + \phi) \tag{5.4a}$$

$$V_2(t) = A_0 \sin(\omega_0 t + \phi) \tag{5.4b}$$

where the phase ϕ is given by:

$$\phi = \tan^{-1}\left(\frac{BC_L + AC_{G_m}}{AC_L - BC_{G_m}}\right) \tag{5.5}$$

and A_0 is a constant. Equation (5.5) indicates that the carrier phase depends on the signs of A and B, i.e. the direction of the injected current impulses $I_1(t)$ and $I_2(t)$. The four possible combinations of $A = \pm 1$ and $B = \pm 1$ actually yield four quadrature phases (ϕ_1, ϕ_2, ϕ_3 and ϕ_4) given by:

$$\phi_1 = \tan^{-1}\left(\frac{C_L + C_{G_m}}{C_L - C_{G_m}}\right) \tag{5.6a}$$

$$\phi_2 = \tan^{-1}\left(\frac{C_{G_m} - C_L}{C_L + C_{G_m}}\right) = \phi_{00} - 90^\circ \tag{5.6b}$$

$$\phi_3 = \tan^{-1}\left(\frac{-C_L - C_{G_m}}{C_{G_m} - C_L}\right) = \phi_{00} - 180^\circ \tag{5.6c}$$

$$\phi_4 = \tan^{-1}\left(\frac{C_L - C_{G_m}}{-C_L - C_{G_m}}\right) = \phi_{00} - 270^\circ \tag{5.6d}$$

Quadrature phase modulation can thus be achieved by manipulating the direction of the current impulses I_1 and I_2 injected into nodes V_1 and V_2.

5.2.2 Oscillator Startup

A circuit schematic of the startup network is shown in Fig. 5.4. CMOS inverters sharpen the edges of the input clock signal and realize two complementary clocks CLK and $\overline{CLK}$, which turn the biasing current of the ring oscillator delay stages and output buffers on and off. Current-starved inverters are then used to split the signal CLK into two signals $CLK+$ and $CLK-$, introducing a very short time delay between them on the order of tens of picoseconds. This delay can be tuned using the control voltage V_{DT}. Four transmission-gate multiplexers T_1–T_2, T_3–T_4, T_5–T_6 and T_7–T_8 are then employed to route $CLK+$ and $CLK-$ to CLK_{I+}, CLK_{I-}, CLK_{Q+} and CLK_{Q-}, which trigger the cross-coupled pairs. If V_{PI} (V_{PQ}) is high, the multiplexers are set such that $CLK+$ and $CLK-$ are passed to CLK_{I+} (CLK_{Q+}) and CLK_{I-} (CLK_{Q-}) respectively. If V_{PI} (V_{PQ}) is low, the opposite occurs and $CLK+$ and $CLK-$ are passed to CLK_{I-} (CLK_{Q-}) and CLK_{I+} (CLK_{Q+}) respectively.

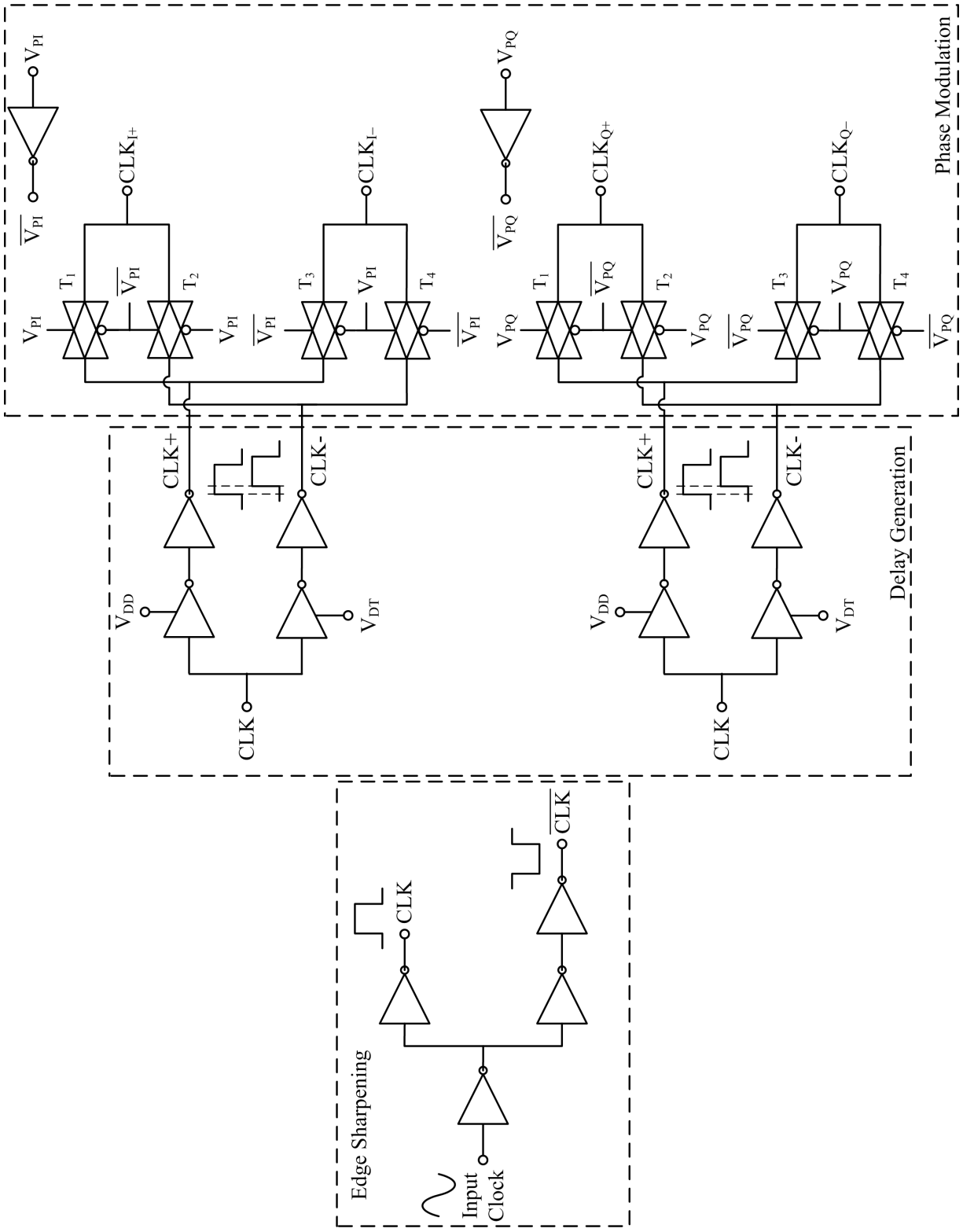


Figure 5.4: Circuit schematic of the startup network.

The bias currents of each cross-coupled pair is switched on and off using a pair of NMOS switches $M_{SW1} - M_{SW2}$ ($M_{SW3} - M_{SW4}$) as shown in Fig. 5.2. By switching on one side of each cross-coupled pair just before the other (e.g. switching on M_{SW1} before M_{SW2}, M_{SW3} before M_{SW4}), an initial current I_{INJI} (I_{INJQ}) flows for a short time through the oscillator nodes as shown in Fig. 5.5. In effect, a current impulse is injected at the oscillator nodes, which quickly starts up the oscillations. It also sets the initial phase of the oscillations at the turn-on instant. By setting the same initial oscillation phase at each clock rising edge, the LO pulses are phase coherent with the input clock and pulse-to-pulse coherency is maintained.

The order in which switches M_{SW1} and M_{SW2} (M_{SW3} and M_{SW4}) are triggered determines the direction of the injected current impulse I_{INJI} (I_{INJQ}) as illustrated in Fig. 5.5. If V_{PI} (V_{PQ}) is high, switch M_{SW1} (M_{SW3}) is activated before M_{SW2} (M_{SW4}) and the injected current I_{INJI} (I_{INJQ}) flows in the direction shown in Fig. 5.5(a). If V_{PI} (V_{PQ}) is low, switch M_{SW2} (M_{SW4}) is activated before M_{SW1} (M_{SW3}), reversing the direction of the injected current I_{INJI} (I_{INJQ}) (Fig. 5.5 (b)). Therefore, the values of V_{PI} and V_{PQ} determine the directions of the injected current impulses I_{INJI} and I_{INJQ} respectively, and the oscillation phase takes on one of four quadrature values thus implementing quadrature phase modulation.

The bias current of the delay stages is controlled using a pair of NMOS transistors M_{CS1}-M_{CS2} as shown in Fig. 5.2. The gate bias voltage V_B of these transistors is created using the biasing circuit shown in Fig. 5.6. The coarse frequency tuning voltage V_C and the fine frequency tuning voltage V_{CF} specify the current I_B that flows through the current mirror M_{P1}-M_{P2}, which sets the bias voltages V_{BI} and V_B. The charging time associated with voltages V_{BI} and V_B determines the settling time

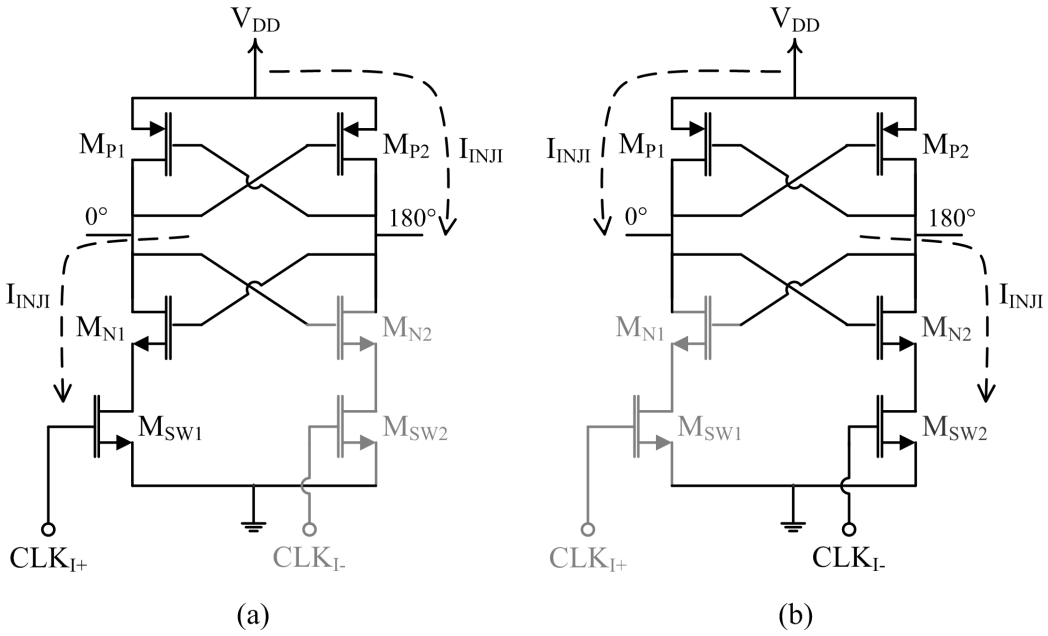


Figure 5.5: Injected current I_{INJI} with: (a) V_{PI} high and (b) V_{PI} low.

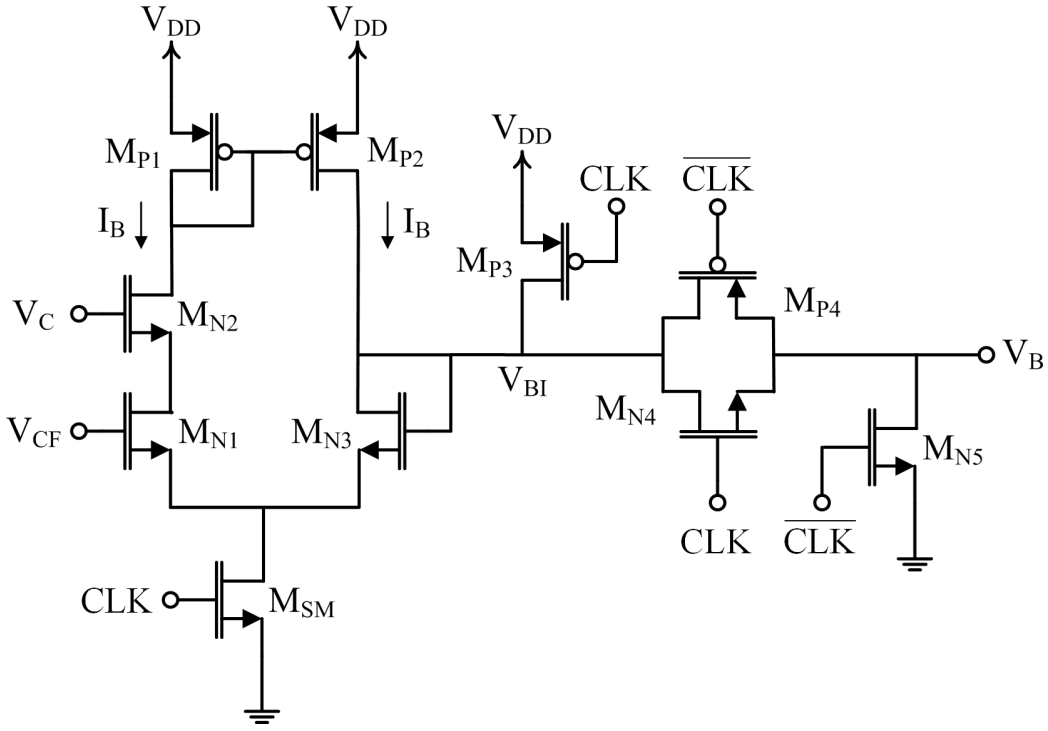


Figure 5.6: Circuit schematic of the bias network used for the delay stages.

of the ring oscillator. For lower values of V_C, the current I_B is reduced and the time required to charge up V_{BI} and V_B is increased. To mitigate this effect, a transistor (M_{P3}) is added to precharge node V_{BI} to the supply voltage V_{DD} before turning on the ring oscillator. This increases the current I_B at the turn on instant, allowing voltages V_{BI} and V_B to settle more quickly for a shorter startup time.

5.2.3 Output Buffers

Differential buffers with on-chip decoupling capacitors are implemented to isolate the oscillator nodes from the 50 Ω output loads (Fig. 5.2). A CMOS inverter-based Cherry-Hooper topology ($M_{PB1} - M_{NB1}$, $M_{PB2} - M_{NB2}$) is employed as a broadband output buffer. The feedback resistor R_F significantly reduces the resistance seen at the input and output of the second inverter ($M_{PB2} - M_{NB2}$). This increases the pole frequencies associated with these nodes, increasing the bandwidth and reducing the settling time of the output voltage. It also decreases the Miller capacitance of the first inverter ($M_{PB1} - M_{NB1}$) and thus the effective input capacitance of the buffer for a higher oscillation frequency.

5.3 Experimental Results

The pulsed quadrature oscillator was fabricated in 0.13 μm CMOS and a photograph of the IC is shown in Fig. 5.7. It occupies a die area of 0.85 mm^2 including bonding pads, decoupling capacitors and the chip guard ring (plus chamfer regions), while the core circuit area is only 0.050 mm^2. The DC or peak power consumption is proportional to the oscillation frequency and is about 23 mW at 3 GHz and 32 mW

at 10 GHz. This includes the power consumption of the output buffers, which is estimated to be approximately 13.5 mW. The average power consumption with a 250 MHz clock frequency is about 13 mW at 3 GHz and 18 mW at 10 GHz. This gives an energy consumption E_p of less than 13.0 pJ and 18 pJ at 3 GHz and 10 GHz respectively for each of the four differential quadrature pulses. The energy consumption E_p is given by:

$$E_p = \frac{P_{AVG} \times PRT}{4} = \frac{P_{AVG}}{PRF \times 4} \tag{5.7}$$

where PRT is the pulse repetition time and PRF is pulse repetition frequency. All biasing circuits were implemented using low power devices to minimize the off-state leakage power to less than 60 nW (estimated), which is significantly lower than the peak power consumption.

The pulsed oscillator IC was measured directly on-wafer using 40GHz coplanar waveguide (CPW) probes and DC probes. The Agilent 50 GHz spectrum analyzer (E4448A) was used to examine the output power spectrum and phase noise (PN), while a 20 GHz Agilent digital oscilloscope was used to observe the pulsed oscillations in the time domain. The input clock is a periodic sinusoidal signal which is readily converted on-chip into a digital square wave using the edge sharpening inverters (Fig. 5.4).

Fig. 5.8 shows the measured output power spectra when the quadrature oscillator is in free running mode, i.e. the input clock is held at logic high (V_{DD} = 1.5V). The tuning voltage V_C is varied from 0.58 V to 0.93 V in steps of 0.05 V to change the oscillation center frequency from 3.15 GHz to 10.07 GHz, while the fine tuning voltage V_{CF} is held constant at the supply voltage V_{DD} = 1.5V. The free-running

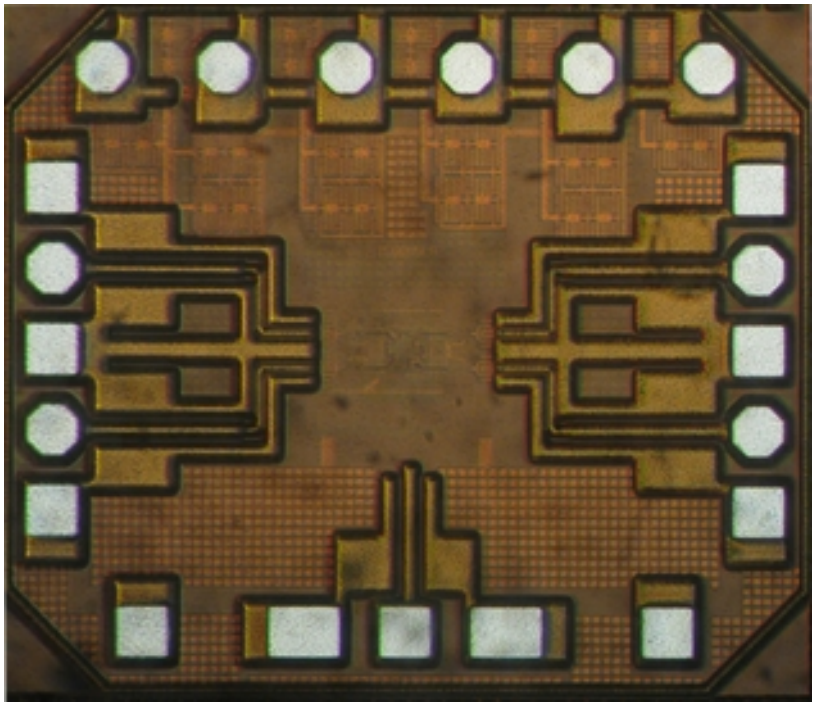


Figure 5.7: Photograph of quadrature UWB pulsed oscillator IC.

output power level is about –6.2 dBm at 3.15 GHz, –8.3 dBm at 6.1 GHz and –10.5 dBm at 10.07 GHz. Fig. 5.9 is a plot of the measured oscillation frequency and output power level against the control voltage V_C. The results indicate that a tuning range of about 7 GHz has been achieved, over which the output power varies by less than ±2 dB. The variation of the oscillation frequency with the fine tuning voltage V_{CF} was also measured at 3.75 GHz, 7.4 GHz and 10.07 GHz i.e. $V_C = 0.63$ V, $V_C = 0.78$ V and $V_C = 0.93$ V, and the results are shown in Fig 5.10. It is apparent that the oscillation frequency can be tuned within 20 MHz for each 0.1 V step in V_{CF} for V_{CF} values between 1.0 V and 1.5 V. The oscillation frequency step remains below 85 MHz for V_{CF} values as low as 0.7 V.

The pulsed output power spectra were measured at an oscillation center frequency of 3.75 GHz, 6.75 GHz and 10.25 GHz, i.e. with the tuning voltage V_C set to 0.58 V,

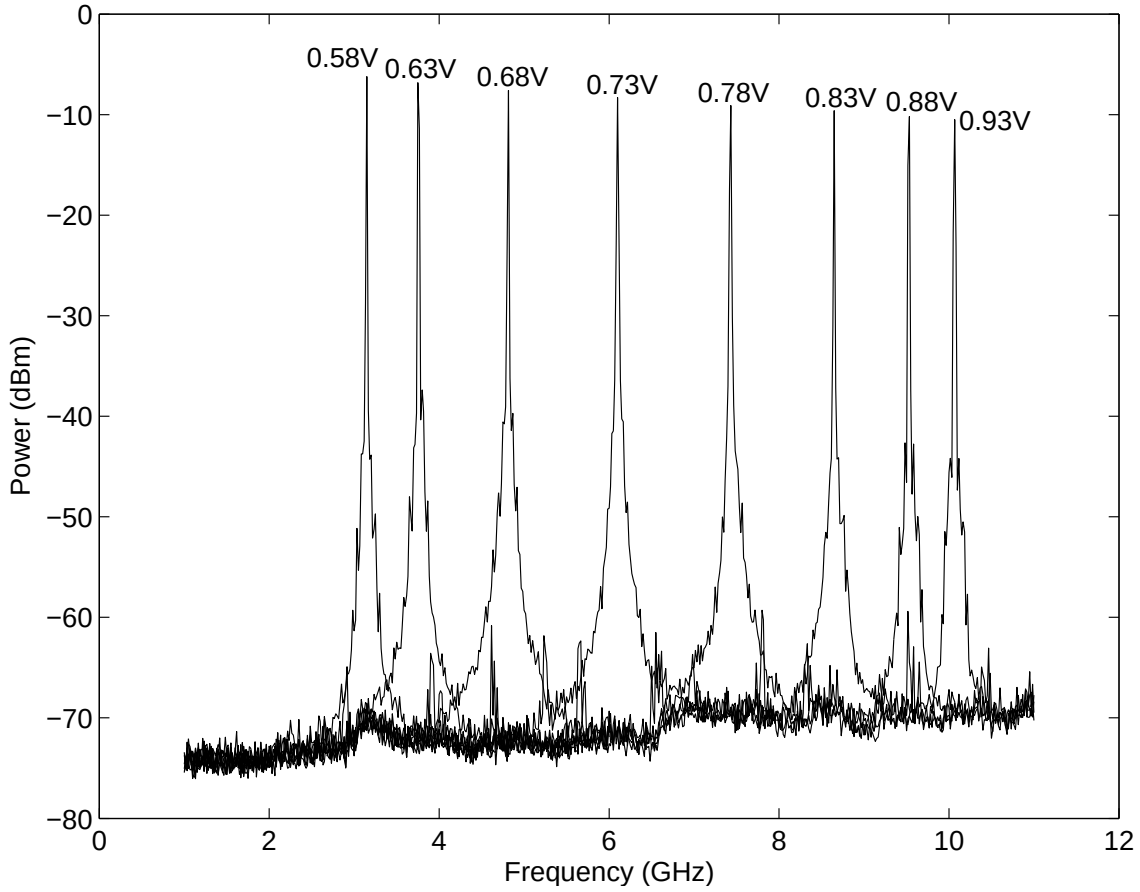


Figure 5.8: Measured free running spectra for different values of tuning voltage V_C.

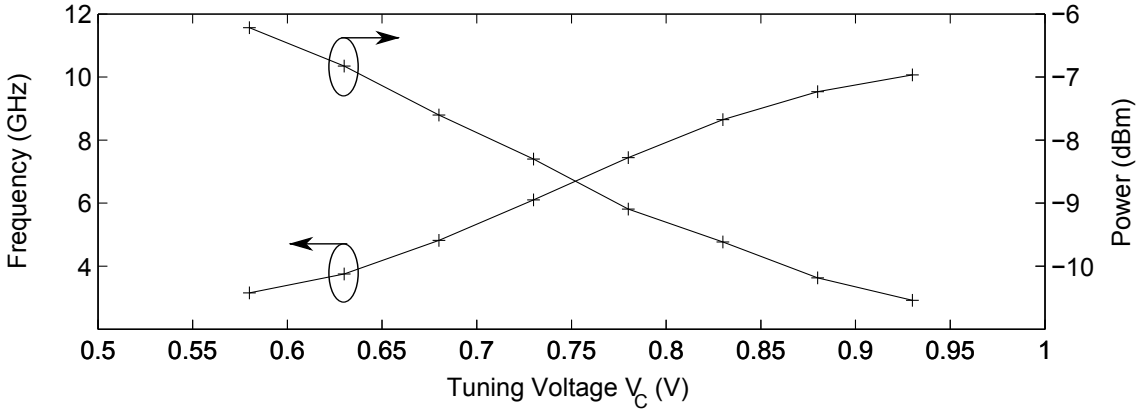
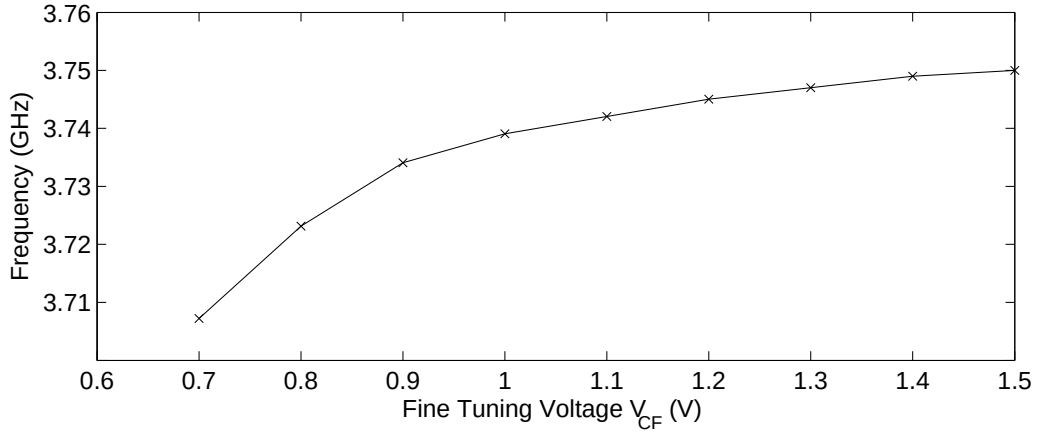
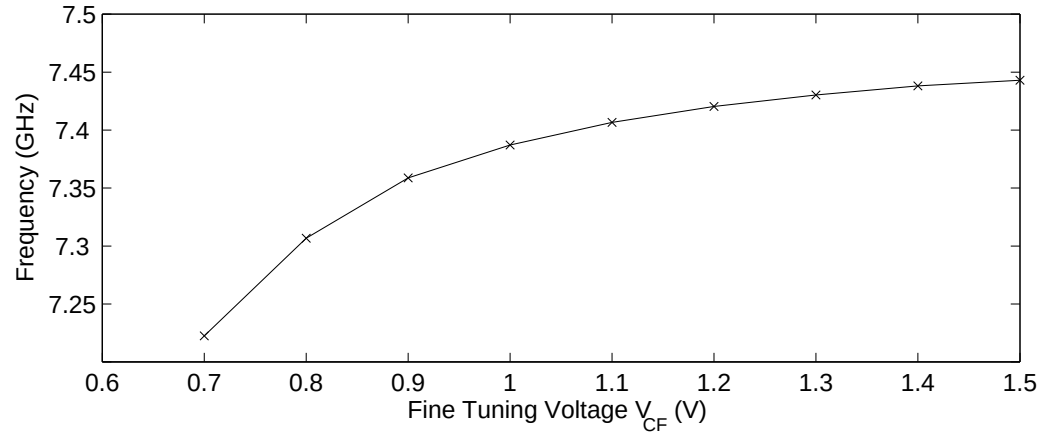


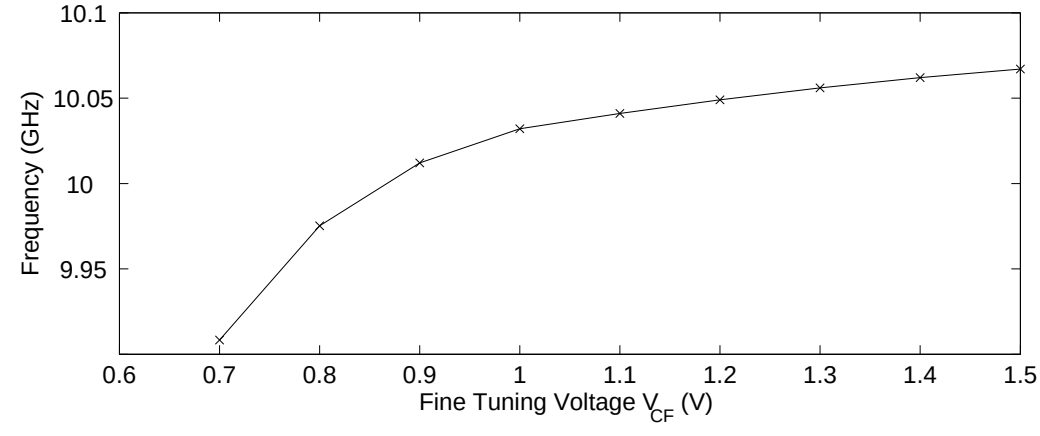
Figure 5.9: Measured free running frequency and output power with different values of V_C.



(a)



(b)



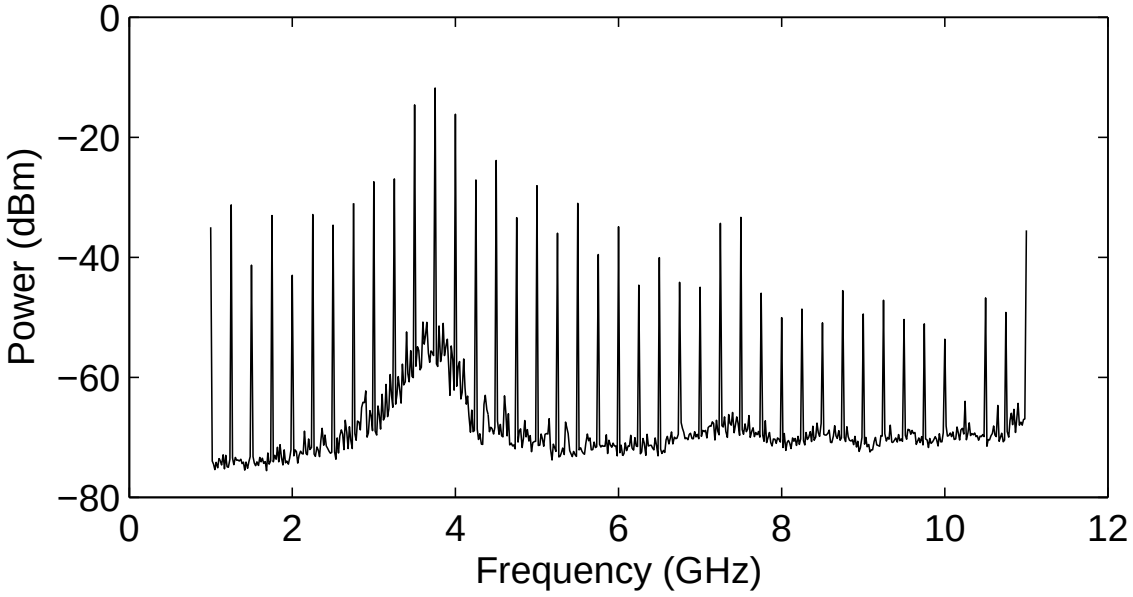
(c)

Figure 5.10: Variation of the oscillation frequency with the fine tuning voltage V_{CF} at 3.75 GHz ($V_C = 0.63$ V), 7.44 GHz ($V_C = 0.78$ V) and 10.07 GHz ($V_C = 0.93$ V).

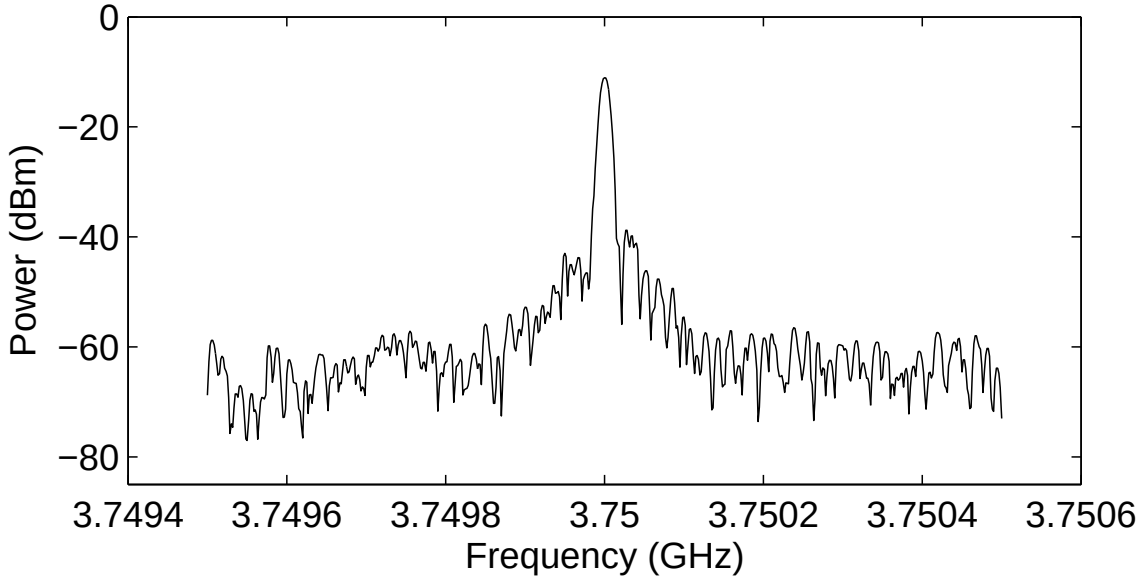
0.75 V and 0.94 V and are plotted in Fig. 5.11, Fig. 5.12 and Fig. 5.13 respectively. The clock frequency was set to 250 MHz for these measurements. The power spectrum exhibits peaks at multiples of the clock frequency since the output is a periodic (unmodulated) extension of the pulses. It is also apparent that the generated harmonic components are coherent and well-defined. Fig. 5.11, Fig. 5.12 and Fig. 5.13 also show the generated peaks at 3.75 GHz, 6.75 GHz and 10.25 GHz respectively in more detail over a span of only 1 MHz, clearly showing stable and locked operation.

Fig. 5.14 shows the measured phase noise of the generated pulsed output at 3.75 GHz, 6.75 GHz and 10.25 GHz. The measured phase noise of the clock reference is also included for comparison. As depicted in Fig. 5.14, the output phase noise at 3.75 GHz, 6.75 GHz and 10.25 GHz matches that of the 250 MHz clock reference but is approximately 24 dB, 29 dB and 33 dB higher respectively. This corresponds to the frequency ratio between the output and the clock reference since 20 log (3.75/0.25) = 24 dB, 20 log (6.75/0.25) = 29 dB and 20 log (10.25/0.25) = 33 dB. Fig. 5.14 verifies that the oscillator is phase locked to the 250 MHz clock reference, achieving a relatively low phase noise of –75 dBc/Hz, –69 dBc/Hz and –65 dBc/Hz at 1kHz for the oscillation frequencies of 3.75 GHz, 6.75 GHz and 10.25 GHz respectively. This amounts to a low integrated RMS jitter of less than 3.8 ps from 100 Hz to 100 MHz.

Fig. 5.15, Fig. 5.16 and Fig. 5.17 show the measured pulsed output in the time-domain at 3.75 GHz, 6.75 GHz and 10.25 GHz respectively with the 250 MHz input clock. It is clear that the oscillations settle after a few cycles and within 1 ns from the turn-on instant for all frequency bands. Moreover the phase difference between the $I+$ and $Q+$ outputs is about 92° at 3.75 GHz, 94° at 6.75 GHz and 95° at 10.25 GHz. It should be noted that the Agilent digital oscilloscope is an

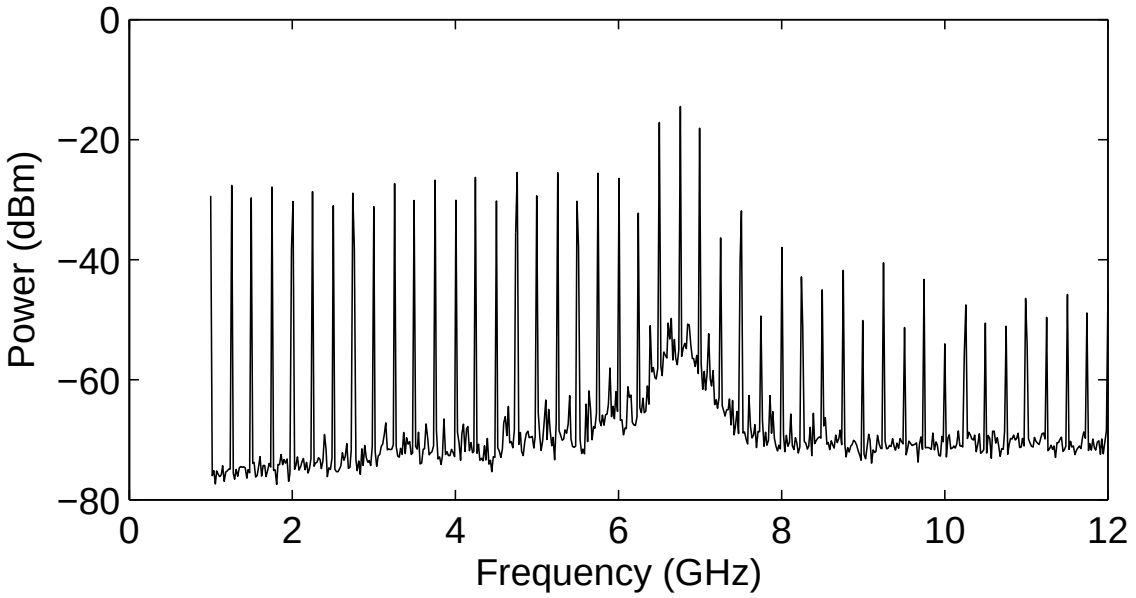


(a)

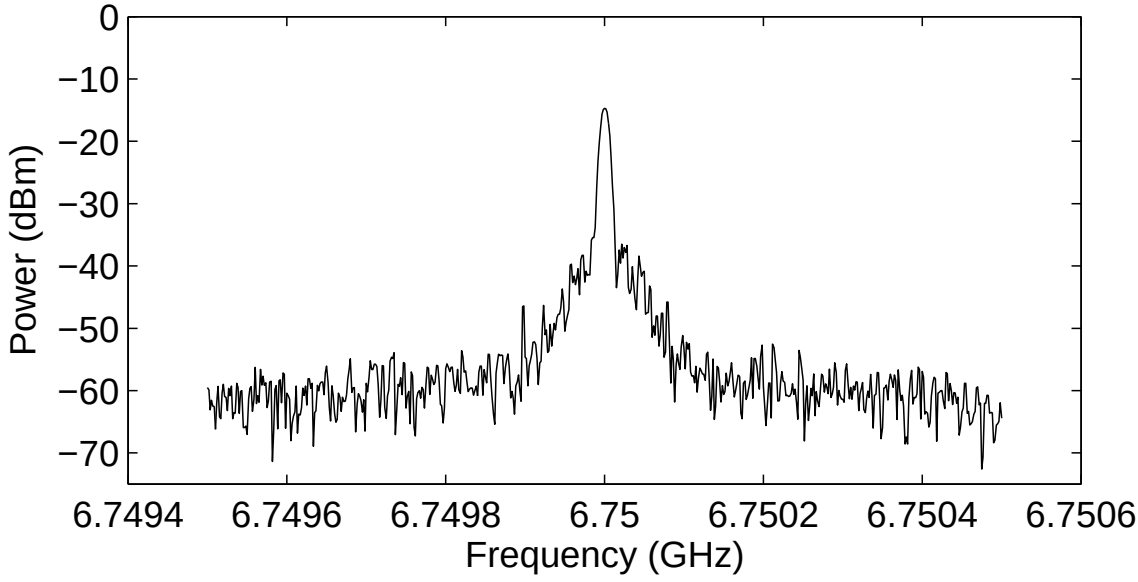


(b)

Figure 5.11: Measured pulsed output spectrum at 3.75 GHz: (a) 10 GHz span and (b) 1 MHz span.

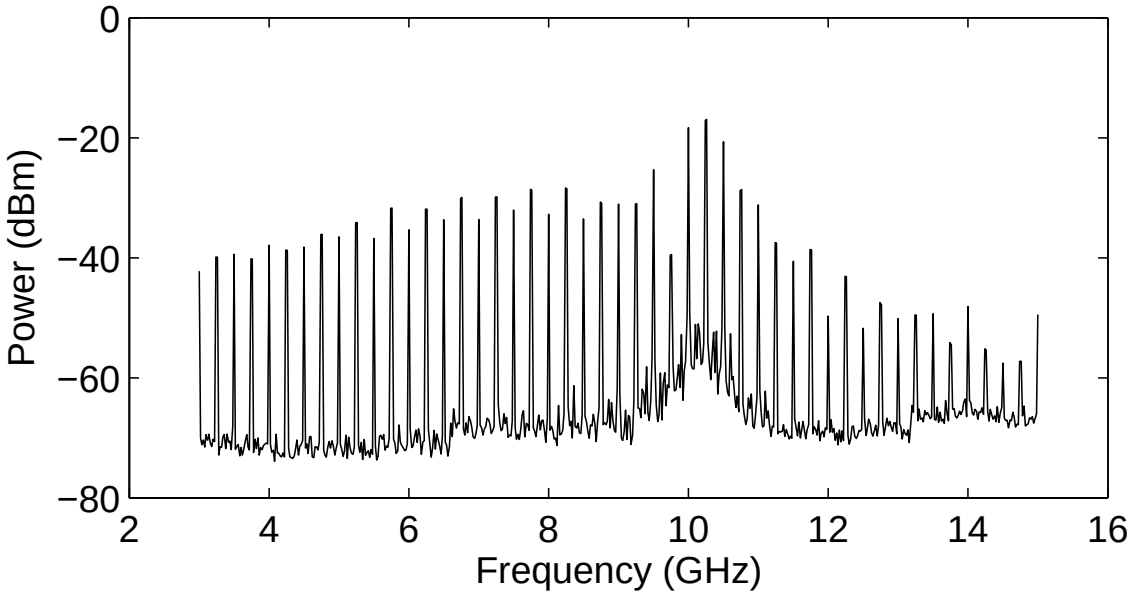


(a)

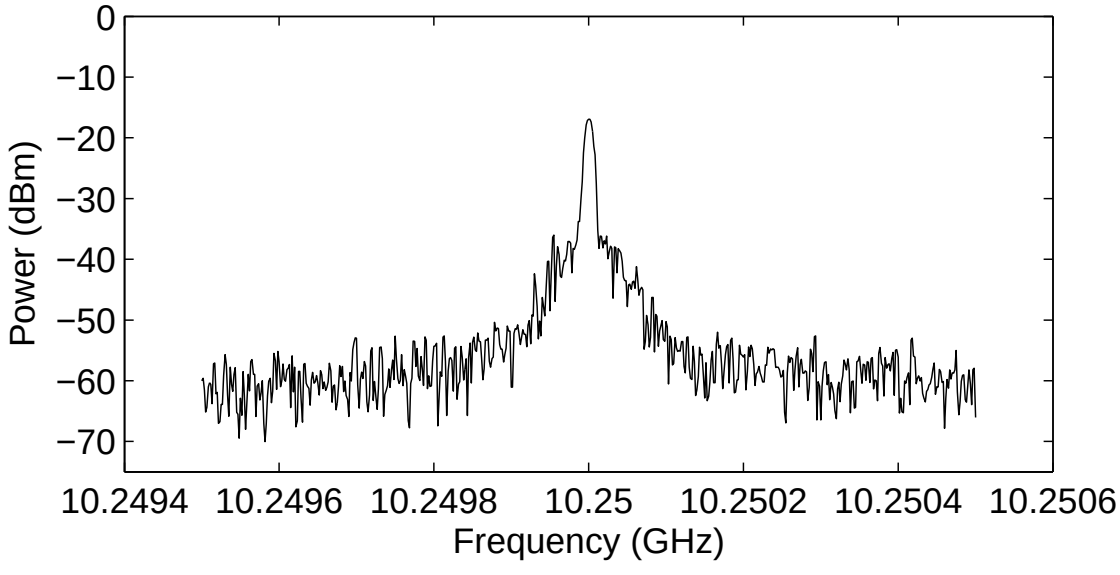


(b)

Figure 5.12: Measured pulsed output spectrum at 6.75 GHz: (a) 11 GHz span and (b) 1 MHz span.

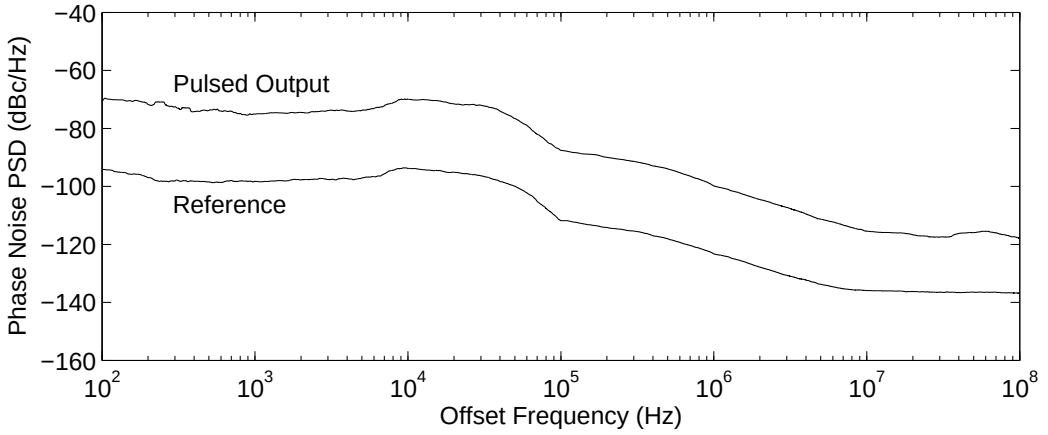


(a)

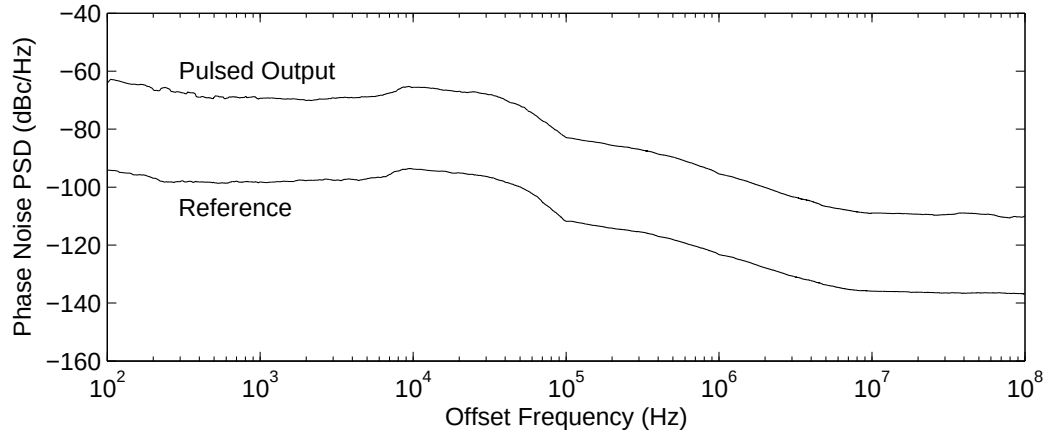


(b)

Figure 5.13: Measured pulsed output spectrum at 10.25 GHz: (a) 12 GHz span and (b) 1 MHz span.



(a)



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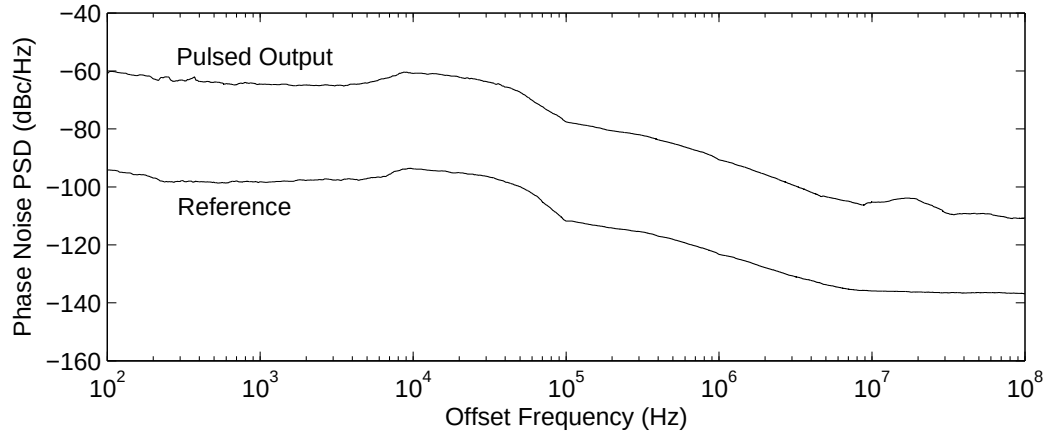


(c)

Figure 5.14: Measured phase noise of pulsed output at: (a) 3.75 GHz, (b) 6.75 GHz and (c) 10.25 GHz.

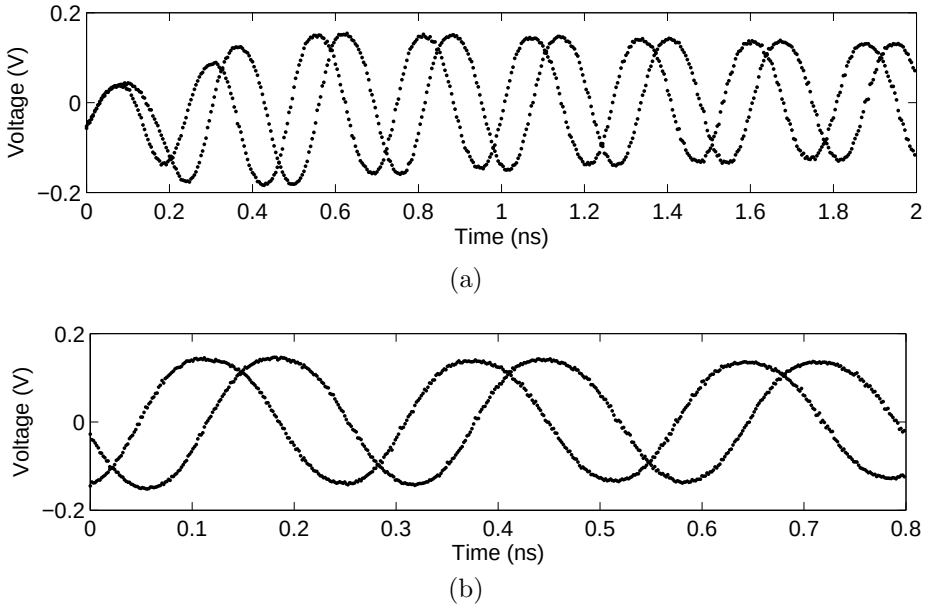
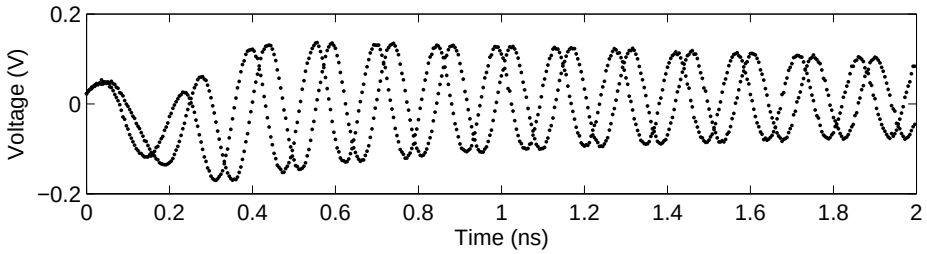
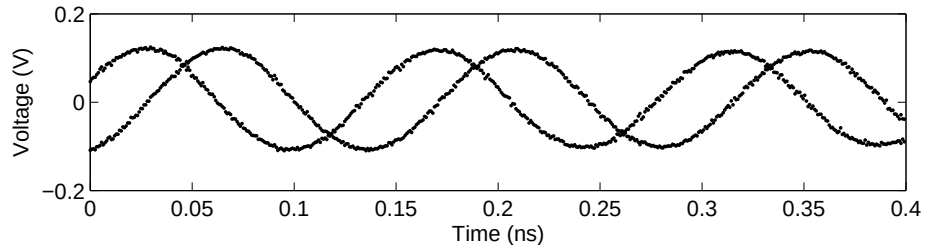


Figure 5.15: Measured pulsed I+ and Q+ outputs in the time-domain at 3.75 GHz: (a) from 0 to 2ns and (b) 3 cycles starting from 0.96 ns.

equivalent time sampling oscilloscope and not a real-time oscilloscope, sampling the signal only once per trigger event. The digital oscilloscope is thus triggered using the input clock for these measurements. Since the 3.75 GHz, 6.75 GHz and 10.25 GHz cycles are clearly visible, the generated pulsed oscillations are indeed coherent with the input clock, and thus pulse-to-pulse coherency is maintained. Furthermore, Fig. 5.18 illustrates the quadrature phase signaling capability of the pulsed oscillator, with the four time-domain measurements superimposed, one for each phase state. Phases 0°, 90°, 180° and 270° correspond to the data patterns 00 ($V_{PI} = 0$V and $V_{PQ} = 0$V), 10 ($V_{PI} = 1.5$V and $V_{PQ} = 0$V), 11 ($V_{PI} = 1.5$V and $V_{PQ} = 1.5$V) and 01 ($V_{PI} = 0$V and $V_{PQ} = 1.5$V) respectively. A good quadrature phase shift of approximately 90° ± 3° is attained for all three oscillation frequencies.

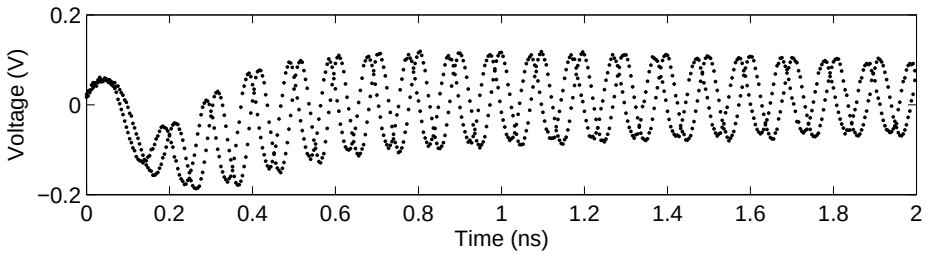


(a)

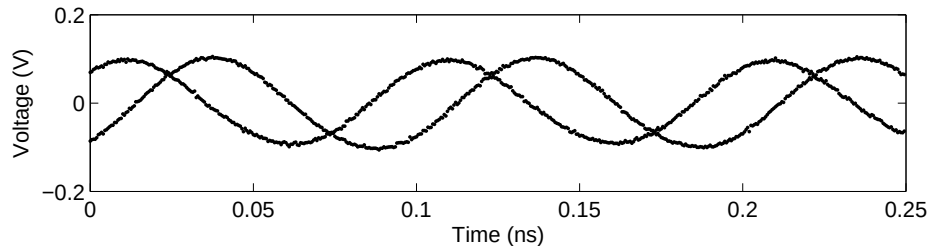


(b)

Figure 5.16: Measured pulsed I+ and Q+ outputs in the time-domain at 6.75 GHz: (a) from 0 to 2ns and (b) 3 cycles starting from 0.96 ns.



(a)



(b)

Figure 5.17: Measured pulsed I+ and Q+ outputs in the time-domain at 10.25 GHz: (a) from 0 to 2ns and (b) 3 cycles starting from 0.96 ns.

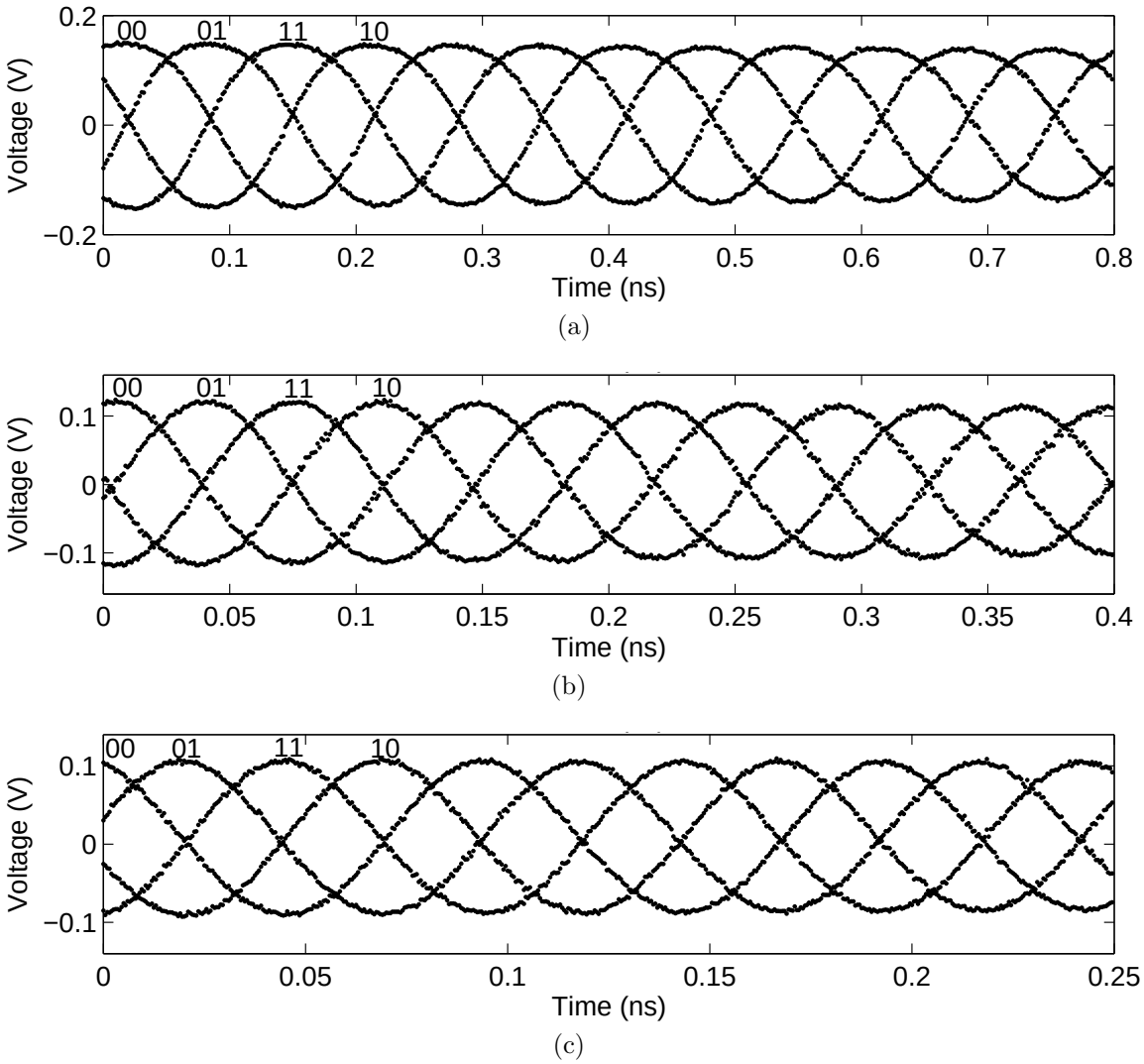


Figure 5.18: Measured pulsed I+ output in the time-domain for the four data patterns and phase states: (a) 3.75 GHz, (b) 6.75 GHz and (c) 10.25 GHz.

Table 5.1 summarizes the proposed pulsed oscillator's performance in comparison with other work [6, 12–15]. Although it can be difficult to make fair comparisons when different specifications, functionalities and technologies are involved, it is apparent that the proposed circuit achieves a relatively low energy consumption of 13–18 pJ/pulse while having comparable phase noise and supporting quadrature phase modulation. The pulsed oscillator's efficiency is also competitive if the energy consumption per pulse is normalized with respect to the output peak-to-peak voltage.

Table 5.1: Summary of pulsed oscillator characteristics.

Reference	**CMOS Process**	**Freq. (GHz)**	**PRF (MHz)**	**Energy (pJ/b)**	**Amplitude (mV)**	**Modulation Scheme**	**PN (dBc/Hz) / RMS Jitter**
[6]	90nm	3–10	1800	126	220	Biphase-PPM	1.9 ps
[12]	180nm	6–10	750	12	30	Biphase	–
[13]	180nm	6–10	50	28	673	On-off	1.8 ps
[14]	180nm	3–5	100	16.8	160	On-off	–
[15]	90nm	3–5	500	56	200	Biphase-PPM	–55 at 1 kHz –122 at 3 MHz
This work	**0.13μm**	**3–10**	**250**	**13–18**	**300–200**	Quadriphase	–75 at 1 kHz 3.8 ps

5.4 Summary

In this chapter, a 3–10 GHz quadrature pulsed oscillator was presented in 0.13 μm CMOS using a two-stage ring architecture with two cross-coupled inverter pairs. Shunt-shunt resistive feedback is employed in the delay stages to extend the frequency tuning range from 3 GHz to more than 10 GHz. Current impulses are injected into the oscillator by switching on one side of each cross-coupled pair just before the other, thus allowing the oscillations to settle within 1 ns. This also locks the phase of the

oscillations to the input clock for high pulse-to-pulse coherence, achieving a low integrated RMS jitter (from 100 Hz to 100 MHz) of less than 3.8 ps. Furthermore, direct quadrature phase modulation was demonstrated over the full UWB bandwidth from 3 GHz to 10 GHz by manipulating the directions of the injected current impulses using a digital startup network. Low power consumption of less than 13 mW at 3 GHz and 18 mW at 10 GHz was achieved with a 250 MHz clock frequency, corresponding to an energy consumption of less than 13–18 pJ per pulse. The IC occupies an active circuit area of only 0.05 mm^2.

Chapter 6

UWB Low Noise Amplifier with Fast Power Switching

6.1 Introduction

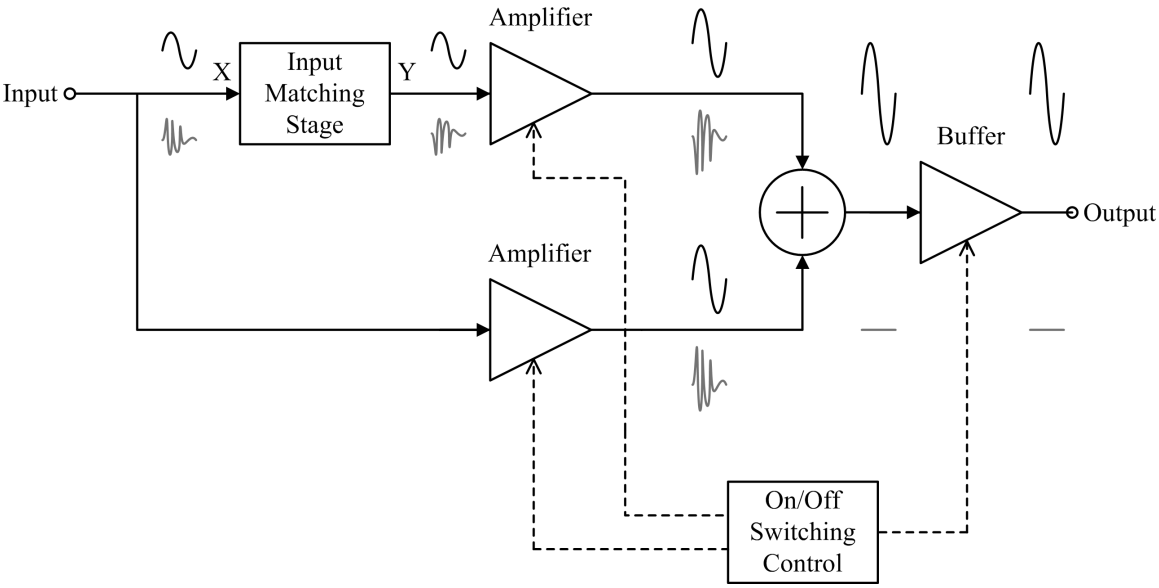
The LNA is not required to operate continuously in pulsed UWB systems, but only when a pulse is being received. Thus applying on and off switching can lead to significant power savings that might not be possible otherwise. However the LNA must respond fast enough to the switching in order to be power efficient. This chapter presents a novel fast switching noise cancelling low noise amplifier (LNA) in 0.13 μm CMOS for pulsed 3.1–10.6 GHz Ultra-Wideband (UWB) applications [45]. Noise cancelling is an effective approach for achieving a low NF and an impedance match simultaneously, however the amplifier stages used for noise cancelling often contribute significant noise themselves at high frequencies degrading the NF [74–77]. New series inductive peaking and inductive degeneration are thus investigated in the noise cancelling topology to simultaneously achieve a sub-4dB flat noise figure (NF) and

a high gain of 16.6 dB for frequencies as high as 10 GHz. Novel fast power switching is also introduced to yield a low power consumption that can be scaled with the duty cycle. It is achieved by bypassing the large DC bias resistors that lead to long charging time constants, allowing the output voltage to settle within only 1.3 ns for a switching frequency as high as 200 MHz. To the author's best knowledge, this is the shortest settling time reported to date. The jitter added by the switched LNA was characterized from the pulsed output phase noise, and the measured integrated RMS jitter is about 750 fs from 10 Hz to 1 MHz. The circuit consumes less than 18 mW of DC power, and it consumes less than 10 mW of average power with a 50% duty-cycle clock. It occupies an active chip area of less than 0.5 mm^2.

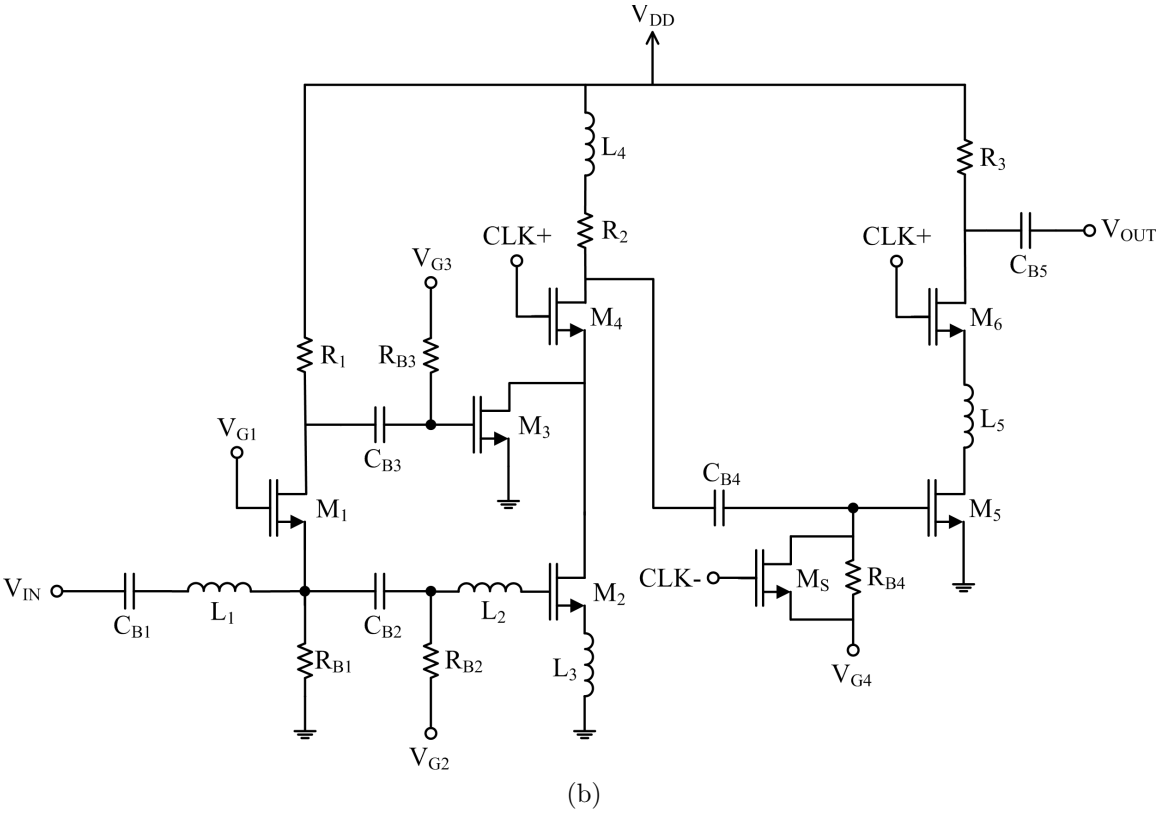
6.2 Circuit Architecture and Design

In this work, a common-gate amplifier is used to provide a wideband input impedance match. As a single stage amplifier can not provide sufficient gain, additional stages (i.e. common-source amplifiers) are added. These amplifiers contribute noise that will affect the NF. However if they are used to cancel the output noise of the input matching device as illustrated in Fig. 6.1a, a lower NF can be achieved [74–77]. In addition, the amplifiers and the output buffer can be quickly switched on and off to save a significant amount of power. The gate of the transistor to be switched on and off should not be in the RF signal path, otherwise isolation will be required and power switching cannot be performed quickly. This way the digital clock circuitry also does not significantly interfere with the RF operation of the LNA, having a small effect on the NF, gain and impedance match.

A circuit schematic of the proposed LNA is shown in Fig. 6.1b. Transistor M_1



(a)



(b)

Figure 6.1: Block diagram and circuit schematic of the proposed LNA.

and resistor R_1 form the common-gate amplifier that provides a wideband input impedance match. An inductor L_1 is connected in series with the source of M_1 to absorb the total parasitic capacitance appearing at this node and improve the input match at high frequencies. The output noise of the matching device (M_1) is cancelled using two other common-source amplifiers M_2 and M_3 as shown in Fig. 6.1b. The noise current of M_1 (i_{ND1}) flows out of the drain but into the source creating two correlated noise voltages with opposite polarities, $V_D \approx -R_1 i_{ND1}/\left(1 + g_{M1}R_S\right)$ and $V_S \approx R_S i_{ND1}/\left(1 + g_{M1}R_S\right)$ respectively, where R_S is the signal source impedance (50 Ω) and g_{M1} is the transconductance of M_1. However, the signal voltages at these nodes are in phase. Thus by amplifying the source and drain voltages using M_2 and M_3 respectively and adding them together, the noise contribution of M_1 can be cancelled while the signal is added. It can be seen that the noise current $\overline{i_{o23}^2}$ at the combined output of M_2 and M_3 is given by:

$$\begin{aligned}\overline{i_{o23}^2} &= \overline{|g_{M2}V_S + g_{M3}V_D|^2} \\ &= \left(\frac{g_{M2}R_S - g_{M3}R_1}{1 + g_{M1}R_S}\right)^2 \overline{i_{ND1}^2}\end{aligned} \tag{6.1}$$

where g_{M2} and g_{M3} is the transconductance of M_2 and M_3 respectively. Cancellation can thus be achieved if, to the first order, $g_{M2}R_S \approx g_{M3}R_1$. When this condition is met, the noise from the noisiest component of the LNA can be eliminated. Note that the noise generated by R_1 can not be cancelled because it appears in phase at the drain and source nodes of transistor M_1. However this noise contribution can be made negligibly small by using a sufficiently large resistance value for R_1.

After cancelling the output noise of matching device M_1, the noise generated by

the common-source device M_2 dominates the NF of the LNA. Note that the gain of the common-gate amplifier M_1 reduces the noise contribution of the common-source amplifier M_3. The width, transconductance and gain of M_2 can be made relatively large to reduce its noise contribution. However this increases the gate-source C_{GS2} and gate-drain C_{GD2} parasitic capacitances diminishing the increase in gain and deteriorating the NF at high frequencies. To mitigate this effect, an inductor (L_2) is connected in series with the gate of M_2 to absorb its parasitic capacitance and increase the bandwidth. In addition, inductive degeneration is used at the source of M_2 (L_3). An equivalent small signal model of M_2, L_2 and L_3 is illustrated in Fig. 6.2. It can be shown that the input impedance (Z_{i2}), effective transonductance (G_{M2}), input-referred noise current ($\overline{i_{NI}^2}$) and input-referred noise voltage ($\overline{v_{NI}^2}$) of the common-source amplifier M_2 are given by:

$$Z_{i2} = \frac{g_{M2}L_3}{C_{GS2}} + j\omega\left(L_2 + L_3\right) - \frac{j}{\omega C_{GS2}}, \tag{6.2a}$$

$$G_{M2} = \frac{g_{M2}}{1 - \omega^2 C_{GS2}\left(L_2 + L_3\right) + j\omega g_{M2}L_3}, \tag{6.2b}$$

$$\overline{i_{NI}^2} = \frac{\omega^2 C_{GS2}^2}{g_{M2}^2}\overline{i_{ND2}^2}, \tag{6.2c}$$

$$\overline{v_{NI}^2} = \frac{\left(1 - \omega^2 C_{GS2}\left(L_2 + L_3\right)\right)^2}{g_{M2}^2}\overline{i_{ND2}^2}. \tag{6.2d}$$

where $\overline{i_{ND2}^2}$ is the drain-source noise current of M_2. Equation (6.2) indicates that L_2 and L_3 can increase G_{M2} and reduce $\overline{v_{NI}^2}$ at high frequencies. This occurs while $\overline{i_{NI}^2}$ remains unaffected. Therefore the gain of the common-source amplifier M_2 can be increased, while its total input-referred noise and NF contribution can be suppressed at high frequencies by using L_2 and L_3. Fig. 6.3 shows the schematic simulation results for the NF and gain $|S_{21}|$ of the LNA with and without the inductors L_2 and L_3.

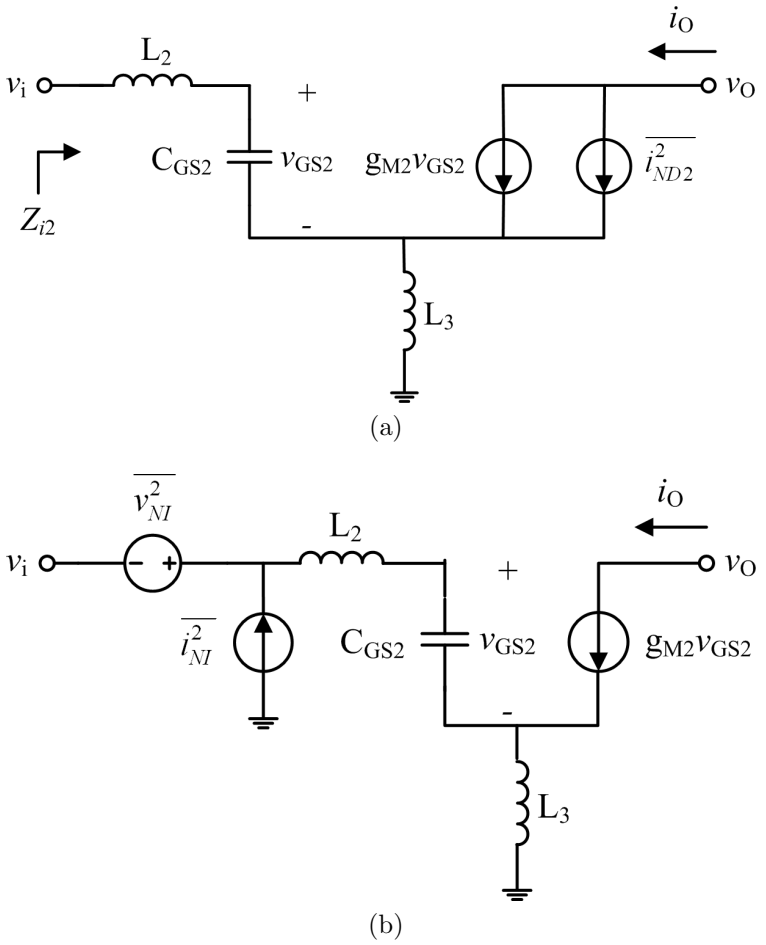
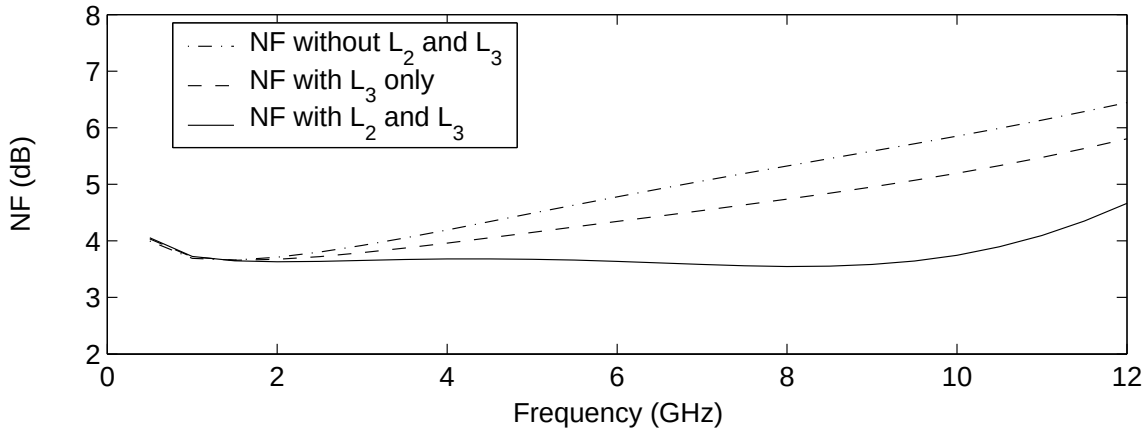


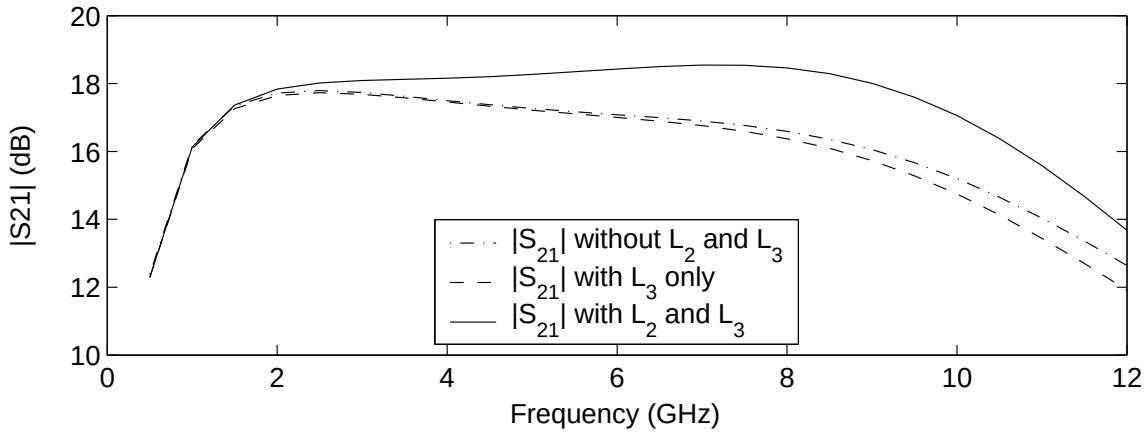
Figure 6.2: Small signal model of the M_2 with L_2 and L_3: (a) output drain-source noise current $\overline{i_{ND2}^2}$, and (b) input-referred noise voltage $\overline{v_{NI}^2}$ and current $\overline{i_{NI}^2}$.

RF models provided by the foundry are used in this simulation for all devices shown in Fig. 6.1b including the transistors, on-chip spiral and line inductors, and metal-insulator-metal (MIM) capacitors as they can predict their measured performance more closely. It is clear that the noise figure can be reduced by about 2 dB at high frequencies around 10 GHz using inductors L_2 and L_3. This is accompanied with an increase in gain of approximately 2 dB at 10 GHz.

The inductor L_3 is also used to provide a wideband input impedance match. Fig.



(a)



(b)

Figure 6.3: Simulated LNA NF and gain $|S_{21}|$ with and without inductors L_2 and L_3.

6.4 shows an equivalent small signal model of the input network consisting of M_1, M_2, L_2 and L_3 from which the input impedance Z_{IN} can be written as:

$$Z_{IN} = j\omega L_1 + \frac{X - jY}{X^2 + Y^2}, \tag{6.3}$$

where

$$X = g_{M1} + \frac{\omega^2 g_{M2} L_3 C_{GS2}}{\omega^2 g_{M2}^2 L_3^2 + \left(1 - \omega^2 C_{GS2}\left(L_2 + L_3\right)\right)^2}, \tag{6.4a}$$

$$Y = \omega C_{GS1} + \frac{\omega C_{GS2}\left(1 - \omega^2 C_{GS2}\left(L_2 + L_3\right)\right)}{\omega^2 g_{M2}^2 L_3^2 + \left(1 - \omega^2 C_{GS2}\left(L_2 + L_3\right)\right)^2}, \tag{6.4b}$$

and C_{GS1} is the gate-source parasitic capacitance of M_1. The inductance L_3 increases the real part of the input impedance $\mathrm{Re}\{Z_{IN}\} = X/\left(X^2 + Y^2\right)$ and improves the input match at high frequencies. This also reduces the quality factor Q of the input network for a wideband input impedance match. The input impedance Z_{IN} is designed to be closest to the source impedance towards the higher end of the UWB band from 6 GHz to 10 GHz, i.e. $\mathrm{Re}\{Z_{IN}\} \approx R_S$ and $\mathrm{Im}\{Z_{IN}\} \approx 0$. A good impedance match is also achieved in the lower end of the UWB band from 3 GHz to 5 GHz due to the low quality factor and broadband frequency response of the input network. Fig. 6.5 shows the schematic simulation result for the input reflection coefficient $|S_{11}|$ of the LNA with and without the inductor L_3. It is clear that the input matching can be improved by about 6 dB at 10 GHz.

The biasing current of the common-source amplifiers M_2 and M_3 is switched on and off by cascoding a second common-gate device M_4 at their outputs, which are connected together for signal combination. This cascode device also acts as a current buffer to reduce the miller effect, improve the high frequency response and increase

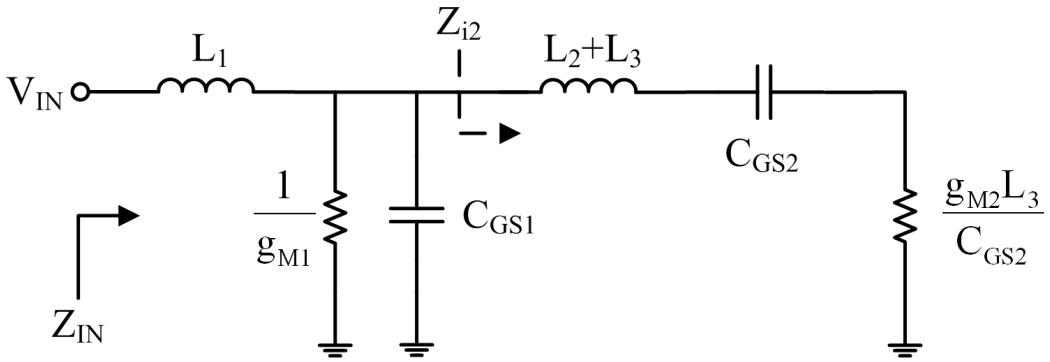


Figure 6.4: Small signal model of the input matching network.

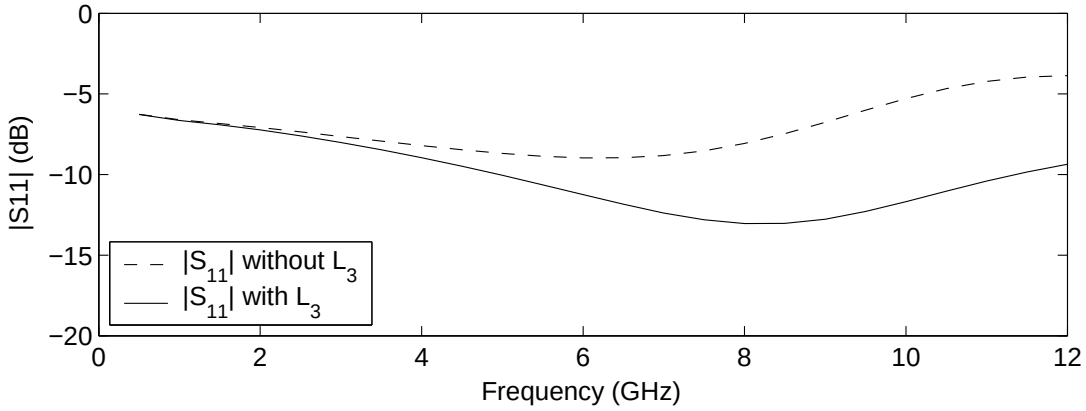


Figure 6.5: Simulated input reflection coefficient $|S_{11}|$ with and without inductor L_3.

the reverse isolation. Shunt inductive peaking (L_4) is employed at the drain of M_4 to increase the bandwidth. Inductive peaking can be intuitively explained from the time-domain step response of the circuit shown in Fig. 6.6. Without the inductor L_4, the charging time constant for the voltage at the drain of M_4 (v_{D4}) would be $\tau \approx R_2 C_T$, and the voltage rise time from 10% to 90% would be $t_r \approx 2.2\tau$, where R_2 is the load resistance and C_T is the total parasitic capacitance seen at the drain of M_4. By adding the inductance L_4 as shown in Fig. 6.6, the load resistance R_2 can be decoupled from the output loading capacitance C_T, to force all of the available charging current from M_4 to flow into the capacitance C_T. This reduces the charging rise time t_r of the drain voltage v_{D4} which implies an increase in the frequency bandwidth. Fig. 6.7 shows schematic simulation results for the gain $|S_{21}|$ of the LNA with and without the inductor L_4. It is clear that the gain can be increased by about 5 dB at high frequencies around 10 GHz using inductor L_4.

A second amplification stage M_5 is added (AC coupled) to increase the gain to more than 16 dB and provide an output impedance match from 3 GHz to 10 GHz. The biasing current of the common-source amplifier M_5 is switched on and off using

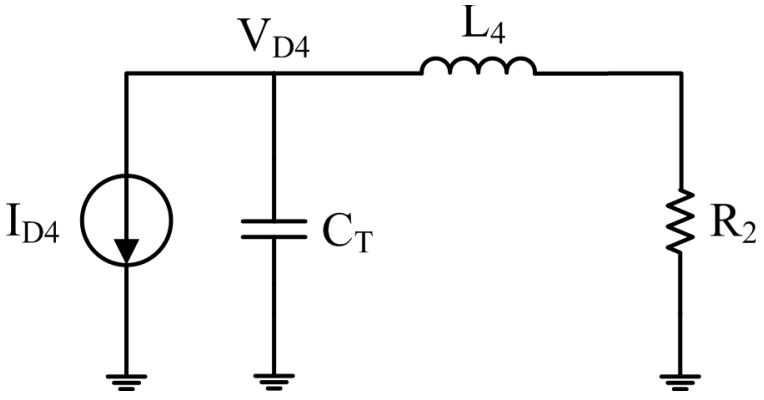


Figure 6.6: Two-pole shunt inductive peaking network.

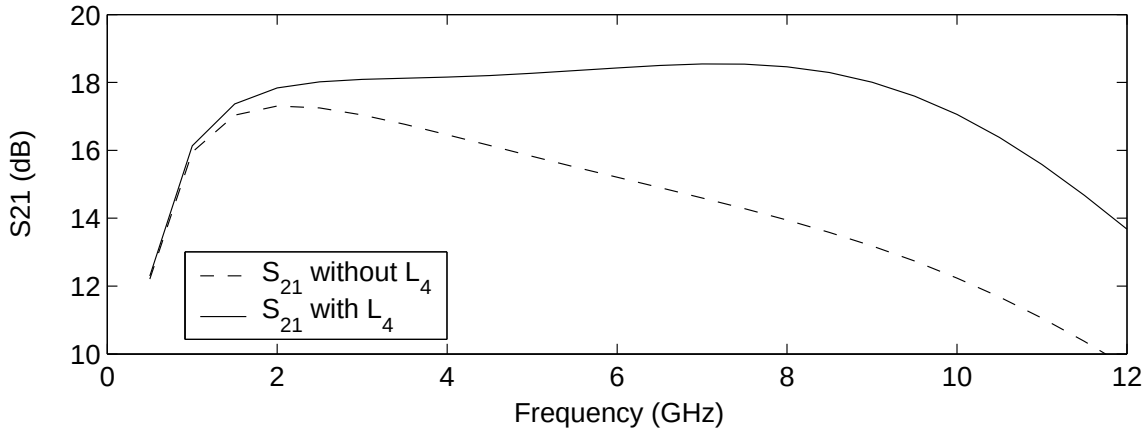


Figure 6.7: Simulated LNA gain $|S_{21}|$ with and without inductor L_4.

the cascode common-gate device M_6, which also reduces the miller effect for a wider bandwidth. An inductor (L_5) is connected between the drain of M_5 and source of M_6 to absorb the parasitic capacitances at these nodes and further extend the bandwidth. Finally, the load resistance value of $R_{D3} = 67\Omega$ is chosen to provide a good broadband output impedance match when driving the 50Ω load impedance of the measurement equipment. Fig. 6.8 shows schematic simulation results for the gain $|S_{21}|$ of the LNA with and without the inductor L_5. It is clear that the gain can be increased by about 1.7 dB at high frequencies around 10 GHz using inductor L_5.

Fast switching can only be achieved by bypassing the large DC bias resistor R_{B4} that leads to a long charging time constant of $\tau \approx R_{B4}C_{B4}$. An NMOS switch M_S is thus added in parallel to the DC bias resistor R_{B4}, which is activated only for a short time period (0.8 ns) after startup. The NMOS device M_S is made sufficiently wide for a relatively small on-resistance R_{MS} to reduce the equivalent bias resistance $R_{MS}||R_{B4}$ during this short period of time. The output voltage amplitude can thus settle within 1.3 ns. A square-wave clock signal and its delayed inverse are created

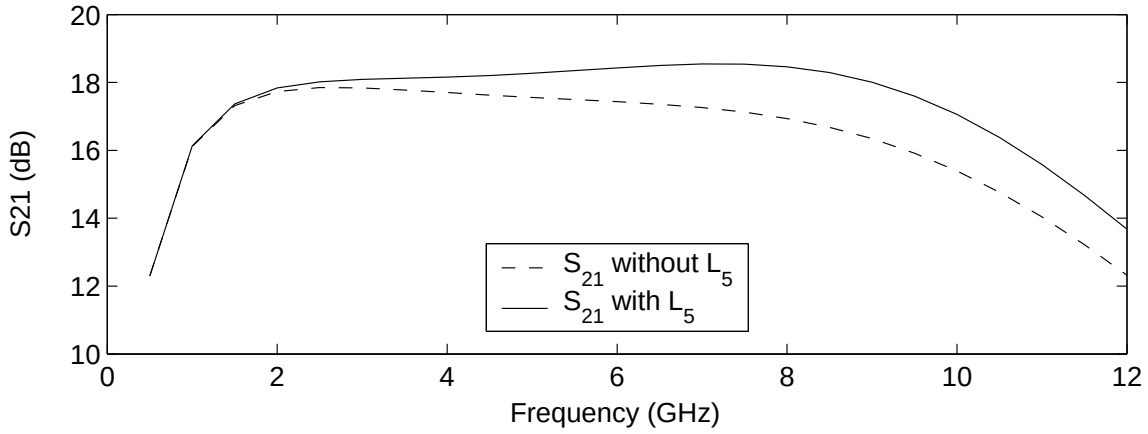


Figure 6.8: Simulated LNA gain $|S_{21}|$ with and without inductor L_5.

from the input sinusoidal clock, namely $CLK+$ and $CLK-$ as shown in Fig. 6.9. The clock signal $CLK+$ is used to trigger the cascode transistors M_4 and M_6, while the delayed and inverted clock signal $CLK-$ is used to activate the switch M_S. There is a short time period (0.8 ns) where $CLK-$ is still held at logic high after the rising edge of $CLK+$, during which the switch M_S remains on to minimize the equivalent bias resistance and reduce the settling time after startup. CMOS inverters are used to sharpen the edges of the input clock, while current-starved CMOS inverters are used to generate the small delay of 0.8 ns between the clock signals $CLK+$ and $CLK-$.

6.3 Simulation and Measurement Results

The LNA was fabricated in a standard 0.13μm CMOS process and a photograph of the IC is shown in Fig. 6.10. It occupies a die area of 1mm^2 including bonding pads, decoupling capacitors and the chip guard ring (plus chamfer regions), while the core circuit area is 660×760μm^2. The circuit consumes less than 18 mW of DC or peak power, while it consumes less than 10 mW of average power (P_{AVG}) at a clock

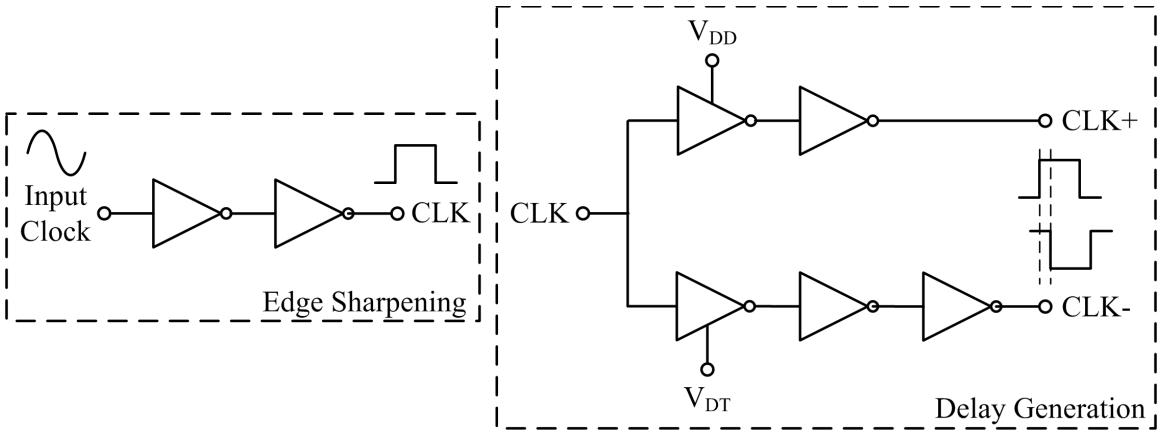


Figure 6.9: Clock edge sharpening and delay generation circuits.

frequency of 100 MHz. The LNA's power when switched off is also about 0.7 mW, which is significantly lower than the peak power consumption.

The UWB LNA IC was measured directly on-wafer using 40GHz coplanar waveguide (CPW) probes and DC probes. A 50GHz Agilent vector network analyzer (8510C VNA) was used for the S-parameter measurements, while a 50GHz Agilent spectrum analyzer (E4448A) was used for noise figure, power spectrum, and phase noise measurements. A 60GHz Tektronix Digital Serial Analyzer (DSA8200) was also used to observe the output in the time domain.

Fig. 6.11 shows the measured two-port S-parameters and NF of the LNA in comparison with the post-layout simulation results. Both measurements and simulation have the same bias conditions, and there is good agreement between the measured and simulated results. Predrawn device layouts characterized and modelled by the foundry were used as-is in this design to achieve the best model-to-hardware correlation. A full-chip extraction was also carried out using Assura RCX to predict the parasitics of the interconnects. It is clear that the transmission coefficient S_{21} and NF are quite flat from 3 GHz to 10 GHz at about 16.6 $\pm$ 0.75 dB and 3.9 $\pm$ 0.28 dB

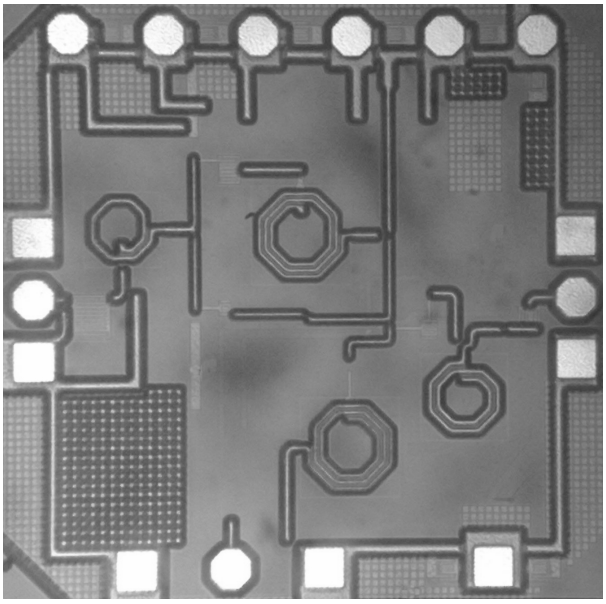
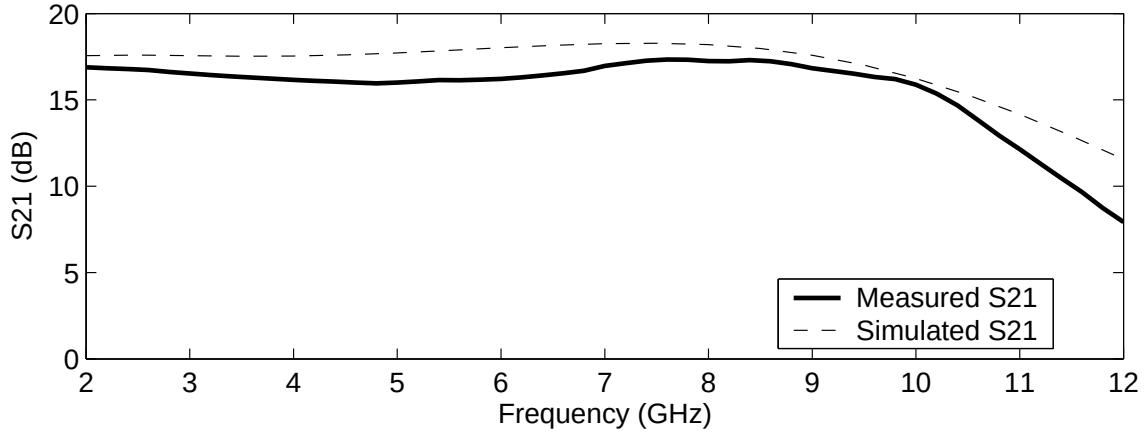


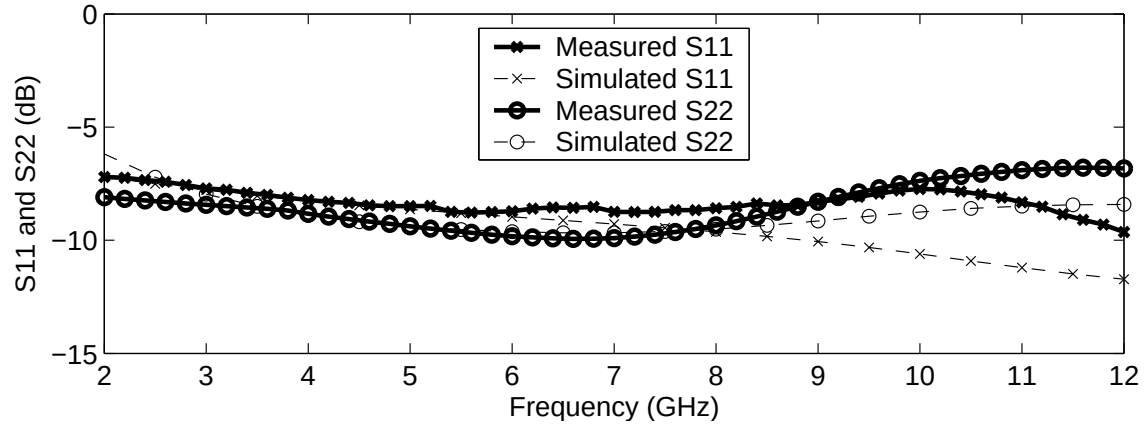
Figure 6.10: Photograph of UWB LNA IC.

respectively. The NF measurement uncertainty in the 3 GHz to 10 GHz frequency range is less than ± 0.24 dB and is depicted in Fig. 6.11c using error bars. The input and output reflection coefficients S_{11} are also below –8 and –7 dB respectively from 3 GHz to 10 GHz. The measured group delay is shown in Fig. 6.12, which depicts an average value of 105ps with a small variation of ± 18ps in the 3 GHz to 10 GHz bandwidth. The linearity of the LNA was tested and the (input) output third-order intercept point varies from (–8.6 dBm) 7.8 dBm to (–9.2 dBm) 6.4 dBm over the 3 GHz to 10 GHz frequency range. The output 1dB compression point were also measured to be –2.2 dBm, –4.0 dBm and –4.6 dBm at 3 GHz, 7 GHz and 10 GHz respectively.

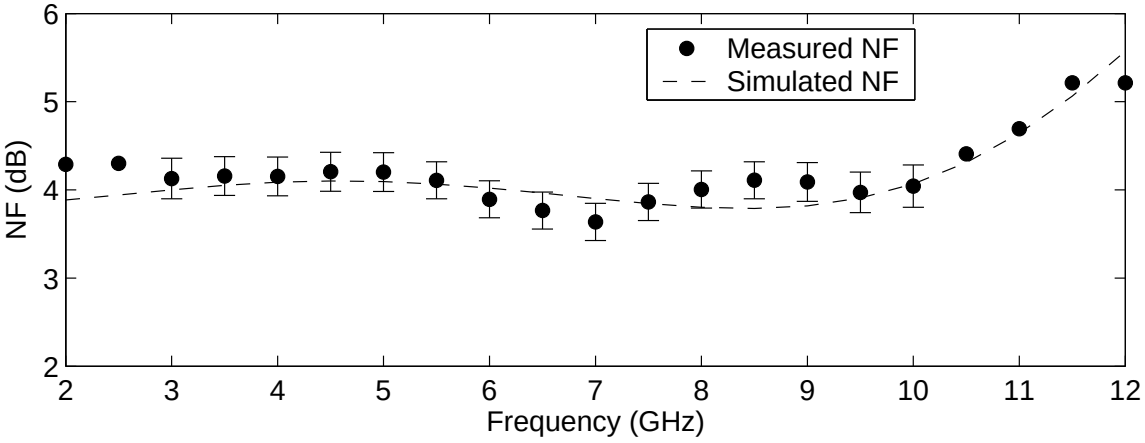
The performance of the LNA while being switched on and off was also tested using 100 MHz and 200 MHz clock signals. The input clock is a periodic sinusoidal signal which is converted on-chip into a digital square wave using the edge sharpening



(a)



(b)



(c)

Figure 6.11: Measured LNA two-port S-parameters ((a), (b)) and NF ((c)).

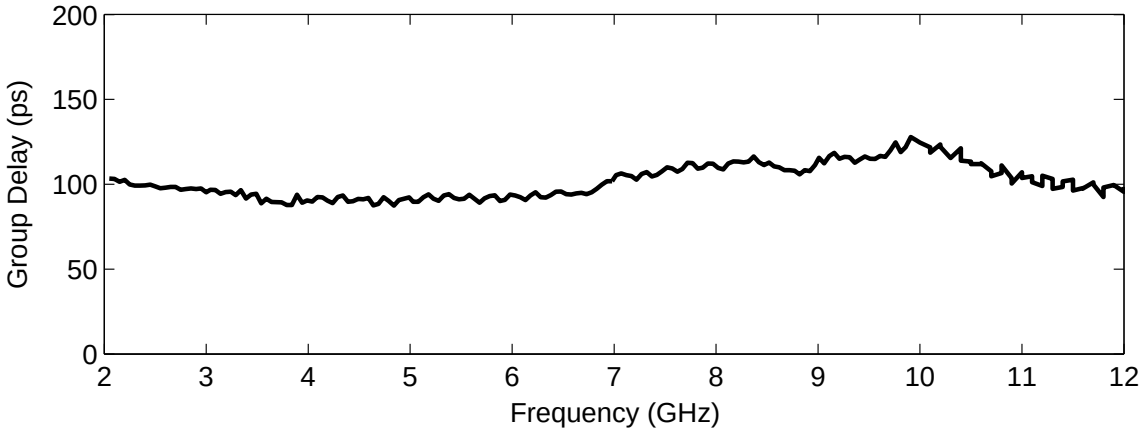
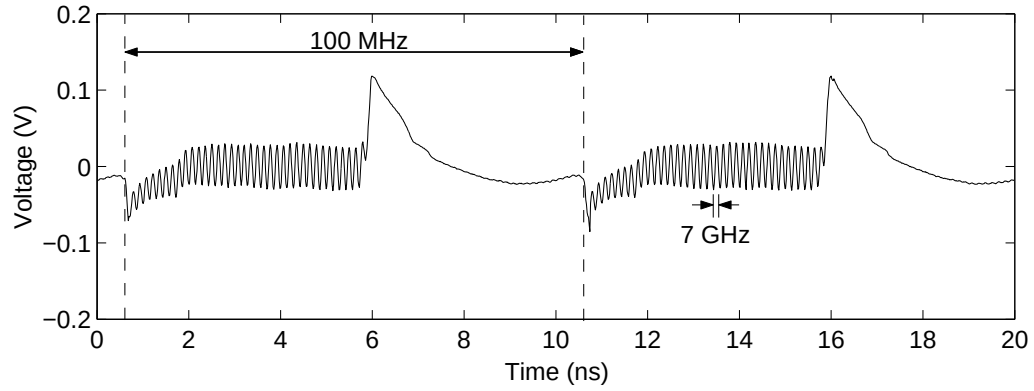


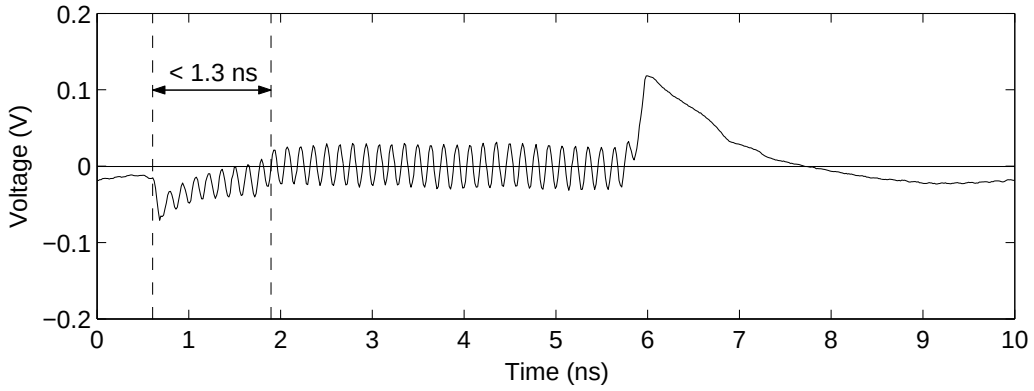
Figure 6.12: Measured LNA group delay from 2 GHz to 12 GHz.

inverters. The output was first measured in the time-domain at 100 MHz and 200 MHz clock frequencies, and Fig. 6.13 and Fig. 6.14 show the DSA's measurement results. A 7 GHz sinusoidal signal was used for the RF input of the LNA for the time-domain measurements. It is clear that the output is periodic and coherent, and that the LNA gain can settle within 1.3ns from the turn-on instant.

The output power spectrum was also measured using the spectrum analyzer and is plotted in Fig. 6.15a over a span of 1 GHz around the center (input) frequency of 7 GHz. It is clear that the harmonic components generated at multiples of the clock frequency (100 MHz) are coherent and well-defined. Fig. 6.15b shows the measured phase noise of the 7 GHz component in the output spectrum. The phase noise of the input 7 GHz reference is also included for comparison. As depicted in Fig. 6.15b, the output phase noise matches that of the input signal but is approximately 6-10 dB higher. This amounts to an integrated RMS jitter (J_{OUT}) of about 750 fs from 10 Hz to 1 MHz. The input integrated RMS jitter (J_{IN}) from 10 Hz to 1 MHz is 420 fs. Also shown in Fig. 6.15b is the residual phase noise added by the switched



(a)



(b)

Figure 6.13: Measured time-domain output at 100 MHz: (a) two clock periods and (b) one clock period.

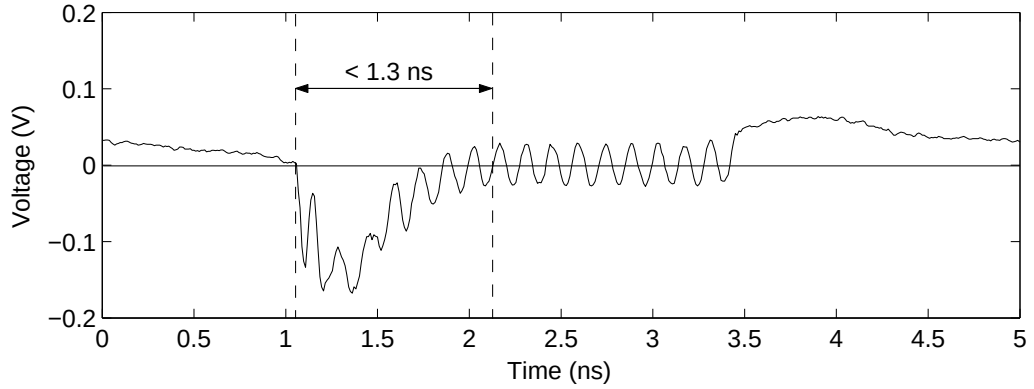


Figure 6.14: Measured time-domain output at 200 MHz (one clock period).

LNA (L_{LNA}), which has been calculated by deducting the input phase noise from the output phase noise (in magnitude), and then converting the result into decibels (dB):

$$L_{LNA} = 10\log\left(10^{\frac{L_{OUT}}{10}} - 10^{\frac{L_{IN}}{10}}\right) \tag{6.5}$$

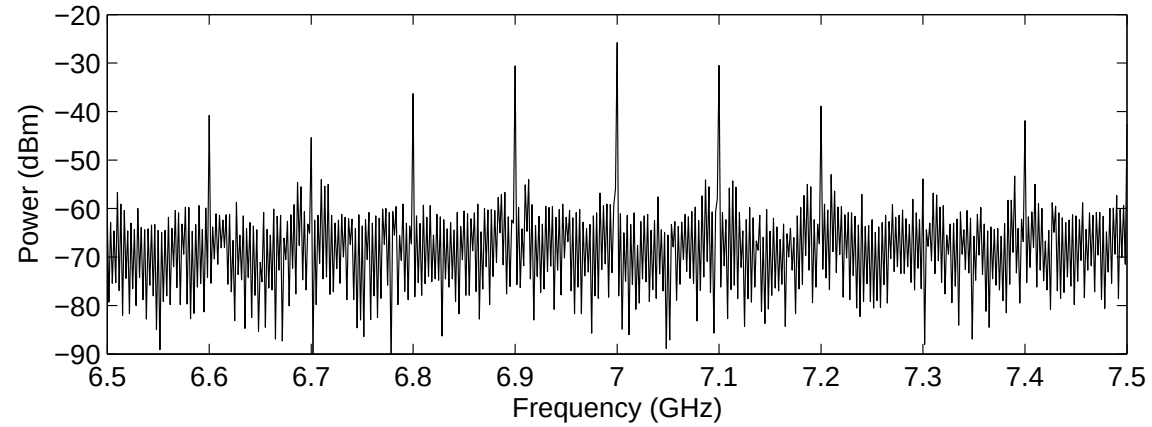
where L_{OUT} and L_{IN} are the measured output and input phase noise respectively shown in Fig. 6.15b. The integrated RMS jitter added by the switched LNA (J_{LNA}) from 10 Hz to 1 MHz can thus be calculated from the switched LNA residual phase noise (L_{LNA}) to be about 620 fs. Note that that this satisfies the relationship:

$$J_{OUT}^2 = J_{LNA}^2 + J_{IN}^2 \tag{6.6}$$

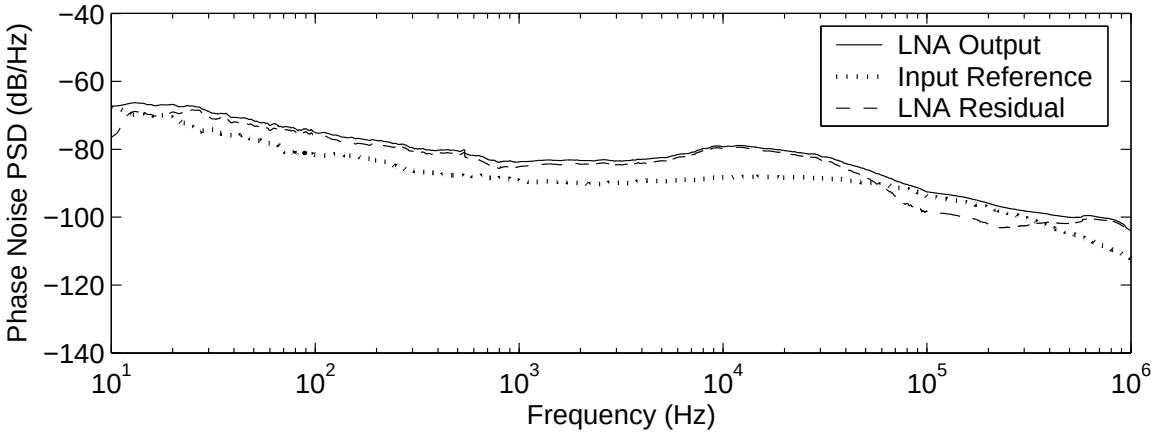
Table 6.1 summarizes the proposed LNA's performance in comparison with other recently reported broadband LNAs. To aid the comparison, a figure of merit (FOM) suitable for the broadband amplifiers has been calculated and is defined as:

$$FOM\,[\text{GHz/mW}] = \frac{|S_{21}|\,[1] \times BW\,[\text{GHz}]}{(NF\,[1] - 1) \times P_{DC}\,[\text{mW}]} \tag{6.7}$$

where $|S_{21}|\,[1]$ is the power gain in magnitude, $BW\,[\text{GHz}]$ is the bandwidth in GHz, $(NF\,[1] - 1)$ is the excess NF in magnitude, and $P_{DC}\,[\text{mW}]$ is the DC power consumption in mW. For the FOM calculation, the 3-dB bandwidth is considered, while the NF is the maximum value within the 3–10 GHz frequency range. The unity current gain frequency f_T or the unity power gain frequency f_{max} of the CMOS process (i.e. technology cost) could not be included in the FOM since it is not explicitly reported in most of the previously published work. As can be seen from Table 6.1,



(a)



(b)

Figure 6.15: Measured LNA output: (a) power spectrum and (b) phase noise.

Table 6.1: Summary of LNA's characteristics.

Reference	**CMOS process**	**Power** (mW)	**S_{21}** (dB)	**Bandwidth** (GHz)	**NF** (dB)	**FOM** (GHz/mW)	**Pulsed?**
[40]	130 nm	37.8/6.86	20.47/11.03	0.4–10.5/0.7–10.9	3.29/4.25	19.33/6.32	No
[41]	130 nm	14.4	12.4	0.1–14	2.7–3.7	12.48	No
[72]	90 nm	20.4	12.7	0.1–20	3.3–5.5	12.98	No
[67]	130 nm	26	15	0.0–12	2.3–4.5	8.63	No
[73]	90 nm	12.5	15.4	0.0–21	4.4–6.0	19.54	No
This Work	**130 nm**	**18/10**	**16 ± 0.75**	**1–10.6**	**3.9±0.28**	**15.07**	**Yes**

our proposed LNA exhibits a good balance between performance metrics and thus a relatively high FOM compared to other work.

6.4 Summary

A fast switching noise cancelling LNA has been demonstrated in 0.13 μm CMOS for 3.1–10.6 GHz UWB applications. A new noise cancelling technique with inductive degeneration and series inductive peaking is employed to simultaneously achieve a flat sub-4dB noise figure (NF) and a flat gain of 16.6 dB for frequencies up to 10 GHz. Large resistors used for DC biasing that lead to long charging time constants are bypassed allowing the output voltage to settle within only 1.3 ns for fast switching speeds of up to 200 MHz. The phase noise and jitter added by the switched LNA were characterized, and the measured output integrated RMS jitter is about 750 fs from 10 Hz to 1 MHz, while the input integrated RMS jitter is 420 fs. The circuit consumes less than 10 mW of average power at 50% duty-cycle and occupies an active chip area of less than 0.5 mm^2.

Chapter 7

Summary and Conclusions

7.1 Summary

Pulsed Ultra Wideband (UWB) technology is based on the transmission of pulses with a short time duration on the order of a nanosecond to spread the signal power over a wide bandwidth for high precision ranging, robustness to multipath fading and high data rates. This duty-cycled nature of pulsed UWB signaling can be exploited in the design of RF transceiver front-ends by only enabling the RF blocks when a pulse is being transmitted or received, thus achieving significant power savings that might not be possible otherwise. By switching off RF components when not in use, the isolation between them can be increased, reducing local oscillator (LO) leakage, LO self-mixing, DC offsets, and interference. Nevertheless such duty-cycled operation of the RF front-end requires fast-settling pulsed RF components, which poses serious challenges in circuit design. In this thesis, pulse generators and pulsed low noise amplifiers were proposed in low-cost CMOS technology that can settle within one nanosecond to fully benefit from the duty-cycled characteristic of pulsed UWB.

An energy-efficient pulse generator was first demonstrated in 0.13 μm CMOS for short-range high-data-rate 3.1–10.6 GHz UWB applications. A ring oscillator consisting of current-starved CMOS inverters is quickly switched on and off for the duration of the pulse, and the amplitude envelope is shaped using a variable attenuator. The ring oscillator is designed to generate an oscillation frequency of 4.8 GHz at a low power consumption, while the passive variable attenuator consumes zero DC power and has a wide bandwidth. A low-power glitch generator (CMOS NOR gate) is integrated on-chip to create a baseband impulse that controls the variable attenuator. The glitch generator combines the falling-edge of the clock signal and its delayed inverse to form the impulse. This allows the duration of the output UWB pulse to be changed by varying the delay between the edges. Several UWB pulses were measured with a time duration varying from 500 ps to 900 ps, a peak-to-peak voltage amplitude of 150 mV and a high out-of-band rejection of more than 20 dB. The entire circuit operates in switched-mode with zero static current for a low average power consumption of less than 3.8 mW at 910 MHz pulse repetition frequency (PRF), or below 4.2 pJ of energy per pulse. It occupies a total area of 725×600 μm^2 including bonding pads and decoupling capacitors, and the active circuit area is only 360×200 μm^2.

A quadrature pulse generator was then investigated for short-range 22–29 GHz UWB vehicular radar. It can be used in pulsed UWB vehicular radar transceivers to provide template pulses for quadrature pulse correlation and detection, or to enable quadrature phase modulation for enhanced pulse compression, detection, and interference mitigation. The pulse generator can be operated at a PRF as high as 600 MHz to be shared between the transmitter and receiver with a time delay as short as 1.66 ns. Two quadrature-coupled inductor-capacitor (LC) oscillators operating at

24 GHz are used for the local oscillator (LO), which are switched on and off using a new technique. By switching on one side of each differential LC oscillator just before the other, a current impulse is injected into the LC tank that has a short time duration and large harmonic components out to 24 GHz, forcing a large initial condition to reduce the settling time to about 0.5 ns. It also locks the initial phase of the oscillations for high pulse-to-pulse coherence. The pulsed output phase noise was measured and characterized, and a relatively low phase noise of -70 dBc/Hz and -100 dBc/Hz was achieved at 1 kHz and 1 MHz offsets respectively with a 500 MHz clock. A π-network attenuator then modulates the LO signal to generate the UWB pulse. The attenuator is controlled using impulses which can be readily tuned to vary the width of the UWB pulse over a wide range from 375 ps to over 1 ns. Several UWB pulses were demonstrated with a time duration ranging from 375 ps to 650 ps, a measured peak-to-peak voltage amplitude of 240 mV, a quadrature phase accuracy of 90 $\pm$ 3° and an out-of-band rejection of more than 20 dB. The fabricated IC in 0.13 μm CMOS consumes only 2.2 mW and 14.8 mW of average power at PRFs of 50 MHz and 600 MHz respectively, or less than 11 pJ of energy for each of the four differential quadrature pulses. It occupies a total die area of 0.94 mm^2, while the active circuit area is only 0.41 mm^2.

Next, a tunable 3–10 GHz quadrature pulsed oscillator was presented using 0.13 μm CMOS for 3.1-10.6 GHz UWB applications. It is intended to be used as part of a quadrature pulse generator, providing template pulses for quadrature pulse correlation, and supporting binary and quadrature phase modulation. A two-stage CMOS ring oscillator with two cross-coupled inverter pairs and shunt-shunt resistive feedback is investigated for a wide tuning range, which is switched on and off using a new

technique. By switching on one side of each cross-coupled inverter pair just before the other, a current impulse is injected that enables fast oscillator startup within 1 ns without significantly affecting the oscillation frequency. It also locks the initial phase of the oscillations to the input clock for high pulse-to-pulse coherence. A low phase noise of –75 dBc/Hz is thus achieved at 1 kHz offset, and the integrated RMS jitter from 100 Hz to 100 MHz is less than 3.8 ps with a 250 MHz clock. Furthermore, binary and quadrature phase modulation are directly implemented, avoiding the use of a power hungry wideband modulator or a large balun. A good quadrature phase modulation accuracy of $90^\circ \pm 3^\circ$ is maintained over the full UWB frequency range. The oscillator is switched off between pulses for a low average power consumption of less than 13 mW at 3 GHz and 18 mW at 10 GHz with a 250 MHz clock frequency. This corresponds to an energy consumption per pulse of 13 pJ at 3 GHz and 18 pJ at 10 GHz. Meanwhile, the measured output peak-to-peak voltage amplitude varies from 300 mV at 3 GHz to 200 mV at 10 GHz, yielding a competitive energy efficiency. The fabricated IC occupies a die area of 0.85 mm^2 including bonding pads and decoupling capacitors, and the active circuit area is only 0.05 mm^2.

Lastly, a novel fast switching noise cancelling low noise amplifier (LNA) was demonstrated using 0.13 μm CMOS for pulsed 3.110.6 GHz UWB applications. A new noise cancelling topology is employed with series inductive peaking and inductive degeneration to achieve a sub-4dB flat noise figure (NF) and a good impedance match for frequencies up to 10 GHz. A second amplification stage is added (AC coupled) to increase the gain to more than 16.5 dB and provide a good output impedance match from 3 GHz to 10 GHz. Fast on and off power switching is achieved by bypassing the large DC bias resistors that lead to long charging time constants. This is performed

by connecting NMOS switches in parallel to the DC bias resistors and activating them only for a short time period after startup (0.8 ns), thereby reducing the equivalent bias resistance momentarily. The output voltage can thus settle within only 1.3 ns from the turn on instant, enabling high switching frequencies of up to 200 MHz. The phase noise and jitter added by the switched LNA were characterized, and the measured output integrated rms jitter is about 750 fs from 10 Hz to 1 MHz, while the input integrated rms jitter is 420 fs. The circuit consumes 18 mW of DC power in the on state. When the circuit is switched on and off with a 50% duty-cycle, the power consumption is less than 10 mW. The fabricated chip occupies a die area of 1 mm^2 including bonding pads, decoupling capacitors and the chip guard ring (plus chamfer regions), while the core circuit area is 0.5 mm^2.

7.2 Future Work

A few enhancements and feature extensions for the proposed pulsed RF circuits can be suggested at this point as future work. Binary and quadrature phase modulation could be directly implemented in the quadrature pulse generator for 22-29 GHz UWB applications, using the same technique proposed in the tunable 3-10 GHz pulsed oscillator. Quadrature phase modulation could be achieved by changing the directions of the two current impulses injected into the quadrature-coupled LC oscillators according to the binary values of two control signals. The direction of each injected current impulse could be flipped by swapping the order in which the two sides of each differential oscillator are switched on. This could be readily performed by using a digital CMOS logic network that includes multiplexers. Furthermore, the nominal oscillation frequency of the quadrature oscillator could be increased from 23.9 GHz

to 25.5 GHz by slightly decreasing the inductance value L in the LC tanks, such that the generated pulse spectrum is centered in the middle of 22-29 GHz frequency band.

A tunable 3-10 GHz quadrature pulse generator could be designed around the quadrature pulsed oscillator. A variable passive attenuator could be added to the output of the pulsed oscillator to shape the amplitude envelope of the pulsed oscillations. A low-power digital baseband pulse generator based on edge combination (using a CMOS NOR or NAND gate) would also be implemented on-chip to create the required control signals for the variable attenuator and form the desired UWB pulse shapes. The delay between the edges should be variable to realize different time durations for the output UWB pulse. Such a pulse generator could generate quadrature UWB pulses with a tunable center frequency and -10 dB bandwidth for multi-band and frequency-hopping applications. Binary and quadrature phase modulation capability would also be directly provided by the integrated pulsed oscillator.

A broadband fast-switching LNA could also be designed for pulsed 22-29 GHz UWB applications. The 3-10 GHz noise-cancelling LNA could be used as a starting point. However the design of a 22-29 GHz amplifier for low noise figure and high gain is expected to be a much more challenging task than the 3-10 GHz counterpart due to the significantly higher frequencies involved. The noise cancelling circuit configuration might not be suitable altogether for the 22-29 GHz frequency range and an investigation of other broadband LNA topologies would be worthwhile in this case.

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