Design of a reflected power canceller for a UHF FMCW radar

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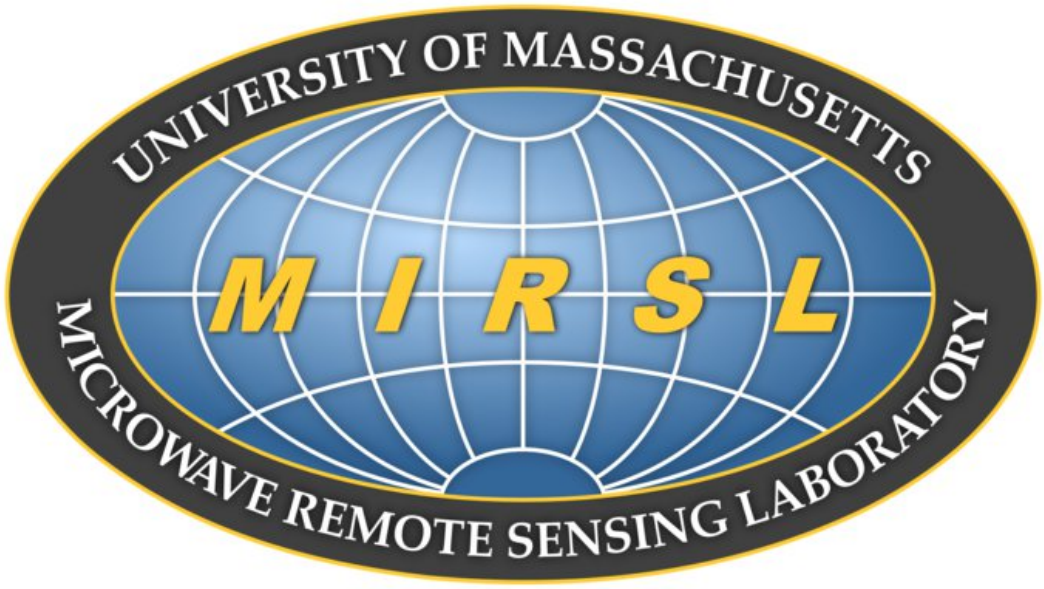
Collaborators



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Summary

Frequency Modulated Continuous Wave radars suffer from an undesirable effect called transmitter leakage. The power leak between transmitter and receiver due to the lack isolation impairs reception performance. The leak, which is orders of magnitude stronger than the desired target echoes, drives the receptor into saturation due to its non-linear characteristics. Since the echoes and leakage are extremely close in frequency it is impossible to use filters to get rid of this problem. Traditionally, the way to increase the isolation has been to use separate antennas to transmission and reception. However, this method presents some drawbacks, e.g. an increase of bulkiness and price. A more elaborate approach is cancelling (subtracting) the leakage before it reaches the receiver. The cancellation system takes advantage of the fact that the leakage and the transmitted signal are of the same form. Subtracting the leakage effectively requires a degree of precision rarely achieved by manual adjustment. This work presents detailed description of a design operating at UHF that uses feedback as a way to achieve a high degree of leakage cancellation. The design validity is demonstrated in a series of tests that quantify the degree of leakage cancellation and assess how different targets are affected by the system.

1 Introduction

Almost all developments in radar technology since its beginnings to the present have been focused on pulsed radars. The main reason for this is the better suitability of these ones to long range and military applications rather than continuous wave radars. Through the last years, however, Frequency-Modulated Continuous-Wave (FMCW) radars have gained interest for these main reasons: the first is that its waveform is highly compatible with solid state electronics and hence, they are significantly easier to build and simpler than pulsed radars. Since fewer components than in other kind of radars are involved, this one offers higher levels of reliability. Second, they have a low probability of intercept, i.e. they are difficult to detect by other devices [1] [2]. Third, FMCW radars provide a much better resolution than pulsed for short ranges, although its performance degrades for long distances, where pulsed radars are superior.

FMCW radars, have been used in limited applications where short ranges are involved, such as airplane altimeters and range detectors used in the automotive and naval industry. They have also been used for meteorological purposes. In fact, one of its first uses was related to ionospheric research [3]. The use of FMCW radars for meteorological purposes has intensified due to advances in solid-state electronics. One close example is the S-band wind profiler designed at MIRSL (University of Massachusetts Amherst) [4].

Of course, FMCW radars do not escape from practical issues. The most common and problematic being what is called transmitter leakage, where the strongest signal at receiver is the power that leaks from transmitter to receiver due to limited isolation between both. The leakage signal degrades reception performance significantly, sometimes to an unacceptable extent. It is worth to note that the leak power is several orders of magnitude stronger than the useful signal, typically in the order of picowatts or less.

Some approaches have been used to mitigate the leakage problem. The most straightforward is using separate antennas for transmission and reception, achieving an isolation usually exceeding 60dB for modest antenna separation. This approach improves the isolation in a great extent but results in a more expensive and bulkier system, which can be excluded from certain applications where mobility is an important factor. Another approach is to use a reflected power canceller (RPC), i.e. a device that eliminates the leakage signal by adding to it a signal in antiphase and equal in amplitude before the first reception stage, usually a low noise amplifier (LNA). This approach is harder to take to practice and usually achieves less cancellation than the former, but if carefully designed it can meet the

requirements for good receiver performance and eliminate the need for multiple antennas. Both approaches can be used simultaneously if any of them used alone does not met the isolation requirements.

2 Objectives

The main objective of this work is to design, fabricate and test a reflected power canceller that exceeds the performance achieved by the first approach used in a UHF wind-profiler present at MIRSL. The design should be ready to be mounted within the wind profiler. Future projects could take this work as an aid for designing RPCs for other uses.

3 Problem definition and context

As stated in the introduction, limited isolation between receiver and transmitter can threaten the performance of reception of a continuous-wave radar significantly. Note that the leakage problem does not affect pulsed radars since they use transmission-reception gating, that is, transmission and reception are not simultaneous. However, in a FMCW radar the problem is inherent since transmission and reception are simultaneous by definition.

There are two main factors that impair the performance of the receiver when strong leakage is present:

1. The leakage noise sidebands can degrade the signal to noise ratio to unacceptable levels, impairing the quality of reception and thus, lowering the minimum detectable signal.

2. A strong signal can desensitize the receiver due to its non-linear nature.

There are various approaches when designing a RPC. Previous implementations include systems with and without feedback, completely analog an partially digital ones. Systems without feedback are usually inferior since they have to be manually adjusted and are very sensitive to component parameter variations due to a variety of factors including temperature. In contrast, closed loop systems are much less sensitive to component variations and keep a better track of the leakage signal [1]. Of course, closed loop systems are more complex. A closed loop canceller can rely completely on analog components or can include a digital signal

[1]The leakage signal depends on the variation of isolation through frequency (See Section 3.2)

processing stage within the loop. Using signal processing adds an extra degree of flexibility, but its implementation is difficult, and a very careful design has to be made. Including a signal processor inherently adds a delay in the loop, limiting the performance of the system. Hence, the algorithms and digital hardware involved must be as efficient as possible to minimize this delay. Analog closed-loop implementations are less flexible, although they avoid the delay problem of digital ones.

The motivation of this work comes from a previous work done at MIRSL. This work focused in building a UHF wind profiler used to retrieve the wind speeds present at the atmospheric boundary layer (ABL), the lowest atmosphere layer. Note that a pulsed radar would not be suitable for this application since the short ranges involved. FMCW radars in the other hand, are a valuable tool in this case due to its excellent resolution at short ranges. The poor performance achieved by its RPC limited the linear operation of the receiving stage, hence lowering its performance.

3.1 FMCW radar basics

FMCW radars, as the acronym states, transmit a FM continuous wave to illuminate targets. The most common waveform is a linear chirp, i.e. a wave whose instantaneous frequency increases linearly. Since the frequency of a linear chirp is described as $f = f_0 + \alpha t$, and the phase in radians is $2\pi \int f\, dt = 2\pi(f_0 t + (\frac{1}{2})\alpha t^2)$. The transmitting signal, a linear chirp, is described by the following expression:

$$a(t) = a_0 \cos[2\pi(f_0 t + (\frac{1}{2})\alpha t^2)] \tag{1}$$

Where f_0 is the initial frequency of the chirp and α is called the chirp rate. The received signal is an attenuated and delayed replica of the transmitted by an amount of τ seconds.

$$b(t) = b_0 \cos[2\pi(f_0(t-\tau) + (\frac{1}{2})\alpha(t-\tau)^2)] \tag{2}$$

The two signals are multiplied and low pass filtered, resulting in what is called intermediate frequency (IF) or also baseband signal in this particular case. From now on, both names will be used. The IF signal has the following form:

$$c(t) = c_0 \cos[2\pi(f_0\tau + \alpha t\tau + (\frac{1}{2})\alpha\tau^2)] \tag{3}$$

Note that the IF signal is a simple sinusoid with a frequency $\alpha\tau$ and phase delay terms. The frequency of this signal is called beat frequency, and is completely

determined by the time delay and the chirp rate. Hence, this signal contains all the information needed to determine the range of a target. Since τ equals the round trip time, the following expression relating the range and beat frequency is found:

$$B = \alpha \frac{2r}{c} \rightarrow r = \frac{cB}{2\alpha} \tag{4}$$

Where r is the target range, c the speed of light and B the beat frequency.

A visual representation of the process is given in Figure 1. TX is the transmitted signal and RX is the received one.

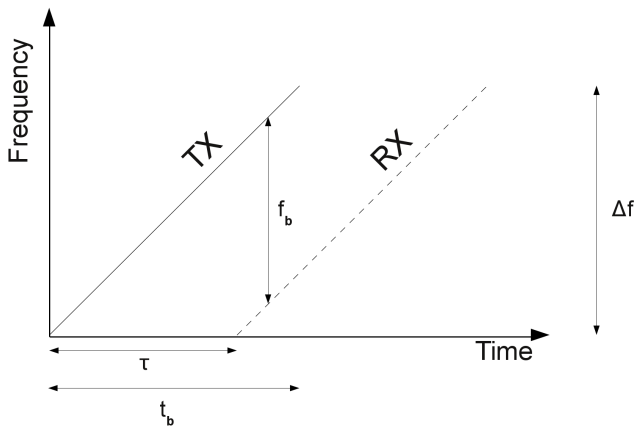


Figure 1: Frequency vs Time. Note that the round trip time is exaggerated to make the figure clear.

FMCW radars are also capable of measuring the target speed and range simultaneously. A derivation can be found at [2]. Note also that there is no theoretical limit in range measurement.

Generally, a single antenna FMCW radar takes the form shown in Figure 2. A transmitter stage delivers the chirped signal to the antenna. A ferrite circulator is included so that the signal received is forwarded only to the LNA. After the signal has been amplified it is mixed with the transmitter signal, also called local oscillator (LO) signal. The resulting product is read and passed to a signal processing stage that extracts target information. A bandpass filter can also be used right after the LNA to improve the SNR. If two antennas are used the ferrite circulator is not needed.

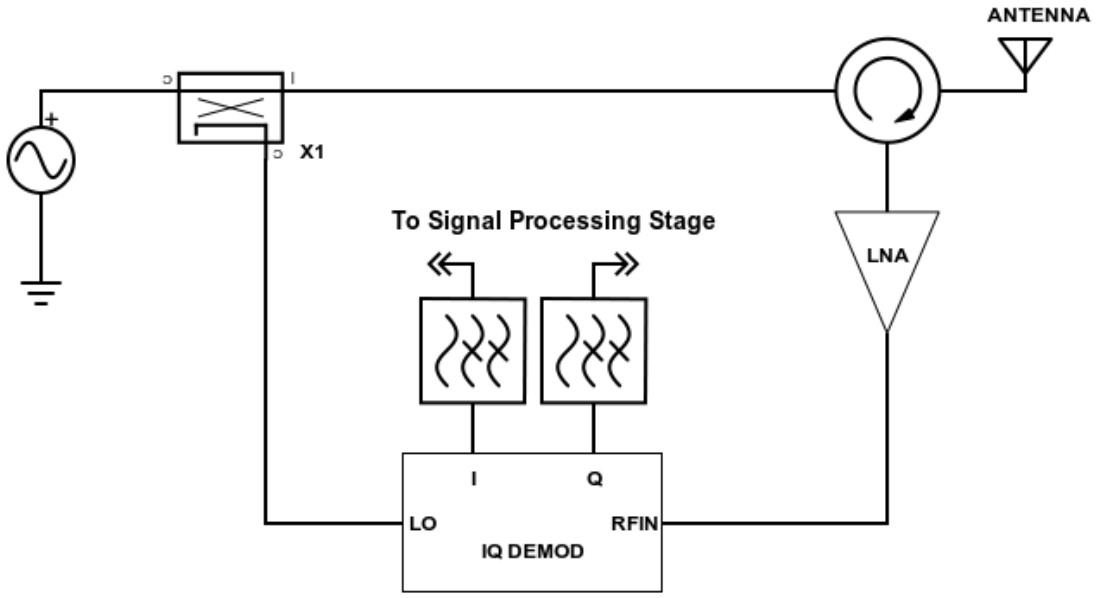


Figure 2: General structure of a single-antenna FMCW radar

3.2 The leakage origin

The main origin of the poor isolation between transmitter and receiver in a single antenna radar is the imperfect matching between the transmission line characteristic impedance Z_0 and the antenna equivalent impedance Z_A. This mismatch causes a reflection at the antenna ports of the transmitter signal that is directly forwarded to the receiver stage by the circulator. The power ratio between the transmitting signal and the reflected one is defined as the return loss (RL), which is defined as follows:

$$RL(dB) = 10\log_{10}(\frac{P_i}{P_r}) = 20\log_{10}(\frac{Z_0 + Z_A}{Z_0 - Z_A}) \tag{5}$$

Where P_i and P_r are the incident and reflected power, respectively. Limited isolation between ports of the circulator is another source of leakage. However, in practical systems this signal is orders of magnitude smaller than the leakage caused by antenna mismatch, so it can be often ignored.

In a multiple antenna radar, such as the UHF wind profiler in MIRSL, the leakage origin is caused by the free space leakage. An interesting reference on this issue [5].

Another source of leakage is clutter, which in this case is mainly caused by close air back-scattering or a variety of close unwanted targets.

It is very important to note that the leakage signal produces a very low beat frequency at the demodulator. This is because the round trip time in equation 3 is only due to time delays within the system itself.[2] Being able to distinguish leakage by its low frequency is what allows the system to treat it differently from the rest of the signals.

3.3 Effects of leakage

An important effect of the leakage signal on the receiver amplification stage is gain desensitization. A practical amplifier has input/output nonlinear characteristics that can be described with the following expression:

$$v_0 = a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 ... \tag{6}$$

Higher order terms are not shown since they have a negligible effect in practical amplifiers. Consider two sinusoidal inputs with amplitudes a and b, being $a \ll b$. a is considered the useful signal and b the leakage. Then $v_i = (a+b)cos(\omega)$ [3] Substituting into equation 6, and retaining only the $cos(\omega)$ terms:

$$v_o = cos(\omega)\left[a_1(a+b) + \frac{3}{4}(a+b)^3 a_3\right] \tag{7}$$

If the amplifier were perfectly linear only the a_1 (blue) term would appear. Non-linearity adds the a_3 (red) term. Since a_3 is negative in a real amplifier, the term b (positive) from the leakage tends to reduce the output signal amplitude associated with $cos(\omega)$

4 Specifications and requirements

Part of the specifications are taken from the previous UHF wind profiler designed at MIRSL. The transmitter power is reduced to make testing easier.

[2] In this case one cannot talk strictly about a round trip time, since leakage is not associated with a target. Although, it is valid to assign to it the delay between the transmitter signal and the leakage.

[3] In a FMCW radar both signals are chirped have a relative delay. However, a valid simpler analysis to illustrate the concept is done considering zero delay and simple sinusoids.

Center Frequency	915MHz
Transmit Power	3dBm
Sweep Time	8.333 ms
Pulse Repetition Frequency (PRF)	100 Hz
Sweep Bandwidth	25 MHz
Target Range	100-1000 m

Note that the beat frequencies associated with targets 100 and 1000 meters away are 2kHz and 20kHz respectively (See Equation 4).

As an initial requirement, the system should achieve a minimum leakage cancellation of 20dB. Another requirement is that the system should cancel the leakage but should not modify or modify in a known way echoes associated with targets.

5 Proposed solution

5.1 Approach justification

The system to be designed will feature a fully analog closed loop. The reasons that justify the choice are the following:

1. Systems without feedback are discarded because of its poor robustness, performance and set-up difficulty.

2. A closed loop system including digital processors presents issues that are difficult to overcome or palliate such as the delay introduced by signal processing and AD conversion and the requirement for high accuracy quantization.

3. A digital approach has already been tried in a previous work at MIRSL with poor results.

4. The digital approach design complexity is not adequate due to time limitations.

5.2 System description, analysis and design

The system is shown in Figure 3. Ideally, the main objective is to eliminate all the leakage by adding a signal of the same amplitude in antiphase to it. To do so, a portion of the transmitted signal is fed to the canceling path (the path from coupler X2 to X3) through a coupler. Without any manipulation this signal may

not arrive at the second coupler (that acts as a weighted adder) with the correct amplitude and phase and thus not achieving the goal of maximum cancellation, or in the worst case producing a constructive addition. The closed loop's job is to actively manipulate this signal amplitude and phase adaptively to achieve this goal.

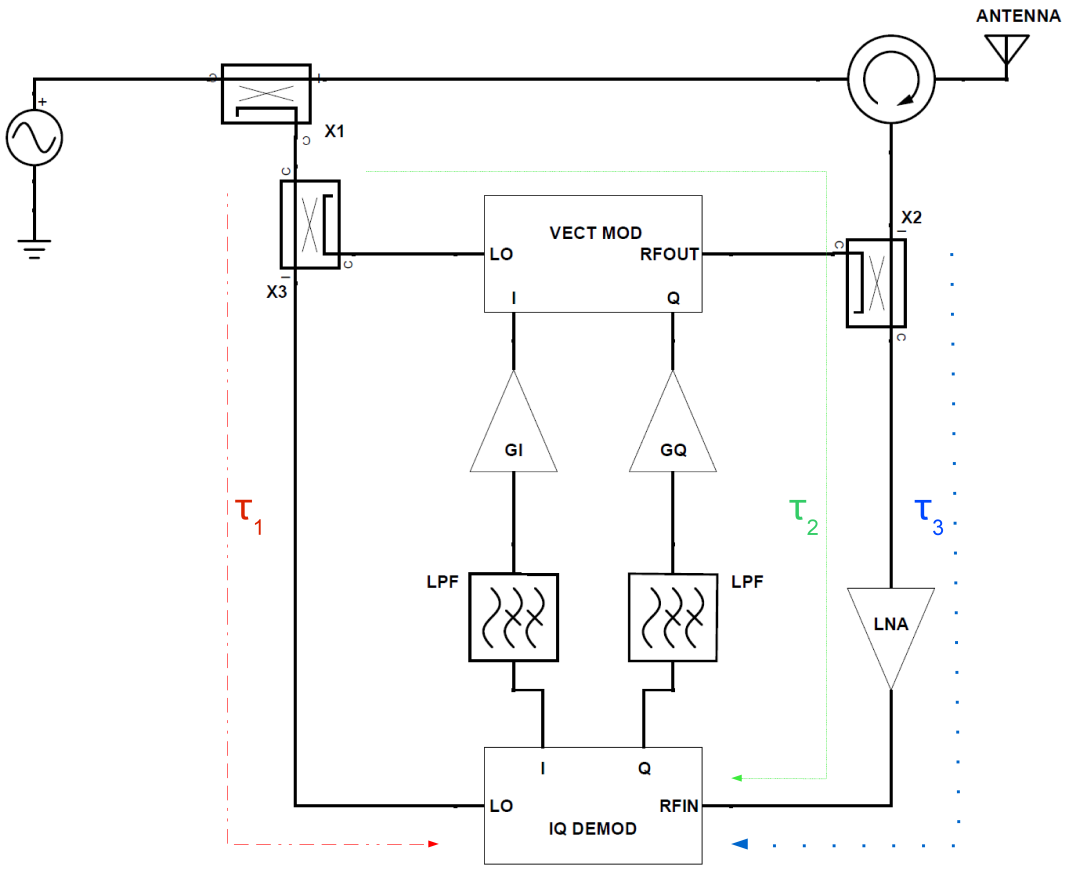


Figure 3: Possible structure of a Reflected Power Canceller

The better way to understand and analyze as RPC is thinking in terms of IQ components. For simplicity, from now on the IQ components will be referenced to the signal at the input of the vector modulator. Consider the signal present in the RF path (the one from the circulator to the IQ demodulator): it has the components Q_{in} and I_{in}. In the same way the signal present in the cancelling path can also be described by the components Q_{can} and I_{can}. Equivalently, the goal of the RPC is to fed the adder a cancelling signal with IQ components of the same

amplitude and opposite sign with respect to the components of the leakage. Figure 4 illustrates the concept.

Clarification: IQ components are actually defined in a punctual location, e.g. the IQ demodulator RF input in the RF path case, and referenced to a punctual location, the input of the vector modulator in this case. However, one can visualize these IQ components extended through a path, since the variation over time can be translated to a distance traveled by the RF signals. Visualizing the IQ components this way helps understanding this system. Also, since the IQ components have a very low wavelength compared to the dimensions of the system, they can be considered constant at any point of a path at a given instant.

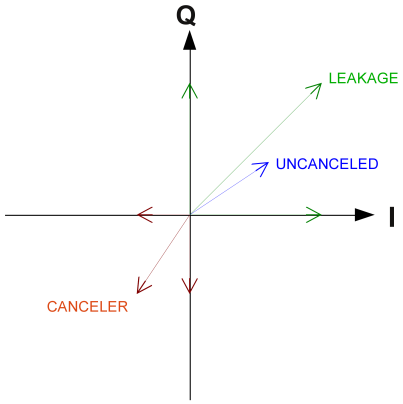


Figure 4: Vectorial representation of cancellation

Before a mathematical analysis an intuitive view of the working principle is given using the IQ approach. Consider a sinusoidal leakage and a zero canceling signal. The signal after the adder will be called the error. This signal is fed into a IQ demodulator that extracts its I and Q components. The components are passed through an amplifying stage (ignore the filters for now) and fed to a vector modulator which outputs a sinusoidal signal with the I and Q components present at its baseband input. Note also that negative feedback is required, so a 180 degree shift must take place somewhere in the feedback loop. Since the output signal of the vector modulator has both I and Q components of opposite sign with respect to the leakage, the error signal will be reduced. The process is continuous, so the error signal is eventually reduced to a large extent.[4].

A very important requirement is that the RPC should cancel the leakage but

[4]The error signal is not zero due to practical limitations

leave the useful signal unaltered or altered in a known way. As will be seen later in section 5.2.3, this goal can be accomplished using filters between the IQ demodulator and the vector modulator.

5.2.1 Equivalent baseband model

A good way to model the system is applying classical feedback theory. However, at first glance the theory does not seem to be easily applicable. Thus, a suitable model has to be derived.

A model easy to work with can be obtained if only IQ information is considered. In other words, all RF signals can be represented only with its IQ components. This will lead to a model in which only IQ information is present. This is justified since all the components present in the system have its baseband equivalent i.e. a model that represents how IQ components are modified by each device.

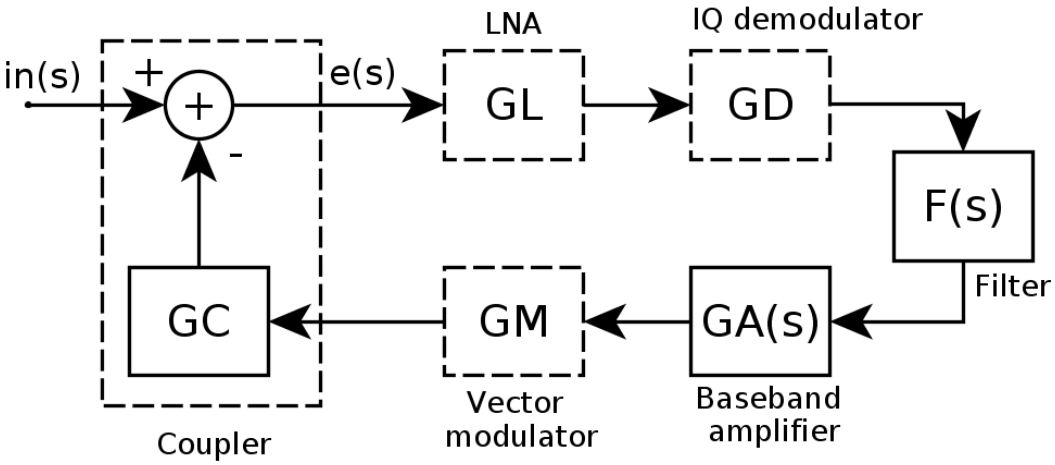


Figure 5: Equivalent baseband model

Figure 5 shows the baseband model. Each dashed box contains blocks that represent a baseband equivalent of a single device.

Justification of baseband equivalents

It is assumed that all components behave linearly within the range of operation. The most straightforward component to model is the LNA: it is trivial that IQ components are multiplied by the gain of the amplifier. The IQ demodulator can also be represented by its conversion gain. Conversion gain is made constant in

most IQ demodulators for its frequency operation range. Finally, the coupler acts as a weighted adder where the signal coming from the coupled port is attenuated and added to the signal in the input port.

The vector modulator can also be represented as a simple gain, but this conversion gain is not as straightforward to know as the demodulator case. From the vector modulator datasheet it can be seen that the voltage conversion gain [5] is flat over a wide range of frequencies and LO input power. However, when examining the IQ demodulator datasheet one can see that the output signal is dependent of both baseband input voltage (the modulating signal) and LO input power (the RF signal to be modulated) [6]. The gain to be known is the voltage gain from baseband input to RF output considering only the I or Q channel. From the datasheet the LO signal component is linearly attenuated from 32dB to 2dB when the baseband input is driven with 500mV and $\pm$ 1V respectively [7]. With this information the following relation can be derived:

$$V_{out} \simeq V_{LO}\frac{0.794}{0.5}V_{baseband} = \sqrt{P_{LO}R_0}\frac{0.794}{0.5}V_{baseband} \tag{8}$$

Where $R_0 = 50\Omega$ is the characteristic impedance present at LO input. Looking at Equation 5.2.1 it can be seen that the gain GM (see Figure 5) can be determined with the LO input power. The validity of his model has been proven experimentally.

5.2.2 Timing considerations

The demodulator aim is to output the I and Q components of the signal present at the coupler so that the system can manipulate them (eliminate or modify). However, due to the fact that UHF signals have a wavelength comparable with the size of the system, some considerations have to be made.

Consider Figure 3. τ_1 represents the time that takes for a signal to travel from the generator to demodulator LO input. Similarly, τ_2 is the time from the signal generator to demodulator RF input via vector modulator.

[5] Voltage conversion gain is defined as the ratio of RF port input voltage and baseband output voltage

[6] This is because a vector modulator uses variable attenuators from LO to RF output controlled by the baseband signals

[7] The attenuation depends on the difference between the input voltage and 500mV. If the difference is negative the input signal is not only attenuated but also shifted 180^o.

The ideal case of $\tau_1 = \tau_2 = \tau$ is analyzed. The signals present at the LO and RF inputs and the IQ outputs are of the form [8]

$$y_{LO}(t) = cos[2\pi(f_0(t-\tau + (\frac{1}{2})\alpha(t-\tau)^2)] \tag{9}$$

$$y_{RF}(t) = cos[2\pi(f_0(t-\tau) + (\frac{1}{2})\alpha(t-\tau)^2) + \phi(t)] \tag{10}$$

$$I = cos(\phi(t));\ Q = sin(\phi(t)) \tag{11}$$

Note that $\phi(t)$ is exactly the phase term of the signal at the coupler output referenced to the LO demodulator input signal and delayed by τ_3 seconds. If the minimum period present in $\phi(t)$ is much smaller than the delay τ_3 this last can be ignored and assume that the demodulators output the IQ components present at the coupler without delay. In almost any practical system this is true. Note that this explanation is strongly related with the clarification in Section 5.2.1.

Consider now $\tau_1 \neq \tau_2$. In this case the IQ components fed to the vector modulator are not consistent with the components detected by the demodulator. However, and far from obvious, this is not as limiting as it seems because the system is stable as long as the phase difference between both signals is less than 90^o [6] [7]. Consider a delay mismatch $\Delta\tau = |\tau_1 - \tau_2|$. The phase difference between both is dependent on frequency:

$$\Delta\phi \simeq 2\pi f \Delta\tau \tag{12}$$

The approximately equal symbol is due to the fact that in this case the signals are chirps and not pure sinusoids. However, the error made by this approximation is extremely small.

A corollary is that a RPC is able to cancel the leakage up to a maximum frequency depending on the mismatch:

$$\frac{\pi}{2} = 2\pi(f_{max})\Delta\tau \Rightarrow f_{max} = \frac{1}{4\Delta t} \tag{13}$$

From specifications the RPC should be able to work up to 932.5 MHz (Center frequency + half the chirp bandwidth), so from the above relation the delay mismatch should be less than 268ps, corresponding to a path length mismatch of 8cm (considering the speed of light).

[8] Amplitudes are not taken into account. The only relevant information in this case is angle.

5.2.3 Frequency domain analysis and design

From classical feedback theory, the error transfer function of a system represented in Figure 5 takes the following form:

$$E(s) = \frac{e(s)}{in(s)} = \frac{1}{1 + GL(s)GD(s)F(s)GA(s)GM(s)GC(s)} = \frac{1}{1 + H(s)} \quad (14)$$

Where $H(s)$ is the closed-loop transfer function. Considering the elements present in the loop the ones that are more flexible to work with are the baseband filter and baseband amplifier. RF components tend to be expensive and inflexible, so changing a component's parameter means to replace it. In contrast, low-frequency circuitry can be adjusted easily with few changes and is relatively cheap. With that in mind, the selection of RF components is based on what is already available in the lab (in particular the components used within the wind-profiler). Once RF components are selected the baseband circuitry is designed. A change in RF components can be easily corrected adjusting the baseband ones.

Filtering
Now, the effect of the filter within the loop is explained. Imagine a loop without the filter. Since the filter transfer function is the only one that contains poles and zeros (that is, it produces a non-flat frequency response), the open-loop transfer function is composed only by flat gains over all frequencies [9]. Then, $E(s)$ is constant and attenuates equally all frequencies so the leakage and the useful signal are affected in the same way. The inclusion of filters model the shape of $E(s)$ so that the leakage and useful signal can be treated differently.

The frequency response of $E(s)$ needs to eliminate low frequencies, associated with the leakage, and pass frequencies associated with targets. In other words, $E(s)$ can take the form of a high-pass or band-pass filter.

The simplest way to create a high-pass response for $E(s)$ is to place a single pole in the open loop transfer function, $H(s)$. From control theory, $E(s)$ will have a zero at the exact position of the open loop pole and a pole whose position depends on the DC gain of the open-loop (from now on referred as K) and the position of the zero. Root locus plots are a very useful graphical tool to represent closed loop poles from open-loop poles and zeros as the K varies. [10]

[9] These gains are considered constant for nominal frequencies.

[10] There are a set of rules used to draw root locus plots that can be found in any control theory book. However, they are not presented here.

That said, the open loop transfer function should take the following form:

$$H(s) = \frac{K}{1 + \frac{s}{2\pi f}} \tag{15}$$

In this case, placing a real pole at any frequency in $H(s)$ results in a fixed zero in the same position and a pole of increasing real value as the K increases in $E(s)$. Thus, there are three parameters in the design: K, frequency of the closed-loop zero (or open-loop pole) and frequency of the closed-loop pole. Each one is determined by the other two, so there are two degrees of freedom in the design. The proposed design approach sets the location of the closed-loop pole and K.

K depends on the amount of cancellation required (recall that voltage cancellation is approximated as $\frac{1}{1+K}$), so K should be chosen so that the cancellation ratio is above the requirement. As the minimum amount of cancellation is 20dB, the design aims to cancel way above that value, so aiming at 40dB could be a good option. Then, K = 99.

The frequency of the closed-loop pole is not fully determined from specifications but from practical considerations. At first glance it may seem obvious to place the pole just below the lower beat frequency from the closest target whose distance is stated in the specifications, 2kHz in this case. This choice would result in a mostly flat response within the target frequency range. However, this decision usually leads to a zero (the open-loop pole) at a very low frequency, thus impairing the practical realizability of filters, since it tends to require components out of the usual range of commercial values. A solution can be to place the pole at the other extreme of the target frequency range. This allows to relax electronic component values. However, the frequency response in that range is no longer flat, but a later signal processing stage can correct the distortion if required.

The closed-loop pole frequency is chosen to coincide with the upper extreme of target frequency range, this is, 20kHz. Using $E(s)$, the position of the closed loop zero is determined to be 200Hz analytically. The position can also be determined very easily using a Bode plot drawing the known asymptotes (-40dB towards DC, 0dB towards infinite and a slope of 20dB/dec between zero and pole). $H(s)$ and $E(s)$ are plotted in Figures 6 and 7.

Equalization effect

Having a zero and a pole at the extremes of the target frequency range in $E(s)$ has another benefit from the electronic perspective: it has an equalization effect in receiver power (See Figure 8). In practice, the required power dynamic range

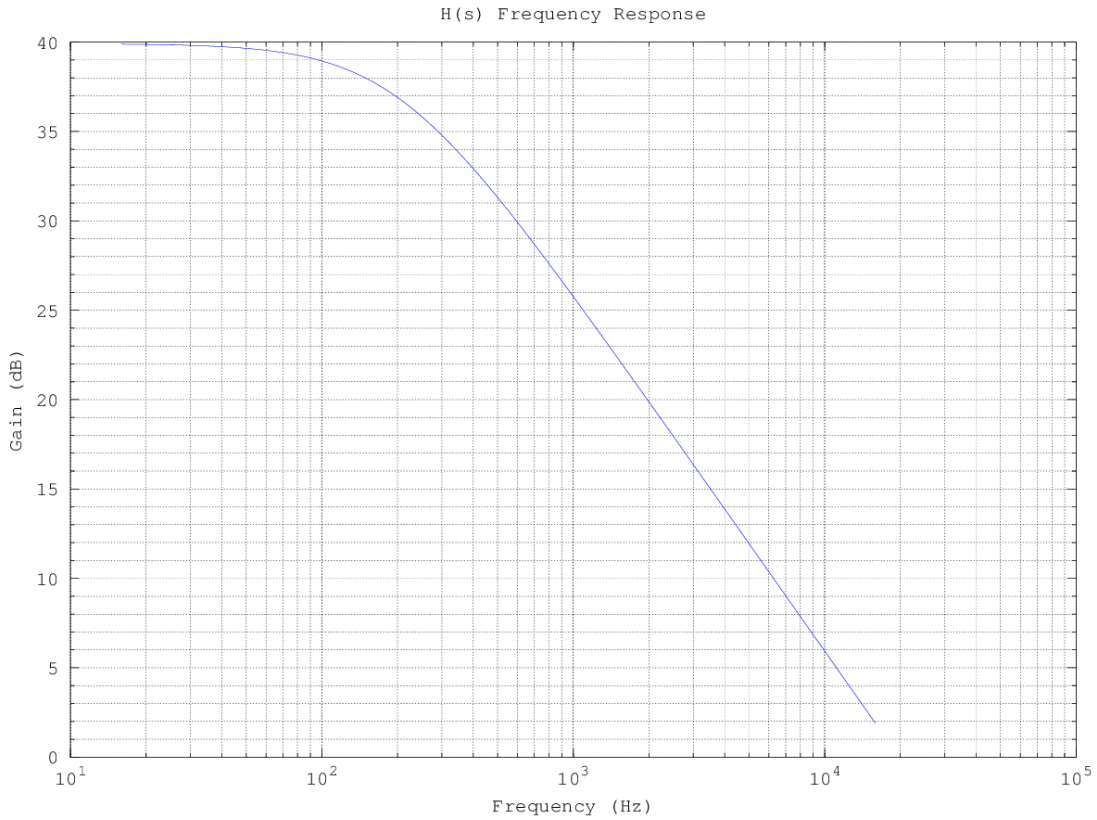


Figure 6: H(s) Frequency Response

of the receiving stage is reduced. A brief mathematical description of this effect is described:

From the radar equation and Equation 4:

$$P_r \propto \frac{1}{R^4} \propto \frac{1}{B^4} \tag{16}$$

$$V_r \propto \frac{1}{R^2} \propto \frac{1}{B^2} \tag{17}$$

Where V_r is the voltage associated with the received power P_r and B the beat frequency. The voltage frequency response can be considered to vary at a rate of 20dB/dec in the range of frequencies associated to useful targets. That is, in linear form:

$$F \propto B \propto R \tag{18}$$

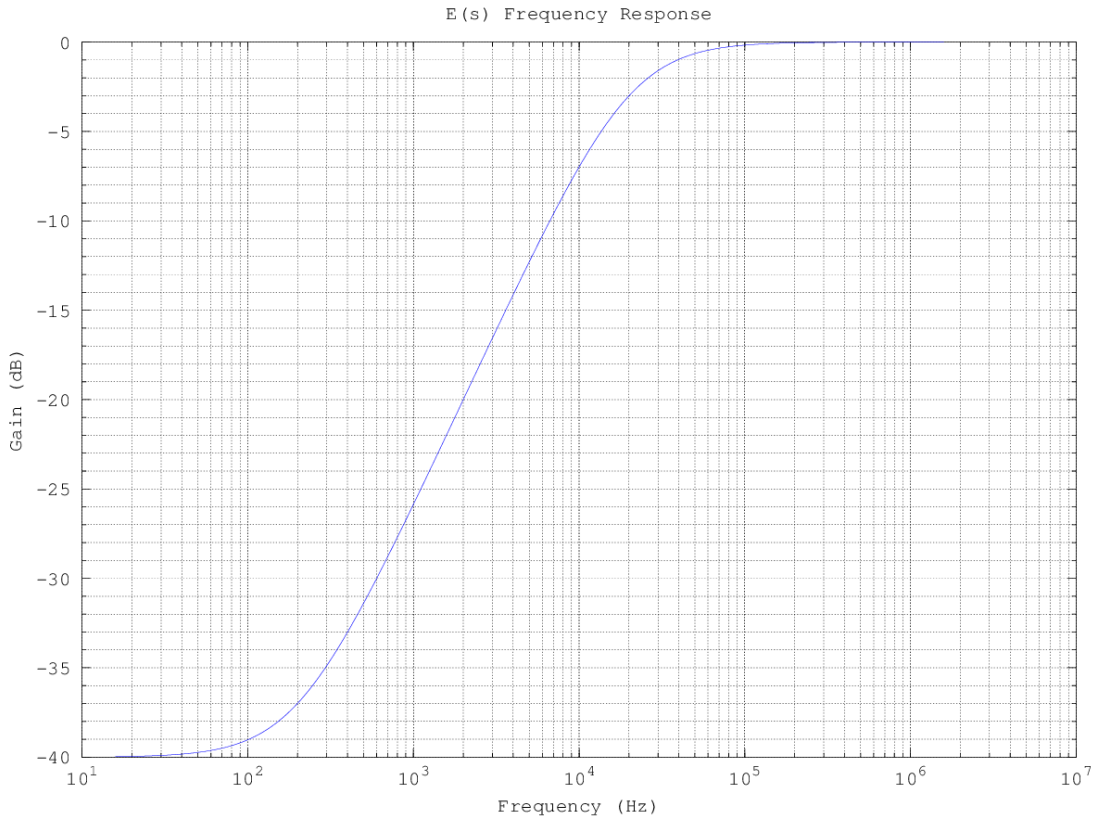


Figure 7: E(s) Frequency Response

Multiplying the voltage frequency response with V_r denotes the equalization effect, flattening the relation between B or R and V_r.

$$V_r' = V_r F \propto \frac{1}{B} \propto \frac{1}{R} \tag{19}$$

Trivially, the effect is the same with power.

Closed-loop gain determination

RF components are chosen taking the wind profiler design as a reference and new components are chosen from different vendor catalogs. Table 1 shows the components used for every block.

Now, each gain in Figure 5 is determined.

- **GL=23dB.** This is the LNA gain.

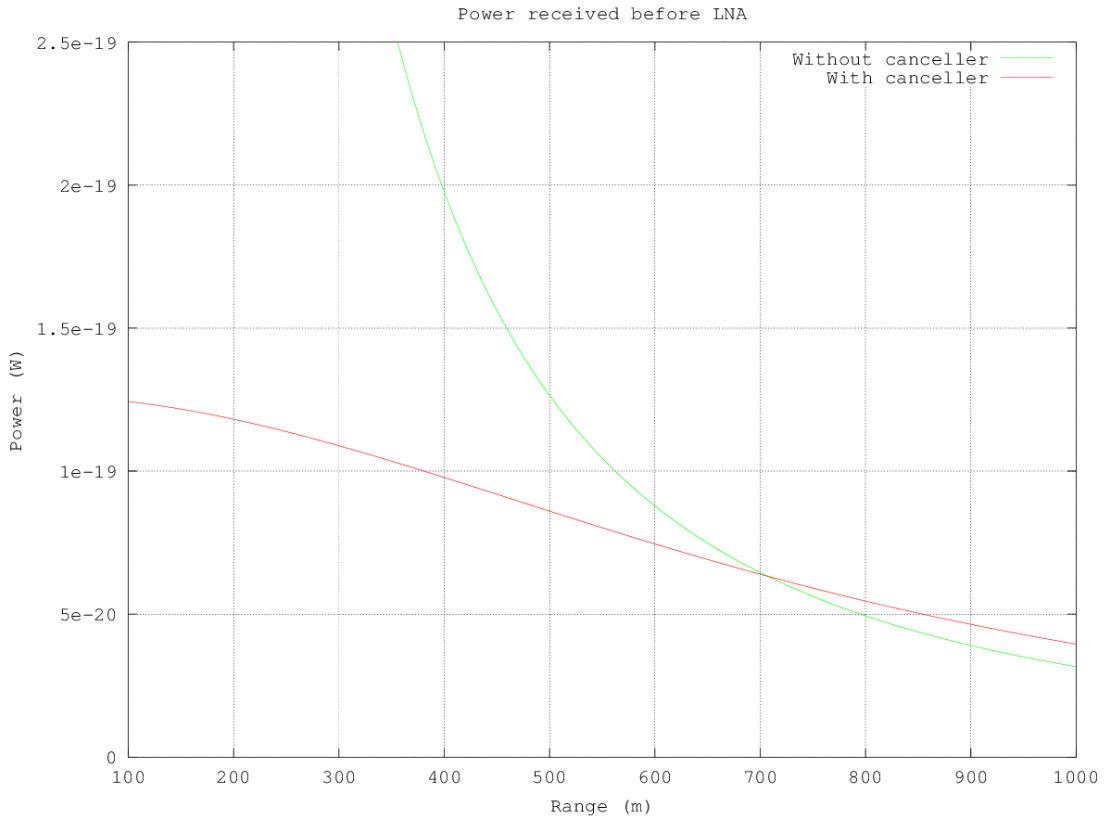


Figure 8: Equalization effect. Power values are taken from [8]

- **GD=23dB.** This is the voltage conversion gain found in the IQ demodulator datasheet[11].
- **GM=-6dB.** From Figure 12 the LO power is 3dBm. GM can be determined using Equation 5.2.1.
- **GC=-20dB** This is the coupling value of the directional coupler.
- **F(s)=0dB at DC**. F(s) represents the baseband filtering block discussed in Section 5.2.3.
- **GA(s)=20dB.** This is the baseband amplification block discussed in 5.2.3. The open-loop DC gain has to be 40dB. GL + GD + F + GM + GC = 1dB, so GA is required to add 20dB.

[11] Although the datasheet indicates a voltage conversion gain of 4dB the measured one is 23dB. The reason is still unknown. A measurement error seems unlikely to be the issue.

Vector Modulator	AD8340 EVAL BOARD
IQ Demodulator*	ADL5382 EVAL BOARD
Directional Couplers	Narda 4242-20
Power Splitter	Minicircuits ZAPD-23-S+
Active Baseband Filter*	LT1994 & Various passive components
LNA	Phoenix PA911C

Table 1: Components used for prototyping. Asterisks denote components that were acquired (not present in the lab before)

Baseband circuitry
The baseband circuitry is the responsible of adding the open loop poles to achieve the desired closed loop frequency response. As stated in section 5.2.3 only one open-loop pole is needed, so the proposed circuits for I and Q channels are designed as shown in Figure 9. The circuit consists of an amplification stage with a fully-differential amplifier and a balanced filtering stage. A single stage would be possible using shunt capacitors with the feedback resistors, but this topology has shown to cause problems in a breadboard probably due to parasitic impedances combined with an active circuit with very low output impedance. Using two stages solves the problem. R2,R3,R4 and R5 set the amplification stage gain while R6,R7 and C28 form a one pole filter. R14 and R15 set the output common mode offset required by the vector modulator. Capacitors at power inputs are used only for decoupling. The frequency response of the stage is shown in Figure 10.

The values of the resistors should be as symetrical as possible since an unsymmetrical fully differential op-amp converts common mode input signal (a bias in this case) into a differential output. Resistors with 1% or 5% tolerance have proven to be a good choice. A detailed reference can be found at [9].

The usage of fully-differential amplifiers has been motivated by the following reasons:

- IQ demodulator and vector modulator use balanced outputs and inputs respectively.
- Differential mode signals have immunity to common-mode noise.
- Differential mode signals have less even order harmonic distortion.

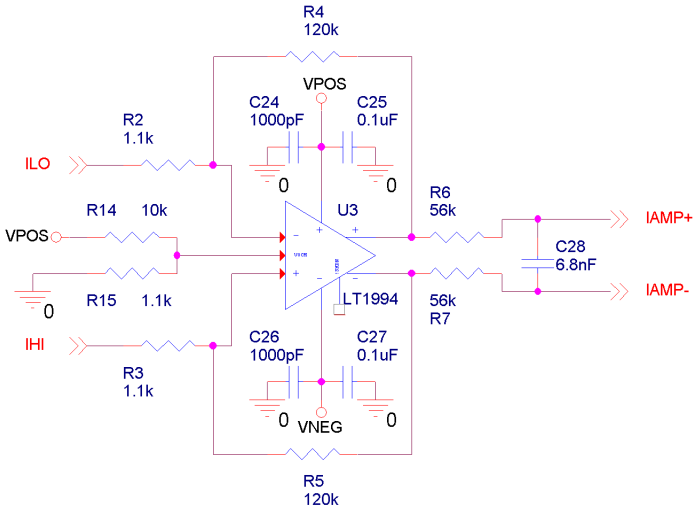


Figure 9: Baseband amplification and filtering circuit

5.3 Integration

After a successful testing of the prototype, part of it is integrated in a single PCB [12]. This integration saves a considerable amount of space, makes the mounting into the radar much easier and prevents connection errors. An "accidental" fact is that the RPC serves as a demodulator, amplifying and filtering stage, so part of the blocks used in a FMCW radar without the canceller for the same purposes may be removed.

For the sake of performance and space optimization all electronic parts with the exception of power connectors are chosen to be SMT.

The board provides three inputs and five outputs:

- LO input. Used as reference for the IQ demodulator. The signal should be a sample of the transmitting signal of a power between -6dBm and 6dBm.
- SAMPLE input. This is the signal whose IQ components are modified to add in antiphase with the leakage. It should be a sample of the transmitted signal with a power of 3dBm [13].

[12] The prototype testing is not shown in this document because results and testing methodology are identical as the testing done with the integrated system. For results see Section 5.4

[13] As stated earlier, note that the cancellation ratio depends on the power of this signal. It could be modified taking into account the effect on the performance.

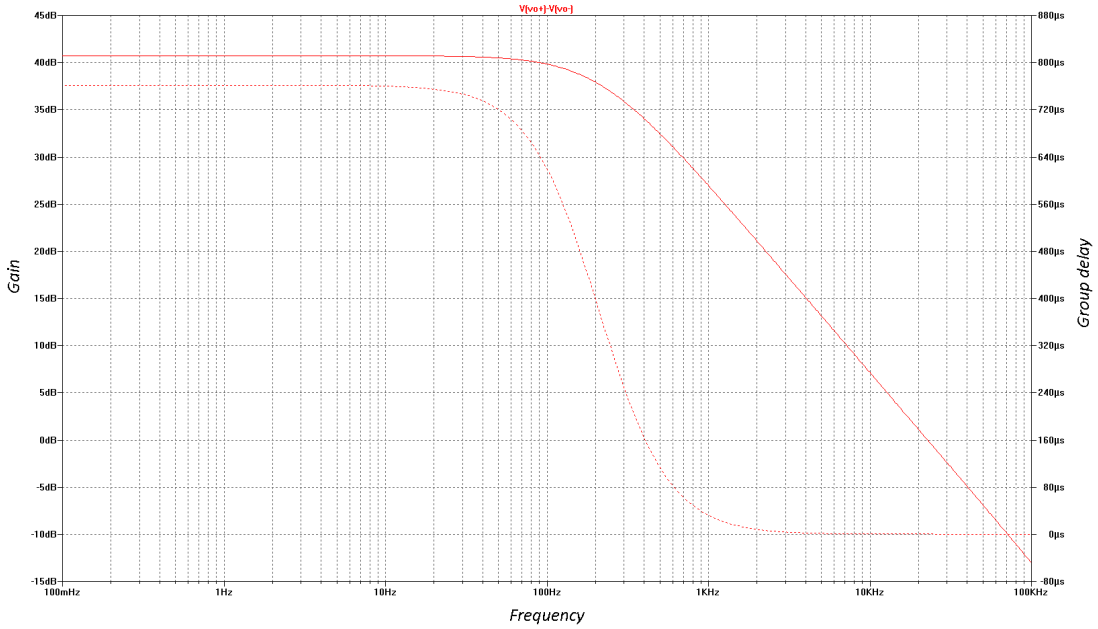


Figure 10: Frequency response of the baseband amplification and filtering circuit. The discontinuous line represents the group delay and the continuous one the gain.

- RF input. This is the received signal including the leakage to be fed to the demodulator.
- CANCELLER output. This is the signal that cancels the leakage.
- QHI, IHI outputs. These are the single-ended signals corresponding to the amplified and filtered Q an I components at the outputs of the IQ demodulator. Care should be taken when using single-ended outputs because balanced mode benefits such as common mode noise suppression are not present here. Also, the common mode biasing of 500mV should be taken into account. Single ended mode is to be used in the wind profiler due to the topology of the following receiver blocks.

The board consists on a rectangle of 3.13"x2" and it has four cooper layers: two routing or signal layers (top and bottom) a ground plane (second layer from top) and a power layer with 5V and -5V (third layer from top). All cooper layers have a thickness of 1oz/ft^2 (1.37 mils or 34.79 microns). Inner layers are separated by a dielectric core of FR-370HR of 40 mils. Outer layers are separated from inner ones by a dielectric layer of FR-370HR of 8 mils. The finished board thickness is 62 mils.

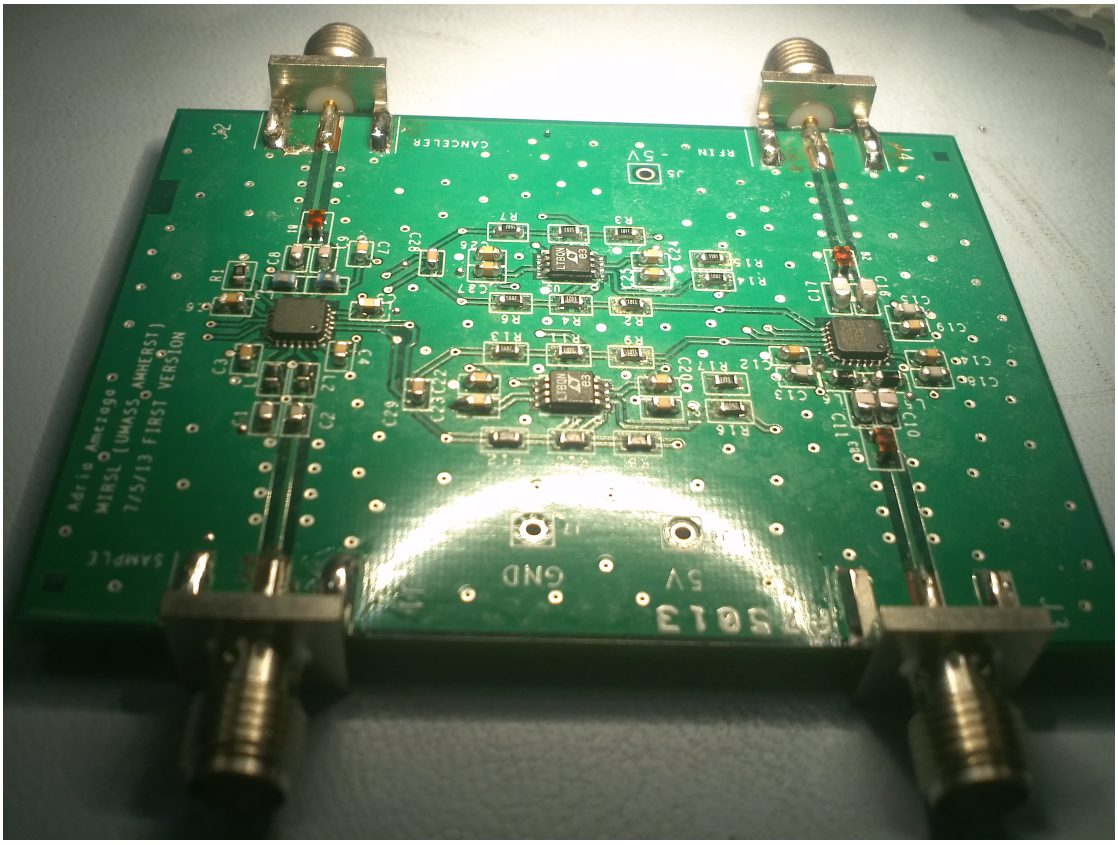


Figure 11: Photo of the first revision of the board. The second revision (the one present in the appendices although not manufactured) adds minor corrections and SMA connectors to sense the baseband signals. It also adds two switches to invert the feedback sign (in case the LO and RF path electric length differ more than 90 degrees and make the system unstable)

Due to the high cost of automatic assembling service per board for a low number of units all the components were soldered manually. All parts were soldered with a fine soldering iron except the vector modulator and the IQ demodulator, that are only available in QFN packaging. Convection soldering was used instead for QFN packages. Since no restrictions in lead presence apply, an eutectic alloy [14] (63/37 Tin/Lead) was used to reduce the chance of damage and ease the soldering work.

The circuits used for the IQ demodulator and vector modulator are based on

[14] An eutectic alloy one the lowest melting temperature within tin alloys. Also, it has no plastic melting phase, which reduces the chance of bad soldering.

the manufacturer recommendations. (See Appendix C).

The schematics and the PCB artwork generated with Cadence Allegro are shown in Appendix A.

Notes on passive electronic component selection for RF:

- RF inductors and capacitors: care must be taken when selecting these components. Self resonances can impair the operation of the circuit. These resonances are found around 1Ghz in a significant number of parts. In general, the self resonant frequencies (SRF) of capacitors and inductors should not lay close to the operation frequency. There are special cases however, e.g. when inductors are used only for biasing purposes as they tend to look like an open circuit close to the SRF.

- Each balun in optimized for its operation in a determined frequency range. It is important to chose a balun that behaves properly at the frequencies the RPC will operate. Phase unbalance is a parameter to consider. In this case a model with a very good phase unbalance at 915Mhz has been chosen.

5.4 Testing and results

The testing methodology is the same for the prototype and the integrated system. The results presented are extracted from the integrated system. The results from the prototype (not shown in the document) are extremely similar to the ones shown here.

The system is tested in two ways:

- First method: Simulating a flat return loss of an antenna with a directional coupler and an attenuator, as seen in Figure 12.

- Second method: Emulating targets at different distances using a fixed BAW delay line [15] in place of the attenuator and a varying chirp rate and sweep time.

[15] BAW refers to Bulk Acoustic Wave. A BAW delay line transduces an electric signal to a BAW which travels through a cylindrical rod of a specific material (usually sapphire or quartz) at the speed of sound, which is transduced back to an electric signal at the other end of the line. These devices suffer an undesired effect called multiple travel caused by internal reflections. The practical implications are that the output presents multiple copies of the input delayed by t, 3t, 5t, 7t... with decreasing power. These importance of these delays depends on the case. can be used right after the attenuator.

- Third method: Field test. Using an antenna to illuminate an environment and another one to receive reflected power.

In the testing methods described above, baseband signals and/or a power measurament right after or before the LNA are measured opening and closing the loop in order to assess the behavior of the system.

The system used to test the leakage cancellation performance of this RPC topology is shown in Figure 12. When assessing the system reaction to different targets, the attenuator is replaced by a BAW delay line or the topology is modified to accommodate two antennas.

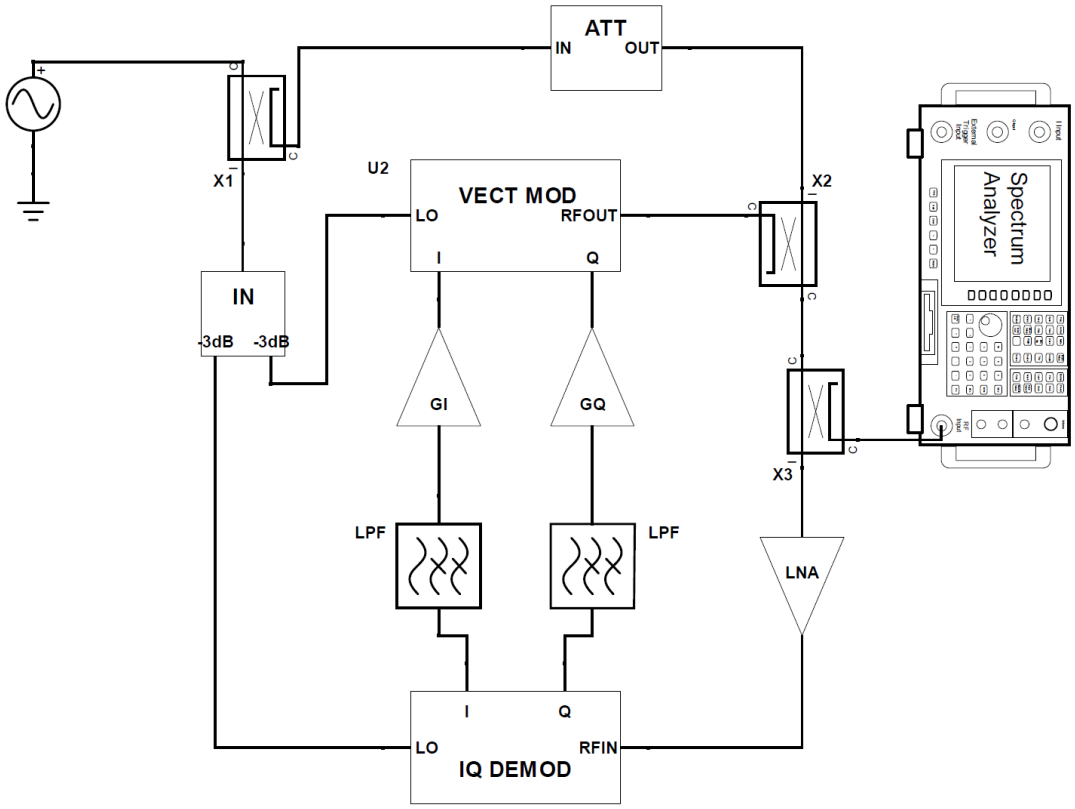


Figure 12: System used for leakage cancellation testing

Note that the coupler X1 is connected differently from Figure 3 and coupler X3 is converted into a power splitter. The topology can vary depending on the power needed at IQ demodulator and vector modulator LO inputs and the power

transmitted. In this case aproximately half the power of the transmitter is fed to the LO inputs of the former devices. Comparing Figure 3 and Figure 12 it can be seen that the impedance mismatch described in Section 3.2 is emulated by the coupling of X1 and an attenuation. To emulate targets at different distances a BAW delay line is used .

First method

Figure 13 shows that the leakage cancellation is almost 40dB over all the useful bandwidth. Consistent with the design. An interesting effect is the peak present at the lowest frequency of the chirp. The most plausible cause is a strong peak present in the temporal response of the error transfer function due to the filtering stage transient response.

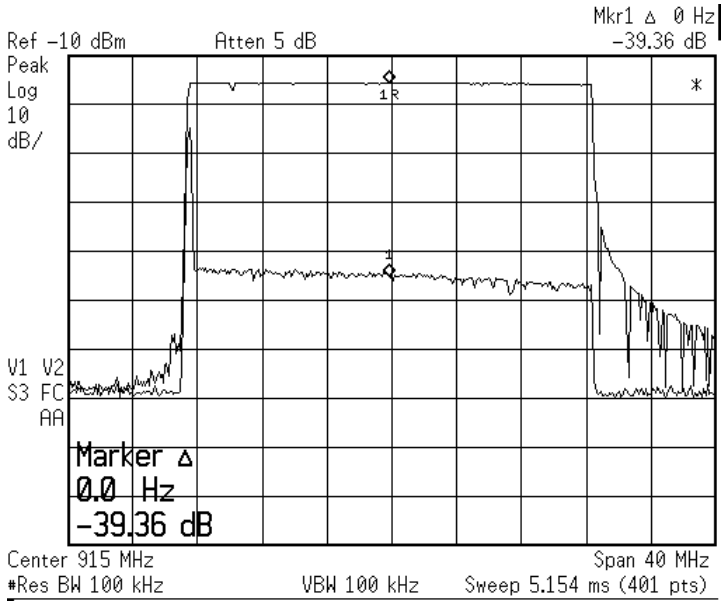


Figure 13: Leakage cancellation achieved by the integrated system.

Second method

Figure 14 shows the power after the LNA to simulated targets producing a a beat frequency of 1kHz and 5kHz. The system attenuates the 5kHz signal 13.7dB while the theoretical calculations show approximately 12dB. Multiple reflections in the

baw are not considered since this is a power measurement and multiple delay signals are much less strong than the main signal. Also, since the multiple delayed signals are very close in frequency they cannot be distinguished using a spectrum analyzer. The performance is also tested using the baseband signal after the IF amplifiers (Figure 15 and Figure 16. In this case multiple delays in the BAW line are benefical since multiple targets can be simulated at a time. The signal corresponding to a 5kHz beat frequeny is attenuated by 10dB, the one corresponding to 15kHz by 7dB and the 25kHz remains practically unchanged.

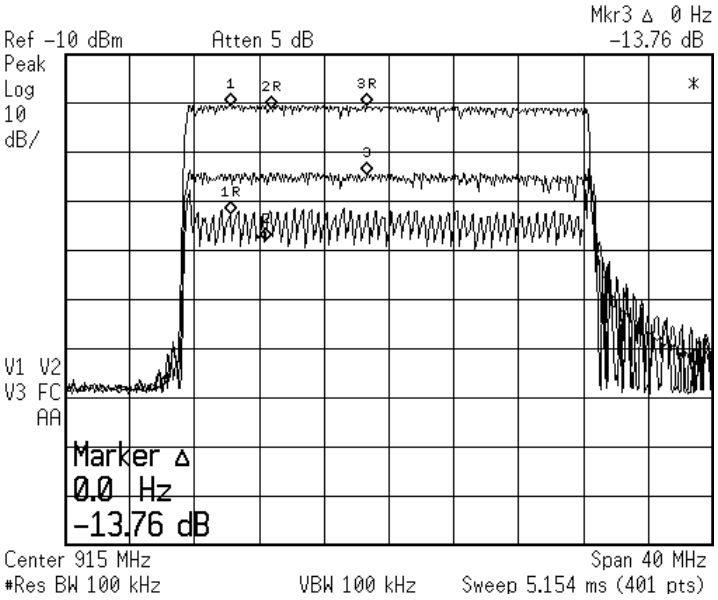


Figure 14: Response to 1kHz and 5kHz beat of the integrated system.

The ripple observed in the response of the 1kHz beat in Figure 14 deserves a special attention. It has been found that the distance between peaks is always exactly the inverse of the delay introduced by the leakage path [16]. In this case the delay line introduces a delay of 2μs, which corresponds to a peak separation of 0.5MHz, exactly the one observed. The most plausible explanation of this effect is found in a non-ideal characteristic of the vector modulator called "gain conformance error". This refers to the error between the gain stated by the baseband inputs (gain setpoint) and the real one. This gain is dependent on the phase change introduced by the modulator (phase setpoint)[17] as can be seen in the page 6 of the datasheet. The error is almost zero when the phase setpoint is zero but

[16]This is, the path that goes from the antenna to the IQ demodulator RF input.

[17]Refer to the datasheet for a detailed explanation of "phase and gain setpoint"

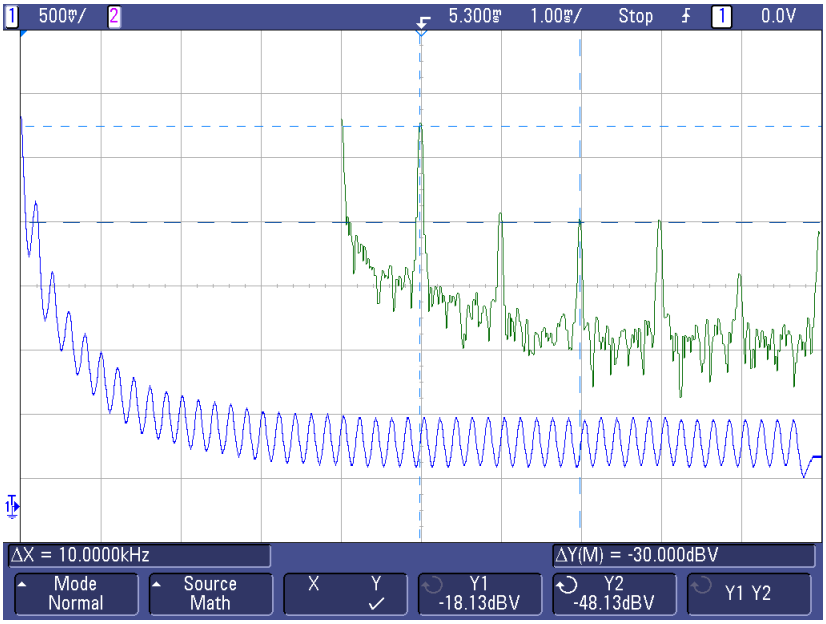


Figure 15: Baseband signal and its FFT after the IF amplifiers produced by a BAW line (5kHz, 15kHz and 25kHz).

there is a deep near 225 degrees. As the frequency changes, the phase setpoint also changes in a periodic fashion due to the delay between paths. The final effect is a periodic vector modulator gain over frequency and hence of the cancellation. The fact that this effect is not observed when the beat frequency is 1kHz supports this hypothesis since the gain conformance error also depends on the gain setpoint. The gain conformance error can also explain the lack of flatness in the leakage cancellation when no delay line is present. This is nothing more than a portion of a ripple with very wide spikes.

The cancellation predicted by the model for 1kHz beat is around 26dB, very close to the minimums of the ripple, which correspond approximately [18] to the greater (most positive) gain conformance error, 0.2dB at worst according to the datasheet.

Another effect that deserves attention is the elimination of the phase noise as can be seen in Figure 13. A mathematical description of this effect can be found in Reference [2]. Unfortunately the phase noise cancellation worsens as the signal delay through the leakage path increases.

[18]The actual minimums are buried below the filter skirts of the spectrum analyzer, however observations show that the actual minimums are very close to the ones shown in Figure 14.

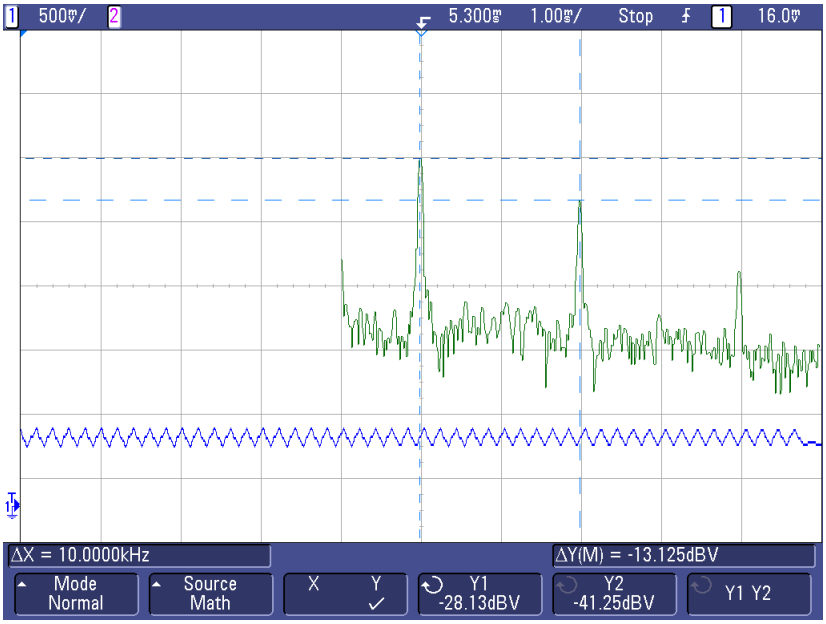


Figure 16: Baseband signal and its FFT after the IF amplifiers produced by a BAW line (5kHz, 15kHz and 25kHz) when RPC is active

Third method

Two Yagi antennas are used to transmit and receive. This kind of antennas have low directivity but this is an advantage in this case since a wide portion of the environment can be illuminated, hence receiving power of a variety of targets at different distances. From Figure 17 and 18 it can be seen that the leakage, which has a beat frequency of 90Hz is reduced by 37dB. Noise impairs the power received from the environment. Averaging and careful observation over sweep realizations is used to detect stable or relatively stable portions of the spectrum. One of the stationary portions is the peak at 1.30kHz indicated by the marker. The cancellation of this peak is 20dB while the theory predicts 26dB. This error is justified because variability on received power was observed through sweep realizations. In general, the cancellation observed from 0Hz to 2kHz (where the signal is buried below the noise level) indicates a correct behaviour of the RPC. The harmonics seen in the cancelled signal are caused by the settling time of the signal generator and can be safely ignored.

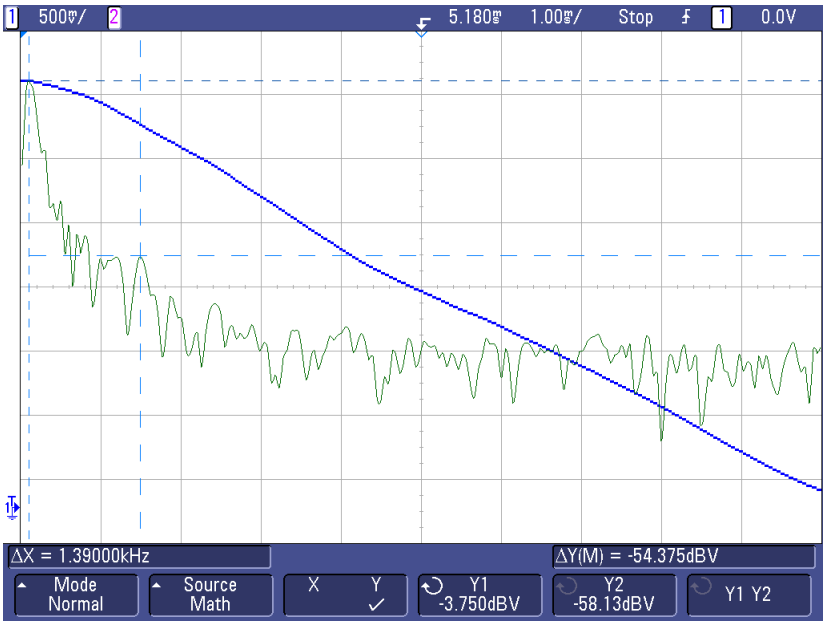


Figure 17: IF signal and its FFT received by the antenna with an open loop.

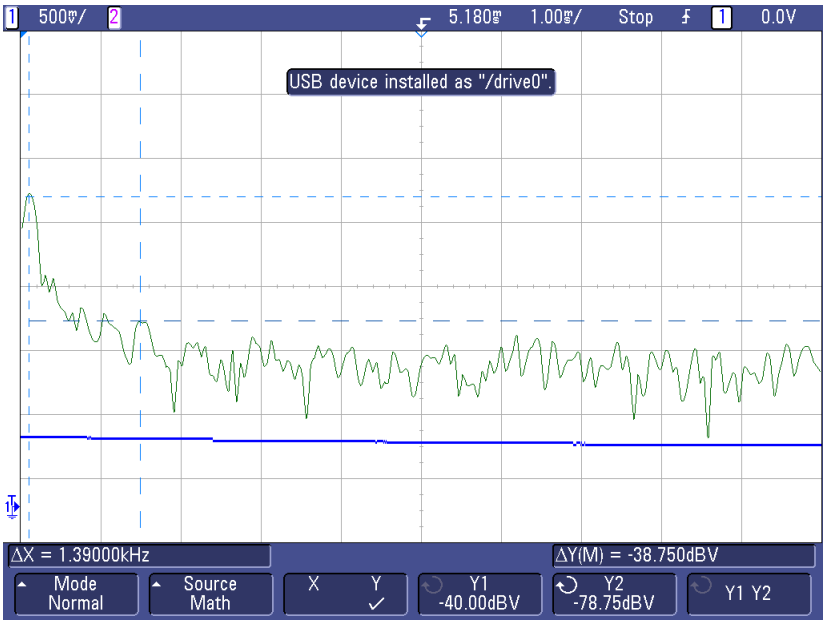
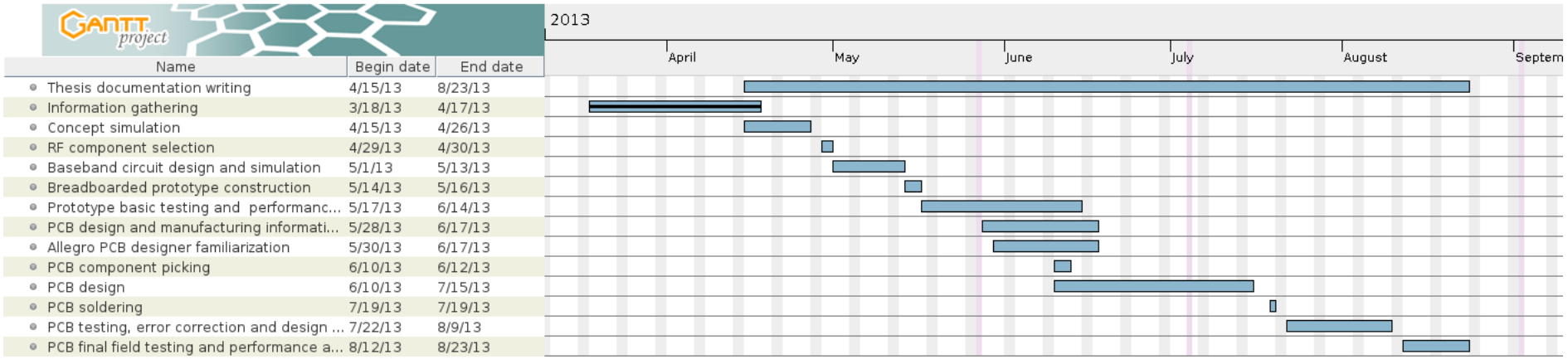


Figure 18: IF signal and its FFT received by the antenna with an closed loop.

6 Conclusions

This work has shown that the RPC structure used to improve the transmitter-receiver isolation solves the problem in a great extent. The conformance between the design goals and the actual test results has been higher than expected. In fact, a cancellation ratio of 40dB seemed a too optimistic goal taking into account the performance reported in the different publications available. Probably this high compliance is due to the fact that the system operates in a relatively low frequency. The work has also presented a design methodology and a description of different issues that any of the papers dedicated to the RPC idea offer with such a level of detail. The explanations and insights may be valuable for any future project involving a RPC, either its design or its implementation in a FMCW radar for UHF or higher frequencies. The immediate future work involves further field testing and the implementation in the UHF wind profiler. The effects of the cancellation frequency ripple described in the testing section should be also investigated. Further work could be to design a RPC for a higher frequency, e.g. X-band and try to achieve a higher level of integration in a single board, taking advantage of the size reduction of RF components such as couplers, splitters and amplifiers.

7 Project Gantt diagram



Name	Begin date	End date
Thesis documentation writing	4/15/13	8/23/13
Information gathering	3/18/13	4/17/13
Concept simulation	4/15/13	4/26/13
RF component selection	4/29/13	4/30/13
Baseband circuit design and simulation	5/1/13	5/13/13
Breadboarded prototype construction	5/14/13	5/16/13
Prototype basic testing and performanc...	5/17/13	6/14/13
PCB design and manufacturing informati...	5/28/13	6/17/13
Allegro PCB designer familiarization	5/30/13	6/17/13
PCB component picking	6/10/13	6/12/13
PCB design	6/10/13	7/15/13
PCB soldering	7/19/13	7/19/13
PCB testing, error correction and design ...	7/22/13	8/9/13
PCB final field testing and performance a...	8/12/13	8/23/13

References

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[9] J. Karki, "Fully-deifferential amplifiers," Texas Instruments, Tech. Rep., 2002, SLOA054D.

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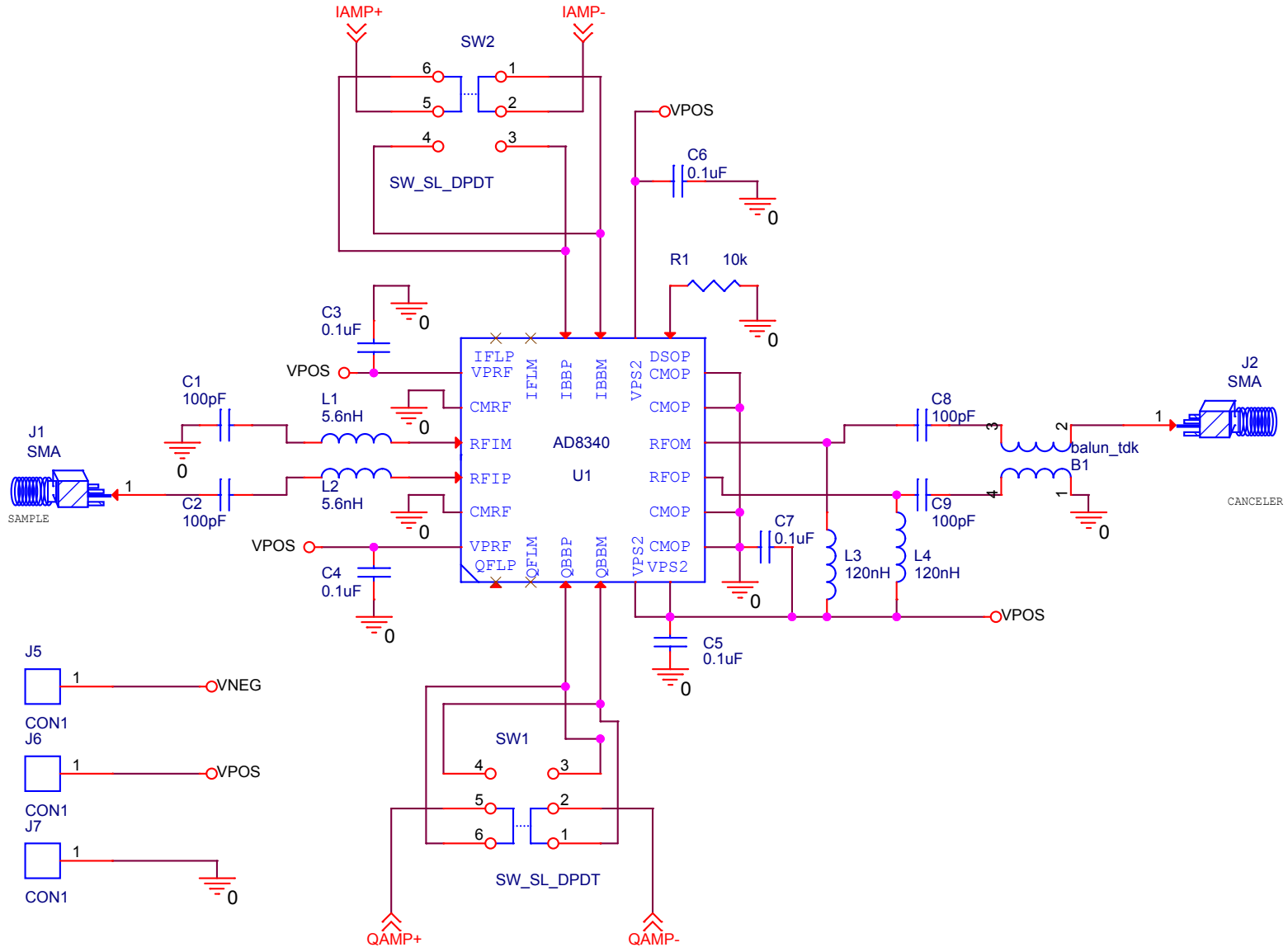
[11] G. M. Brooker, "Understanding Millimetre Wave FMCW Radars." Australian Centre for Field Robotics, University of Sydney.

Appendices

A Board schematics and artwork

The documents in this appendix are in order:

- Board schematics
- Top cooper plane artwork
- Second cooper plane artwork
- Third cooper plane artwork
- Bottom cooper layer artwork
- Top silkscreen artwork
- Top soldermask artwork
- Bottom soldermask artwork
- Board component drawing and manufacturing notes document.



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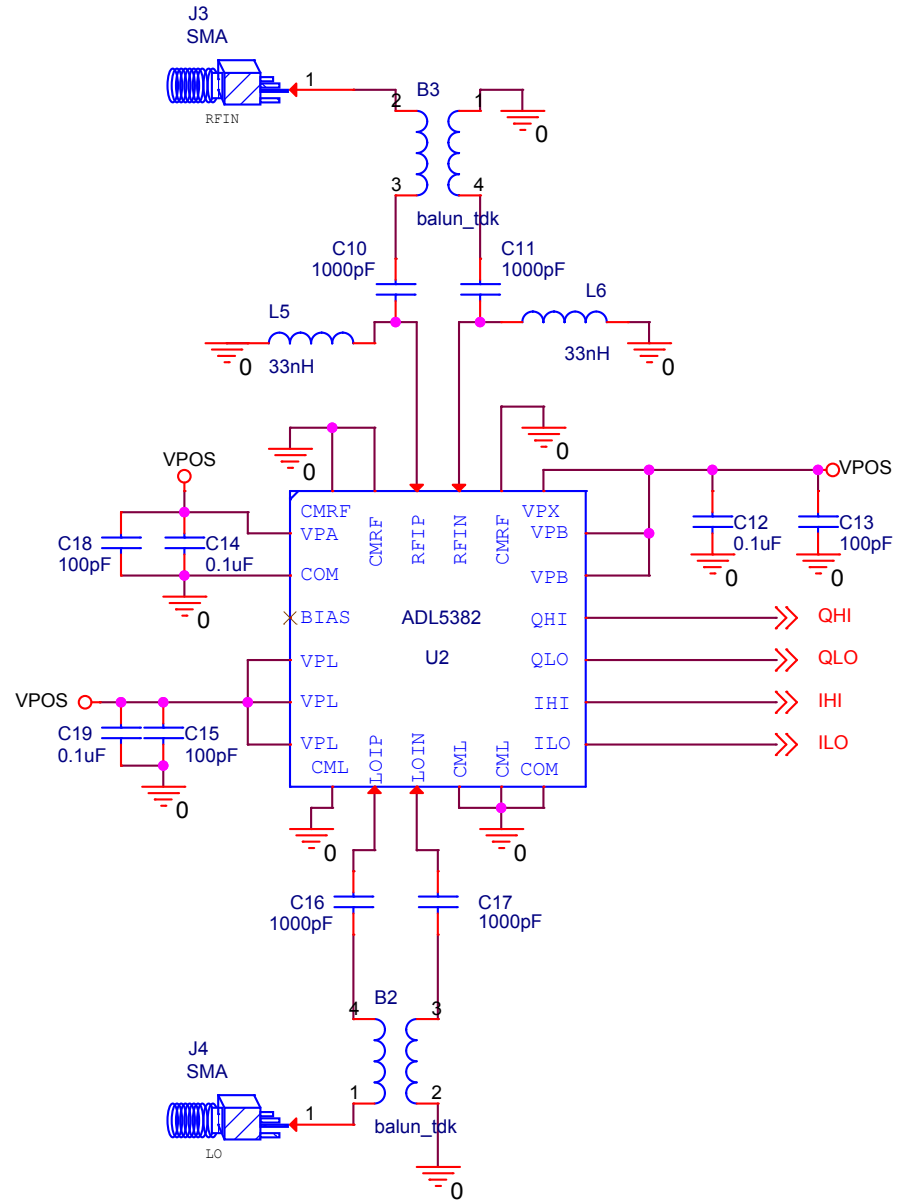
Date: Saturday, July 20, 2013	Sheet 1 of 3		



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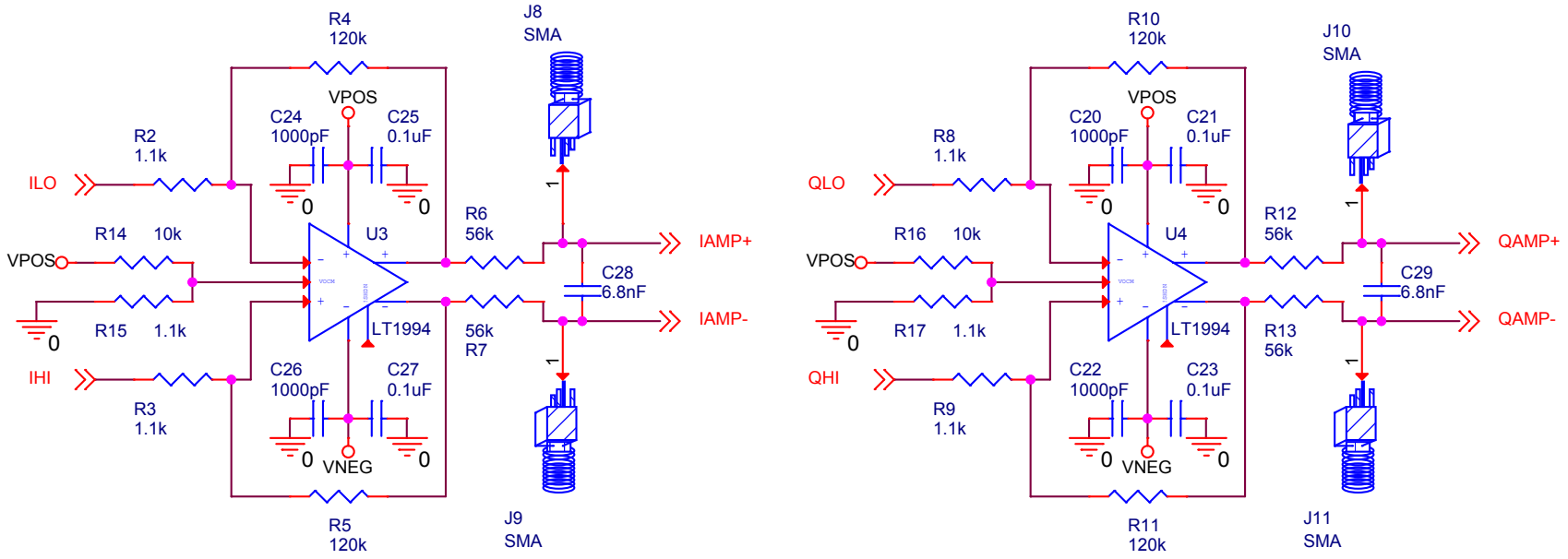
Date: Friday, July 19, 2013	Sheet 2 of 3		



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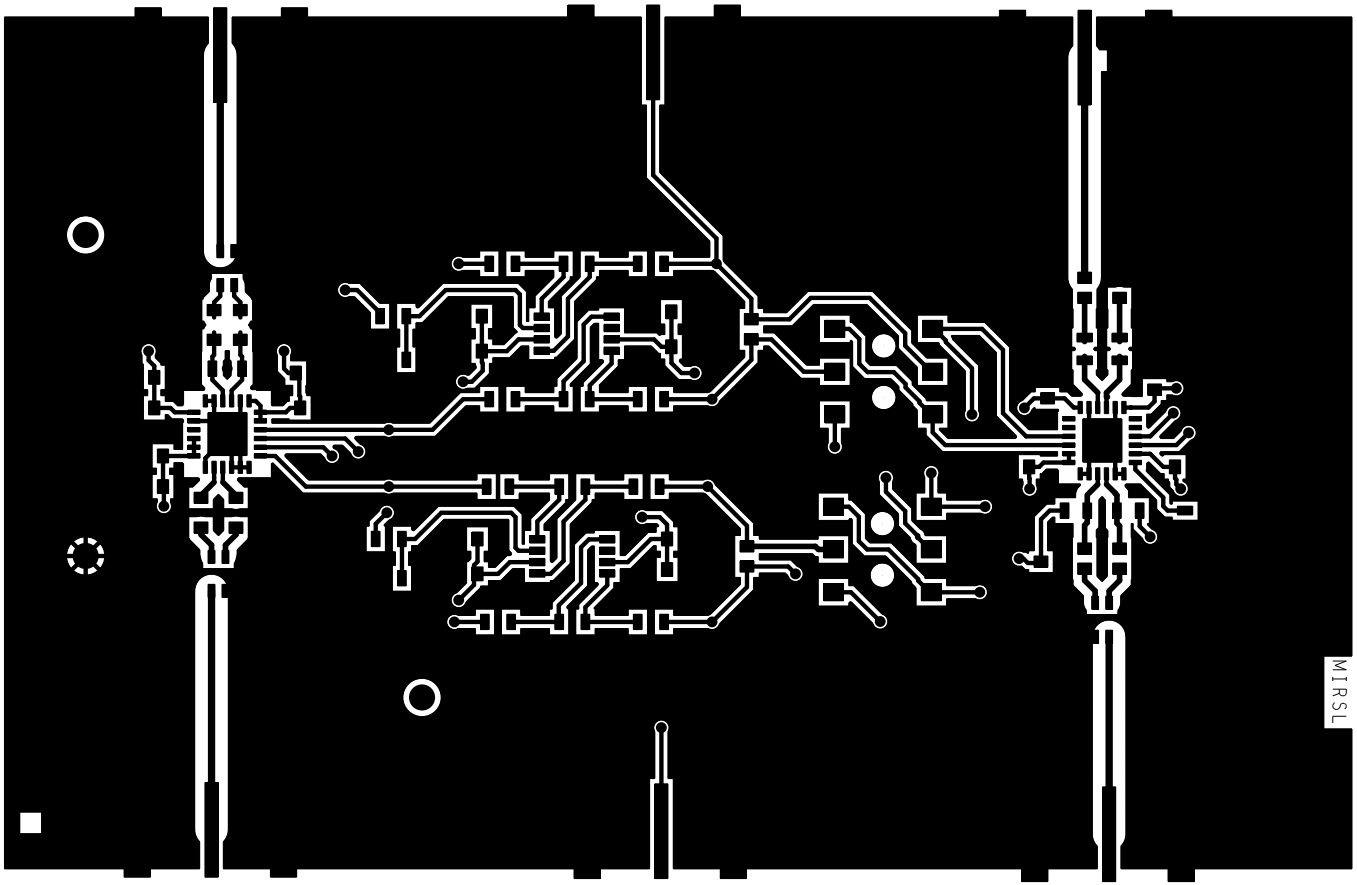
Date: Saturday, July 20, 2013	Sheet 3 of 3	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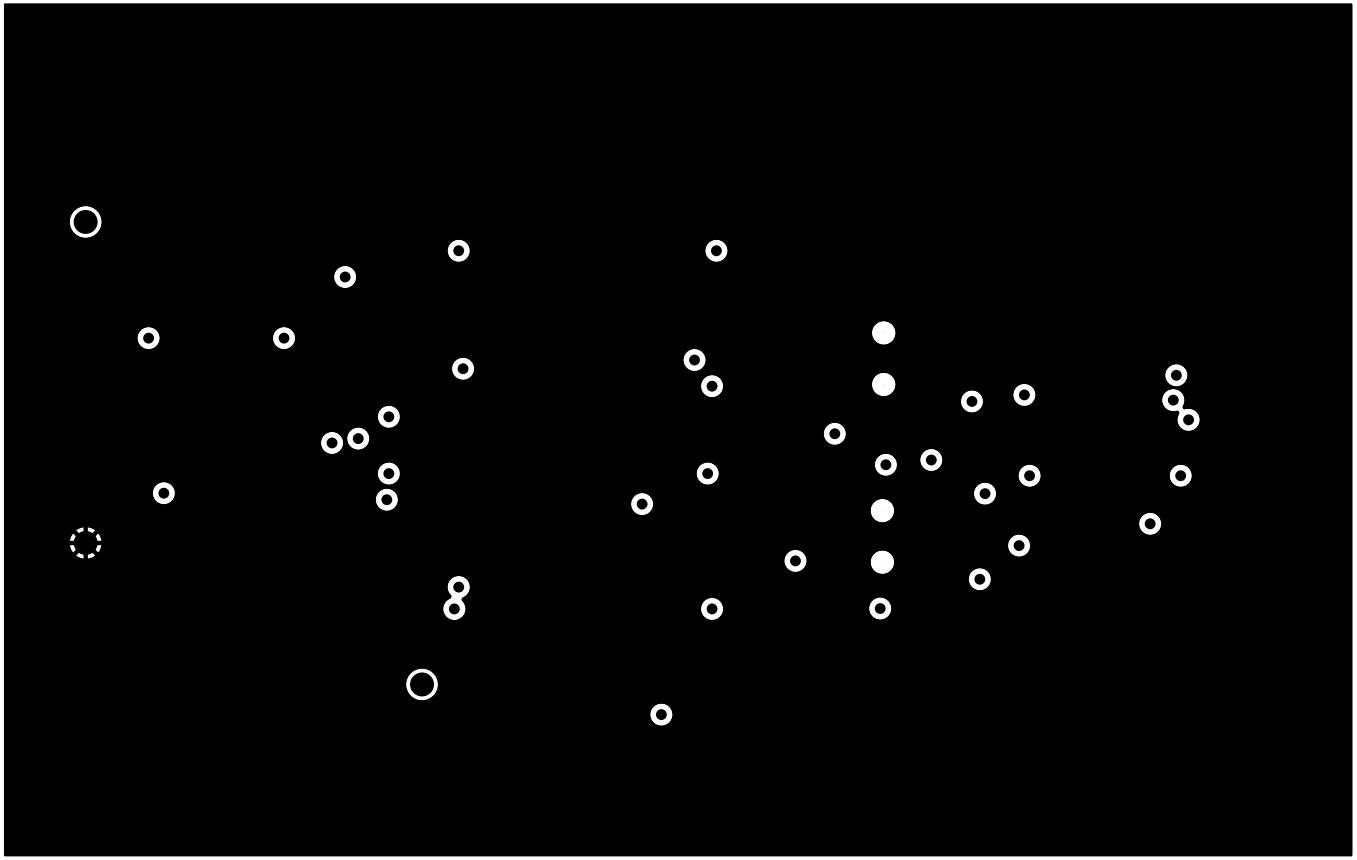
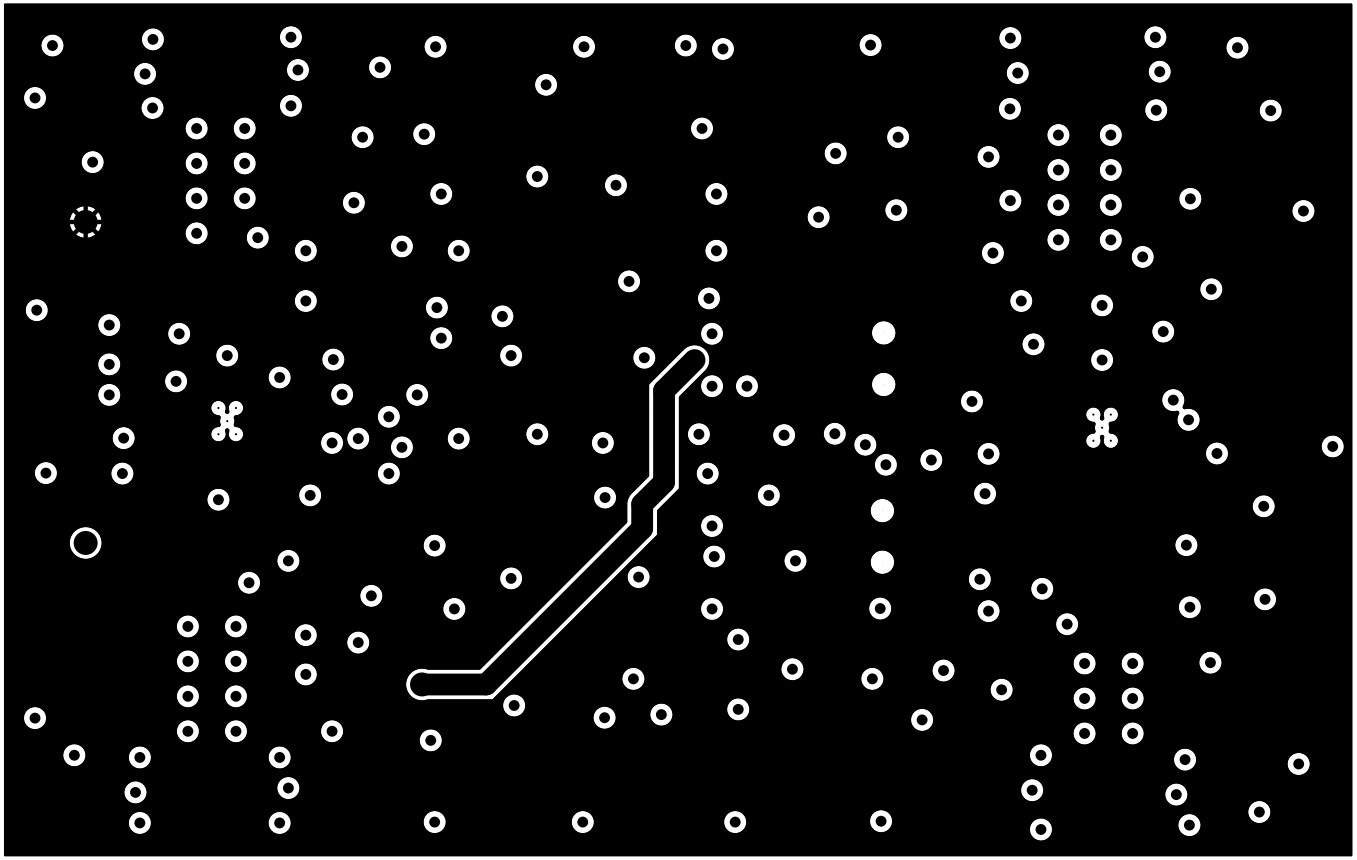
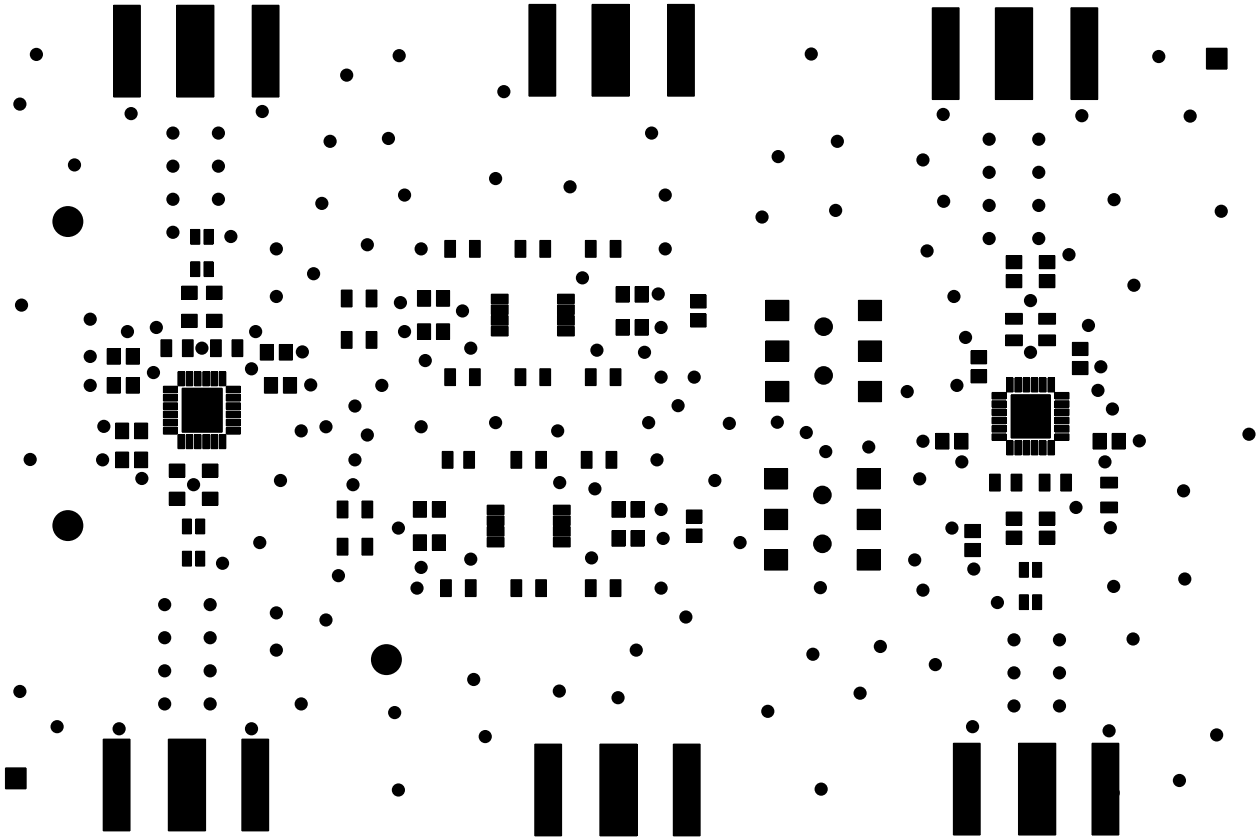
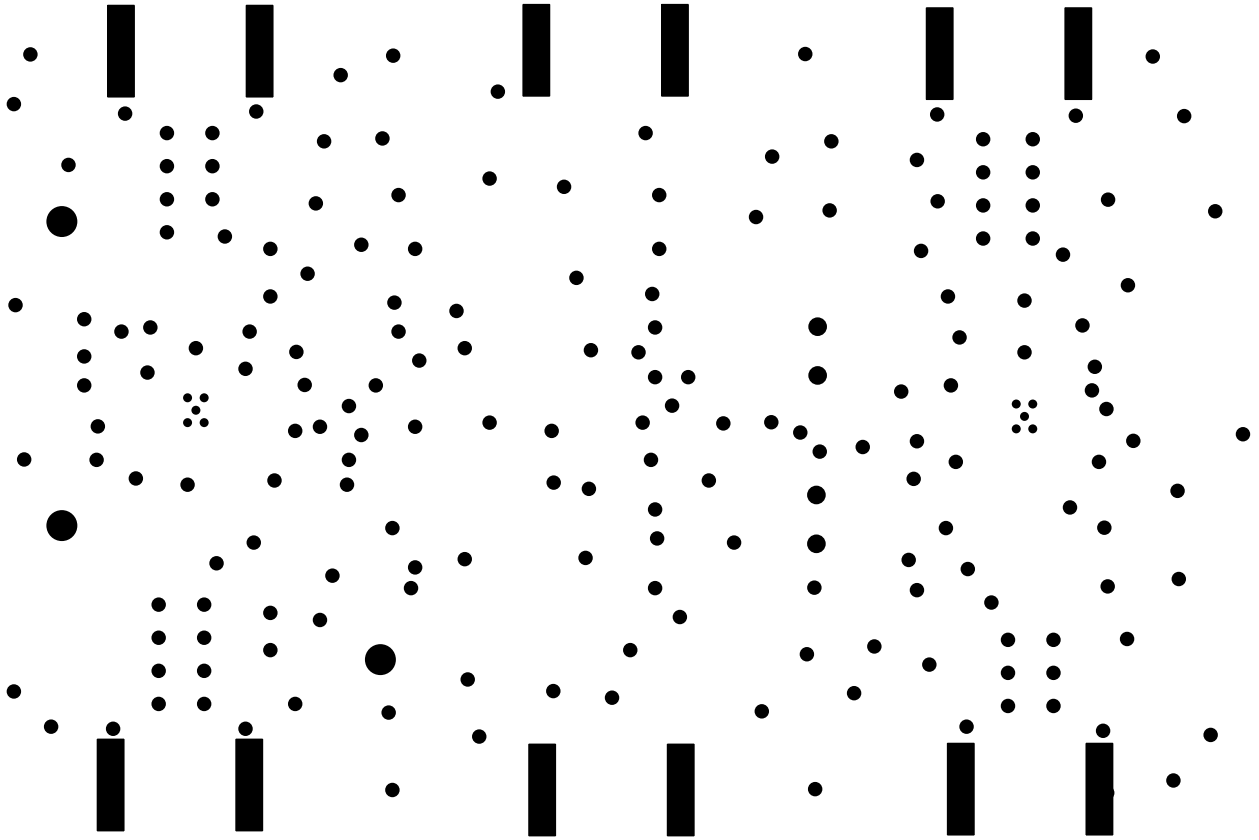


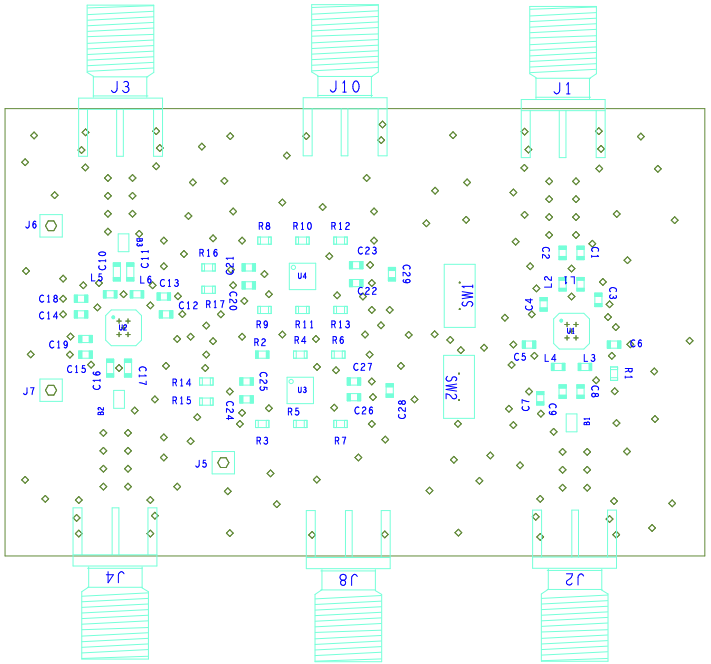


JSBIM

ADRIA AMEZAGA
MIRSL (UMASS AMHERST)
07/22/13 SECOND REVISION



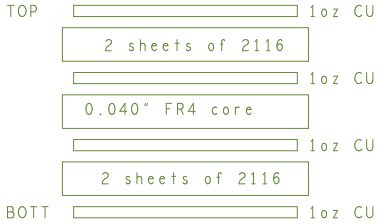




NOTES

1. All dimensions are in decimal inches unless otherwise specified
2. Part number: RPC_JULY_2013_REV2
3. Tolerances for vias: STANDARD
4. BASE MATERIAL
   Top dielectric should be FR-370HR
5. PCB Thickness
   0.0062 +/- 10% measured over metal
6. SOLDER MASK
   Color: Green
7. SILKSCREEN
   White non conductive ink
   No ink to appear on plated through holes or SMT pins
8. IMPEDANCES
   This board is not subjected to controlled impedances
9. Board outlines
   This PCB consists on a board of 3.13"x2"

DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILS			
FIGURE	SIZE	PLATED	QTY
+	12.0	PLATED	10
◇	13.0	PLATED	208
⬡	36.0	PLATED	3
·	36.0	PLATED	4



B Study of costs

DIGIKEY PART NUMBER	QTY PER BOARD		PART QTY			UNIT PART COST PER QTY OF BOARDS			TOTAL PART COST PER QTY OF BOARDS		
		BOARD QTY	50	500	5000	50	500	5000	50	500	5000
445-9282-1-ND	3										
720-1325-1-ND	4		150	1500	15000	0.402	0.25548	0.25548	60.3	383.22	3832.2
399-1096-1-ND	9		200	2000	20000	0.5853	0.43898	0.43898	117.06	877.96	8779.6
720-1340-1-ND	4		450	4500	45000	0.00694	0.0054	0.0054	3.123	24.3	243
445-2314-1-ND	3		200	2000	20000	0.794	0.58868	0.58868	158.8	1177.36	11773.6
445-1298-1-ND	4		150	1500	15000	0.0292	0.01593	0.01593	4.38	23.895	238.95
445-3426-1-ND	2		200	2000	20000	0.022	0.012	0.012	4.4	24	240
J716-ND	6		100	1000	10000	0.0499	0.03518	0.02887	4.99	35.18	288.7
A105161CT-ND	3		300	3000	30000	2.90564	2.1132	2.1132	871.692	6339.6	63396
P14804CT-ND	2		150	1500	15000	0.098	0.07096	0.0642	14.7	106.44	963
A102560CT-ND	2		100	1000	10000	0.2265	0.14558	0.14558	22.65	145.58	1455.8
P14831CT-ND	2		100	1000	10000	0.311	0.22803	0.22803	31.1	228.03	2280.3
541-10.0KHCT-ND	3		100	1000	10000	0.286	0.18383	0.18383	28.6	183.83	1838.3
401-2013-1-ND	2		150	1500	15000	0.0251	0.01711	0.01711	3.765	25.665	256.65
541-120KHCT-ND	4		100	1000	10000	1.0604	0.87484	0.87484	106.04	874.84	8748.4
541-56.0KHCT-ND	4		200	2000	20000	0.0251	0.01711	0.01711	5.02	34.22	342.2
541-1.10KHCT-ND	2		200	2000	20000	0.0251	0.01711	0.01711	5.02	34.22	342.2
AD8340ACPZ-REEL7CT-ND	1		100	1000	10000	0.0251	0.01711	0.01711	2.51	17.11	171.1
ADL5382ACPZ-R7CT-ND	1		50	500	5000	15.1272	11.8008	11.8008	756.36	5900.4	59004
LT1994CMS8#PBF-ND	2		50	500	5000	9.0764	7.08048	7.08048	453.82	3540.24	35402.4
			100	1000	10000	1.95	1.95	1.95	195	1950	19500
								COST PER BOARD	56.9866	43.85218	43.81928
								TOTAL	2849.33	21926.09	219096.4

BOARD COST WITHOUT PARTS			
QTY OF BOARDS	50	500	5000
UNIT BOARD COST	12.57	3.68	2.54
TOTAL BOARD COST	628.5	1840	12700

PART ASSEMBLY COST			
QTY OF BOARDS	50	500	5000
COST PER BOARD	25.43	17.03	16.19
TOTAL ASSEMBLY COST	1271.5	8515	80950

NOTE: ALL PRICES ARE PRESENTED UN USD

TOTAL COST			
QTY OF BOARDS	50	500	5000
UNIT BOARD COST	69.5566	47.53218	46.35928
TOTAL BOARD COST	3477.83	23766.09	231796.4

C Datasheets

700 MHz to 1000 MHz RF Vector Modulator

AD8340

FEATURES

Cartesian amplitude and phase modulation
700 MHz to 1.0 GHz frequency range
Continuous magnitude control of −2 dB to −32 dB
Continuous phase control of 0° to 360°
Output third-order intercept 24 dBm
Output 1 dB compression point 11 dBm
Output noise floor −149 dBm/Hz @ full gain
Adjustable modulation bandwidth up to 230 MHz
Fast output power disable
4.75 V to 5.25 V single-supply voltage

FUNCTIONAL BLOCK DIAGRAM

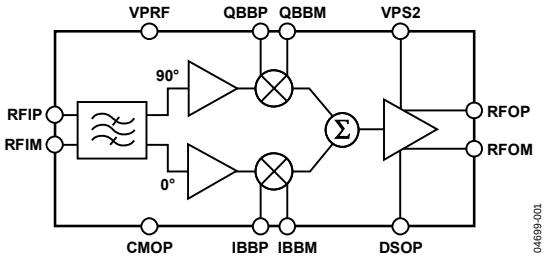


Figure 1.

APPLICATIONS

RF PA linearization/RF predistortion
Amplitude and phase modulation
Variable attenuators and phase shifters
CDMA2000, GSM/EDGE linear power amplifiers
Smart antennas

GENERAL DESCRIPTION

The AD8340 vector modulator performs arbitrary amplitude and phase modulation of an RF signal. Because the RF signal path is linear, the original modulation is preserved. This part can be used as a general-purpose RF modulator, a variable attenuator/phase shifter, or a remodulator. The amplitude can be controlled from a maximum of −2 dB to less than −32 dB, and the phase can be shifted continuously over the entire 360° range. For maximum gain, the AD8340 delivers an OP1dB of 11 dBm, an OIP3 of 24 dBm, and an output noise floor of −149 dBm/Hz, independent of phase. It operates over a frequency range of 700 MHz to 1.0 GHz.

The baseband inputs in Cartesian I and Q format control the amplitude and phase modulation imposed on the RF input signal. Both I and Q inputs are dc-coupled with a ±500 mV differential full-scale range. The maximum modulation bandwidth is 230 MHz, which can be reduced by adding external capacitors to limit the noise bandwidth on the control lines.

Both the RF inputs and outputs can be used differentially or single-ended and must be ac-coupled. The RF input and output impedances are nominally 50 Ω over the operating frequency range. The DSOP pin allows the output stage to be disabled quickly to protect subsequent stages from overdrive. The AD8340 operates off supply voltages from 4.75 V to 5.25 V while consuming approximately 130 mA.

The AD8340 is fabricated using the Analog Devices, Inc. proprietary, high performance 25 GHz SOI complementary bipolar IC process. It is available in a 24-lead RoHS-compliant LFCSP package and operates over a −40°C to +85°C temperature range. Evaluation boards are available.

Rev. B
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Changes to Figure 30 12
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7/07—Rev. 0 to Rev. A

Replaced Pin Configuration and Function Descriptions Section 5
Changes to Ordering Guide 20

6/04—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, Z_O = 50 Ω, f = 880 MHz, single-ended, ac-coupled source drive to RFIP through 5.6 nH series inductor, RFIM ac-coupled through 5.6 nH series inductor to common, differential-to-single-ended conversion at output using 1:1 balun.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		700		1000	MHz
Maximum Gain	Maximum gain setpoint for all phase setpoints		−2		dB
Minimum Gain	$V_{BBI} = V_{BBQ}$ = 0 V		−32		dB
Gain Control Range	Relative to maximum gain		30		dB
Phase Control Range	Over 30 dB control range		360		Degrees
Gain Flatness	Over any 60 MHz bandwidth		0.25		dB
Group Delay Flatness	Over any 60 MHz bandwidth		10		ps
RF INPUT STAGE	RFIM, RFIP (Pin 21 and Pin 22)				
Input Return Loss	From RFIP to CMRF (with 5.6 nH series inductors)		20		dB
CARTESIAN CONTROL INTERFACE (I and Q)	IBBP, IBBM, QBBP, QBBM (Pin 16, Pin 15, Pin 3, Pin 4)				
Gain Scaling			2		1/V
Modulation Bandwidth	250 mV p-p sinusoidal baseband input single-ended		230		MHz
Second Harmonic Distortion	250 mV p-p, 1 MHz, sinusoidal baseband input differential		47		dBc
Third Harmonic Distortion	250 mV p-p, 1 MHz, sinusoidal baseband input differential		45		dBc
Step Response	For gain setpoint from 0.1 to 0.9 (V_{BBP} = 0.5 V, V_{BBM} = 0.55 V to 0.95 V)		45		ns
	For gain setpoint from 0.9 to 0.1 (V_{BBP} = 0.5 V, V_{BBM} = 0.95 V to 0.55 V)		47		ns
RF OUTPUT STAGE	RFOP, RFOM (Pin 9 and Pin 10)				
Output Return Loss	Measured through balun		7.5		dB
f = 880 MHz					
Gain	Maximum gain setpoint		−2		dB
Output Noise Floor	Maximum gain setpoint, no input		−149		dBm/Hz
	P_{IN} = 0 dBm, frequency offset = 20 MHz		−147		dBm/Hz
Output IP3	f1 = 880 MHz, f2 = 877.5 MHz, maximum gain setpoint		24		dBm
ACPR	IS-95, single carrier, P_{OUT} = 0 dBm, maximum gain, phase setpoint = 45°		62		dBc
Output 1 dB Compression Point	Maximum gain		11		dBm
POWER SUPPLY	VPS2 (Pin 5, Pin 6, Pin 14); RFOP, RFOM (Pin 9 and Pin 10)				
Positive Supply Voltage		4.75	5	5.25	V
Total Supply Current	Includes load current	110	130	150	mA
OUTPUT DISABLE	DSOP (Pin 13)				
Disable Threshold			2.5		V
Maximum Attenuation	DSOP = 5 V		40		dB
Enable Response Time	Delay following high-to-low transition until device meets full specifications		15		ns
Disable Response Time	Delay following low-to-high transition until device produces full attenuation		10		ns

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage VPRF, VPS2	5.5 V
DSOP	5.5 V
IBBP, IBBM, QBBP, QBBM	2.5 V
RFOP, RFOM	5.5 V
RF Input Power at Maximum Gain (50 Ω)	13 dBm
(RFIP or RFIM, Single-Ended Drive)	
Equivalent Voltage	2.8 V p-p
Internal Power Dissipation	825 mW
θ_{JA} (with Pad Soldered to Board)	59°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

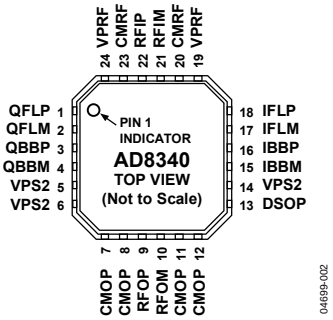


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1; 2	QFLP; QFLM	Q Baseband Input Filter Pins. Connect optional capacitor to reduce Q baseband channel low-pass corner frequency.
3; 4	QBBP; QBBM	Q Channel Differential Baseband Inputs.
5, 6, 14; 19, 24	VPS2; VPRF	Positive Supply Voltage, 4.75 V to 5.25 V.
7, 8, 11, 12; 20, 23	CMOP; CMRF	Device Common. Connect via lowest possible impedance to external circuit common.
9; 10	RFOP; RFOM	Differential RF Outputs. Must be ac-coupled. Differential impedance 50 Ω nominal.
13	DSOP	Output Disable. Pull high to disable output stage.
15; 16	IBBM; IBBP	I Channel Differential Baseband Inputs.
17; 18	IFLM; IFLP	I Baseband Input Filter Pins. Connect optional capacitor to reduce I baseband channel low-pass corner frequency.
21; 22	RFIM; RFIP	Differential RF Inputs. Must be ac-coupled. Differential impedance 50 Ω nominal.

TYPICAL PERFORMANCE CHARACTERISTICS

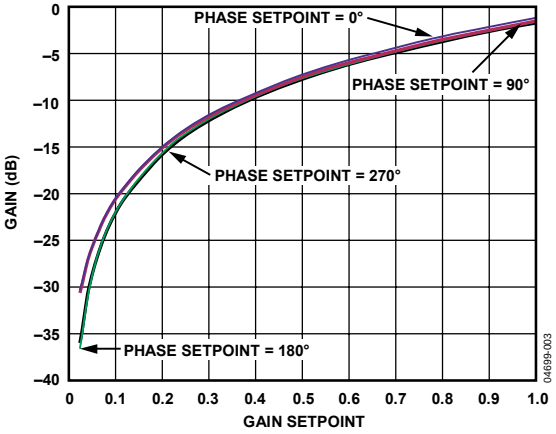


Figure 3. Gain Magnitude vs. Gain Setpoint at Different Phase Setpoints, RF Frequency = 880 MHz

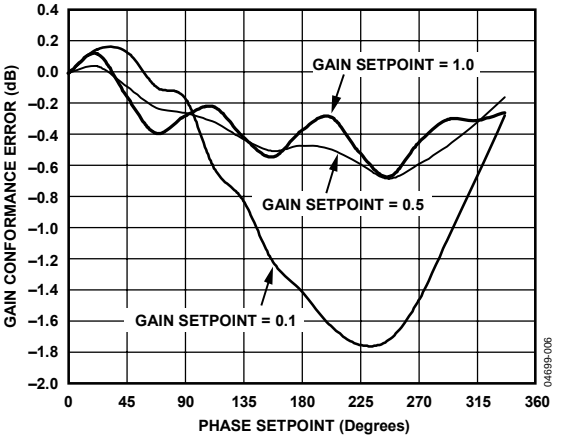


Figure 6. Gain Conformance Error vs. Phase Setpoint at Different Gain Setpoints

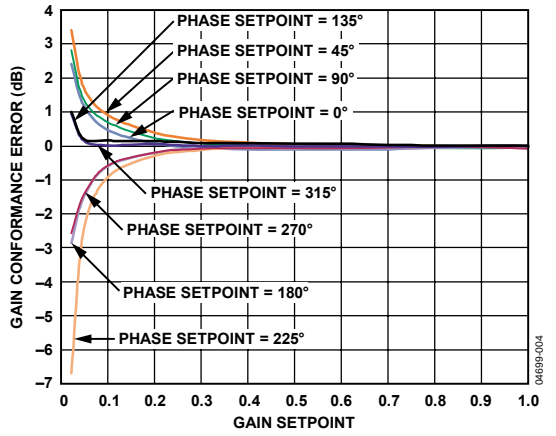


Figure 4. Gain Conformance Error vs. Gain Setpoint at Different Phase Setpoints

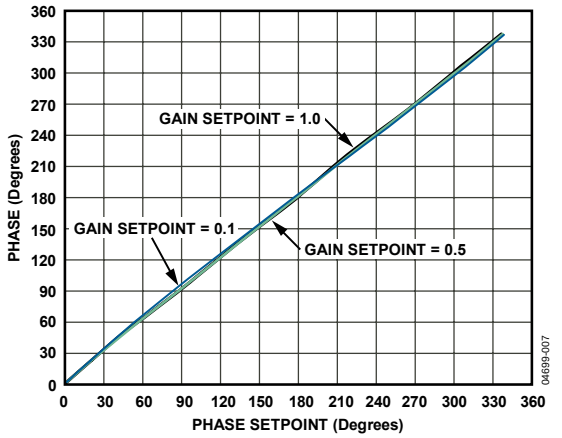


Figure 7. Phase vs. Phase Setpoint at Different Gain Setpoints

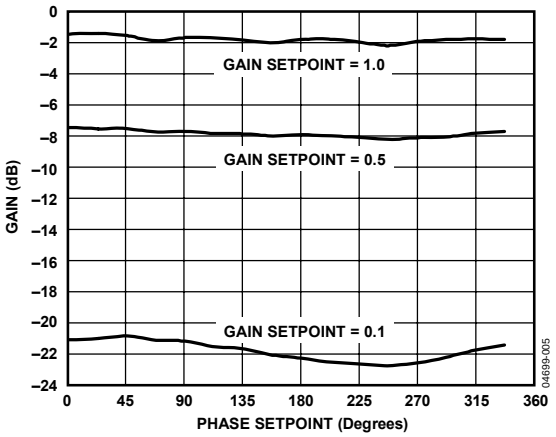


Figure 5. Gain Magnitude vs. Phase Setpoint at Different Gain Setpoints

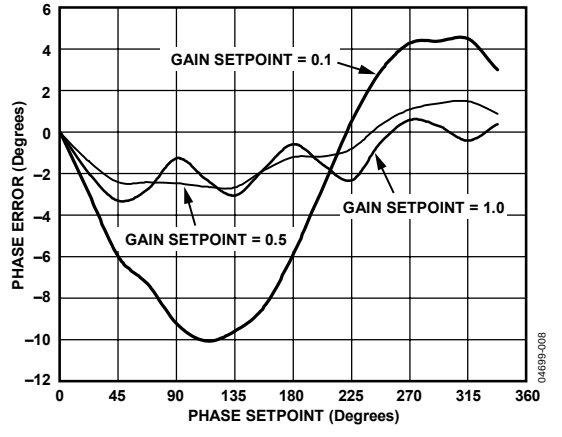


Figure 8. Phase Error vs. Phase Setpoint at Different Gain Setpoints

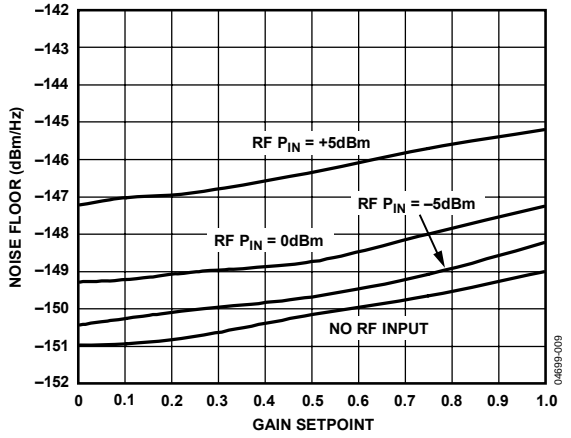


Figure 9. Output Noise Floor vs. Gain, Noise in dBm/Hz, No Carrier, With Carrier (20 MHz Offset) P_{IN} = –5 dBm, 0 dBm, and +5 dBm

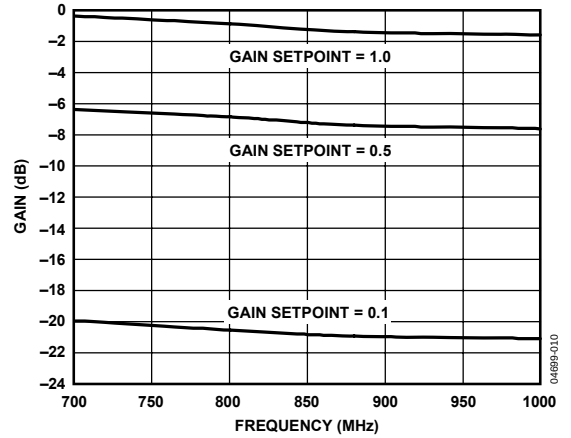


Figure 10. Gain vs. Frequency at Different Gain Setpoints (700 MHz to 1000 MHz), Phase Setpoint = 0°

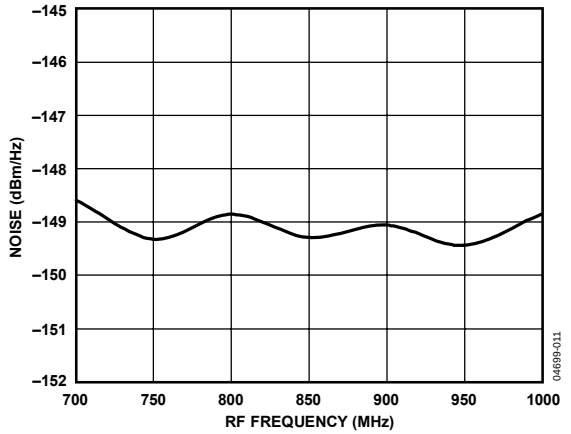


Figure 11. Output Noise Floor vs. Frequency, Maximum Gain, No RF Carrier, Phase Setpoint = 0°

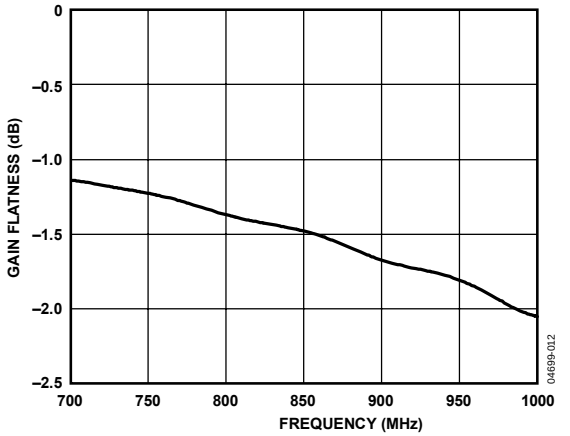


Figure 12. Gain Flatness vs. Frequency, Maximum Gain, Phase Setpoint = 0°

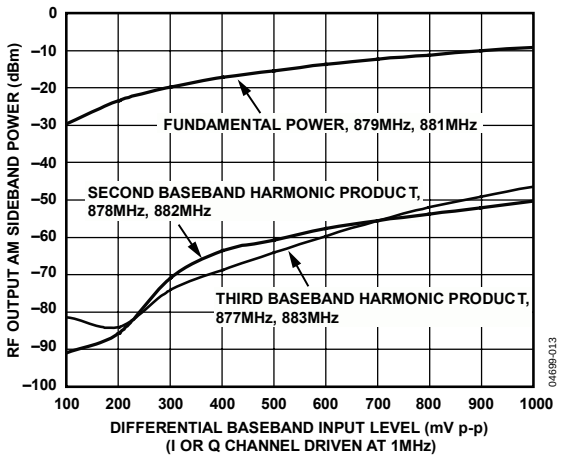


Figure 13. Baseband Harmonic Distortion (I and Q Channel, RF Input = 0 dBm, Balun and Cable Losses of Approximately 2 dB Not Accounted for in Plot)

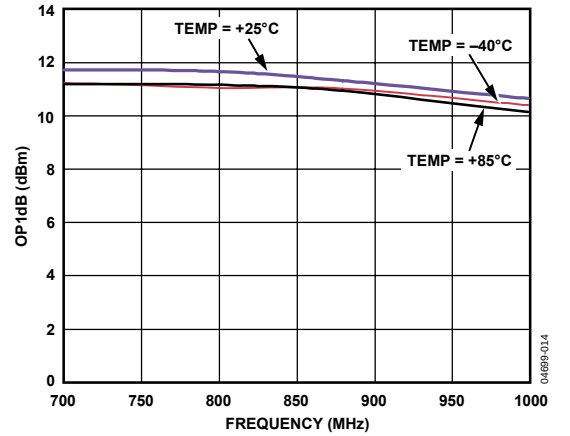


Figure 14. Output 1 dB Compression Point vs. Frequency and Temperature, Maximum Gain, Phase Setpoint = 0°

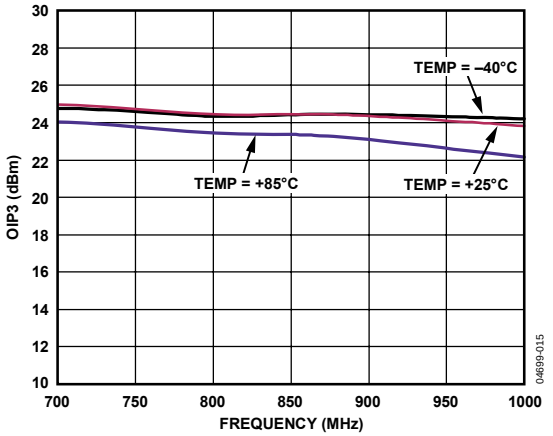


Figure 15. Output IP3 vs. Frequency and Temperature, Maximum Gain, I Only

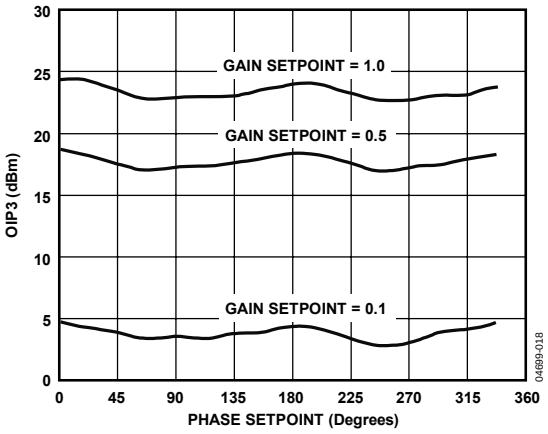


Figure 18. Output IP3 vs. Gain and Phase Setpoints, 2.5 MHz Carrier Spacing

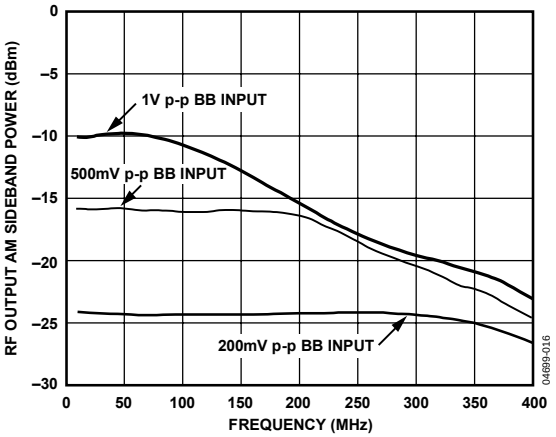


Figure 16. I/Q Modulation Bandwidth vs. Baseband Magnitude

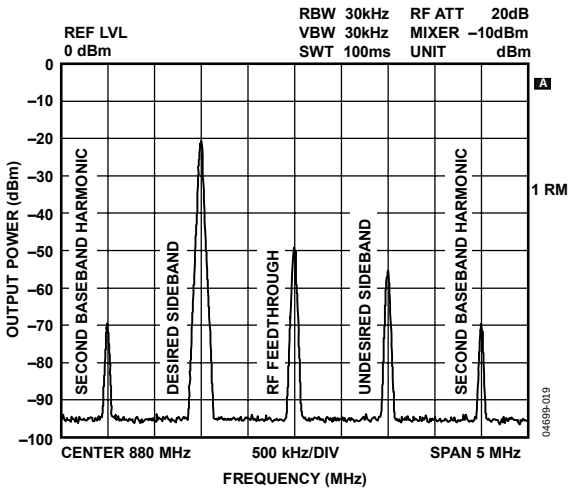


Figure 19. Single-Sideband Performance, 880 MHz, −10 dBm RF Input; 1 MHz, 500 mV p-p Differential BB Drive

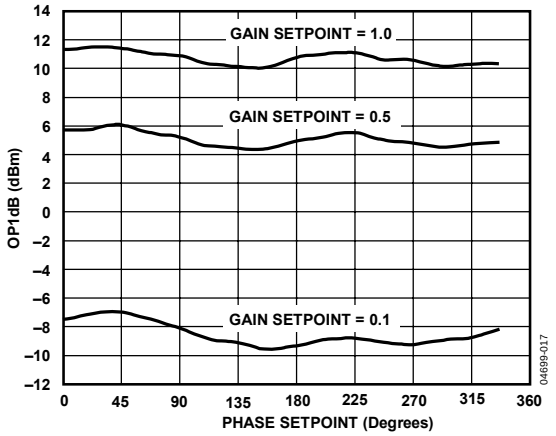


Figure 17. Output 1dB Compression Point vs. Gain and Phase Setpoints

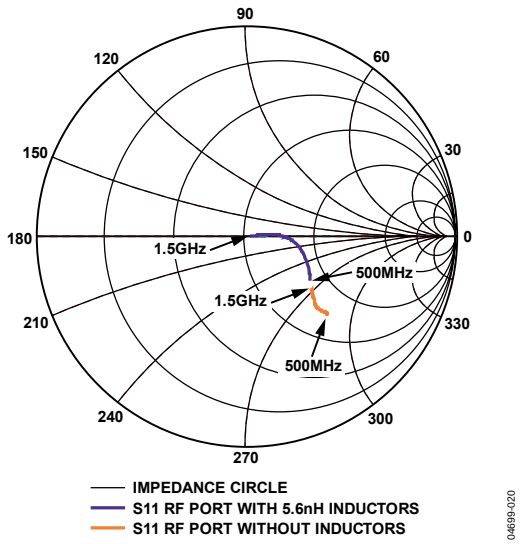


Figure 20. Input and Output Impedance Smith Chart (with Frequency Markers)

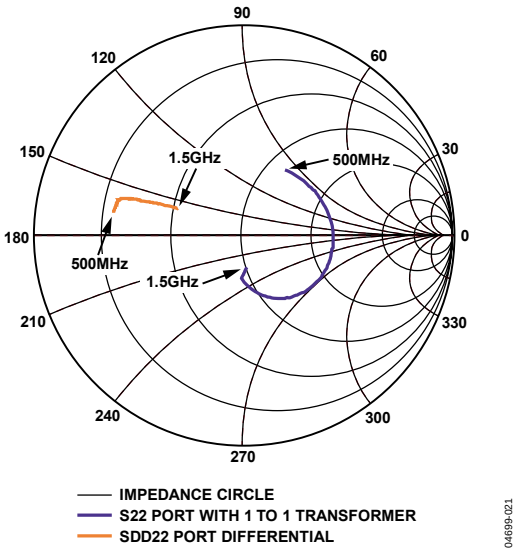


Figure 21. Output Impedance Smith Chart (with Frequency Markers)

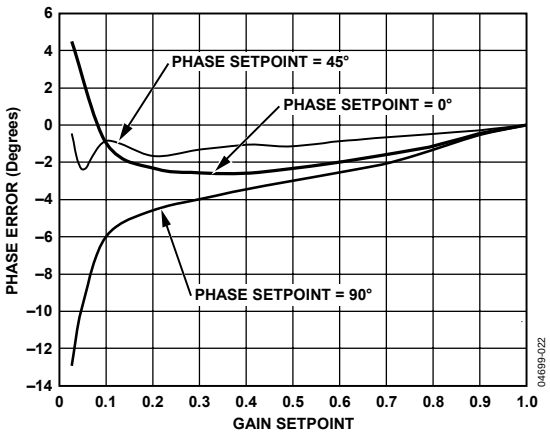


Figure 22. Phase Error vs. Gain Setpoint by Phase Setpoint, 5 V DC, 25°C, 880 MHz

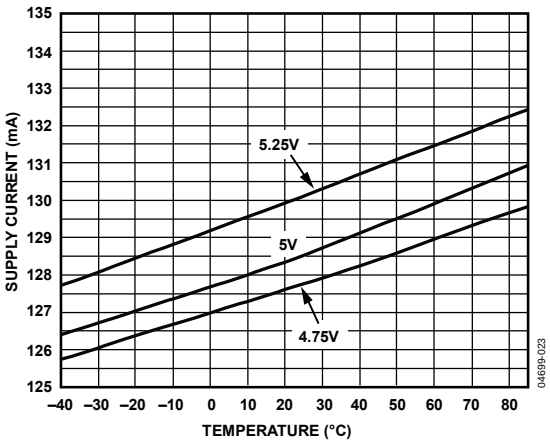


Figure 23. Supply Current vs. Temperature

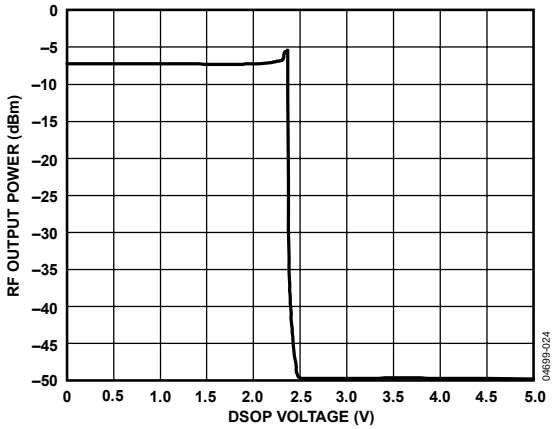


Figure 24. Power Shutdown Attenuation

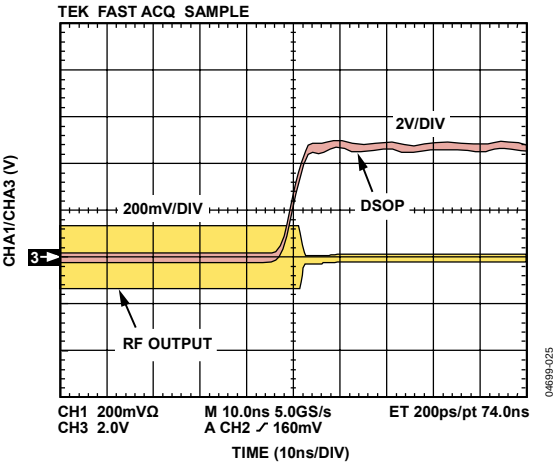


Figure 25. Power Shutdown Response Time

THEORY OF OPERATION

The AD8340 is a linear RF vector modulator with Cartesian baseband controls. In the simplified block diagram shown in Figure 26, the RF signal propagates from the left to the right while baseband controls are placed above and below. The RF input is first split into in-phase (I) and quadrature (Q) components. The variable attenuators independently scale the I and Q components of the RF input. The attenuator outputs are then summed and buffered to the output.

By controlling the relative amounts of I and Q components that are summed, the AD8340 allows continuous magnitude and phase control of the gain. Consider the vector gain representation of the AD8340 expressed in polar form in Figure 27. The attenuation factors for the I and Q signal components are represented on the x- and y-axis, respectively, by the baseband inputs, V_{BBI} and V_{BBQ}. The resultant vector sum represents the vector gain, which can also be expressed as a magnitude and phase. By applying different combinations of baseband inputs, any vector gain within the unit circle can be programmed.

A change in sign of V_{BBI} or V_{BBQ} can be viewed as a change in sign of the gain or as a 180° phase change. The outermost circle represents the maximum gain magnitude of unity. The circle origin implies, in theory, a gain of 0. In practice, circuit mismatches and unavoidable signal feedthrough limit the minimum gain to approximately −40 dB. The phase angle between the resultant gain vector and the positive x-axis is defined as the phase shift. Note that there is a nominal, systematic insertion phase through the AD8340 to which the phase shift is added. In the following discussions, the systematic insertion phase is normalized to 0°.

The correspondence between the desired gain and phase setpoints, $Gain_{SP}$ and $Phase_{SP}$, and the Cartesian inputs, V_{BBI} and V_{BBQ}, is given by simple trigonometric identities.

$$Gain_{SP} = \sqrt{(V_{BBI} / V_O)^2 + (V_{BBQ} / V_O)^2}$$

$$Phase_{SP} = \arctan(V_{BBQ} / V_{BBI})$$

where:
V_O is the baseband scaling constant (500 mV).
V_{BBI} and V_{BBQ} are the differential I and Q baseband voltages, respectively.

Note that when evaluating the arctangent function, the proper phase quadrant must be selected. For example, if the principal value of the arctangent (known as the arctangent(x)) is used, Quadrant 2 and Quadrant 3 would be interpreted mistakenly as Quadrant 4 and Quadrant 1, respectively. In general, both V_{BBI} and V_{BBQ} are needed in concert to modulate the gain and the phase.

Pure amplitude modulation is represented by radial movement of the gain vector tip at a fixed angle, while pure phase modulation is represented by rotation of the tip around the circle at a fixed radius. Unlike traditional I-Q modulators, the AD8340 is designed to have a linear RF signal path from input to output. Traditional I-Q modulators provide a limited LO carrier path through which any amplitude information is removed.

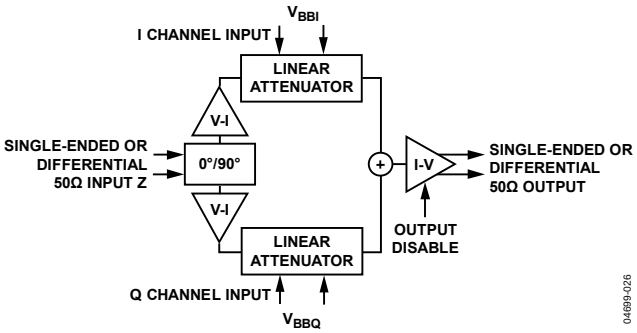


Figure 26. Simplified Architecture of the AD8340

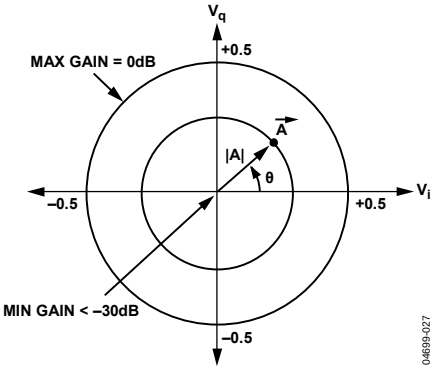


Figure 27. Vector Gain Representation

RF QUADRATURE GENERATOR

The RF input is directly coupled differentially or single-endedly to the quadrature generator, which consists of a multistage RC polyphase network tuned over the operating frequency range of 700 MHz to 1000 MHz. The recycling nature of the polyphase network generates two replicas of the input signal, which are in precise quadrature, that is, 90°, to each other. Because the passive network is perfectly linear, the amplitude and phase information contained in the RF input is transmitted faithfully to both channels. The quadrature outputs are then separately buffered to drive the respective attenuators. The characteristic impedance of the polyphase network is used to set the input impedance to the AD8340.

I-Q ATTENUATORS AND BASEBAND AMPLIFIERS

The proprietary linear-responding attenuator structure is an active solution with differential inputs and outputs that offer excellent linearity, low noise, and greater immunity from mismatches than other variable attenuator methods. The gain, in linear terms, of the I and Q channels is proportional to its control voltage with a scaling factor designed to be 2/V, that is, a full-scale gain setpoint of 1.0 (−2 dB) for $V_{BBI\,(Q)}$ of 500 mV. The control voltages can be driven differentially or single-endedly. The combination of the baseband amplifiers and attenuators allows for maximum modulation bandwidths in excess of 200 MHz.

OUTPUT AMPLIFIER

The output amplifier accepts the sum of the attenuator outputs and delivers a differential output signal into the external load. The output pins must be pulled up to an external supply, preferably through RF chokes. When the 50 Ω load is taken differentially, an OP1dB of 11 dBm and OIP3 of 24 dBm are achieved at 880 MHz. The output can be taken in single-ended fashion, albeit at lower performance levels.

NOISE AND DISTORTION

The output noise floor and distortion levels vary with the gain magnitude but do not vary significantly with the phase. At the higher gain magnitude setpoints, the OIP3 and the noise floor vary in direct proportion with the gain. At lower gain magnitude setpoints, the noise floor levels off while the OIP3 continues to vary with the gain.

GAIN AND PHASE ACCURACY

There are numerous ways to express the accuracy of the AD8340. Ideally, the gain and phase should precisely follow the setpoints. Figure 4 illustrates the gain error in decibels (dB) from a best fit line, normalized to the gain measured at the gain setpoint = 1.0, for the different phase setpoints. Figure 6 shows the gain error in a different form; the phase setpoint is swept from 0° to 360° for different gain setpoints. Figure 8 and Figure 22 show analogous errors for the phase error as a function of gain and phase setpoints. The accuracy clearly depends on the region of operation within the vector gain unit circle. Operation very close to the origin generally results in larger errors as the relative accuracy of the I and Q vectors degrades.

RF FREQUENCY RANGE

The frequency range on the RF input is limited by the internal polyphase quadrature phase-splitter. The phase-splitter splits the incoming RF input into two signals, 90° out of phase, as previously described in the RF Quadrature Generator section. This polyphase network has been designed to ensure robust quadrature accuracy over standard fabrication process parameter variations for the 700 MHz to 1 GHz specified RF frequency range. Using the AD8340 as a single-sideband modulator and measuring the resulting sideband suppression is a good gauge of how the quadrature accuracy is maintained over RF frequency. A typical plot of sideband suppression from 500 MHz to 1.5 GHz is shown in Figure 28. The level of sideband suppression degradation outside the 700 MHz to 1 GHz specified range is subject to manufacturing process variations.

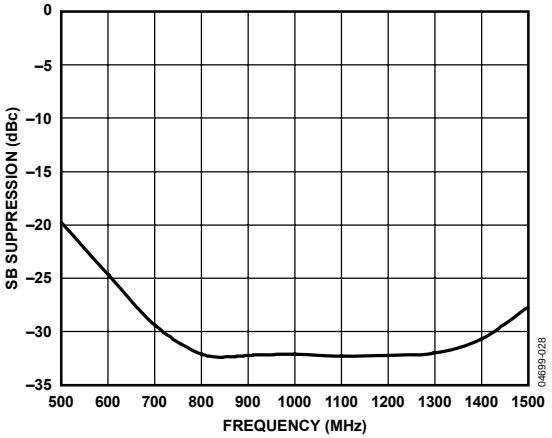


Figure 28. Sideband Suppression vs. Frequency

APPLICATIONS INFORMATION

USING THE AD8340

The AD8340 is designed to operate in a 50 Ω impedance system. Figure 30 illustrates where the RF input is driven in a single-ended fashion while the differential RF output is converted to a single-ended output with an RF balun. The baseband controls for the I and Q channels are typically driven from differential DAC outputs. The power supplies, VPRF and VPS2, should be bypassed appropriately with 0.1 µF and 100 pF capacitors. Low inductance grounding of the CMOP and CMRF common pins is essential to prevent unintentional peaking of the gain.

RF INPUT AND MATCHING

The input impedance of the AD8340 is defined by the characteristics of the polyphase network. The capacitive component of the network causes its impedance to roll off with frequency, albeit at a slower rate than 6 dB/octave. With matching inductors on the order of 5.6 nH in series with each of the RF inputs, RFIP and RFIM, a 50 Ω match is achieved with a return loss of >10 dB over the operating frequency range. Different matching inductors can improve matching over a narrower frequency range. The single-ended and differential input impedances are exactly the same.

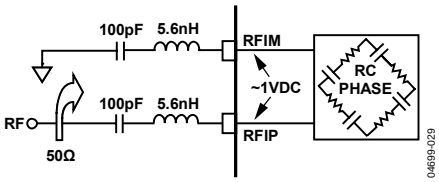


Figure 29. RF Input Interface to the AD8340 Showing Coupling Capacitors and Matching Inductors

The RFIP and RFIM should be ac-coupled through low loss series capacitors as shown in Figure 29. The internal dc levels are at approximately 1 V. For single-ended operation, one input is driven by the RF signal and the other input is ac grounded.

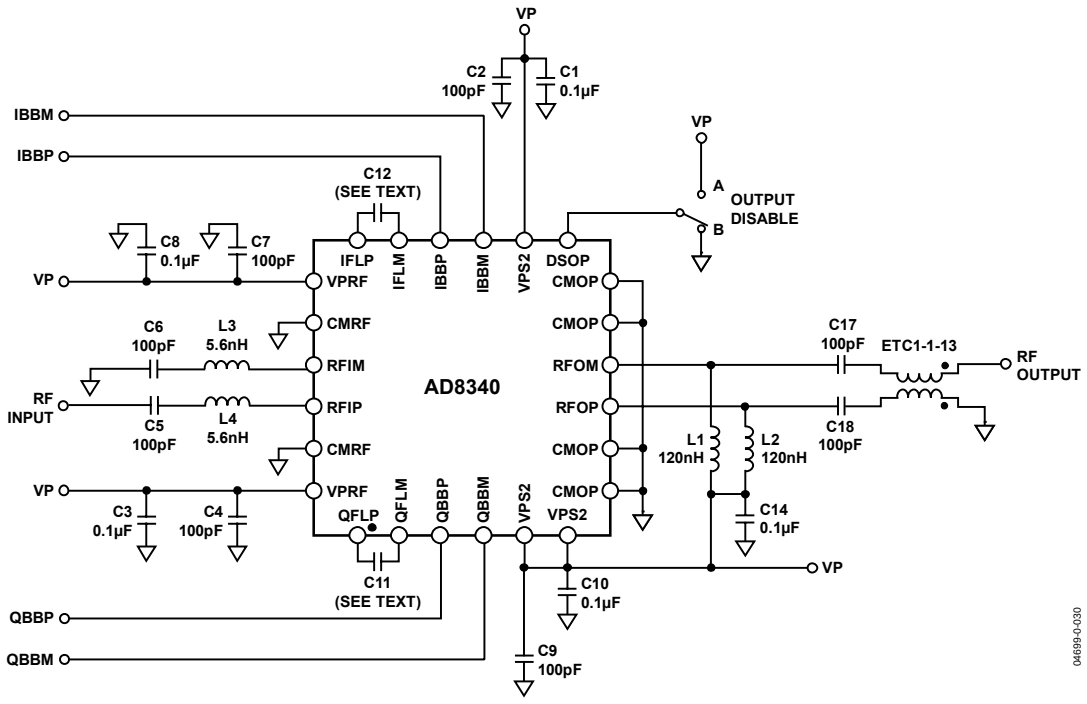


Figure 30. Basic Connections

RF OUTPUT AND MATCHING

The RF outputs of the AD8340, RFOP, and RFOM, are open collectors of a transimpedance amplifier that needs to be pulled up to the positive supply, preferably with RF chokes, as shown in Figure 31. The nominal output impedance looking into each individual output pin is 25 Ω. Consequently, the differential output impedance is 50 Ω.

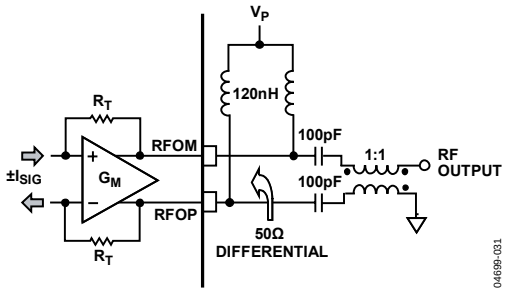


Figure 31. RF Output Interface to the AD8340 Showing Coupling Capacitors, Pull-Up RF Chokes, and Balun

Because the output dc levels are at the positive supply, ac coupling capacitors are usually needed between the AD8340 outputs and the next stage in the system.

A 1:1 RF broadband output balun, such as the ETC1-1-13 (M/A-COM), converts the differential output of the AD8340 into a single-ended signal. Note that the loss and balance of the balun directly impact the apparent output power, noise floor, and gain/phase errors of the AD8340. In critical applications, narrow-band baluns with low loss and superior balance are recommended.

If the output is taken in a single-ended fashion directly into a 50 Ω load through a coupling capacitor, there is an impedance mismatch. This can be resolved with a 1:2 balun to convert the single-ended 25 Ω output impedance to 50 Ω. If loss-of-signal swing is not critical, a 25 Ω back termination in series with the output pin can also be used. The unused output pin must still be pulled up to the positive supply. The user can load it through a coupling capacitor with a dummy load to preserve balance. The gain of the AD8340 when the output is single-ended varies slightly with the dummy load value, as shown in Figure 32.

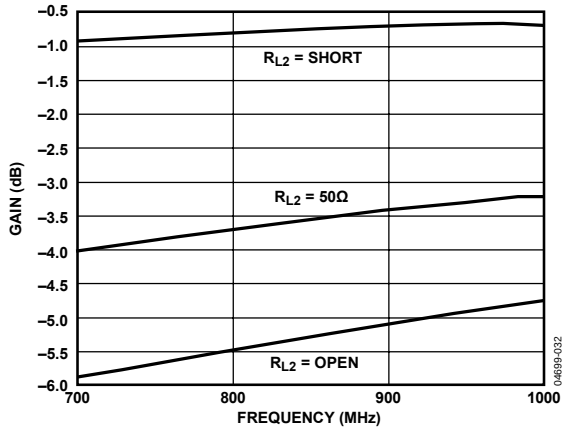


Figure 32. Gain of the AD8340 Using a Single-Ended Output with Different Dummy Loads, R_{L2} on the Unused Output

The RF output signal can be disabled by raising the DSOP pin to the positive supply. The shutdown function provides >40 dB attenuation of the input signal even at full gain. The interface to DSOP is high impedance, and the shutdown and turn-on response times are <100 ns. If the disable function is not needed, the DSOP should be tied to ground.

DRIVING THE I-Q BASEBAND CONTROLS

The I and Q inputs to the AD8340 set the gain and phase between input and output. These inputs are differential and should normally have a common-mode level of 0.5 V. However, when differentially driven, the common mode can vary from 250 mV to 750 mV while still allowing full gain control. Each input pair has a nominal input swing of ±0.5 V differential around the common-mode level. The maximum gain of unity is achieved if the differential voltage is equal to +500 mV or −500 mV. Therefore, with a common-mode level of 500 mV, IBBP and IBBM each swings between 250 mV and 750 mV.

The I and Q inputs can also be driven with a single-ended signal. In this case, one side of each input should be tied to a low noise 0.5 V voltage source (a 0.1 μF decoupling capacitor located close to the pin is recommended), while the other input swings from 0 V to 1 V. Differential drive generally offers superior even-order distortion and lower noise than single-ended drive.

The bandwidth of the baseband controls exceeds 200 MHz even at full-scale baseband drive. This allows for very fast gain and phase modulation of the RF input signal. In cases where lower modulation bandwidths are acceptable or desired, external filter capacitors can be connected across Pin IFLP to Pin IFLM, and across Pin QFLP to Pin QFLM, to reduce the ingress of baseband noise and spurious signal into the control path.

The 3 dB bandwidth is set by choosing C_{FLT} according to the following equation:

$$f_{3\,dB} \approx \frac{45\ \text{kHz} \times 10\ \text{nF}}{C_{EXTERNAL} + 0.5\ \text{pF}}$$

This equation has been verified for values of C_{FLT} from 10 pF to 0.1 μF (bandwidth settings of approximately 4.5 kHz to 43 MHz).

INTERFACING TO HIGH SPEED DACs

The AD977x family of dual DACs is well suited for driving the I and Q vector controls of the AD8340. While these inputs can in general be driven by any DAC, the differential outputs and bias level of the Analog Devices TxDAC® family allow for a direct connection between DAC and modulator.

The AD977x family of dual DACs has differential current outputs. The full-scale current is user programmable and is usually set to 20 mA, that is, each output swings from 0 mA to 20 mA.

The basic interface between the AD9777 DAC outputs and the AD8340 I and Q inputs is shown in Figure 33. The resistors R1 and R2 set the dc bias level according to the equation:

$$Bias\ Level = Average\ Output\ Current \times R1$$

For example, if the full-scale current from each output is 20 mA, each output will have an average current of 10 mA. Therefore, to set the bias level to the recommended 0.5 V, R1 and R2 should be set to 50 Ω each. R1 and R2 should always be equal.

If R3 is omitted, this results in an available swing from the DAC of 2 V p-p differential, which is twice the maximum voltage range required by the AD8340. DAC resolution can be maximized by adding R3, which scales down this voltage according to the following equation:

$$Full-Scale\ Swing = 2 \times I_{MAX}\left(R1 \left\| (R2+R3)\right.\right) \times \left(1 - \frac{R2}{R2+R3}\right)$$

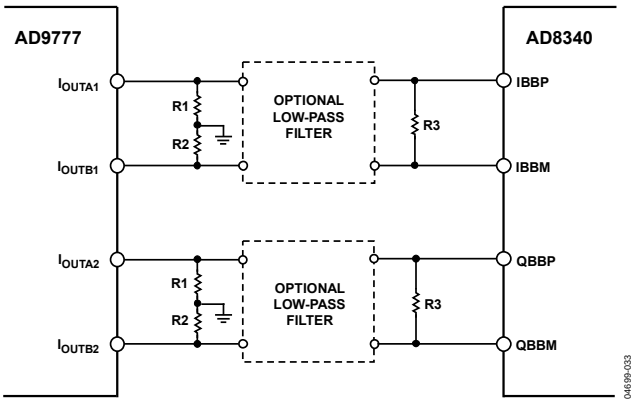


Figure 33. Basic AD9777 to AD8340 Interface

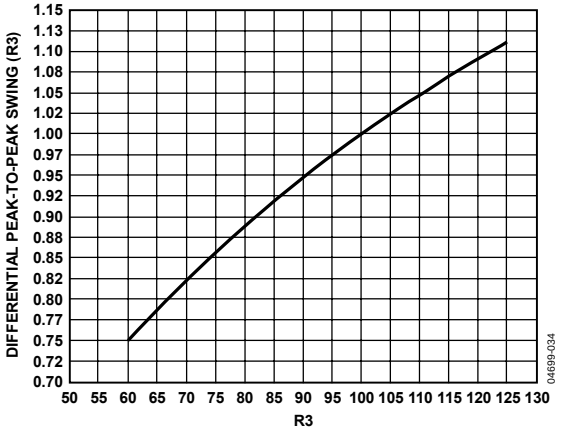


Figure 34. Peak-to-Peak DAC Output Swing vs. Swing Scaling Resistor R3 (R1 = R2 = 50 Ω)

Figure 34 shows the relationship between the value of R3 and the peak baseband voltage with R1 and R2 equal to 50 Ω. Figure 34 shows that a value of 100 Ω for R3 provides a peak-to-peak swing of 1 V p-p differential into the AD8340 I and Q inputs.

When using a DAC, low-pass image reject filters are typically used to eliminate the Nyquist images produced by the DAC. They also provide the added benefit of eliminating broadband noise that might feed into the modulator from the DAC.

CDMA2000 APPLICATION

To test the compliance to the CDMA2000 base station standard, a single-carrier CDMA2000 test model signal (forward pilot, sync, paging, and six traffic as per 3GPP2 C.S0010-B, Table 6.5.2.1) was applied to the AD8340. A cavity-tuned filter was used to reduce noise from the signal source being applied to the device. The 4.6 MHz pass band of this filter is apparent in the subsequent spectral plots (see Figure 35 to Figure 38).

Figure 35 shows a plot of the spectrum of the output signal under nominal conditions. P_{OUT} is equal to −5 dBm and $V_I = V_Q$ = 0.353 V, that is, VIBBP − VIBBM = VQBBP − VQBBM = 0.353 V. Adjacent channel power is measured in 30 kHz resolution bandwidth at 750 kHz and 1.98 MHz carrier offset. Noise floor is measured at ±4 MHz carrier offset.

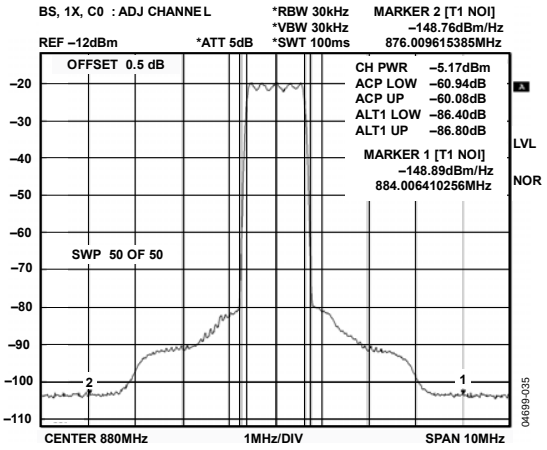


Figure 35. Output Spectrum, Single-Carrier CDMA2000 Test Model at −5 dBm $V_I = V_Q = 0.353$ V, ACP Measured at 750 kHz and 1.98 MHz Carrier Offset, Noise Measured at ±4 MHz Carrier Offset, Input Signal Filtered Using a Cavity Tuned Filter (Pass Band = 4.6 MHz)

Holding the I and Q control voltages steady at 0.353 V, input power was swept. Figure 36 shows the resulting output power, noise floor, and adjacent channel power ratio. Noise floor is presented as noise in a 1 MHz bandwidth as defined by the 3GPP2 specification.

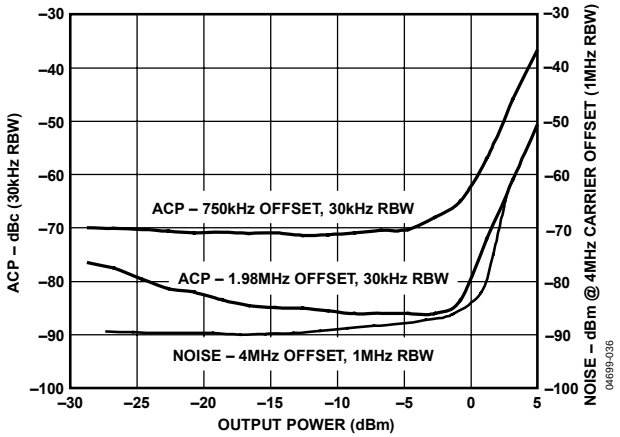


Figure 36. Noise and ACP vs. Output Power, Single-Carrier CDMA2000 Test Model, $V_I = V_Q = 0.353$, ACP Measured in 30 kHz RBW at ±750 kHz and ±1.98 MHz Carrier Offset, Noise Measured at ±4 MHz Carrier Offset

The results show that at an output power of 3 dBm, ACP is still in compliance with the standard (<−45 dBc @ 750 MHz and <−60 dBc @ 1.98 MHz). At low output power levels, ACP at 1.98 MHz, carrier offset degrades as the noise floor of the AD8340 becomes the dominant contributor to measured ACP. Measured noise at 4 MHz carrier offset begins to increase sharply above 0 dBm output power. This increase is not due to noise. but results from increased carrier-induced distortion. As output power drops below 0 dBm, the noise floor drops towards −90 dBm.

With a fixed input power of 2.4 dBm, the output power was again swept by exercising the I and Q inputs. V_I and V_Q were kept equal and were swept from 10 mV to 500 mV. The resulting output power, ACP, and noise floor are shown in Figure 37.

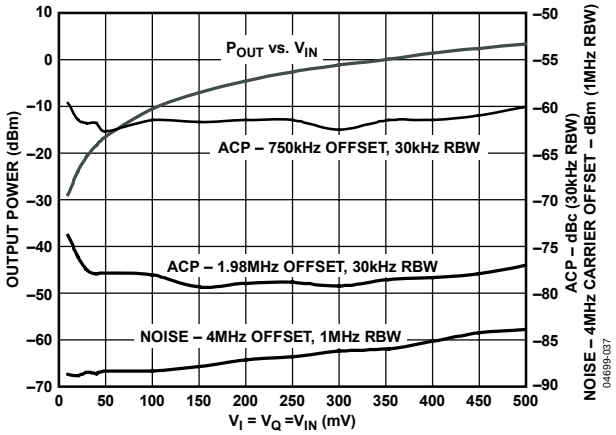


Figure 37. Output Power, Noise, and ACP vs. I and Q Control Voltages, CDMA2000 Test Model, $V_I = V_Q$, ACP Measured in 30 kHz RBW at ±750 kHz and ±1.98 MHz Carrier Offset, Noise Measured at ±4 MHz Carrier Offset

In contrast to Figure 36, Figure 37 shows that for a fixed input power, ACP remains fairly constant as gain and phase are changed (this is not true for very high input powers). The noise floor still drops with decreasing gain, but it never reaches the −90 dBm level shown in Figure 37.

Figure 38 shows the output spectrum for a 3-carrier CDMA2000 spectrum. Again, the signal being applied to the AD8340 is filtered by a cavity-tuned filter with a −3 dB bandwidth of 4.6 MHz. To reduce distortion, the total output carrier power was reduced to approximately −8 dBm (*per-carrier power* = −12.6 dBm). Adjacent channel power ratios of −61 dBc (2 MHz from center of spectrum) and −82 dBc (3.23 MHz from center of spectrum) were measured. The noise floor, measured at 5.25 MHz carrier offset, is approximately −149 dBm/Hz (−89 dBm in a 1 MHz bandwidth). While some dynamic range is lost due to output power back-off, ACP stays approximately equal and noise floor improves slightly.

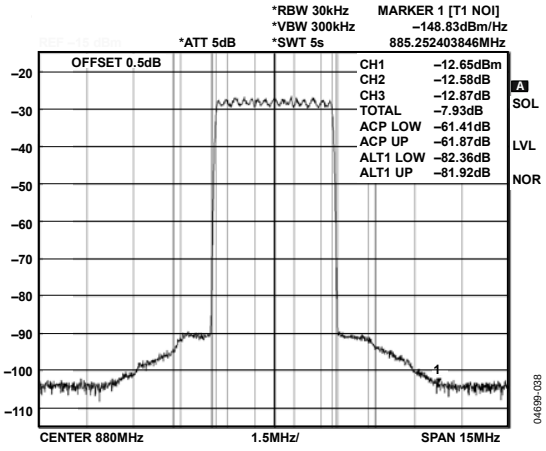


Figure 38. Output Spectrum, 3-Carrier CDMA2000 Test Model at −12.5 dBm/Carrier, $V_I = V_Q = 0.353$ V, ACP Measured at 2 MHz and 3.23 kHz Offset from Center of Spectrum, Noise Measured at 5.25 MHz Carrier Offset, Input Signal Filtered Using a Cavity-Tuned Filter (Pass Band = 4.6 MHz)

EVALUATION BOARD

The evaluation board circuit schematic for the AD8340 is shown in Figure 39.

The evaluation board is configured to be driven from a single-ended 50 Ω source. Although the input of the AD8340 is differential, it may be driven single-ended with no loss of performance.

The low-pass corner frequency of the baseband I and Q channels can be reduced by installing capacitors in the C11 and C12 positions. The low-pass corner frequency for either channel is approximated by

$$f_{3\,dB} \approx \frac{45\ kHz \times 10\ nF}{C_{EXTERNAL} + 0.5\ pF}$$

On the evaluation board, the I and Q baseband circuits are identical, so the following description applies equally to each. The connections and circuit configuration for the Q baseband inputs are described in Table 4.

The baseband input of the AD8340 requires a differential voltage drive. The evaluation board is set up to allow such a drive by connecting the differential voltage source to QBBP and QBBM. The common-mode voltage should be maintained at approximately 0.5 V. For this configuration, Jumper W1 to Jumper W4 should be removed.

The baseband input of the evaluation board can also be driven with a single-ended voltage. In this case, a bias level is provided to the unused input from Potentiometer R10 by installing either W1 or W2.

Setting SW1 in Position B disables the AD8340 output amplifier. With SW1 set to Position A, the output amplifier is enabled and an external voltage signal, such as a pulse, can be applied to the DSOP SMA connector to exercise the output amplifier enable/disable function.

Table 4. Evaluation Board Configuration Options

Components	Description	Default Conditions
R7, R9, R11, R14, R15, R19, R20, R21, C15, C19, W3, W4	I Channel Baseband Interface. Resistor R7 and Resistor R9 can be installed to accommodate a baseband source that requires a specific terminating impedance. C15 and C19 are bypass capacitors. For single-ended baseband drive, Potentiometer R11 can be used to provide a bias level to the unused input (install either W3 or W4).	R7, R9 = open R11 = potentiometer, 2 kΩ, 10 turns (Bourns) R14 = 4 kΩ (Size 0603) R15 = 44 kΩ (Size 0603) R19, R20, R21 = 0 Ω (Size 0603) C15, C19 = 0.1 µF (Size 0603) W3 = jumper (installed) W4 = jumper (open)
R1, R3, R10, R12, R13, R16, R17, R18, C16, C20, W1, W2	Q Channel Baseband Interface. See the I Channel Baseband Interface description.	R1, R3 = open R10 = potentiometer, 2 kΩ, 10 turns (Bourns) R12 = 4 kΩ (Size 0603) R13 = 44 kΩ (Size 0603) R16, R17, R18 = 0 Ω (Size 0603) C16, C20 = 0.1 µF (Size 0603) W1 = jumper (installed) W2 = jumper (open)
C11, C12	Baseband Low-Pass Filtering. By adding Capacitor C11 between QFLP and QFLM, and Capacitor C12 between IFLP and IFLM, the 3 dB low-pass corner frequency of the baseband interface can be reduced from 230 MHz (nominal). See the equation in the Evaluation Board section.	C11, C12 = open
T1, C17, C18, L1, L2	Output Interface. The 1:1 balun transformer, T1, converts the 50 Ω differential output to 50 Ω single-ended. C17 and C18 are dc blocks. L1 and L2 provide dc bias for the output.	C17, C18 = 100 pF (Size 0603) T1 = ETC1-1-13 (M/A-COM) L1, L2 = 120 nH (Size 0603)
L3, L4, C5, C6	Input Interface. The input impedance of the AD8340 requires 5.6 nH inductors in series with RFIP and RFIM for optimum return loss when driven by a single-ended 50 Ω line. C5 and C6 are dc blocks.	L3, L4 = 5.6 nH (Size 0402) C5, C6 = 100 pF (Size 0603)
C2, C4, C7, C9, C14, C1, C3, C8, C10, R2, R4, R5, R6	Supply Decoupling.	C2, C4, C7, C9 = open (Size 0603) C1, C3, C8, C10, C14 = 0.1 µF (Size 0603) R2, R4, R5, R6 = 0 Ω (Size 0603)
R8, SW1	Output Disable Interface. The output stage of the AD8340 is disabled by applying a high voltage to the DSOP pin by moving SW1 to Position B. The output stage is enabled by moving SW1 to Position A. The output disable function can also be exercised by applying an external high or low voltage to the DSOP SMA connector with SW1 in Position A.	R8 = 10 kΩ (Size 0603) SW1 = SPDT (Position A, output enabled)

SCHEMATIC AND ARTWORK

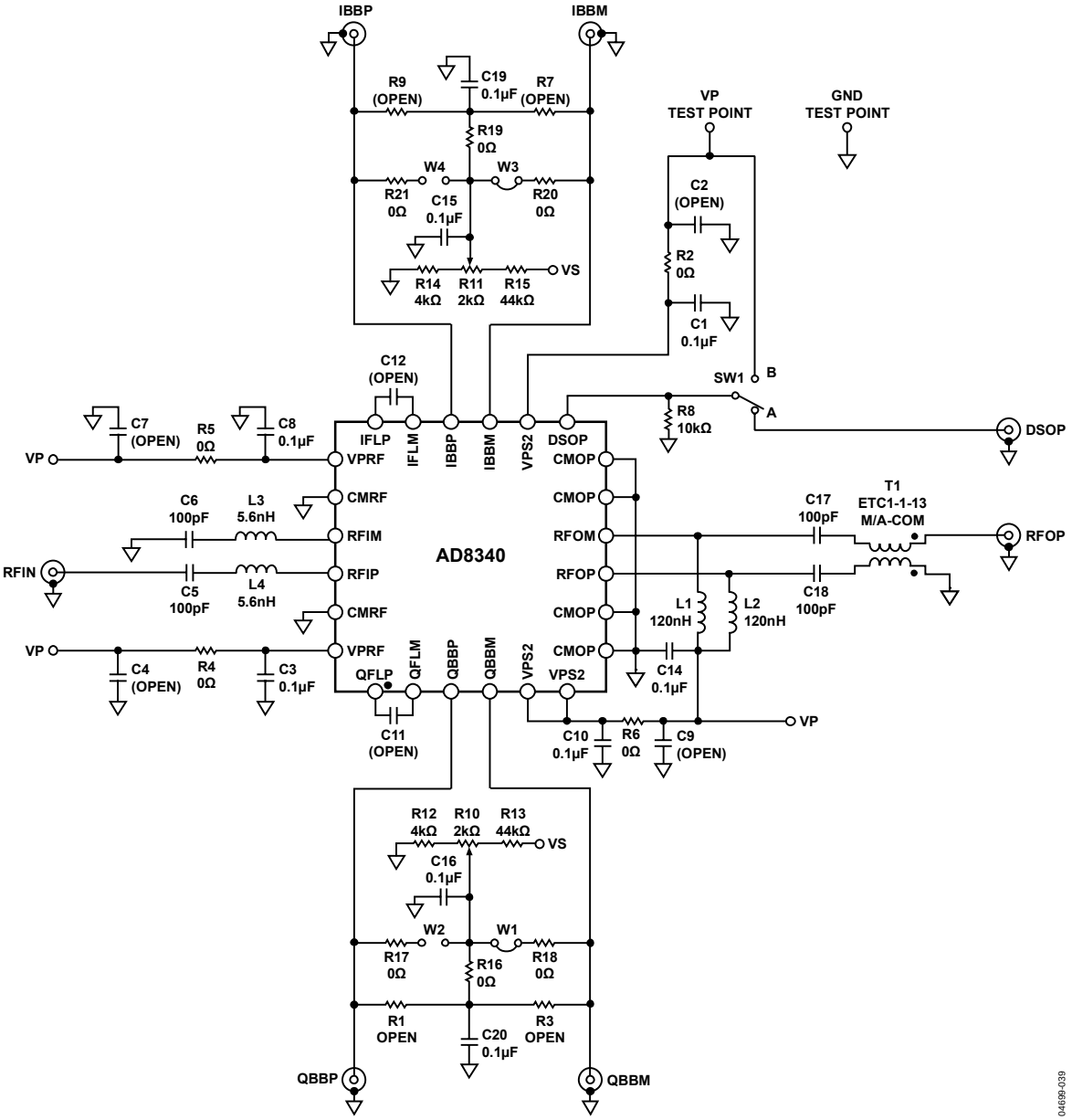


Figure 39. Evaluation Board Schematic

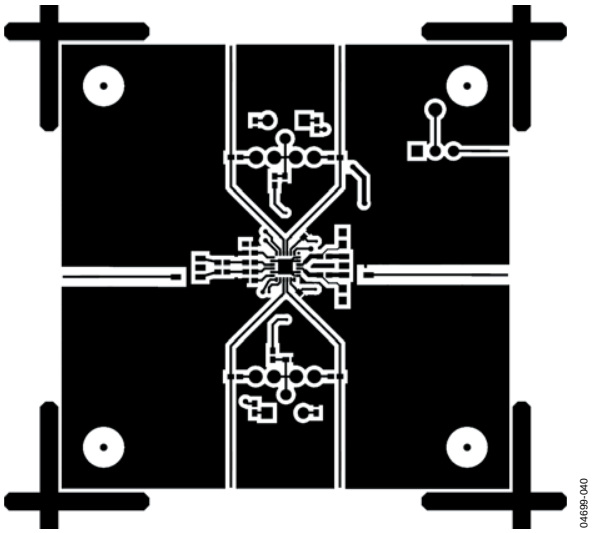


Figure 40. Component Side Layout

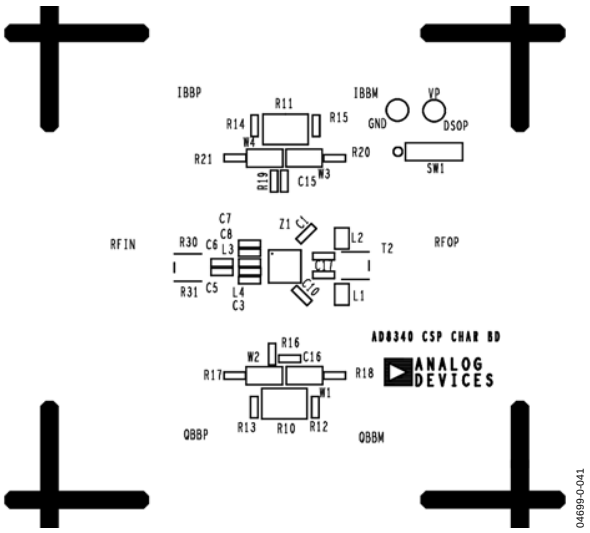
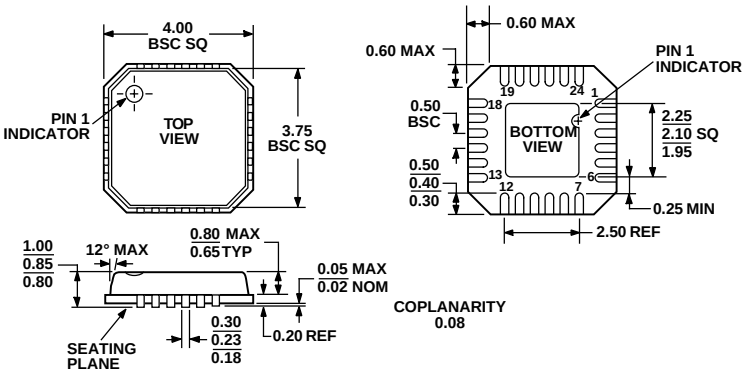


Figure 41. Component Side Silkscreen

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-2

Figure 42. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-24-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
AD8340ACPZ-WP[1, 2]	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-24-1	64
AD8340ACPZ-REEL7[1]	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-24-1	1,500
AD8340-EVALZ[1]		Evaluation Board		1

[1] Z = RoHS Compliant Part.
[2] WP = Waffle pack.

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D04699-0-8/07(B)

700 MHz to 2.7 GHz Quadrature Demodulator

Data Sheet

ADL5382

FEATURES

Operating RF and LO frequency: 700 MHz to 2.7 GHz
Input IP3
33.5 dBm @ 900 MHz
30.5 dBm @1900 MHz
Input IP2: >70 dBm @ 900 MHz
Input P1dB: 14.7 dBm @ 900 MHz
Noise figure (NF)
14.0 dB @ 900 MHz
15.6 dB @ 1900 MHz
Voltage conversion gain: ~4 dB
Quadrature demodulation accuracy
Phase accuracy: ~0.2°
Amplitude balance: ~0.05 dB
Demodulation bandwidth: ~370 MHz
Baseband I/Q drive: 2 V p-p into 200 Ω
Single 5 V supply

FUNCTIONAL BLOCK DIAGRAM

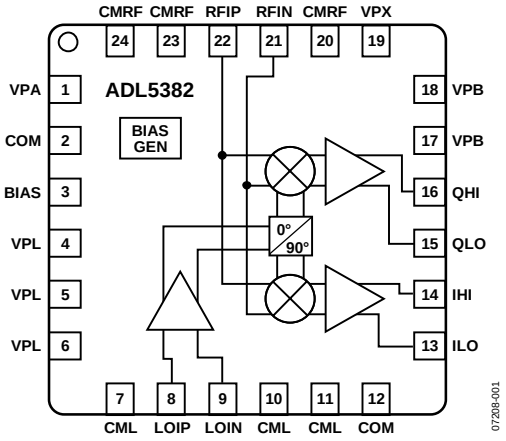

Figure 1.

APPLICATIONS

Cellular W-CDMA/CDMA/CDMA2000/GSM
Microwave point-to-(multi)point radios
Broadband wireless and WiMAX

GENERAL DESCRIPTION

The ADL5382 is a broadband quadrature I-Q demodulator that covers an RF input frequency range from 700 MHz to 2.7 GHz. With a NF = 14 dB, IP1dB = 14.7 dBm, and IIP3 = 33.5 dBm at 900 MHz, the ADL5382 demodulator offers outstanding dynamic range suitable for the demanding infrastructure direct-conversion requirements. The differential RF inputs provide a well-behaved broadband input impedance of 50 Ω and are best driven from a 1:1 balun for optimum performance.

Excellent demodulation accuracy is achieved with amplitude and phase balances ~0.05 dB and ~0.2°, respectively. The demodulated in-phase (I) and quadrature (Q) differential outputs are fully buffered and provide a voltage conversion gain of ~4 dB. The buffered baseband outputs are capable of driving a 2 V p-p differential signal into 200 Ω.

The fully balanced design minimizes effects from second-order distortion. The leakage from the LO port to the RF port is <−65 dBc. Differential dc offsets at the I and Q outputs are typically <10 mV. Both of these factors contribute to the excellent IIP2 specifications which is >60 dBm.

The ADL5382 operates off a single 4.75 V to 5.25 V supply. The supply current is adjustable with an external resistor from the BIAS pin to ground.

The ADL5382 is fabricated using the Analog Devices, Inc., advanced Silicon-Germanium bipolar process and is available in a 24-lead exposed paddle LFCSP.

Rev. A
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REVISION HISTORY

5/12—Rev. 0 to Rev. A

Added θ_{JC} = 3°C/W to Table 2 ... 5
Added EPAD Note to Figure 2 ... 6
Updated Outline Dimensions ... 27

3/08—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, f_{LO} = 900 MHz, f_{IF} = 4.5 MHz, P_{LO} = 0 dBm, BIAS pin open, Z_O = 50 Ω, unless otherwise noted. Baseband outputs differentially loaded with 450 Ω. Loss of the balun used to drive the RF port was de-embedded from these measurements.

Table 1.

Parameter	Condition	Min	Typ	Max	Unit
OPERATING CONDITIONS					
LO and RF Frequency Range		0.7		2.7	GHz
LO INPUT	LOIP, LOIN				
Input Return Loss	LO driven differentially through a balun at 900 MHz		−11		dB
LO Input Level		−6	0	+6	dBm
I/Q BASEBAND OUTPUTS	QHI, QLO, IHI, ILO				
Voltage Conversion Gain	450 Ω differential load on I and Q outputs at 900 MHz		3.9		dB
	200 Ω differential load on I and Q outputs at 900 MHz		3.0		dB
Demodulation Bandwidth	1 V p-p signal, 3 dB bandwidth		370		MHz
Quadrature Phase Error	At 900 MHz		0.2		Degrees
I/Q Amplitude Imbalance			0.05		dB
Output DC Offset (Differential)	0 dBm LO input at 900 MHz		±5		mV
Output Common Mode			VPOS − 2.8		V
0.1 dB Gain Flatness			50		MHz
Output Swing	Differential 200 Ω load		2		V p-p
Peak Output Current	Each pin		12		mA
POWER SUPPLIES	VPA, VPL, VPB, VPX				
Voltage		4.75		5.25	V
Current	BIAS pin open		220		mA
	R_{BIAS} = 4 kΩ		196		mA
DYNAMIC PERFORMANCE at RF = 900 MHz					
Conversion Gain			3.9		dB
Input P1dB			14.7		dBm
Second-Order Input Intercept (IIP2)	−5 dBm each input tone		73		dBm
Third-Order Input Intercept (IIP3)	−5 dBm each input tone		33.5		dBm
LO to RF	RFIN, RFIP terminated in 50 Ω		−92		dBm
RF to LO	LOIN, LOIP terminated in 50 Ω		−89		dBc
IQ Magnitude Imbalance			0.05		dB
IQ Phase Imbalance			0.2		Degrees
LO to IQ	RFIN, RFIP terminated in 50 Ω		−43		dBm
Noise Figure			14.0		dB
Noise Figure under Blocking Conditions	With a −5 dBm interferer 5 MHz away		19.9		dB
DYNAMIC PERFORMANCE at RF = 1900 MHz					
Conversion Gain			3.9		dB
Input P1dB			14.4		dBm
Second-Order Input Intercept (IIP2)	−5 dBm each input tone		65		dBm
Third-Order Input Intercept (IIP3)	−5 dBm each input tone		30.5		dBm
LO to RF	RFIN, RFIP terminated in 50 Ω		−71		dBm
RF to LO	LOIN, LOIP terminated in 50 Ω		−78		dBc
IQ Magnitude Imbalance			0.05		dB
IQ Phase Imbalance			0.2		Degrees
LO to IQ	RFIN, RFIP terminated in 50 Ω		−41		dBm
Noise Figure			15.6		dB
Noise Figure under Blocking Conditions	With a −5 dBm interferer 5 MHz away		20.5		dB

Parameter	Condition	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE at RF = 2700 MHz	RFIP, RFIN				
Conversion Gain			3.3		dB
Input P1dB			14.5		dBm
Second-Order Input Intercept (IIP2)	−5 dBm each input tone		52		dBm
Third-Order Input Intercept (IIP3)	−5 dBm each input tone		28.3		dBm
LO to RF	RFIN, RFIP terminated in 50 Ω, 1xLO appearing at RF port		−70		dBm
RF to LO	LOIN, LOIP terminated in 50 Ω		−55		dBc
IQ Magnitude Imbalance			0.16		dB
IQ Phase Imbalance			0.1		Degrees
LO to IQ	RFIN, RFIP terminated in 50 Ω, 1xLO appearing at BB port		−42		dBm
Noise Figure			17.6		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (VPA, VPL, VPB, VPX)	5.5 V
LO Input Power	13 dBm (re: 50 Ω)
RF Input Power	15 dBm (re: 50 Ω)
Internal Maximum Power Dissipation	1230 mW
θ_{JA}	54°C/W
θ_{JC}	3°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

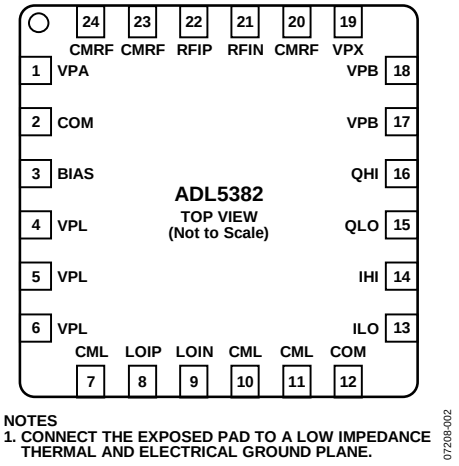

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4 to 6, 17 to 19	VPA, VPL, VPB, VPX	Supply. Positive supply for LO, IF, biasing, and baseband sections. These pins should be decoupled to the board ground using appropriate-sized capacitors.
2, 7, 10 to 12, 20, 23, 24	COM, CML, CMRF	Ground. Connect to a low impedance ground plane.
3	BIAS	Bias Control. A resistor (R_{BIAS}) can be connected between BIAS and COM to reduce the mixer core current. The default setting for this pin is open.
8, 9	LOIP, LOIN	Local Oscillator Input. Pins must be ac-coupled. A differential drive through a balun (recommended balun is the M/A-COM ETC1-1-13) is necessary to achieve optimal performance.
13 to 16	ILO, IHI, QLO, QHI	I Channel and Q Channel Mixer Baseband Outputs. These outputs have a 50 Ω differential output impedance (25 Ω per pin). The bias level on these pins is equal to VPOS − 2.8 V. Each output pair can swing 2 V p-p (differential) into a load of 200 Ω. Output 3 dB bandwidth is 370 MHz.
21, 22	RFIN, RFIP	RF Input. A single-ended 50 Ω signal can be applied to the RF inputs through a 1:1 balun (recommended balun is the M/A-COM ETC1-1-13). Ground-referenced inductors must also be connected to RFIP and RFIN (recommended values = 33 nH).
	EP	Exposed Paddle. Connect to a low impedance thermal and electrical ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, LO drive level = 0 dBm, R_{BIAS} = open, RF input balun loss is de-embedded, unless otherwise noted.

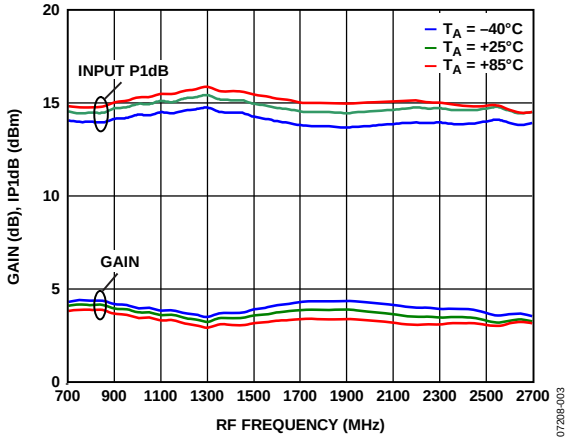

Figure 3. Conversion Gain and Input IP1 dB Compression Point (IP1dB) vs. RF Frequency

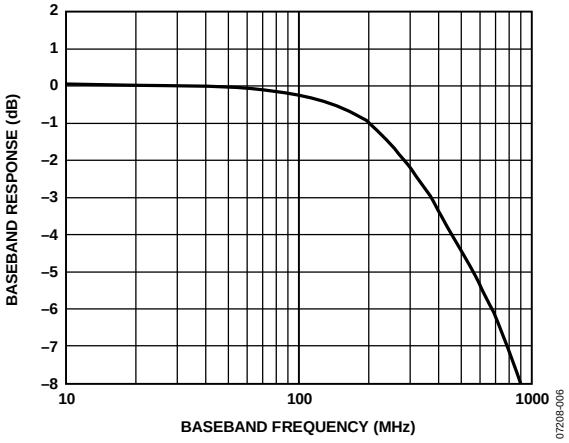

Figure 6. Normalized IQ Baseband Frequency Response

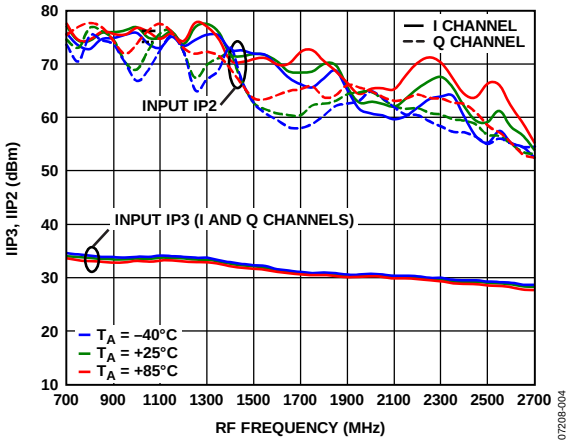

Figure 4. Input Third-Order Intercept (IIP3) and Input Second-Order Intercept Point (IIP2) vs. RF Frequency

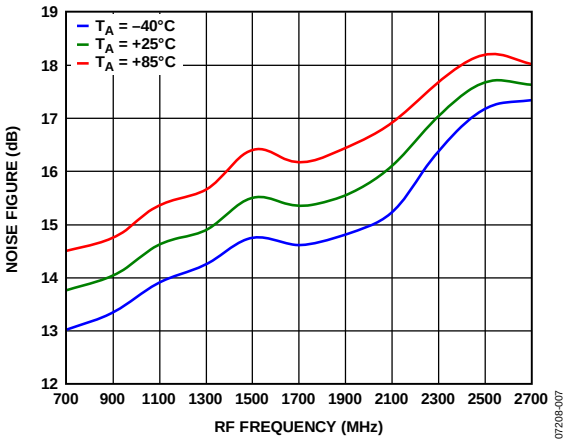

Figure 7. Noise Figure vs. RF Frequency

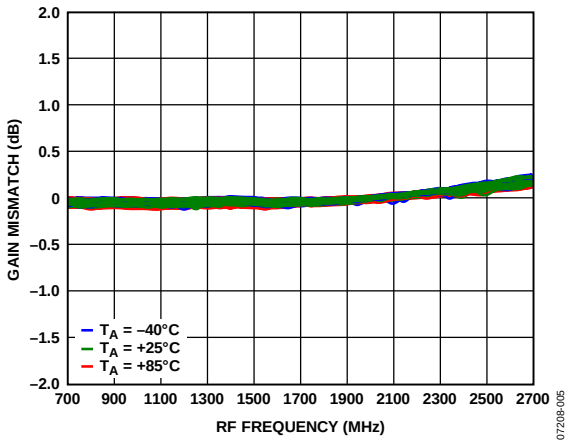

Figure 5. IQ Gain Mismatch vs. RF Frequency

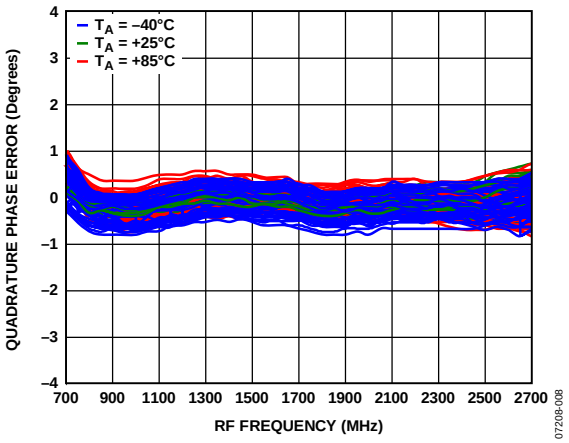

Figure 8. IQ Quadrature Phase Error vs. RF Frequency

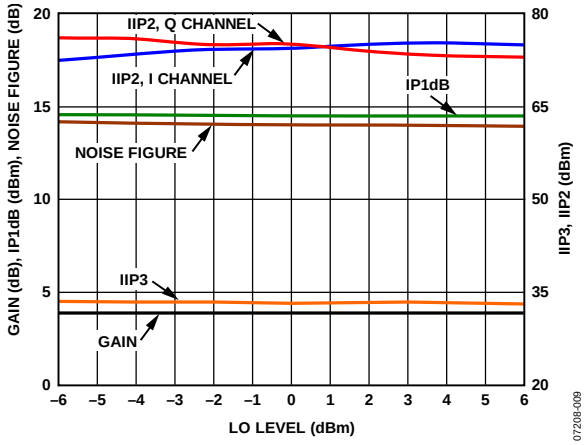

Figure 9. Conversion Gain, IP1dB, Noise Figure, IIP3, and IIP2 vs. LO Level, f_{RF} = 900 MHz

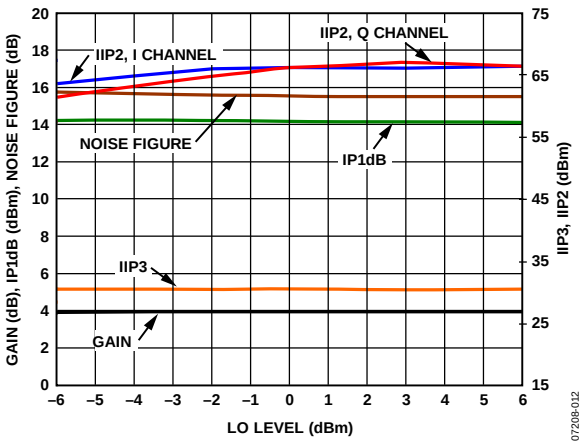

Figure 12. Conversion Gain, IP1dB, Noise Figure, IIP3, and IIP2 vs. LO Level, f_{RF} = 1900 MHz

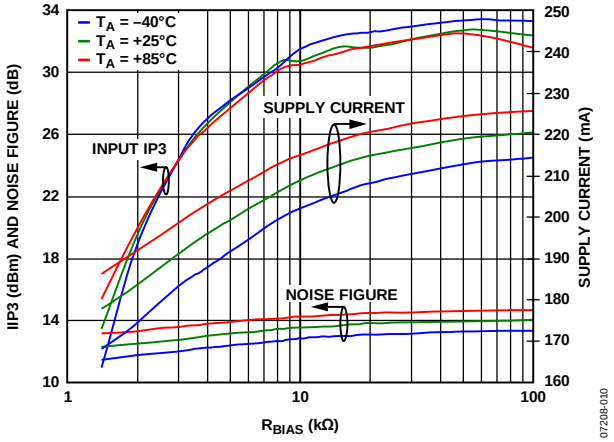

Figure 10. IIP3, Noise Figure, and Supply Current vs. R_{BIAS}, f_{RF} = 900 MHz

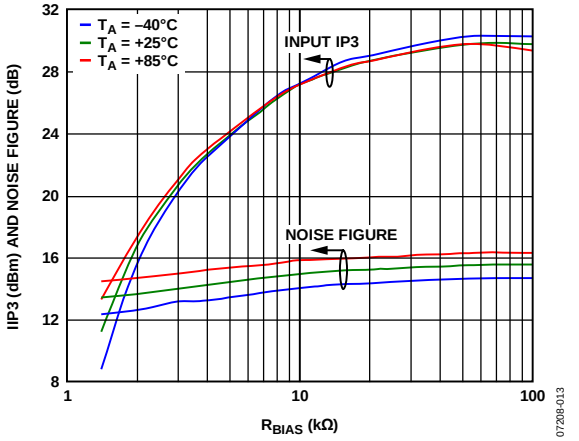

Figure 13. IIP3 and Noise Figure vs. R_{BIAS}, f_{RF} = 1900 MHz

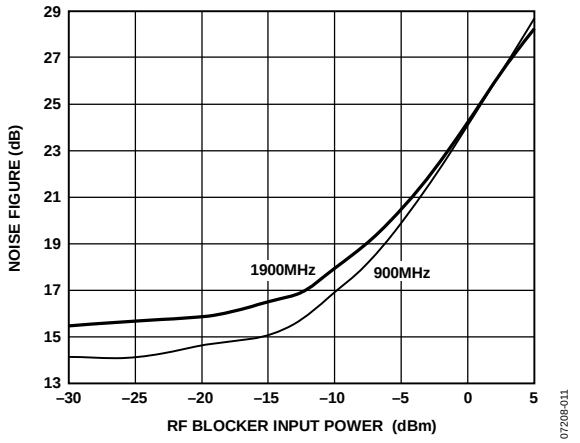

Figure 11. Noise Figure vs. Input Blocker Level, f_{RF} = 900 MHz, 1900 MHz (RF Blocker 5 MHz Offset)

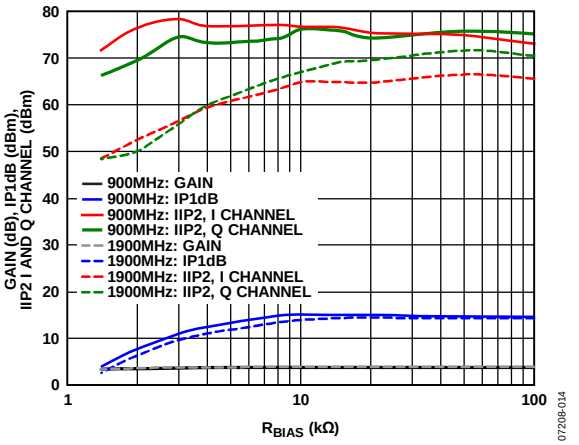

Figure 14. Conversion Gain, IP1dB, IIP2_I, and IIP2_Q vs. R_{BIAS}, f_{RF} = 900 MHz, 1900MHz

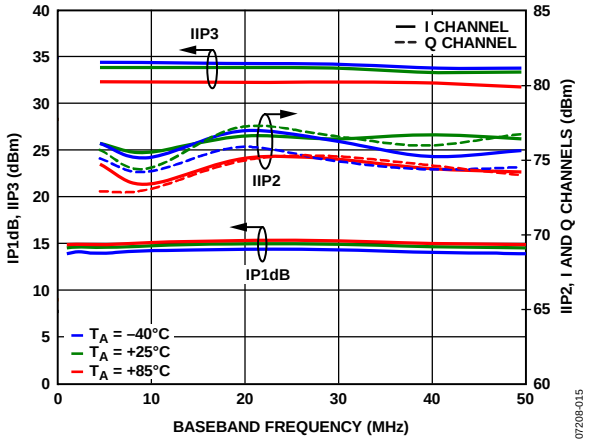

Figure 15. IP1dB, IIP3, and IIP2 vs. Baseband Frequency

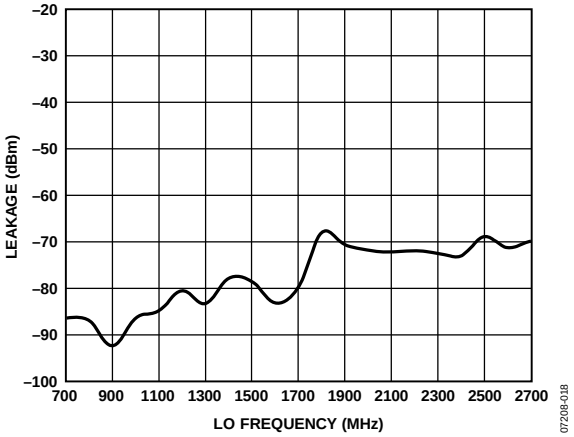

Figure 18. LO-to-RF Leakage vs. LO Frequency

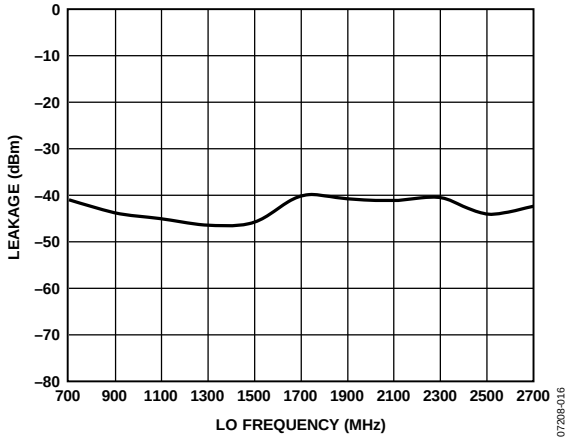

Figure 16. LO-to-BB Leakage vs. LO Frequency

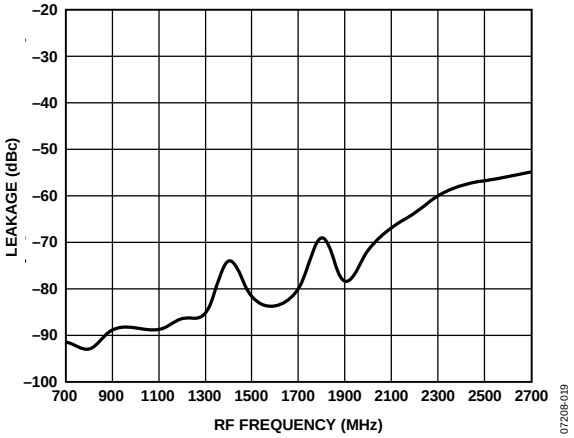

Figure 19. RF-to-LO Leakage vs. RF Frequency

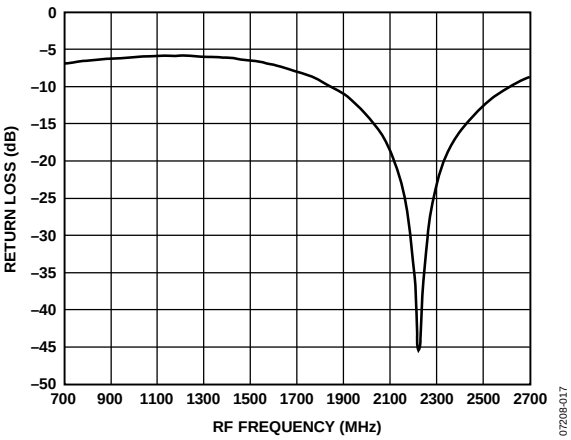

Figure 17. RF Port Return Loss vs. RF Frequency Measured on a Characterization Board through an ETC1-1-13 Balun with 33 nH Bias Inductors

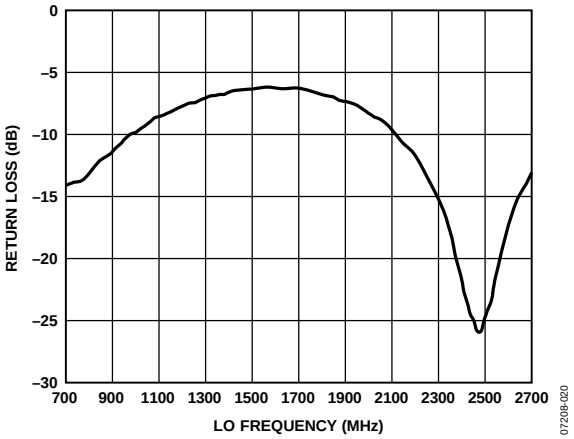

Figure 20. LO Port Return Loss vs. LO Frequency Measured on Characterization Board through an ETC1-1-13 Balun

DISTRIBUTIONS FOR f_{RF} = 900 MHz

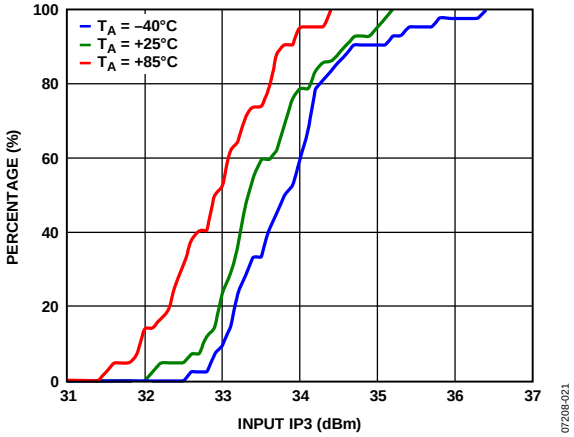

Figure 21. IIP3 Distributions, f_{RF} = 900 MHz

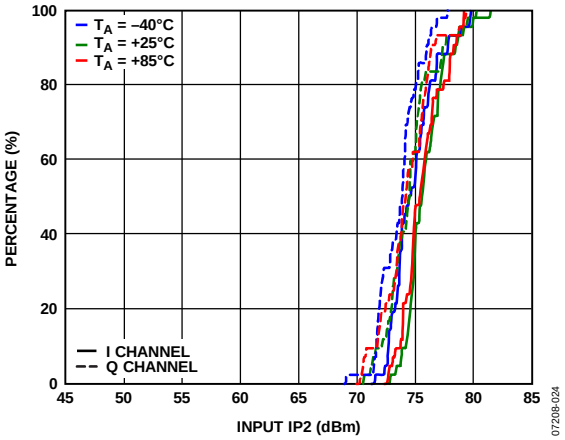

Figure 24. IIP2 Distributions for I Channel and Q Channel, f_{RF} = 900 MHz

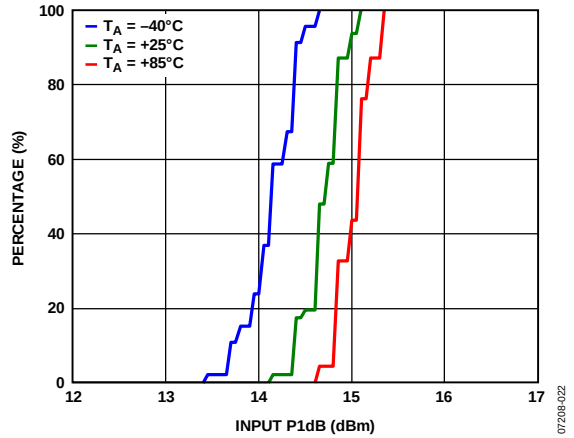

Figure 22. IP1dB Distributions, f_{RF} = 900 MHz

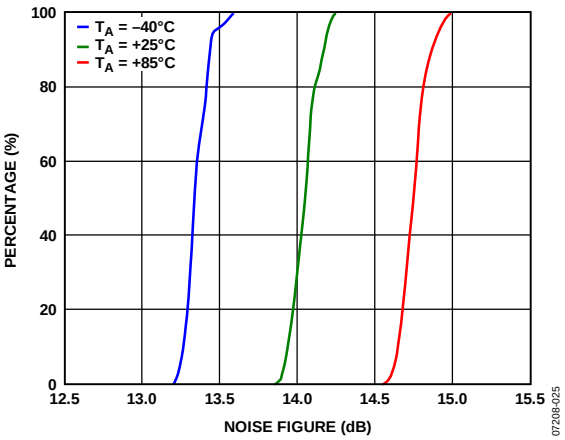

Figure 25. Noise Figure Distributions, f_{RF} = 900 MHz

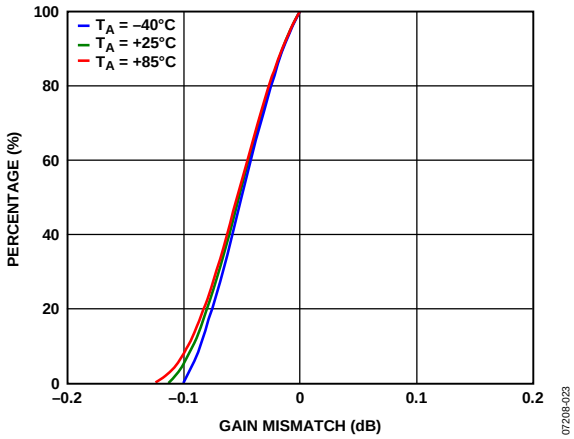

Figure 23. IQ Gain Mismatch Distributions, f_{RF} = 900 MHz

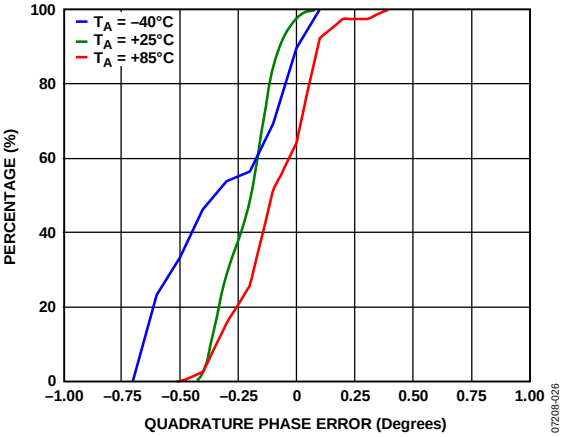

Figure 26. IQ Quadrature Phase Error Distributions, f_{RF} = 900 MHz

DISTRIBUTIONS FOR f_{RF} = 1900 MHz

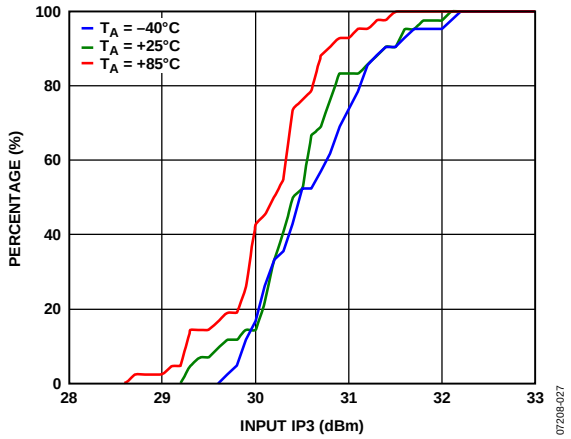

Figure 27. IIP3 Distributions, f_{RF} = 1900 MHz

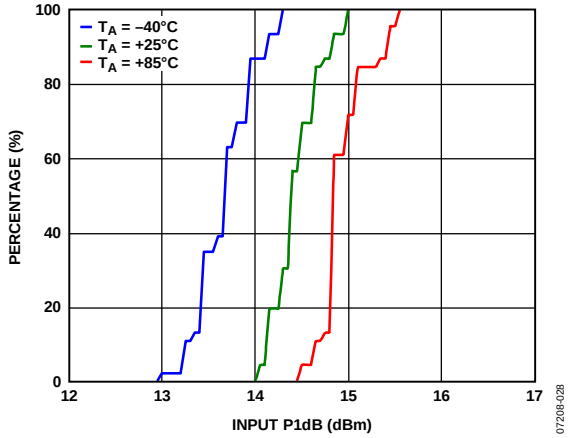

Figure 28. IP1dB Distributions, f_{RF} = 1900 MHz

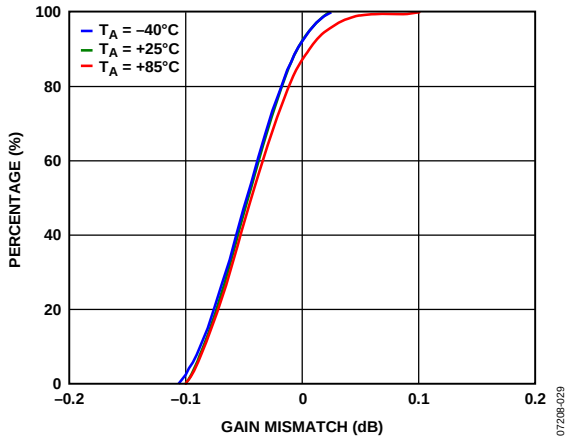

Figure 29. IQ Gain Mismatch Distributions, f_{RF} = 1900 MHz

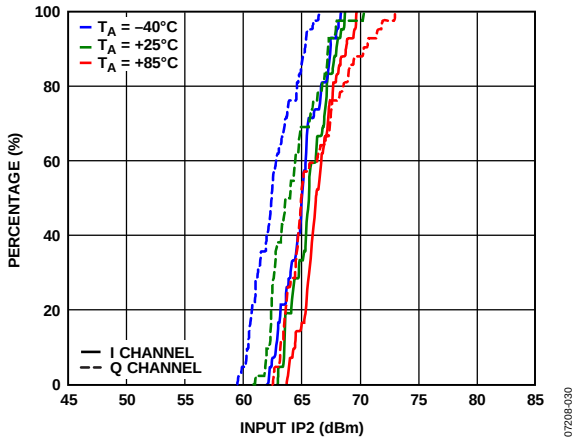

Figure 30. IIP2 Distributions for I Channel and Q Channel, f_{RF} = 1900 MHz

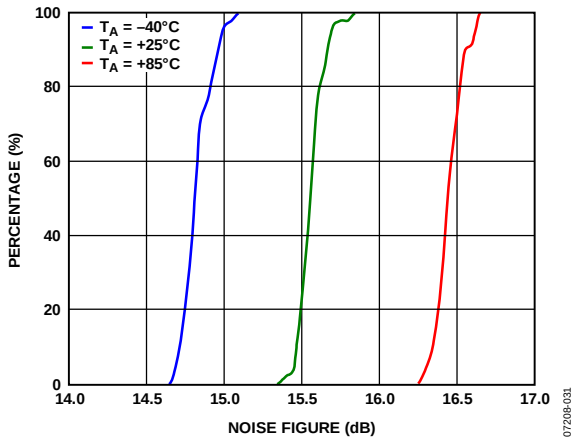

Figure 31. Noise Figure Distributions, f_{RF} = 1900 MHz

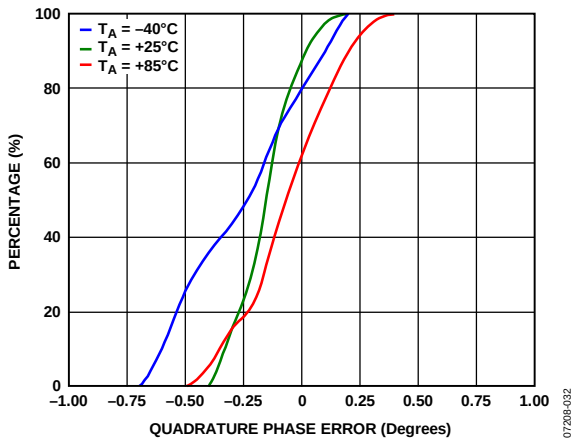

Figure 32. IQ Quadrature Phase Error Distributions, f_{RF} = 1900 MHz

DISTRIBUTIONS FOR f_{RF} = 2700 MHz

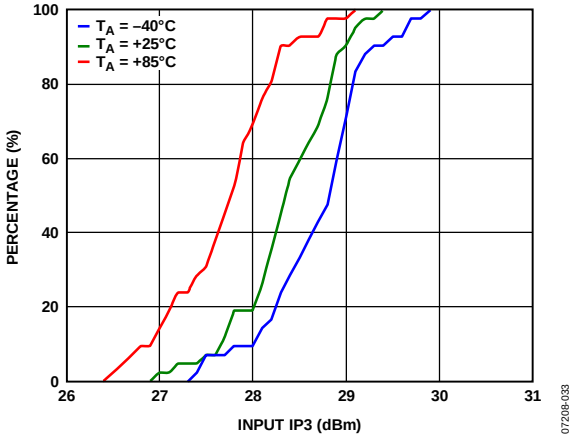

Figure 33. IIP3 Distributions, f_{RF} = 2700 MHz

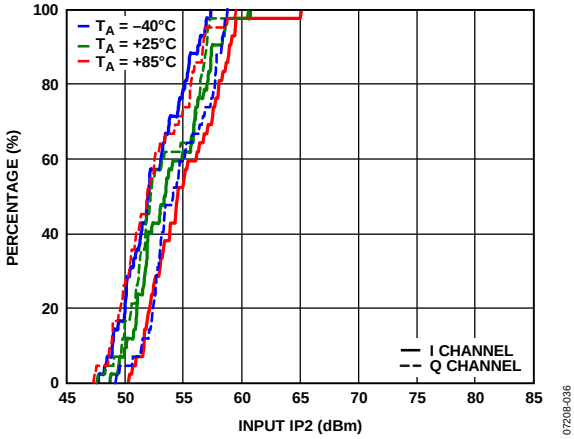

Figure 36. IIP2 Distributions for I Channel and Q Channel, f_{RF} = 2700 MHz

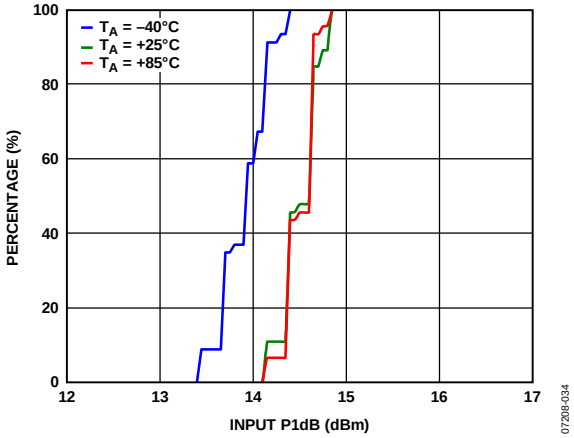

Figure 34. IP1dB Distributions, f_{RF} = 2700 MHz

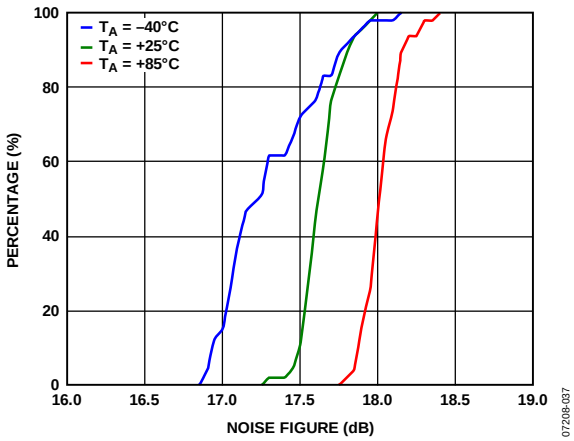

Figure 37. Noise Figure Distributions, f_{RF} = 2700 MHz

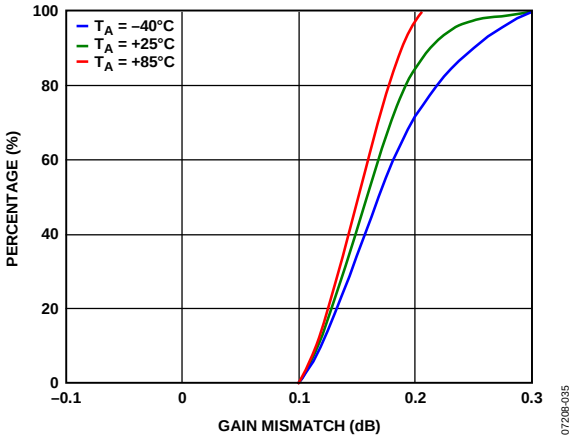

Figure 35. IQ Gain Mismatch Distributions, f_{RF} = 2700 MHz

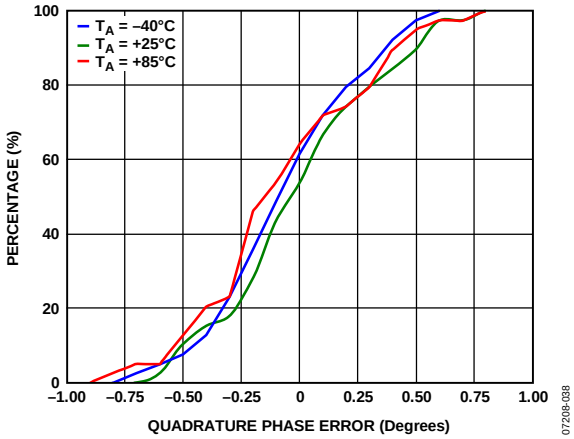

Figure 38. IQ Quadrature Phase Error Distributions, f_{RF} = 2700 MHz

CIRCUIT DESCRIPTION

The ADL5382 can be divided into five sections: the local oscillator (LO) interface, the RF voltage-to-current (V-to-I) converter, the mixers, the differential emitter follower outputs, and the bias circuit. A detailed block diagram of the device is shown in Figure 39.

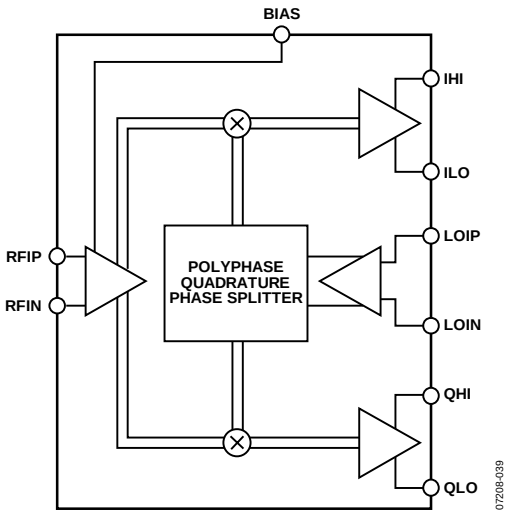

Figure 39. Block Diagram

The LO interface generates two LO signals at 90° of phase difference to drive two mixers in quadrature. RF signals are converted into currents by the V-to-I converters that feed into the two mixers. The differential I and Q outputs of the mixers are buffered via emitter followers. Reference currents to each section are generated by the bias circuit. A detailed description of each section follows.

LO INTERFACE

The LO interface consists of a polyphase quadrature splitter followed by a limiting amplifier. The LO input impedance is set by the polyphase, which splits the LO signal into two differential signals in quadrature. Each quadrature LO signal then passes through a limiting amplifier that provides the mixer with a limited drive signal. For optimal performance, the LO inputs must be driven differentially.

V-TO-I CONVERTER

The differential RF input signal is applied to a resistively degenerated common base stage, which converts the differential input voltage to output currents. The output currents then modulate the two half frequency LO carriers in the mixer stage.

MIXERS

The ADL5382 has two double-balanced mixers: one for the in-phase channel (I channel) and one for the quadrature channel (Q channel). These mixers are based on the Gilbert cell design of four cross-connected transistors. The output currents from the two mixers are summed together in the resistive loads that then feed into the subsequent emitter follower buffers.

EMITTER FOLLOWER BUFFERS

The output emitter followers drive the differential I and Q signals off-chip. The output impedance is set by on-chip 25 Ω series resistors that yield a 50 Ω differential output impedance for each baseband port. The fixed output impedance forms a voltage divider with the load impedance that reduces the effective gain. For example, a 500 Ω differential load has 1 dB lower effective gain than a high (10 kΩ) differential load impedance.

BIAS CIRCUIT

A band gap reference circuit generates the proportional-to-absolute temperature (PTAT) as well as temperature-independent reference currents used by different sections. The mixer current can be reduced via an external resistor between the BIAS pin and ground. When the BIAS pin is open, the mixer runs at maximum current and therefore the greatest dynamic range. The mixer current can be reduced by placing a resistance to ground; therefore, reducing overall power consumption, noise figure, and IIP3. The effect on each of these parameters is shown in Figure 10, Figure 13, and Figure 14.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 41 shows the basic connections schematic for the ADL5382.

POWER SUPPLY

The nominal voltage supply for the ADL5382 is 5 V and is applied to the VPA, VPB, VPL, and VPX pins. Ground should be connected to the COM, CML, and CMRF pins. The exposed paddle on the underside of the package should also be soldered to a low thermal and electrical impedance ground plane. If the ground plane spans multiple layers on the circuit board, these layers should be stitched together with nine vias under the exposed paddle. The Application Note AN-772 discusses the thermal and electrical grounding of the LFCSP in detail. Each of the supply pins should be decoupled using two capacitors; recommended capacitor values are 100 pF and 0.1 µF.

LOCAL OSCILLATOR (LO) INPUT

For optimum performance, the LO port should be driven differentially through a balun. The recommended balun is the M/A-COM ETC1-1-13. The LO inputs to the device should be ac-coupled with 1000 pF capacitors. The LO port is designed for a broadband 50 Ω match from 700 MHz to 2.7 GHz. The LO return loss can be seen in Figure 20. Figure 40 shows the LO input configuration.

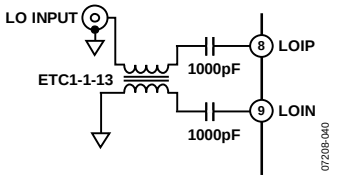

Figure 40. Differential LO Drive

The recommended LO drive level is between −6 dBm and +6 dBm. The applied LO frequency range is between 700 MHz and 2.7 GHz.

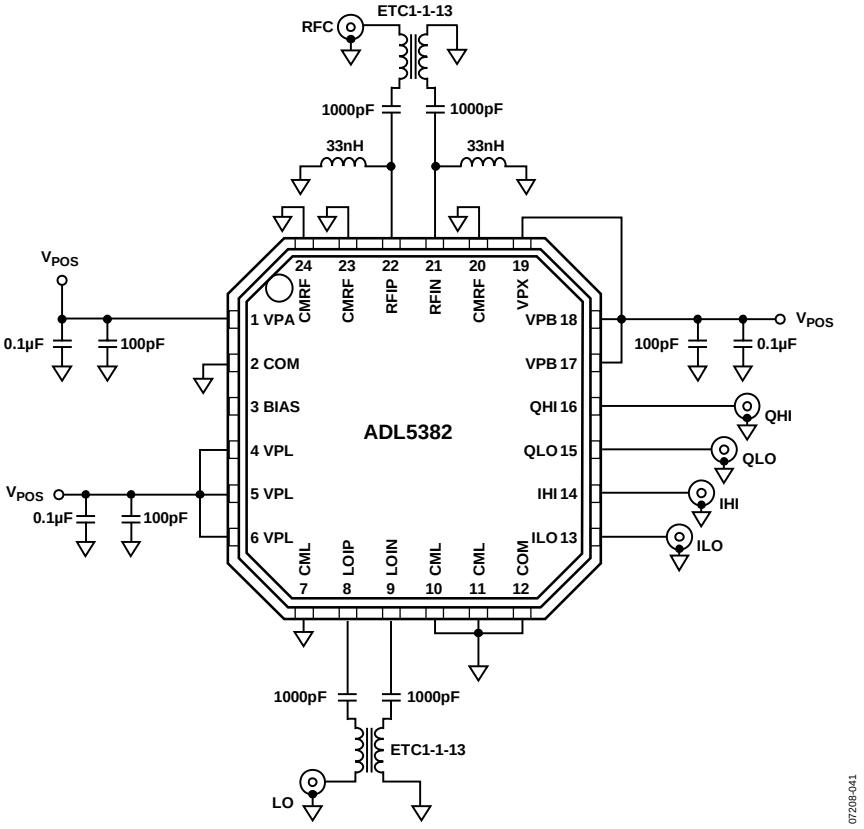

Figure 41. Basic Connections Schematic

RF INPUT

The RF inputs have a differential input impedance of approximately 50 Ω. For optimum performance, the RF port should be driven differentially through a balun. The recommended balun is the M/A-COM ETC1-1-13. The RF inputs to the device should be ac-coupled with 1000 pF capacitors. Ground-referenced choke inductors must also be connected to RFIP and RFIN (the recommended value is 33 nH, Coilcraft 0603CS-33NX) for appropriate biasing. Several important aspects must be taken into account when selecting an appropriate choke inductor for this application. First, the inductor must be able to handle the approximately 40 mA of standing dc current being delivered from each of the RF input pins (RFIP, RFIN). The suggested 0603 inductor has a 600 mA current rating. The purpose of the choke inductors is to provide a very low resistance dc path to ground and high ac impedance at the RF frequency so as not to affect the RF input impedance. A choke inductor that has a self-resonant frequency greater than the RF input frequency ensures that the choke is still looking inductive and therefore has a more predictable ac impedance (jωL) at the RF frequency. Figure 42 shows the RF input configuration.

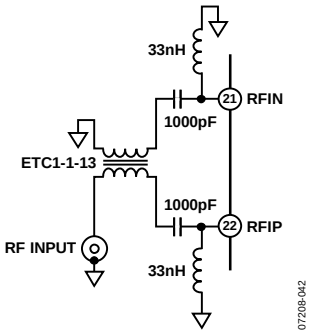

Figure 42. RF Input

The differential RF port return loss is characterized as shown in Figure 43.

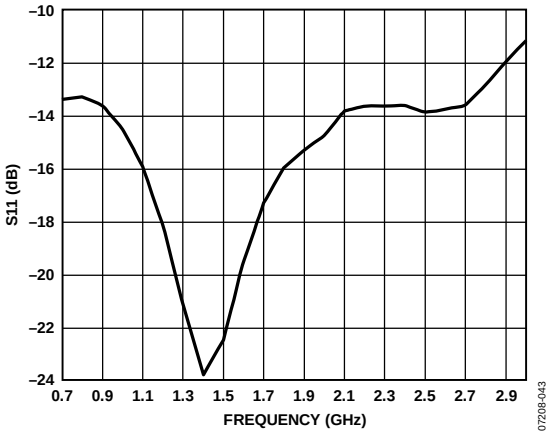

Figure 43. Differential RF Port Return Loss

BASEBAND OUTPUTS

The baseband outputs QHI, QLO, IHI, and ILO are fixed impedance ports. Each baseband pair has a 50 Ω differential output impedance. The outputs can be presented with differential loads as low as 200 Ω (with some degradation in gain) or high impedance differential loads (500 Ω or greater impedance yields the same excellent linearity) that is typical of an ADC. The TCM9-1 9:1 balun converts the differential IF output to single-ended. When loaded with 50 Ω, this balun presents a 450 Ω load to the device. The typical maximum linear voltage swing for these outputs is 2 V p-p differential. The bias level on these pins is equal to VPOS − 2.8 V. The output 3 dB bandwidth is 370 MHz. Figure 44 shows the baseband output configuration.

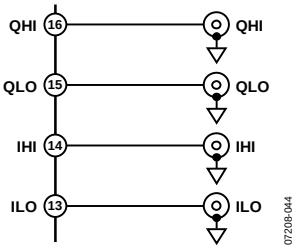

Figure 44. Baseband Output Configuration

ERROR VECTOR MAGNITUDE (EVM) PERFORMANCE

EVM is a measure used to quantify the performance of a digital radio transmitter or receiver. A signal received by a receiver would have all constellation points at the ideal locations; however, various imperfections in the implementation (such as magnitude imbalance, noise floor, and phase imbalance) cause the actual constellation points to deviate from the ideal locations.

The ADL5382 shows excellent EVM performance for various modulation schemes. Figure 45 shows the EVM performance of the ADL5382 with a 16 QAM, 200 kHz low IF.

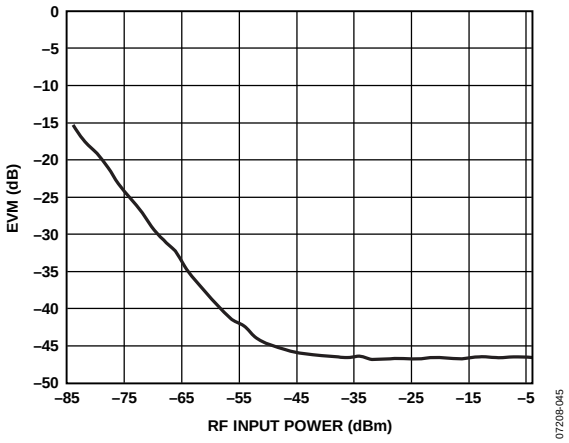

Figure 45. EVM, RF = 900 MHz, IF = 200 kHz vs. RF Input Power for a 16 QAM 160 ksym/s Signal

Figure 46 shows the zero-IF EVM performance of a 10 MHz IEEE 802.16e WiMAX signal through the ADL5382. The differential dc offsets on the ADL5382 are in the order of a few millivolts. However, ac coupling the baseband outputs with 10 µF capacitors eliminates dc offsets and enhances EVM performance. With a 10 MHz BW signal, 10 µF ac coupling capacitors with the 500 Ω differential load results in a high-pass corner frequency of ~64 Hz, which absorbs an insignificant amount of modulated signal energy from the baseband signal. By using ac-coupling capacitors at the baseband outputs, the dc offset effects, which can limit dynamic range at low input power levels, can be eliminated.

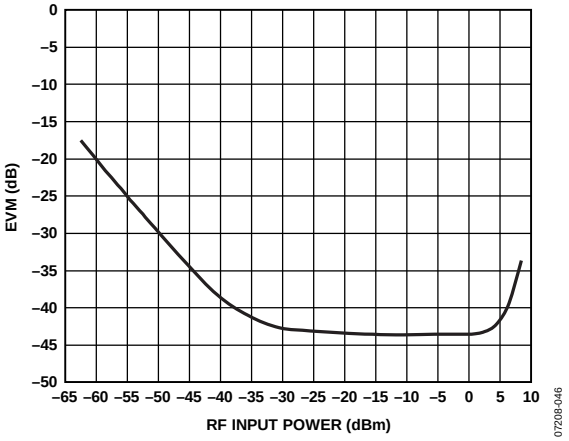

Figure 46. EVM, RF = 2.6 GHz, IF = 0 Hz vs. RF Input Power for a 16 QAM 10 MHz Bandwidth Mobile WiMAX Signal (AC-Coupled Baseband Outputs)

Figure 47 exhibits multiple W-CDMA low-IF EVM performance curves over a wide RF input power range into the ADL5382. In the case of zero-IF, the noise contribution by the vector signal analyzer becomes predominant at lower power levels, making it difficult to measure SNR accurately.

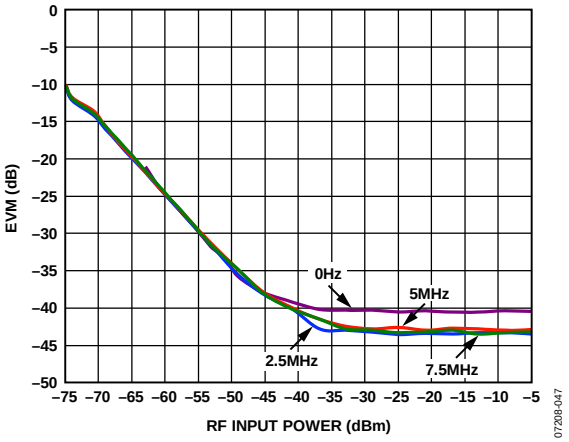

Figure 47. EVM, RF = 1900 MHz, IF = 0 Hz, 2.5 MHz, 5 MHz, and 7.5 MHz vs. RF Input Power for a W-CDMA Signal (AC-Coupled Baseband Outputs)

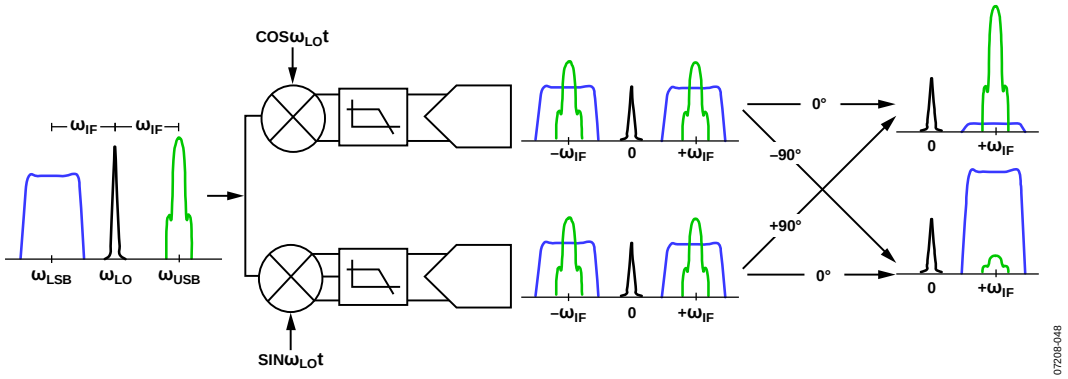

Figure 48. Illustration of the Image Problem

LOW IF IMAGE REJECTION

The image rejection ratio is the ratio of the intermediate frequency (IF) signal level produced by the desired input frequency to that produced by the image frequency. The image rejection ratio is expressed in decibels. Appropriate image rejection is critical because the image power can be much higher than that of the desired signal, thereby plaguing the down conversion process. Figure 48 illustrates the image problem. If the upper sideband (lower sideband) is the desired band, a 90° shift to the Q channel (I channel) cancels the image at the lower sideband (upper sideband). Phase and gain balance between I and Q channels are critical for high levels of image rejection.

Figure 49 shows the excellent image rejection capabilities of the ADL5382 for low IF applications, such as W-CDMA. The ADL5382 exhibits image rejection greater than 45 dB over a broad frequency range.

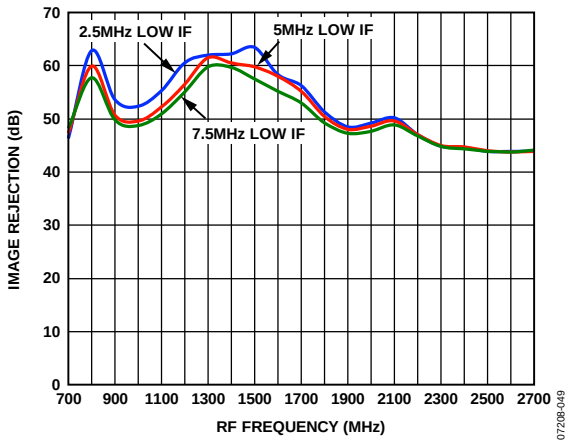

Figure 49. Image Rejection vs. RF Frequency for a W-CDMA Signal, IF = 2.5 MHz, 5 MHz, and 7.5 MHz

EXAMPLE BASEBAND INTERFACE

In most direct conversion receiver designs, it is desirable to select a wanted carrier within a specified band. The desired channel can be demodulated by tuning the LO to the appropriate carrier frequency. If the desired RF band contains multiple carriers of interest, the adjacent carriers would also be down converted to a lower IF frequency. These adjacent carriers can be problematic if they are large relative to the wanted carrier as they can overdrive the baseband signal detection circuitry. As a result, it is often necessary to insert a filter to provide sufficient rejection of the adjacent carriers.

It is necessary to consider the overall source and load impedance presented by the ADL5382 and ADC input to design the filter network. The differential baseband output impedance of the ADL5382 is 50 Ω. The ADL5382 is designed to drive a high impedance ADC input. It may be desirable to terminate the ADC input down to lower impedance by using a terminating resistor, such as 500 Ω. The terminating resistor helps to better define the input impedance at the ADC input at the cost of a slightly reduced gain (see the Circuit Description section for details on the emitter-follower output loading effects). The order and type of filter network depends on the desired high frequency rejection required, pass-band ripple, and group delay. Filter design tables provide outlines for various filter types and orders, illustrating the normalized inductor and capacitor values for a 1 Hz cutoff frequency and 1 Ω load. After scaling the normalized prototype element values by the actual desired cut-off frequency and load impedance, the series reactance elements are halved to realize the final balanced filter network component values.

As an example, a second-order Butterworth, low-pass filter design is shown in Figure 50 where the differential load impedance is 500 Ω and the source impedance of the ADL5382 is 50 Ω. The normalized series inductor value for the 10-to-1, load-to-source impedance ratio is 0.074 H, and the normalized shunt capacitor is 14.814 F. For a 10.9 MHz cutoff frequency, the single-ended equivalent circuit consists of a 0.54 μH series inductor followed by a 433 pF shunt capacitor.

The balanced configuration is realized as the 0.54 μH inductor is split in half to realize the network shown in Figure 50.

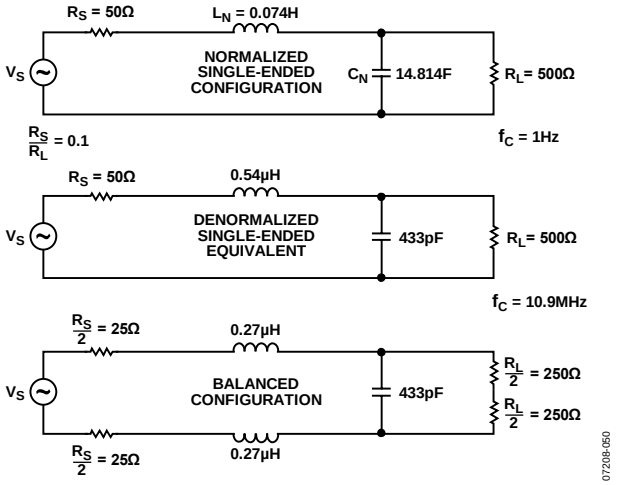

Figure 50. Second-Order Butterworth, Low-Pass Filter Design Example

A complete design example is shown in Figure 53. A sixth-order Butterworth differential filter having a 1.9 MHz corner frequency interfaces the output of the ADL5382 to that of an ADC input. The 500 Ω load resistor defines the input impedance of the ADC. The filter adheres to typical direct conversion W-CDMA applications, where 1.92 MHz away from the carrier IF frequency, 1 dB of rejection is desired and 2.7 MHz away 10 dB of rejection is desired.

Figure 51 and Figure 52 show the measured frequency response and group delay of the filter.

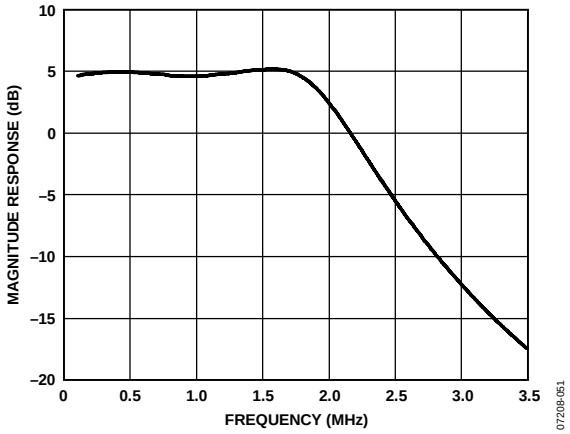

Figure 51. Sixth-Order Baseband Filter Response

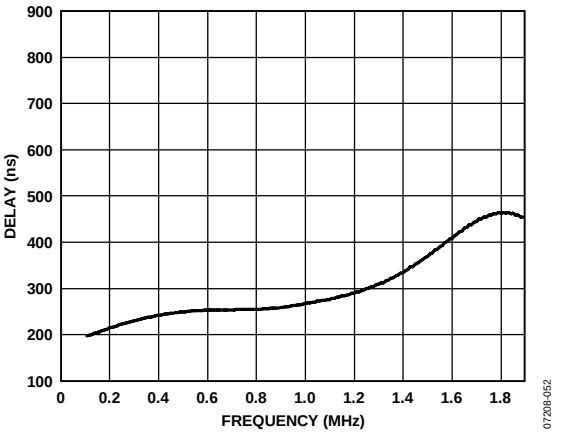

Figure 52. Sixth-Order Baseband Filter Group Delay

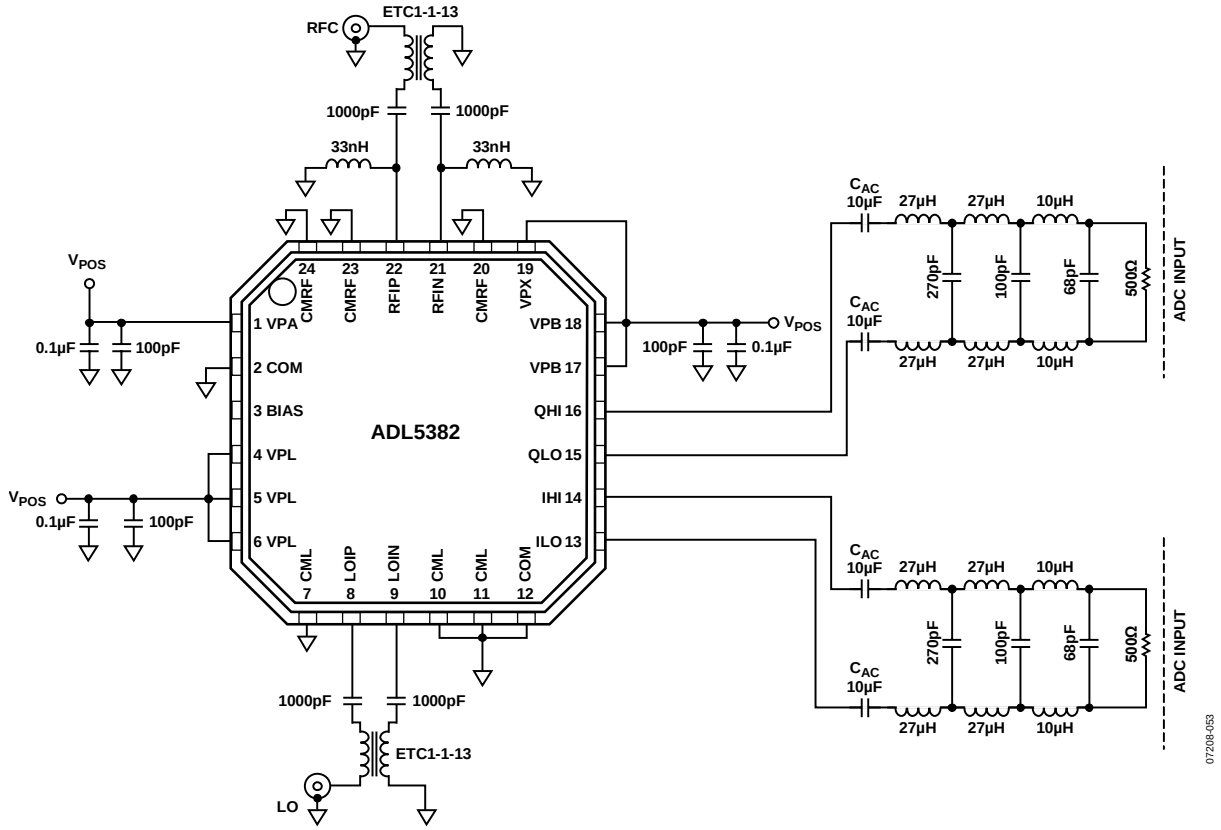

Figure 53. Sixth-Order Low-Pass Butterworth, Baseband Filter Schematic

As the load impedance of the filter increases, the filter design becomes more challenging in terms of meeting the required rejection and pass band specifications. In the previous W-CDMA example, the 500 Ω load impedance resulted in the design of a sixth-order filter that has relatively large inductor values and small capacitor values. If the load impedance is 200 Ω, the filter design becomes much more manageable. As shown in Figure 54, the resultant inductor and capacitor values become much more practical.

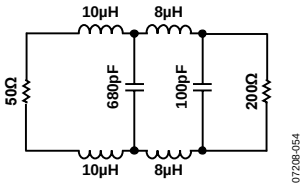

Figure 54. Fourth-Order Low-Pass W-CDMA Filter Schematic

Figure 55 and Figure 56 illustrate the magnitude response and group delay response of the fourth-order filter, respectively.

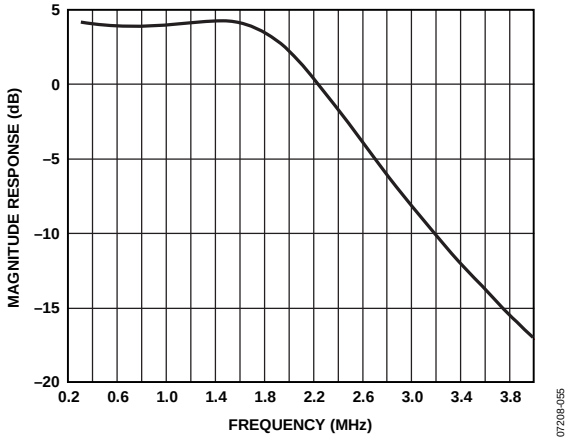

Figure 55. Fourth-Order Low-Pass W-CDMA Filter Magnitude Response

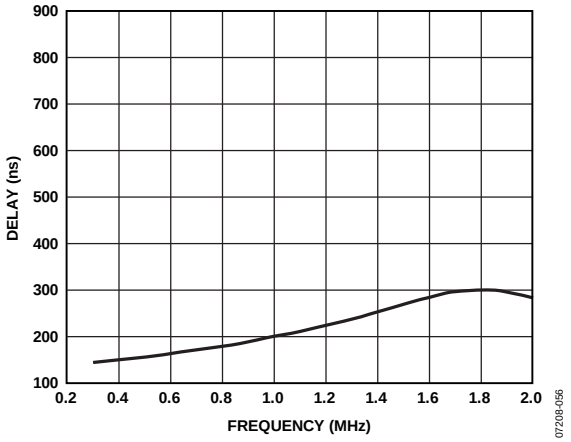

Figure 56. Fourth-Order Low-Pass W-CDMA Filter Group Delay Response

CHARACTERIZATION SETUPS

Figure 57 to Figure 59 show the general characterization bench setups used extensively for the ADL5382. The setup shown in Figure 59 was used to do the bulk of the testing and used sinusoidal signals on both the LO and RF inputs. An automated Agilent VEE program was used to control the equipment over the IEEE bus. This setup was used to measure gain, IP1dB, IIP2, IIP3, I/Q gain match, and quadrature error. The ADL5382 characterization board had a 9-to-1 impedance transformer on each of the differential baseband ports to do the differential-to-single-ended conversion, which presented a 450 Ω differential load to each baseband port, when interfaced with 50 Ω test equipment. For all measurements of the ADL5382, the loss of the RF input balun (the M/A-COM ETC1-1-13 was used on RF input during characterization) was de-embedded.

The two setups shown in Figure 57 and Figure 58 were used for making NF measurements. Figure 57 shows the setup for measuring NF with no blocker signal applied while Figure 58 was used to measure NF in the presence of a blocker. For both setups, the noise was measured at a baseband frequency of 10 MHz. For the case where a blocker was applied, the output blocker was at a 15 MHz baseband frequency. Note that great care must be taken when measuring NF in the presence of a blocker. The RF blocker generator must be filtered to prevent its noise (which increases with increasing generator output power) from swamping the noise contribution of the ADL5382. At least 30 dB of attention at the RF and image frequencies is desired. For example, assume a 915 MHz signal applied to the LO inputs of the ADL5382. To obtain a 15 MHz output blocker signal, the RF blocker generator is set to 930 MHz and the filters tuned such that there is at least 30 dB of attenuation from the generator at both the desired RF frequency (925 MHz) and the image RF frequency (905 MHz). Finally, the blocker must be removed from the output (by the 10 MHz low-pass filter) to prevent the blocker from swamping the analyzer.

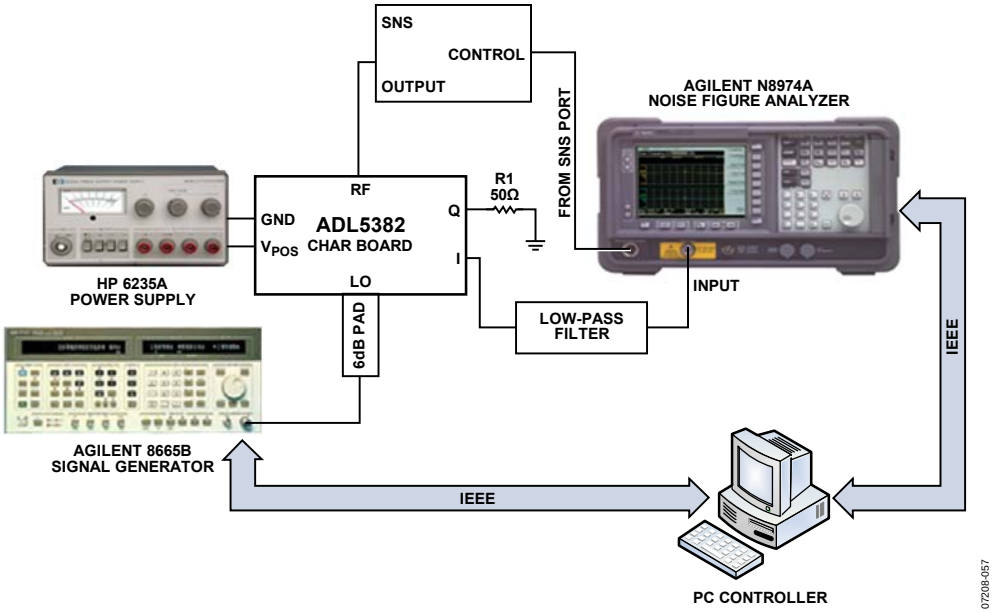

Figure 57. General Noise Figure Measurement Setup

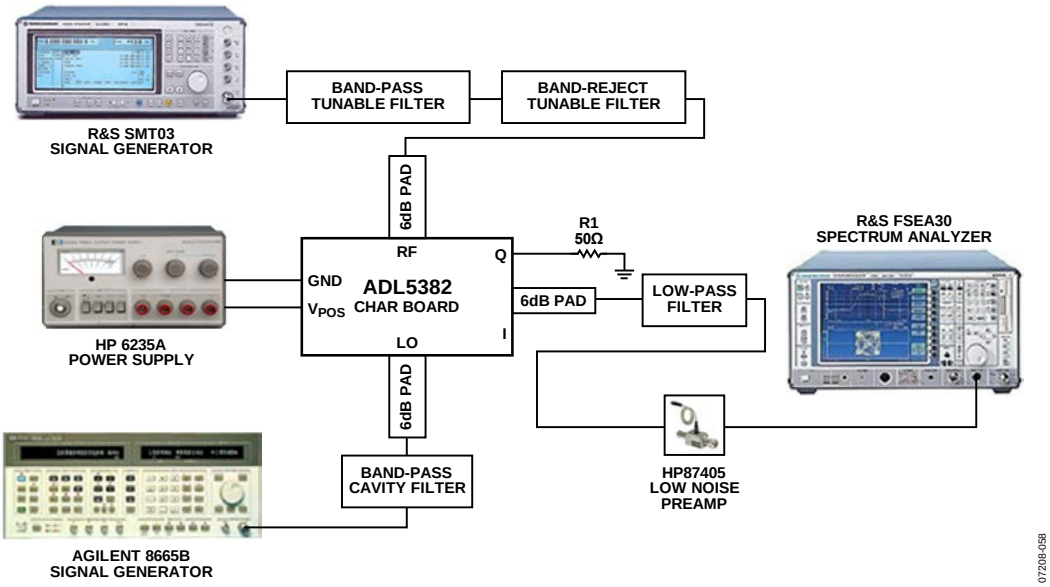

Figure 58. Measurement Setup for Noise Figure in the Presence of a Blocker

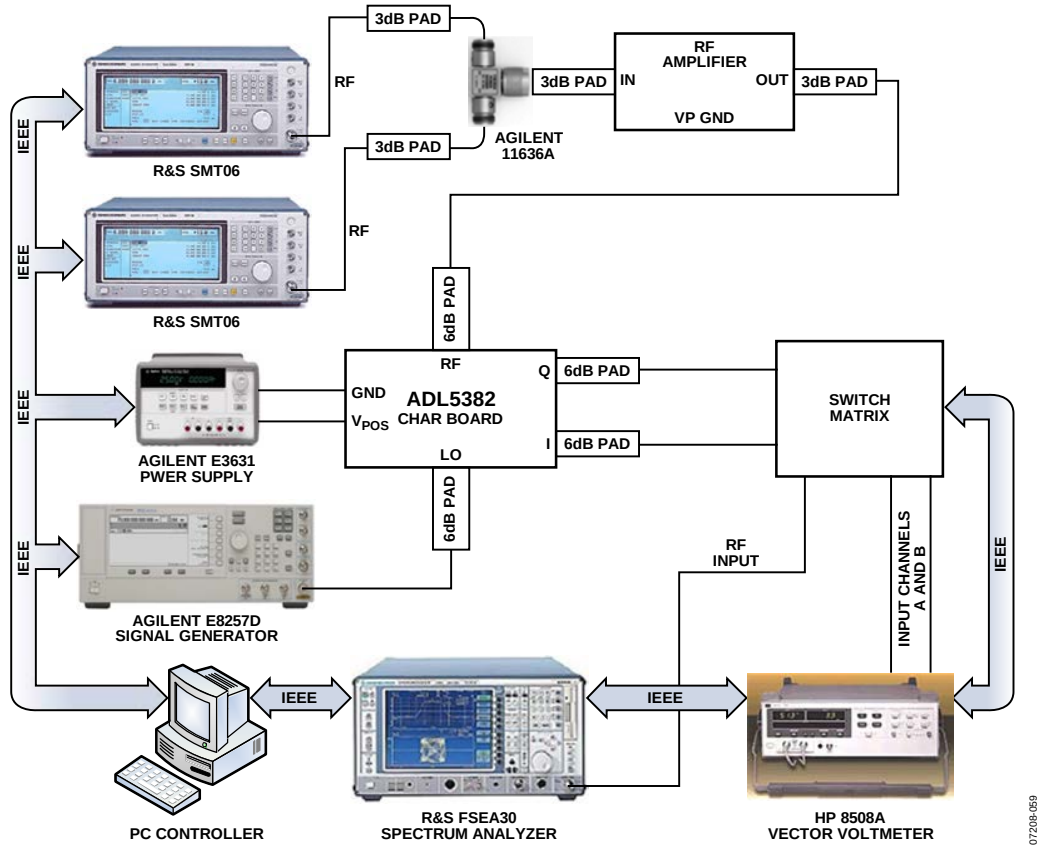

Figure 59. General Characterization Setup

EVALUATION BOARD

The ADL5382 evaluation board is available. The board can be used for single-ended or differential baseband analysis. The default configuration of the board is for single-ended baseband analysis.

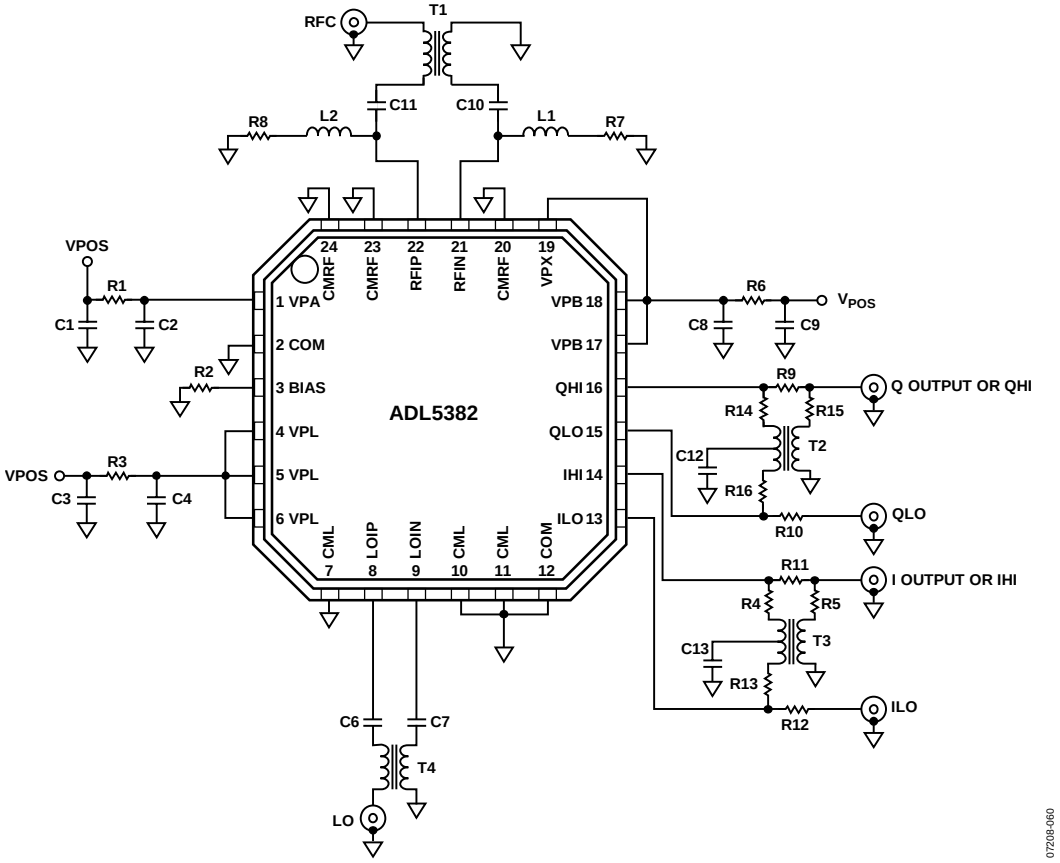

Figure 60. Evaluation Board Schematic

Table 4. Evaluation Board Configuration Options

Component	Function	Default Condition
VPOS, GND	Power Supply and Ground Vector Pins.	Not applicable
R1, R3, R6	Power Supply Decoupling. Shorts or power supply decoupling resistors.	R1, R3, R6 = 0 Ω (0603)
C1, C2, C3, C4, C8, C9	These capacitors provide the required decoupling up to 2.7 GHz.	C2, C4, C8 = 100 pF (0402) C1, C3, C9 = 0.1 µF (0603)
C6, C7, C10, C11	AC Coupling Capacitors. These capacitors provide the required ac coupling from 700 MHz to 2.7 GHz.	C6, C10, C11 = 1000 pF (0402) C7 = open
R4, R5, R9 to R16	Single-Ended Baseband Output Path. This is the default configuration of the evaluation board. R14 to R16 and R4, R5, and R13 are populated for appropriate balun interface. R9, R10 and R11, R12 are not populated. Baseband outputs are taken from QHI and IHI. The user can reconfigure the board to use full differential baseband outputs. R9 to R12 provide a means to bypass the 9:1 TCM9-1 transformer to allow for differential baseband outputs. Access the differential baseband signals by populating R9 to R12 with 0 Ω and not populating R4, R5, R13 to R16. This way the transformer does not need to be removed. The baseband outputs are taken from the SMAs of Q_HI, Q_LO, I_HI, and I_LO.	R4, R5, R13 to R16 = 0 Ω (0402) R9 to R12 = open
L1, L2, R7, R8	Input Biasing. Inductance and resistance sets the input biasing of the common base input stage. The default value is 33 nH.	L1, L2 = 33 nH (0603CS-33NX, Coilcraft) R7, R8 = 0 Ω (0402)
T2, T3	IF Output Interface. TCM9-1 converts a differential high impedance IF output to a single-ended output. When loaded with 50 Ω, this balun presents a 450 Ω load to the device. The center tap can be decoupled through a capacitor to ground.	T2, T3 = TCM9-1, 9:1 (Mini-Circuits)
C12, C13	Decoupling Capacitors. C12 and C13 are the decoupling capacitors used to reject noise on the center tap of the TCM9-1.	C12, C13 = 0.1 µF (0402)
T4	LO Input Interface. The LO is driven differentially. ETC1-1-13 is a 1:1 RF balun that converts the single-ended RF input to differential signal.	T4 = ETC1-1-13, 1:1 (M/A-COM)
T1	RF Input Interface. ETC1-1-13 is a 1:1 RF balun that converts the single-ended RF input to differential signal.	T1 = ETC1-1-13, 1:1 (M/A-COM)
R2	R_{BIAS}. Optional bias setting resistor. See the Bias Circuit section to see how to use this feature.	R2 = open

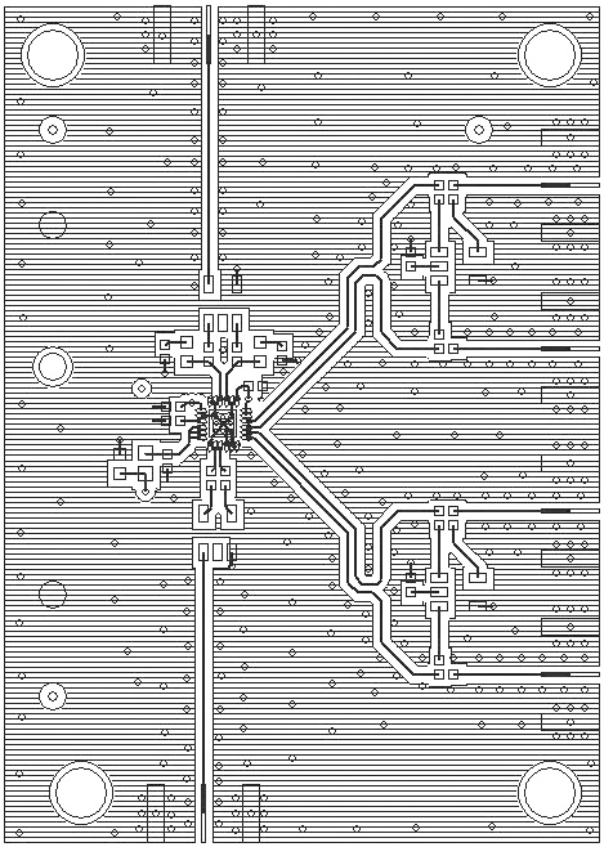

Figure 61. Evaluation Board Top Layer

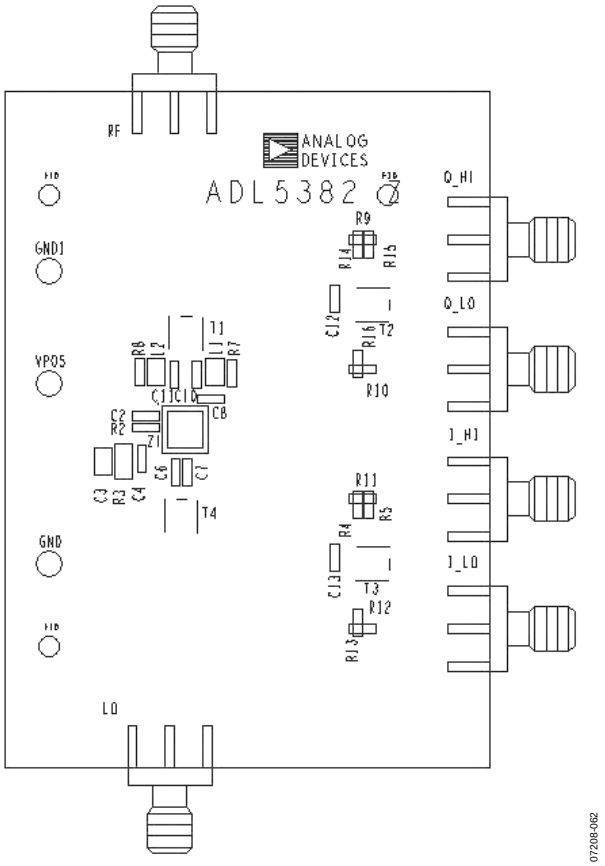

Figure 62. Evaluation Board Top Layer Silkscreen

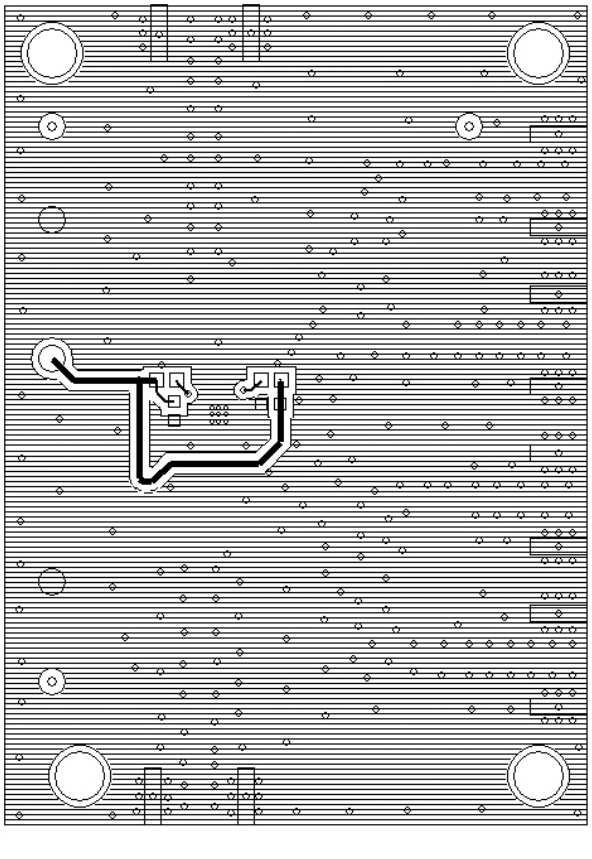

Figure 63. Evaluation Board Bottom Layer

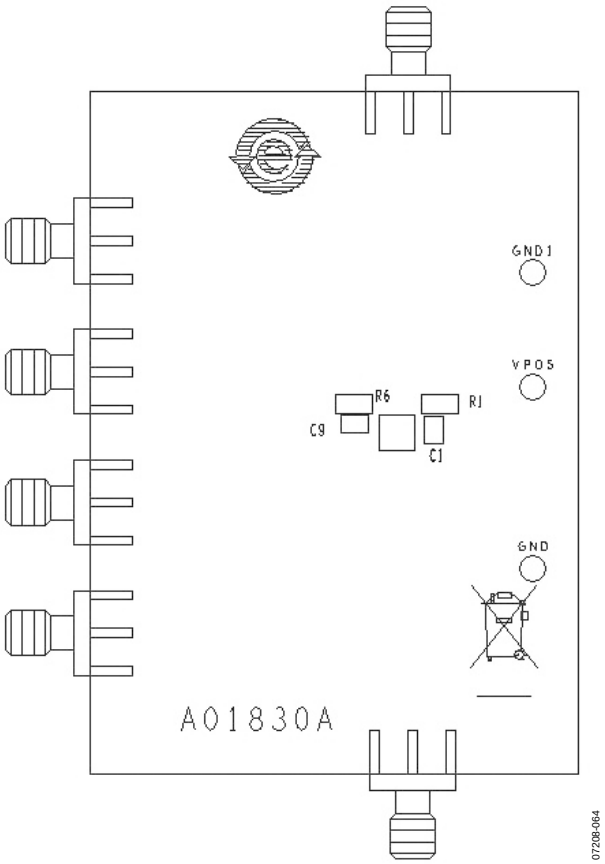

Figure 64. Evaluation Board Bottom Layer Silkscreen

OUTLINE DIMENSIONS

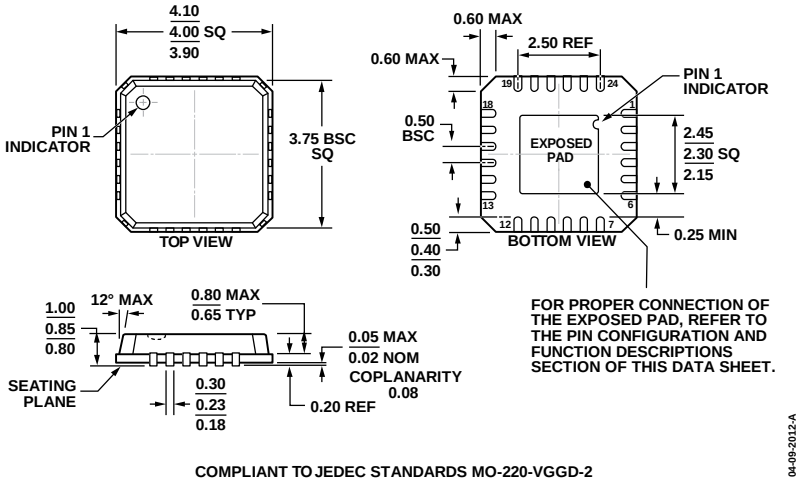

Figure 65. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-24-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5382ACPZ-R7	–40°C to +85°C	24-Lead LFCSP_VQ, 7" Tape and Reel	CP-24-2	1,500
ADL5382ACPZ-WP	–40°C to +85°C	24-Lead LFCSP_VQ, Waffle Pack	CP-24-2	64
ADL5382-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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D07208-0-5/12(A)

Low Noise, Low Distortion Fully Differential Input/ Output Amplifier/Driver

FEATURES

- **Fully Differential Input and Output**
- **Wide Supply Range: 2.375V to 12.6V**
- **Rail-to-Rail Output Swing**
- **Low Noise: 3nV/√Hz**
- **Low Distortion, $2V_{P-P}$, 1MHz: –94dBc**
- **Adjustable Output Common Mode Voltage**
- Unity-Gain Stable
- Gain-Bandwidth: 70MHz
- Slew Rate: 65V/µs
- Large Output Current: 85mA
- DC Voltage Offset <2mV Max
- Open-Loop Gain: 100V/mV
- Low Power Shutdown
- 8-Pin MSOP or 3mm × 3mm DFN Package

APPLICATIONS

- Differential Input A/D Converter Driver
- Single-Ended to Differential Conversion
- Differential Amplification with Common Mode Translation
- Rail-to-Rail Differential Line Driver/Receiver
- Low Voltage, Low Noise, Differential Signal Processing

DESCRIPTION

The LT®1994 is a high precision, very low noise, low distortion, fully differential input/output amplifier optimized for 3V, single-supply operation. The LT1994's output common mode voltage is independent of the input common mode voltage, and is adjustable by applying a voltage on the V_{OCM} pin. A separate internal common mode feedback path provides accurate output phase balancing and reduced even-order harmonics. This makes the LT1994 ideal for level shifting ground referenced signals for driving differential input, single-supply ADCs.

The LT1994 output can swing rail-to-rail and is capable of sourcing and sinking up to 85mA. In addition to the low distortion characteristics, the LT1994 has a low input referred voltage noise of 3nV/√Hz. This part maintains its performance for supply voltages as low as 2.375V. It draws only 13.3mA of supply current and has a hardware shutdown feature that reduces current consumption to 225µA.

The LT1994 is available in an 8-pin MSOP or 8-pin DFN package.

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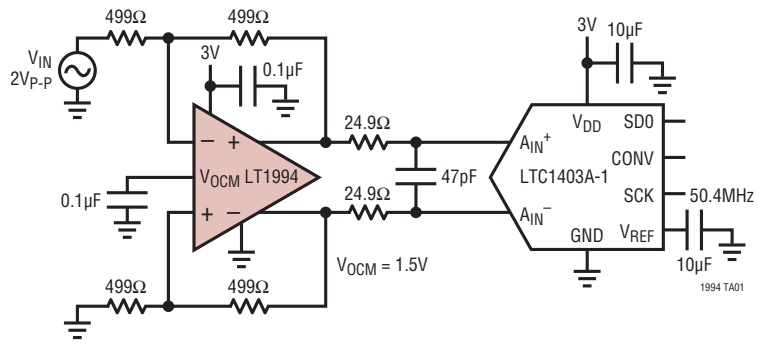
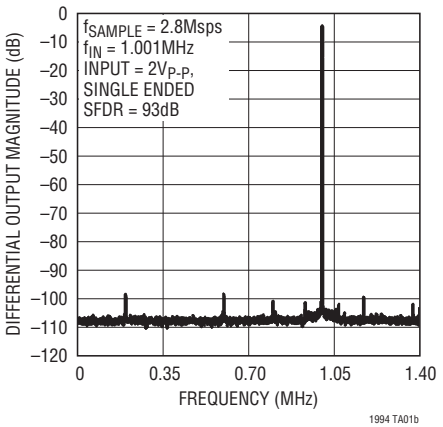
All other trademarks are the property of their respective owners.

TYPICAL APPLICATION

A/D Preamplifier: Single-Ended Input to Differential Output with Common Mode Level Shifting



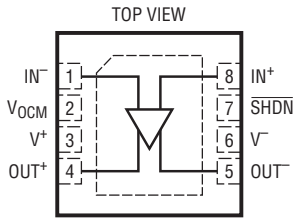
LT1994 Driving an LTC1403A-1 1MHz Sine Wave, 8192 Point FFT Plot



ABSOLUTE MAXIMUM RATINGS (Note 1)

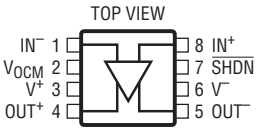
Total Supply Voltage (V^+ to V^-) 12.6V
Input Voltage (Note 2) ..... $\pm V_S$
Input Current (Note 2) ..... ±10mA
Input Current (V_{OCM}, $\overline{SHDN}$) ..... ±10mA
V_{OCM}, $\overline{SHDN}$ ..... $\pm V_S$
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4)
LT1994C ..... –40°C to 85°C
LT1994I ..... –40°C to 85°C
LT1994H ..... –40°C to 125°C
LT1994MP ..... –55°C to 125°C
Specified Temperature Range (Note 5)
LT1994C ..... 0°C to 70°C
LT1994I ..... –40°C to 85°C
LT1994H ..... –40°C to 125°C
LT1994MP ..... –55°C to 125°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO V^-



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 140°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1994CDD#PBF	LT1994CDD#TRPBF	LBQM	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LT1994IDD#PBF	LT1994IDD#TRPBF	LBQM	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT1994HDD#PBF	LT1994HDD#TRPBF	LBQM	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT1994MPDD#PBF	LT1994MPDD#TRPBF	LDXQ	8-Lead (3mm × 3mm) Plastic DFN	–55°C to 125°C
LT1994CMS8#PBF	LT1994CMS8#TRPBF	LTBQN	8-Lead Plastic MSOP	0°C to 70°C
LT1994IMS8#PBF	LT1994IMS8#TRPBF	LTBQN	8-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = mid-supply, $V_{\overline{SHDN}}$ = OPEN, R_I = R_F = 499Ω, R_L = 800Ω to a mid-supply voltage (See Figure 1) unless otherwise noted. V_S is defined ($V^+ – V^-$). V_{OUTCM} is defined as ($V_{OUT}^+ + V_{OUT}^-$)/2. V_{ICM} is defined as ($V_{IN}^+ + V_{IN}^-$)/2. $V_{OUTDIFF}$ is defined as ($V_{OUT}^+ – V_{OUT}^-$). V_{INDIFF} is defined as ($V_{IN}^+ – V_{IN}^-$).

SYMBOL	PARAMETER	CONDITIONS		C/I GRADES MIN	C/I GRADES TYP	C/I GRADES MAX	H/MP GRADES MIN	H/MP GRADES TYP	H/MP GRADES MAX	UNITS
V_{OSDIFF}	Differential Offset Voltage (Input Referred)	V_S = 2.375V, V_{ICM} = V_S/4	●			±2			±2	mV
		V_S = 3V	●			±2			±2	mV
		V_S = 5V	●			±2			±2	mV
		V_S = ±5V	●			±3			±3	mV
$\Delta V_{OSDIFF}/\Delta T$	Differential Offset Voltage Drift (Input Referred)	V_S = 2.375V, V_{ICM} = V_S/4			3					µV/°C
		V_S = 3V			3					µV/°C
		V_S = 5V			3					µV/°C
		V_S = ±5V			3					µV/°C
I_B	Input Bias Current (Note 6)	V_S = 2.375V, V_{ICM} = V_S/4	●	–45	–18	–3	–45	–18	–3	µA
		V_S = 3V	●	–45	–18	–3	–45	–18	–3	µA
		V_S = 5V	●	–45	–18	–3	–45	–18	–3	µA
		V_S = ±5V	●	–45	–18	–3	–45	–18	–3	µA
I_{OS}	Input Offset Current (Note 6)	V_S = 2.375V, V_{ICM} = V_S/4	●		±0.2	±2		±0.2	±2	µA
		V_S = 3V	●		±0.2	±2		±0.2	±2	µA
		V_S = 5V	●		±0.2	±3		±0.2	±3	µA
		V_S = ±5V	●		±0.2	±4		±0.2	±4	µA
R_{IN}	Input Resistance	Common Mode			700			700		kΩ
		Differential Mode			4.5			4.5		kΩ
C_{IN}	Input Capacitance	Differential			2			2		pF
e_n	Differential Input Referred Noise Voltage Density	f = 50kHz			3			3		nV/√Hz
i_n	Input Noise Current Density	f = 50kHz			2.5			2.5		pA/√Hz
e_{nVOCM}	Input Referred Common Mode Output Noise Voltage Density	f = 50kHz, V_{OCM} Shorted to Ground			15			15		nV/√Hz
V_{ICMR} (Note 7)	Input Signal Common Mode Range	V_S = 3V	●	0		1.75	0		1.75	V
		V_S = ±5V	●	–5		3.75	–5		3.75	V
CMRRI (Note 8)	Input Common Mode Rejection Ratio (Input Referred) $\Delta V_{ICM}/\Delta V_{OSDIFF}$	V_S = 3V, ΔV_{ICM} = 0.75V	●	55	85		55	85		dB
CMRRIO (Note 8)	Output Common Mode Rejection Ratio (Input Referred) $\Delta V_{OCM}/\Delta V_{OSDIFF}$	V_S = 5V, ΔV_{OCM} = 2V	●	65	85		65	85		dB
PSRR (Note 9)	Differential Power Supply Rejection ($\Delta V_S/\Delta V_{OSDIFF}$)	V_S = 3V to ±5V	●	69	105		69	105		dB
PSRRCM (Note 9)	Output Common Mode Power Supply Rejection ($\Delta V_S/\Delta V_{OSCM}$)	V_S = 3V to ±5V	●	45	70		45	70		dB
G_{CM}	Common Mode Gain ($\Delta V_{OUTCM}/\Delta V_{OCM}$)	V_S = ±2.5V	●		1					V/V
	Common Mode Gain Error 100 • (G_{CM} – 1)	V_S = ±2.5V	●		–0.15	±1				%
BAL	Output Balance ($\Delta V_{OUTCM}/\Delta V_{OUTDIFF}$)	$\Delta V_{OUTDIFF}$ = 2V								
		Single-Ended Input	●		–65	–46		–65	–46	dB
		Differential Input	●		–71	–50		–71	–50	dB
V_{OSCM}	Common Mode Offset Voltage (V_{OUTCM} – V_{OCM})	V_S = 2.375V, V_{ICM} = V_S/4	●		±2.5	±25		±2.5	±25	mV
		V_S = 3V	●		±2.5	±25		±2.5	±25	mV
		V_S = 5V	●		±2.5	±30		±2.5	±30	mV
		V_S = ±5V	●		±2.5	±40		±2.5	±40	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = mid-supply, $V_{\overline{SHDN}}$ = OPEN, R_I = R_F = 499Ω, R_L = 800Ω to a mid-supply voltage (See Figure 1) unless otherwise noted. V_S is defined ($V^+ – V^-$). V_{OUTCM} is defined as ($V_{OUT}^+ + V_{OUT}^-$)/2. V_{ICM} is defined as ($V_{IN}^+ + V_{IN}^-$)/2. $V_{OUTDIFF}$ is defined as ($V_{OUT}^+ – V_{OUT}^-$). V_{INDIFF} is defined as ($V_{IN}^+ – V_{IN}^-$).

SYMBOL	PARAMETER	CONDITIONS		C/I GRADES MIN	C/I GRADES TYP	C/I GRADES MAX	H/MP GRADES MIN	H/MP GRADES TYP	H/MP GRADES MAX	UNITS
$\Delta V_{OSCM}/\Delta T$	Common Mode Offset Voltage Drift	V_S = 2.375V, V_{ICM} = V_S/4			5			5		µV/°C
		V_S = 3V			5			5		µV/°C
		V_S = 5V			5			5		µV/°C
		V_S = ±5V			5			5		µV/°C
V_{OUTCMR} (Note 7)	Output Signal Common Mode Range (Voltage Range for the V_{OCM} Pin)	V_S = 3V, ±5V	●	V^- + 1.1		V^+ – 0.8	V^- + 1.1		V^+ – 0.8	V
R_{INVOCM}	Input Resistance, V_{OCM} Pin		●	30	40	60	30	40	60	kΩ
V_{MID}	Voltage at the V_{OCM} Pin	V_S = 5V	●	2.45	2.5	2.55	2.45	2.5	2.55	V
V_{OUT}	Output Voltage, High, Either Output Pin (Note 10)	V_S = 3V, No Load	●		70	140		70	140	mV
		V_S = 3V, R_L = 800Ω	●		90	175		90	175	mV
		V_S = 3V, R_L = 100Ω	●		200	400		200	400	mV
		V_S = ±5V, No Load	●		150	325		150	325	mV
		V_S = ±5V, R_L = 800Ω	●		200	450		200	450	mV
		V_S = ±5V, R_L = 100Ω	●		900	2400		900	2400	mV
	Output Voltage, Low, Either Output Pin (Note 10)	V_S = 3V, No Load	●		30	70		30	70	mV
		V_S = 3V, R_L = 800Ω	●		50	90		50	90	mV
		V_S = 3V, R_L = 100Ω	●		125	250		125	250	mV
		V_S = ±5V, No Load	●		80	180		80	180	mV
		V_S = ±5V, R_L = 800Ω	●		125	250		125	250	mV
		V_S = ±5V, R_L = 100Ω	●		900	2400		900	2400	mV
I_{SC}	Output Short-Circuit Current, Either Output Pin (Note 11)	V_S = 2.375V, R_L = 10Ω	●	±25	±35		±10	±35		mA
		V_S = 3V, R_L = 10Ω	●	±30	±40		±15	±40		mA
		V_S = 5V, R_L = 10Ω	●	±40	±65		±40	±65		mA
		V_S = ±5V, V_{CM} = 0V, R_L = 10Ω	●	±45	±85		±45	±85		mA
SR	Slew Rate	V_S = 5V, $\Delta V_{OUT}^+ = -\Delta V_{OUT}^-$ = 1V	●	50	65	85	50	65	85	V/µS
		V_S = ±5V, V_{CM} = 0V, $\Delta V_{OUT}^+ = -\Delta V_{OUT}^-$ = 1.8V	●	50	65	85	50	65	85	V/µS
GBW	Gain-Bandwidth Product (f_{TEST} = 1MHz)	V_S = 3V, T_A = 25°C	●	58	70		58	70		MHz
		V_S = ±5V, V_{CM} = 0V, T_A = 25°C	●	58	70		58	70		MHz
	Distortion	V_S = 3V, R_L = 800Ω, f_{IN} = 1MHz, $V_{OUT}^+ – V_{OUT}^-$ = $2V_{P-P}$								
		Differential Input								
		2nd Harmonic			–99			–99		dBc
		3rd Harmonic			–96			–96		dBc
		Single-Ended Input								
		2nd Harmonic			–94			–94		dBc
		3rd Harmonic			–108			–108		dBc
t_S	Settling Time	V_S = 3V, 0.01%, 2V Step			120			120		ns
		V_S = 3V, 0.1%, 2V Step			90			90		ns
A_{VOL}	Large-Signal Voltage Gain	V_S = 3V			100			100		dB
V_S	Supply Voltage Range		●	2.375		12.6	2.375		12.6	V
I_S	Supply Current	V_S = 3V	●		13.3	18.5		13.3	20.0	mA
		V_S = 5V	●		13.9	19.5		13.9	20.5	mA
		V_S = ±5V	●		14.8	20.5		14.8	21.5	mA
$I_{\overline{SHDN}}$	Supply Current in Shutdown	V_S = 3V	●		0.225	0.8		0.225	0.8	mA
		V_S = 5V	●		0.375	1.75		0.375	1.75	mA
		V_S = ±5V	●		0.7	2.5		0.7	2.5	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = mid-supply, $V_{\overline{SHDN}}$ = OPEN, R_I = R_F = 499Ω, R_L = 800Ω to a mid-supply voltage (See Figure 1) unless otherwise noted. V_S is defined ($V^+ - V^-$). V_{OUTCM} is defined as ($V_{OUT}^+ + V_{OUT}^-$)/2. V_{ICM} is defined as ($V_{IN}^+ + V_{IN}^-$)/2. $V_{OUTDIFF}$ is defined as ($V_{OUT}^+ - V_{OUT}^-$). V_{INDIFF} is defined as ($V_{IN}^+ - V_{IN}^-$).

SYMBOL	PARAMETER	CONDITIONS		C/I GRADES MIN	C/I GRADES TYP	C/I GRADES MAX	H/MP GRADES MIN	H/MP GRADES TYP	H/MP GRADES MAX	UNITS
V_{IL}	$\overline{SHDN}$ Input Logic Low	V_S = 3V to ±5V	●			$V^+ - 2.1$			$V^+ - 2.1$	V
V_{IH}	$\overline{SHDN}$ Input Logic High	V_S = 3V to ±5V	●	$V^+ - 0.6$			$V^+ - 0.6$			V
$R_{\overline{SHDN}}$	$\overline{SHDN}$ Pull-Up Resistor	V_S = 2.375V to ±5V		40	55	75	40	55	75	kΩ
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ 0.5V to 3V			1			1		µs
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ 3V to 0.5V			1			1		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by a pair of back-to-back diodes. If the differential input voltage exceeds 1V, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LT1994C/LT1994I are guaranteed functional over the operating temperature range –40°C to 85°C. The LT1994H is guaranteed functional over the operating temperature range –40°C to 125°C. The LT1994MP is guaranteed functional over the operating temperature range –55°C to 125°C.

Note 5: The LT1994C is guaranteed to meet specified performance from 0°C to 70°C. The LT1994C is designed, characterized, and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LT1994I is guaranteed to meet specified performance from –40°C to 85°C. The LT1994H is guaranteed to meet specified performance from –40°C to 125°C. The LT1994MP is guaranteed to meet specified performance from –55°C to 125°C.

Note 6: Input bias current is defined as the average of the input currents flowing into Pin 1 and Pin 8 (IN^- and IN^+). Input Offset current is defined as the difference of the input currents flowing into Pin 8 and Pin 1 ($I_{OS} = I_B^+ - I_B^-$).

Note 7: Input Common Mode Range is tested using the Test Circuit of Figure 1 ($R_F = R_I$) by applying a single ended $2V_{P-P}$ 1kHz signal to V_{INP} (V_{INM} = 0), and measuring the output distortion (THD) at the common mode Voltage Range limits listed in the Electrical Characteristics table, and confirming the output THD is better than –40dB. The voltage range for the output common mode range (Pin 2) is tested using the Test Circuit of Figure 1 ($R_F = R_I$) by applying a 0.5V peak, 1kHz signal to the V_{OCM} Pin 2 (with $V_{INP} = V_{INM}$ = 0) and measuring the output distortion (THD) at V_{OUTCM} with V_{OCM} biased 0.5V from the V_{OCM} pin range limits listed in the Electrical Characteristics Table, and confirming the THD is better than –40dB.

Note 8: Input CMRR is defined as the ratio of the change in the input common mode voltage at the pins IN^+ or IN^- to the change in differential input referred voltage offset. Output CMRR is defined as the ratio of the change in the voltage at the V_{OCM} pin to the change in differential input referred voltage offset.

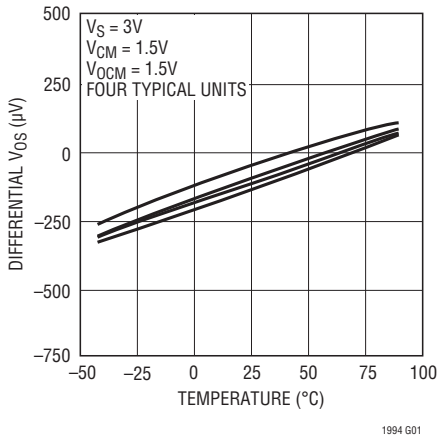
Note 9: Differential Power Supply Rejection (PSRR) is defined as the ratio of the change in supply voltage to the change in differential input referred voltage offset. Common Mode Power Supply Rejection (PSRRCM) is defined as the ratio of the change in supply voltage to the change in the common mode offset, $V_{OUTCM} - V_{OCM}$.

Note 10: Output swings are measured as differences between the output and the respective power supply rail.

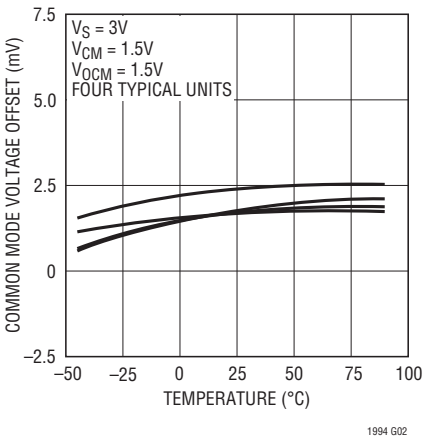
Note 11: Extended operation with the output shorted may cause junction temperatures to exceed the 150°C limit and is not recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

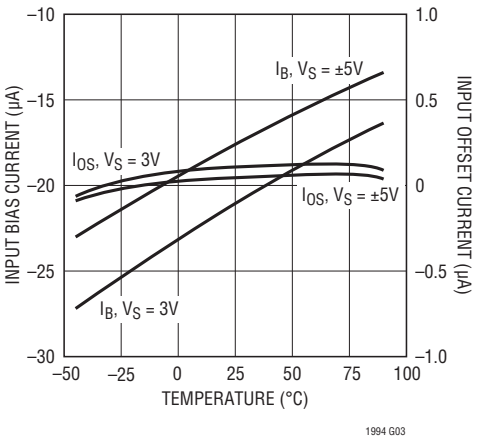
Differential Input Referred Voltage Offset vs Temperature



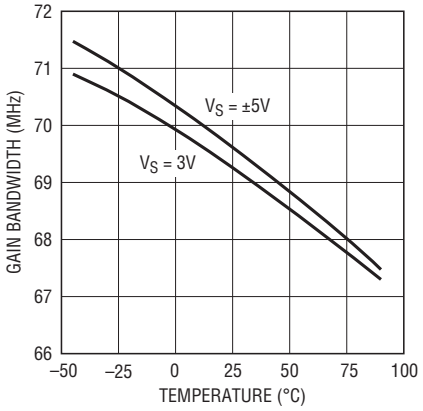
Common Mode Voltage Offset vs Temperature



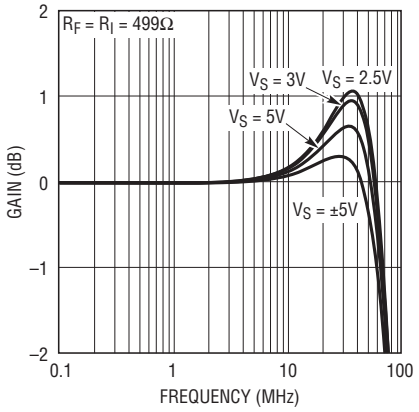
Input Bias Current and Input Offset Current vs Temperature



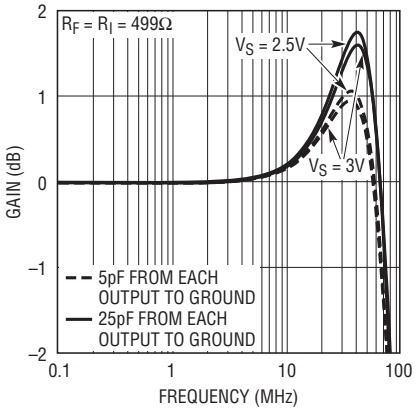
Gain Bandwidth vs Temperature



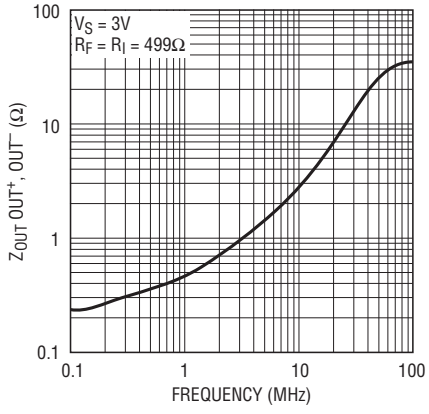
Frequency Response vs Supply Voltage



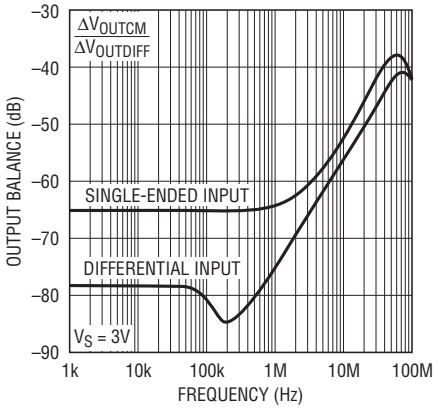
Frequency Response vs Load Capacitance



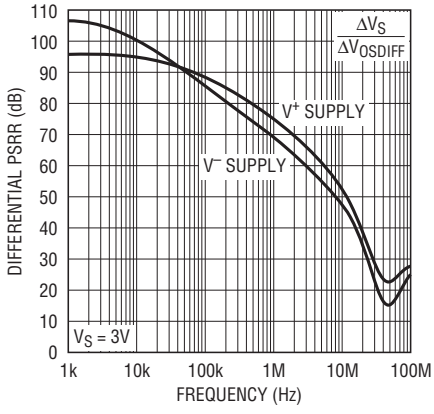
Output Impedance vs Frequency



Output Balance vs Frequency

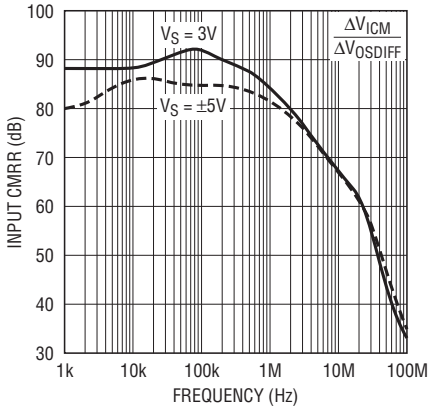


Differential Power Supply Rejection vs Frequency



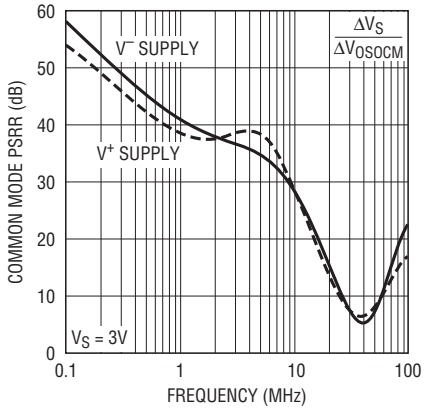
TYPICAL PERFORMANCE CHARACTERISTICS

Input Common Mode Rejection vs Frequency



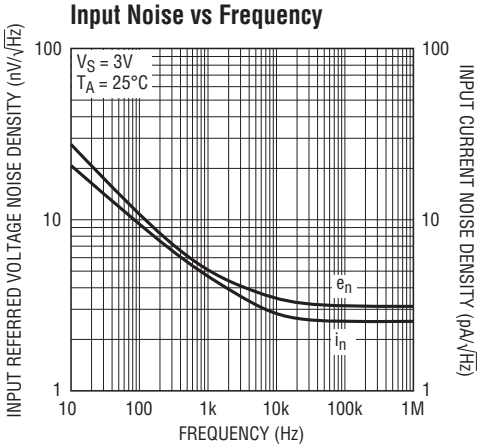
1995 G10

Common Mode Output Power Supply Rejection vs Frequency



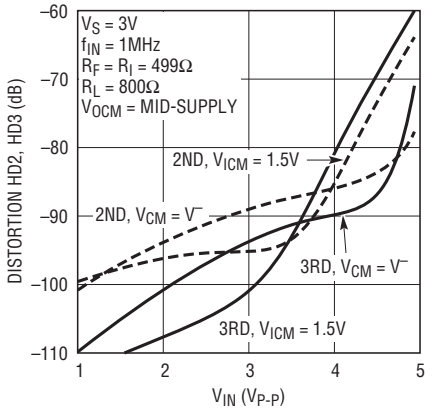
1995 G11

Input Noise vs Frequency



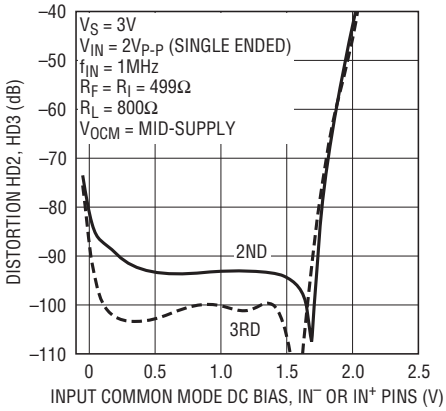
1995 G12

Differential Distortion vs Input Amplitude (Single-Ended Input)



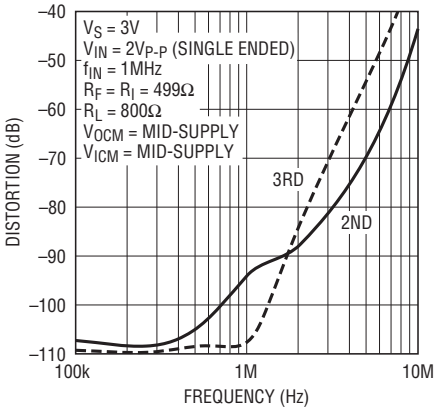
1994 G13

Differential Distortion vs Input Common Mode Level



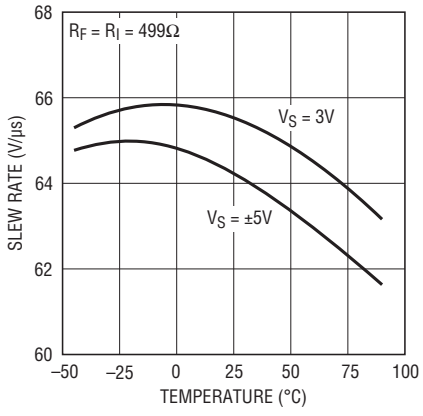
1994 G14

Differential Distortion vs Frequency



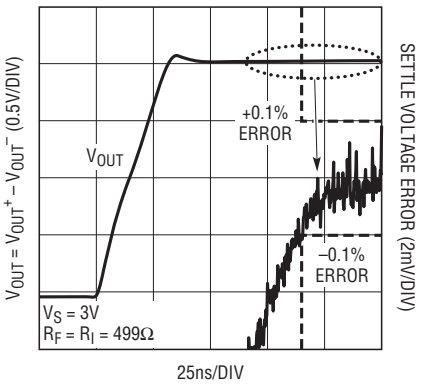
1994 G15

Slew Rate vs Temperature



1994 G16

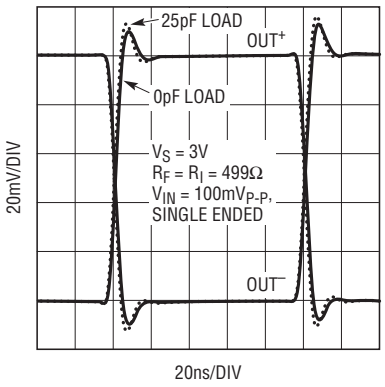
2V Step Response Settling



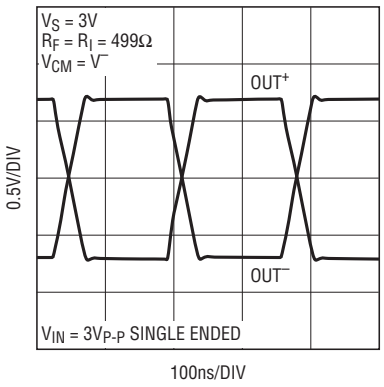
1994 G17

TYPICAL PERFORMANCE CHARACTERISTICS

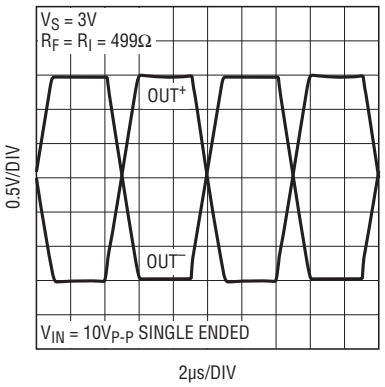
Small-Signal Step Response



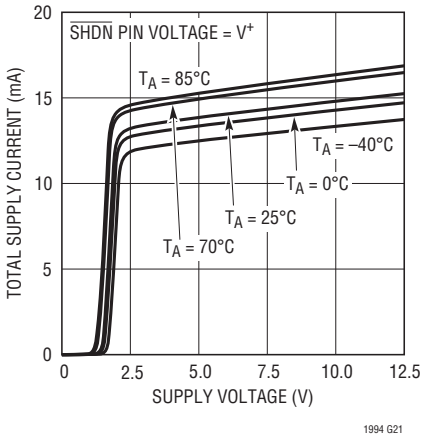
Large-Signal Step Response



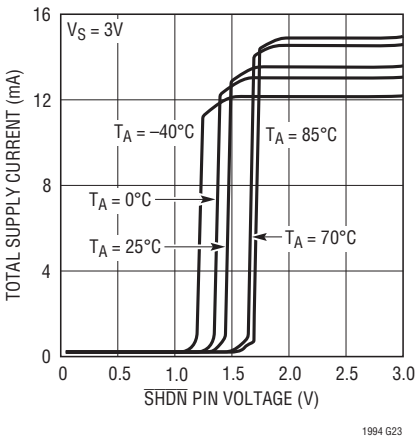
Output with Large Input Overdrive



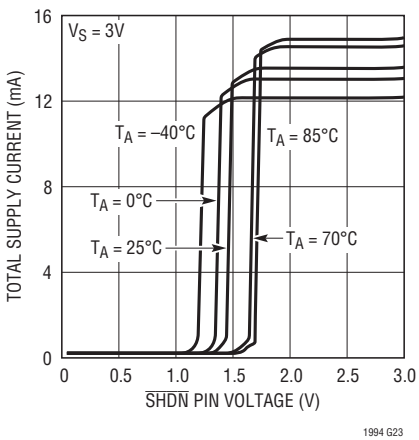
Supply Current vs Supply Voltage



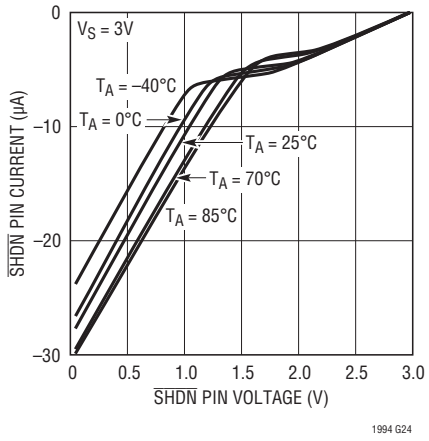
Supply Current vs $\overline{SHDN}$ Voltage



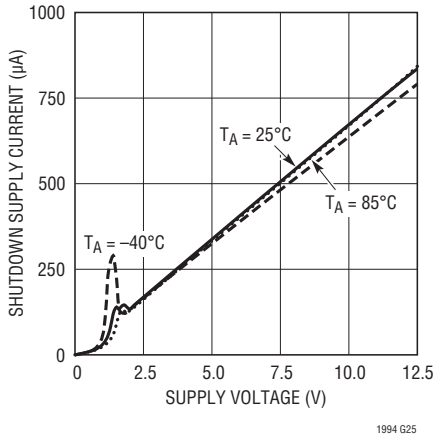
Supply Current vs $\overline{SHDN}$ Voltage



$\overline{SHDN}$ Pin Current vs $\overline{SHDN}$ Pin Voltage



Shutdown Supply Current vs Supply Voltage



PIN FUNCTIONS

IN^+, IN^- (Pins 1, 8): Noninverting and Inverting Input Pins of the Amplifier, Respectively. For best performance, it is highly recommended that stray capacitance be kept to an absolute minimum by keeping printed circuit connections as short as possible, and if necessary, stripping back nearby surrounding ground plane away from these pins.

V_{OCM} (Pin 2): Output Common Mode Reference Voltage. The V_{OCM} pin is the midpoint of an internal resistive voltage divider between the supplies, developing a (default) mid-supply voltage potential to maximize output signal swing. V_{OCM} has a Thevenin equivalent resistance of approximately 40k and can be overdriven by an external voltage reference. The voltage on V_{OCM} sets the output common mode voltage level (which is defined as the average of the voltages on the OUT^+ and OUT^- pins). V_{OCM} should be bypassed with a high quality ceramic bypass capacitor of at least 0.1µF (unless connected directly to a low impedance, low noise ground plane) to minimize common mode noise from being converted to differential noise by impedance mismatches both externally and internally to the IC.

V^+, V^- (Pins 3, 6): Power Supply Pins. For single-supply applications (Pin 6 grounded) it is recommended that high quality 1µF and 0.1µF ceramic bypass capacitors be placed from the positive supply pin (Pin 3) to the negative supply pin (Pin 6) with minimal routing. Pin 6 should be directly tied to a low impedance ground plane. For dual power supplies, it is recommended that high quality, 0.1µF ceramic capacitors are used to bypass Pin 3 to ground and Pin 6 to ground. It is also highly recommended that high quality 1µF and 0.1µF ceramic bypass capacitors be placed across the power supply pins (Pins 3 and 6) with minimal routing.

OUT^+, OUT^- (Pins 4, 5): Output Pins. Each pin can drive approximately 100Ω to ground with a short-circuit current limit of up to ±85mA. Each amplifier output is designed to drive a load capacitance of 25pF. This basically means the amplifier can drive 25pF from each output to ground or 12.5pF differentially. Larger capacitive loads should be decoupled with at least 25Ω resistors from each output.

$\overline{SHDN}$ (Pin 7): When Pin 7 ($\overline{SHDN}$) is floating or when Pin 7 is directly tied to V^+, the LT1994 is in the normal operating mode. When Pin 7 is pulled a minimum of 2.1V below V^+, the LT1994 enters into a low power shutdown state. Refer to the $\overline{SHDN}$ pin section under Applications Information for a description of the LT1994 output impedance in the shutdown state.

APPLICATIONS INFORMATION

Functional Description

The LT1994 is a small outline, wideband, low noise and low distortion fully-differential amplifier with accurate output-phase balancing. The LT1994 is optimized to drive low voltage, single-supply, differential input analog-to-digital converters (ADCs). The LT1994's output is capable of swinging rail-to-rail on supplies as low as 2.5V, which makes the amplifier ideal for converting ground referenced, single-ended signals into V_{OCM} referenced differential signals in preparation for driving low voltage, single-supply, differential input ADCs. Unlike traditional op amps which have a single output, the LT1994 has two outputs to process signals differentially. This allows for two times the signal swing in low voltage systems when compared to single-ended output amplifiers. The balanced differential nature of the amplifier also provides even-order harmonic distortion cancellation, and less susceptibility to common mode noise (like power supply noise). The LT1994 can be used as a single-ended input to differential output amplifier, or as a differential input to differential output amplifier.

The LT1994's output common mode voltage, defined as the average of the two output voltages, is independent of the input common mode voltage, and is adjusted by applying a voltage on the V_{OCM} pin. If the pin is left open, there is an internal resistive voltage divider, which develops a potential halfway between the V^+ and V^- pins. The V_{OCM} pin will have an equivalent Thevenin equivalent resistance of 40k, and a Thevenin equivalent voltage of half supply. Whenever this pin is not hard tied to a low impedance ground plane, it is recommended that a high quality ceramic capacitor is used to bypass the V_{OCM} pin to a low impedance ground plane (see Layout Considerations in this document). The LT1994's internal common mode feedback path forces accurate output phase balancing to reduce even order harmonics, and centers each individual output about the potential set by the V_{OCM} pin.

$$V_{OUTCM} = V_{OCM} = \frac{V_{OUT}^{+} + V_{OUT}^{-}}{2}$$

The outputs (OUT^+ and OUT^-) of the LT1994 are capable of swinging rail-to-rail. They can source or sink up to approximately 85mA of current. Each output is rated to drive approximately 25pF to ground (12.5pF differentially). Higher load capacitances should be decoupled with at least 25Ω of series resistance from each output.

Input Pin Protection

The LT1994's input stage is protected against differential input voltages that exceed 1V by two pairs of back-to-back diodes that protect against emitter base breakdown of the input transistors. In addition, the input pins have steering diodes to either power supply. If the input pair is overdriven, the current should be limited to under 10mA to prevent damage to the IC. The LT1994 also has steering diodes to either power supply on the V_{OCM}, and $\overline{SHDN}$ pins (Pins 2 and 7) and if exposed to voltages that exceed either supply, they too should be current limited to under 10mA.

$\overline{SHDN}$ Pin

If the $\overline{SHDN}$ pin (Pin 7) is pulled 2.1V below the positive supply, an internal current is generated that is used to power down the LT1994. The pin will have the Thevenin equivalent impedance of approximately 55kΩ to V^+. If the pin is left unconnected, an internal pull-up resistor of 120k will keep the part in normal active operation. Care should be taken to control leakage currents at this pin to under 1µA to prevent leakage currents from inadvertently putting the LT1994 into shutdown. In shutdown, all biasing current sources are shut off, and the output pins OUT^+ and OUT^- will each appear as open collectors with a nonlinear capacitor in parallel, and steering diodes to either supply. Because of the nonlinear capacitance, the outputs still have the ability to sink and source small amounts of transient current if exposed to significant voltage transients. The inputs (IN^+ and IN^-) have anti-parallel diodes that can conduct if voltage transients at the input exceed 1V. The inputs also have steering diodes to either supply. The turn-on and turn-off time between the shutdown and active states are on the order of 1µs but depends on the circuit configuration.

APPLICATIONS INFORMATION

General Amplifier Applications

As levels of integration have increased and, correspondingly, system supply voltages decreased, there has been a need for ADCs to process signals differentially in order to maintain good signal-to-noise ratios. These ADCs are typically supplied from a single-supply voltage that can be as low as 2.5V and will have an optimal common mode input range near mid-supply. The LT1994 makes interfacing to these ADCs trivial, by providing both single-ended to differential conversion as well as common mode level shifting. Figure 1 shows a general single-supply application with perfectly matched feedback networks from OUT^+ and OUT^-. The gain to $V_{OUTDIFF}$ from V_{INM} and V_{INP} is:

$$V_{OUTDIFF} = V_{OUT}^{+} - V_{OUT}^{-} \approx \frac{R_F}{R_I} \bullet (V_{INP} - V_{INM})$$

Note from the above equation that the differential output voltage ($V_{OUT}^+ - V_{OUT}^-$) is completely independent of input and output common mode voltages, or the voltage at the common mode pin. This makes the LT1994 ideally suited pre-amplification, level shifting, and conversion of single-ended signals to differential output signals in preparation for driving differential input ADCs.

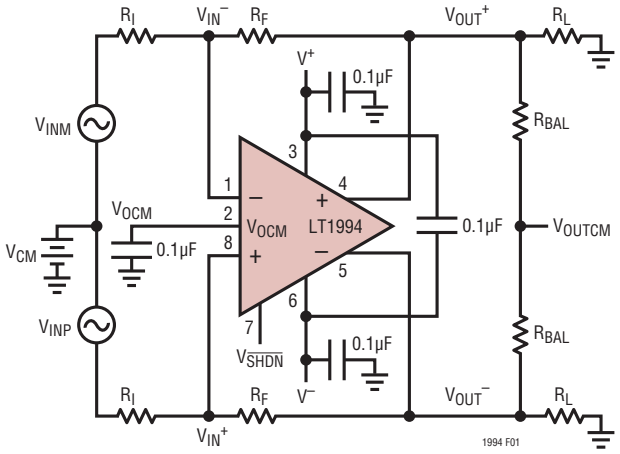


Figure 1. Test Circuit

Effects of Resistor Pair Mismatch

Figure 2 shows a circuit diagram that takes into consideration that real world resistors will not perfectly match. Assuming infinite open-loop gain, the differential output relationship is given by the equation:

$$V_{OUTDIFF} = V_{OUT}^{+} - V_{OUT}^{-} \cong \frac{R_F}{R_I} \bullet V_{INDIFF} + \frac{\Delta\beta}{\beta_{AVG}} \bullet V_{ICM} - \frac{\Delta\beta}{\beta_{AVG}} \bullet V_{OCM},$$

where:

R_F is the average of R_{F1} and R_{F2}, and R_I is the average of R_{I1} and R_{I2}.

β_{AVG} is defined as the average feedback factor (or gain) from the outputs to their respective inputs:

$$\beta_{AVG} = \frac{1}{2} \bullet \left(\frac{R_{I2}}{R_{I2} + R_{F2}} + \frac{R_{I1}}{R_{I1} + R_{F1}} \right)$$

$\Delta\beta$ is defined as the difference in feedback factors:

$$\Delta\beta = \frac{R_{I2}}{R_{I2} + R_{F2}} - \frac{R_{I1}}{R_{I1} + R_{F1}}$$

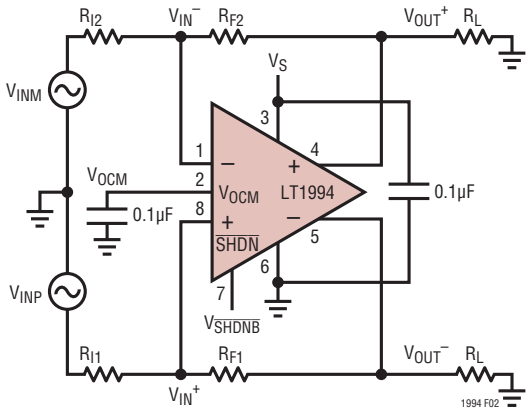


Figure 2. Real-World Application

APPLICATIONS INFORMATION

V_{ICM} is defined as the average of the two input voltages, V_{INP} and V_{INM} (also called the input common mode voltage):

$$V_{ICM} = \frac{1}{2} \bullet (V_{INP} + V_{INM})$$

and V_{INDIFF} is defined as the difference of the input voltages:

$$V_{INDIFF} = V_{INP} - V_{INM}$$

When the feedback ratios mismatch ($\Delta\beta$), common mode to differential conversion occurs.

Setting the differential input to zero ($V_{INDIFF} = 0$), the degree of common mode to differential conversion is given by the equation:

$$V_{OUTDIFF} = V_{OUT}^{+} - V_{OUT}^{-} \approx (V_{ICM} - V_{OCM}) \bullet \frac{\Delta\beta}{\beta_{AVG}} \Bigg|_{V_{INDIFF} = 0}$$

In general, the degree of feedback pair mismatch is a source of common mode to differential conversion of both signals and noise. Using 1% resistors or better will provide about 28dB of common mode rejection. Using 0.1% resistors will provide about 48dB of common mode rejection. A low impedance ground plane should be used as a reference for both the input signal source and the V_{OCM} pin. A direct short of V_{OCM} to this ground plane or bypassing the V_{OCM} with a high quality 0.1µF ceramic capacitor to this ground plane will further mitigate against common mode signals from being converted to differential.

Input Impedance and Loading Effects

The input impedance looking into the V_{INP} or V_{INM} input of Figure 1 depends on whether or not the sources V_{INP} and V_{INM} are fully differential. For balanced input sources ($V_{INP} = -V_{INM}$), the input impedance seen at either input is simply:

$$R_{INP} = R_{INM} = R_I$$

For single-ended inputs, because of the signal imbalance at the input, the input impedance actually increases over the balanced differential case. The input impedance looking into either input is:

$$R_{INP} = R_{INM} = \frac{R_I}{\left(1 - \frac{1}{2} \bullet \left[\frac{R_F}{R_I + R_F}\right]\right)}$$

Input signal sources with non-zero output impedances can also cause feedback imbalance between the pair of feedback networks. For the best performance, it is recommended that the source's output impedance be compensated for. If input impedance matching is required by the source, R1 should be chosen (see Figure 3):

$$R1 = \frac{R_{INM} \bullet R_S}{R_{INM} - R_S}$$

According to Figure 3, the input impedance looking into the differential amp (R_{INM}) reflects the single-ended source case, thus:

$$R_{INM} = \frac{R_I}{\left(1 - \frac{1}{2} \bullet \left[\frac{R_F}{R_I + R_F}\right]\right)}$$

R2 is chosen to balance $R1 || R_S$:

$$R2 = \frac{R1 \bullet R_S}{R1 + R_S}$$

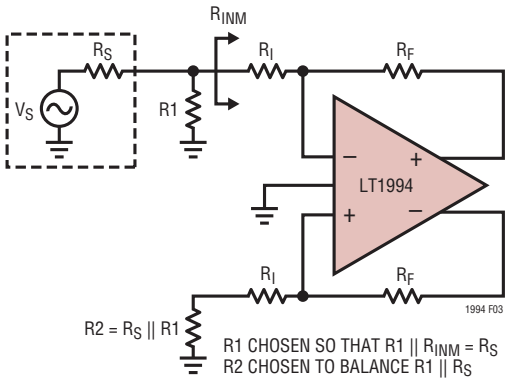


Figure 3. Optimal Compensation for Signal-Source Impedance

APPLICATIONS INFORMATION

Input Common Mode Voltage Range

The LT1994's input common mode voltage (V_{ICM}) is defined as the average of the two input voltages, V_{IN}^+, and V_{IN}^-. It extends from V^- to approximately 1.25V below V^+. The input common mode range depends on the circuit configuration (gain), V_{OCM} and V_{CM} (refer to Figure 4). For fully differential input applications, where $V_{INP} = -V_{INM}$, the common mode input is approximately:

$$V_{ICM} = \frac{V_{IN}^+ + V_{IN}^-}{2} \approx V_{OCM} \bullet \left(\frac{R_I}{R_I + R_F}\right) + V_{CM} \bullet \left(\frac{R_F}{R_F + R_I}\right)$$

With singled-ended inputs, there is an input signal component to the input common mode voltage. Applying only V_{INP} (setting V_{INM} to zero), the input common voltage is approximately:

$$V_{ICM} = \frac{V_{IN}^+ + V_{IN}^-}{2} \approx V_{OCM} \bullet \left(\frac{R_I}{R_I + R_F}\right) + V_{CM} \bullet \left(\frac{R_F}{R_F + R_I}\right) + \frac{V_{INP}}{2} \bullet \left(\frac{R_F}{R_F + R_I}\right)$$

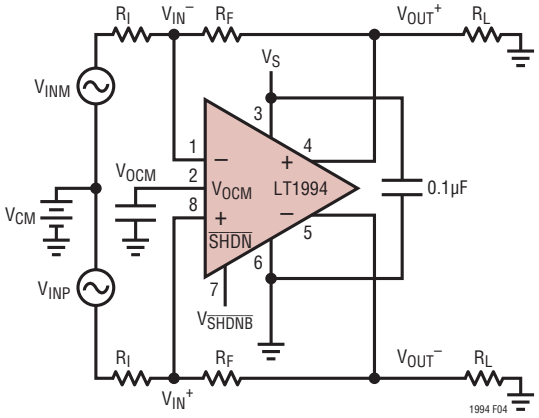


Figure 4. Circuit for Common Mode Range

Output Common Mode Voltage Range

The output common mode voltage is defined as the average of the two outputs:

$$V_{OUTCM} = V_{OCM} = \frac{V_{OUT}^+ + V_{OUT}^-}{2}$$

The V_{OCM} sets this average by an internal common mode feedback loop which internally forces $V_{OUT}^+ = -V_{OUT}^-$. The output common mode range extends from approximately 1.1V above V^- to approximately 0.8V below V^+. The V_{OCM} pin sits in the middle of an 80kΩ to 80kΩ voltage divider that sets the default mid-supply open-circuit potential.

In single-supply applications, where the LT1994 is used to interface to an ADC, the optimal common mode input range to the ADC is often determined by the ADC's reference. If the ADC makes a reference available for setting the input common mode voltage, it can be directly tied to the V_{OCM} pin, but must be capable of driving a 40k equivalent resistance that is tied to a mid-supply potential. If an external reference drives the V_{OCM} pin, it should still be bypassed with a high quality 0.1µF capacitor to a low impedance ground plane to filter any thermal noise and to prevent common mode signals on this pin from being inadvertently converted to differential signals.

Noise Considerations

The LT1994's input referred voltage noise is on the order of $3nV/\sqrt{Hz}$. Its input referred current noise is on the order of $2.5pA/\sqrt{Hz}$. In addition to the noise generated by the amplifier, the surrounding feedback resistors also contribute noise. The output noise generated by both the amplifier and the feedback components is given by the equation:

$$e_{no} = \sqrt{\left(e_{ni} \bullet \left[1 + \frac{R_F}{R_I}\right]\right)^2 + 2 \bullet \left(I_n \bullet R_F\right)^2 + 2 \bullet \left(e_{nRI} \bullet \left[\frac{R_F}{R_I}\right]\right)^2 + 2 \bullet e_{nRF}^2}$$

APPLICATIONS INFORMATION

A plot of this equation and a plot of the noise generated by the feedback components are shown in Figure 6.

The LT1994's input referred voltage noise contributes the equivalent noise of a 560Ω resistor. When the feedback network is comprised of resistors whose values are less than this, the LT1994's output noise is voltage noise dominant (See Figure 6):

$$e_{no} \approx e_{ni} \bullet \left(1 + \frac{R_F}{R_I}\right)$$

Feedback networks consisting of resistors with values greater than about 10k will result in output noise which is amplifier current noise dominant.

$$e_{no} \approx \sqrt{2} \bullet I_n \bullet R_F$$

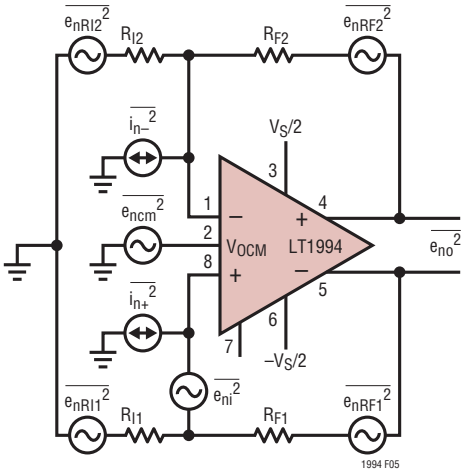


Figure 5. Noise Analysis

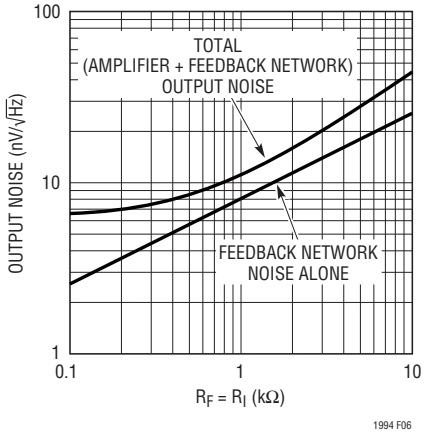


Figure 6. LT1994 Output Spot Noise vs Spot Noise Contributed by Feedback Network Alone

Lower resistor values always result in lower noise at the penalty of increased distortion due to increased loading of the feedback network on the output. Higher resistor values will result in higher output noise, but improved distortion due to less loading on the output.

Figure 6 shows the noise voltage that will appear differentially between the outputs. The common mode output noise voltage does not add to this differential noise. For optimum noise and distortion performance, use a differential output configuration.

Power Dissipation Considerations

The LT1994 is housed in either an 8-lead MSOP package (θ_{JA} = 140°C/W or an 8-lead DD package (θ_{JA} = 43°C/W). The LT1994 combines high speed and large output current with a small die and small package so there is a need to be sure the die temperature does not exceed 150°C. In the 8-lead MSOP, LT1994 has its V^- lead fused to the frame so it is possible to lower the package thermal impedance by connecting the V^- pin to a large ground plane or metal trace. Metal trace and plated through holes can be used to spread the heat generated by the device to the backside of the PC board. For example, an 8-lead MSOP on a 3/32" FR-4 board with 540mm^2 of 2oz. copper on both sides of the PC board tied to the V^- pin can drop the θ_{JA} from 140°C/W to 110°C/W (see Table 1).

The underside of the DD package has exposed metal (4mm^2) from the lead frame where the die is attached. This provides for the direct transfer of heat from the die junction to the printed circuit board to help control the maximum operating junction temperature. The dual-in-line pin arrangement allows for extended metal beyond the ends of the package on the topside (component side) of a circuit board. Table 1 summarizes for the MSOP package, the thermal resistance from the die junction-to-ambient that can be obtained using various amounts of topside, and backside metal (2oz. copper). On multilayer boards, further reductions can be obtained using additional metal on inner PCB layers connected through vias beneath the package.

APPLICATIONS INFORMATION

In general, the die temperature can be estimated from the ambient temperature T_A, and the device power dissipation P_D:

$$T_J = T_A^+ + P_D \bullet \theta_{JA}$$

The power dissipation in the IC is a function of the supply voltage, the output voltage, and the load resistance. For fully differential output amplifiers at a given supply voltage ($\pm V_{CC}$), and a given differential load (R_{LOAD}), the worst-case power dissipation $P_{D(MAX)}$ occurs at the worst-case quiescent current ($I_{Q(MAX)}$ = 20.5mA) and when the load current is given by the expression:

$$I_{LOAD} = \frac{V_{CC}}{R_{LOAD}}$$

The worst-case power dissipation in the LT1994 at

$$I_{LOAD} = \frac{V_{CC}}{R_{LOAD}} \text{ is:}$$

$$P_{D(MAX)} = 2 \bullet V_{CC} \bullet \left(I_{LOAD} + I_{Q(MAX)}\right) - I_{LOAD}{}^2 \bullet$$

$$R_{LOAD} = \frac{V_{CC}{}^2}{R_{LOAD}} + 2 \bullet V_{CC} \bullet I_{Q(MAX)}$$

Example: A LT1994 is mounted on a circuit board in a MSOP-8 package (θ_{JA} = 140°C/W), and is running off of ±5V supplies driving an equivalent load (external load plus feedback network) of 75Ω. The worst-case power that would be dissipated in the device occurs when:

$$P_{D(MAX)} = \frac{V_{CC}{}^2}{R_{LOAD}} + 2 \bullet V_{CC} \bullet I_{Q(MAX)}$$

$$= \frac{5V^2}{75\Omega} + 2 \bullet 5V \bullet 17.5MA = 0.54W$$

The maximum ambient temperature the 8-lead MSOP is allowed to operate under these conditions is:

$T_A = T_{JMAX} – P_D \bullet \theta_{JA}$ = 150°C – (0.54W) • (140°C/W) = 75°C

To operate the device at higher ambient temperature, connect more copper to the $V^–$ pin to reduce the thermal resistance of the package as indicated in Table 1.

Table 1. LT1994 MSOP Package Thermal Resistivity

COPPER AREA TOPSIDE (mm^2)	COPPER AREA BACKSIDE (mm^2)	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
0	0	140
30	0	135
100	0	130
100	100	120
540	540	110

Layout Considerations

Because the LT1994 is a high speed amplifier, it is sensitive to both stray capacitance and stray inductance. Components connected to the LT1994 should be connected with as short and direct connections as possible. A low noise, low impedance ground plane is critical for the highest performance. In single-supply applications, high quality surface mount 1µF and 0.1µF ceramic bypass capacitors with minimum PCB trace should be used directly across the power supplies V^+ to $V^–$. In split supply applications, high quality surface mount 1µF and 0.1µF ceramic bypass capacitors should be placed across the power supplies V^+ to $V^–$, and individual high quality surface mount 0.1µF bypass capacitors should be used from each supply to ground with direct (short) connections.

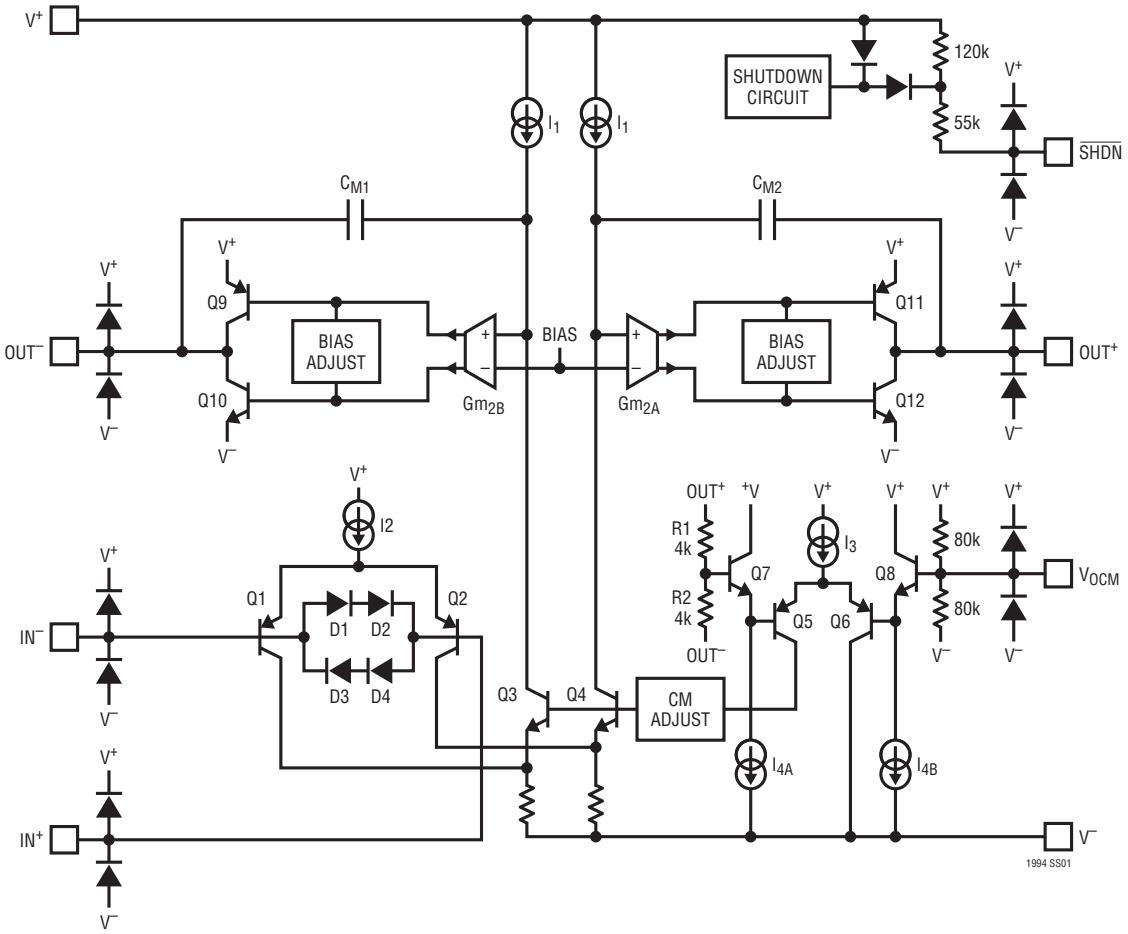
Any stray parasitic capacitance to ground at the summing junctions, IN^+ and $IN^–$ should be kept to an absolute minimum even if it means stripping back the ground plane away from any trace attached to this node. This becomes especially true when the feedback resistor network uses resistor values >500Ω in circuits with $R_F = R_I$. Excessive peaking in the frequency response can be mitigated by adding small amounts of feedback capacitance around RF (2pF to 5pF). Always keep in mind the differential nature of the LT1994, and that it is critical that the output impedances seen by both outputs (stray or intended) should be as balanced and symmetric as possible. This will help preserve the natural balance of the LT1994, which minimizes the generation of even order harmonics, and preserves the rejection of common mode signals and noise.

It is highly recommended that the V_{OCM} pin be either hard tied to a low impedance ground plane (in split supply applications) or bypassed to ground with a high quality

APPLICATIONS INFORMATION

0.1µF ceramic capacitor in single-supply applications. This will help prevent thermal noise from the internal 80kΩ-80kΩ voltage divider (25nV/√Hz) and other external sources of noise from being converted to differential noise due to mismatches in the feedback networks. It is also recommended that the resistive feedback networks be comprised of 1% resistors (or better) to enhance the output common mode rejection. This will also prevent V_{OCM} input referred common mode noise of the common mode amplifier path (which cannot be filtered) from being converted to differential noise, degrading the differential noise performance.

SIMPLIFIED SCHEMATIC

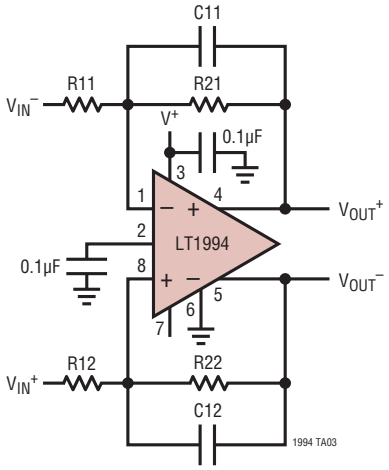


TYPICAL APPLICATIONS

Differential 1st Order Lowpass Filter

Maximum –3dB frequency (f_{3dB}) 2MHz

Stopband attenuation: –6dB at 2 • f_{3dB} and 14dB at 5 • f_{3dB}



Component Calculation:

R11 = R12, R21 = R22

$$f_{3dB} \leq 2MHz \text{ and Gain} \leq \frac{2MHz}{f_{3dB}}$$

1. Calculate an absolute value for C11 ($C11_{abs}$) using a specified –3dB frequency

$$C11_{abs} = \frac{4 \bullet 10^5}{f_{3dB}} \text{ ($C11_{abs}$ in pF and f_{3dB} in kHz)}$$

2. Select a standard 5% capacitor value nearest the absolute value for C11
3. Calculate R11 and R21 using the standard 5% C11 value, f_{3dB} and desired gain

   R11 and R21 equations (C11 in pF and f_{3dB} in kHz)

$$R21 = \frac{159.2 \bullet 10^6}{C11 \bullet f_{3dB}}$$

$$R11 = \frac{R21}{Gain}$$

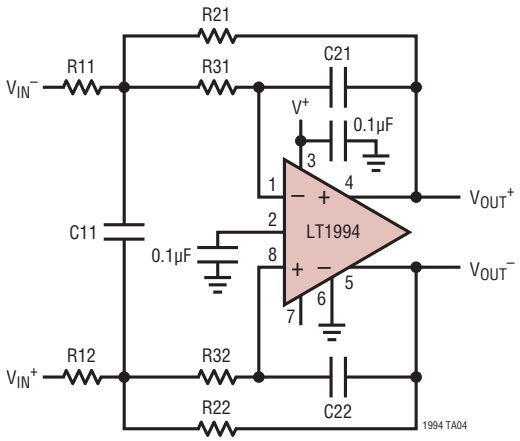
Example: The specified –3dB frequency is 1MHz Gain = 4

1. Using f_{3dB} = 1000kHz, $C11_{abs}$ = 400pF
2. Nearest standard 5% value to 400pF is 390pF and C11 = C12 = 390pF
3. Using f_{3dB} = 1000kHz, C11 = 390pF and Gain = 4, R21 = R22 = 412Ω and R11 = R12 = 102Ω (nearest 1% value)

Differential 2nd Order Butterworth Lowpass Filter

Maximum –3dB frequency (f_{3dB}) 1MHz

Stopband attenuation: –12dB at 2 • f_{3dB} and –28dB at 5 • f_{3dB}



Component Calculation:

R11 = R12, R21 = R22, R31 = R32, C21 = C22, C11 = 10 • C21, R1 = R11, R2 = R21, R3 = R31, C2 = C21 and C1 = C11

1. Calculate an absolute value for C2 ($C2_{abs}$) using a specified –3dB frequency

$$C2_{abs} = \frac{4 \bullet 10^5}{f_{3dB}} \text{ ($C2_{abs}$ in pF and f_{3dB} in kHz) (Note 2)}$$

2. Select a standard 5% capacitor value nearest the absolute value for C2 (C1 = 10 • C2)

TYPICAL APPLICATIONS

3. Calculate R3, R2 and R1 using the standard 5% C2 value, the specified f_{3dB} and the specified passband gain (Gn)

$$f_{3dB} \leq 1MHz \text{ and } Gain \leq 8.8 \text{ or } Gain \leq \frac{1MHz}{f_{3dB}}$$

R1, R2 and R3 equations (C2 in pF and f_{3dB} in kHz)

$$R3 = \frac{\left(1.121 - \sqrt{(1.131 - 0.127 \bullet Gn)}\right) \bullet 10^8}{(Gn+1) \bullet C2 \bullet f_{3dB}} \text{ (Note 1)}$$

$$R2 = \frac{1.266 \bullet 10^{15}}{R3 \bullet C2^2 \bullet f_{3dB}^2}$$

$$R1 = \frac{R2}{Gn}$$

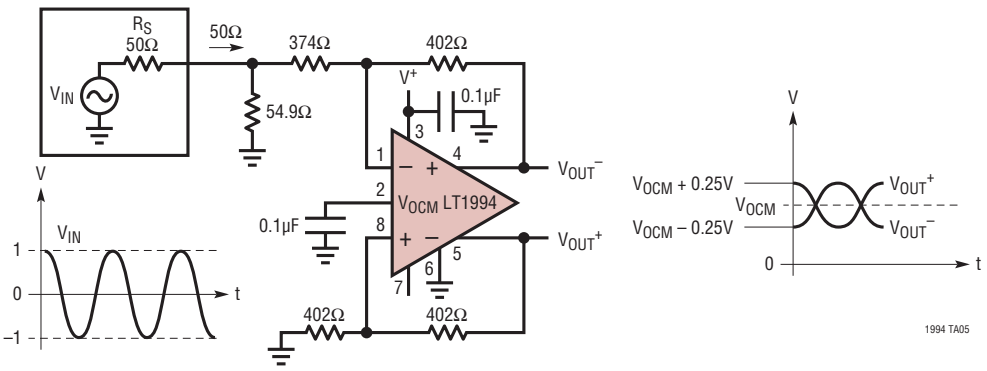
Example: The specified –3dB frequency is 1MHz Gain = 1

1. Using f_{3dB} = 1000kHz, $C2_{abs}$ = 400pF
2. Nearest standard 5% value to 400pF is 390pF and C21 = C22 = 390pF and C11 = 3900pF
3. Using f_{3dB} = 1000kHz, C2 = 390pF and Gain = 1, R1 = 549Ω, R2 = 549Ω and R3 = 15.4Ω (nearest 1% values). R11 = R21 = 549Ω, R21 = R22 = 549Ω and R31 = R32 = 15.4Ω.

Note 1: The equations for R1, R2, R3 are ideal and do not account for the finite gain bandwidth product (GBW) of the LT1994 (70MHz). The maximum gain is set by the C1/C2 ratio (which for convenience is set equal to ten).

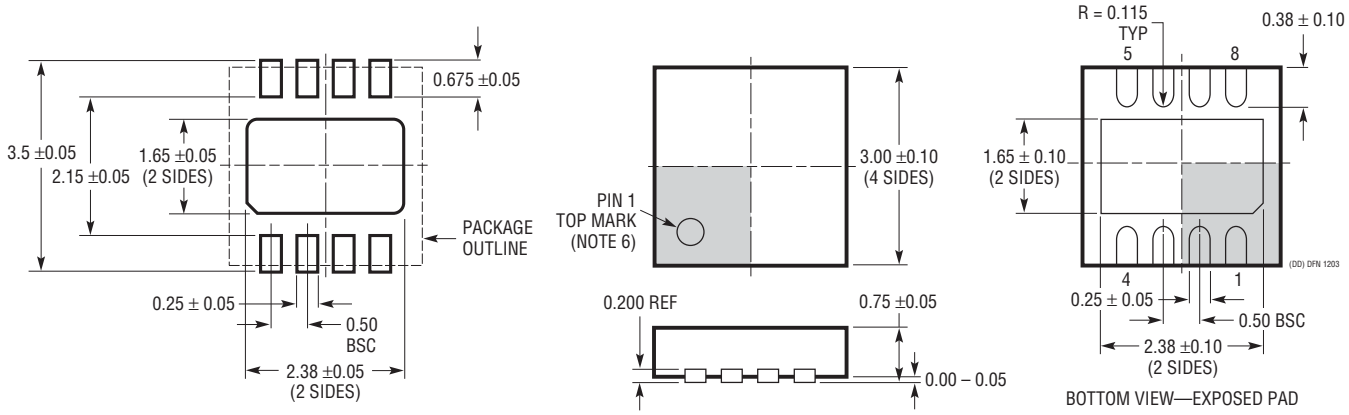
Note 2: The calculated value of a capacitor is chosen to produce input resistors less than 600Ω. If a higher value input resistance is required then multiply all resistor values and divide all capacitor values by the same number.

A Single-Ended to Differential Voltage Conversion with Source Impedance Matching and Level Shifting



PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)

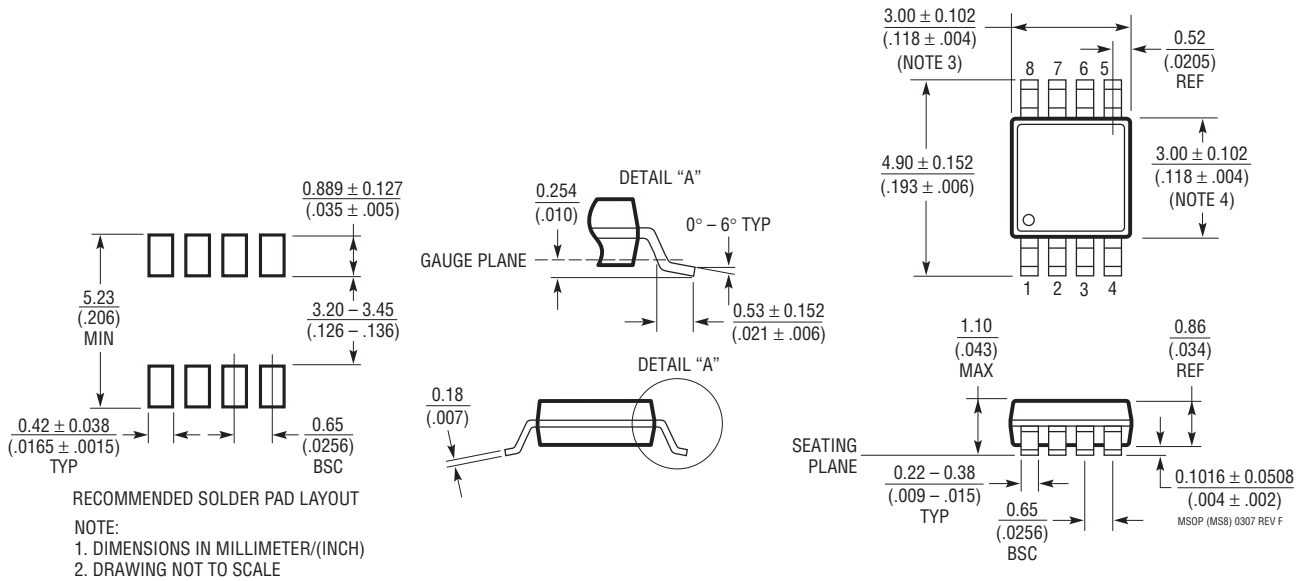


BOTTOM VIEW—EXPOSED PAD

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)

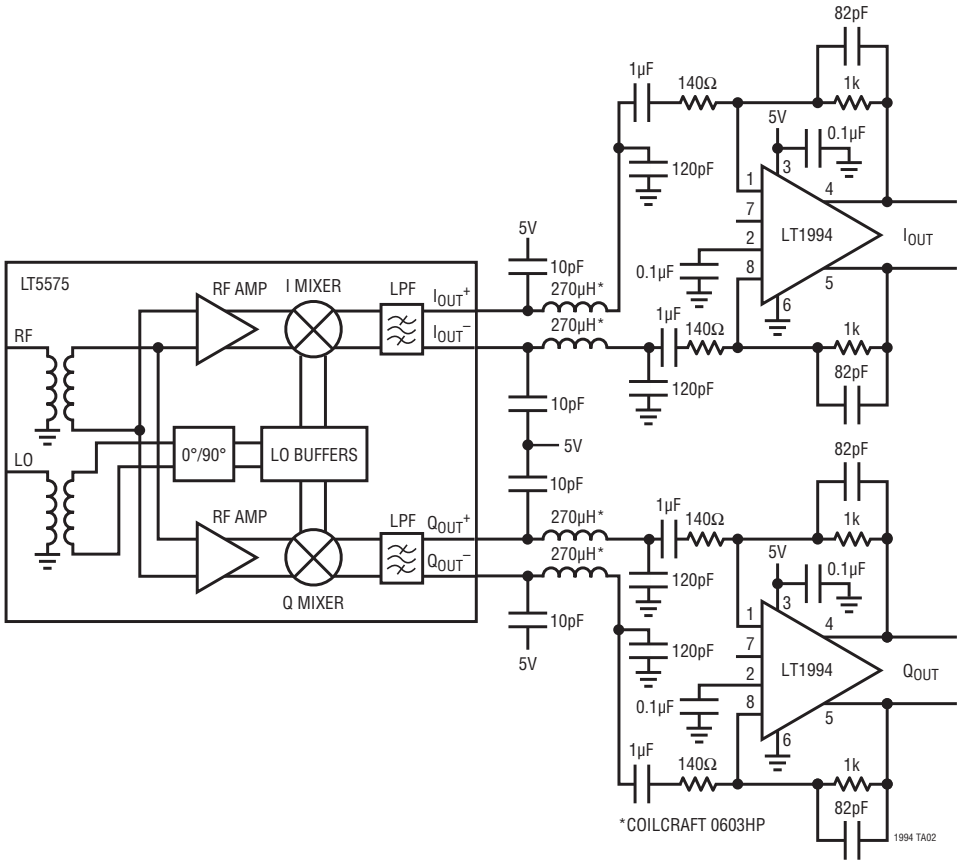


RECOMMENDED SOLDER PAD LAYOUT

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

RFID Receiver Front-End, 1kHz < –3dB BW < 2MHz
(Baseband Gain = 5)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1167	Precision, Instrumentation Amp	Single Gain Set Resistor: G = 1 to 10,000
LT1806/LT1807	Single/Dual Low Distortion Rail-to-Rail Amp	325MHz, 140V/µs Slew Rate, 3.5nV/√Hz Noise
LT1809/LT1810	Single/Dual Low Distortion Rail-to-Rail Amp	180MHz, 350V/µs Slew Rate, Shutdown
LT1990	High Voltage Gain Selectable Differential Amp	±250V Common Mode, Micropower, Gain = 1, 10
LT1991	Precision Gain Selectable Differential Amp	Micropower, Pin Selectable Gain = –13 to 14
LTC1992/LTC1992-x	Fully Differential Input/Output Amplifiers	Programmable Gain or Fixed Gain (G = 1, 2, 5, 10)
LT1993-2/-4/-10	Low Distortion and Noise, Differential In/Out	Fixed Gain (G = 2, 4, 10)
LT1995	High Speed Gain Selectable Differential Amp	30MHz, 1000V/µs, Pin Selectable Gain = –7 to 8
LT1996	Precision, 100µA, Gain Selectable Differential Amp	Pin Selectable Gain = 9 to 117
LTC6403	Low Noise, Low Power Fully Differential Amp	11mA Supply Current
LTC6404-1/LTC6404-2 LTC6404-4	600MHz AC Precision Fully Differential Amp	Available H-Grade (–40°C to 125°C)
LT6600-2.5/-5/-10/-15/-20	Differential Amp and Lowpass, Chebyshev Filter	Filter Cutoff = 2.5MHz, 5MHz, 10MHz, 15MHz or 20MHz

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