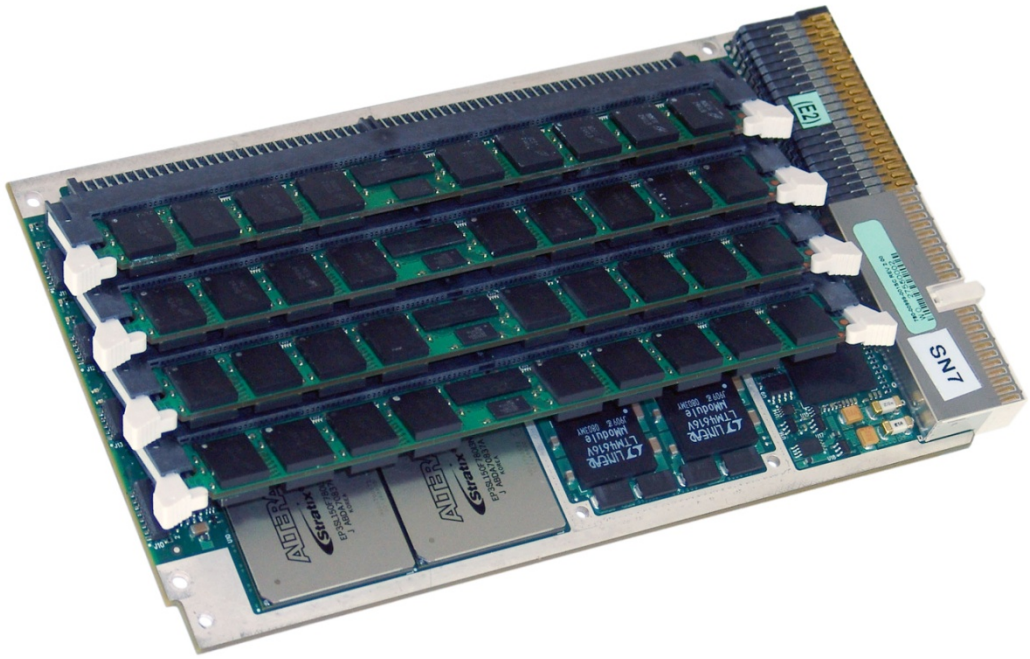
Digital Receiver Technology, Inc.

Approved for Public Release

DEL1
Delay Memory Module 1



DESCRIPTION

The Delay Memory Module 1 (DEL1) can accept up to two wideband digital IF (DIF) data streams via the backplane and output time-delayed data streams for use in signal processing applications on other system modules. The maximum time delay for one wideband DIF data stream is 178 seconds at 96 MHz. Two DIF data streams can each be delayed for half of this time. Additional delay can be achieved by cascading multiple DEL1 modules within a system. The real-time delay is achieved using high-speed volatile Registered Dual In-Line Memory Modules (RDIMMs) along with Field Programmable Gate Arrays (FPGAs) for data stream routing and processing. The total memory depth is 32 Gigabytes (GB) per DEL1.

The DEL1 control processor monitors device status and has a built-in CompactPCI (cPCI) bus interface allowing module control by the system controller. The DEL1 RDIMM memory controller is implemented within an FPGA for maximum flexibility. The DEL1 generates all internal non-standard voltages and only requires the standard +3.3V and +5.0V cPCI voltages from the system backplane. It occupies one 3U cPCI slot within DRT1000C and DRT2000C systems and has heat sink covers to ensure adequate cooling.

Features

- Four 8GB RDIMMs (Micron MT72HVQ1G72P) provide for delay storage giving a total of 32GB of delay memory. Each RDIMM contains large banks of quad-ranked DDR2 SDRAM which can sustain a 3200 MB/s interface data rate. This fast data rate allows extended power-down periods for the SDRAM which reduces overall power consumption.
- High-Performance Fixed-Point Digital Signal Processor (Texas Instruments C6424) running at 400 MHz core frequency provides the latest generation DSP core for increased processing and improved power efficiency.
- Two large FPGAs (Altera Stratix-3 SL150) allow flexible routing of wideband DIF data streams with up to two input and two delayed output data streams via the backplane.
- High Speed Hard Metric (HSHM) J2 backplane connector for improved backplane signal integrity.
- cPCI (Rev 2.1) compliant interface.
- Software controlled on-board temperature and power measurement along with built-in test capability.
- Future enhancements possible via FPGA firmware upgrades. The FPGAs contain DSP blocks for processing applications and can also decimate/interpolate the data stream for increased time delay for smaller bandwidth signals.

Physical/Environmental

- **Operating Temperature Range** — -20°C to +60°C (-4°F to +140°F) inlet air temperature of any DRT system in which the module is installed
- **Size** — Single-slot: 0.8 in (20.32 mm) wide
3U: 3.9 in x 6.2 in (100 mm x 160 mm)
- **Weight** — ~726g (1.6 lbs) with Heat Sink
- **Power Consumption** — ~25 Watts (typical)

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