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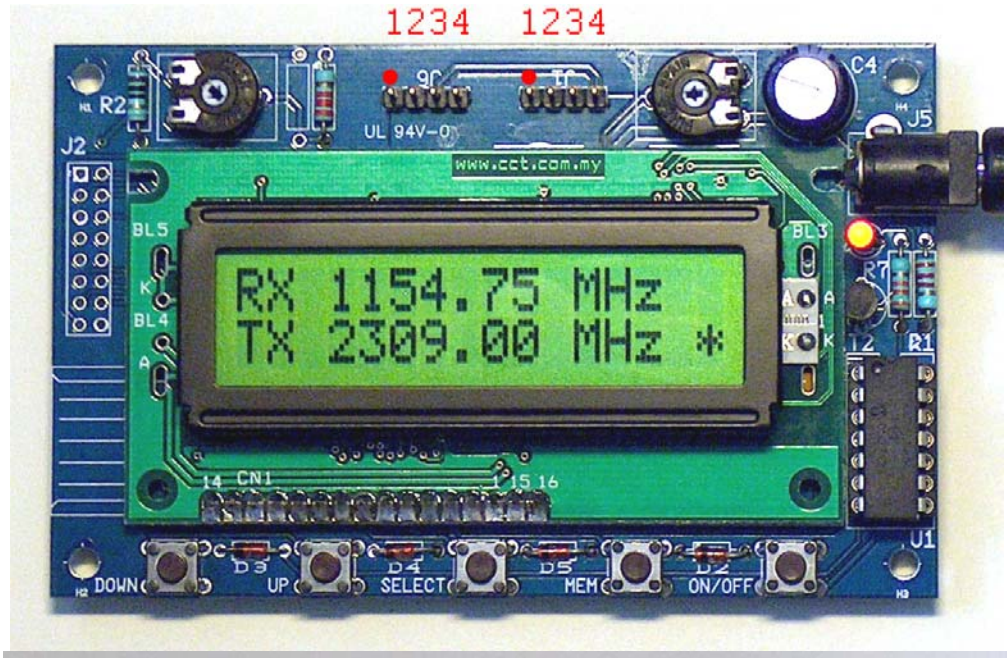
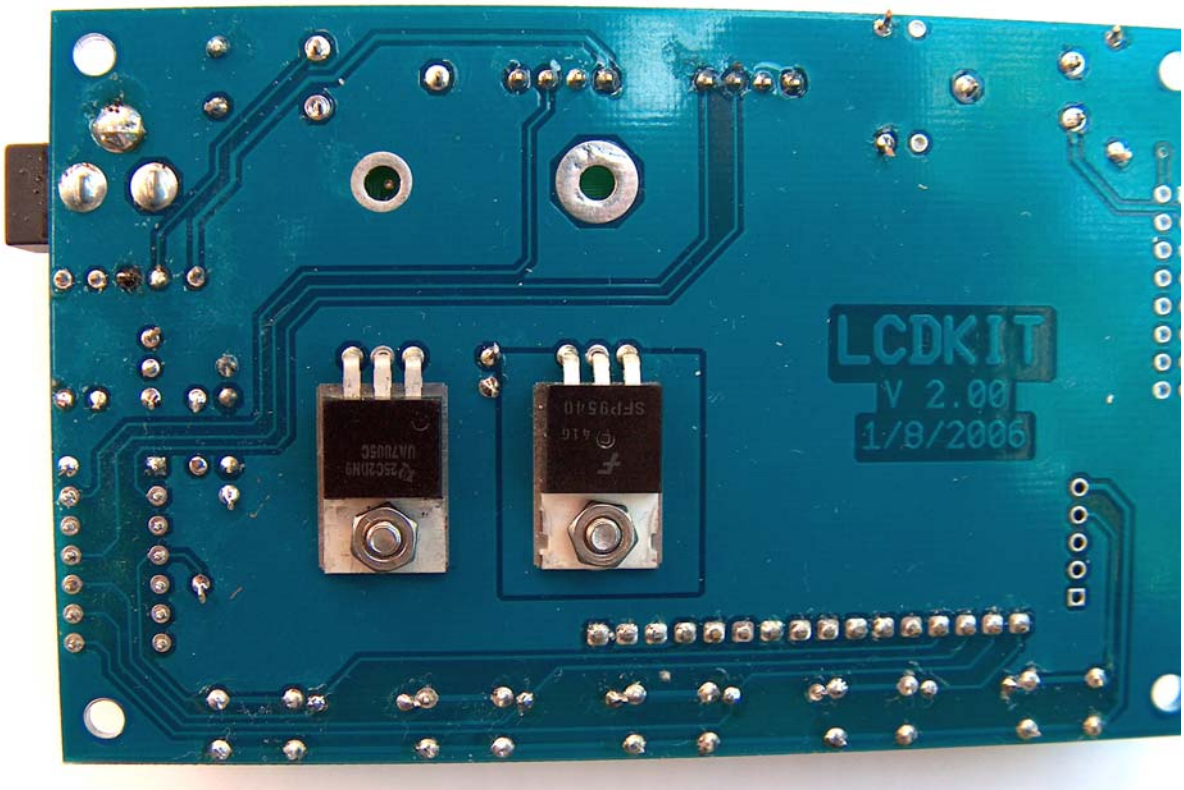
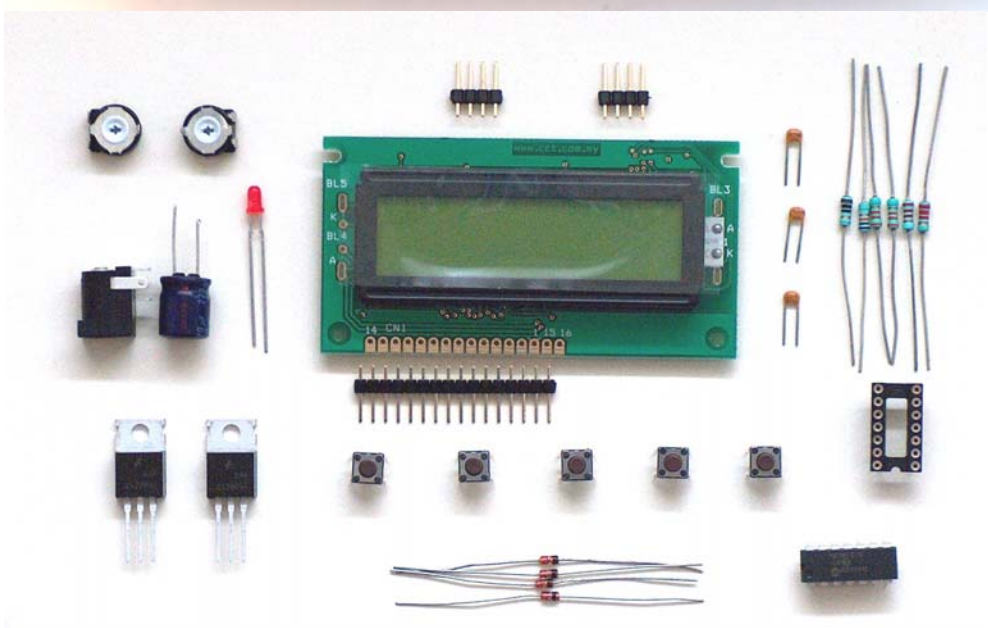
ATV LCD KIT FOR DFM BOARDS

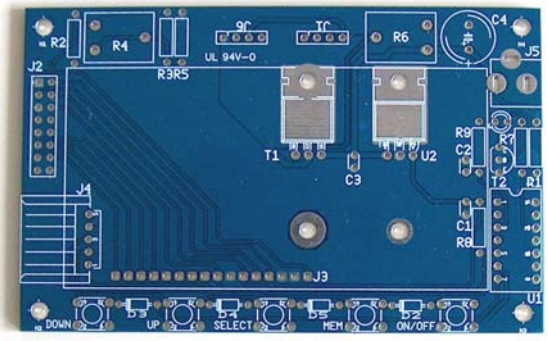


Receiver Frequency and S-Meter Readout

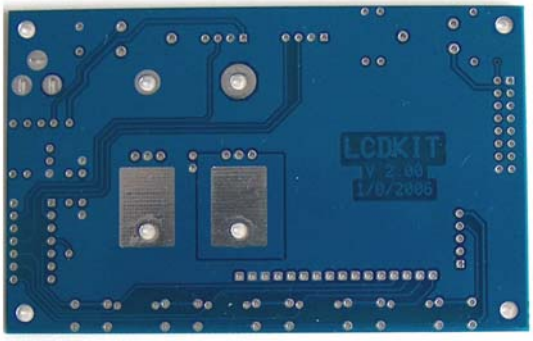
Receiver and Transmitter Frequency Readout





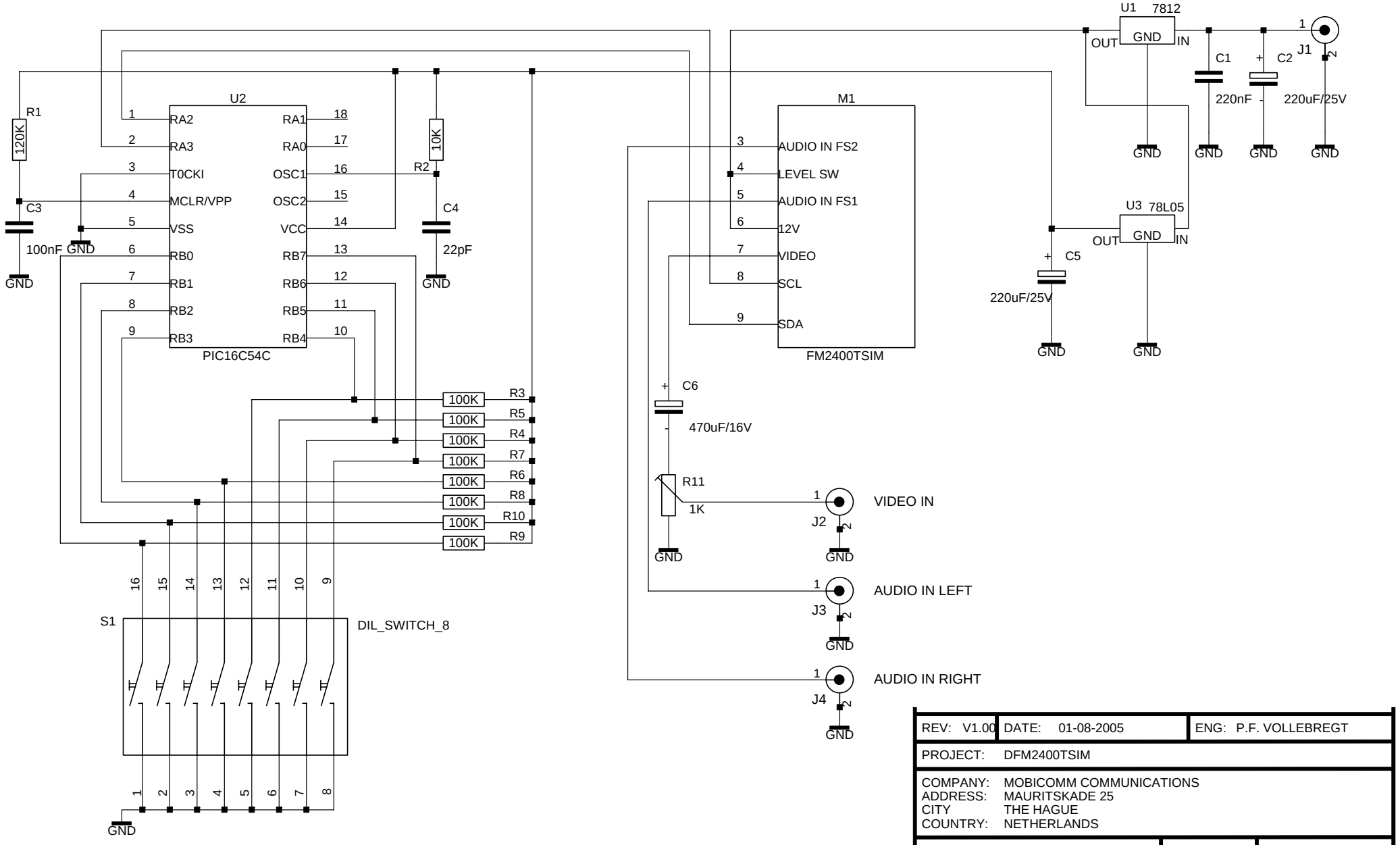


Top Layer



Bottom Layer

DFM2400TSIM



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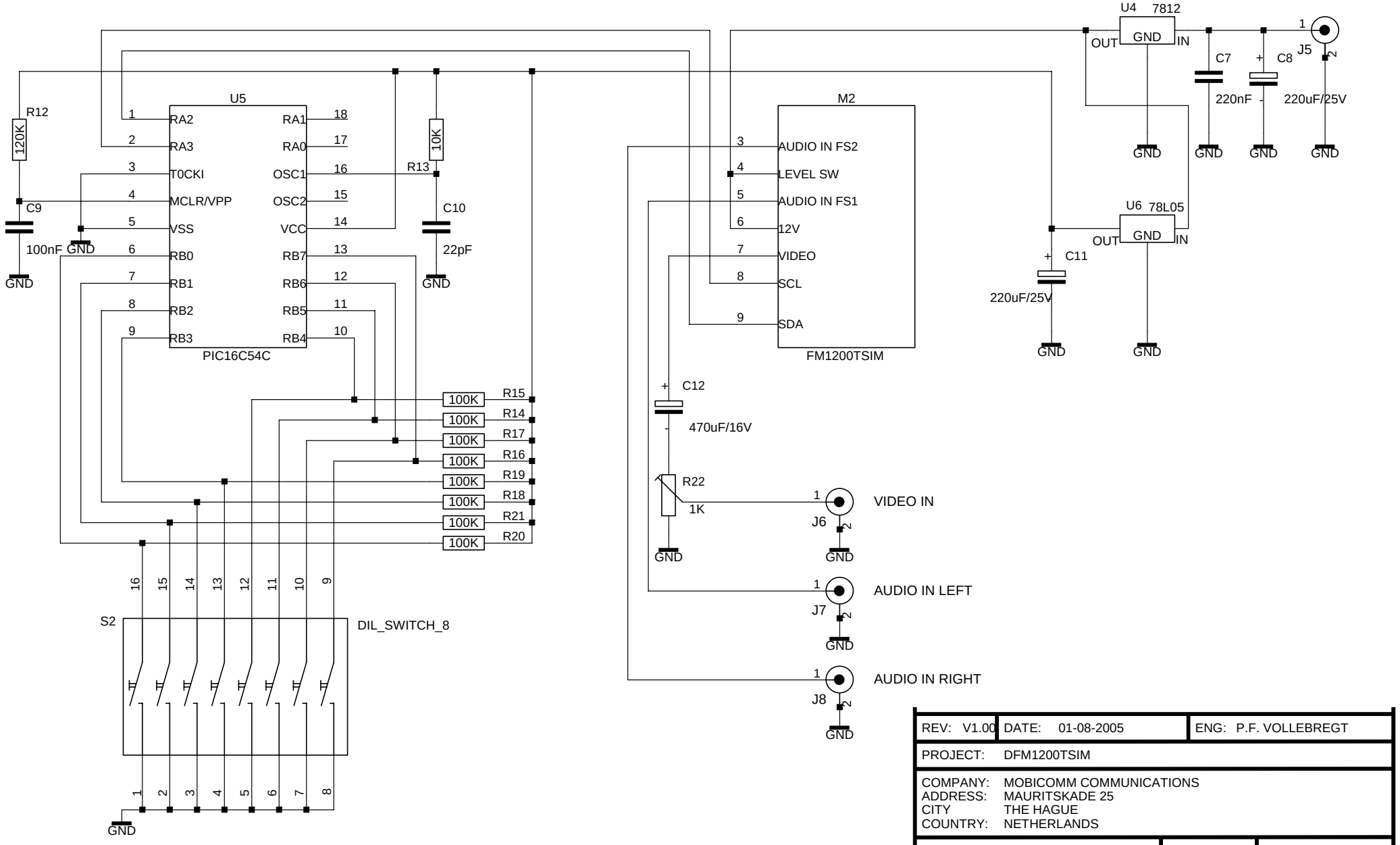
PROJECT: DFM2400TSIM		
COMPANY: MOBICOMM COMMUNICATIONS ADDRESS: MAURITSKADE 25 CITY THE HAGUE COUNTRY: NETHERLANDS		
INITIAL 01-08-2005	PAGE: 1	OF: 1

DFM1200TSIM



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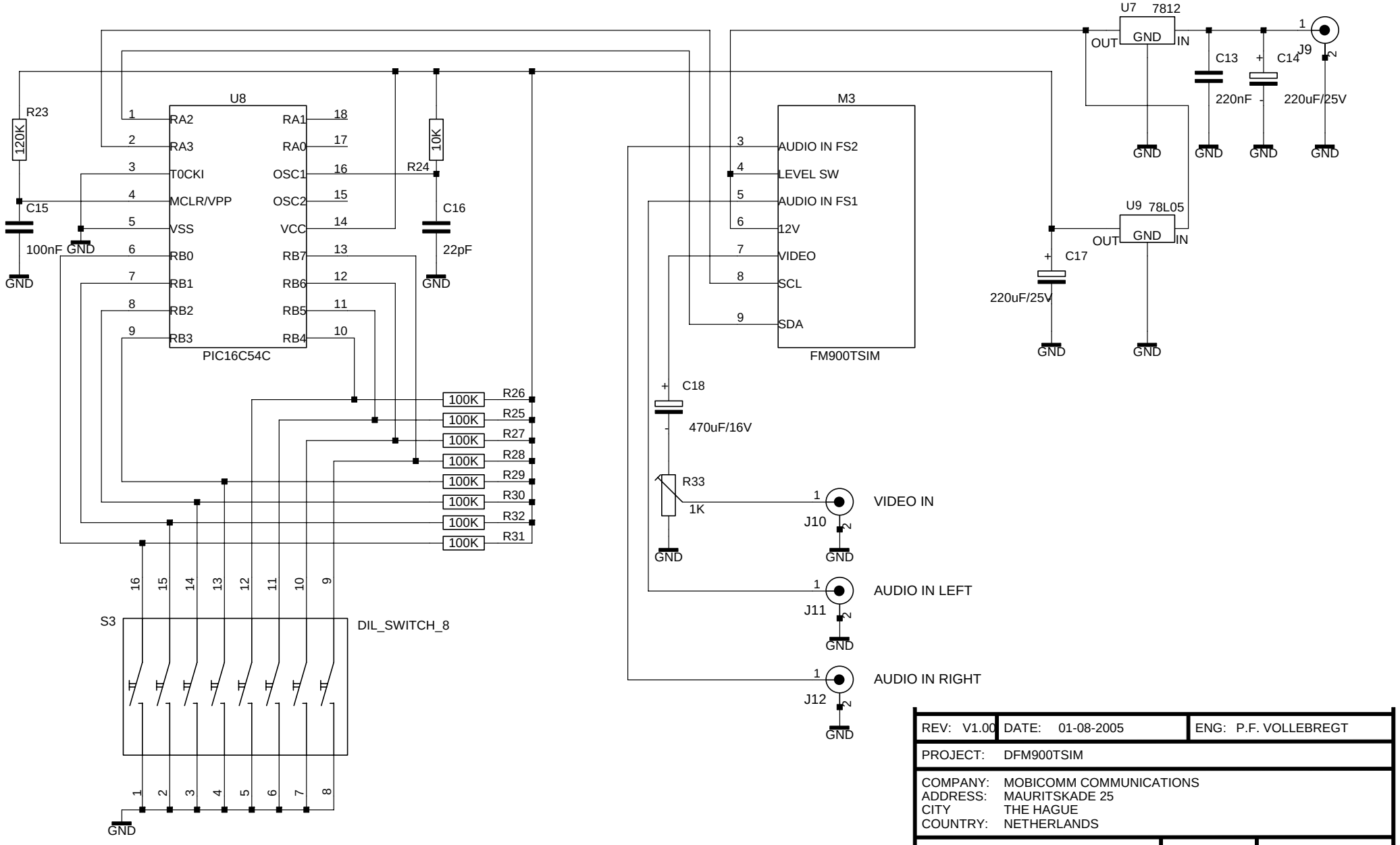
PROJECT: DFM1200TSIM		
COMPANY: MOBICOMM COMMUNICATIONS ADDRESS: MAURITSKADE 25 CITY THE HAGUE COUNTRY: NETHERLANDS		
INITIAL 01-08-2005	PAGE: 1	OF: 1

DFM900TSIM



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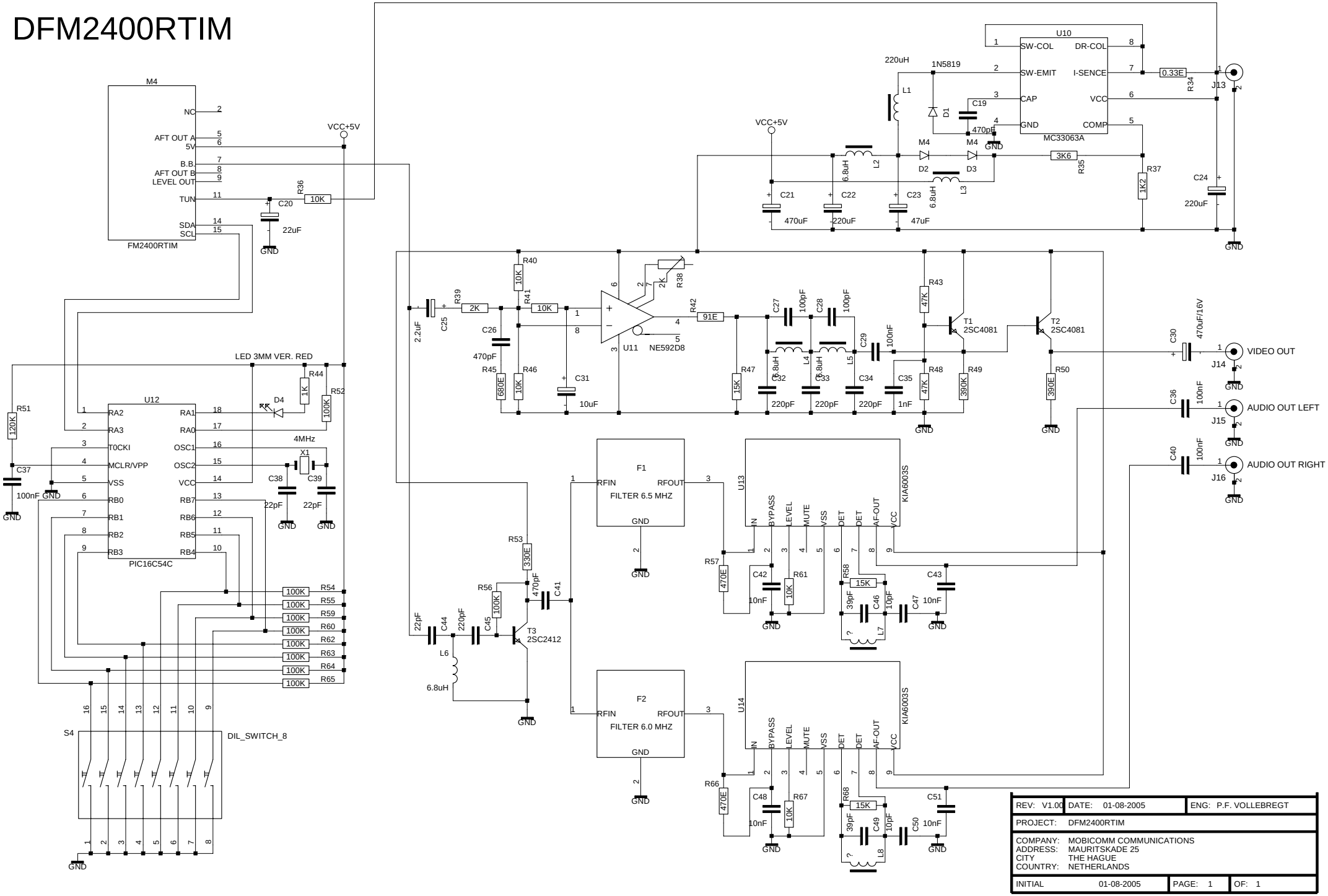
PROJECT: DFM900TSIM		
COMPANY: MOBICOMM COMMUNICATIONS ADDRESS: MAURITSKADE 25 CITY THE HAGUE COUNTRY: NETHERLANDS		
INITIAL 01-08-2005	PAGE: 1	OF: 1

DFM2400RTIM



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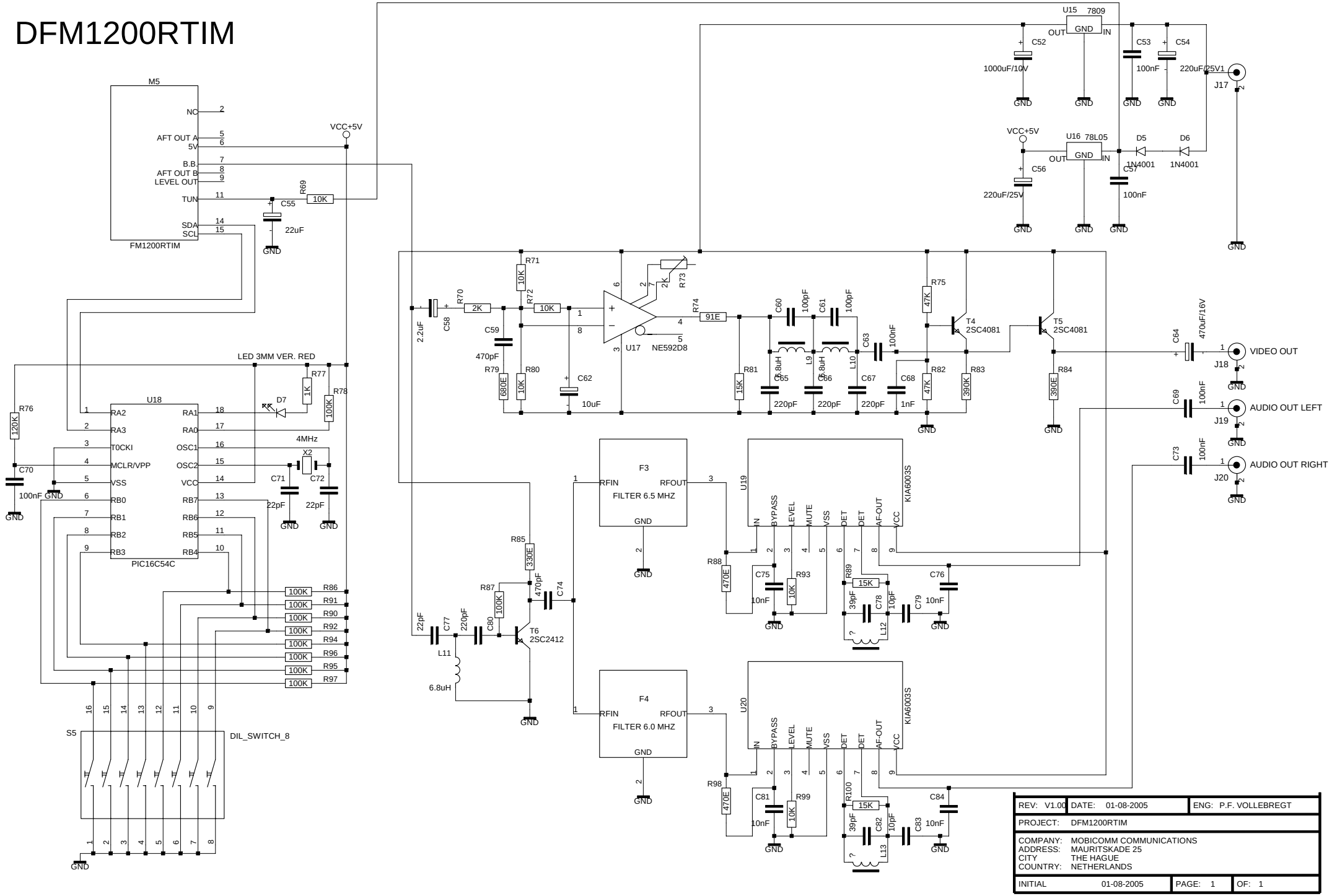
PROJECT: DFM2400RTIM			
COMPANY: MOBICOMM COMMUNICATIONS ADDRESS: MAURITSKADE 25 CITY THE HAGUE COUNTRY: NETHERLANDS			
INITIAL 01-08-2005	PAGE: 1	OF: 1	

DFM1200RTIM



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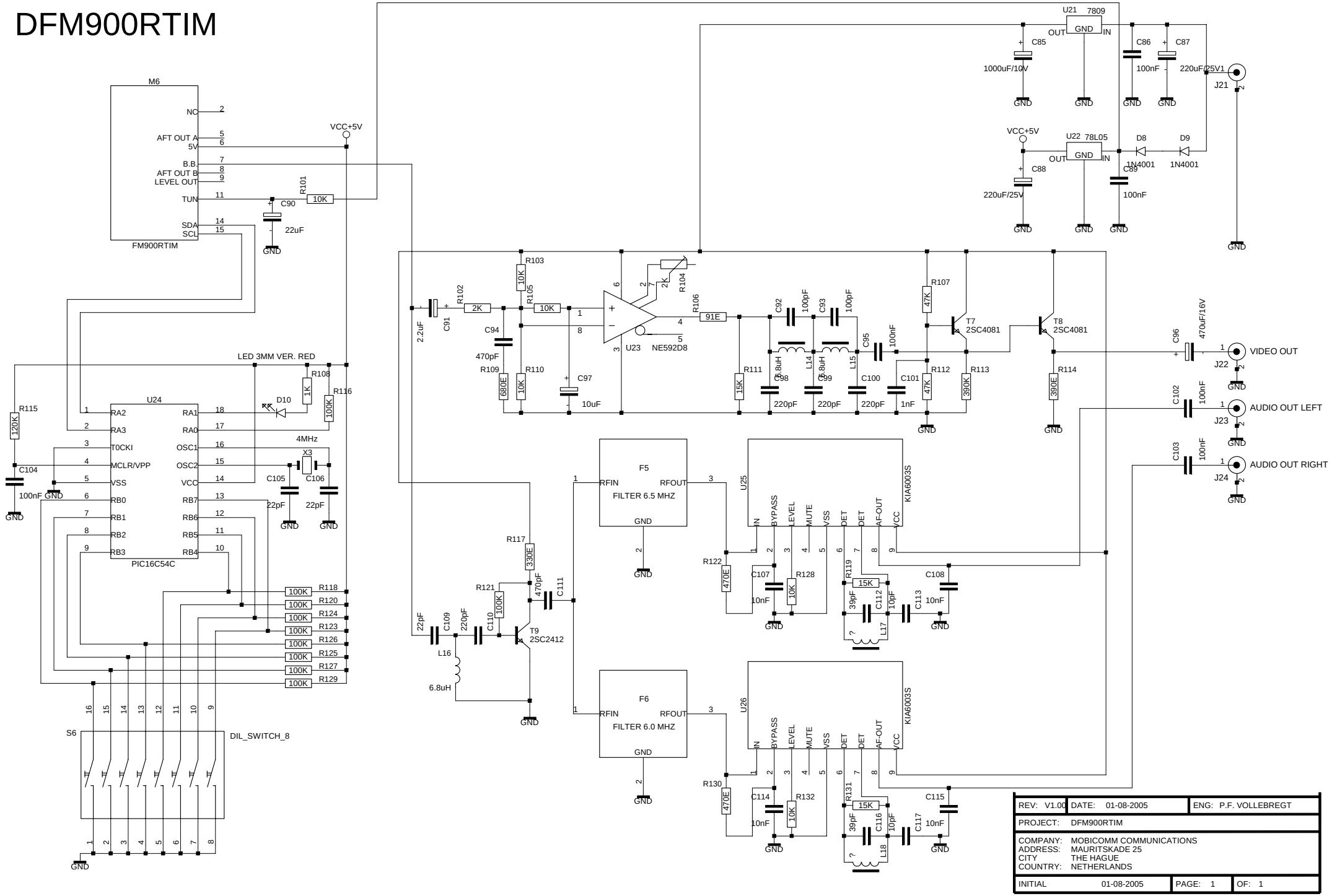
PROJECT:	DFM1200RTIM		
COMPANY: MOBICOMM COMMUNICATIONS ADDRESS: MAURITSKADE 25 CITY THE HAGUE COUNTRY: NETHERLANDS			
INITIAL	01-08-2005	PAGE: 1	OF: 1

DFM900RTIM



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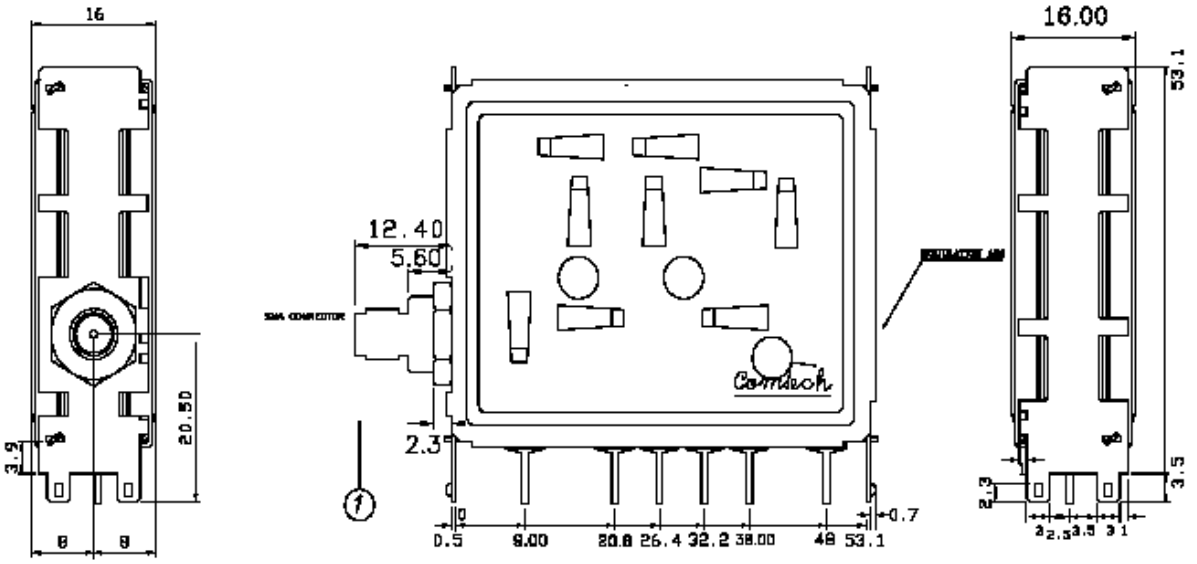
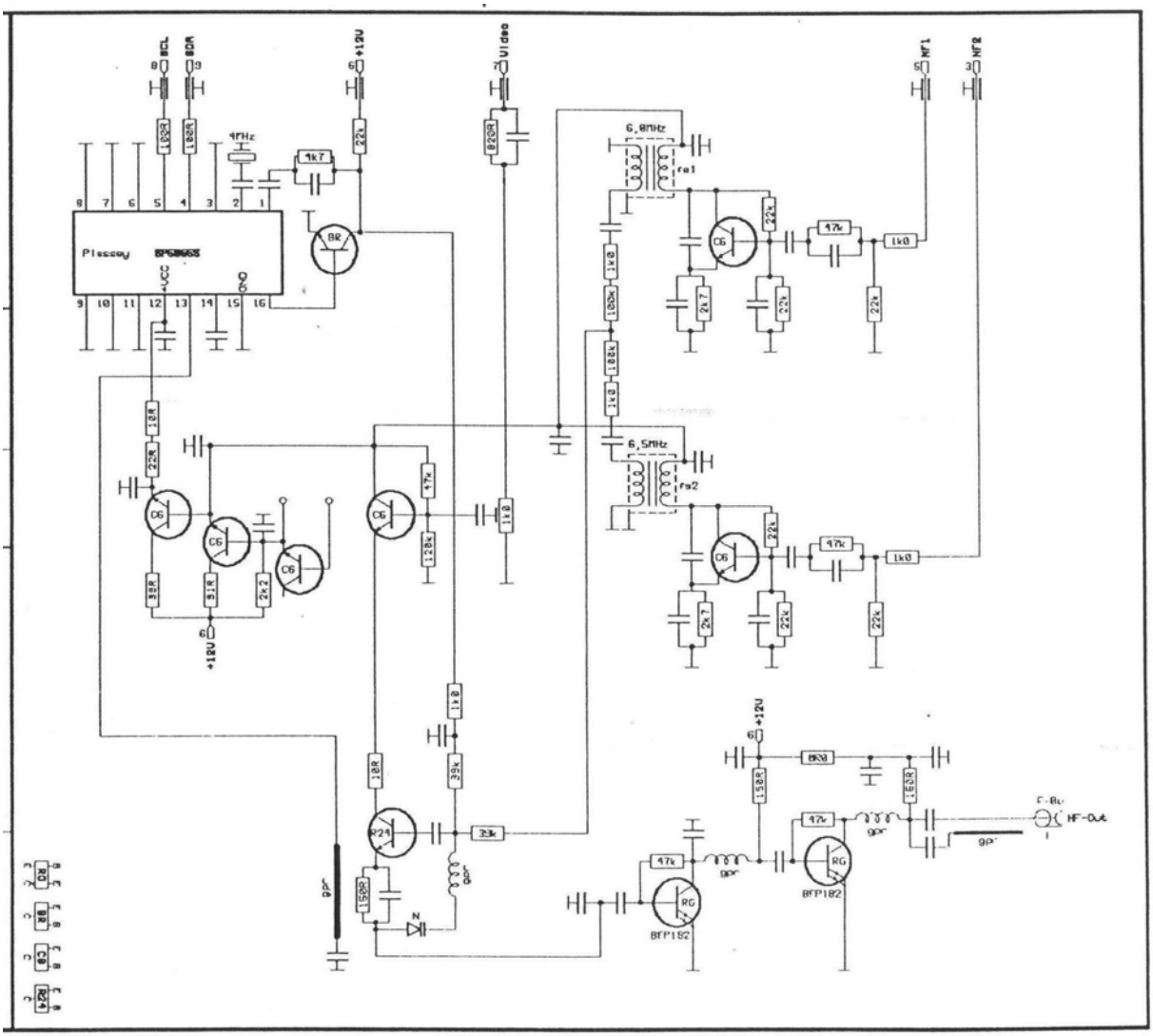
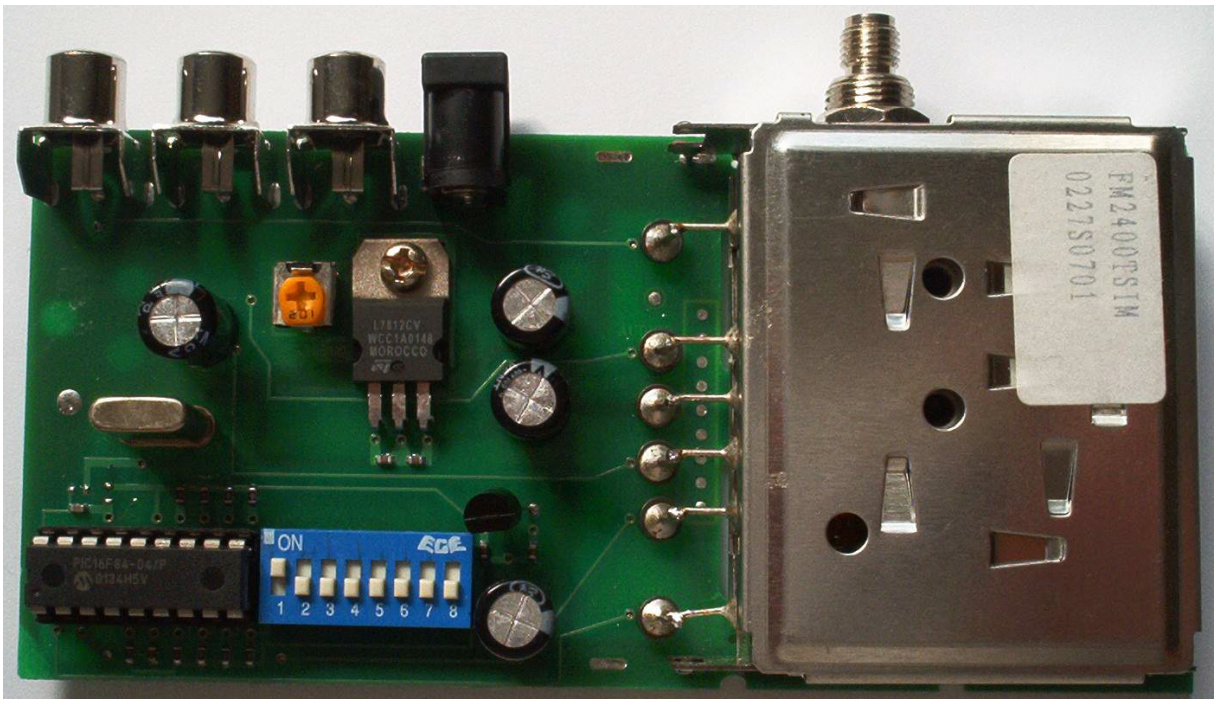
COMPANY: MOBICOMM COMMUNICATIONS ADDRESS: MAURITSKADE 25 CITY THE HAGUE COUNTRY: NETHERLANDS			
INITIAL 01-08-2005		PAGE: 1	OF: 1

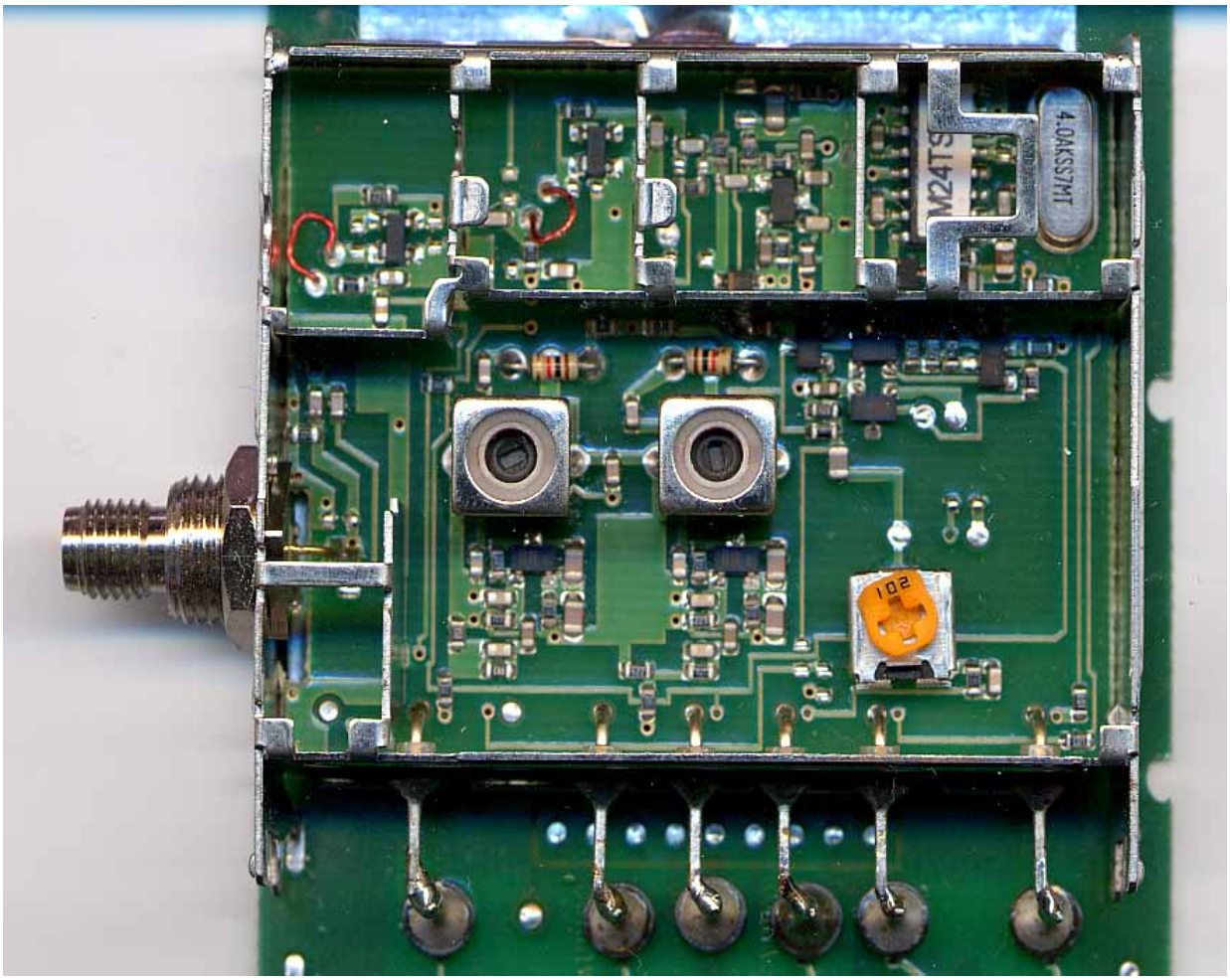
FM900TSIM, FM1200TSIM, FM2400TSIM



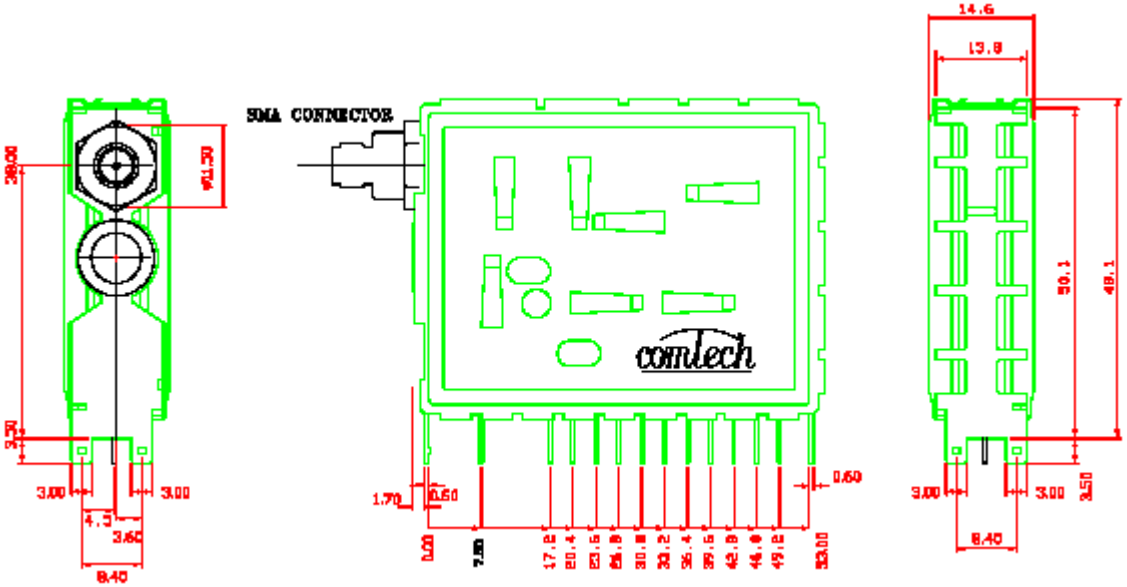


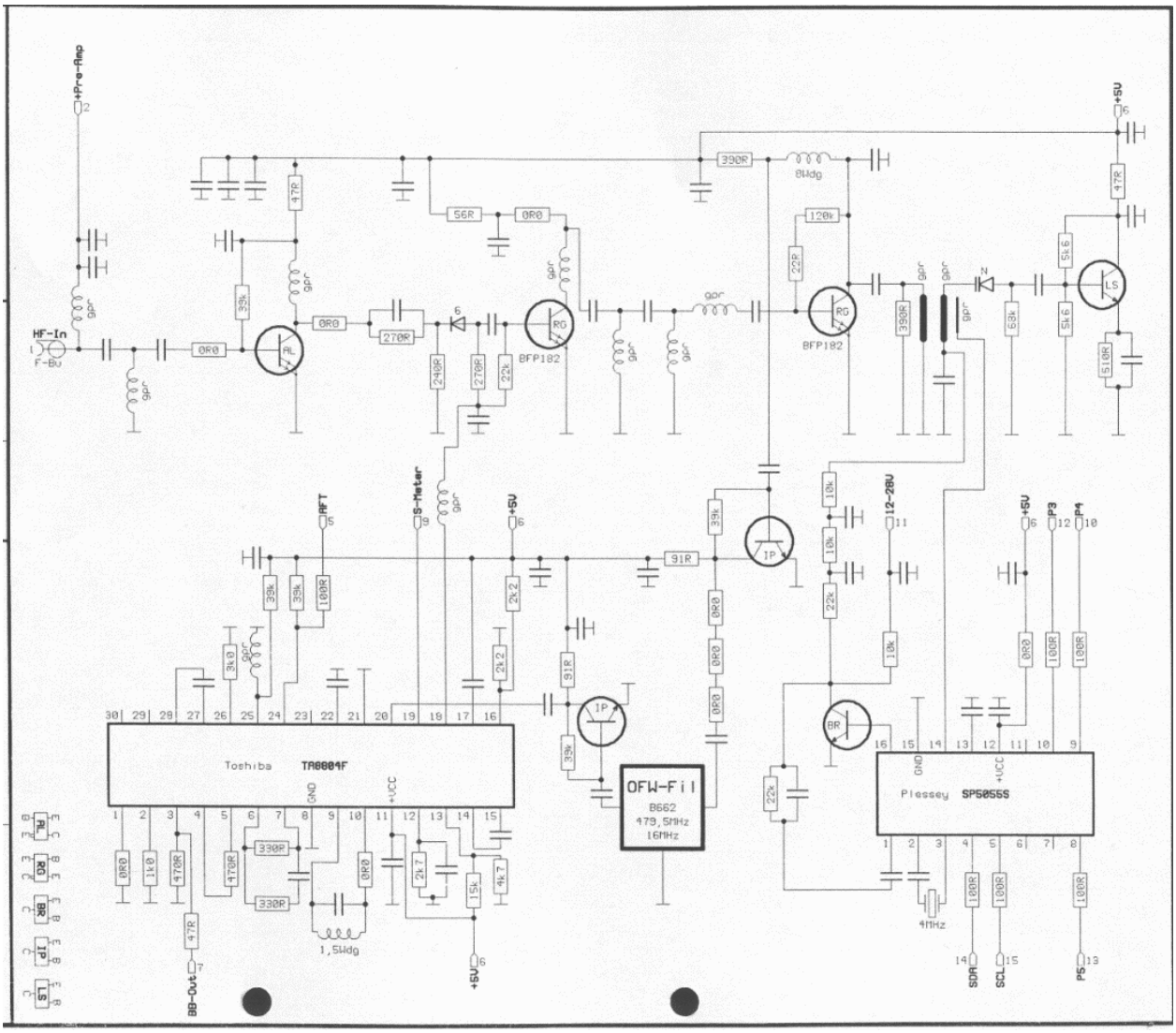
DFM900TSIM, DFM1200TSIM, DFM2400TSIM



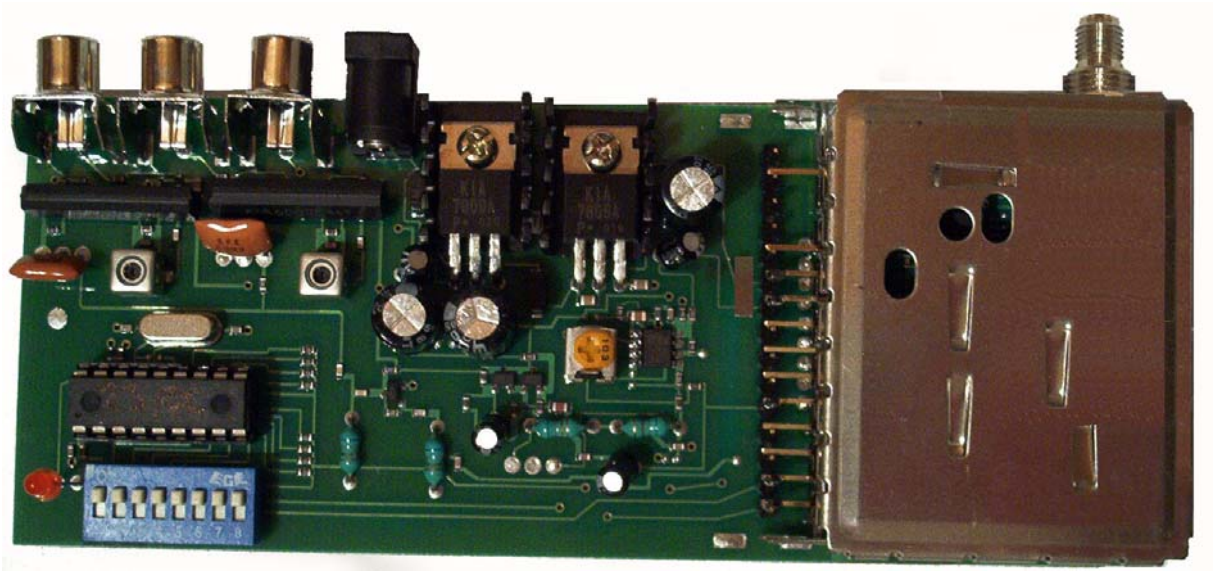


DFM900RTIM, DFM1200RTIM, DFM2400RTIM

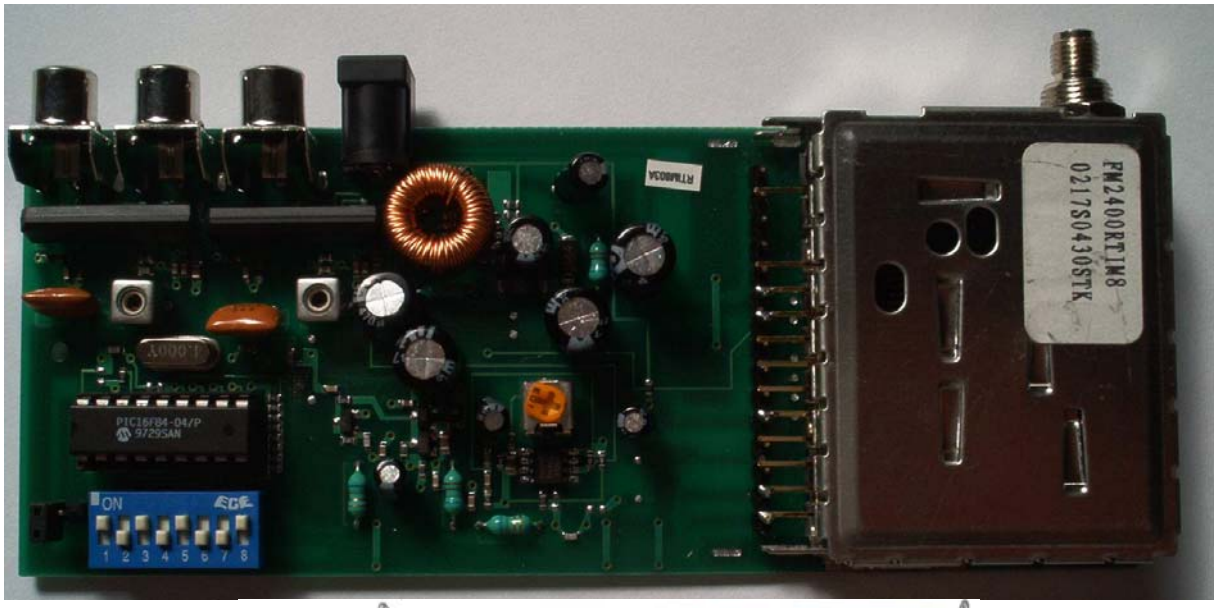


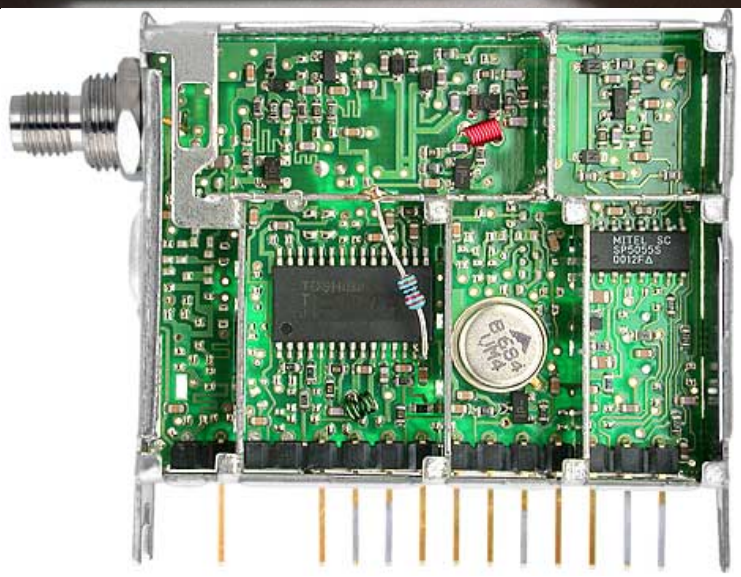


DFM900RTIM, DFM1200RTIM



DFM2400RTIM





1. SCOPE

This specification outlines the pertinent electrical requirements of the RF output modulator which converts the FM video and FM audio signal into the RF signal for television standard transmission system.

2.GENERAL SPECIFICATIONS

2-1. Output frequency 950 ~1200MHz (I^2C PLL controller from outside)

2-2. Supply voltage 12V+/-0.2V

2-3. Consumption current 140+/-20mA

2-4. Operation and storage Temperature 0-50°C

Conditions for guarantee Humidity 85% or less

3.Test Conditions

3-1. Testing ambient conditions

Defined as temperature of 25+/-2°C and humidity of 65+/-5% RH.

Note : that temperatures of 5-30°C and humidity of 45-85%RH may be regarded as standard.

3-2. Unit setting conditions

(1). Picture --10 step wave signal 1.0Vp-p(82Ohm load)

(2). Audio -- 1.0Vp-p of sine wave 1KHz

4. Electrical Performance

4-1. Video system characteristics

	parameter	Specification Min	Typ	Max	Unit	Remark
4-1-1	Input impedance		1.7k		Ohm	Measure at 0.5-5MHz
4-1-2	Input signal level		1.0		Vp-p	Load of 82ohm connected Negative synchronous
4-1-3	Modulation 950 Sine Wave 1000 10KHz 1Vp-p 1050 1100 1150 1200	6	8 6 6 6 7	10 6	MHz	Superimposed sinuous wave. (3.58mhz) is 20% of the step input level. measure under the apl of 10-90% differential gain of demodulator unit is to be compensated
4-1-4	Differential gain	-8		8	%	
4-1-5	Differential phase	8		8	deg	-ditto-
4-1-6	S/N	45			dB	Measure with respect to standard demodulator output.
4-1-7	Out level taper		4	6	dB	fp 950~1200MHz
4-2. Audio system characteristics						
4-2-1	Input impedance		1.4		KOhm	Measure at 0.1-10KHz
4-2-2	Modulation	35	40	45	KHz	
4-2-3	Distortion factor			3	%	Audoi input signal 1.0Vp-p 1KHz modulation 50% (sine wave) video input signal all black (sync.only) use standard demodulator of inter -carrier system. De-emphasis(50 usec) is on.
4-2-4	S/N	40			dB	The same as 4-2-3

4-3. Output system characteristics

	Parameter	Specification Min	Typ	Max	Unit	Remark
4-3-1	Video carrier frequency	50	fp	+50	KHz	Test at 25^{O}C temperature and 65%RH of humidity Fs1 6.0 MHZ Fs2 6.5 MHz *output channel
4-3-2	Video output level 950~1200MHz	14	16	18	dBm	
4-3-3	Audio output level difference(p/s ratio) fp:950~1200MHz	22	27	32	dB	
4-3-4	Audio carrier frequency	-8 -8	fs_1 fs_2	+8 +8	KHz KHz	Input signal none the measurement is taken after 30 sec. from the power-on.
4-3-5	Audio modulator fs1 fs2	60	70	80	KHz	Measurement difference video of carrier frequency output level for 0-1ghz. except to fp. fp+/-fs . against video carrier output level.
4-3-6	Out-band spurious	45	50		dB	
4-3-7	Output impedance		75		Ohm	Unbalanced.

5-1. PLL section characteristics

No	Item	Specification	notes
5-2.	IIC Bus (1) SDA.SCL Input voltage	Under standard test condition	V
	(2) Address	C2 (on write date format)	
	(3) SDA.SCL Input impedance	SDA/SCL are in the high impedance and there should be no reliablity problem with 5V continually on the SDA/SCL,if power supply is switched off.	

Condition	Min	Typ	Max
High voltage	3		5
Low voltage	0		1.5

(4) Data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	Byte1
Programmable Divider	0	14 2	13 2	12 2	11 2	10 2	9 2	8 2	A	Byte2
Programmable Divider	7 2	6 2	5 2	4 2	3 2	2 2	1 2	0 2	A	Byte3
Charge pump and test bits	1	(0) cp	t1	t0	1	1	1	(0) os	A	Byte4
I/O port control bits	p7	p6	p5	p4	p3	p2	p1	p0	A	Byte5

Table 1 write data format (MSB is transmitted first)

Address	1	1	0	0	0	MA1	MA2	1	A	Byte1
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	A	Byte2

Table 2 read date format

A: Acknowledge bit.

MA1,MA0: Voltage address bits.

CP: Charge pump current select.

T1: Test mode selection,T0: Charge pump disable

OS: Varactor drive output disable switch.

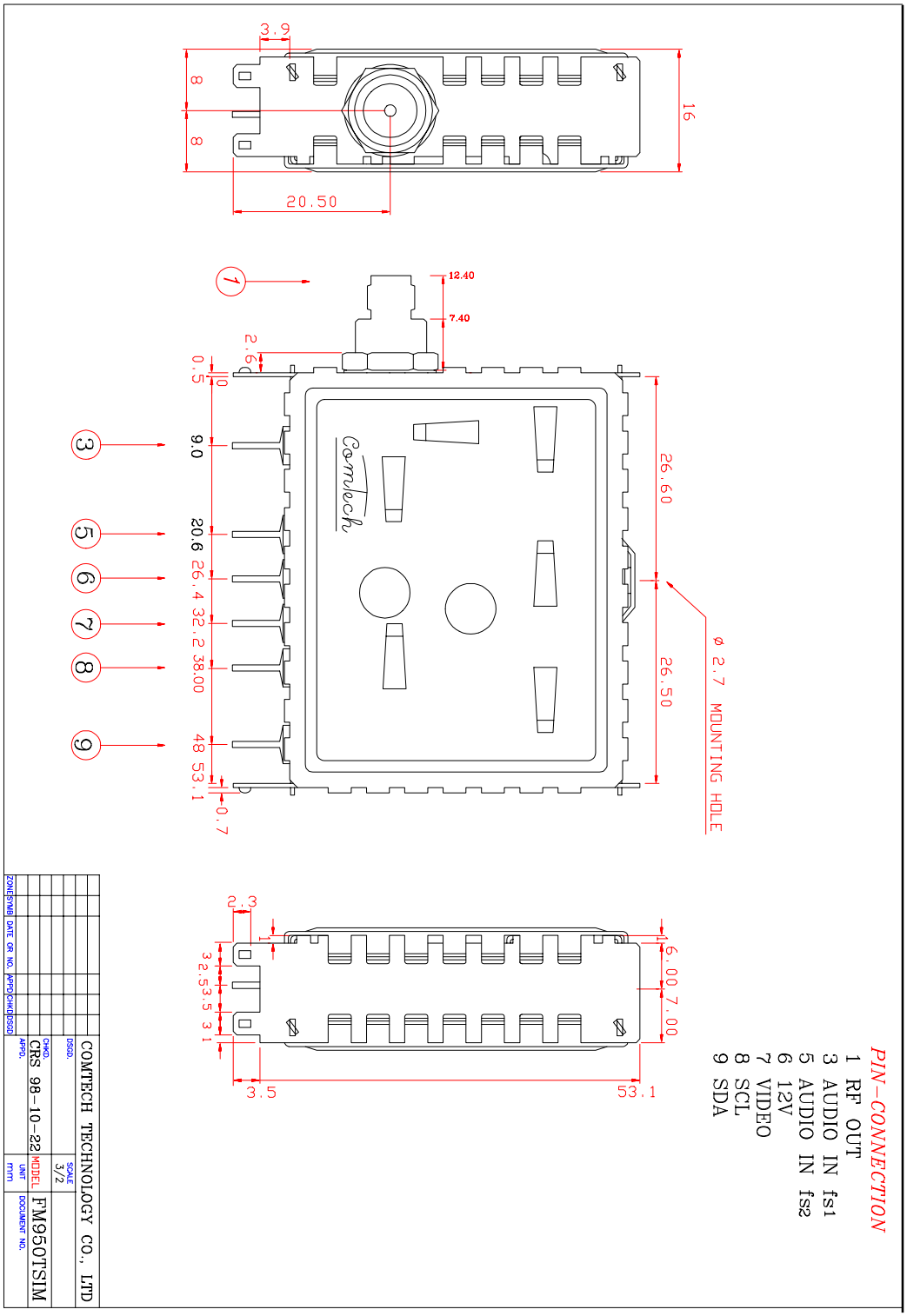
P7,P6,P5,P4,P3,P2,P1,P0: Control output states.

POR: Power on reset indicator

FL: Phase lock detect flag

I2,I1,I0: Digital information from ports P7,P5,and P4.

A2,A1,A0: 5 level adc data from P6


PIN-CONNECTION
1 RF OUT
3 AUDIO IN fs1
5 AUDIO IN fs2
6 12V
7 VIDEO
8 SCL
9 SDA
ø 2.7 MOUNTING HOLE
COMTECH TECHNOLOGY CO., LTD
FM950TSIM
CRS 98-10-22
SCALE 3/2
UNIT mm

1. General Specification

1-1 Input Frequency Range	900 MHz - 1650 MHz	
1-3 One Input Connector	F Fe-Male	
1-4 Nominal Input Impedance	75 Ohm	**Note:**
1-5 Tuning Circuit	Built-in PLL	SP5055
1-6 IF Frequency	479.50 MHz Center	(PLESSEY)
1-7 IF Bandwidth	18 MHz Nominal (Selectable)	**Note:**
1-8 Demodulation	Phase Locked Loop	TA8804F
1-9 Video Output Polarity	Positive Going	
1-10 Operating Voltage	+12V (+/-5%)	
	+5V (+/-5%)	
1-11 Operating Temperature	-10°C ~ +60°C	
1-12 Operating Humidity	less than 80% R. H. (at 40°C)	
1-13 Storage Temperature	-20°C ~ +70°C	
1-14 Storage Humidity	less than 95% R. H. (at 40°C)	

2. Standard Test Condition

test for electrical specification shall be preformed at following condition unless otherwise specified.

2-1 Ambient Condition

Temperature 25°C +/- 2°C
Humidity 65% +/- 5% R. H.
if no doubt on test results
Temperature +5°C ~ +30°C
Humidity 45% ~ 80% R. H.
could be applied

2-2 Measurement to Start

30 minutes after DC power supplied

2-3 Power Supply

Terminal	Supply Voltage
+5V	+5V (+/-) 0.1V
TU	+12V (+/-) 0.1V
SDA	specified tuning
SCL	pulse

3. Current Consumption

Terminal	Min.	Typ.	Max.	Unit
+5V	190	240	290	mA
TU	0.5	1.0	3.0	mA

4. Absolute Maximum Voltage

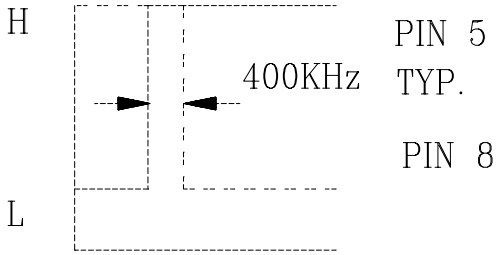
Terminal	Max. Supply Voltage
LNB Power	DC +25V
+5V	DC +5.25V
TU	DC +15V
SDA,SCL	OV TO The Same Voltage AS +5V Terminal

Terminal	Max. Take Off Current
LNB Power	500mA
B. B. Output	0.5 mA

5. Electrical Specification

under standard test condition
Test Channel: DBS 20 CH
Input Level: -45 dBm
unless otherwise specified

	Condition	Min.	Typ.	Max.	Note
5-1 Input VSWR	900 ~ 2050 MHz		2.0	3.0	
5-2 Noise Figure	900 ~ 2050 MHz		8.0 dB	12.dB	AGC fullgain
5-3 Local Leakage at Input Terminal	1430~2530 MHz		-70.0	-63.0	dBm
5-4 Tuning Voltage Curve	900 MHz	1	1.6		
	950 MHz		2.2		
	1150 MHz		4.0		V
	1250 MHz		5.0		
	1450 MHz		5.7		
	1650 MHz		9.2	12	
5-5 Local Oscillator +B Shift	Tuning voltage shift with +B +/- 5%			+/- 0.8	With Tuner PLL Locked
5-6 Local Oscillator Temperature Drift	tuning voltage shift with -10°C ~ +60°C			+/- 1.3	V
5-7 IF 3dB Bandwidth	3dB down		18		MHz
5-8 AFT Output (2 bit Output)	Center Frequency Error (f0)	-2		+2	MHz



5-9 B. B. Output Characteristics

Condition	Min.	Typ.	Max.	Note

1) Video Output Level

video waveform white 100% PAL frequency deviation 16 MHz p-p without pre-emphasis

white to SYNC	0.72	0.90	1.12	Vp-p

2) Gain-Frequency Response

test modulation frequency: 60 Hz ~ 8 MHz without energy disposal modulation, reference frequency 100 KHz, IF BW: 27 MHz

Freugency Response		+/- 1	+/- 3	dB

3) Group Delay Response

test frequency: 60 Hz ~ 8 MHz without energy disposal modulation, reference frequency 100 KHz, IF BW: 27 MHz

Group Delay		+/- 10	+/- 50	nsec

4) DG/DP

10 step siaircase 16MHz p-p PAL without energy disposal modulation, positive video amplifier with de-emphasis should be applied
IF BW: 27 MHz

DG (APL 50%)		4.0	8.0	%
DP (APL 50%)		3.0	5.0	deg

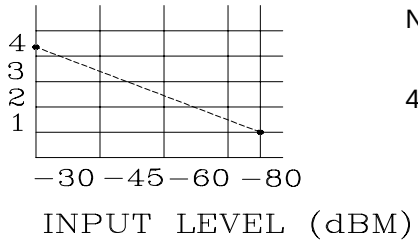
5) S/N

input C/N = 14 dB (Noise BW: 27 MHz)
white 100% video 16 MHz p-p PAL with audio subcarrier modulation 3.4 MHz p-p DEV. @6.5 MHz
positive video amplifier with de-emphasis should be applied 100 Hz ~ 5 MHz unweighted S/N, POR power on reset indicator

S/N	34.0	36.0	dB

7-1 Signal Level Out Voltage (V)

SIGNAL LEVEL OUT



Note:

47 KOhm loaded

7-2 IIC Bus

1) SDA, SCL Input Voltage — under standard test condition

Condition	Min.	Typ.	Max.	Note
High Voltage	3		5	V
Low Voltage	0		1.5	V

2) Address — C2 (on write data format)

3) SDA, SCL Input Impedance — SDA/SCL are in the high impedance and there should be no reliablity problem with 5V continually on the SDA/SCL if power supply is switched off.

4) Date Format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	BYTE 1
Programmable Divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	BYTE 2
Programmable Divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	BYTE 3
Charge Pump and Test Bits	1	CP	T1	T0	1	1	1	OS	A	BYTE 4
I/O Port Control Bits	P7	P6	P5	P4	P3	P2	P1	P0	A	BYTE 5

table 1 write data format (MSB is transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	BYTE1
Status Byte	FOR	FL	I2	I1	I0	A2	A1	A0	A	BYTE 2

table 2 read data format

A: acknowledge bit

MA1, MA0: voltage address bits

CP: charge pump current select

T1: test mode selection

T0: charge pump disable

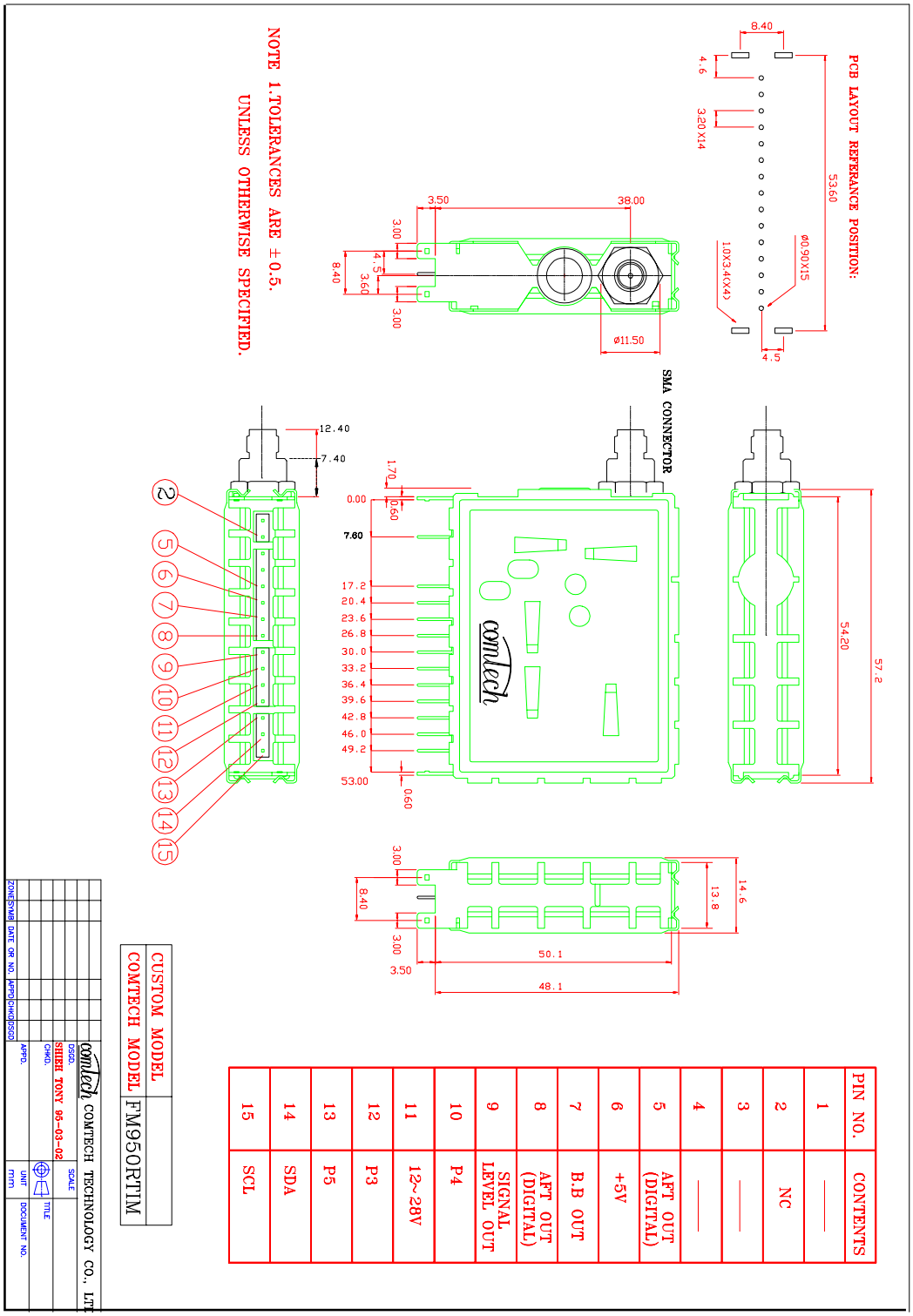
OS: varactor drive output disable switch

P7, P6, P5, P4, P3, P2, P1, P0: control output states

POR: power on reset indicator

I2, I1, I0: digital information from ports P7, P5 and P4

A2, A1, A0: 5 level ADC data from P6



PIN NO.	CONTENTS
1	——
2	NC
3	——
4	——
5	AFT OUT (DIGITAL)
6	+5V
7	B.B OUT
8	AFT OUT (DIGITAL)
9	SIGNAL LEVEL OUT
10	P4
11	12~28V
12	P3
13	P5
14	SDA
15	SCL

1. SCOPE

This specification outlines the pertinent electrical requirements of the RF output modulator which converts the FM video and FM audio signal into the RF signal for television standard transmission system.

2.GENERAL SPECIFICATIONS

2-1. Output frequency 1100~1300mhz (I^2C PLL controller from outside)

2-2. Supply voltage 12V+/-0.2V

2-3. Consumption current 140+/-20mA

2-4. Operation and storage Temperature 0-50°C

Conditions for guarantee Humidity 85% or less

3.Test Conditions

3-1. Testing ambient conditions

Defined as temperature of 25+/-2°C and humidity of 65+/-5% RH.

Note: That temperatures of 5-30°C and humidity of 45-85%RH may be regarded as standard.

3-2. Unit setting conditions

(1). Picture --10 step wave signal 1.0Vp-p(8Ohm load)

(2). Audio -- 1.0Vp-p of sine wave 1KHz

4. Electrical Performance

4-1. Video system characteristics

	parameter	Specification Min	Typ	Max	Unit	Remark
4-1-1	Input impedance		1.7		KOhm	Measure at 0.5-5MHz
4-1-2	Input signal level		1.0		Vp-p	Load of 82Ohm connected negative synchronous
4-1-3	Modulation 1100~1300 sine wave 10khz 1Vp-p	5	6	7	MHz	Superimposed sinuous wave. (3.58MHz)is 20% of the step input level measure under the apl of 10-90% differential gain of demodulator unit is to be compensated
4-1-4	Differential gain	8		8	%	
4-1-5	Differential phase	-8		8	deg	-ditto-
4-1-6	S/N	45			dB	Measure with respect to standard demodulator output.
4-1-7	Out level taper		4	6	dB	fp 1100~1300MHz

4-2. Audio system characteristics

4-2-1	Input impedance		1.4		KOhm	Measure at 0.1-10KHz
4-2-2	Modulation	35	40	45	KHz	
4-2-3	Distortion factor			3	%	Audoi input signal 1.0Vp-p 1KHz modulation 50% (sine wave) video input signal all black (sync.only) use standard demodulator of inter -carrier system. De-emphasis(50 usec) is on.
4-2-4	S/N	40			dB	The same as 4-2-3

4-3. Output system characteristics

	Parameter	Specification. Min	Typ	Max	Unit	Remark
4-3-1	Video carrier frequency	50	fp	+50	KHz	Test at 25^{O}C temperature and 65%RH of humidity Fs1 6.5 MHz Fs2 6.5 MHz *output channel
4-3-2	Video output level 1100~1300MHz	15	17	19		
4-3-3	Audio output level difference(p/s ratio) fp:1100~1300MHz	22	27	32	dB	
4-3-4	Audio carrier frequency	-8	fs_1	+8	KHz	Input signal none the measurement is taken after 30 sec. from the power-on.
4-3-5	Audio modulator fs1 fs2	60	70	80	KHz	Measurement difference video of carrier frequency output level for 0-1GHz. except to fp. fp+/-fs . against video carrier output level.
4-3-6	Out-band spurious	50	55		dB	
4-3-7	Output impedance		75		Ohm	Unbalanced.

5-1. PLL section characteristics

No	Item	Specification	notes
5-2.	IIC Bus (1) Sda.scl Input voltage	Under standard test condition	V
	(2) Address	C2 (on write date format)	
	(3) Sda scl Input impedance	SDA/SCLl are in the high impedance and there should be no reliablity problem with 5V continually on the SDA/SCL,if power supply is switched off.	

Condition	Min	Typ	Max
High voltage	3		5
Low voltage	0		1.5

(4) Data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	Byte1
Programmable Divider	0	14 2	13 2	12 2	11 2	10 2	9 2	8 2	A	Byte2
Programmable Divider	7 2	6 2	5 2	4 2	3 2	2 2	1 2	0 2	A	Byte3
Charge pump and test bits	1	(0) cp	t1	t0	1	1	1	(0) os	A	Byte4
I/O port control bits	p7	p6	p5	p4	p3	p2	p1	p0	A	Byte5

Table 1 write data format (MSB is transmitted first)

Address	1	1	0	0	0	MA1	MA2	1	A	Byte1
Status byte	POR	fl	I2	I1	I0	A2	A1	A0	A	Byte2

Table 2 read date format

A: Acknowledge bit.

MA1,MA0: Voltage address bits.

CP: Charge pump current select.

T1: Test mode selection,T0:Charge pump disable

OS: Varactor drive output disable switch.

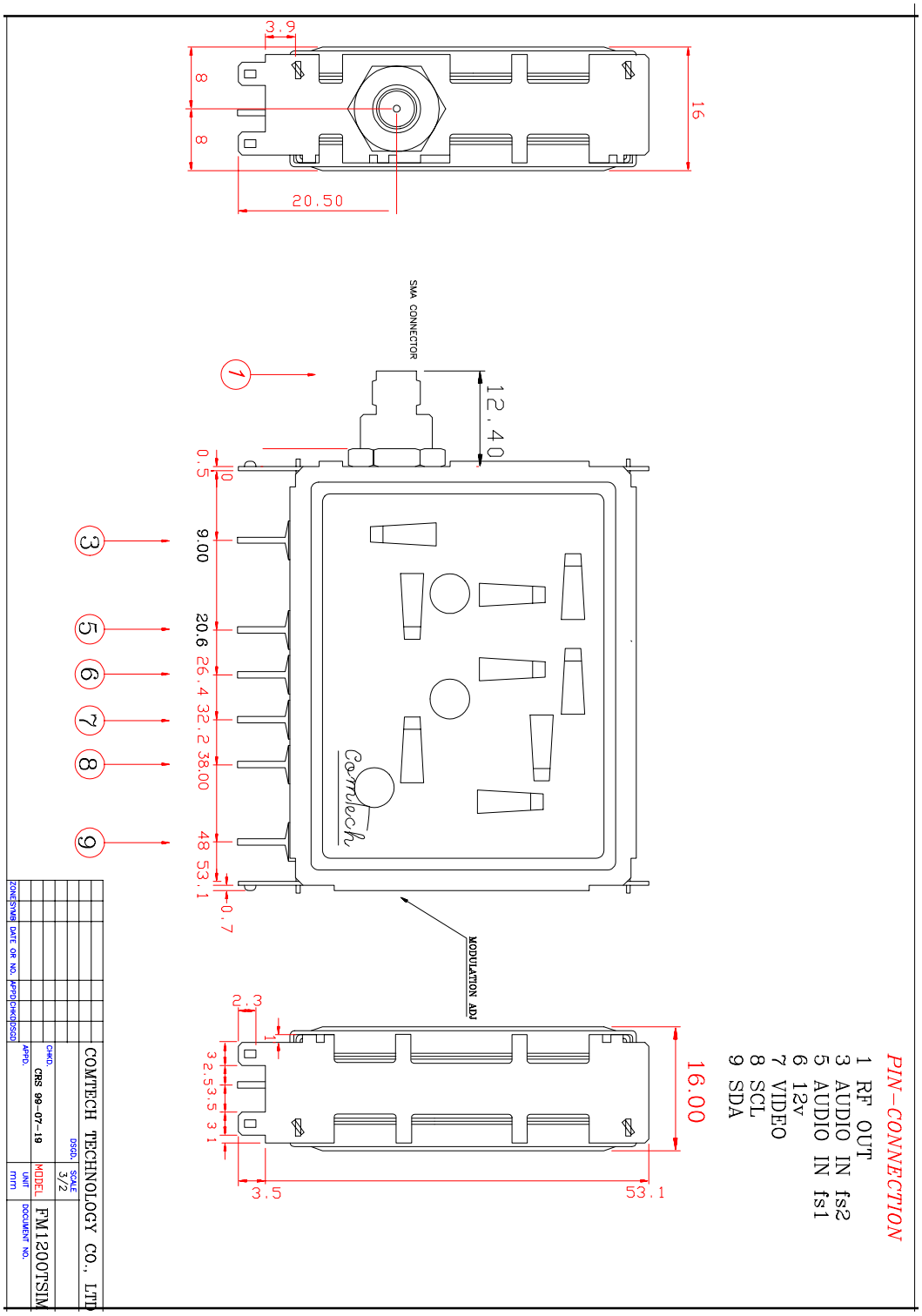
P7,P6,P5,P4,P3,P2,P1,P0: Control output states.

POR: Power on reset indicator

PL: Phase lock detect flag

I2,I1,I0: Digital information from ports P7,P5,and P4.

A2,A1,A0: 5 level adc data from P6


PIN-CONNECTION
1 RF OUT
3 AUDIO IN fs2
5 AUDIO IN fs1
6 12v
7 VIDEO
8 SCL
9 SDA
SMA CONNECTOR
MODULATION ADJ
Comtech
20.50
16
12.40
9.00
20.6
26.4
32.2
38.00
48
53.1
16.00
COMTECH TECHNOLOGY CO., LTD
FM1200TSIM

1. General Specification

1-1 Input Frequency Range	1100 MHz - 1300 MHz	
1-3 One Input Connector	F Fe-Male	
1-4 Nominal Input Impedance	75 Ohm	**Note:**
1-5 Tuning Circuit	Built-in PLL	SP5055
1-6 IF Frequency	479.50 MHz Center	(PLESSEY)
1-7 IF Bandwidth	18 MHz Nominal (Selectable)	**Note:**
1-8 Demodulation	Phase Locked Loop	TA8804F
1-9 Video Output Polarity	Positive Going	
1-10 Operating Voltage	+12V (+/-5%)	
	+5V (+/-5%)	
1-11 Operating Temperature	-10°C ~ +60°C	
1-12 Operating Humidity	less than 80% R. H. (at 40°C)	
1-13 Storage Temperature	-20°C ~ +70°C	
1-14 Storage Humidity	less than 95% R. H. (at 40°C)	

2. Standard Test Condition

test for electrical specification shall be preformed at following condition unless otherwise specified.

2-1 Ambient Condition

Temperature 25°C +/- 2°C
Humidity 65% +/- 5% R. H.
if no doubt on test results
Temperature +5°C ~ +30°C
Humidity 45% ~ 80% R. H.
could be applied

2-2 Measurement to Start

30 minutes after DC power supplied

2-3 Power Supply

Terminal	Supply Voltage
+5V	+5V (+/-) 0.1V
TU	+12V (+/-) 0.1V
SDA	specified tuning
SCL	pulse

3. Current Consumption

Terminal	Min.	Typ.	Max.	Unit
+5V	190	240	290	mA
TU	0.5	1.0	3.0	mA

4. Absolute Maximum Voltage

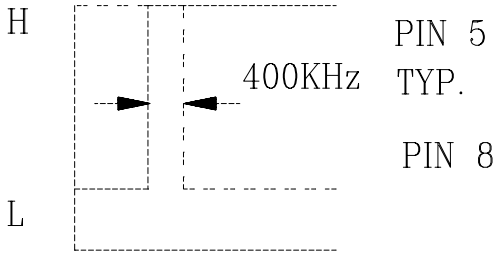
Terminal	Max. Supply Voltage
LNB Power	DC +25V
+5V	DC +5.25V
TU	DC +15V
SDA,SCL	OV TO The Same Voltage AS +5V Terminal

Terminal	Max. Take Off Current
LNB Power	500mA
B. B. Output	0.5 mA

5. Electrical Specification

under standard test condition
Test Channel: DBS 20 CH
Input Level: -45 dBm
unless otherwise specified

	Condition	Min.	Typ.	Max.	Note
5-1 Input VSWR	1100 ~ 1300 MHz		2.0	3.0	
5-2 Noise Figure	1100 ~ 1300 MHz		8.0 dB	12.dB	AGC fullgain
5-3 Local Leakage at Input Terminal	1579.5~1779.5 MHz		-70.0	-63.0	dBm
5-4 Tuning Voltage Curve	1100 ~ 1300 MHz	2.5V		7.0V	with tuing
					PLL locked
5-5 Local Oscillator +B Shift	tuning voltage shift			+/- 0.8	
	with +B +/- 5%				
5-6 Local Oscillator Temperature Drift	tuning voltage shift			+/- 1.3	
	with -10°C ~ +60°C				
5-7 IF 3dB Bandwidth	3dB down		18		MHz
5-8 AFT Output (2 bit Output)	Center Frequency	-2		+2	MHz
	Error (f0)				



5-9 B. B. Output Characteristics

Condition	Min.	Typ.	Max.	Note

1) Video Output Level

video waveform white 100% PAL frequency deviation 16 MHz p-p without pre-emphasis

white to SYNC	0.72	0.90	1.12	Vp-p

2) Gain-Frequency Response

test modulation frequency: 60 Hz ~ 8 MHz without energy disposal modulation, reference frequency 100 KHz, IF BW: 27 MHz

Freugency Response		+/- 1	+/- 3	dB

3) Group Delay Response

test frequency: 60 Hz ~ 8 MHz without energy disposal modulation, reference frequency 100 KHz, IF BW: 27 MHz

Group Delay		+/- 10	+/- 50	nsec

4) DG/DP

10 step siaircase 16MHz p-p PAL without energy disposal modulation, positive video amplifier with de-emphasis should be applied
IF BW: 27 MHz

DG (APL 50%)		4.0	8.0	%
DP (APL 50%)		3.0	5.0	deg

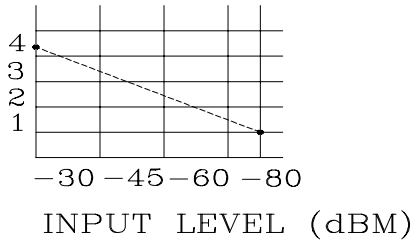
5) S/N

input C/N = 14 dB (Noise BW: 27 MHz)
white 100% video 16 MHz p-p PAL with audio subcarrier modulation 3.4 MHz p-p DEV. @6.5 MHz
positive video amplifier with de-emphasis should be applied 100 Hz ~ 5 MHz unweighted S/N, for power on reset indicator

S/N	34.0	36.0	dB

7-1 Signal Level Out Voltage (V)

SIGNAL LEVEL OUT



7-2 IIC Bus

1) SDA, SCL Input Voltage — under standard test condition

Condition	Min.	Typ.	Max.	Note
High Voltage	3		5	V
Low Voltage	0		1.5	V

2) Address — C2 (on write data format)

3) SDA, SCL Input Impedance — SDA/SCL are in the high impedance and there should be no reliablity problem with 5V continually on the SDA/SCL if power supply is switched off.

4) Date Format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	BYTE 1
Programmable Divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	BYTE 2
Programmable Divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	BYTE 3
Charge Pump and Test Bits	1	CP	T1	T0	1	1	1	OS	A	BYTE 4
I/O Port Control Bits	P7	P6	P5	P4	P3	P2	P1	P0	A	BYTE 5

table 1 write data format (MSB is transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	BYTE1
Status Byte	FOR	FL	I2	I1	I0	A2	A1	A0	A	BYTE 2

table 2 read data format

A: acknowledge bit

MA1, MA0: voltage address bits

CP: charge pomp current select

T1: test mode selection

T0: charge pump disable

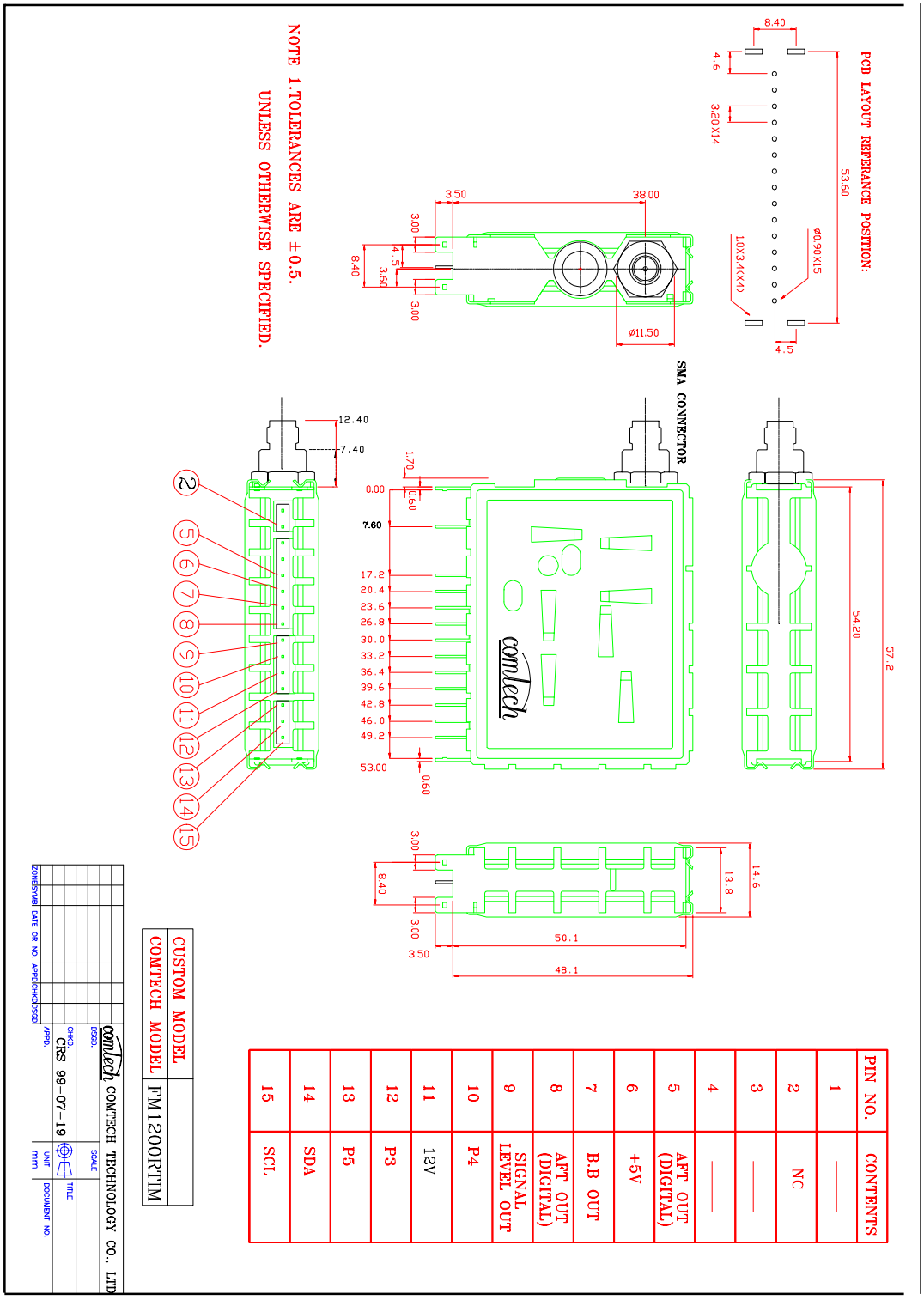
OS: varactor drive output disable switch

P7, P6, P5, P4, P3, P2, P1, P0: control output states

POR: power on reset indicator

I2, I1, I0: digital information from ports P7, P5 and P4

A2, A1, A0: 5 level ADC data from P6



PIN NO.	CONTENTS
1	———
2	NC
3	———
4	———
5	AFT OUT (DIGITAL)
6	+5V
7	B.B OUT
8	AFT OUT (DIGITAL)
9	SIGNAL LEVEL OUT
10	P4
11	12V
12	P3
13	P5
14	SDA
15	SCL

CUSTOM MODEL	
COMTECH MODEL	FM1200RTIM

comtech COMTECH TECHNOLOGY CO., LTD.

ZONE	SYMB	DATE OR NO.	APPD	CHK	DSGD

DSGD.
CHKD.
APPD.
SCALE
CRS 99-07-19
TITLE
UNIT mm
DOCUMENT NO.

1. SCOPE

This specification outlines the pertinent electrical requirements of the RF output modulator which converts the FM video and FM audio signal into the RF signal for television standard transmission system.

2.CENERAL SPECIFICATIONS

2-1. Output frequency 2400~2483 MHz (I^2C PLL controller from outside)
2-2.
2-3. Supply voltage 12V+/-0.2V
2-4. Consumption current 140+/-20 mA
2-5. Operation and storage temperature 0-50°C
Conditions for guarantee humidity 85% or less

3.TEST CONDITIONS

3-1. Testing ambient conditions defined as temperature of 25+/-2°C and humidity of 65+/-5% RH
Note: that temperatures of 5~30°C and humidity of 45-85%rh may be regarded as standard.
3-2. Unit setting conditions
1) Picture --10 step wave signal 1.0 Vp-p(82 ohm load)
2) Audio -- 1.0Vp-p of sine wave 1KHz

4. ELECTRICAL PERFORMANCE

4-1. Video system characteristics

	Parameter	Specification min	typ	max	unit	Remark
4-1-1	Input impedance			1.3	K	measure at 0.5 ~ 5 MHz
4-1-2	Input signal level			1	Vp-p	load of 92 ohm connected negative synchronous
4-1-3	Modulation fp 2480 MHz (sine wave 300KHz 1Vp-p)	2	3	4	MHz	Superimposed sinuous wave (2.58 MHz) is 20% of the step input level. Measure with under the APL of 10~90% differential gain of demodulator unit is to be compensated..
4-1-4	Differential gain	8		8	%	
4-1-5	Differential phase	-8		8	deg	-ditto-
4-1-6	S/N	45			dB	Measure with respeot to standard demodulator output.
4-1-7	Out level taper		4	6	dB	Fp 2400~2483mhz.

4-2. Audio system characteristics

4-2-1	Input impedance		1.4		Kohm	Measure at 0.1-10khz
4-2-2	Modulation	35	40	45	khz	
4-2-3	Distortion factor			3	%	Audoi input signal 1.0Vp-p 1khz modulation 50% (sine wave).Video input signal all black (sync.only) use standard demodulator of inter -carrier system.
						De-emphasis(50 usec) is on.
4-2-4	S/n	40			dB	The same as 4-2-3

4-3. Output system characteristics

	Parameter	Specification. min	typ	max	unit	Remark
4-3-1	Video carrier frequency	-50	fp	+50	KHz	Test at 25^{O}C temperature and
4-3-2	Video output level	13	14	16	dBm	65% RH of humidity
4-3-3	Audio output level difference(P/S ratio)	22	27	32	dB	Fp 2400~2483 Mhz Fs1 6.5 mhZ Fs2 6.5 mhz *output channel
4-3-4	Audio carrier frequency	-8	fs	+8	KHz	Input signal none the measurement is taken after 30 sec. from the power-on.
4-3-5	Audio modulator fs1 fs2	35 35	50 50	65 65	KHz	Measurement difference video of carrier frequency output level for
4-3-6	Out-band spurious	50	55		dB	2400~2483 Mhz except to fp.
4-3-7	In-band spurious within bandwidth	60			dB	fp+/-fs against video carrier output level.
4-3-8	Output impedance		75		ohm	Unbalanced.

5-1. PLL section characteristics

No	Item	Specification	notes
5-2.	IIC Bus (1) SDA SCL input voltage	Under standard test condition Condition / Min / Typ / Max High voltage / 3 / / 5 Low voltage / 0 / / 1.5	V
	(2) Address	C2 (on write date format)	
	(3) SDA SCL input impedance	SDA/SCL are in the high impedance and there should be no reliablity problem with 5V continually on the SDA/SCL, if power supply is switched off.	

(4) Data format MSB LSB

Address	1	1	0	0	0	MA1	MA0	0	A	Byte1
Programmable Divider	0	14 2	13 2	12 2	11 2	10 2	9 2	8 2	A	Byte2
Programmable Divider	7 2	6 2	5 2	4 2	3 2	2 2	1 2	0 2	A	Byte3
Charge pump and test bits	1	(0) CP	T1	T0	1	1	1	(0) os	A	Byte4
I/O port control bits	P7	P6	P5	P4	P3	P2	P1	P0	A	Byte5

Table 1 write data format (MSB is transmitted first)

Address	1	1	0	0	0	Ma1	Ma2	1	A	Byte1
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	A	Byte2

Table 2 read date format

A: acknowledge bit.

Ma1,Ma0: voltage address bits.

CP: charge pump current select.

T1: test mode selection,T0:charge pump disable

OS: varactor drive output disable switch.

P7,P6,P5,P4,P3,P2,P1,P0:control output states

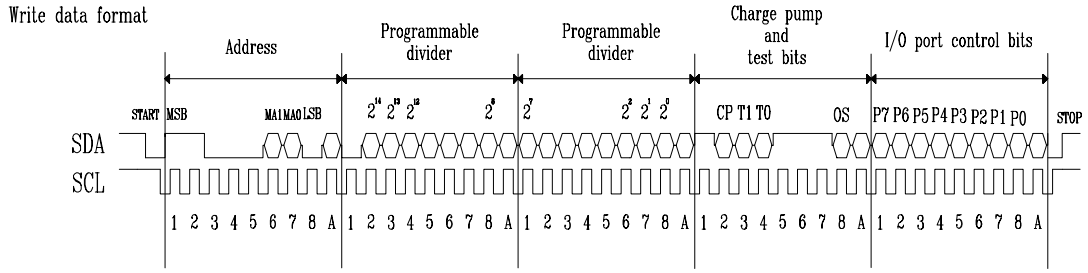
POR: power on reset indicator

PL: phase lock detect flag

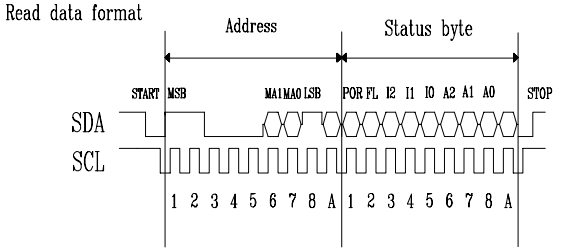
I2,I1,I0: digital information from ports P7,P5,and P4.

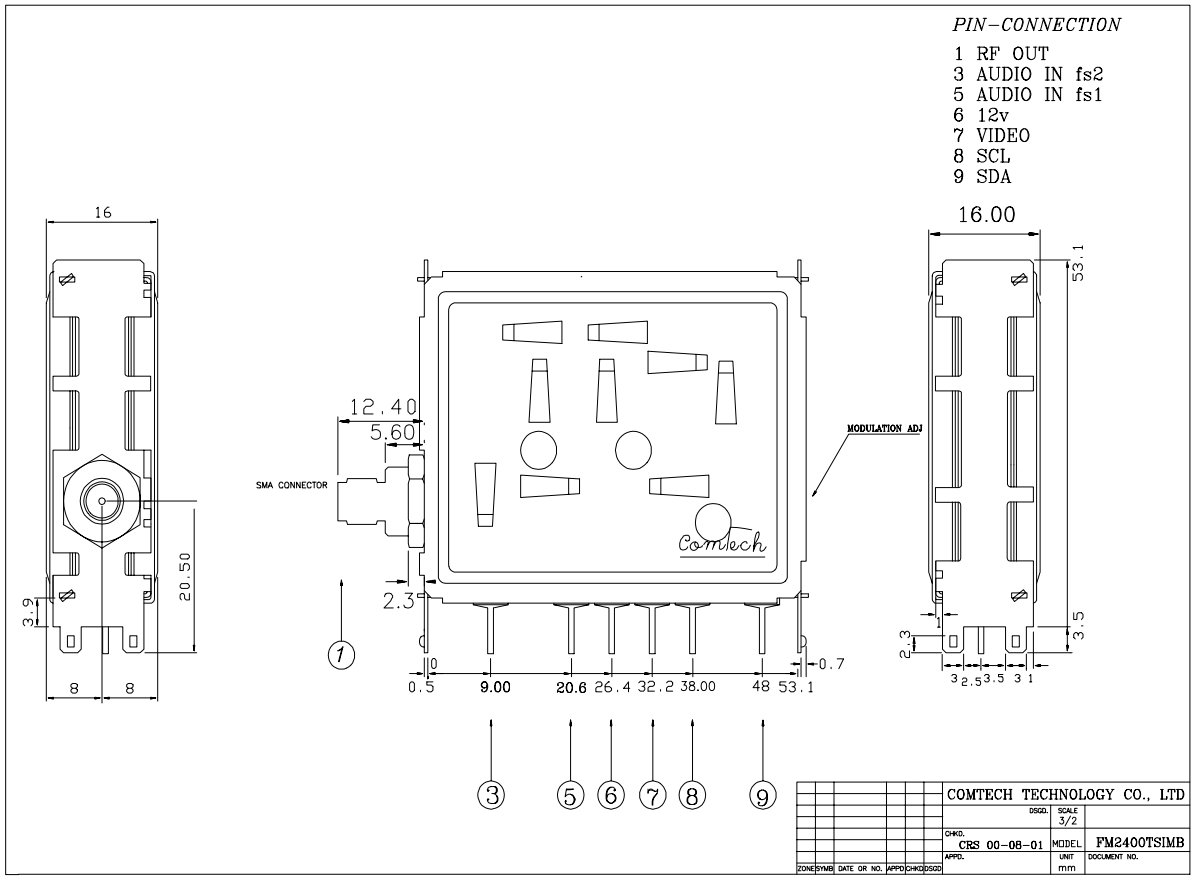
A2,A1,A0: 5 level ADC data from P6

Write data format



Read data format





1. General Specification

1-1 Input Frequency Range	2.4 GHz - 2.4835 GHz	
1-3 One Input Connector	SMA Connector	
1-4 Nominal Input Impedance	75 Ohm	**Note:**
1-5 Tuning Circuit	Built-in PLL	U6239B (TEMIC)
1-6 IF Frequency	479.50 MHz Center	
1-7 IF Bandwidth	18 MHz Nominal (Selectable)	**Note:**
1-8 Demodulation	Phase Locked Loop	TA8804F
1-9 Video Output Polarity	Negative	
1-10 Operating Voltage	+28V (+/-5%)	
	+5V (+/-5%)	
1-11 Operating Temperature	-10°C ~ +60°C	
1-12 Operating Humidity	less than 80% R. H. (at 40°C)	
1-13 Storage Temperature	-20°C ~ +70°C	
1-14 Storage Humidity	less than 95% R. H. (at 40°C)	

2. Standard Test Condition

test for electrical specification shall be preformed at following condition unless otherwise specified.

2-1 Ambient Condition

Temperature 25°C +/- 2°C
Humidity 65% +/- 5% R. H.
if no doubt on test results
Temperature 5°C +/- 30°C
Humidity 45% ~ 80% R. H.
could be applied

2-2 Measurement to Start

30 minutes after DC power supplied

2-3 Power Supply

Terminal	Supply Voltage
+5V	+5V (+/-) 0.1V
+12V	+12V (+/-) 0.1V
SDA	specified tuning
SCL	pulse

3. Current Consumption

Terminal	Min.	Typ.	Max.	Unit
+5V	190	240	290	mA
+12V	0.5	1.0	3.0	mA

4. Absolute Maximum Voltage

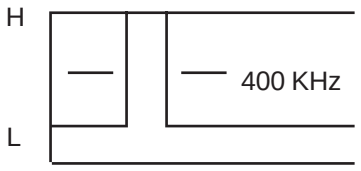
Terminal	Max. Supply Voltage
+5V	DC +5.25V
+12V	DC +30V

Terminal	Max. Take Off Current
B. B. Output	0.5 mA

5. Electrical Specification

under standard test condition
Test Channel: DBS 20 CH
Input Level: -45 dBm
unless otherwise specified

	Condition	Min.	Typ.	Max.	Note
5-1 Input VSWR	2.4 ~ 2.4835 GHz		2.0	3.0	
5-2 Noise Figure	2.4 ~ 2.4835 GHz		3.5 dB		AGC fullgain
5-3 Local Leakage at Input Terminal	1.920 ~ 2.4835 GHz			-63.0	dBm
5-4 Tuning Voltage Curve	2.4 ~ 2.4835 GHz	5V		10V	with tuing PLL locked
5-5 Local Oscillator +B Shift	tuning voltage shift with +B +/- 5%			+/- 0.8	
5-6 Local Oscillator Temperature Drift	tuning voltage shift with -10°C ~ +60°C			+/- 1.3	
5-7 IF 3dB Bandwidth	3dB down		18		MHz
5-8 AFT Output (2 bit Output)	Center Frequency Error (f0)	-2		+2	MHz

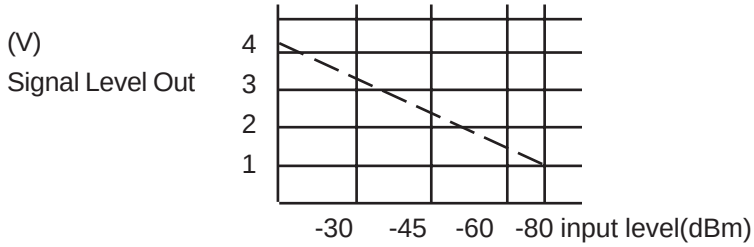


Pin 5
Typ.
Pin 8

5-8 B. B. Output Characteristics

	Condition	Min.	Typ.	Max.	Note
1) Video Output Level	video waveform white 100% PAL frequency deviation 8 MHz p-p without pre-emphasis				
	white to SYNC	0.72	0.90	1.12	Vp-p
2) Gain-Frequency Response	test modulation frequency: 60 Hz ~ 8 MHz without energy disposal modulation, reference frequency 100 KHz, IF BW: 18 MHz				
	Freugency Response		+/- 1	+/- 3	dB
3) Group Delay Response	test frequency: 60 Hz ~ 8 MHz without energy disposal modulation, reference frequency 100 KHz, IF BW: 18 MHz				
	Group Delay		+/- 10	+/- 50	nsec
4) DG/DP	10 step siaircase 8 MHz p-p PAL without energy disposal modulation, positive video amplifier with de-emphasis should be applied IF BW: 18 MHz				
	DG (APL 50%)		4.0	8.0	%
	DP (APL 50%)		3.0	5.0	deg
5) S/N	input C/N = 14 dB (Noise BW: 16 MHz) white 100% video 8 MHz p-p PAL with audio subcarrier modulation 3.4 MHz p-p DEV. @6.5 MHz positive video amplifier with de-emphasis should be applied 100 Hz ~ 5 MHz unweighted S/N, POR: power on reset indicator				
	S/N	34.0	36.0		dB

7-1 Signal Level Out Voltage



7-2 IIC Bus

1) SDA, SCL Input Voltage — under standard test condition

Condition	Min.	Typ.	Max.	Note
High Voltage	3		5	V
Low Voltage	0		1.5	V

2) Address — C2 (on write data format)

3) SDA, SCL Input Impedance — SDA/SCL are in the high impedance and there should be no reliablity problem with 5V continually on the SDA/SCL if power supply is switched off.

4) Date Format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	BYTE 1
Programmable Divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	BYTE 2
Programmable Divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	BYTE 3
Charge Pump and Test Bits	1	CP	T1	T0	1	1	1	OS	A	BYTE 4
I/O Port Control Bits	P7	P6	P5	P4	P3	P2	P1	P0	A	BYTE 5

table 1 write data format (MSB is transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	BYTE1
Status Byte	FOR	FL	I2	I1	I0	A2	A1	A0	A	BYTE 2

table 2 read data format

A: acknowledge bit

MA1, MA0: voltage address bits

CP: charge pomp current select

T1: test mode selection

T0: charge pump disable

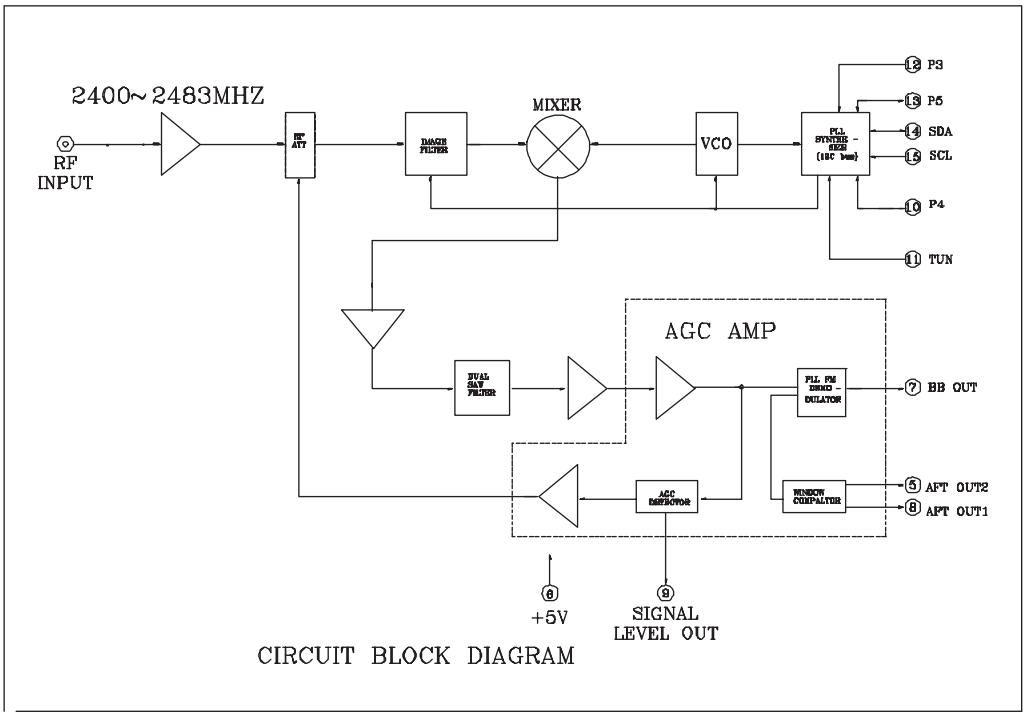
OS: varactor drive output disable switch

P7, P6, P5, P4, P3, P2, P1, P0: control output states

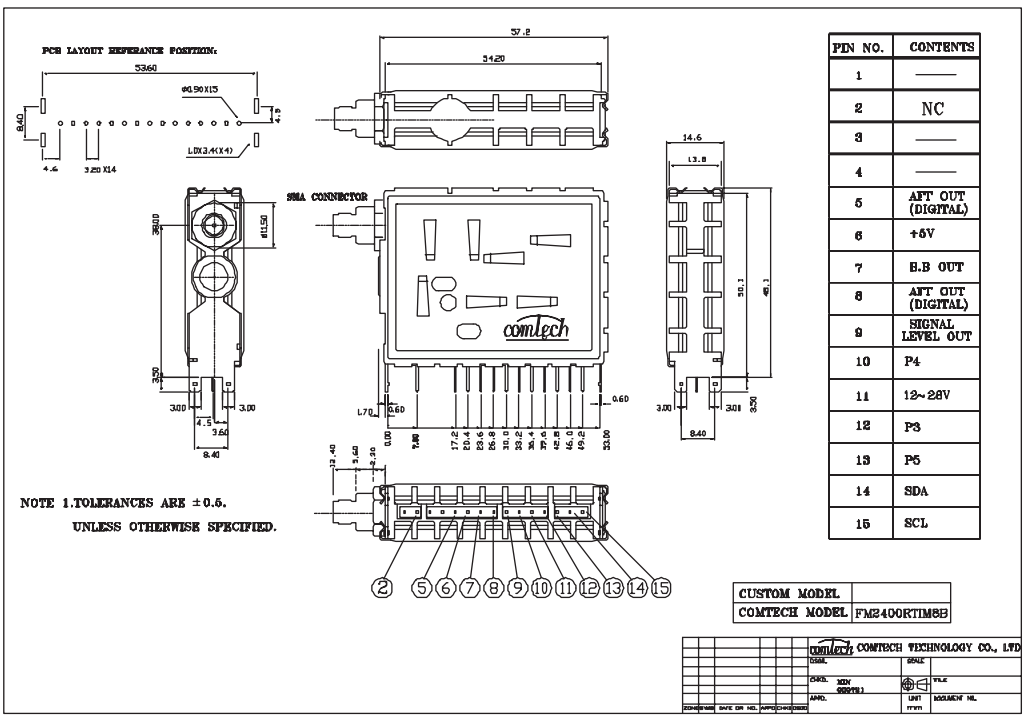
POR: power on reset indicator

I2, I1, I0: digital information from ports P7, P5 and P4

A2, A1, A0: 5 level ADC data from P6



CIRCUIT BLOCK DIAGRAM



PIN NO.	CONTENTS
1	——
2	NC
3	——
4	——
5	AFT OUT (DIGITAL)
6	+5V
7	B.B OUT
8	AFT OUT (DIGITAL)
9	SIGNAL LEVEL OUT
10	P4
11	12~28V
12	P3
13	P5
14	SDA
15	SCL

SP5055

2.6GHz Bidirectional I²C BUS Controlled Synthesiser

Supersedes version in April 1994 Consumer IC Handbook, HB3120 - 2.0 DS2384 - 4.4 May 1996

The SP5055 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device contains 4 addressable current limited outputs and 4 addressable Bi-Directional open collector ports one of which is a 3 bit ADC. The information on these ports can be read via the I²C BUS. The device has one fixed I²C BUS address and 3 programmable addresses, programmed by applying a specific input voltage to one of the current limited outputs. This enables 2 or more synthesisers to be used in a system.

FEATURES

- Complete 2.6GHz Single Chip System
- Programmable via I²C BUS
- Low power consumption (5V 65mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 6 Controllable Outputs, 4 Bi-Directional
- 5 Level ADC
- Variable I²C BUS Address For Multi Tuner Applications
- Full ESD Protection*

* Normal ESD handling procedures should be observed.

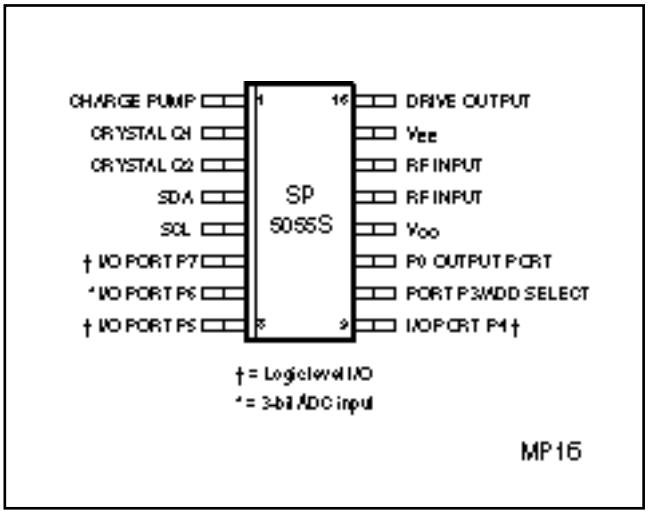


Fig. 1 Pin connections – top view

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

ORDERING INFORMATION

SP5055S MP - (16 lead Miniature Plastic package)

ELECTRICAL CHARACTERISTICS

T_{amb} = -20°C to +80°C, V_{CC} = +4.7V to 5.3V.
These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated. Reference frequency = 4MHz unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	12		65	80	mA	V_{CC} = 5V
Prescaler input voltage	13, 14	50		300	mV_{RMS}	500MHz to 2.6GHz Sinewave
Prescaler input voltage	13, 14	100		300	mV_{RMS}	120MHz, see Fig. 5
Prescaler input impedance	13, 14		50		Ω	
Prescaler input capacitance			2		pF	
SDA, SCL						
Input high voltage	4, 5	3		5.5	V	
Input low voltage	4, 5	0		1.5	V	
Input high current	4, 5			10	µA	Input voltage = V_{CC}
Input low current	4, 5			-10	µA	Input voltage = 0V
Leakage current	4, 5			10	µA	When V_{CC} = 0V
SDA						
Output voltage	4			0.4	V	I_{sink} = 3mA
Charge pump current low	1		±50		µA	Byte 4, bit 2 = 0, pin 1 = 2V
Charge pump current high	1		±170		µA	Byte 4, bit 2 = 1, pin 1 = 2V
Charge pump output leakage current	1			±5	nA	Byte 4, bit 4 = 1, pin 1 = 2V
Charge pump drive output current	16	500			µA	$V_{pin\ 16}$ = 0·7V
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	Ω	
Crystal oscillator drive level	2		80		mVp-p	
Crystal oscillator negative resistance	2	750			Ω	
Output Ports						
P0, P3 sink current	10, 11	0.7	1	1.5	mA	V_{OUT} = 12V
P0, P3 leakage current	10, 11			10	µA	V_{OUT} = 13·2V
P4-P7 sink current	9-6	10			mA	V_{OUT} = 0.7V
P4-P7 leakage current	9-6			10	µA	V_{OUT} = 13·2V
Input Ports						
P3 input current high	10			+10	µA	$V_{pin\ 10}$ = 13.2V
P3 input current low	10			-10	µA	$V_{pin\ 10}$ = 0V
P4,P5,P7 input voltage low	9,8,6			0.8	V	
P4,P5,P7 input voltage high	9,8,6	2.7			V	
P6 input current high	7			+10	µA	See Table 3 for ADC Levels
P6 input current low	7			-10	µA	

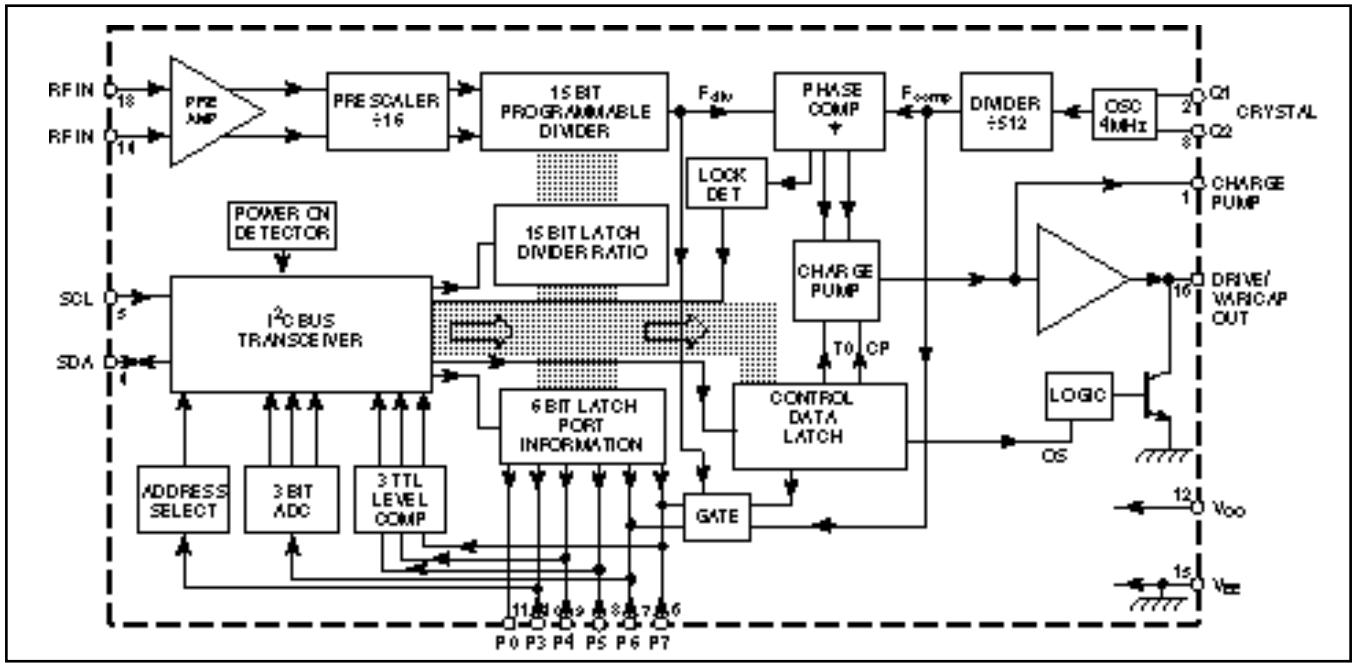


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

The SP5055 is programmed from an I^2C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I^2C BUS format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I^2C Bus system. Table 4 shows how the address is selected by applying a voltage to P3. The last bit of the address byte (R/W) sets the device into read mode if it is high and write mode if it is low. When the SP5055 receives a correct address byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data bytes are programmed. When the SP5055 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2 + 3 select the synthesised frequency while bytes 4 + 5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first Bit of the next Byte determines whether that byte is interpreted as byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data bytes can be entered without the need to re-address the device until an I^2C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (i.e., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-16 prescaler and amplifier to give excellent sensitivity at the local oscillator input; see Fig 5. The input impedance is shown in Fig 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 16 times the comparison frequency F_{comp}.

When frequency data is entered, the phase comparator, via the charge pump and varactor drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-board 4MHz crystal controlled oscillator.

Note that the comparison frequency is 7·8125kHz when a 4MHz reference is used.

Bit 2 of byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for ±170µA and a logic 0 for ±50µA, allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{comp} to P6 and F_{div} to P7.

Byte 5 programs the output ports P0 to P7; on a logic 0 for a high impedance output, logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power-on reset indicator and is set to a logic 1 if the power supply to the device has dropped below 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2,I1,I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with TTL type voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5 level ADC.

The 5 level ADC can be used to feed AFC information to the microprocessor from the IF section of the receiver, as illustrated in the typical application circuit.

APPLICATION

A typical Application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**Byte 2**
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**Byte 3**
Charge pump and test bits	1	CP	T1	T0	1	1	1	OS	A	**Byte 4**
I/O port control bits	P7	P6	P5	P4	P3	X	X	P0	A	**Byte 5**

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	A	**Byte 2**

Table 2 Read data format (MSB is transmitted first)

A	:	Acknowledge bit
MA1, MA0	:	Variable address bits (see Table 4)
CP	:	Charge Pump current select
T1	:	Test mode selection
T0	:	Charge pump disable
OS	:	Varactor drive Output disable Switch
P7, P6, P5, P4, P3, P0	:	Control output states
POR	:	Power On Reset indicator
FL	:	Phase lock detect flag
I2, I1, I0	:	Digital information from Ports P7, P5 and P4, respectively
A2, A1, A0	:	5 Level ADC data from P6 (see Table 3)
X	:	Don't care

A2	A1	A0	Voltage input to P6
1	0	0	$0.6V_{CC}$ to 13.2V
0	1	1	$0{\cdot}45V_{CC}$ to $0{\cdot}6V_{CC}$
0	1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}45V_{CC}$
0	0	1	$0{\cdot}15V_{CC}$ to $0{\cdot}3V_{CC}$
0	0	0	0 to $0.15V_{CC}$

Table 3 ADC levels

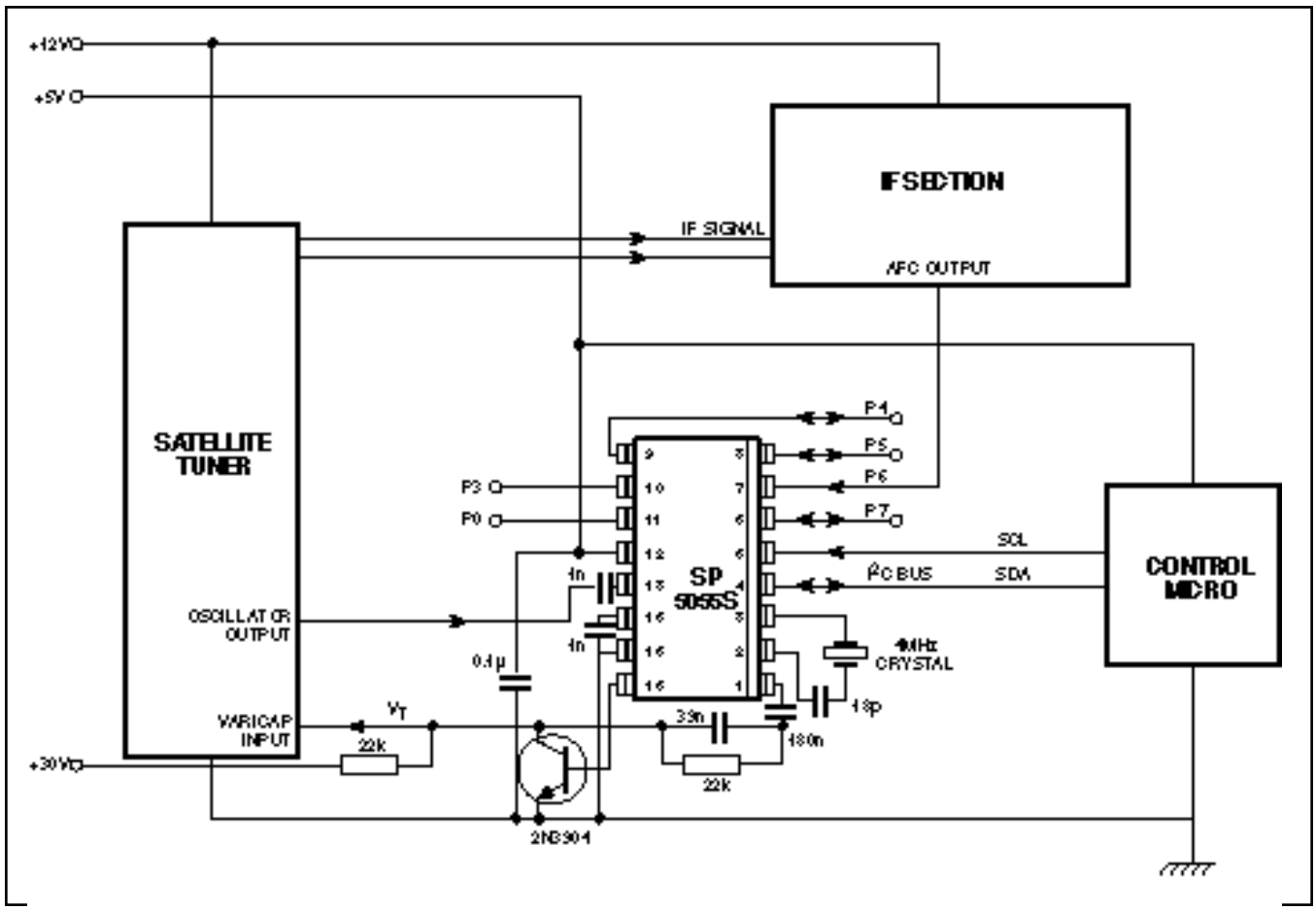
MA1	MA0	Voltage input to P3
0	0	0V to $0{\cdot}2V_{CC}$
0	1	Always valid
1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}7V_{CC}$
1	1	$0{\cdot}8V_{CC}$ -13.2V

Table 4 Address selection

Fig. 3 Data formats

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.



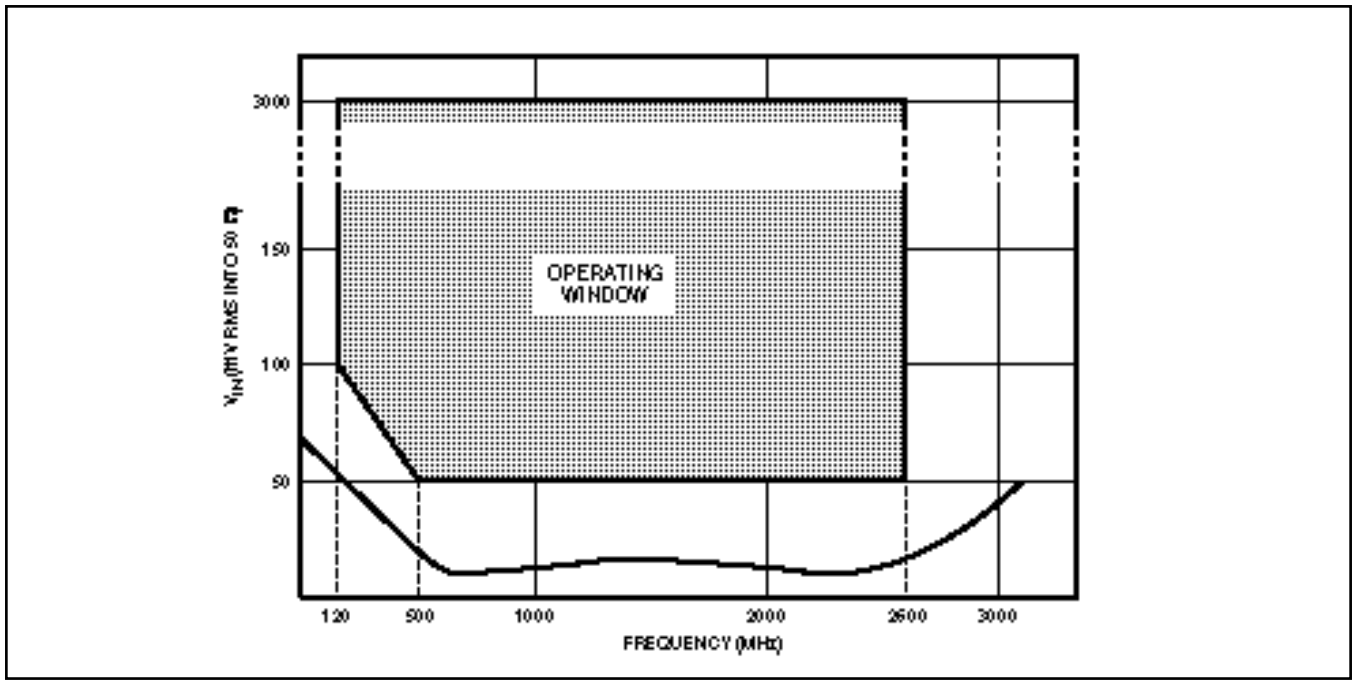


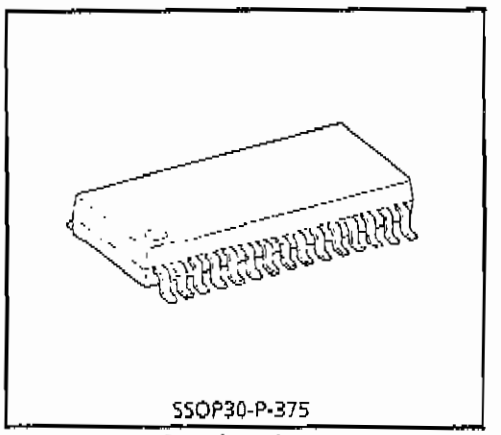
Fig. 5 Typical input sensitivity

TA8804F

SILICON MONOLITHIC

FM DEMODULATION IC FOR BROADCASTING SATELLITE RECEIVER

The TA8804F combines the necessary function on a single monolithic integrated circuit to modulate FM signal of the 2nd IF of DBS.



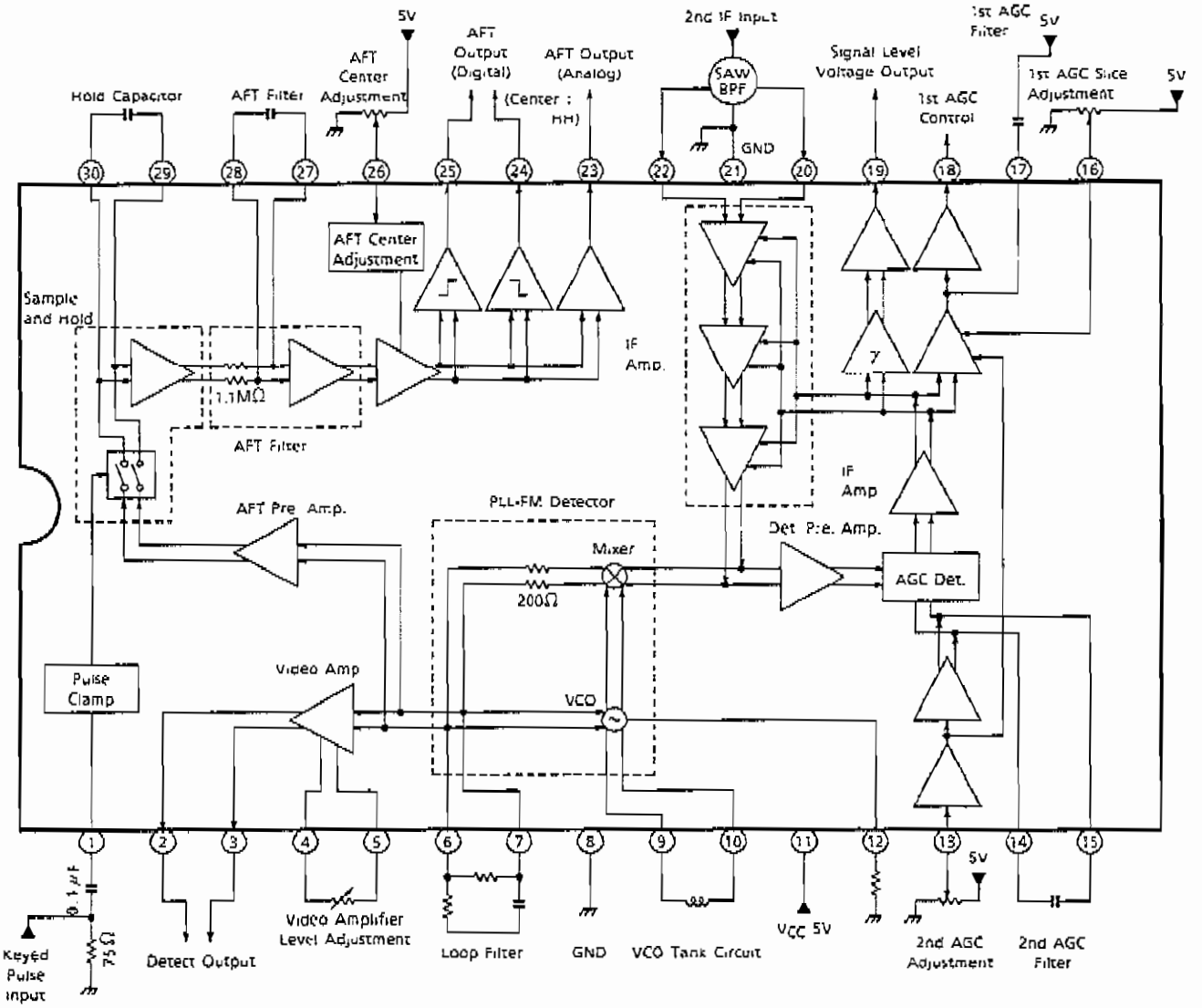
SSOP30-P-375

Weight : 0.63g (Typ.)

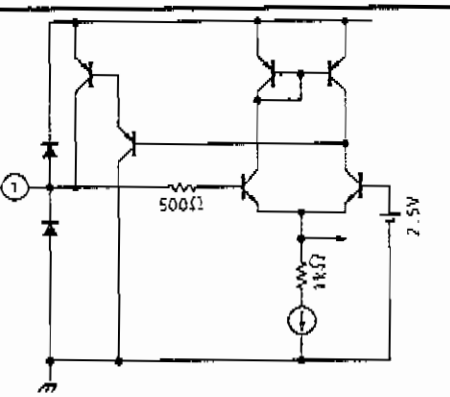
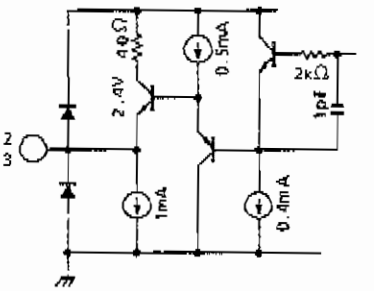
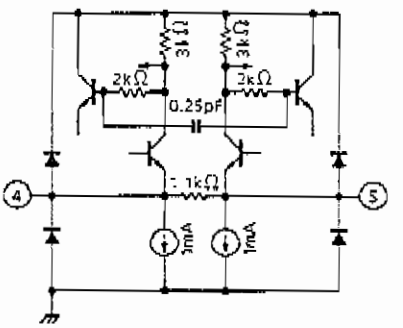
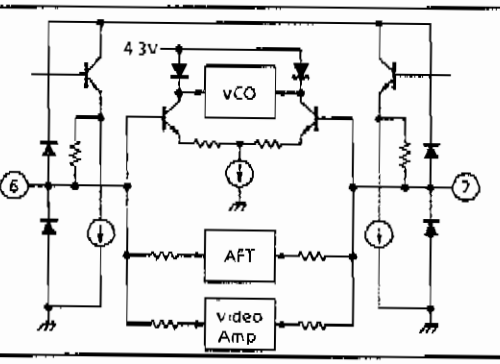
FEATURES

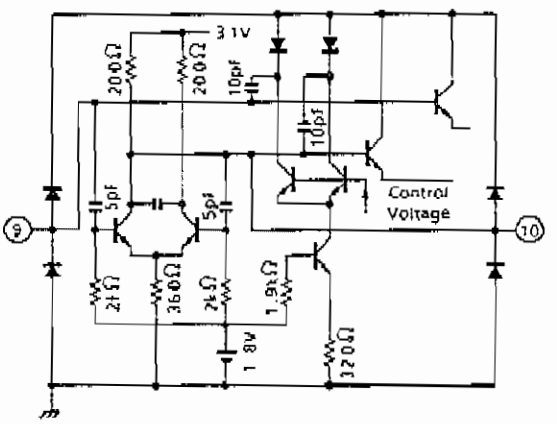
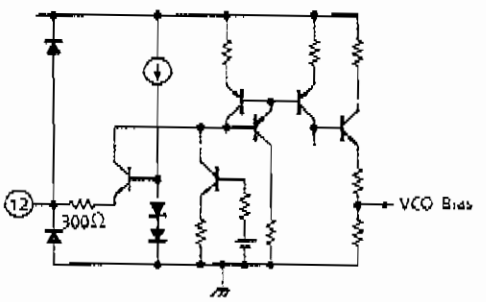
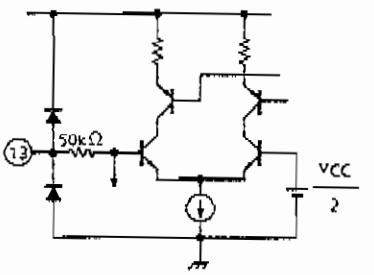
- 5V Power Supply
- 2nd IF AGC Amp
- dB-Linear Signal Level Amp
- PLL FM Detector
- Keyed AFT

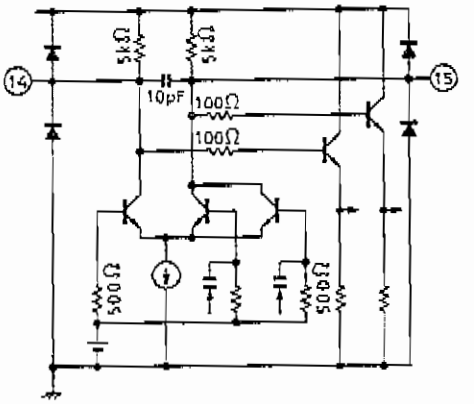
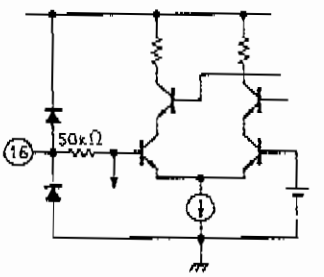
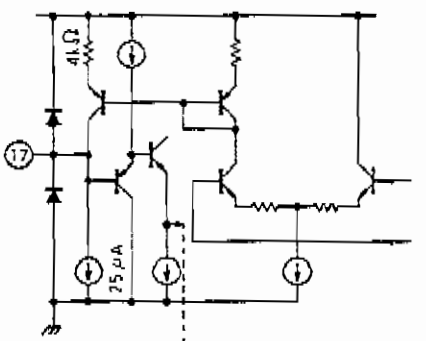
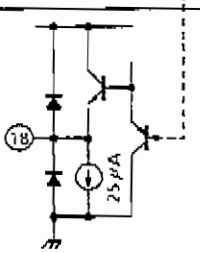
BLOCK DIAGRAM

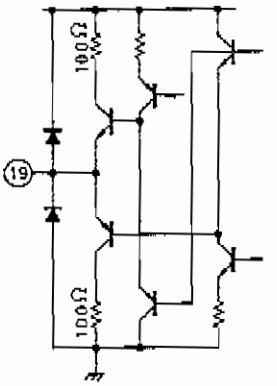
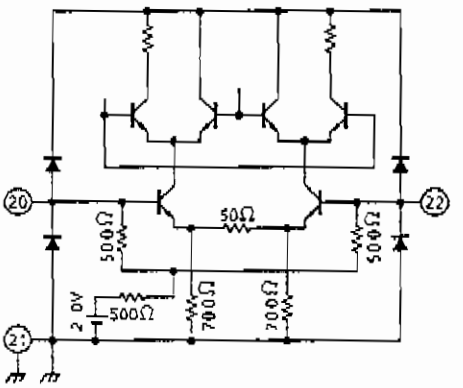
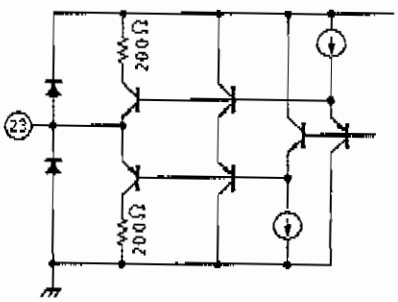


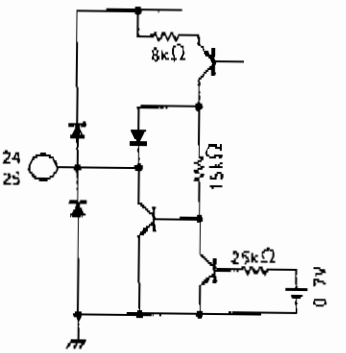
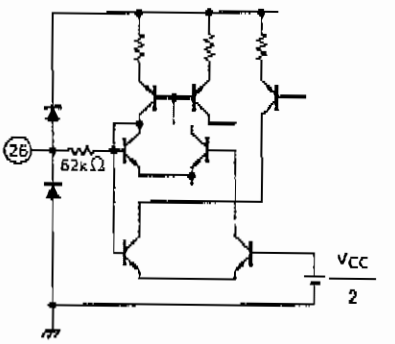
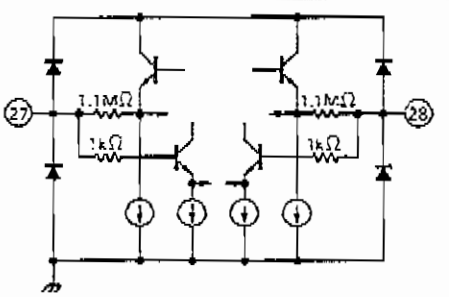
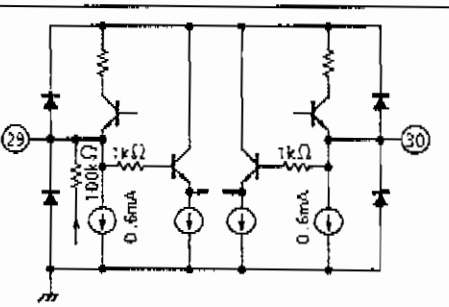
TERMINAL FUNCTION

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
1	Keyed Pulse Input	It clamps at the pulse peak and generates the reference level. The input impedance is 3kΩ. • If any keyed pulse input, Keyed pulse : low level sample state Keyed pulse : high level hold state • If no keyed pulse input, sample state at all time	
2 3	Detect Output	It outputs the detection output through a low-pass filter of 30MHz cut off frequency using an emitter follower.	
4 5	Video Amplifier Level Adjustment	It controls the level adjustment by varying the emitter resistance of a differential amplifier. If the resistance between pins 4 and 5 is reduced the output will be greater, however, since the output dynamic range is narrow the output level should be used in the range of lower than $0.7V_{p\text{-}p}$.	
6 7	Loop Filter	The output impedance is 200Ω. In the application circuit, $\omega \fallingdotseq 174MHz$ $\xi \fallingdotseq 0.81$	

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
8	GND1	It is the GND of VCO circuit blocks that are VCO (pins 9, 10, 12), loop filter (pins 6, 7), video amplifier (pins 4, 5) AFT system (pins 1, 23, 24, 25, 26, 27, 28) and S/H (pins 29, 30).	—
9 10	VCO Coil	It is the VCO using variations in internal impedance of diode for control voltage from mixer. Use a UJ characteristic for the capacitor of the external tank circuit to correct the internal temperature drift.	
12	VCO Temperature Compensate Bias	The VCO bias is composed of a synthesis of bias in proportion to V_{BE} and V_T of transistor, and this terminal generates a bias proportioned to the V_{BE}. If the external resistance reduced, the VCO sensitivity will rise.	
13	2nd AGC Adjustment	It changes the input level for a AGC detector. It adjusts by adding the direct current offset to pins 14 and 15. The variation width of about 8dB can be added. Internal bias is 2.5V.	

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
14 15	2nd AGC Filter	It generates the AGC voltage by filtering the 402.78MHz (479.5MHz) IF signal by means of an internal resistance and an external condenser. If applying the V_{CC} to pin 15, the AGC will be minimum gain and the VCO oscillates at free-running frequency.	
16	1st AGC Slice Adjustment	It sets the input level threshold for generating the control signal to lower gain from the IC to the 2nd converter of front stage when excessive input. Even if the 2nd AGC adjustment varies, the 1st AGC adjustment point hardly changes. The internal bias is 2.5V.	
17	1st AGC Filter	It outputs by comparating with the AGC and 1st AGC slice level adjustment voltages. This comparator is constructed by the active load type high gain amplifier and determines its response by a capacitor connected to this terminal.	
18	1st AGC Control	It outputs the control voltage using an emitter follower (active low level). The internal current sink has only 25μA.	

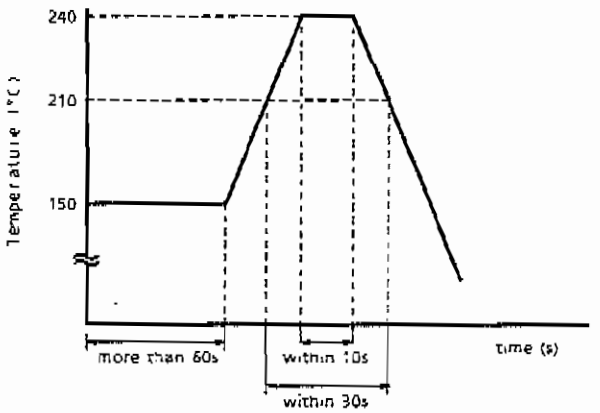
PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
19	Signal Level Out	It outputs the AGC voltage by doing logarithm <-> linear conversion. In the TA8804F the level detection can be carried out even after the 1st AGC is effective and input is reduced using the 1st AGC output.	
20 22	2nd IF In	The IF amplifier constructed by the 3-step series connection of variable gm type gain control, of which the maximum gain is 47dB and minimum gain −8dB. In order to prevent a sneak of radio frequency all the circuits are balance-connected. Therefore, the differential combination is also desirable for the IC input. The internal bias is 2.0V and input impedance 1kΩ.	
23	AFT Output (Analog)	It outputs by integrating the detection output by means of pin 27 and 28 filters, doing center adjustment and multiplying about five times as much.	

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
24 25	AFT Output (Digital)	It outputs by converting the analog AFT output to binary with a comparator. In the case of center detection, the each output will be high level. The width of dead gone is determined by the internal threshold and VCO sensitivity, that cannot be adjusted externally.	
26	AFT Center Adjustment	It moves the AFT center frequency in the width of 10MHz and absorbs the center gap caused by dispersion of each AFT circuit.	
27 28	AFT Filter	It constructs a filter whose cut off frequency is less than 1Hz (capacitor : 0.7Hz at 0.1μF) with an internal 1.1MΩ resistance and external condenser.	
29 30	Hold Capacitor	Sample and hold by charge / discharging the condenser using the switching signal regenerated by keyed pulse.	

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	$V_{CC\ MAX}$	6.0	V
Power Dissipation	$P_{D\ MAX}$	1000	mW
Operation Temperature	T_{opr}	−20~75	°C
Storage Temperature	T_{stg}	−55~150	°C
Lead Temperature	—	260°C, 10s	

Recommended assembly method : Recommended temperature profile of reflow soldering of far and medium infrared rays



RECOMMENDED POWER SUPPLY VOLTAGE

PIN No.	PIN NAME	MIN.	TYP.	MAX.	UNIT
11	V_{CC}	4.5	5.0	5.5	V

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (Unless otherwise specified, V_{CC} = 5.0V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current		I_{CC}	1	—	55	80	105	mA
Terminal Voltage	Pin 1	V_1	1	—	2.0	2.5	3.0	V
	Pin 2	V_2		—	1.9	2.4	2.9	
	Pin 3	V_3		—	1.9	2.4	2.9	
	Pin 4	V_4		—	0.8	1.3	1.8	
	Pin 5	V_5		—	0.8	1.3	1.8	
	Pin 6	V_6		—	1.7	2.1	2.5	
	Pin 7	V_7		—	1.7	2.1	2.5	
	Pin 9	V_9		—	2.4	2.8	3.2	
	Pin 10	V_{10}		—	2.4	2.8	3.2	
	Pin 12	V_{12}		—	0.4	0.7	1.0	
	Pin 13	V_{13}		—	2.3	2.5	2.7	
	Pin 14	V_{14}		—	—	3.6	—	
	Pin 15	V_{15}		—	—	3.6	—	
	Pin 16	V_{16}		—	2.1	2.5	2.9	
	Pin 18	V_{18h}		Pin 17 : 1kΩ-GND	—	1.0	1.3	
		V_{18l}		Pin 17 : V_{CC}	3.9	4.3	4.7	
	Pin 20	V_{20}		—	1.5	2.0	2.5	
	Pin 22	V_{22}		—	1.5	2.0	2.5	
	Pin 27	V_{27}		—	—	2.3	2.8	
	Pin 28	V_{28}		—	—	2.3	2.8	
	Pin 29	V_{29}		—	1.8	2.3	2.8	
	Pin 30	V_{30}		—	1.8	2.3	2.8	
Pin 2, 3 Acceptable Output Current		I_2, I_3	1	—	−1.0	—	6.0	mA
1'st AGC Output Current		I_{18}	1	—	−0.02	—	6.0	mA

AC CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
IF Input Frequency Range	f_{in}	—	—	350	400	550	MHz
IF Input Level Range	v_{in}	—	—	−60	—	−10	dBmW (50Ω)
1st AGC Shoulder Level Range	AGC_{MAX}	2	(Note 1)	—	−20	−10	dBmW (50Ω)
1st AGC Control Sensitivity	ΔAGC	2	(Note 2)	1.0	3.5	6.0	V/dB
Signal Level Sensitivity	ΔV/Δv	2	(Note 3)	10	35	60	mV/dB
VCO Conversion Sensitivity	β	2	Converting to output rate Pin 4, 5 : open / (Note 4)	—	110	130	MHz/V
VCO Temperature Drift	Δf_{Ta}	2	Ta = −10~65°C / (Note 5)	—	±1.0	±2.5	MHz
PLL Lock Range	f_L	2	(Note 6)	±25	±30	—	MHz
PLL Capture Range	fca	2	(Note 6)	±25	±30	—	MHz
Demodulation Output Level	V_{out}	2	$\Delta f = 10MHz_{p-p}$ / (Note 7)	0.15	0.26	0.40	V_{p-p}
Video Amplifier Variable Width	$V_{outS}/5$	2	Pin 4, 5 : short, 5kΩ / (Note 8)	10	14	—	dB
Demodulation Output Amplitude Frequency Characteristics 1	V_{outA1}	2	f = 0.2~4MHz / (Note 9)	—	—	±0.5	dB
Demodulation Output Amplitude Frequency Characteristics 2	V_{outA2}	2	f = 4~9MHz / (Note 9)	—	—	±2	dB
Group Delay Characteristics 1	τpd1	2	f = 0.2~4MHz / (Note 9)	—	—	±10	ns
Group Delay Characteristics 2	τpd2	2	f = 4~9MHz / (Note 9)	—	—	±40	ns
AFT Sensitivity	Δf/ΔV	2	(Note 12)	2.4	3.2	4.0	MHz/V
S/H Sample Speed	Δf_{spl}	2	Converting to input frequency rate / (Note 10)	0.1	0.2	—	MHz/μs
Keyed AFT Input Range	V_1	2	—	0.35	0.5	0.65	V_{p-p}
Keyed AFT Input Frequency	T_1	2	(Note 11)	8.0	16.7	50	ms
AFT Width of Dead Zone	V_{DEAD}	2	(Note 13)	250	340	400	kHz
Digital AFT Voltage Low Level	V_{20L}	2	(Note 13)	—	0.3	0.5	V
DG	DG	application circuit	APL 90% / (Note 14)	—	±2.0	±5.0	%

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DP	DP	application circuit	APL 90% / (Note 14)	—	±2.0	±5.0	°
Inter-Modulation 2	IM2	application circuit	2.15MHz beat level / (Note 15)	40	45	—	dB
Inter-Modulation 3	IM3	application circuit	1.43MHz beat level / (Note 15)	40	50	—	dB
Video Output S/N	S/N_{SAT}	application circuit	C/N = ∞	48	51	—	dB

MEASUREMENT CONDITION

(Note 1) 1st AGC Shoulder Level Range : AGC_{MAX}

F = 402.78MHz input level v_{in} = 0 to −40dBmW (50Ω) to pin 20. Measure v_{in} that pin 18 voltage is lower than 4V by opening pin 16 and raising v_{in}.

(Note 2) 1st AGC Control Sensitivity : ΔAGC

Input f = 402.78MHz v_{in} = 0~−40dBmW (50Ω) to pin 20. Calculate v_{in} that pin 18 voltage is 4V / 1V (as v_{in1}, v_{in2}), using the equation below.

$\Delta AGC = -3/(v_{in1} - v_{in2})$ V/dB

(Note 3) Signal Level Sensitivity : ΔV/Δv

Measure each output voltage of pin 19 at v_{in} = −40, −60dBmW (50Ω)

$\Delta V/\Delta V = (V_{-60} - V_{-40})/20$ mV/dB

(Note 4) VCO Conversion Sensitivity : β

Input mainly f = 402.78MHz and sweep ±5MHz, v_{in} = −30dBmW (50Ω) to pin 20.
Calculate $\beta = 10/(Vdet_{+5} - Vdet_{-5})$ and multiply the gain portion (2.66) of video amplifier when outputting a direct current voltage to pin 3 at 407.78MHz, 397.78MHz as $Vdet_{+5}$ and $Vdet_{-5}$ each.

(Note 5) VCO Temperature Drift : Δf_{Ta}

Short pin 6 and 7, and connect pin 14 to GND.
Measure the VCO frequency at ambient temperature Ta = 25°C, −10°C +65°C and calculate how much changes from 25°C. (read out the VCO leakage output by spectrum analyzer.)

(Note 6) PLL Lock Range : f_L, Capture Range : fca

Measure the range that synchronizes with VCO by putting pin 20 input frequency away from the free-running frequency.

(Note 7) Demodulation Output Level : V_{out}

Input pin 20 f = 402.78MHz, f_m = 100kHz, Δf = 10MHz$_{p-p}$, v_{in} = −30dBmW (50Ω)
Open pin 4 and 5 and measure the output level of pin 3.

(Note 8) Video Amplifier Variable Width : V_{outS}, V_{out5}

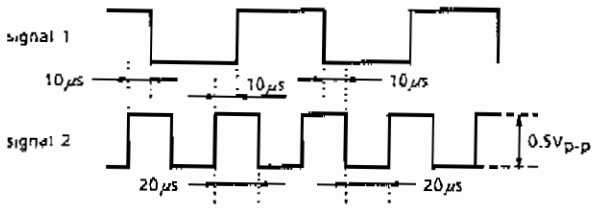
Input pin 20 f = 402.78MHz, f_m = 100kHz, Δf = 10MHz$_{p-p}$, v_{in} = −30dBmW (50Ω)
Measure the variation of video output by shorting between pin 4 and 5 and connecting a 5kΩ resistance.

(Note 9) Demodulation Output level Width, Group Delay Characteristics : V_{outA}, τpd

Input pin 20 f = 402.78MHz, f_m = 100kHz, 60Hz to 4MHz to 9MHz, Δf = 5MHz$_{p-p}$, v_{in} = −30dBmW (50Ω)
Compare to the value at 100kHz by opening pin 4 and 5, and measuring the output level and group delay of pin 3.

(Note 10) S/H Sample Speed : Δf_{spl}

Input the signal 1 below for a modulation signal. Input the signal 2 below to pin 1. Observe the differential voltage waveform between pin 29 and 30, and measure the slew rate in the sampling period.



(Note 11) Keyed Pulse Allowable Period : T_1

Input the signal below to pin 1 and open pin 27 and 28. Observe the pin 23 output and change f so as to be 2.5V voltage.

Measure the frequency range in which a 2kHz sine wave does not output to pin 23, by changing the signal 3 period.
If the sample-hold circuit malfunctions, the 2kHz sine wave will be outputted from pin 23.

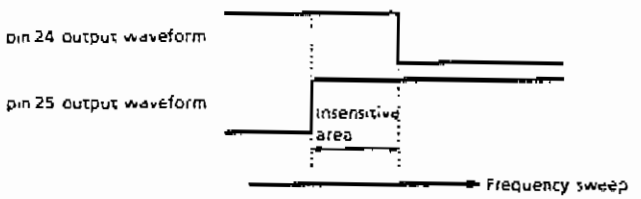
(Note 12) AFT Sensitivity : $\Delta f / \Delta V_{23}$

Input pin 20 f = 402.78MHz ± 1MHz, v_{in} = −30dBmW (50Ω)
Adjust f so that pin 23 output will be 2.5V. By moving f up. and down, calculate each frequency as f_H, f_L when pin 23 voltage varies 0.5V using the following equation.

$\Delta f / \Delta V_{23} = f_H - f_L$ (MHz / V)

(Note 13) AFT Digital Output Width of Blind Sector : f_{DEAD}

Input pin 20 f = 402.78MHz ± 5MHz, v_{in} = −30dBmW (50Ω)
Measure the input frequency range in which both pin 24 and 25 become high level, by sweeping f.



(Note 14) DG, DP

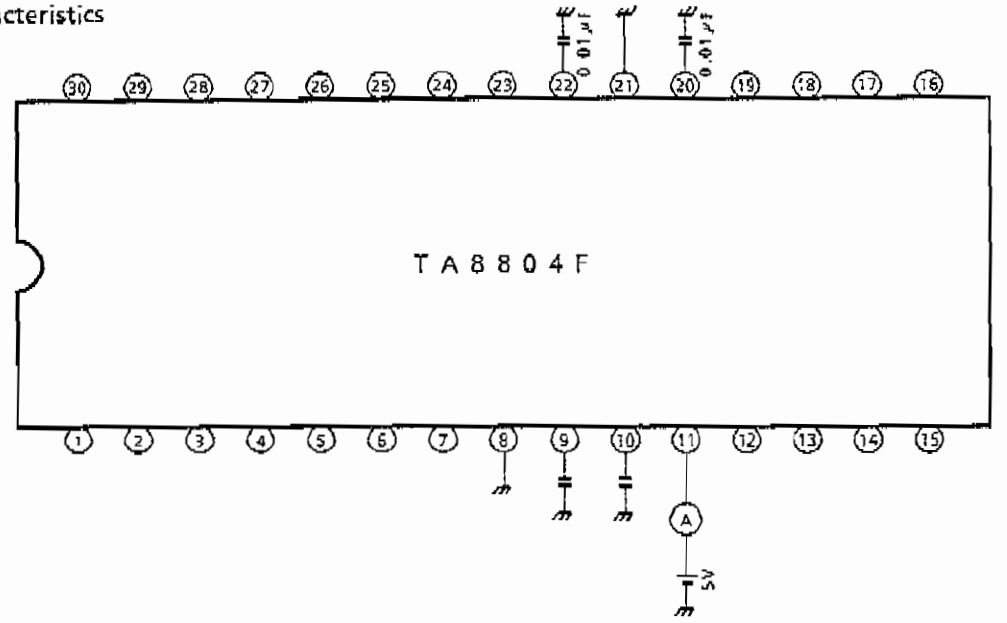
Input pin 20 f = 402.78MHz ± 5MHz, v_{in} = −30dBmW (50Ω), $\Delta f = 17MHz_{p-p}$, Gray level video signal (APL : 10~90%)··· Pre-emphasis-on

(Note 15) IM2, IM3

Input pin 20 f = 402.78MHz ± 5MHz, v_{in} = −30dBmW (50Ω), $\Delta f = 17MHz_{p-p}$. Color subcarrier (3.579MHz), Sound subcarrier (5.7272MHz) ···
Observe the frequency component outputting to the screen output pin (pin 3) through the video gate of a video noise meter by spectrum analyzer, and measure the level difference between 3.579MHz component and 2.15MHz, 1.43MHz components.

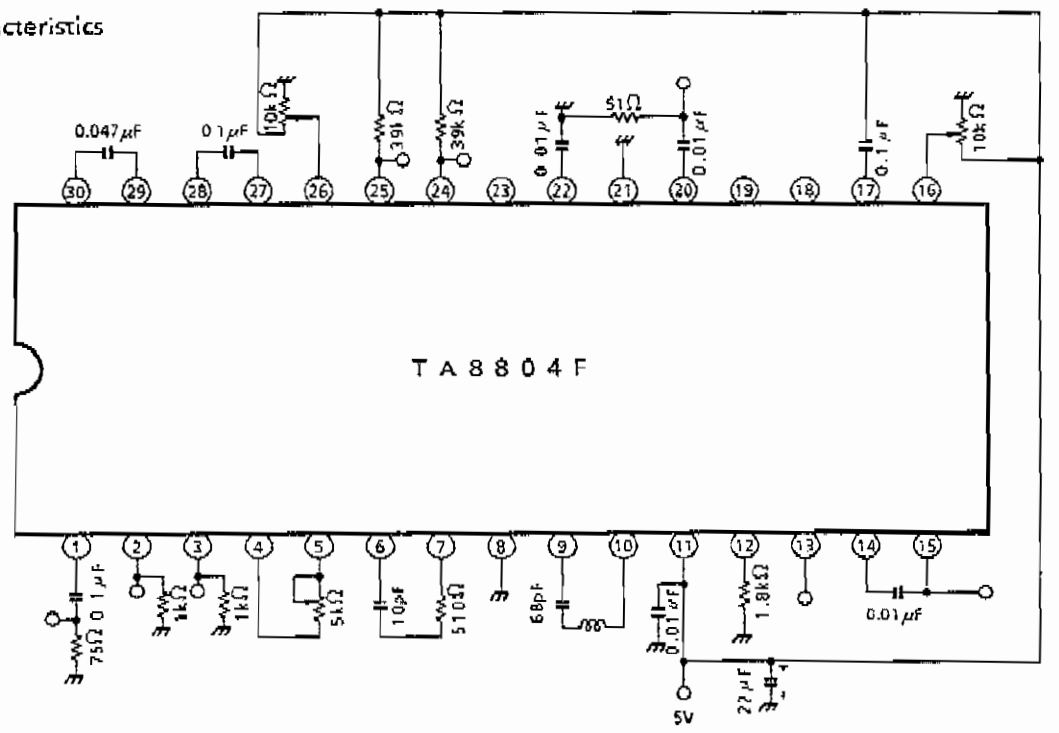
TEST CIRCUIT 1

DC characteristics



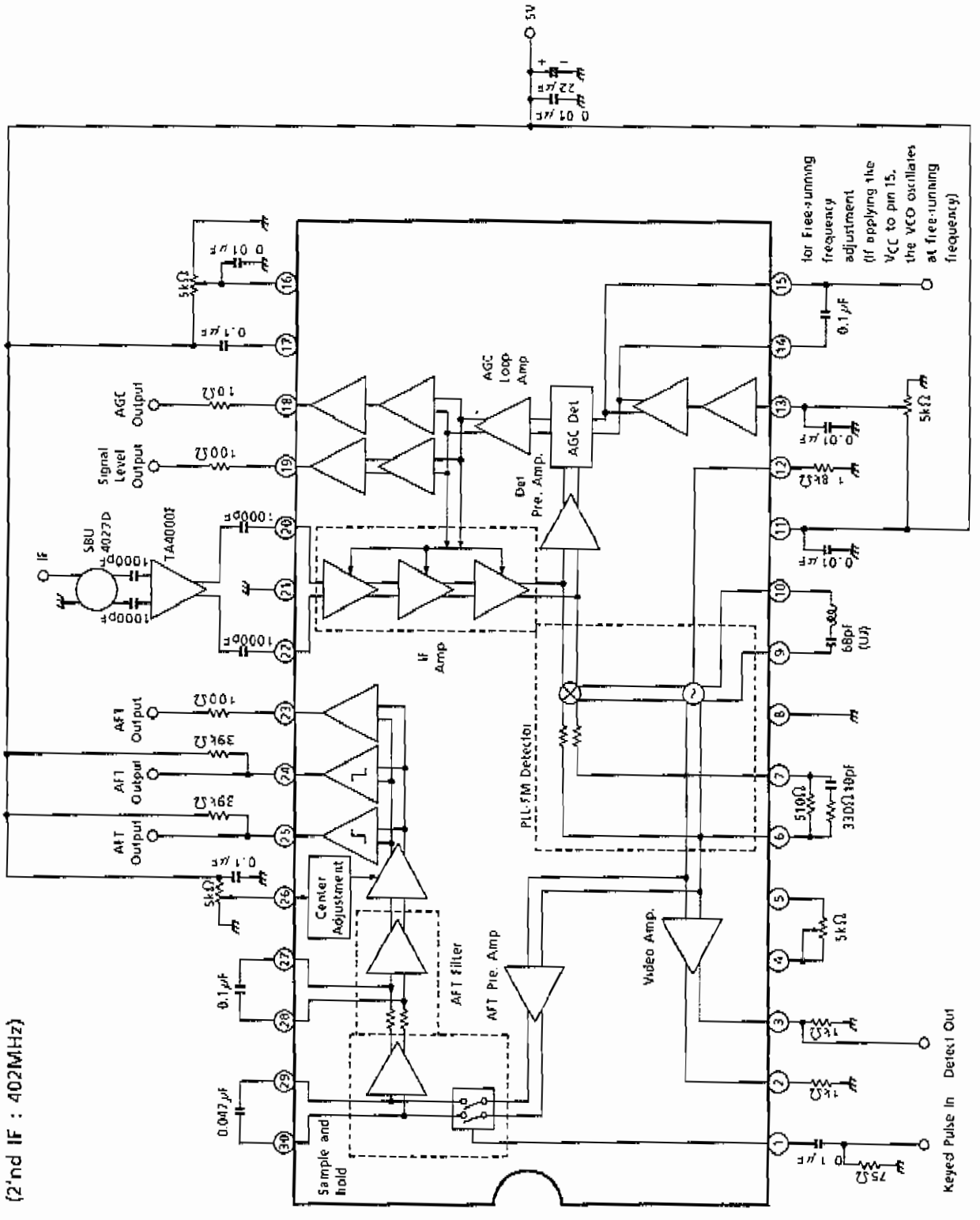
TEST CIRCUIT 2

AC characteristics



APPLICATION CIRCUIT

(2'nd IF : 402MHz)

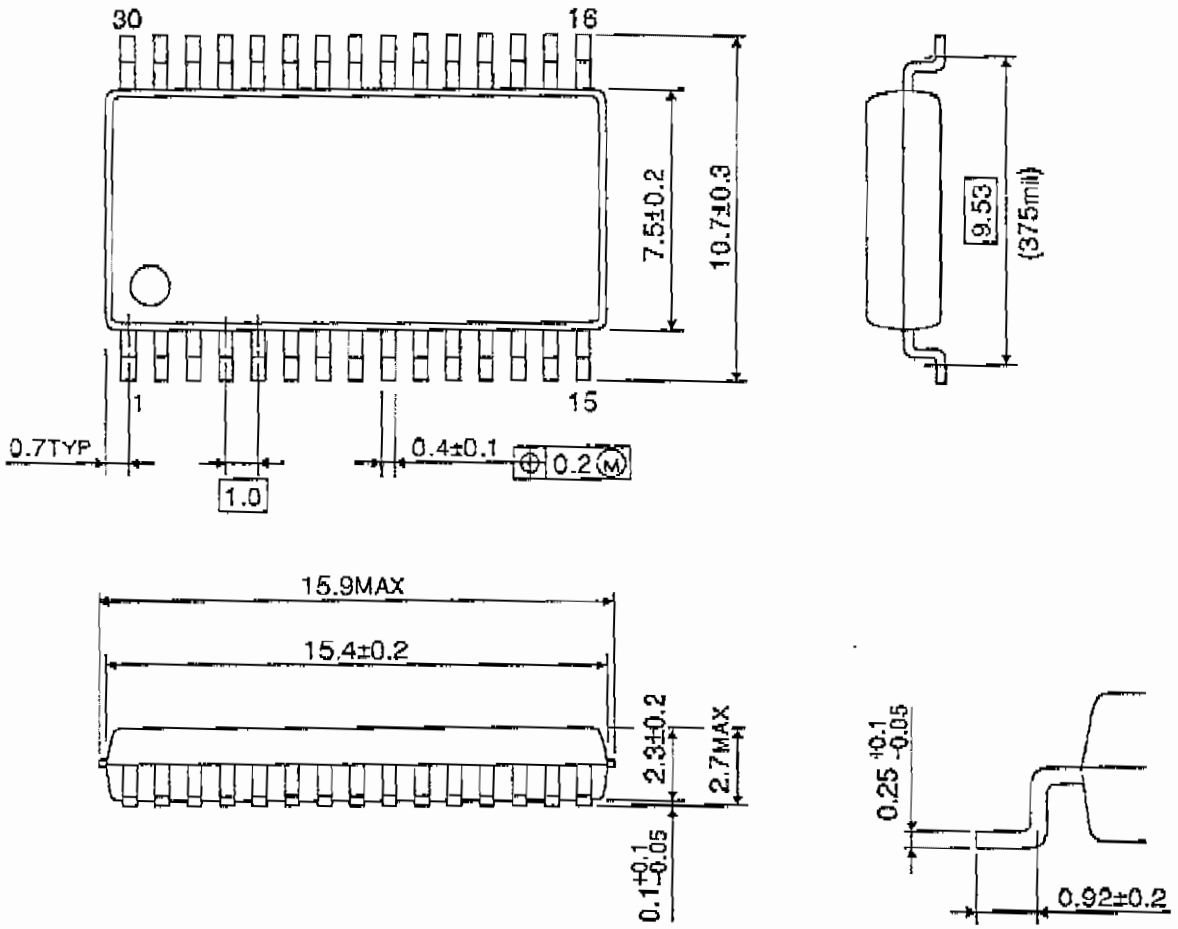


TA8804F – 15

OUTLINE DRAWING

SSOP30-P-375

Unit : mm



Weight : 0.63g (Typ.)

- **Adjustable Gain to 400 Typ**
- **No Frequency Compensation Required**
- **Low Noise . . . 3 μV Typ V_n**

description

This device is a monolithic two-stage video amplifier with differential inputs and differential outputs. It features internal series-shunt feedback that provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

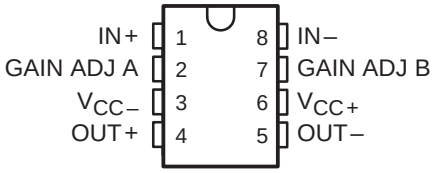
The differential gain is typically 400 when the gain adjust pins are connected together, or amplification may be adjusted for near 0 to 400 by the use of a single external resistor connected between the gain adjustment pins A and B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disk-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general-purpose video and pulse amplifiers.

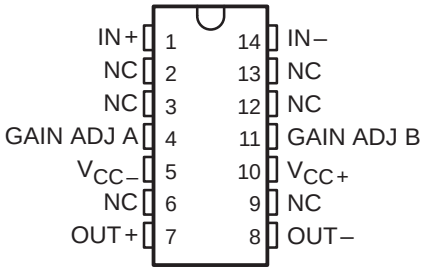
The device achieves low equivalent noise voltage through special processing and a new circuit layout incorporating input transistors with low base resistance.

The TL592B is characterized for operation from 0°C to 70°C.

D8† OR P PACKAGE
(TOP VIEW)

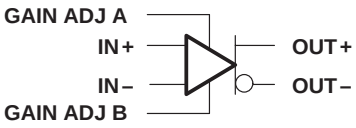


D14† OR N PACKAGE
(TOP VIEW)

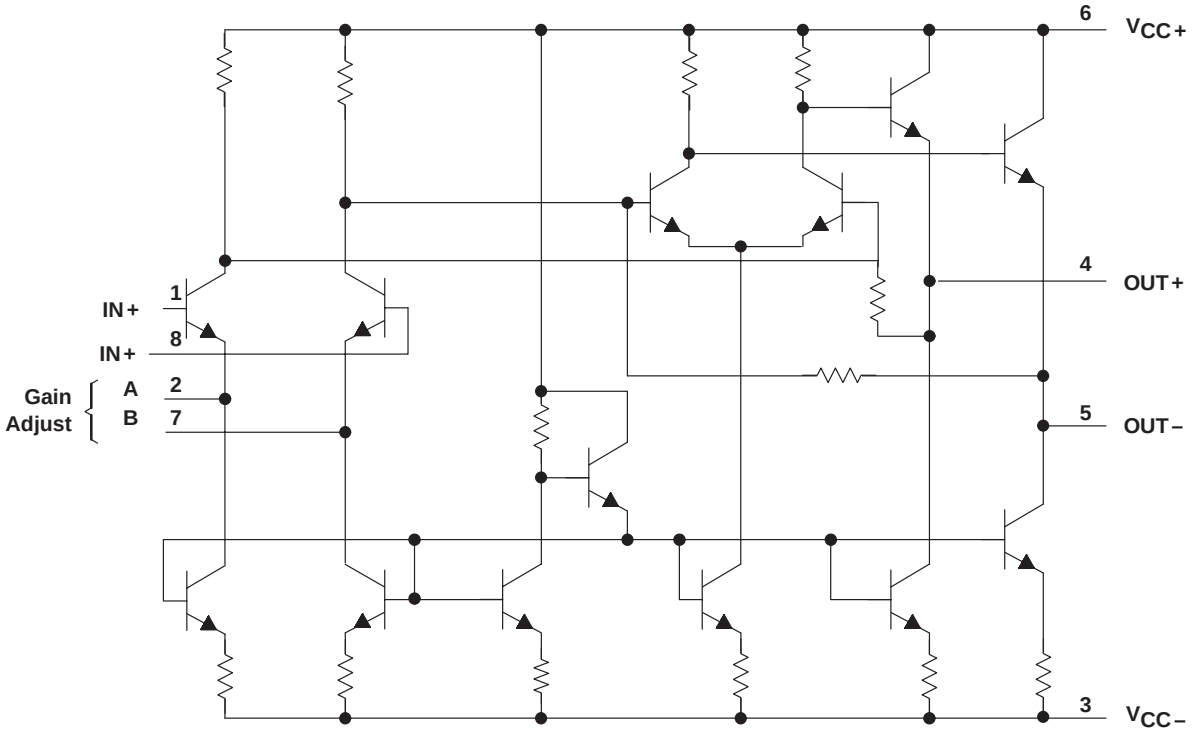


† D8 and D14 are the codes to differentiate the 8-pin and 14-pin versions, respectively.

symbol



schematic



Pin numbers are for D8 and P packages.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 8 V
Supply voltage, V_{CC-} . . . . . –8 V
Differential input voltage . . . . . ±5 V
Voltage range, any input . . . . . V_{CC+} to V_{CC-}
Output current . . . . . 10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values except differential input voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D8	530 mW	5.8 mW/°C	59°C	464 mW
D14	530 mW	N/A	N/A	530 mW
N	530 mW	N/A	N/A	530 mW
P	530 mW	N/A	N/A	530 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	3	6	8	V
Supply voltage, V_{CC-}	–3	–6	–8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±6 V, R_L = 2 kΩ (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		T_A	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V, R_{AB} = 0	R_L = 2 kΩ,	25°C	300	400	500	V/V
					0°C to 70°C	250		600	
A_{VD2}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V, R_{AB} = 1 kΩ	R_L = 2 kΩ,	25°C		13		V/V
BW	Bandwidth (–3 dB)	2	V_{OPP} = 1 V,	R_{AB} = 0	25°C		50		MHz
I_{IO}	Input offset current				25°C		0.4	5	µA
					0°C to 70°C			6	
I_{IB}	Input bias current				25°C		9	30	µA
					0°C to 70°C			40	
V_{ICR}	Common-mode input voltage range	3			25°C	±1			V
					0°C to 70°C	±1			
V_{OC}	Common-mode output voltage	1	R_L = ∞		25°C	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	R_{AB} = ∞,	25°C		0.35	0.75	V
					0°C to 70°C			1.5	
V_{OPP}	Peak-to-peak output voltage swing	1	R_L = 2 kΩ,	R_{AB} = 0	25°C	3	4		V
					0°C to 70°C	2.8			
r_i	Input resistance		V_{OD} = 1 V,	R_{AB} = 0	25°C		4		kΩ
					0°C to 70°C		3.6		
r_o	Output resistance				0°C to 70°C			30	Ω
C_i	Input capacitance				25°C		5		pF
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, R_{AB} = 0	f = 100 kHz	25°C	60	86		dB
				f = 5 MHz			60		
				f = 100 kHz	0°C to 70°C	50			
				f = 5 MHz			60		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ± 0.5 V, ΔV_{CC-} = ± 0.5 V,	R_{AB} = 0	25°C	50	70		dB
					0°C to 70°C	50			
V_n	Broadband equivalent input noise voltage	4	BW = 1 kHz to 10 MHz		25°C		3		µV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V		25°C		7.5		ns
t_r	Rise time	2	ΔV_O = 1 V		25°C		10.5		ns
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V,	V_O = 3 V		3	4		mA
I_{CC}	Supply current		No load,	No signal	25°C		18	24	mA
					0°C to 70°C			27	

† R_{AB} is the gain-adjustment resistor connected between gain-adjust pins A and B. If not specified for a particular parameter, its value is irrelevant to that parameter.

PARAMETER MEASUREMENT INFORMATION

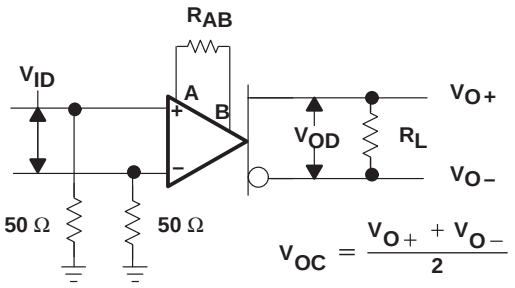


Figure 1

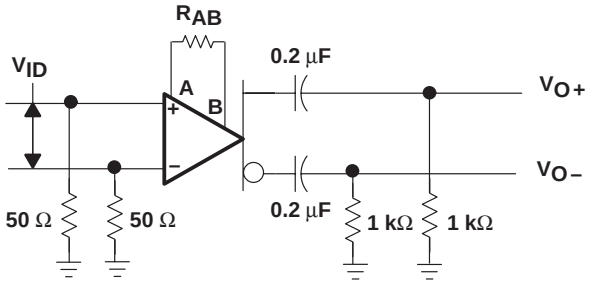


Figure 2

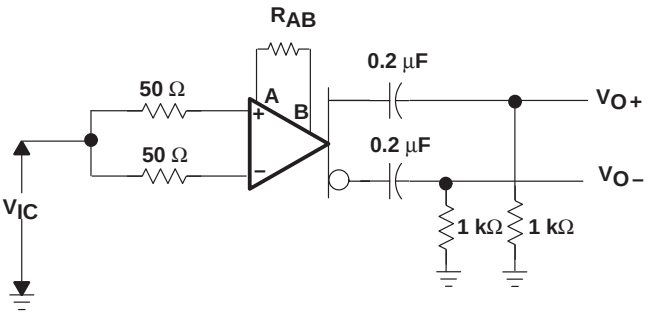


Figure 3

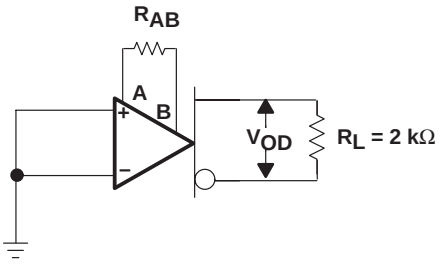


Figure 4

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

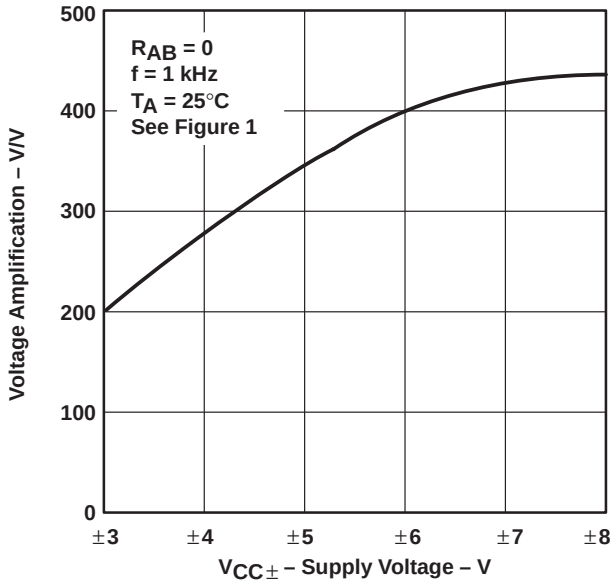


Figure 5

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs GAIN-ADJUSTMENT RESISTANCE

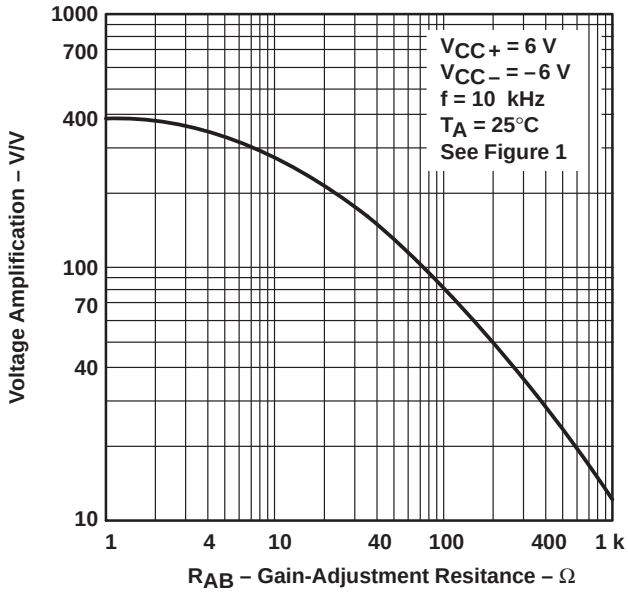


Figure 6

SUPPLY CURRENT vs SUPPLY VOLTAGE

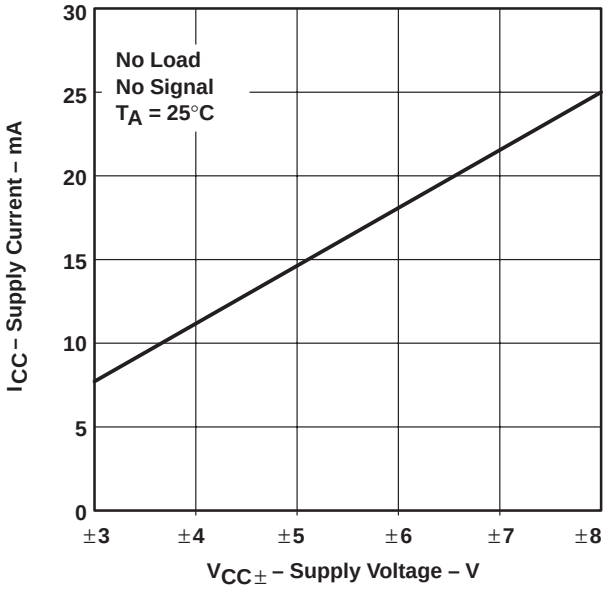


Figure 7

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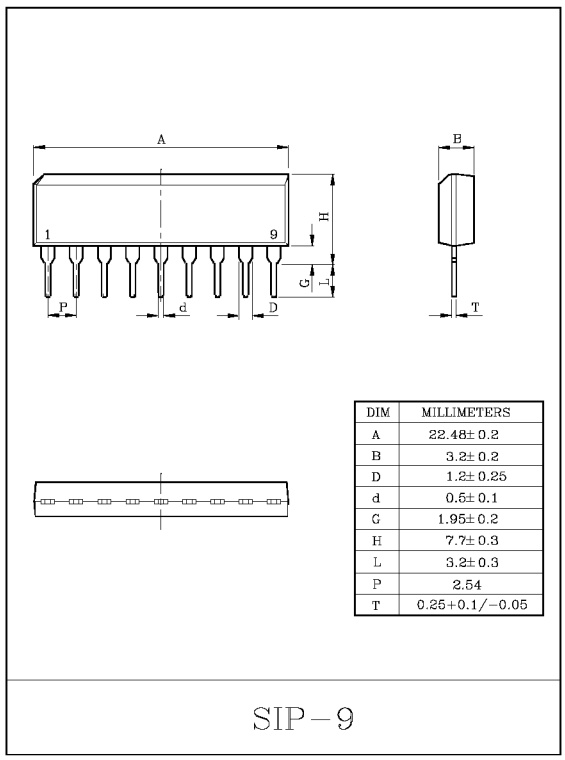
FM IF SYSTEM IC

- 3 Stage Differential IF Amplifier.
- Differential Peak Detector.
- Muting Circuit.
- High Recovered Output Voltage : V_{OD}=500mV_{rms}(Typ.).
- Low Distortion : THD=0.1% (Typ.).
- Wide Operating Supply Voltage Range :V_{CC}=8~15V(Typ.).
- Signal Meter Drive Voltage : V_3=4V(Typ.)
- Variable Muting Point.
- Muting Off at Open Terminal.
- Simplified Single Coil Tuning.
- Very Few External Parts.



DIM	MILLIMETERS
A	22.48±0.2
B	3.2±0.2
D	1.2±0.25
d	0.5±0.1
G	1.95±0.2
H	7.7±0.3
L	3.2±0.3
P	2.54
T	0.25+0.1/−0.05

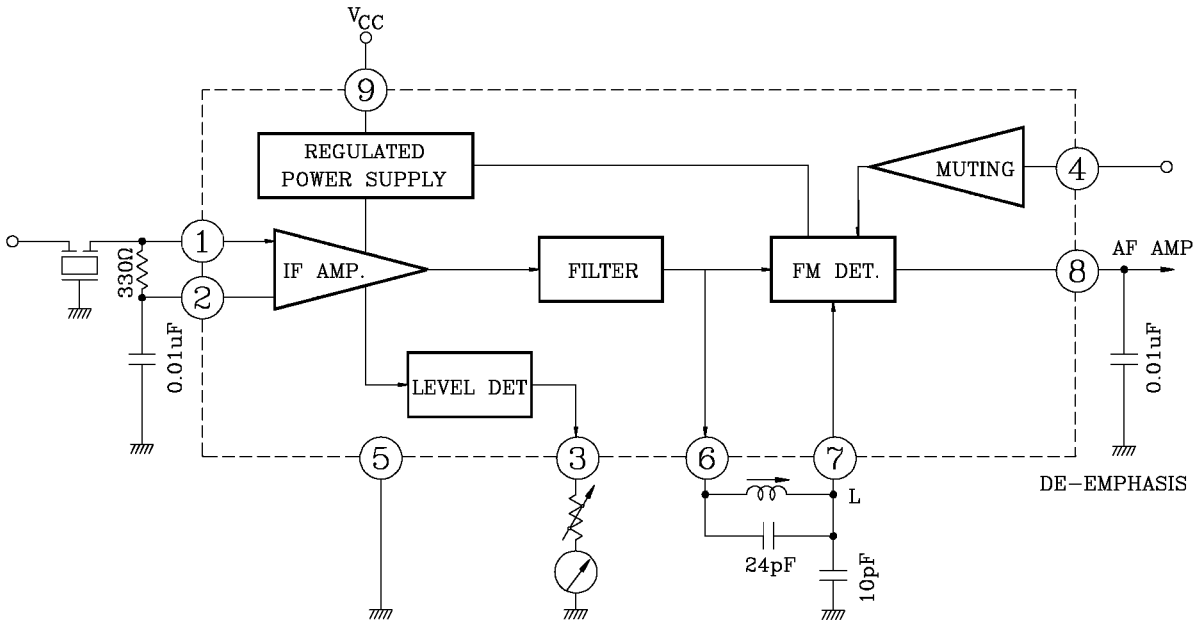
SIP-9

MAXIMUM RATINGS (Ta=25℃)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	15	V
Input Voltage	V_{IN}	0.7	V
Power Dissipation (Note)	P_D	750	mW
Operating Temperature	T_{opr}	-25~75	℃
Storage Temperature	T_{stg}	-55~150	℃

Note : Derated above Ta=25℃ in the proportion of 4mW/℃ for KIA6003S

BLOCK DIAGRAM



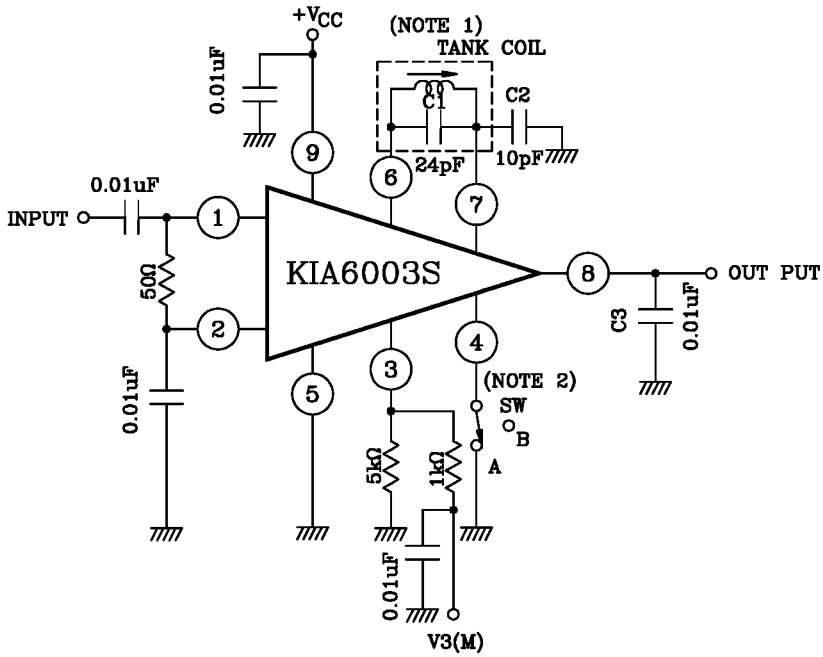
ELECTRICAL CHARACTERISTICS (V_{CC}=12V, f=10.7MHz, fm=400Hz, Ta=25℃)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current		I_{CC}	1	V_{IN}=0	10	14	18	mA
Input Limiting Voltage		$V_{IN(lim)}$	1	Δf=±75kHz dev. -3dB LIMITING	-	50	55	dBμV
AM Rejection Ratio		AMR	1	FM: Δf=±75kHz dev. AM: 30% Mod. V_{IN}=80dBμV	-	50	-	dB
Recovered Output Voltage		V_{OD}	1	Δf=±75kHz dev. V_{IN}=80dBμV	300	500	700	mV_{rms}
Total Harmonic Distortion		THD	1	Δf=±22.5kHz dev. V_{IN}=80dBμV	-	0.1	-	%
Signal to Noise Ratio		S/N	1	Δf=±75kHz V_{IN}=80dBμV	-	75	-	dB
Muting Attenuation		MA	1	Δf=±75kHz dev. V_{IN}=80dBμV, V_4=0	-	70	-	dB
Meter Drive Voltage		$V_{3(Max.)}$	1	V_{IN}=110dBμV	-	4	-	V
Input Impedance	Parallel Input Resistance	r_{ip}	-	f=10.7MHz, ①pin-GND	-	5	-	kΩ
	Parallel Input Capacitance	C_{ip}	-		-	4.5	-	pF
Output Impedance	Parallel Output Resistance	r_{op}	-	f=10.7MHz, ⑥pin-GND	-	1.3	-	kΩ
	Parallel Output Capacitance	C_{op}	-		-	4	-	pF
Output Resistance		R_O	-	f=400Hz, ⑧pin-GND	-	7.7	-	kΩ

Note : V_{OD} Rank (at Δf=±22.5kHz)

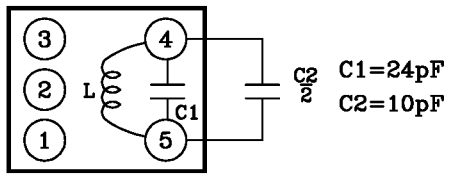
RANK	MIN.	MAX.	UNIT
B	90	150	mV_{rms}
C	130	210	mV_{rms}

TEST CIRCUIT 1



TANK COIL

WIRE	2 UEW 0.08mmø
TURNS	21
QU	130± 15%



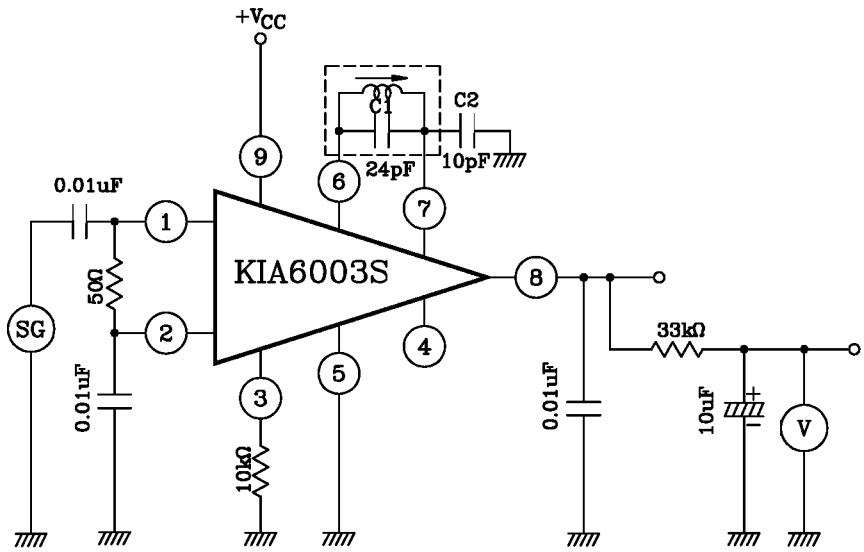
COVERED RESONANT FREQUENCY
10.7MHz± 250kHz

$$f_O = \left(\frac{1}{2\pi \sqrt{L\,(C_1 + \frac{C_2}{2})}} \right)$$

(Note 1) Tuning coil is adjusted to make recovered output voltage maximum at f=10.7MIIz.

(Note 2) SW : To A for muting attenuation test only.

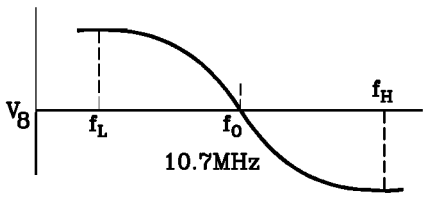
TEST CIRCUIT 2



f_L : LOWER PEAK FREQUENCY

f_O : CENTER FREQUENCY

f_H : UPPER FREQUENCY

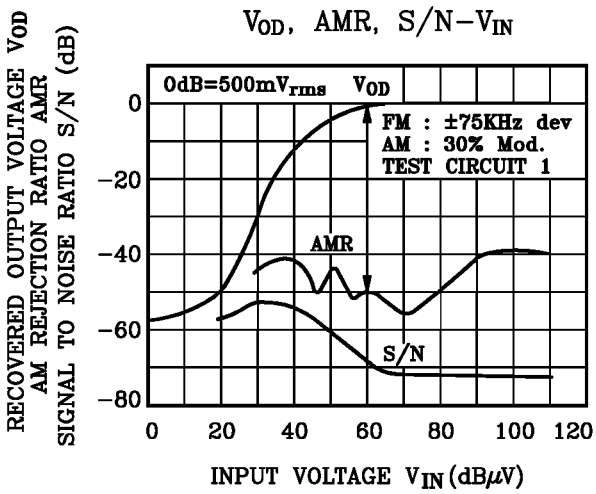


$$f_L = \frac{1}{2\pi \sqrt{L\,(C_1 + C_2)}}$$

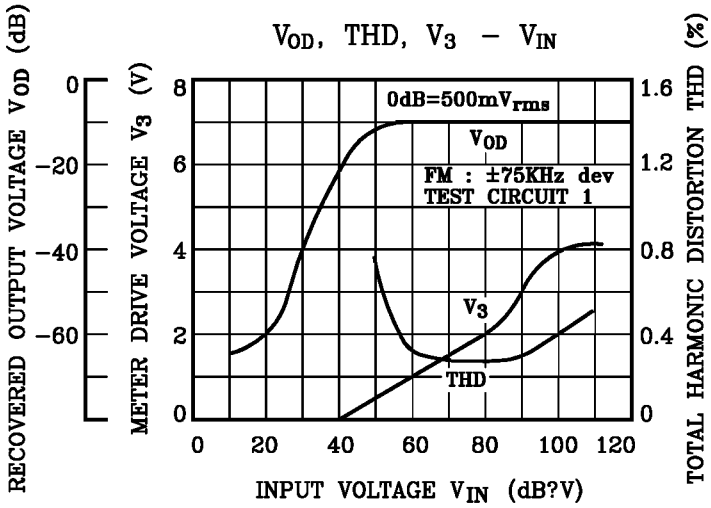
$$f_O = \frac{1}{2\pi \sqrt{L\,(C_1 + \frac{C_2}{2})}}$$

$$f_H = \frac{1}{2\pi \sqrt{LC_1}}$$

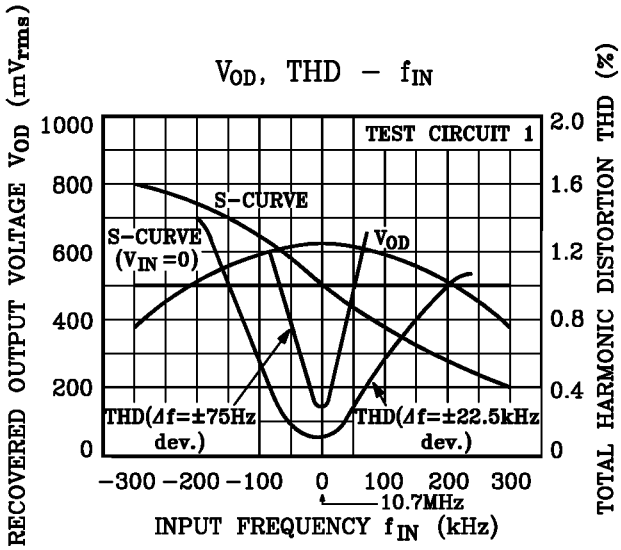
V_{OD}, AMR, S/N–V_{IN}



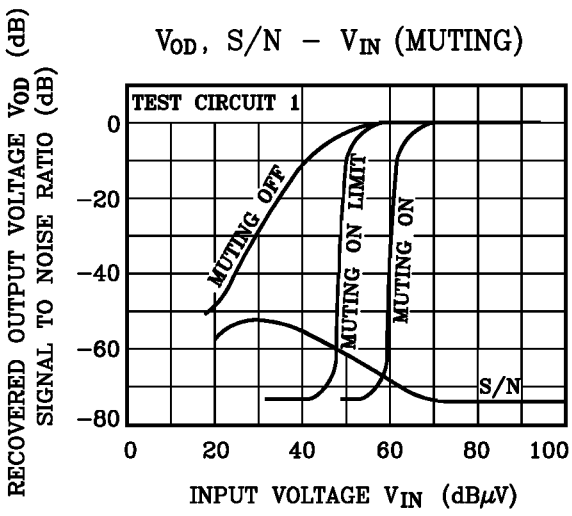
V_{OD}, THD, V_3 – V_{IN}



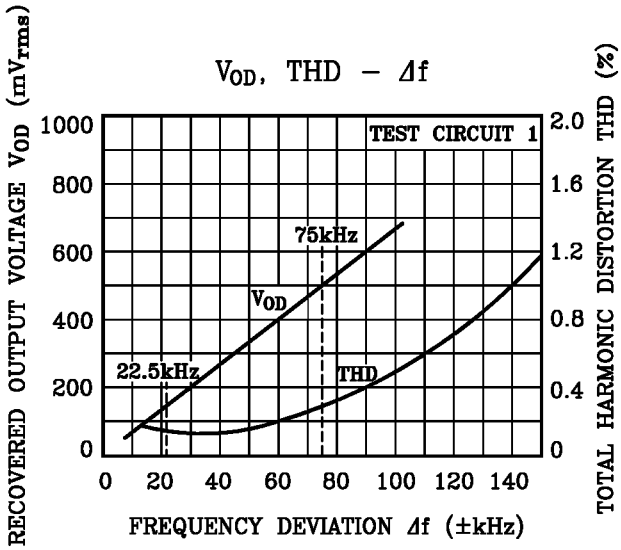
V_{OD}, THD – f_{IN}



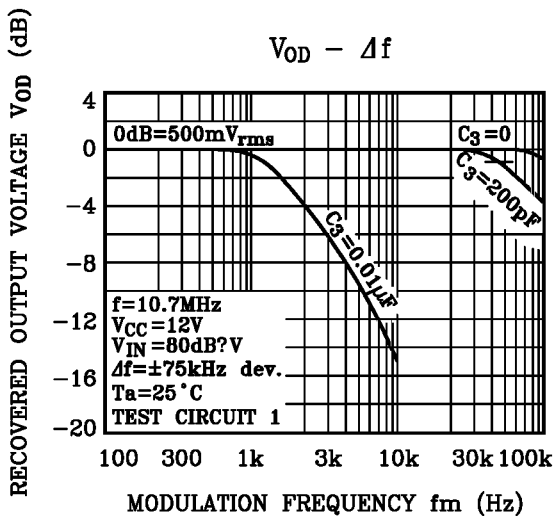
V_{OD}, S/N – V_{IN} (MUTING)



V_{OD}, THD – Δf



V_{OD} – Δf

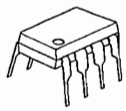


DC/DC CONVERTER CONTROL IC

■ GENERAL DESCRIPTION

The NJM2360 is a DC to DC converter control IC. Due to the internalization of a high current output switch, 1.5A switching operations are available. The NJM2360 is designed to be incorporated in step-up, step-down and inverting applications with a minimum number of external components. Output current is limited by an external resistor.

■ PACKAGE OUTLINE



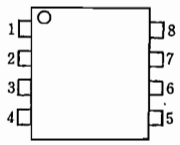
NJM2360D

NJM2360M

■ FEATURES

- Operating Voltage (2.5V~40V)
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5A
- Supply Voltage V^+ 2.5~40V
- Output Voltage V_{OR} 1.25~40V
- Oscillator Frequency f_{OSC} 100Hz~100kHz
- Package Outline DIP8, DMP8
- Bipolar Technology

■ PIN COFIGURATION

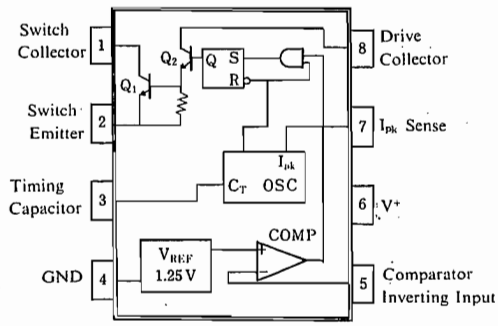


NJM2360D
NJM2360M

PIN FUNCTION

1. C_S
2. E_S
3. C_T
4. GND
5. INV_{IN}
6. V^+
7. S_I
8. C_D

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	40	V
Comparator Input Voltage Range	V_{IR}	$-0.3 \sim V^+$	V
Power Dissipation	P_D	(DIP8) 700 (DMP8) 600 (note 1)	mW mW
Switch Current	I_{SW}	1.5	A
Operating Temperature Range	T_{opr}	$-40 \sim +85$	℃
Storage Temperature Range	T_{stg}	$-40 \sim +125$	℃

(note 1) At on PC board

■ ELECTRICAL CHARACTERISTICS

- DC Characteristics (V^+=5V, Ta=25℃)

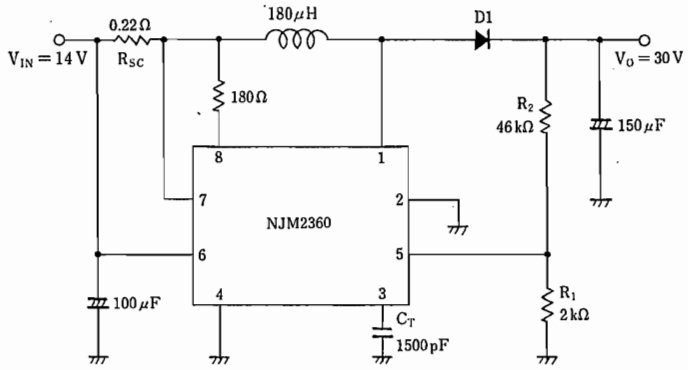
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	$5V \leqq V^+ \leqq 40V$, $C_T=0.001\mu F$ $S_I=V^+$, $INV_{IN} > V_{th}$, $E_S=GND$	—	2.4	3.5	mA
Oscillator						
Charge Current	I_{chg}	$5V \leqq V^+ \leqq 40V$	20	35	50	μA
Discharge Current	I_{dischg}	$5V \leqq V^+ \leqq 40V$	150	200	250	μA
Voltage Swing	V_{OSC}		—	0.5	—	V_{P-P}
Discharge to Charge Current Ratio	I_{dischg}/I_{chg}	$S_I=V^+$	—	6	—	—
Peak Current Sense Voltage	$V_{IPK(sense)}$	$I_{chg}=I_{dischg}$	250	300	350	mV
Output Switch (Note 2)						
Saturation Voltage 1	$V_{CE(sat)}1$	Darlington Connection ($C_S=C_D$) I_{SW}=1.0A	—	1.0	1.3	V
Saturation Voltage 2	$V_{CE(sat)}2$	I_{SW}=1.0A, $I_{C(driver)}$=50mA (Forced $\beta \fallingdotseq 20$)	—	0.5	0.7	V
DC Current Gain	h_{FE}	I_{SW}=1.0A, V_{CE}=5.0V	35	120	—	—
Collector Off−State Current	$I_{C(off)}$	V_{CE}=40V	—	10	—	nA
Comparator						
Threshold Voltage	V_{th}		1.18	1.25	1.32	V
Input Bias Current	I_{IB}	V_{IN}= 0V	—	40	400	nA

Note 2 : Output switch tests are performed under pulsed conditions to minimize power dissipation.

6

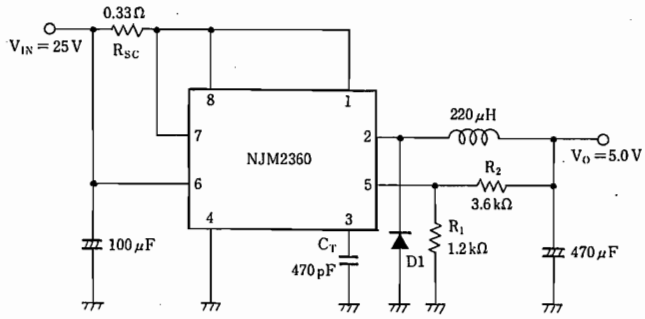
■ TYPICAL APPLICATIONS

1. Step-Up Converter



∗D1 : SBD(EK14)

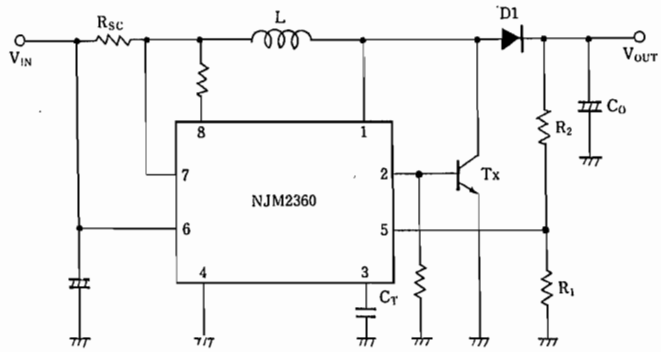
2. Step-Down Converter



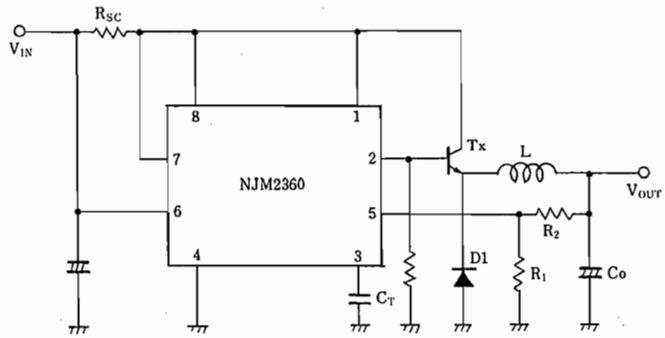
∗D1 : SBD(EK14)

■ TYPICAL APPLICATIONS

3. Step-Up Converter (High Current)



4. Step-Down Converter (High Current)



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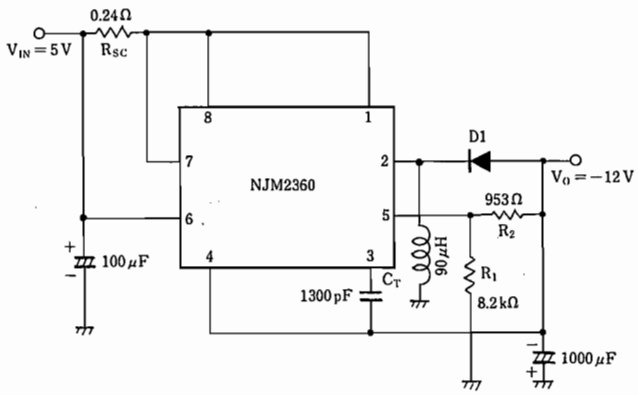
5. Inverting Converter



*D1 : SBD(EK14)

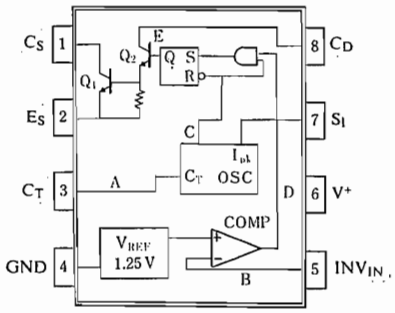


Fig.1 Block Diagram

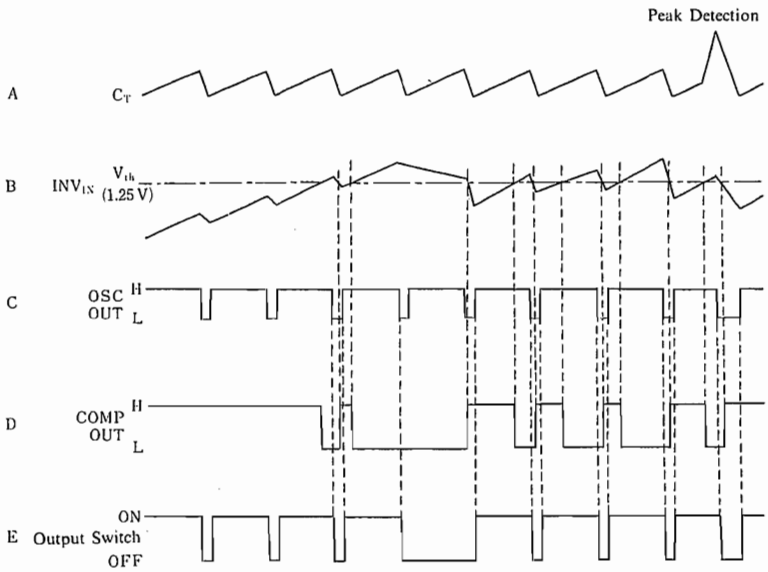
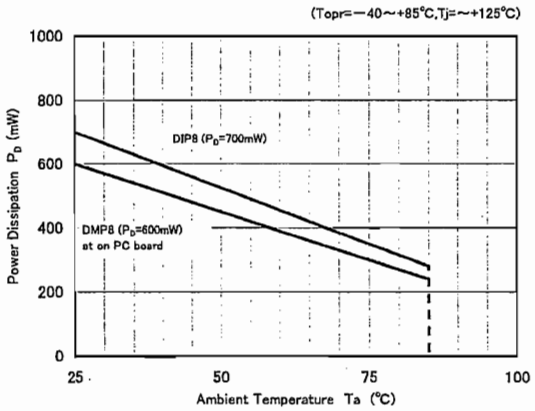


Fig. 2 Timing Chart

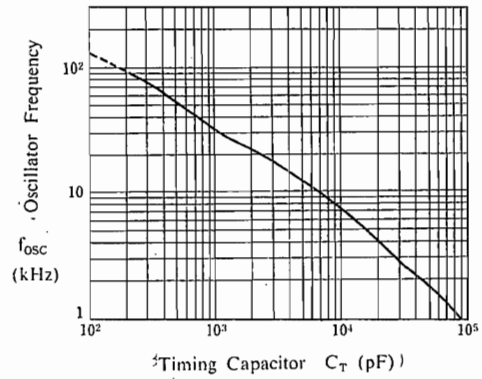
■ POWER DISSIPATION VS. TEMPERATURE



■ TYPICAL CHARACTERISTICS

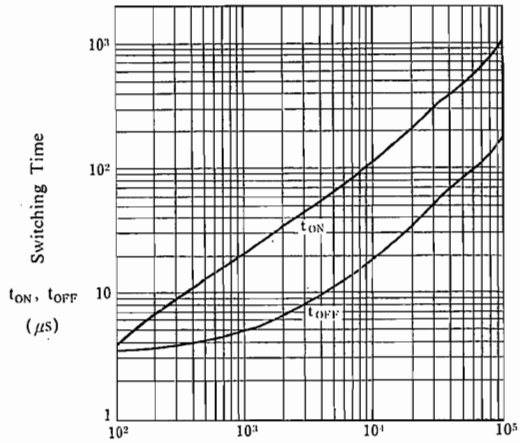
Oscillator Frequency vs. Timing Capacitor

(V_{IN} = 5 V, S_1 = V^+, Pin5 = GND, Ta = 25°C)



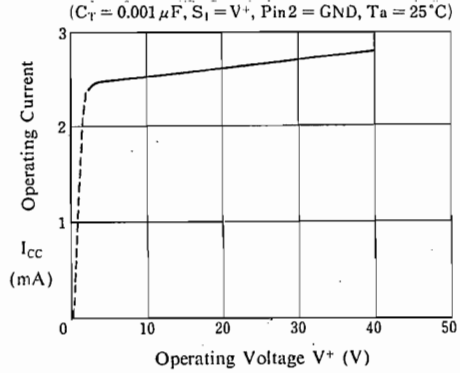
Switching Time vs. Timing Capacitor

(V_{IN} = 5 V, S_1 = V^+, Pin5 = GND, Ta = 25°C)



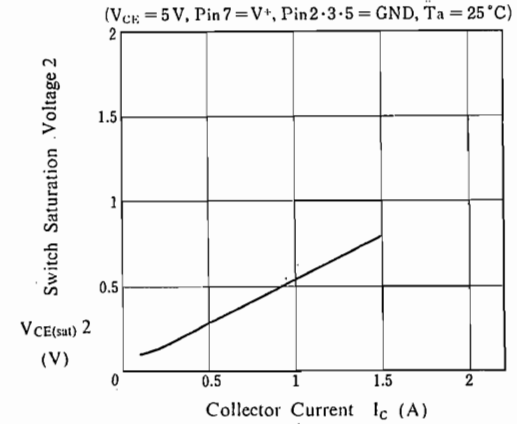
Operating Current vs. Operating Voltage

(C_T = 0.001 μF, S_1 = V^+, Pin2 = GND, Ta = 25°C)



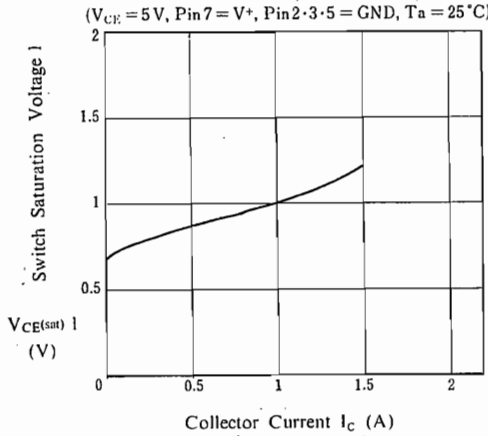
Switch Saturation Voltage 2 vs. Collector Current ($\beta \fallingdotseq 20$)

(V_{CE} = 5 V, Pin7 = V^+, Pin2·3·5 = GND, Ta = 25°C)



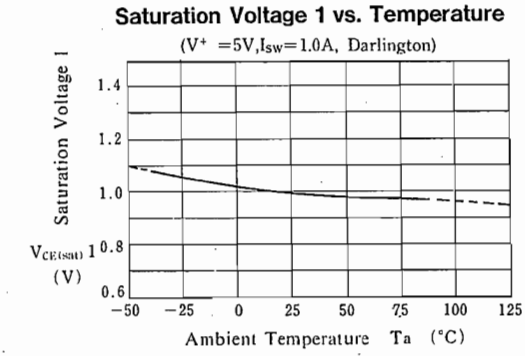
Switch Saturation Voltage 1 vs. Collector Current (Darlington)

(V_{CE} = 5 V, Pin7 = V^+, Pin2·3·5 = GND, Ta = 25°C)



Saturation Voltage 1 vs. Temperature

(V^+ = 5V, I_{SW} = 1.0A, Darlington)



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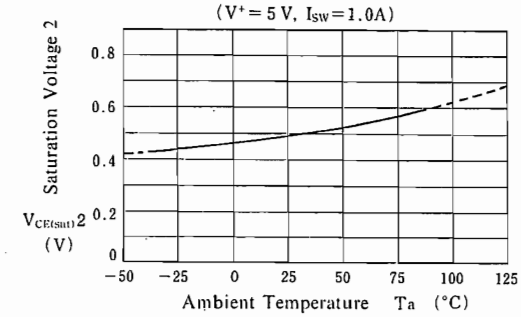
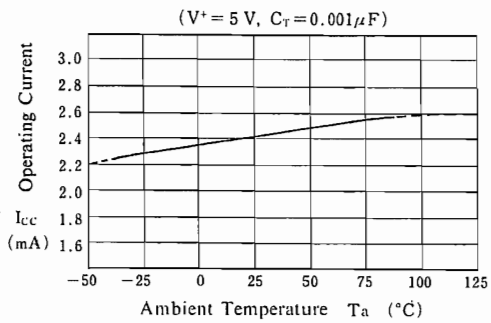
■ TYPICAL CHARACTERISTICS

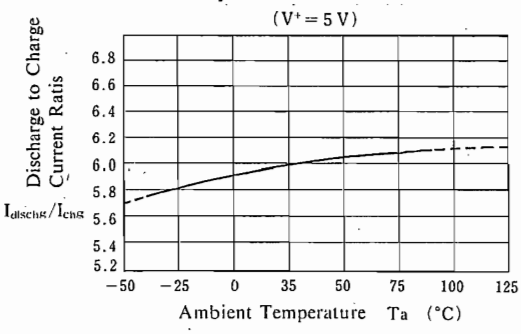
Saturation Voltage 2 vs. Temperature



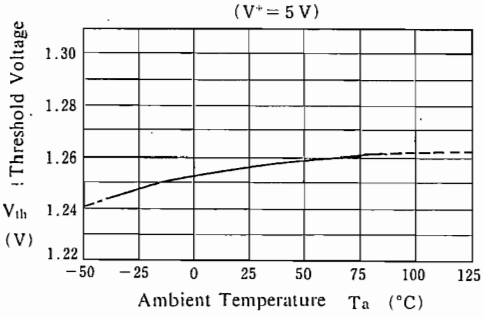
Operating Current vs. Temperature



Discharge to Charge Current Ratio vs. Temperature



Threshold Voltage vs. Temperature



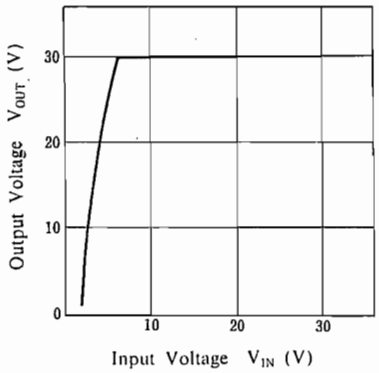
6

■ TYPICAL CHARACTERISTICS (Application)

1. Step-Up Converter

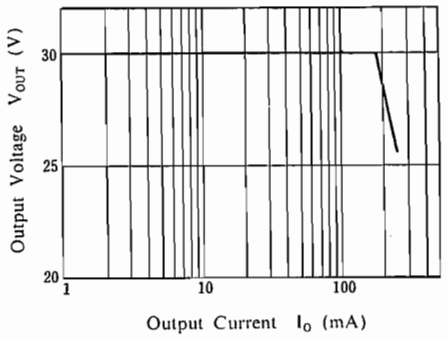
Output Voltage vs. Input Voltage

($V_O = 30\,V$, $I_O = 100\,mA$, $C_T = 1500\,pF$, $L = 180\,\mu H$, $Ta = 25°C$)



Output Voltage vs. Output Current

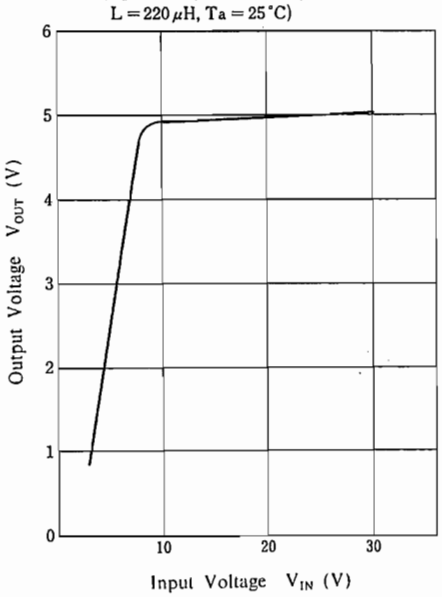
($V_{IN} = 14\,V$, $V_O = 30\,V$, $C_T = 1500\,pF$, $L = 180\,\mu H$, $Ta = 25°C$)



2. Step-Down Converter

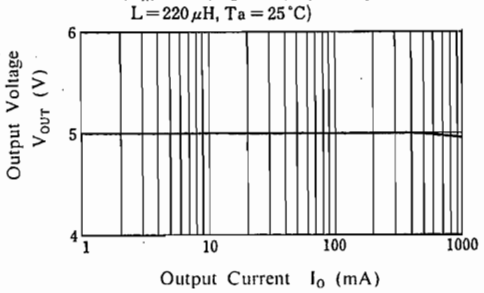
Output Voltage vs. Input Voltage

($V_O = 5\,V$, $I_O = 500\,mA$, $C_T = 470\,pF$, $L = 220\,\mu H$, $Ta = 25°C$)



Output Voltage vs. Output Current

($V_{IN} = 25\,V$, $V_O = 5\,V$, $C_T = 470\,pF$, $L = 220\,\mu H$, $Ta = 25°C$)



MEMO